TI world-wide sales offices

ALABAMA
Sahara Office Park Bldg., Suite 111
3313 Memorial Parkway, S.W.
Huntsville, Alabama 35801
205-881-4061

ARIZONA
United Bank Bldg., Suite 1702
3550 North Central Avenue
Phoenix, Arizona 85012
602-279-5531

CALIFORNIA
1800 North Argyle Ave.
Hollywood, California 90028
213-466-7251

5005 West Century Blvd., Suite 208
Inglewood, California 90301
213-673-3943

230 California Ave., Suite 201
Palo Alto, California 94306
415-326-6770

1505 East 17th St., Suite 201
Santa Ana, California 92701
714-547-6506

Balboa Towers Bldg., Suite 805
5252 Balboa Avenue
San Diego, California 92117
714-279-2622

COLORADO
2186 South Holly St., Suite 205
Denver, Colorado 80222
303-758-2151

CONNECTICUT
300 Amity Road
Woodbridge, Connecticut 06525
203-389-4521

FLORIDA
601 W. Oakland Park Blvd.
Fort Lauderdale, Florida 33311
305-566-3294

5400 Diplomat Circle
Diplomat Bldg., Suite 252
Orlando, Florida 32810
305-644-3535

300 Bldg. West, Suite 204
3151 Third Ave., North
St. Petersburg, Florida 33713
813-898-0807

ILLINOIS
Suite 205, Executive Towers
5901 N. Cicero Ave.
Chicago, Illinois 60646
312-286-1000

INDIANA
8539 Encanto Way
Ft. Wayne, Indiana 46805
219-485-1959

MASSACHUSETTS
60 Hickory Drive
Waltham, Mass. 02154
617-891-8450
Effective Oct. 30: 617-890-7400

MICHIGAN
Suite 706 West, Northland Towers Bldg.
15565 Northland Dr.
Southfield, Michigan 48075
313-352-5720

MINNESOTA
7615 Metro Blvd.
Suite 202, Analysis Inc., Bldg.
Edina, Minn. 55435
612-941-4384

NEW JERSEY
25 U.S. Highway #22
Springfield, New Jersey 07081
201-376-9400

NEW MEXICO
Suite 9, Marberry Plaza
6101 Marble Avenue, N.W.
Albuquerque, New Mexico 87110
505-265-8491

NEW YORK
P.O. Box 618, 112 Nanticoke Ave.
Endicott, New York 13760
607-785-9987

245 Newtown Road
Plainview, New York 11803
516-293-2560

167 Main Street
Fishkill, New York 12524
914-896-6793

6563 Ridings Rd.
Syracuse, New York 13206
315-463-9291

NORTH CAROLINA
4310 Starmount Dr.
Greensboro, N.C. 27410
919-299-9112

OHIO
23811 Chagrin Blvd., Suite 100
Cleveland, Ohio 44122
216-464-1192

Suite 205, Paul Welch Bldg.
3300 South Dixie Dr.
Dayton, Ohio 45439
513-298-7513

PENNSYLVANIA
275 Commerce Drive
Fort Washington, Pa. 19034
215-643-6450

TEXAS
MS366—P.O. Box 5012
Dallas, Texas 75222
214-238-6805

3939 Ann Arbor
Houston, Texas 77042
713-785-6906

WASHINGTON
5801 Sixth Ave. S.
Seattle, Washington 98108
206-762-4240

WASHINGTON, D.C.
1875 Connecticut Ave., N.W., Suite 913
Washington, D.C. 20009
202-234-9320

ARGENTINA
Texas Instruments Argentina S.A.I.C.F.

C.C. Box 2296—Correo Central
Buenos Aires, Argentina
744-1041

ASIA
Texas Instruments Asia Limited

5F Aoyama Tower Bldg.
24-15 Minami Aoyama Chome
Minato-ku, Tokyo 107, Japan
402-6171

Room 1502, Star House
Harbour Center, Kowloon
Hong Kong
K673139

AUSTRALIA
Texas Instruments Australia Ltd.

P.O. Box 63, 171-175 Philip Highway
Elizabeth, South Australia
55 29 14

Room 5, Rural Bank Bldg.
38 Railway Parade
Burwood N.S.W. Australia
74-1859

BRAZIL
Texas Instrumentos Electronicos
do Brasil Ltda.

Rua Cesario Alvim 770
Caixa Postal 30.103
Sao Paulo 6, Brasil
93-8278

CANADA
Texas Instruments Incorporated

2750 Pitfield Blvd.
St. Laurent 386
Quebec, Canada
514-332-3550

5F Caesar Avenue
Ottawa 12
Ontario, Canada
613-825-3716

280 Centre Str. East
Richmond Hill (Toronto)
Ontario, Canada
416-889-7373

DENMARK
Texas Instruments A/S

46D, Marielundvej
2730 Herlev, Denmark
91 74 00

FINLAND
Texas Instruments Finland OY

Fredrikinkatu 56, D 38
Helsinki 10, Finland
44 12 75

FRANCE
Texas Instruments France

379 Av de la Liberation
92 Clamart, France
644 55 30

30-31 Quai Rambaud
69 Lyon, France
42 78 50

3, Rue Lafayette
35 Rennes, France
30 56 85

20, Avenue Honore'Serres
31 Toulouse, France
62 82 85

GERMANY
Texas Instruments Deutschland GmbH

Arabellastrasse 4, Sternhaus/V
8000 Munchen 81, Germany
0811/91 10 61-9

Lazarettstr, 19
4300 Essen, Germany
2141/20916

Kuntzelstrasse 57
43 Essen, Germay
02141/86 10 6

Westendstrasse 52
6000 Frankfurt a.M., Germany
0611/72 64 41

Am Mittelfelde 169
3000 Hanover, Germany
0511/86 10 16

Im Kaisemer 5
7000 Stutgart 1, Germany
0711/22 38 20

ITALY
Texas Instruments Italia SpA

Viale Lunigiana 46
20125 Milano, Italy
688 31 41

Via Val di Chiana 56
50127 Firenze, Italy
512 36 10

Via Padre Semeria
00154 Roma, Italy
512 36 10

Via Barbaroux 2
10122 Torino, Italy
54 06 93

MEXICO
Texas Instruments de Mexico S.A.

Poniente 116 #489
Col. Industrial Vallejo
Mexico City, D.F., Mexico
567-92-00

NETHERLANDS
Texas Instruments Holland N.V.

Entrepot Gebouw-Kamer 223
P.O. Box 7603
Schiphol-Centrum
020-15 92 93

UNITED KINGDOM
Texas Instruments Limited

165 Bath Road
Slough, Buckinghamshire, England
Slough 33411

2259 Coventry Road
Sheldon, Birmingham 26, England
021-743-5293

24 Rutland Street
Edinburgh EH12AN, Scotland
031-229-1481

York House, 12 York Street
Manchester 2, England
061-236-7282

46 F. Nichols Road
Southampton, Hants, England
0703-27267

For Continuing Information on TI Integrated Circuits

This catalog provides technical descriptions and specifications on integrated circuits supplied by Texas Instruments. As the leading manufacturer of integrated circuits, TI is continually developing and introducing new products to the electronics industry.

So that we can register your name as a holder of this new IC catalog and to inform you of other catalogs as they become available, please complete and return the form provided below.

Texas Instruments Incorporated
Components Group, Market Communications Dept.
P. O. Box 5012, M. S. 84
Dallas, Texas 75222

☐ Please register my name as a recipient of *The Integrated Circuits Catalog for Design Engineers*.

☐ Please inform me of availability of other integrated circuit catalogs and supplements.

NAME _____

TITLE _____

FIRM _____

ADDRESS _____

CITY _____ STATE _____ ZIP _____

$4.95

The Integrated Circuits Catalog

for

Design Engineers

First Edition

TEXAS INSTRUMENTS
INCORPORATED

CC-401
10072-41-US

Printed in U.S.A.

IMPORTANT NOTICES

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TI cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

A

General Information

A

THE INTEGRATED CIRCUITS CATALOG

In this 1616-page data book, Texas Instruments is pleased to present important technical information on industry's broadest line of integrated circuits.

You'll find essential design information on TTL (including Standard 54/74, low-power, high-speed, and Schottky), Linear, MOS, ECL, Hybrid, and Radiation Hardened–plus Systems Interface circuits and line summaries of DTL, High-Noise-Immunity Logic and SNF/SNG.

The indexes are designed for ease in circuit selection with margin tabs to guide you quickly to general circuit catagories, and numerical and functional indexes to help you locate specific circuits. Selection and cross-reference guides for many circuits are presented to help you identify TI's nearest equivalent to competitive circuits.

High reliability of ICs is covered in a section devoted to the MACH IV Procurement Specification in accordance with MIL STD 883 – a program initiated by TI to ensure that quality and reliability are *built* into, not *tested* into integrated circuits.

In addition to the circuits included in this catalog, TI's extensive custom capability is structured to manufacture circuits to individual customers' specification. For more information on how TI can design, build, and test circuits tailored to your specific requirements, contact your TI field sales engineer.

Although this volume offers design and specification data only for integrated circuits, we provide a listing of all TI standard discrete semiconductors and components in the section immediately following the IC indexes. The discrete listing includes a breakout by classification and application of the popular *Preferred* line of TI semiconductors and components. Complete technical data for any of these Preferred Semiconductors and Components are available from your nearest TI field sales office, local authorized TI distributor, or by writing direct to: Marketing and Information Services, Texas Instruments Incorporated, P. O. Box 5012, MS 308, Dallas, Texas. 75222.

We sincerely hope you will find The Integrated Circuits Catalog for Design Engineers a meaningful addition to your technical library. It represents fourteen years of continuing circuit innovation, refinement, and sophistication by TI engineers.

A

LETTER SYMBOLS, TERMS, AND DEFINITIONS FOR DIGITAL INTEGRATED CIRCUITS

The material which follows applies particularly to the following product lines: TTL, DTL, ECL, and interface circuits having TTL-compatible inputs or outputs.

When several letter symbols are shown, the first is the symbol used on the more recently issued data sheets; the symbol in parentheses was used on earlier data sheets and has the same meaning. Many of these older symbols contain a numeral one or zero which represents the binary logic level, assuming positive logic (1 = high level, 0 = low level). The newer symbols are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for national use and by the International Electrotechnical Commission (IEC) for international use.

The final section contains definitions relating to the classification of circuits by degree of complexity. The definitions for MSI and LSI have been agreed by the JEDEC Council.

VOLTAGES

V_{IH}, ($V_{in(1)}$) High-level input voltage

An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified which is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL}, ($V_{in(0)}$) Low-level input voltage

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified which is the most-positive (least-negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{T+} Positive-going threshold voltage

The voltage level at a transition-operated input which, as the input voltage rises from the defined low level, causes operation of the logic element according to specification.

V_{T-} Negative-going threshold voltage

The voltage level at a transition-operated input which, as the input voltage falls from the defined high level, causes operation of the logic element according to specification.

V_{OH}, ($V_{out(1)}$) High-level output voltage

The voltage at an output terminal for a specified output current I_{OH} (I_{load}) with input conditions applied which according to the product specification will establish a high level at the output.

V_{OL}, ($V_{out(0)}$) Low-level output voltage

The voltage at an output terminal for a specified output current I_{OL} (I_{sink}) with input conditions applied which according to the product specification will establish a low level at the output.

$V_{O(on)}$, (V_{on}) On-state output voltage

The voltage at an output terminal for a specified output current with input conditions applied which according to the product specification will cause the output switching element to be in the on state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

$V_{O(off)}$, (V_{off}) Off-state output voltage

The voltage at an output terminal for a specified output current with input conditions applied which according to the product specification will cause the output switching element to be in the off state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

CURRENTS

I_{IH}, ($I_{in(1)}$) High-level input current
The current flowing into* an input when a specified high-level voltage is applied to that input.

I_{IL}, ($I_{in(0)}$) Low-level input current
The current flowing into* an input when a specified low-level voltage is applied to that input.

I_{OH}, ($I_{out(1)}$) High-level output current
The current flowing into* the output with a specified high-level output voltage V_{OH} ($V_{out(1)}$) applied.

Note: This parameter is usually specified for outputs intended to drive other logic circuits.

$I_{O(off)}$, (I_{off}) Off-state output current
The current flowing into* an output with a specified output voltage applied and input conditions applied which according to the product specification will cause the output switching element to be in the off state.

Note: This parameter is usually specified for outputs intended to drive devices other than logic circuits.

I_{OS} Short-circuit output current
The current which flows into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{CCH}, ($I_{CC(1)}$), I_{EEH} etc. Supply current, high-level output
The current flowing into* the indicated supply terminal of a microcircuit when the output is (or all outputs are) at a high-level voltage.

I_{CCL}, ($I_{CC(0)}$), I_{EEL} etc. Supply current, low-level output
The current flowing into* the indicated supply terminal of a microcircuit when the output is (or all outputs are) at a low-level voltage.

DYNAMIC CHARACTERISTICS

f_{max} Maximum clock frequency (previously shown as "f_{clock}" under "switching characteristics")
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output in accordance with the truth table or specified logic rules.

t_{TLH}, (t_1) Transition time, low-to-high-level (step or output)
The time between a specified low-level voltage and a specified high-level voltage on a waveform which is changing from the defined low level to the defined high level.

t_{THL}, (t_0) Transition time, high-to-low-level (step or output)
The time between a specified high-level voltage and a specified low-level voltage on a waveform which is changing from the defined high level to the defined low level.

t_{PLH}, ($t_{pd(1)}$) Propagation delay time, low-to-high-level output
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

*Current flowing out of a terminal is a negative value.

DYNAMIC CHARACTERISTICS (continued)

t_{PHL}, ($t_{pd(0)}$) Propagation delay time, high-to-low-level output
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_w, (t_p) Average pulse width
The time between 50-percent-amplitude points (or other specified reference points) on the leading and trailing edges of a pulse.

t_{hold} Hold time
The interval immediately following the active transition of the timing pulse (usually the clock pulse) during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. For a dynamic (transition-operated) input, this is the interval immediately following the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure recognition of the transition.

t_{setup} Setup time
The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) during which interval the data to be recognized must be maintained at the input (unless release is specifically permitted) to ensure its recognition. For a dynamic (transition-operated) input, this is the interval immediately preceding the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure recognition of the transition.

$t_{release}$ Release time
The interval between the release of data and the active transition of the timing pulse (usually the clock pulse), this interval being sufficiently short to ensure recognition of the released data.

Note: When specified, the interval designated "release time" falls within the setup interval and constitutes, in effect, a negative hold time.

CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate equivalent circuit
A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

LSI Large-scale integration
A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether logical or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

MSI Medium-scale integration
A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

SSI Small-scale integration
Integrated circuits of less complexity than medium-scale integration (MSI).

THERMAL RESISTANCE OF INTEGRATED CIRCUIT PACKAGES

Typical thermal resistance values of standard integrated circuit packages are shown in the table below. The values shown do not imply any guarantee, but represent the latest and best available data. Steady-state thermal conditions are implied in the resistance measurements. Also, the following definitions apply:

$R_{\theta JC}$ – thermal resistance from junction to case using freon as a heat sink. This parameter offers good repeatability and a high degree (±5%) of correlation.

$R_{\theta JX}$ – thermal resistance from junction to still air (25°C ambient) with package in a specified socket. This parameter is highly dependent on test conditions which are difficult to reproduce accurately.

BIPOLAR PRODUCTS
TYPICAL THERMAL RESISTANCES

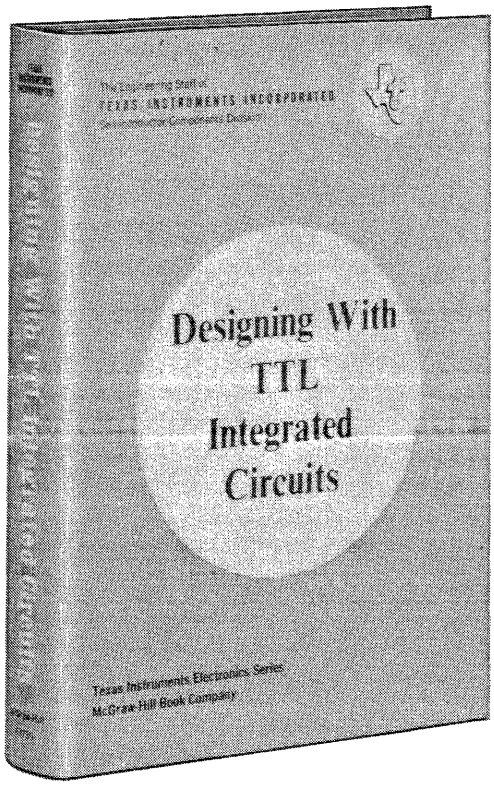
PACKAGE DESCRIPTION	PACKAGE DESIGNATION	°C/WATT		SOCKET USED FOR	POWER
		$R_{\theta JC}$ ±5%	$R_{\theta JX}$ ±15%	$R_{\theta JX}$ MEASUREMENT	(mW)
8-Pin Plastic DIP	P	52	95	Augat	300
14- or 16-Pin Plastic DIP	N	45	90	Augat	300
24-Pin Plastic DIP	N	35	65	Barnes	500
14- or 16-Pin Ceramic DIP	J	20	70	Augat	300
14- or 16-Pin Ceramic Flat Pak (Alloy Mounted)	W, U	45	160	Barnes Carrier/ Contactor	500
14-Pin Ceramic Flat Pak (Glass Mounted)	Z	70	190	Mech-Pak Carrier	300
8- or 10-Pin Plug-In (Alloy Mounted)	L	40	120	Barnes	400
8- or 10-Pin Plug-In (Glass Mounted)	L	90	170	Barnes	700

Special test chips were used to obtain the above information.

A

NEW IN 1971

DESIGNING WITH TTL INTEGRATED CIRCUITS



BY THE IC APPLICATIONS STAFF OF TEXAS INSTRUMENTS INCORPORATED

384 Pages • 399 Illustrations • Hardback • Shipping Weight 2-lb 10-oz • Price $18.50

THIS IS THE ELEVENTH VOLUME in the TI–McGraw-Hill Electrical Engineering Series. Prepared by TI's practical theorists in IC applications, it's devoted exclusively to the implementation of a wide variety of logic functions using TTL. Circuit designers will find this text-and-reference book especially helpful because it offers more than a hundred complete logic designs that can be used with or without modification to solve industrial problems.

But more than that, the book is also designed to give managers, purchasing agents, value analysts, and technicians valuable background even without understanding the mathematics. "Designing With TTL Integrated Circuits" is an indispensable reference work for every electronics library.

CHAPTERS:

1. Introduction to Digital Logic
2. Series 54/74 Overview
3. Circuit Analysis and Characteristics of Series 54/74
4. Extended-Range Operation
5. Noise Considerations
6. Combinational Logic Design
7. Flip-Flops
8. Decoders
9. Arithmetic Elements
10. Counters
11. Shift Registers
12. Other Applications

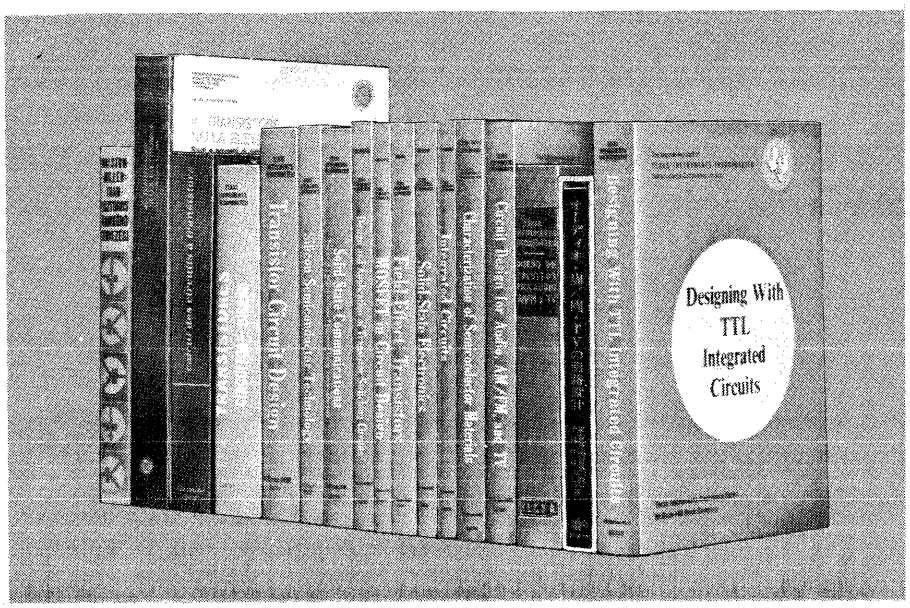
ORDERING INSTRUCTIONS

Source: Order from McGraw-Hill Book Company, either through a bookstore or by writing (with your name, address, company, and position) to:

McGraw-Hill Book Company
P.O. Box 400
Hightstown, N. J. 08520

Mail Order Terms: Ten days' examination on approval. If you remit price plus local tax with your order, McGraw-Hill pays the delivery cost. Otherwise, when book arrives you are billed for delivery cost in addition to the price and local tax, and payment or returned book is due at end of ten-day approval period.

TI-McGraw-Hill Books for Creative Circuit Designers



DESIGNING WITH TTL INTEGRATED CIRCUITS
384 Pages • 399 Illustrations •
Shipping Weight 2-lb 9-oz • $18.50

SOLID STATE ELECTRONICS
170 Pages • 90 Illustrations •
Shipping Weight 1-lb 12-oz • $9.50

INTEGRATED CIRCUITS: A BASIC COURSE
170 Pages • 133 Illustrations •
Shipping Weight 1-lb 10-oz • $9.95

TRANSISTOR CIRCUIT DESIGN
523 Pages • 526 Illustrations •
Shipping Weight 3-lb 4-oz • $16.50
(Also available in French, Italian, Spanish, Hungarian, and Japanese)

FIELD-EFFECT TRANSISTORS
138 Pages • 173 Illustrations •
Shipping Weight 1-lb 10-oz • $10.00

MOSFET IN CIRCUIT DESIGN
136 Pages • 100 Illustrations •
Shipping Weight 1-lb 10-oz • $11.00

CIRCUIT DESIGN FOR AUDIO, AM/FM AND TV
352 Pages • 145 Illustrations •
Shipping Weight 2-lb 8-oz • $16.50
(Also available in Spanish and Japanese)

SILICON SEMICONDUCTOR TECHNOLOGY
256 Pages • 301 Illustrations •
Shipping Weight 2-lb 9-oz • $16.50

DESIGN AND APPLICATION OF TRANSISTOR SWITCHING CIRCUITS
278 Pages • 315 Illustrations •
Shipping Weight 2-lb •$14.50

SOLID STATE COMMUNICATIONS
366 Pages • 417 Illustrations •
Shipping Weight 2-lb 9-oz • $13.75

CHARACTERIZATION OF SEMICONDUCTOR MATERIALS
351 Pages • 221 Illustrations •
Shipping Weight 2-lb 9-oz • $18.50

ORDERING INSTRUCTIONS

Source: Order from McGraw-Hill Book Company, either through a bookstore or by writing (with your name, address, company, and position) to:

McGraw-Hill Book Company
P.O. Box 400
Hightstown, N.J. 08520

Mail Order Terms: Ten days' examination on approval. If you remit price plus local tax with your order, McGraw-Hill pays the delivery cost. Otherwise, when book arrives you are billed for delivery cost in addition to the price and local tax, and payment or returned book is due at end of ten-day approval period.

B

Indexes

Numerical·Functional·Cross-Reference

B

NUMERICAL INDEX

NUMERICAL INDEX

B

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

NUMERICAL INDEX

B

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

NUMERICAL INDEX

B

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

LINEAR CIRCUITS
FUNCTIONAL INDEX

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*					SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line			Plug-In	Flat	
OPERATIONAL AMPLIFIERS								
General Purpose Operational Amplifiers	SN52702A			N		L	S	3-18
	SN52702	SN72702		N		L	S	3-18
High-Performance Operational Amplifiers	SN52101A	SN72301A	J	N	P	L	Z	3-5
	SN52107	SN72307	J	N	P	L	Z	3-9
	SN52709A			N	P	L	S	3-27
	SN52709	SN72709		N	P	L	S	3-27
	SN52741	SN72741	J	N	P	L	Z	3-34
	SN52748	SN72748	J	N	P	L	Z	3-43
	SN52770	SN72770	J	N	P	L	Z	3-47
	SN52771	SN72771	J	N	P	L	Z	3-53
Dual High-Performance Operational Amplifiers	SN52558	SN72558			P	L		3-13
	SN52747	SN72747	J	N				3-39
DIFFERENTIAL COMPARATORS								
Differential Comparators	SN52710	SN72710	J	N		L	S	3-68
	SN52810	SN72810	J	N	P	L	Z	3-79
Differential Comparators with Strobes	SN52510	SN72510	J	N	P	L	Z	3-60
Dual-Channel Differential Comparators with Strobes	SN52711	SN72711	J	N		L	S	3-72
	SN52811	SN72811	J	N		L		3-85
Dual Differential Comparators		SN72720		N				3-77
	SN52820	SN72820	J	N				3-91
Dual Differential Comparators with Strobes	SN52514	SN72514	J	N				3-66
VIDEO AMPLIFIERS								
Differential Video Amplifiers	SN52733	SN72733		N		L		3-94
	SN5510					L	F	3-101
		SN7510				L	F	3-108
	SN5511	SN7511		N		L	F	3-115
	SM5512	SM7512				L		3-121
	SN5514	SN7514				L		3-121
LINE CIRCUITS								
Dual Line Drivers	SN55109		J					3-130
		SN75109	J	N				3-130
	SN55110		J					3-130
		SN75110	J	N				3-130
Dual Line Receivers	SN55107A		J					3-130
		SN75107A	J	N				3-130
	SN55108A		J					3-130
		SN75108A	J	N				3-130
		SN75150	J	N	P			3-149
Dual Differential Line Receiver		SN75100L				L		3-126
Quadruple Line Receiver		SN75154	J	N				3-153

*For outline drawings of all packages, see Section 1.

LINEAR CIRCUITS
FUNCTIONAL INDEX

B

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*					SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Plug-In		Flat	
SENSE AMPLIFIERS								
Dual-Channel Sense Amplifiers		SN7522	J	N				3-166
		SN7523	J	N				3-166
Dual-Channel Sense Amplifiers with Complementary Outputs		SN7520	J	N				3-164
		SN7521	J	N				3-164
Dual-Channel Sense Amplifiers with Output Registers		SN7526	J	N				3-172
		SN7527	J	N				3-172
Dual Sense Amplifiers		SN7524	J	N				3-170
		SN7525	J	N				3-170
		SN75234	J	N				3-176
		SN75235	J	N				3-176
Dual Sense Amplifiers with Preamplifier Test Points		SN7528	J	N				3-174
		SN7529	J	N				3-174
		SN75238	J	N				3-178
		SN75239	J	N				3-178
MEMORY AND PERIPHERAL DRIVERS								
2 X 4 Transistor Arrays		SN75303		N			S	3-212
		SN75308	J	N				3-217
Memory Driver		SN75325						3-230
Memory Driver with Decode Inputs		SN75324						3-222
Dual Peripheral Drivers		SN75450A		N				3-247
		SN75451A			P			3-249
		SN75452		P	P			3-250
		SN75453			P			3-251
		SN75454			P			3-252
Diode Arrays	TID21A Series			N			F	3-264
VOLTAGE REGULATOR								
Voltage Regulator		SN72400		N		L		3-270
COMMUNICATIONS CIRCUITS								
Logarithmic Amplifiers	SN56502	SN76502	J	N				3-277
Balanced Mixers	SN56514	SN76514	J	N		L		3-284
CONSUMER CIRCUITS								
Consumer Circuits Summary								3-289
Stereo Demodulator		SN76110		N				3-290

*For outline drawings of all packages, see Section 1.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES 54S/74S CIRCUITS
FUNCTIONAL INDEX

SERIES 54S/74S
FEATURING 3-ns SPEED AND 20-mW-PER-GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

B

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	PAGE
NAND/NOR GATES						
Quadruple 2-Input Positive-NAND Gates	SN54S00	SN74S00	J	N	W	5-4
Quadruple 2-Input Positive-NAND Gates (with Open-Collector Output)	SN54S03	SN74S03	J	N	W	5-8
Hex Inverters	SN54S04	SN74S04	J	N	W	5-4
Hex Inverters (with Open-Collector Output)	SN54S05	SN74S05	J	N	W	5-8
Triple 3-Input Positive-NAND Gates	SN54S10	SN74S10	J	N	W	5-4
Triple 3-Input Positive-AND Gates	SN54S11	SN74S11	J	N	W	5-10
Triple 3-Input Position-AND Gates (with Open-Collector Output)	SN54S15	SN74S15	J	N	W	5-10
Dual 4-Input Positive-NAND Gates	SN54S20	SN74S20	J	N	W	5-4
Dual 4-Input Positive-NAND Gates (with Open-Collector Output)	SN54S22	SN74S22	J	N	W	5-8
Dual 4-Input Positive-NAND Buffers	SN54S40	SN74S40	J	N	W	5-12
Dual 4-Input Positive-NAND Line Drivers	SN54S140	SN74S140	J	N	W	5-12
AND-OR-INVERT GATES						
4-2-3-2-Input AND-OR-INVERT Gates	SN54S64	SN74S64	J	N	W	5-13
4-2-3-2-Input AND-OR-INVERT Gates (with Open-Collector Output)	SN54S65	SN74S65	J	N	W	5-13
FLIP-FLOPS						
Dual D-Type Edge-Triggered Flip-Flops	SN54S74	SN74S74	J	N	W	5-15
Dual J-K Negative Edge-Triggered Flip-Flops (80 MHz) with Preset and Clear	SN54S112	SN74S112	J	N	W	5-17
Dual J-K Negative Edge-Triggered Flip-Flops (80 MHz) with Preset	SN54S113	SN74S113	J	N	W	5-21
Dual J-K Negative Edge-Triggered Flip-Flops (80 MHz) Common Clock and Common Clear	SN54S114	SN74S114	J	N	W	5-21

*For outline drawings of all packages, see Section 1.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES 54/74
FEATURING 10 ns SPEED AND 10 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

B

FUNCTION	OPERATING TEMPERATURE RANGES		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
NAND/NOR/AND/OR GATES AND BUFFERS						
Quadruple 2-Input Positive NAND Gates	SN5400	SN7400	J	N	W	6-5
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN5401	SN7401	J	N	W	6-6
Quadruple 2-Input Positive NOR Gates	SN5402	SN7402	J	N	W	6-9
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN5403	SN7403	J	N		6-10
Hex Inverters	SN5404	SN7404	J	N	W	6-11
Hex Inverters (with Open-Collector Output)	SN5405	SN7405	J	N	W	6-12
Hex Inverter Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5406	SN7406	J	N	W	6-13
Hex Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5407	SN7407	J	N	W	6-15
Quadruple 2-Input Positive AND Gates	SN5408	SN7408	J	N	W	6-17
Quadruple 2-Input Positive AND Gates	SN5409	SN7409	J	N	W	6-17
Triple 3-Input Positive NAND Gates	SN5410	SN7410	J	N	W	6-20
Triple 3-Input Positive NAND Gates (with Open-Collector Output)	SN5412	SN7412	J	N	W	6-21
Dual NAND Schmitt Triggers	SN5413	SN7413	J	N	W	6-22
Hex Inverter Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5416	SN7416	J	N	W	6-13
Hex Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5417	SN7417	J	N	W	6-15
Dual 4-Input Positive NAND Gates	SN5420	SN7420	J	N	W	6-26
Expandable Dual 4-Input Positive NOR Gates (with Strobe)	SN5423	SN7423	J	N	W	6-27
Dual 4-Input Positive NOR Gates	SN5425	SN7425	J	N	W	6-27
Quadruple 2-Input High-Voltage Interface NAND Gates	SN5426	SN7426	J	N		6-30
Triple 3-Input Positive NOR Gates	SN5427	SN7427	J	N	W	6-32
8-Input Positive NAND Gates	SN5430	SN7430	J	N	W	6-34
Quadruple 2-Input Positive OR Gates	SN5432	SN7432	J	N	W	6-35
Quadruple 2-Input Positive NAND Buffers	SN5437	SN7437	J	N	W	6-37
Quadruple 2-Input Positive NAND Buffers (with Open-Collector Output)	SN5438	SN7438	J	N	W	6-37
Dual 4-Input Positive NAND Buffers	SN5440	SN7440	J	N	W	6-39

*For outline drawings of all packages, see Section 1.

SERIES 54/74 CIRCUITS
FUNCTIONAL INDEX

B

SERIES 54/74
FEATURING 10 ns SPEED AND 10 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGES		PACKAGES*			
	–55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	SEC.-PAGE
AND-OR-INVERT GATES						
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN5450	SN7450	J	N	W	6-40
Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN5451	SN7451	J	N	W	6-40
Expandable 4-Wide 2-Input AND-OR-INVERT Gates	SN5453	SN7453	J	N	W	6-42
4-Wide 2-Input AND-OR-INVERT Gates	SN5454	SN7454	J	N	W	6-42
EXPANDERS						
Dual 4-Input Expander	SN5460		J	N	W	6-44
Dual 4-Input Expander		SN7460	J	N	W	6-45
FLIP-FLOPS						
Positive Edge-Triggered J-K Flip-Flops (AND Inputs)	SN5470	SN7470	J	N	W	6-46
J-K Master-Slave Flip-Flops (AND Inputs)	SN5472	SN7472	J	N	W	6-49
Dual J-K Master-Slave Flip-Flops	SN5473	SN7473	J	N	W	6-52
Dual D-Type Edge-Triggered Flip-Flops	SN5474	SN7474	J	N	W	6-55
Dual-J-K Master-Slave Flip-Flops with Preset and Clear	SN5476	SN7476	J	N	W	6-58
Gated J-K Master-Slave Flip-Flops	SN54104	SN74104	J	N	W	6-61
Gated J-K Master-Slave Flip-Flops	SN54105	SN74105	J	N	W	6-61
Dual J-K Master-Slave Flip-Flops (V_{CC}-14, Gnd-7)	SN54107	SN74107	J	N		6-52
Gated J-K Master-Slave Flip-Flops with Data Lockout	SN54110	SN74110	J	N	W	6-66
Dual J-K Master-Slave Flip-Flops with Data Lockout	SN54111	SN74111	J	N	W	6-69
Monostable Multivibrators	SN54121	SN74121	J	N	W	6-72
Retriggerable Monostable Multivibrators with Clear	SN54122	SN74122	J	N	W	6-79
Dual Retriggerable Monostable Multivibrators with Clear	SN54123	SN74123	J	N	W	6-79

*For outline drawings of all packages, see Section 1.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

B

SERIES 54H/74H
FEATURING 6 ns SPEED AND 22 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
NAND/NOR GATES						
Quadruple 2-Input Positive NAND Gates	SN54H00	SN74H00	J	N	W	7-5
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN54H01	SN74H01	J	N	W	7-6
Hex Inverters	SN54H04	SN74H04	J	N	W	7-9
Hex Inverters (with Open-Collector Output)	SN54H05	SN74H05	J	N	W	7-10
Triple 3-Input Positive NAND Gates	SN54H10	SN74H10	J	N	W	7-11
Triple 3-Input Positive AND Gates	SN54H11	SN74H11	J	N	W	7-12
Dual 4-Input Positive NAND Gates	SN54H20	SN74H20	J	N	W	7-13
Dual 4-Input Positive AND Gates	SN54H21	SN74H21	J	N	W	7-14
Dual 4-Input Positive NAND Gates (with Open-Collector Output)	SN54H22	SN74H22	J	N	W	7-15
8-Input Positive NAND Gates	SN54H30	SN74H30	J	N	W	7-16
Dual 4-Input Positive NAND Buffers	SN54H40	SN74H40	J	N	W	7-17
AND-OR/AND-OR-INVERT GATES						
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN54H50	SN74H50	J	N	W	7-18
Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN54H51	SN74H51	J	N	W	7-18
Expandable 2-2-2-3-Input AND-OR Gates	SN54H52	SN74H52	J	N	W	7-20
Expandable 2-2-2-3-Input AND-OR-INVERT Gates	SN54H53	SN74H53	J	N	W	7-22
4-Wide 2-Input AND-OR-INVERT Gates	SN54H54	SN74H54	J	N	W	7-22
Expandable 2-Wide 4-Input AND-OR-INVERT Gates	SN54H55	SN74H55	J	N	W	7-24
EXPANDERS						
Dual 4-Input Expander	SN54H60		J	N	W	7-26
Dual 4-Input Expander		SN74H60	J	N	W	7-27
Triple 3-Input Expanders	SN54H61	SN74H61	J	N	W	7-28
3-2-2-3-Input AND-OR Expander	SN54H62		J	N	W	7-29
3-2-2-3-Input Expander		SN74H62	J	N	W	7-30

*For outline drawings of all packages, see Section 1.

SERIES 54H/74H CIRCUITS
FUNCTIONAL INDEX

B

SERIES 54H/74H
FEATURING 6 ns SPEED AND 22 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
FLIP-FLOPS						
J-K Master-Slave Flip-Flops (AND-OR Inputs)	SN54H71	SN74H71	J	N	W	7-31
J-K Master-Slave Flip-Flops (AND Inputs)	SN54H72	SN74H72	J	N	W	7-34
Dual J-K Master-Slave Flip-Flops	SN54H73	SN74H73	J	N	W	7-37
Dual D-Type Edge-Triggered Flip-Flops	SN54H74	SN74H74	J	N	W	7-40
Dual J-K Master-Slave Flip-Flops with Preset and Clear	SN54H76	SN74H76	J	N	W	7-44
Dual J-K Master-Slave Flip-Flops (Common Clock)	SN54H78	SN74H78	J	N	W	7-47
J-K Negative Edge-Triggered Flip-Flops with AND-OR Inputs (50 MHz)	SN54H101	SN74H101	J	N	W	7-50
J-K Negative Edge-Triggered Flip-Flops with AND Inputs (50 MHz)	SN54H102	SN74H102	J	N	W	7-53
Dual J-K Negative Edge-Triggered Flip-Flops (50 MHz)	SN54H103	SN74H103	J	N	W	7-56
Dual J-K Negative Edge-Triggered Flip-Flops (50 MHz) with Preset and Clear	SN54H106	SN74H106	J	N	W	7-59
Dual J-K Negative Edge-Triggered Flip-Flops (50 MHz) (Common Clock)	SN54H108	SN74H108	J	N	W	7-62

*For outline drawings of all packages, see Section 1.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

B

SERIES 54L/74L
FEATURING 1 mW AND 33 ns PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
NAND/NOR GATES						
Quadruple 2-Input Positive NAND Gates	SN54L00	SN74L00	J	N	T	8-4
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN54L01	SN74L01	J	N	T	8-5
Quadruple 2-Input Positive NOR Gates	SN54L02	SN74L02	J	N	T	8-6
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN54L03	SN74L03	J	N	T	8-5
Hex Inverters	SN54L04	SN74L04	J	N	T	8-9
Triple 3-Input Positive NAND Gates	SN54L10	SN74L10	J	N	T	8-10
Dual 4-Input Positive NAND Gates	SN54L20	SN74L20	J	N	T	8-11
8-Input Positive NAND Gates	SN54L30	SN74L30	J	N	T	8-12
AND-OR-INVERT GATES						
Dual 2-Wide AND-OR-INVERT Gates	SN54L51	SN74L51	J	N	T	8-13
4-Wide 3-2-2-3-Input AND-OR-INVERT Gates	SN54L54	SN74L54	J	N	T	8-14
2-Wide 4-Input AND-OR-INVERT Gates	SN54L55	SN74L55	J	N	T	8-15
FLIP-FLOPS						
R-S Master-Slave Flip-Flops	SN54L71	SN74L71	J	N	T	8-16
J-K Master-Slave Flip-Flops	SN54L72	SN74L72	J	N	T	8-19
Dual J-K Master-Slave Flip-Flops	SN54L73	SN74L73	J	N	T	8-22
Dual D-Type Edge-Triggered Flip-Flops	SN54L74	SN74L74	J	N	T	8-25
Dual J-K Master-Slave Flip-Flops (Common Clock)	SN54L78	SN74L78	J	N	T	8-28
Retriggerable Monostable Multivibrators with Clear	SN54L122	SN74L122	J	N	T	8-31

*For outline drawings of all packages, see Section 1.

TTL MSI CIRCUITS
FUNCTIONAL INDEX

TTL
MEDIUM SCALE INTEGRATION (MSI)

B

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	–55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
ASYNCHRONOUS COUNTERS						
Decade Counters	SN5490	SN7490	J	N	W	9-4
Decade Counters (Low Power)	SN54L90	SN74L90	J	N	T	9-9
Divide-by-Twelve Counters	SN5492	SN7492	J	N	W	9-14
4-Bit Binary Counters	SN5493	SN7493	J	N	W	9-19
4-Bit Binary Counters (Low Power)	SN54L93	SN74L93	J	N	T	9-24
50-MHz Preset Table Decade Counters/Latches	SN54196	SN74196	J	N	W	9-29
50-MHz Preset Table 4-Bit Binary Counters/Latches	SN54197	SN74197	J	N	W	9-29
SYNCHRONOUS COUNTERS						
Synchronous 6-Bit Binary Rate Multiplier		SN7497	J	N	W	9-35
Sychronous Decade Counters	SN54160	SN74160	J	N	W	9-41
Synchronous 4-Bit Binary Counters	SN54161	SN74161	J	N	W	9-41
Fully Synchronous Decade Counters	SN54162	SN74162	J	N	W	9-41
Fully Synchronous 4-Bit Binary Counters	SN54163	SN74163	J	N	W	9-41
Synchronous Decade Decimal Rate Multiplier		SN74167	J	N	W	9-35
Synchronous Up/Down Decade Counters (Single Clock Line)	SN54190	SN74190	J	N	W	9-49
Synchronous Up/Down 4-Bit Binary Counters (Single Clock Line)	SN54191	SN74191	J	N	W	9-49
Synchronous Up/Down Decade Counters (Two Clock Lines)	SN54192	SN74192	J	N	W	9-57
Synchronous Up/Down 4-Bit Binary Counters (Two Clock Lines)	SN54193	SN74193	J	N	W	9-57
4-BIT, 5-BIT, 6-BIT SHIFT/STORAGE REGISTERS						
4-Bit Shift Registers (Parallel-In, Serial-Out)	SN5494	SN7494	J	N	W	9-58
4-Bit Universal Shift Registers (Parallel-In, Parallel-Out)	SN5495A	SN7495A	J	N	W	9-72
4-Bit Universal Shift Registers (Parallel-In, Parallel-Out) (Low Power)	SN54L95	SN74L95	J	N	T	9-79
5-Bit Shift Registers (Dual-Parallel-In, Parallel-Out)	SN5496	SN7496	J	N	W	9-86
4-Bit Data Selectors/Storage Registers (Low Power)	SN54L98	SN74L98	J	N		9-90
4-Bit Right-Shift Registers with J K and D (Low Power)	SN54L99	SN74L99	J	N		9-96
4-Bit Parallel-In, Parallel-Out Bidirectional Shift Registers	SN54194	SN74194	J	N	W	9-104
4-Bit Parallel-In, Parallel-Out Shift Register (J-$\overline{K}$ Inputs to First Stage)	SN54195	SN74195	J	N	W	9-108

*For outline drawings of all packages, see Section 1.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TTL
MEDIUM SCALE INTEGRATION (MSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
8-BIT SHIFT REGISTERS						
8-Bit Shift Registers	SN5491A	SN7491A	J	N	W	9-112
8-Bit Shift Registers (Low Power)	SN54L91	SN74L91	J	N	T	9-117
8-Bit Parallel-Out Shift Registers	SN54164	SN74164	J	N	W	9-122
8-Bit Parallel-Out Shift Registers (Low Power)	SN54L164	SN74L164	J	N	T	9-126
Parallel-Load 8-Bit Shift Registers	SN54165	SN74165	J	N	W	9-130
Parallel-Load 8-Bit Shift Registers	SN54166	SN74166	J	N	W	9-134
8-Bit Parallel-In, Parallel-Out Bidirectional Shift Registers	SN54198	SN74198	J	N	W	9-134
8-Bit Parallel-In, Parallel-Out Shift Registers (J-$\overline{K}$ Inputs to First Stage)	SN54199	SN74199	J	N	W	9-134
CODE CONVERTERS						
BCD-to-Binary Converters	SN54184	SN74184	J	N	W	9-142
Binary-to-BCD Converters	SN54185A	SN74185A	J	N	W	9-142
DECODERS/DEMULTIPLEXERS						
BCD-to-Decimal Decoders	SN5442	SN7442	J	N	W	9-148
BCD-to-Decimal Decoders (Low Power)	SN54L42	SN74L42	J	N		9-154
Excess-3-to-Decimal Decoders	SN5443	SN7443	J	N	W	9-148
Excess-3-to-Decimal Decoders (Low Power)	SN54L43	SN74L43	J	N		9-154
Excess-3-Gray-to-Decimal Decoders	SN5444	SN7444	J	N	W	9-148
Excess-3-Gray-to-Decimal Decoders (Low Power)	SN54L44	SN74L44	J	N	W	9-154
4-Line-to-16-Line (1 of 16) Decoders/Demultiplexers	SN54154	SN74154	J	N	W	9-160
Dual 2-Line-to-4-Line Decoders/Demultiplexers	SN54155	SN74155	J	N	W	9-167
Dual 2-Line-to-4-Line Decoders/Demultiplexers (with Open-Collector Output)	SN54156	SN74156	J	N	W	9-167
DECODERS/LAMP DRIVERS/BUFFERS						
BCD-to-Decimal Decoders/Drivers with 30-V Output	SN5445	SN7445	J	N	W	9-175
BCD-to-Decimal Decoders/Drivers with 15-V Output	SN54145	SN74145	J	N	W	9-175
BCD-to-Seven-Segment Decoders/Drivers with 30-V Output	SN5446A	SN7446A	J	N	W	9-181
BCD-to-Seven-Segment Decoders/Drivers with 30-V Output (Low Power)	SN54L46	SN74L46	J	N		9-198
BCD-to-Seven-Segment Decoders/Drivers with 15 V Output	SN5447A	SN7447A	J	N	W	9-181
BCD-to-Seven-Segment Decoders/Drivers with 15-V Output (Low Power)	SN54L47	SN74L47	J	N		9-198
BCD-to-Seven-Segment Decoders	SN5448	SN7448	J	N	W	9-181
BCD-to-Seven-Segment Decoders (14-pin Function)	SN5449	SN7449	J	N	W	9-181
BCD-to-Decimal Decoder/Driver		SN74141	J	N	W	9-208

*For outline drawings of all packages, see Section 1.

TTL MSI CIRCUITS
FUNCTIONAL INDEX

TTL
MEDIUM SCALE INTEGRATION (MSI)

B

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
LATCHES						
Quadruple Bistable Latches	SN5475	SN7475	J	N	W	9-213
Quadruple Bistable Latches (14-pin Function)	SN5477	SN7477			W	9-213
8-Bit Bistable Latches	SN54100	SN74100	J	N	W	9-213
MEMORIES						
16-Bit Random-Access Memories (16W by 1B)	SN5481	SN7481	J	N	W	9-221
16-Bit Random-Access Memories with Gated Write Inputs (16W by 1B)	SN5484	SN7484	J	N	W	9-221
64-Bit Random-Access Memory (16W by 4B)		SN7489	J	N	W	9-230
256-Bit Read-Only Memories (32W by 8B)	SN5488A	SN7488A		N		9-235
1024-Bit Read-Only Memories (256W by 4B)	SN54187	SN74187	J	N	W	9-244
4-By-4 Register Files	SN54170	SN74170	J	N	W	9-248
ARITHMETIC ELEMENTS						
Gated Full Adders	SN5480	SN7480	J	N	W	9-255
2-Bit Binary Full Adders	SN5482	SN7482	J	N	W	9-264
4-Bit Binary Full Adders	SN5483	SN7483	J	N	W	9-271
4-Bit Binary Full Adders (Low-Power Schottky)	SN54LS83	SN74LS83	J	N		9-279
4-Bit Magnitude Comparators	SN5485	SN7485	J	N	W	9-286
4-Bit Magnitude Comparators (Low Power)	SN54L85	SN74L85	J	N		9-289
Quadruple 2-Input Exclusive-OR Gates	SN5486	SN7486	J	N	W	9-296
Quadruple 2-Input Exclusive-OR Gates (Low Power)	SN54L86	SN74L86	J	N	T	9-300
4-Bit True/Complement Zero-One Elements	SN54H87	SN54H87	J	N	W	9-304
8-Bit Odd/Even Parity Generators/Checkers	SN54180	SN74180	J	N	W	9-309
4-Bit Arithmetic Logic Unit (ALU) and Function Generators	SN54181	SN74181	J	N	W	9-315
Look-Ahead Carry Generators (for ALU)	SN54182	SN74182	J	N	W	9-326
Dual Carry-Save Full Adders	SN54H183	SN74H183	J	N	W	9-332
DATA SELECTORS/MULTIPLEXERS						
16-Bit Data Selectors/Multiplexers	SN54150	SN74150	J	N	W	9-339
8-Bit Data Selectors/Multiplexers with Strobe	SN54151	SN74151	J	N	W	9-339
8-Bit Data Selectors/Multiplexers	SN54152	SN74152			W	9-339
Dual 4-Line-to-1-Line Data Selectors/Multiplexers	SN54153	SN74153	J	N	W	9-351
Dual 4-Line-to-1-Line Data Selectors/Multiplexers (Low Power)	SN54L153	SN74L153	J	N		9-358
LOGIC DIODE MATRICES						
Series TIDM1, TIDM2 Monolithic Diode Matrices			J		F, W	9-365

*For outline drawings of all packages, see Section 1.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

RADIATION HARDENED CIRCUITS
FUNCTIONAL INDEX

FUNCTION	TYPE NO.	PACKAGE	SEC.-PAGE
LINEAR CIRCUITS			
High-Performance Operational Amplifier	RSN52709	H	10-58
Threshold Detector	RSN55909	H	10-55
Dual-Channel Switched Preamplifier	RSN55910	H	10-55
D-C Coupled 4-Channel Sense Amplifier	RSN55920	H	10-55
TTL CIRCUITS			
Quadruple 2-Input Positive-NAND Gates	RSN5400	H	10-6
	RSN54H00	H	10-6
	RSN54L00	H	10-32
Hex Inverters	RSN5404	H	10-8
	RSN54H04	H	10-8
Triple 3-Input Positive-NAND Gates	RSN5410	H	10-6
	RSN54H10	H	10-6
	RSN54L10	H	10-32
Dual 4-Input Positive-NAND Gates	RSN5420	H	10-6
	RSN54H20	H	10-6
	RSN54L20	H	10-32
11-Input Positive-NAND Gates	RSN5431	H	10-6
	RSN54H31	H	10-6
Dual 4-Input Positive-NAND Buffers	RSN5440	H	10-9
	RSN54H40	H	10-9
2-Wide 3-Input, 2-Wide 2-Input, Dual AND-OR-INVERT Gates	RSN5456	H	10-10
	RSN54H56	H	10-10
3-3-2-3-Input AND-OR-INVERT Gates	RSN5457	H	10-10
	RSN54H57	H	10-10
3-3-3-2-Input AND-OR-INVERT Gate	RSN54L57	H	10-34
2-Wide 4-Input AND-OR-INVERT Gates	RSN5458	H	10-10
	RSN54H58	H	10-10
R-S Master-Slave Flip-Flop	RSN54L71	H	10-35
J-K Master-Slave Flip-Flop	RSN54L72	H	10-38
Dual D-Type Edge-Triggered Flip-Flops	RSN5474	H	10-12
	RSN54H74	H	10-12
	RSN54L74	H	10-41
Dual J-K Edge-Triggered Flip-Flop	RSN54H103	H	10-15
Dual 3-Input Positive-NAND Gate	RSN54L130	H	10-32
Dual Expandable 3-Input Positive-NAND Gate	RSN54L131	H	10-32
DTL CIRCUITS			
Expandable Dual 4-Input NAND Gate	RSN15930	H	10-57
Expandable Dual 4-Input NAND Buffer Gate	RSN15932	H	10-57
Expandable Dual 4-Input NAND Power Gate	RSN15944	H	10-57
J-K/S-R Flip-Flop	RSN15945	H	10-57
Triple 3-Input NAND Gate	RSN15962	H	10-57
DIODE ARRAYS			
7-Diode Array	RSN14925	H	10-57
16-Diode Array	RSN14097	H	10-57

DTL CIRCUITS
FUNCTIONAL INDEX

B

Function	Operating Temperature Ranges		Packages*		
	−55°C to 125°C	0°C to 75°C	Dual-In-Line		Flat
GATES WITH 6-kΩ PULL-UP RESISTORS					
Expandable Dual 4-Input NAND Gates	SN15930	SN15830	J	N	U
Quadruple 2-Input NAND Gates	SN15946	SN15846	J	N	U
Triple 3-Input NAND Gates	SN15962	SN15862	J	N	U
Dual 5-Input NAND Gates	SN151900	SN151800	J	N	U
Expandable 8-Input NAND Gates	SN151902	SN151802	J	N	U
10-Input NAND Gates	SN151904	SN151804	J	N	U
Quadruple 2-Input AND Gates	SN151906	SN151806	J	N	U
Quadruple 2-Input OR Gates	SN151908	SN151808	J	N	U
Quadruple 2-Input NOR Gates	SN151910	SN151810	J	N	U
Quadruple 2-Input Exclusive-OR Gates	SN151912	SN151812	J	N	U
GATES WITH 2-kΩ PULL-UP RESISTORS					
Quadruple 2-Input NAND Gates	SN15949	SN15849	J	N	U
Expandable Dual 4-Input NAND Gates	SN15961	SN15861	J	N	U
Triple 3-Input NAND Gates	SN15963	SN15863	J	N	U
Dual 5-Input NAND Gates	SN151901	SN151801	J	N	U
Expandable 8-Input NAND Gates	SN151903	SN151803	J	N	U
10-Input NAND Gates	SN151905	SN151805	J	N	U
Quadruple 2-Input AND Gates	SN151907	SN151807	J	N	U
Quadruple 2-Input OR Gates	SN151909	SN151809	J	N	U
Quadruple 2-Input NOR Gates	SN151911	SN151811	J	N	U
POWER/BUFFER GATES					
Expandable Dual 4-Input NAND Buffer Gates	SN15932	SN15832	J	N	U
Expandable Dual 4-Input NAND Power Gates	SN15944	SN15844	J	N	U
Quadruple 2-Input NAND Buffer Gates	SN15957	SN15857	J	N	U
Quadruple 2-Input NAND Power Gates	SN15958	SN15858	J	N	U
HEX INVERTERS					
6-kΩ Pull-Up Resistors	SN15934	SN15834	J	N	U
Expandable (Open-Base) or Translator Inputs	SN15935	SN15835	J	N	U
6-kΩ Pull-Up Resistors	SN15936	SN15836	J	N	U
2-kΩ Pull-Up Resistors	SN15937	SN15837	J	N	U
Open-Collector Outputs	SN15938	SN15838	J	N	U
EXPANDERS					
Dual 4-Input Expanders	SN15933	SN15833	J	N	U
FLIP-FLOPS					
Gated J-K/R-S (6-kΩ Pull-Up Resistors)	SN15931	SN15831	J	N	U
Gated J-K/R-S (6-kΩ Pull-Up Resistors)	SN15945	SN15845	J	N	U
Gated J-K/R-S (2-kΩ Pull-Up Resistors)	SN15948	SN15848	J	N	U
Pulse-Triggered Binary (Active Pull-Up)	SN15950	SN15850	J	N	U
Dual J-K, Individual Clocks and Presets (6-kΩ Pull-Up Resistors)	SN159093	SN158093	J	N	U
Dual J-K, Individual Clocks and Presets (2-kΩ Pull-Up Resistors)	SN159094	SN158094	J	N	U
Dual J-K, Common Clocks and Clears (2-kΩ Pull-Up Resistors)	SN159097	SN158097	J	N	U
Dual J-K, Common Clocks and Clears (6-kΩ Pull-Up Resistors)	SN159099	SN158099	J	N	U
MONOSTABLE MULTIVIBRATORS					
Gated, Negative-Edge-Triggered	SN15951	SN15851	J	N	U

*For outline drawings of all packages, see Section 1.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

FUNCTIONS	OPERATING TEMPERATURE RANGE −55°C to 125°C	FAN-OUT	OPERATING TEMPERATURE RANGE 0°C to 75°C	FAN-OUT	PACKAGES‡ Dual-In-Line		Flat
Dual 4-Input NAND Gates	SNG40 SNG41	15 7	SNG42 SNG43	12 6	J	N	U
Expandable 2-2-2-3-Input AND-OR-INVERT Gates	SNG50 SNG51	15 7	SNG52 SNG53	12 6	J	N	U
8-Input NAND Gates	SNG60 SNG61	15 7	SNG62 SNG63	12 6	J	N	U
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gates	SNG70 SNG71	15 7	SNG72 SNG73	12 6	J	N	U
Dual Pulse Shaper/Delay AND Gates	SNG80 SNG81	15 7	SNG82 SNG83	12 6	J	N	U
2-Wide 3-Input AND-OR-INVERT Gates with 2-Input Gated Complement	SNG90 SNG91	15 7	SNG92 SNG93	12 6	J	N	U
Expandable 3-Wide 3-Input AND-OR-INVERT Gates	SNG100 SNG101	15 7	SNG102 SNG103	12 6	J	N	U
Expandable 2-Wide 4-Input AND-OR-INVERT Gates	SNG110 SNG111	15 7	SNG112 SNG113	12 6	J	N	U
Expandable 8-Input NAND Gates	SNG120 SNG121	15 7	SNG122 SNG123	12 6	J	N	U
Dual 4-Input Line Drivers	SNG130 SNG131	30 15	SNG132 SNG133	24 12	J	N	U
Quadruple 2-Input NAND Gates	SNG140 SNG141	15 7	SNG142 SNG143	12 6	J	N	U
3-2-2-3-Input Expanders for AND-OR-INVERT Gates	SNG150 SNG151		SNG152 SNG153		J	N	U
Triple 2-Input NAND Drivers	SNG160 SNG161	15 7	SNG162 SNG163	12 6	J	N	U
Dual 4-Input Expanders for AND-OR-INVERT Gates	SNG170 SNG171		SNG172 SNG173		J	N	U
Dual 4-Input Expanders for NAND Gates	SNG180 SNG181		SNG182 SNG183		J	N	U
Triple 3-Input NAND Gates	SNG190 SNG191	15 7	SNG192 SNG193	12 6	J	N	U
Expandable 8-Input NAND Gates	SNG200 SNG201	11 6	SNG202 SNG203	9 5	J	N	U
Expandable 2-Wide 4-Input AND-OR-INVERT Gates	SNG210 SNG211	11 6	SNG212 SNG213	9 5	J	N	U
Quadruple 2-Input NAND Gates	SNG220 SNG221	11 6	SNG222 SNG223	9 5	J	N	U
3-2-2-3-Input Expanders for AND-OR-INVERT Gates	SNG230 SNG231		SNG232 SNG233		J	N	U
Dual 4-Input NAND Gates	SNG240 SNG241	11 6	SNG242 SNG243	9 5	J	N	U
Expandable 2-2-2-3-Input AND-OR-INVERT Gates	SNG250 SNG251	11 6	SNG252 SNG253	9 5	J	N	U
8-Input NAND Gates	SNG260 SNG261	11 6	SNG262 SNG263	9 5	J	N	U
Dual 4-Input Expanders for AND-OR-INVERT Gates	SNG270 SNG271		SNG272 SNG273		J	N	U
OR-Expandable Dual 4-Input AND Gates	SNG280 SNG281	15 7	SNG282 SNG283	12 6	J	N	U
Dual 2-3-Input Expanders for OR Expandable AND Gates	SNG290 SNG291		SNG292 SNG293		J	N	U
Expandable 3-Wide 3-Input AND-OR-INVERT Gates	SNG300 SNG301	11 6	SNG302 SNG303	9 5	J	N	U
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gates	SNG310 SNG311	11 6	SNG312 SNG313	9 5	J	N	U
Triple 3-Input NAND Gates	SNG320 SNG321	11 6	SNG322 SNG323	9 5	J	N	U
Quadruple 2-Input NAND Lamp/Line Drivers	SNG351	30	SNG353	24	J	N	U

MOS/LSI CIRCUITS
FUNCTIONAL INDEX

B

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CROSS-REFERENCE GUIDE

(alphabetically by manufacturers)

Direct replacements were selected as pin-for-pin equivalent circuits based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangability in particular applications is not guaranteed. Before using a substitute, the user should compare the specifications of the substitute device with the detailed specifications of the original device.

B

TI makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained in this list.

LINEAR CIRCUITS

Fairchild

Type Number	Direct TI Replacement	Nearest TI Replacement	Sec.
UA702	SN52702		3
UA702C	SN72702		3
UA703		SN76603	3
UA703C	SN76603		3
UA708		SN76665	3
UA709	SN52709		3
UA709C	SN72709		3
UA709A	SN52709A		3
UA710	SN52710		3
UA710C	SN72710		3
UA710A		SN52810	3
UA711	SN52711		3
UA711C	SN72711		3
UA715		SN5511	3
UA715C		SN7511	3
UA719		SN76619	3
UA719C	SN76619		3
UA723		SN72400	3
UA723C		SN72400	3
UA729C		SN76110	3
UA730		SN5510	3
UA730C		SN7510	3
UA732C		SN76110	3
UA733	SN52733		3
UA733C	SN72733		3

Type Number	Direct TI Replacement	Nearest TI Replacement	Sec.
UA739C	SN76131		3
UA740		SN52770	3
UA740C		SN72770	3
UA741	SN52741		3
UA741C	SN72741		3
UA746C	SN76246		3
UA747	SN52747		3
UA747C	SN72747		3
UA748	SN52748		3
UA748C	SN72748		3
UA749		SN52747	3
UA749C		SN72747	3
UA751C		SN7510	3
UA754C		SN76665	3
UA761C	SN7524		3
UA767	SN76110		3
UA796		SN56514	3
UA796C		SN76514	3
9614	SN75114		3
9615	SN75115		3
9620	SN75120		3
9621		SN75109	3
9622		SN75107	3
9624		SN75450	3
9625		SN75450	3

Motorola

Type Number	Direct TI Replacement	Nearest TI Replacement	Sec.
MC130L		SN76131	3
MC1304P	SN76104		3
MC1305P	SN76105		3
MC1306P		SN76010	3
MC1307P	SN76110		3
MC1316P		SN76003	3
MC1325P		SN76246	3
MC1326P		SN76246	3
MC1328P	SN76246		3
MC1330P	SN76530		3
MC1350P	SN76600		3
MC1351P		SN76665	3
MC1352P	SN76650		3
MC1357	SN76642		3
MC1410	SN7510		3
MC1414L	SN72514		3
MC1429G		SN7511	3
MC1430		SN72702	3
MC1431		SN72702	3
MC1433		SN72709	3
MC1439		SN72748	3
MC1440		SN7524	3

Type Number	Direct TI Replacement	Nearest TI Replacement	Sec.
MC1441		SN7520	3
MC1454G		SN76010	3
MC1455G	SN72771		3
MC1458	SN72558		3
MC1460		SN72400	3
MC1461		SN72400	3
MC1488L		SN75150	3
MC1489L		SN75154	3
MC1509		SN5510	3
MC1510	SN5510		3
MC1514L	SN52514		3
MC1520		SN5511	3
MC1524G		SN76010	3
MC1525G		SN52733	3
MC1526G		SN52733	3
MC1529G		SN5511	3
MC1530		SN52702	3
MC1531		SN52702	3
MC1533		SN52709	3
MC1539		SN52748	3
MC1540		SN5524	3
MC1541		SN5520	3

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

LINEAR CIRCUITS

Motorola, Cont.

Type Number	Direct TI Replacement	Nearest TI Replacement	Sec.
MC1552G		SN52733	3
MC1553G		SN52733	3
MC1554G		SN76010	3
MC1556G	SN52771		3
MC1558	SN52558		3
MC1560		SN72400	3
MC1561		SN72400	3
MC1580L		SN55107-110	3
MC1582L		SN55109-110	3
MC1583L		SN55108	3
MC1584L		SN55107	3
MC1590G	SN76600		3
MC1596G		SN56514L	3
MC1709	SN52709		3
MC1709C	SN72709		3
MC1710	SN52710		3
MC1710C	SN72710		3
MC1711	SN52711		3
MC1711C	SN72711		3
MC1712	SN52702		3
MC1712C	SN72702		3
MC1723		SN72400	3
MC1741	SN52741		3
MC1741C	SN72741		3
MC7520	SN7520		3
MC7521	SN7521		3
MC7524	SN7524		3
MC7525	SN7525		3
MCH1439G		SN72741	3
MCH1539G		SN52741	3
MFC4000P		SN76010	3
MFC4010P		SN7514	3
MFC6000		SN76010	3
MFC6010		SN76641	3
MFC8000P		SN76131	3
MFC8001P		SN76131	3
MFC8002P		SN76131	3
MFC8010		SN76010	3
MFC9000		SN76005	3
MFC9010		SN76005	3

National

Type Number	Direct TI Replacement	Nearest TI Replacement	Sec.
LH101	SN52741		3
LM101	SN52748		3
LM101A	SN52101A		3
LM106	SN52106		3
LM107	SN52107		3
LM108		SN52770	3
LM111		SN52810	3
LM112		SN52771	3
LH201	SN52741		3
LM201	SN52748		3
LM201A	SN52101A		3
LM205		SN72400	3
LM206	SN52106		3
LM207	SN52107		3
LM208		SN52770	3
LM211		SN52810	3
LM212		SN52771	3
LM301A	SN72301A		3
LM305		SN72400	3
LM305A		SN72400	3
LM306	SN72306		3
LM307	SN72307		3
LM308		SN72770	3
LM311		SN72810	3
LM312		SN72771	3
LM1304	SN76104		3
LM1458	SN72558		3
LM1558	SN52558		3
LM3065	SN76665		3
LM709	SN52709		3
LM709A	SN52709A		3
LM709C	SN72709		3
LM709CN	SN72709N		3
LM710	SN52710		3
LM710A		SN52810	3
LM710C	SN72710		3
LM710CN	SN72710N		3
LM711	SN52711		3
LM711C	SN72711		3
LM711CN	SN72711N		3
LM723		SN72400	3
LM723C		SN72400	3
LM741	SN52741		3
LM741C	SN72741		3
LM741CN	SN72741N		3
LM747	SN52747		3
LM747D	SN52747J		3
LM747C	SN72747		3
LM747CD	SN72747J		3
LM747CN	SN72747N		3
LM748	SN52748		3
LM748C	SN72748		3
LM5520D	SN5520J		3
LM5521D	SN5521J		3
LM5522D	SN5522J		3
LM5523D	SN5523J		3
LM5524D	SN5524J		3
LM5525D	SN5525J		3
LM5528D	SN5528J		3
LM5529D	SN5529J		3
LM7520D	SN7520J		3
LM7520N	SN7520N		3
LM7521D	SN7521J		3
LM7521N	SN7521N		3
LM7522D	SN7522J		3
LM7522N	SN7522N		3
LM7523D	SN7523J		3
LM7523N	SN7523N		3
LM7524D	SN7524J		3
LM7524N	SN7524N		3
LM7525D	SN7525J		3
LM7525N	SN7525N		3
LM7528D	SN7528J		3
LM7528N	SN7528N		3

B

National, Cont.

Type Number	Direct TI Replacement	Nearest TI Replacement	Sec.
LM7529D	SN7529J		3
LM7529N	SN7529N		3
LM7534	SN75234		3
LM7535	SN75235		3
LM7538	SN75238		3
LM7539	SN75239		3
DM7800		SN75450	3
DM7820		SN55115	3
DM7830		SN55114	3
DM8800		SN75450	3
DM8820		SN75115	3
DM8822		SN75154	3
DM8830		SN75114	3
DM8831		SN75113	3
DM8832		SN75150	3
NH0002	HIC037		15
NH0006		SN75451	3
NH0006C		SN75451L	3
NH0006CN		SN75451P	3
NH0008		HIC040	15
NH0008C		HIC040	15
NH0008CN		HIC040	15
NH0011		SN75451	3
NH0011C		SN75451	3
NH0011CN		SN75451	3
NH0016CN		SN75451	3
NH0017CN		HIC040	15
NH0018CN		HIC040	15

Signetics

Type Number	Direct TI Replacement	Nearest TI Replacement	Sec.
N5101A	SN72748N		3
N5101T	SN72748L		3
N5101V	SN72748P		3
N5111A	SN76643		3
N5556T	SN72771L		3
N5556V	SN72771P		3
N5558T	SN72558L		3
N5558V	SN72558P		3
N5596A		SN76514N	3
N5709A	SN72709N		3
N5709T	SN72709L		3
N5710A	SN72710N		3
N5710T	SN72710L		3
N5711A	SN72711N		3
N5711T	SN72711L		3
N5723A		SN72400N	3
N5723L		SN72400N	3
N5733A	SN72733N		3
N5733K	SN72733L		3
N5741A	SN72741N		3
N5741T	SN72741L		3
N5741V	SN72741P		3
N5748A	SN72748N		3
N5748T	SN72748L		3
N5748V	SN72748P		3
N7520B	SN7520N		3
N7521B	SN7521N		3
N7522B	SN7522N		3
N7523B	SN7523N		3
N7524B	SN7524N		3
N7525B	SN7525N		3
S5101T	SN52748L		3
S5556T	SN52771L		3
S5558T	SN52558L		3
S5596T		SN56514L	3
S5709T	SN52709L		3
S5710T	SN52710L		3
S5711T	SN52711L		3
S5723L		SN72400N	3
S5733K	SN52733L		3
S5741T	SN52741L		3
S5748T	SN52748L		3
NE501		SN7511	3
NE510		SN76600	3
NE511B		SN76600	3
NE515		SN7511	3
NE516		SN7511	3
NE518		SN75107	3
NE525		SN7524	3
NE526		SN75107	3
NE550L		SN72400N	3
SE501		SN5511	3
SE510		SN76600	3
SE511B		SN76600	3
SE515		SN5511	3
SE516		SN5511	3
SE518		SN55107	3
SE526		SN55107	3
SE550L		SN72400N	3
8T15		SN75150	3
8T16		SN75154	3

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DTL/TTL CIRCUITS

Fairchild DTL

Type Number	Direct Replacement	Recommended for New Designs	Sec.
U3I909351X	SN159093U	SN5473W	6
U3I909359X	SN158093U	SN7473W	6
U3I909451X	SN159094U	SN5473W	6
U3I909459X	SN158094U	SN7473W	6
U3I909751X	SN159097U	SN5476W	6
U3I909759X	SN158097U	SN7476W	6
U3I909951X	SN159099U	SN5476W	6
U3I909959X	SN158099U	SN7476W	6
U3I993051X	SN15930U	SN5420W	6
U3I993059X	SN15830U	SN7420W	6
U3I993151X	SN15931U	SN54110W	6
U3I993159X	SN15831U	SN74110W	6
U3I993251X	SN15932U	SN5440W	6
U3I993259X	SN15832U	SN7440W	6
U3I993351X	SN15933U	SN5460W	6
U3I993359X	SN15833U	SN7460W	6
U3I993551X	SN15935U	SN5405W	6
U3I993559X	SN15835U	SN7405W	6
U3I993651X	SN15936U	SN5405W	6
U3I993659X	SN15836U	SN7405W	6
U3I993751X	SN15937U	SN5405W	6
U3I993759X	SN15837U	SN7405W	6
U3I994451X	SN15944U	SN5440W	6
U3I994459X	SN15844U	SN7440W	6
U3I994551X	SN15945U	SN54110W	6
U3I994559X	SN15845U	SN74110W	6
U3I994651X	SN15946U	SN5400W	6
U3I994659X	SN15846U	SN7400W	6
U3I994851X	SN15948U	SN54110W	6
U3I994859X	SN15848U	SN74110W	6
U3I994951X	SN15949U	SN5400W	6
U3I994959X	SN15849U	SN7400W	6
U3I995051X	SN15950U	SN54H101W	7
U3I995059X	SN15850U	SN74H101W	7
U3I995151X	SN15951U	SN54121W	6
U3I995159X	SN15851U	SN74121W	6
U3I996151X	SN15961U	SN5420W	6
U3I996159X	SN15861U	SN7420W	6
U3I996251X	SN15962U	SN5410W	6
U3I996259X	SN15862U	SN7410W	6
U3I996351X	SN15963U	SN5410W	6
U3I996359X	SN15863U	SN7410W	6

Type Number	Direct Replacement	Recommended for New Designs	Sec.
U6A909351X	SN159093J, N	SN5473J, N	6
U6A909359X	SN158093J, N	SN7473J, N	6
U6A909451X	SN159094J, N	SN5473J, N	6
U6A909459X	SN158094J, N	SN7473J, N	6
U6A909751X	SN159097J, N	SN5476J, N	6
U6A909759X	SN158097J, N	SN7476J, N	6
U6A909951X	SN159099J, N	SN5476J, N	6
U6A909959X	SN158099J, N	SN7476J, N	6
U6A993051X	SN15930J, N	SN5420J, N	6
U6A993059X	SN15830J, N	SN7420J, N	6
U6A993151X	SN15931J, N	SN54110J, N	6
U6A993159X	SN15831J, N	SN74110J, N	6
U6A993251X	SN15932J, N	SN5440J, N	6
U6A993259X	SN15832J, N	SN7440J, N	6
U6A993351X	SN15933J, N	SN5460J, N	6
U6A993359X	SN15833J, N	SN7460J, N	6
U6A993551X	SN15935J, N	SN5405J, N	6
U6A993559X	SN15835J, N	SN7405J, N	6
U6A993651X	SN15936J, N	SN5405J, N	6
U6A993659X	SN15836J, N	SN7405J, N	6
U6A993751X	SN15937J, N	SN5405J, N	6
U6A993759X	SN15837J, N	SN7405J, N	6
U6A994451X	SN15944J, N	SN5440J, N	6
U6A994459X	SN15844J, N	SN7440J, N	6
U6A994551X	SN15945J, N	SN54110J, N	6
U6A994559X	SN15845J, N	SN74110J, N	6
U6A994651X	SN15946J, N	SN5400J, N	6
U6A994659X	SN15846J, N	SN7400J, N	6
U6A994851X	SN15948J, N	SN54110J, N	6
U6A994859X	SN15848J, N	SN74110J, N	6
U6A994951X	SN15949J, N	SN5400J, N	6
U6A994959X	SN15849J, N	SN7400J, N	6
U6A995051X	SN15950J, N	SN54H101J, N	7
U6A995059X	SN15850J, N	SN74H101J, N	7
U6A995151X	SN15951J, N	SN54121J, N	6
U6A995159X	SN15851J, N	SN74121J, N	6
U6A996151X	SN15961J, N	SN5420J, N	6
U6A996159X	SN15861J, N	SN7420J, N	6
U6A996251X	SN15962J, N	SN5410J, N	6
U6A996259X	SN15862J, N	SN7410J, N	6
U6A996351X	SN15963J, N	SN5410J, N	6
U6A996359X	SN15863J, N	SN7410J, N	6

Fairchild TTL

Type Number	Direct Replacement	Recommended for New Designs	Sec.
A3I9033512	SN5481W	SN5489W	9
A3I9033591	SN7481W	SN7489W	9
A3I9033592	SN7481W	SN7489W	9
A4L410359X	SN7489W	SN7489W	9
A6A9033512	SN5481W	SN5489W	9
A6A9033591	SN7481W	SN7489W	9
A6A9033592	SN7481W	SN7489W	9
A7B410359X	SN7489J, N	SN7489J, N	9
A7B9034A1B	SN5488AW	SN5488AW	9
A7B9034A9B	SN7488AW	SN7488AW	9
U3I540051X	SN5400W	SN5400W	6
U3I540151X	SN5401W	SN5401W	6
U3I540251X	SN5402W	SN5402W	6
U3I540451X	SN5404W	SN5404W	6
U3I540551X	SN5405W	SN5405W	6

Type Number	Direct Replacement	Recommended For New Designs	Sec.
U3I540851X	SN5408W	SN5408W	6
U3I5410451X	SN54104W	SN54104W	6
U3I541051X	SN5410W	SN5410W	6
U3I5410551X	SN54105W	SN54105W	6
U3I542051X	SN5420W	SN5420W	6
U3I543051X	SN5430W	SN5430W	6
U3I544051X	SN5440W	SN5440W	6
U3I544951X	SN5449W	SN5449W	9
U3I545051X	SN5450W	SN5450W	6
U3I545151X	SN5451W	SN5451W	6
U3I545351X	SN5453W	SN5453W	6
U3I545451X	SN5454W	SN5454W	6
U3I546051X	SN5460W	SN5460W	6
U3I547051X	SN5470W	SN5470W	6
U3I547251X	SN5472W	SN5472W	6

Fairchild TTL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
U3I547351X	SN5473W	SN5473W	6
U3I547451X	SN5474W	SN5474W	6
U3I547751X	SN5477W	SN5477W	9
U3I548051X	SN5480W	SN5480W	9
U31548251X	SN5482W	SN5482W	9
U31548651X	SN5486W	SN5486W	9
U3I549051X	SN5490W	SN5490W	9
U3I549151X	SN5491AW	SN5491AW	9
U3I549251X	SN5492W	SN5492W	9
U3I549351X	SN5493W	SN5493W	9
U3I549551X	SN5495AW	SN5495AW	9
U3I740059X	SN7400W	SN7400W	6
U3I740159X	SN7401W	SN7401W	6
U3I740459X	SN7404W	SN7404W	6
U3I740559X	SN7405W	SN7405W	6
U3I740859X	SN7408W	SN7408W	6
U3I7410459X	SN74104W	SN74104W	6
U3I7410559X	SN74105W	SN74105W	6
U3I741059X	SN7410W	SN7410W	6
U3I742059X	SN7420W	SN7420W	6
U3I743059X	SN7430W	SN7430W	6
U3I744059X	SN7440W	SN7440W	6
U3I744959X	SN7449W	SN7449W	9
U3I745059X	SN7450W	SN7450W	6
U3I745159X	SN7451W	SN7451W	6
U3I745359X	SN7453W	SN7453W	6
U3I745459X	SN7454W	SN7454W	6
U3I746059X	SN7460W	SN7460W	6
U3I747059X	SN7470W	SN7470W	6
U3I747259X	SN7472W	SN7472W	6
U3I747359X	SN7473W	SN7473W	6
U3I747459X	SN7474W	SN7474W	6
U3I747759X	SN7477W	SN7477W	9
U3I748059X	SN7480W	SN7480W	9
U31748259X	SN7482W	SN7482W	9
U3I748659X	SN7486W	SN7486W	9
U3I749059X	SN7490W	SN7490W	9
U3I749159X	SN7491AW	SN7491AW	9
U3I749259X	SN7492W	SN7492W	9
U3I749359X	SN7493W	SN7493W	9
U3I749559X	SN7495AW	SN7495AW	9
U3I9N0051X	SN5400W	SN5400W	6
U3I9N0059X	SN7400W	SN7400W	6
U3I9N0151X	SN5401W	SN5401W	6
U3I9N0159X	SN7401W	SN7401W	6
U3I9N0251X	SN5402W	SN5402W	6
U3I9N0259X	SN7402W	SN7402W	6
U3I9N0451X	SN5404W	SN5404W	6
U3I9N0459X	SN7404W	SN7404W	6
U3I9N0551X	SN5405W	SN5405W	6
U3I9N0559X	SN7405W	SN7405W	6
U3I9N0851X	SN5408W	SN5408W	6
U3I9N0859X	SN7408W	SN7408W	6
U3I9N10451X	SN54104W	SN54104W	6
U3I9N10459X	SN74104W	SN74104W	6
U3I9N1051X	SN5410W	SN5410W	6
U3I9N10551X	SN54105W	SN54105W	6
U3I9N10559X	SN74105W	SN74105W	6
U3I9N1059X	SN7410W	SN7410W	6
U3I9N2051X	SN5420W	SN5420W	6
U3I9N2059X	SN7420W	SN7420W	6
U3I9N3051X	SN5430W	SN5430W	6
U3I9N3059X	SN7430W	SN7430W	6
U3I9N4051X	SN5440W	SN5440W	6
U3I9N4059X	SN7440W	SN7440W	6
U3I9N5051X	SN5450W	SN5450W	6
U3I9N5059X	SN7450W	SN7450W	6

Type Number	Direct Replacement	Recommended for New Designs	Sec.
U3I9N5151X	SN5451W	SN5451W	6
U3I9N5159X	SN7451W	SN7451W	6
U3I9N5351X	SN5453W	SN5453W	6
U3I9N5359X	SN7453W	SN7453W	6
U3I9N5451X	SN5454W	SN5454W	6
U3I9N5459X	SN7454W	SN7454W	6
U3I9N6051X	SN5460W	SN5460W	6
U3I9N6059X	SN7460W	SN7460W	6
U3I9N7051X	SN5470W	SN5470W	6
U3I9N7059X	SN7470W	SN7470W	6
U3I9N7251X	SN5472W	SN5472W	6
U3I9N7259X	SN7472W	SN7472W	6
U3I9N7351X	SN5473W	SN5473W	6
U3I9N7359X	SN7473W	SN7473W	6
U3I9N7451X	SN5474W	SN5474W	6
U3I9N7459X	SN7474W	SN7474W	6
U3I9N8651X	SN5486W	SN5486W	9
U3I9N8659X	SN7486W	SN7486W	9
U3I900051X	SN54104W	SN54104W	6
U3I900059X	SN74104W	SN74104W	6
U31900151X	SN54105W	SN54105W	6
U3I900159X	SN74105W	SN74105W	6
U3I900251X		SN5400W	6
U3I900259X		SN7400W	6
U3I900351X		SN5410W	6
U3I900359X		SN7410W	6
U3I900451X		SN5420W	6
U3I900459X		SN7420W	6
U3I900551X		SN5450W	6
U3I900559X		SN7450W	6
U3I900651X		SN5460W	6
U3I900659X		SN7460W	6
U3I900751X		SN5430W	6
U3I900759X		SN7430W	6
U3I900851X		SN5453W	6
U3I900859X		SN7453W	6
U3I900951X		SN5440W	6
U3I900959X		SN7440W	6
U3I901251X		SN5401W	6
U3I901259X		SN7401W	6
U3I901651X		SN5404W	6
U3I901659X		SN7404W	6
U3I901751X		SN5405W	6
U3I901759X		SN7405W	6
U3I935951X	SN5449W	SN5449W	9
U3I935959X	SN7449W	SN7449W	9
U3I937751X	SN5477W	SN5477W	9
U3I937759X	SN7477W	SN7477W	9
U3I938051X	SN5480W	SN5480W	9
U3I938059X	SN7480W	SN7480W	9
U3I938251X	SN5482W	SN5482W	9
U3I938259X	SN7482W	SN7482W	9
U3I939051X	SN5490W	SN5490W	9
U31939059X	SN7490W	SN7490W	9
U3I939151X	SN5491AW	SN5491AW	9
U3I939159X	SN7491AW	SN7491AW	9
U3I939251X	SN5492W	SN5492W	9
U3I939259X	SN7492W	SN7492W	9
U3I939351X	SN5493W	SN5493W	9
U3I939359X	SN7493W	SN7493W	9
U3I939551X	SN5495AW	SN5495AW	9
U3I939559X	SN7495W	SN7495W	9
U3I960051X		SN54122W	6
U3I960059X		SN74122W	6
U3I960151X	SN54122W	SN54122W	6
U3I960159X	SN74122W	SN74122W	6
U4L5418251X	SN54182W	SN54182W	9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DTL/TTL CIRCUITS

Fairchild TTL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
U4L5419251X	SN54192W	SN54192W	9
U4L5419351X	SN54193W	SN54193W	9
U4L548351X	SN5483W	SN5483W	9
U4L549451X	SN5494W	SN5494W	9
U4L549651X	SN5496W	SN5496W	9
U4L7418259X	SN74182W	SN74182W	9
U4L7419259X	SN74192W	SN74192W	9
U4L7419359X	SN74193W	SN74193W	9
U4L901451X		SN5486W	9
U4L901459X		SN7486W	9
U4L902051X		SN54111W	6
U4L902059X		SN74111W	6
U4L902251X		SN54111W	6
U4L902259X		SN74111W	6
U4L902451X		SN54111W	6
U4L902459X		SN74111W	6
U4L930051X	SN54195W	SN54195W	9
U4L930059X	SN74195W	SN75195W	9
U4L930151X		SN5442W	9
U4L930159X		SN7442W	9
U4L930451X		SN5482W	9
U4L930459X		SN7482W	9
U4L930651X		SN54190W	9
U4L930659X		SN74190W	9
U4L930751X	SN5448W	SN5448W	9
U4L930759X	SN7448W	SN7448W	9
U4L930951X		SN54153W	9
U4L930959X		SN74153W	9
U4L931051X	SN54160W	SN54160W	9
U4L931059X	SN74160W	SN74160W	9
U4L931251X		SN54151W	9
U4L931259X		SN74151W	9
U4L931451X		SN5475W	9
U4L931459X		SN7475W	9
U4L931559X	SN74141W	SN74141W	9
U4L931651X	SN54161W	SN54163W	9
U4L931659X	SN74161W	SN74163W	9
U4L9317511	SN5446AW	SN5446AW	9
U4L9317512	SN5447AW	SN5447AW	9
U4L9317513	SN5446AW	SN5446AW	9
U4L9317514	SN5447AW	SN5447AW	9
U4L9317591	SN7446AW	SN7446AW	9
U4L9317592	SN7447AW	SN7447AW	9
U4L9317593	SN7446AW	SN7446AW	9
U4L9317594	SN7447AW	SN7447AW	9
U4L932151X		SN54153W	9
U4L932159X		SN74153W	9
U4L932251X		SN54153W	9
U4L932259X		SN74153W	9
U4L932451X		SN5485W	9
U4L932459X		SN7485W	9
U4L932559X	SN74141W	SN74141W	9
U4L9327511	SN5448W	SN5448W	9
U4L9327512	SN5448W	SN5448W	9
U4L9327591	SN7448W	SN7448W	9
U4L9327592	SN7448W	SN7448W	9
U4L932851X		SN5491AW	9
U4L932859X		SN7491AW	9
U4L934251X	SN54182W	SN54182W	9
U4L934259X	SN74182W	SN74182W	9
U4L934851X		SN54180W	9
U4L934859X		SN74180W	9
U4L936051X	SN54192W	SN54192W	9
U4L936059X	SN74192W	SN74192W	9
U4L936651X	SN54193W	SN54193W	9
U4L936659X	SN74193W	SN74193W	9
U4L960251X		SN54123W	6
U4L960259X		SN74123W	6
U4M5418151X	SN54181W	SN54181W	9
U4M7418159X	SN74181W	SN74181W	9
U4M931151X		SN54150W	9
U4M931159X		SN74150W	9
U4M934051X		SN54181W	9
U4M934059X		SN74181W	9
U4M934151X	SN54181W	SN54181W	9
U4M934159X	SN74181W	SN74181W	9
U6A540051X	SN5400J, N	SN5400J, N	6
U6A540151X	SN5401J, N	SN5401J, N	6
U6A540251X	SN5402J, N	SN5402J, N	6
U6A540351X	SN5403J, N	SN5403J, N	6
U6A540451X	SN5404J, N	SN5404J, N	6
U6A540551X	SN5405J, N	SN5405J, N	6
U6A540851X	SN5408J, N	SN5408J, N	6
U6A5410451X	SN54104J, N	SN54104J, N	6
U6A541051X	SN5410J, N	SN5410J, N	6
U6A5410551X	SN54105J, N	SN54105J, N	6
U6A5410751X	SN54107J, N	SN54107J, N	6
U6A542051X	SN5420J, N	SN5420J, N	6
U6A543051X	SN5430J, N	SN5430J, N	6
U6A544051X	SN5440J, N	SN5440J, N	6
U6A545051X	SN5450J, N	SN5450J, N	6
U6A545151X	SN5451J, N	SN5451J, N	6
U6A545351X	SN5453J, N	SN5453J, N	6
U6A545451X	SN5454J, N	SN5454J, N	6
U6A546051X	SN5460J, N	SN5460J, N	6
U6A547051X	SN5470J, N	SN5470J, N	6
U6A547251X	SN5472J, N	SN5472J, N	6
U6A547351X	SN5473J, N	SN5473J, N	6
U6A547451X	SN5474J, N	SN5474J, N	6
U6A548051X	SN5480J, N	SN5480J, N	9
U6A548251X	SN5482J, N	SN5482J, N	9
U6A548651X	SN5486J, N	SN5486J, N	9
U6A549051X	SN5490J, N	SN5490J, N	9
U6A549151X	SN5491AJ, N	SN5491AJ, N	9
U6A549251X	SN5492J, N	SN5492J, N	9
U6A549351X	SN5493J, N	SN5493J, N	9
U6A549551X	SN5495AJ, N	SN5495AJ, N	9
U6A740059X	SN7400J, N	SN7400J, N	6
U6A740159X	SN7401J, N	SN7401J, N	6
U6A740259X	SN7402J, N	SN7402J, N	6
U6A740359X	SN7403J, N	SN7403J, N	6
U6A740459X	SN7404J, N	SN7404J, N	6
U6A740559X	SN7405J, N	SN7405J, N	6
U6A740859X	SN7408J, N	SN7408J, N	6
U6A7410459X	SN74104J, N	SN74104J, N	6
U6A7410559X	SN74105J, N	SN74105J, N	6
U6A741059X	SN7410J, N	SN7410J, N	6
U6A7410759X	SN74107J, N	SN74107J, N	6
U6A742059X	SN7420J, N	SN7420J, N	6
U6A743059X	SN7430J, N	SN7430J, N	6
U6A744059X	SN7440J, N	SN7440J, N	6
U6A745059X	SN7450J, N	SN7450J, N	6
U6A745159X	SN7451J, N	SN7451J, N	6
U6A745359X	SN7453J, N	SN7453J, N	6
U6A745459X	SN7454J, N	SN7454J, N	6
U6A746059X	SN7460J, N	SN7460J, N	6
U6A747059X	SN7470J, N	SN7470J, N	6
U6A747259X	SN7472J, N	SN7472J, N	6
U6A747359X	SN7473J, N	SN7473J, N	6
U6A747459X	SN7474J, N	SN7474J, N	6
U6A748059X	SN7480J, N	SN7480J, N	9
U6A748259X	SN7482J, N	SN7482J, N	9
U6A748659X	SN7486J, N	SN7486J, N	9
U6A749059X	SN7490J, N	SN7490J, N	9

Fairchild TTL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
U6A749159X	SN7491AJ, N	SN7491AJ, N	9
U6A749259X	SN7492J, N	SN7492J, N	9
U6A749359X	SN7493J, N	SN7493J, N	9
U6A749559X	SN7495AJ, N	SN7495AJ, N	9
U6A9N0051X	SN5400J, N	SN5400J, N	6
U6A9N0059X	SN7400J, N	SN7400J, N	6
U6A9N0151X	SN5401J, N	SN5401J, N	6
U6A9N0159X	SN7401J, N	SN7401J, N	6
U6A9N0251X	SN5402J, N	SN5402J, N	6
U6A9N0259X	SN7402J, N	SN7402J, N	6
U6A9N0351X	SN5403J, N	SN5403J, N	6
U6A9N0359X	SN7403J, N	SN7403J, N	6
U6A9N0451X	SN5404J, N	SN5404J, N	6
U6A9N0459X	SN7404J, N	SN7404J, N	6
U6A9N0551X	SN5405J, N	SN5405J, N	6
U6A9N0559X	SN7405J, N	SN7405J, N	6
U6A9N0851X	SN5408J, N	SN5408J, N	6
U6A9N0859X	SN7408J, N	SN7408J, N	6
U6A9N10451X	SN54104J, N	SN54104J, N	6
U6A9N10459X	SN74104J, N	SN74104J, N	6
U6A9N1051X	SN5410J, N	SN5410J, N	6
U6A9N10551X	SN54105J, N	SN54105J, N	6
U6A9N10559X	SN74105J, N	SN74105J, N	6
U6A9N1059X	SN7410J, N	SN7410J, N	6
U6A9N10751X	SN54107J, N	SN54107J, N	6
U6A9N10759X	SN74107J, N	SN74107J, N	6
U6A9N2051X	SN5420J, N	SN5420J, N	6
U6A9N2059X	SN7420J, N	SN7420J, N	6
U6A9N3051X	SN5430J, N	SN5430J, N	6
U6A9N3059X	SN7430J, N	SN7430J, N	6
U6A9N4051X	SN5440J, N	SN5440J, N	6
U6A9N4059X	SN7440J, N	SN7440J, N	6
U6A9N5051X	SN5450J, N	SN5450J, N	6
U6A9N5059X	SN7450J, N	SN7450J, N	6
U6A9N5151X	SN5451J, N	SN5451J, N	6
U6A9N5159X	SN7451J, N	SN7451J, N	6
U6A9N5351X	SN5453J, N	SN5453J, N	6
U6A9N5359X	SN7453J, N	SN7453J, N	6
U6A9N5451X	SN5454J, N	SN5454J, N	6
U6A9N5459X	SN7454J, N	SN7454J, N	6
U6A9N6051X	SN5460J, N	SN5460J, N	6
U6A9N6059X	SN7460J, N	SN7460J, N	6
U6A9N7051X	SN5470J, N	SN5470J, N	6
U6A9N7059X	SN7470J, N	SN7470J, N	6
U6A9N7251X	SN5472J, N	SN5472J, N	6
U6A9N7259X	SN7472J, N	SN7472J, N	6
U6A9N7351X	SN5473J, N	SN5473J, N	6
U6A9N7359X	SN7473J, N	SN7473J, N	6
U6A9N7451X	SN5474J, N	SN5474J, N	6
U6A9N7459X	SN7474J, N	SN7474J, N	6
U6A9N8651X	SN5486J, N	SN5486J, N	9
U6A9N8659X	SN7486J, N	SN7486J, N	9
U6A900051X	SN54104J, N	SN54104J, N	6
U6A900059X	SN74104J, N	SN74104J, N	6
U6A900151X	SN54105J, N	SN54105J, N	6
U6A900159X	SN74105J, N	SN74105J, N	6
U6A900251X	SN5400J, N	SN5400J, N	6
U6A900259X	SN7400J, N	SN7400J, N	6
U6A900351X	SN5410J, N	SN5410J, N	6
U6A900359X	SN7410J, N	SN7410J, N	6
U6A900451X	SN5420J, N	SN5420J, N	6
U6A900459X	SN7420J, N	SN7420J, N	6
U6A900551X	SN5450J, N	SN5450J, N	6
U6A900559X	SN7450J, N	SN7450J, N	6
U6A900651X	SN5460J, N	SN5460J, N	6
U6A900659X	SN7460J, N	SN7460J, N	6
U6A900751X		SN5430J, N	6

Type Number	Direct Replacement	Recommended for New Designs	Sec.
U6A900759X		SN7430J, N	6
U6A900851X	SN54H53J, N	SN5453J, N	6
U6A900859X	SN74H53J, N	SN7453J, N	6
U6A900951X	SN5440J, N	SN5440J, N	6
U6A900959X	SN7440J, N	SN7440J, N	6
U6A901251X	SN5403J, N	SN5401J, N	6
U6A901259X	SN7403J, N	SN7401J, N	6
U6A901651X	SN5404J, N	SN5404J, N	6
U6A901659X	SN7404J, N	SN7404J, N	6
U6A901751X	SN5405J, N	SN5405J, N	6
U6A901759X	SN7405J, N	SN7405J, N	6
U6A938051X	SN5480J, N	SN5480J, N	9
U6A938059X	SN7480J, N	SN7480J, N	9
U6A938251X	SN5482J, N	SN5482J, N	9
U6A938259X	SN7482J, N	SN7482J, N	9
U6A939051X	SN5490J, N	SN5490J, N	9
U6A939059X	SN7490J, N	SN7490J, N	9
U6A939151X	SN5491AJ, N	SN5491AJ, N	9
U6A939159X	SN7491AJ, N	SN7491AJ, N	9
U6A939251X	SN5492J, N	SN5492J, N	9
U6A939259X	SN7492J, N	SN7492J, N	9
U6A939351X	SN5493J, N	SN5493J, N	9
U6A939359X	SN7493J, N	SN7493J, N	9
U6A939551X	SN5495AJ, N	SN5495AJ, N	9
U6A939559X	SN7495AJ, N	SN7495AJ, N	9
U6A960051X		SN54122J, N	6
U6A960059X		SN74122J, N	6
U6A960151X	SN54122J, N	SN54122J, N	6
U6A960159X	SN74122J, N	SN74122J, N	6
U6B9N7651X	SN5476J, N	SN5476J, N	6
U6B9N7659X	SN7476J, N	SN7476J, N	6
U6B547551X	SN5475J, N	SN5475J, N	9
U6B547651X	SN5476J, N	SN5476J, N	6
U6B548351X	SN5483J, N	SN5483J, N	9
U6B7414159X	SN74141J, N	SN74141J, N	9
U6B744159X	SN74141J, N	SN74141J, N	9
U6B747559X	SN7475J, N	SN7475J, N	9
U6B747659X	SN7476J, N	SN7476J, N	6
U6B748359X	SN7483J, N	SN7483J, N	9
U6B901451X		SN5486J, N	9
U6B901459X		SN7486J, N	9
U6B901551X		SN5402J, N	6
U6B901559X		SN7402J, N	6
U6B930451X		SN5482J, N	9
U6B930459X		SN7482J, N	9
U6B930751X	SN5448J, N	SN5448J, N	9
U6B930759X	SN7448J, N	SN7448J, N	9
U6B930951X		SN54153J, N	9
U6B930959X		SN74153J, N	9
U6B931559X	SN74141J, N	SN74141J, N	9
U6B932559X	SN74141J, N	SN74141J, N	9
U6B934851X		SN54180J, N	9
U6B934859X		SN74180J, N	9
U6B937551X	SN5475J, N	SN5475J, N	9
U6B937559X	SN7475J, N	SN7475J, N	9
U6B938351X	SN5483J, N	SN5483J, N	9
U6B938359X	SN7483J, N	SN7483J, N	9
U6N5418151X	SN54181J, N	SN54181J, N	9
U6N7418159X	SN74181J, N	SN74181J, N	9
U6N930651X		SN54190J, N	9
U6N930659X		SN74190J, N	9
U6N931151X	SN54154J, N	SN54154J, N	9
U6N931159X	SN74154J, N	SN74154J, N	9
U6N934051X		SN54181J, N	9
U6N934059X		SN74181J, N	9
U6N934151X	SN54181J, N	SN54181J, N	9
U6N934159X	SN74181J, N	SN74181J, N	9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DTL/TTL CIRCUITS

Fairchild TTL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
U7A935061X		SN5490J, N	9
U7A935059X		SN7490J, N	9
U7A935651X		SN5493J, N	9
U7A935659X		SN7493J, N	9
U7B5418251X	SN54182J, N	SN54182J, N	9
U7B5419251X	SN54192J, N	SN54192J, N	9
U7B5419351X	SN54193J, N	SN54193J, N	9
U7B544251X	SN5442J, N	SN5442J, N	9
U7B544351X	SN5443J, N	SN5443J, N	9
U7B544451X	SN5444J, N	SN5444J, N	9
U7B544651X	SN5446J, N	SN5446J, N	9
U7B544751X	SN5447J, N	SN5447J, N	9
U7B544851X	SN5448J, N	SN5448J, N	9
U7B549451X	SN5494J, N	SN5494J, N	9
U7B549651X	SN5496J, N	SN5496J, N	9
U7B7418259X	SN74182J, N	SN74182J, N	9
U7B7419259X	SN74192J, N	SN74192J, N	9
U7B7419359X	SN74193J, N	SN74193J, N	9
U7B744259X	SN7442J, N	SN7442J, N	9
U7B744359X	SN7443J, N	SN7443J, N	9
U7B744459X	SN7444J, N	SN7444J, N	9
U7B744659X	SN7446J, N	SN7446J, N	9
U7B744759X	SN7447J, N	SN7447J, N	9
U7B744859X	SN7448J, N	SN7448J, N	9
U7B749459X	SN7494J, N	SN7494J, N	9
U7B749659X	SN7496J, N	SN7496J, N	9
U7B902051X		SN54111J, N	6
U7B902059X		SN74111J, N	6
U7B902251X		SN54111J, N	6
U7B902259X		SN74111J, N	6
U7B902451X		SN54111J, N	6
U7B902459X		SN74111J, N	6
U7B930051X	SN54195J, N	SN54195J, N	9
U7B930059X	SN74195J, N	SN74195J, N	9
U7B930151X		SN5442J, N	9
U7B930159X		SN7442J, N	9
U7B931051X	SN54160J, N	SN54160J, N	9
U7B931059X	SN74160J, N	SN74160J, N	9
U7B931251X		SN54151J, N	9
U7B931259X		SN74151J, N	9
U7B931451X		SN5475J, N	9
U7B931459X		SN7475J, N	9
U7B931651X	SN54161J, N	SN54161J, N	9
U7B931659X	SN74161J, N	SN74161J, N	9
U7B9317511	SN5446AJ, N	SN5446AJ, N	9
U7B9317512	SN5447AJ, N	SN5447AJ, N	9
U7B9317513	SN5446AJ, N	SN5446AJ, N	9
U7B9317514	SN5447AJ, N	SN5447AJ, N	9
U7B9317591	SN7446AJ, N	SN7446AJ, N	9
U7B9317592	SN7447AJ, N	SN7447AJ, N	9
U7B9317593	SN7446AJ, N	SN7446AJ, N	9
U7B9317594	SN7447AJ, N	SN7447AJ, N	9
U7B932151X		SN54153J, N	9
U7B932159X		SN74153J, N	9
U7B932251X		SN54153J, N	9
U7B932259X		SN74153J, N	9
U7B932451X		SN5485J, N	9
U7B932459X		SN7485J, N	9
U7B9327511	SN5448J, N	SN5448J, N	9
U7B9327512	SN5448J, N	SN5448J, N	9
U7B9327591	SN7448J, N	SN7448J, N	9
U7B9327592	SN7448J, N	SN7448J, N	9
U7B932851X		SN5491AJ, N	9
U7B932859X		SN7491AJ, N	9
U7B934251X	SN54182J, N	SN54182J, N	9
U7B934259X	SN74182J, N	SN74182J, N	9
U7B935251X	SN5442J, N	SN5442J, N	9
U7B935259X	SN7442J, N	SN7442J, N	9
U7B935351X	SN5443J, N	SN5443J, N	9
U7B935359X	SN7443J, N	SN7443J, N	9
U7B935451X	SN5444J, N	SN5444J, N	9
U7B935459X	SN7444J, N	SN7444J, N	9
U7B9357511	SN5446AJ, N	SN5446AJ, N	9
U7B9357512	SN5447AJ, N	SN5447AJ, N	9
U7B9357591	SN7446AJ, N	SN7446AJ, N	9
U7B9357592	SN7447AJ, N	SN7447AJ, N	9
U7B935851X	SN5448J, N	SN5448J, N	9
U7B935859X	SN7448J, N	SN7448J, N	9
U7B936051X	SN54192J, N	SN54192J, N	9
U7B936059X	SN74192J, N	SN74192J, N	9
U7B936651X	SN54193J, N	SN54193J, N	9
U7B936659X	SN74193J, N	SN74193J, N	9
U7B939451X	SN5494J, N	SN5494J, N	9
U7B939459X	SN7494J, N	SN7494J, N	9
U7B939651X	SN5496J, N	SN5496J, N	9
U7B939659X	SN7496J, N	SN7496J, N	9
U7B960251X		SN54123J, N	6
U7B960259X		SN74123J, N	6

Motorola DTL

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC830F	SN15830U	SN7420W	6
MC830L, P	SN15830J, N	SN7420J, N	6
MC831F	SN15831U	SN74110W	6
MC831L, P	SN15831J, N	SN74110J, N	6
MC832F	SN15832U	SN7440W	6
MC832L, P	SN15832J, N	SN7440J, N	6
MC833F	SN15833U	SN7460W	6
MC833L, P	SN15833J, N	SN7460J, N	6
MC834F	SN15834U	SN7405W	6
MC834L, P	SN15834J, N	SN7405J, N	6
MC835F	SN15838U	SN7405W	6
MC835L, P	SN15838J, N	SN7405J, N	6
MC836F	SN15836U	SN7405W	6
MC836L, P	SN15836J, N	SN7405J, N	6
MC837F	SN15837U	SN7405W	6
MC837L, P	SN15837J, N	SN7405J, N	6
MC838F		SN74162W	9
MC838L, P		SN74162J, N	9
MC839F		SN74163W	9
MC839L, P		SN74163J, N	9
MC840F	SN15835U	SN7405W	6
MC840L, P	SN15835J, N	SN7405J, N	6
MC842F		SN7474W	6
MC842L, P		SN7474J, N	6
MC844F	SN15844U	SN7440W	6
MC844L, P	SN15844J, N	SN7440J, N	6

DTL/TTL CIRCUITS

Motorola DTL, Cont.

B

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC845F	SN15845U	SN74110W	6
MC845L, P	SN15846J, N	SN74110J, N	6
MC846F	SN15846W	SN7400W	6
MC846L, P	SN15846J, N	SN7400J, N	6
MC848F	SN15848U	SN74110W	6
MC848L, P	SN15848J, N	SN74110J, N	6
MC849F	SN15849U	SN7400W	6
MC849L, P	SN15849J, N	SN7400J, N	6
MC850F	SN15850U	SN74110W	6
MC850L, P	SN15850J, N	SN74110J, N	6
MC851F	SN15851U	SN74121W	6
MC851L, P	SN15851J, N	SN74121J, W	6
MC852F	SN158099U	SN7476W	6
MC852L, P	SN158099J, N	SN7476J, N	6
MC853F	SN158093U	SN7473W	6
MC853L, P	SN158093J, N	SN7473J, N	6
MC855F	SN158097U	SN7476W	6
MC855L, P	SN158097J, N	SN7476J, N	6
MC856F	SN158094U	SN7473W	6
MC856L, P	SN158094J, N	SN7473J, N	6
MC857F	SN15857U	SN7437W	6
MC857L, P	SN15857J, N	SN7437J, N	6
MC858F	SN15858U	SN7437W	6
MC858L, P	SN15858J, N	SN7437J, N	6
MC860F		SN74H103W	7
MC860L, P		SN74H103J, N	7
MC861F	SN15861U	SN7420W	6
MC861L, P	SN15861J, N	SN7420J, N	6
MC862F	SN15862U	SN7410W	6
MC862L, P	SN15862J, N	SN7410J, N	6
MC863F	SN15863U	SN7410W	6
MC863L, P	SN15863J, N	SN7410J, N	6
MC1800F	SN151800U	SN7420W	6
MC1800L, P	SN151800J, N	SN7420J, N	6
MC1801F	SN151801U	SN7420W	6
MC1801L, P	SN151801J, N	SN7420J, N	6
MC1802F	SN151802U	SN7430W	6
MC1802L, P	SN151802J, N	SN7430J, N	6
MC1803F	SN151803U	SN7430W	6
MC1803L, P	SN151803J, N	SN7430J, N	6
MC1804F	SN151804U	SN7430W	6
MC1804L, P	SN151804J, N	SN7430J, N	6
MC1805F	SN151805U	SN7430W	6
MC1805L, P	SN151805J, N	SN7430J, N	6
MC1806F	SN151806U	SN7408W	6
MC1806L, P	SN151806J, N	SN7408J, N	6
MC1807F	SN151807U	SN7408W	6
MC1807L, P	SN151807J, N	SN7408J, N	6
MC1808F	SN151808U	SN7432W	6
MC1808L, P	SN151808J, N	SN7432J, N	6
MC1809F	SN151809U	SN7432W	6
MC1809L, P	SN151809J, N	SN7432J, N	6
MC1810F	SN151810U	SN7402W	6
MC1810L, P	SN151810J, N	SN7402J, N	6
MC1811F	SN151811U	SN7402W	6
MC1811L, P	SN151811J, N	SN7402J, N	6
MC1812F	SN151812U	SN7486W	9
MC1812L, P	SN151812J, N	SN7486J, N	9
MC1813L, P		SN7475J, N	9
MC1814F		SN7475W	9
MC1814L, P		SN7475J, N	9
MC1815F		SN74H101W	7
MC1815L, P		SN74H101J, N	7
MC1816F		SN74H101W	7
MC1816L, P		SN74H101J, N	7
MC1818F		SN7403W	6
MC1820L, P		SN7403J, N	6
MC1820L, P	SN151820J, N	SN7406J, N	6

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC930F	SN15930U	SN5420W	6
MC930L	SN15930J, N	SN5420J, N	6
MC931F	SN15931U	SN54110W	6
MC931L	SN15931J, N	SN54110J, N	6
MC932F	SN15932U	SN5440W	6
MC932L	SN15932J, N	SN5440J, N	6
MC933F	SN15933U	SN5460W	6
MC933L	SN15933J, N	SN5460J, N	6
MC934F	SN15934U	SN5405W	6
MC934L	SN15934J, N	SN5405J, N	6
MC935F	SN15938U	SN5405W	6
MC935L	SN15938J, N	SN5405J, N	6
MC936F	SN15936U	SN5405W	6
MC936L	SN15936J, N	SN5405J, N	6
MC937F	SN15937U	SN5405W	6
MC937L	SN15937J, N	SN5405J, N	6
MC938F		SN54162W	9
MC938L		SN54162J, N	9
MC939F		SN54163W	9
MC939L		SN54163J, N	9
MC940F	SN15935U	SN5405W	6
MC940L	SN15935J, N	SN5405J, N	6
MC842F		SN5474W	6
MC842L		SN5474J, N	6
MC944F	SN15944U	SN5440W	6
MC944L	SN15944J, N	SN5440J, N	6
MC945F	SN15945U	SN54110W	6
MC945L	SN15945J, N	SN54110J, N	6
MC946F	SN15946U	SN5400W	6
MC946L	SN15946J, N	SN5400J, N	6
MC948F	SN15948U	SN54110W	6
MC948L	SN15948J, N	SN54110J, N	6
MC949F	SN15949U	SN5400W	6
MC949L	SN15949J, N	SN5400J, N	6
MC950F	SN15950U	SN54110W	6
MC950L	SN15950J, N	SN54110J, N	6
MC951F	SN15951U	SN54121W	6
MC951L	SN15951J, N	SN5412J, N	6
MC952F	SN159099U	SN5476W	6
MC952L	SN159099J, N	SN5476J, N	6
MC953F	SN159093U	SN5473W	6
MC953L	SN159093J, N	SN5473J, N	6
MC955F	SN159097U	SN5476W	6
MC955L	SN159097J, N	SN5476J, N	6
MC956F	SN159094U	SN5473W	6
MC956L	SN159094J, N	SN5473J, N	6
MC957F	SN15957U	SN5437W	6
MC957L	SN15957J, N	SN5437J, N	6
MC958F	SN15958U	SN5437W	6
MC958L	SN15958J, N	SN5437J, N	6
MC860F		SN54H103W	7
MC860L		SN54H103J, N	7
MC961F	SN15961U	SN5420W	6
MC961L	SN15961J, N	SN5420J, N	6
MC962F	SN15962U	SN5410W	6
MC962L	SN15962J, N	SN5410J, N	6
MC963F	SN15963U	SN5410W	6
MC963L	SN15963J, N	SN5410J, N	6
MC1900F	SN151900U	SN5420W	6
MC1900L	SN151900J, N	SN5420J, N	6
MC1901F	SN151901U	SN5420W	6
MC1901L	SN151901J, N	SN5420J, N	6
MC1902F	SN151902U	SN5430W	6
MC1902L	SN151902J, N	SN5430J, N	6
MC1903F	SN151903U	SN5430W	6
MC1903L	SN151903J, N	SN5430J, N	6
MC1904F	SN151904U	SN5430W	6
MC1904L	SN151904J, N	SN5430J, N	6

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DTL/TTL CIRCUITS

Motorola DTL, cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC1905F	SN151905U	SN5430W	6
MC1905L	SN151905J, N	SN5430J, N	6
MC1906F	SN151906U	SN5408W	6
MC1906L	SN151906J, N	SN5408J, N	6
MC1907F	SN151907U	SN5408W	6
MC1907L	SN151907J, N	SN5408J, N	6
MC1908F	SN151908U	SN5432W	6
MC1908L	SN151908J, N	SN5432J, N	6
MC1909F	SN151909U	SN5432W	6
MC1909L	SN151909J, N	SN5432J, N	6
MC1910F	SN151910U	SN5402W	6
MC1910L	SN151910J, N	SN5402J, N	6
MC1911F	SN151911U	SN5402W	6
MC1911L	SN151911J, N	SN5402J, N	6
MC1912L	SN151912U	SN5486W	9
MC1912L	SN151912J, N	SN5486J, N	9
MC1913F		SN5475W	9
MC1913L		SN5475J, N	9
MC1914F		SN5475W	9
MC1914L		SN5475J, N	9
MC1915F		SN54H101W	7
MC1915L		SN54H101J, N	7
MC1916F		SN54H101W	7
MC1916L		SN54H101J, N	7
MC1918F		SN5403W	6
MC1918L		SN5403J, N	6
MC1920L	SN151920J, N	SN5406J, N	6

Motorola TTL

Type Number	Direct Replacement	Recommended For New Designs	Sec. Page
MC400F	SNG42U	SN7420W	6
MC400L, P	SNG42J, N	SN7420J, N	6
MC401F	SNG52U	SN7453W	6
MC401L, P	SNG52J, N	SN7453J, N	6
MC402F	SNG62U	SN7430W	6
MC402L, P	SNG62J, N	SN7430J, N	6
MC403F	SNG92U	SN7486W	9
MC403L, P	SNG92J, N	SN7486J, N	9
MC404F	SNG102U	SN7453W	6
MC404L, P	SNG102J, N	SN7453J, N	6
MC405F	SNG112U	SN74H55W	7
MC405L, P	SNG112J, N	SN74H55J, N	6
MC406F	SNG122U	SN7430W	6
MC406L, P	SNG122J, N	SN7430J, N	6
MC407F	SNG132U	SN74S140W	5
MC407L, P	SNG132J, N	SN74S140J, N	5
MC408F	SNG142U	SN7400W	6
MC408L, P	SNG142J, N	SN7400J, N	6
MC409F	SNG152U	SN74H62W	7
MC409L, P	SNG152J, N	SN74H62J, N	7
MC410F	SNG172U	SN7460W	6
MC410L, P	SNG172J, N	SN7460J, N	6
MC411F	SNG182U	SN7430W	6
MC411L, P	SNG182J, N	SN7430J, N	6
MC412F	SNG192U	SN7410W	6
MC412L, P	SNG192J, N	SN7410J, N	6
MC413F	SNF12U	SN7472W	6
MC413L, P	SNF12J, N	SN7472J, N	6
MC414F	SNF22U	SN7472W	6
MC414L, P	SNF22J, N	SN7472J, N	6
MC415F	SNF52U	SN7472W	6
MC415L, P	SNF52J, N	SN7472J, N	6
MC416F	SNF62U	SN74H101W	7
MC416L, P	SNF62J, N	SN74H101J, N	7
MC417F		SN74105W	6
MC417L, P		SN74105J, N	6
MC419F	SNG162U	SN7438W	6
MC419L, P	SNG162J, N	SN7438J, N	6
MC420F	SNG72U	SN7450W	6
MC420L, P	SNG72J, N	SN7450J, N	6
MC421F	SNF32U	SN74104W	6
MC421L, P	SNF32J, N	SN74104J, N	6
MC422F		SN7474W	6
MC422L, P		SN7474J, N	6
MC423F	SNF102U	SN7473W	6
MC423L, P	SNF102J, N	SN7473J, N	6
MC424F	SNF112U	SN7476W	6
MC424L, P	SNF112J, N	SN7476J, N	6
MC425F		SN7404W	6
MC425L, P		SN7404J, N	6
MC426F	SNG82U	SN7413W	6
MC426L, P	SNG82J, N	SN7413J, N	6
MC427F	SNG282U	SN74H52W	7
MC427L, P	SNG282J, N	SN74H52J, N	7
MC428F		SN74H61W	7
MC428L, P		SN74H61J, N	7
MC450F	SNG43U	SN7420W	6
MC450L, P	SNG43J, N	SN7420J, N	6
MC451F	SNG53U	SN7453J, N	6
MC451L, P	SNG53J, N	SN7453J, N	6
MC452F	SNG63U	SN7430W	6
MC452L, P	SNG63J, N	SN7430J, N	6
MC453F	SNG93U	SN7486W	9
MC453L, P	SNG93J, N	SN7486J, N	9
MC454F	SNG103U	SN7453W	6
MC454L, P	SNG103J, N	SN7453J, N	6
MC455F	SNG113U	SN74H55W	7
MC455L, P	SNG113J, N	SN74H55J, N	7
MC456F	SNG123U	SN7430W	6
MC456L, P	SNG123J, N	SN7430J, N	6
MC457F	SNG133U	SN75S140W	5
MC4571L, P	SNG133J, N	SN74S140J, N	5
MC458F	SNG143U	SN7400W	6
MC458L, P	SNG143J, N	SN7400J, N	6
MC459F	SNG153U	SN74H62W	7
MC459L, P	SNG153J, N	SN74H62J, N	7
MC460F	SNG173U	SN7460W	6
MC460L, P	SNG173J, N	SN7460J, N	6
MC461F	SNG183U	SN7430W	6
MC461L, P	SNG183J, N	SN7430J, N	6
MC462F	SNG193U	SN7410W	6
MC462L, P	SNG193J, N	SN7410J, N	6
MC463F	SNF13U	SN7472W	6
MC463L, P	SNF13J, N	SN7472J, N	6
MC464F	SNF23U	SN7472W	6
MC464F	SNF23J, N	SN7472J, N	6
MC465F	SNF53U	SN7472W	6
MC465L, P	SNF53J, N	SN7472J, N	6

Motorola TTL, Cont

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC466F	SNF63U	SN74H101W	7
MC466L, P	SNF63J, N	SN74H101J, N	7
MC467F		SN74105W	6
MC467L, P		SN74105J, N	6
MC469F	SNG163U	SN7438W	6
MC469L, P	SNG163J, N	SN7438J, N	6
MC470F	SNG73U	SN7450W	6
MC470L, P	SNG73J, N	SN7450J, N	6
MC471F	SNF33U	SN74104W	6
MC471L, P	SNF33J, N	SN74104J, N	6
MC472F		SN7474W	6
MC472L, P		SN7474J, N	6
MC473F	SNF103U	SN7473W	6
MC473L, P	SNF103J, N	SN7473J, N	6
MC474F	SNF113U	SN7476W	6
MC474L, P	SNF113J, N	SN7476J, N	6
MC475F		SN7404W	6
MC475L, P		SN7404J, N	6
MC476F	SNG83U	SN7413W	6
MC476L, P	SNG83J, N	SN7413J, N	6
MC477F	SNG283U	SN74H52W	7
MC477L, P	SNG283J, N	SN74H52J, N	7
MC478F		SN74H61W	7
MC478L, P		SN74H61J, N	7
MC500F	SNG40U	SN5420W	6
MC500L	SNG40J, N	SN5420J, N	6
MC501F	SNG50U	SN5453W	6
MC501L	SNG50J, N	SN5453J, N	6
MC502F	SNG60U	SN5430W	6
MC502L	SNG60J, N	SN5430J, N	6
MC503F	SNG90U	SN5486W	9
MC503L	SNG90J, N	SN5486J, N	9
MC504F	SNG100U	SN5453W	6
MC504L	SNG100J, N	SN5453J, N	6
MC505F	SNG110U	SN54H55W	7
MC505L	SNG110J, N	SN54H55J, N	7
MC506F	SNG120U	SN5430W	6
MC506L	SNG120J, N	SN5430J, N	6
MC507F	SNG130U	SN54S140W	5
MC507L	SNG130J, N	SN54S140J, N	5
MC508F	SNG140U	SN5400W	6
MC508L	SNG140J, N	SN5400J, N	6
MC509F	SNG150U	SN54H62W	7
MC509L	SNG150J, N	SN54H62J, N	7
MC510F	SNG170U	SN5460W	6
MC510L	SNG170J, N	SN5460J, N	6
MC511F	SNG180U	SN5430W	6
MC511L	SNG180J, N	SN5430J, N	6
MC512F	SNG190U	SN5410W	6
MC512L	SNG190J, N	SN5410J, N	6
MC513F	SNF10U	SN5472W	6
MC513L	SNF10J, N	SN5472J, N	6
MC514F	SNF20U	SN5472W	6
MC514L	SNF20J, N	SN5472J, N	6
MC515F	SNF50U	SN5472W	6
MC515L	SNF50J, N	SN5472J, N	6
MC516F	SNF60U	SN54H101W	7
MC516L	SNF60J, N	SN54H101J, N	7
MC517F		SN54105W	6
MC517L		SN54105J, N	6
MC519F	SNG160U	SN5438W	6
MC519L	SNG160J, N	SN5438J, N	6
MC520F	SNG70U	SN5450W	6
MC520L	SNG70J, N	SN5450J, N	6
MC521F	SNF30U	SN54104W	6
MC521L	SNF30J, N	SN54104J, N	6
MC522F		SN5474W	6
MC522L		SN5474J, N	6
MC523F	SNF100U	SN5473W	6
MC523L	SNF100J, N	SN5473J, N	6
MC524F	SNF110U	SN5476W	6
MC524L	SNF110J, N	SN5476J, N	6
MC525F		SN5404W	6
MC525L		SN5404J, N	6
MC526F	SNG80U	SN5413W	6
MC526L	SNG80J, N	SN5413J, N	6
MC527F	SNG280U	SN54H52W	7
MC527L	SNG280J, N	SN54H52J, N	7
MC528F		SN54H61W	7
MC528L		SN54H61J, N	7
MC550F	SNG41U	SN5420W	6
MC550L	SNG41J, N	SN5420J, N	6
MC551F	SNG51U	SN5453W	6
MC551L	SNG51J, N	SN5453J, N	6
MC552F	SNG61U	SN5430W	6
MC552L	SNG61J, N	SN5430J, N	6
MC553F	SNG91U	SN5486W	9
MC553L	SNG91J, N	SN5486J, N	9
MC554F	SNG101U	SN5453W	6
MC554L	SNG101J, N	SN5453J, N	6
MC55F	SNG111U	SN54H55W	7
MC55L	SNG111J, N	SN54H55J, N	7
MC556F	SNG121U	SN5430W	6
MC556L	SNG121J, N	SN5430J, N	6
MC557F	SNG131U	SN54S140W	5
MC557L	SNG131J, N	SN54S140J, N	5
MC558F	SNG141W	SN5400W	6
MC558L	SNG141J, N	SN5400J, N	6
MC559F	SNG151U	SN54H62W	7
MC559L	SNG151J, N	SN54H62J, N	7
MC560F	SNG171U	SN5460W	6
MC560L	SNG171J, N	SN5460J, N	6
MC561F	SNG181U	SN5430W	6
MC561L	SNG181J, N	SN5430J, N	6
MC562F	SNG191U	SN5410W	6
MC562L	SNG191J, N	SN5410J, N	6
MC563F	SNF11U	SN5472W	6
MC563L	SNF11J, N	SN5472J, N	6
MC564F	SNF21U	SN5472W	6
MC564L	SNF21J, N	SN5472J, N	6
MC565F	SNF51U	SN5472W	6
MC565L	SNF51J, N	SN5472J, N	6
MC566F	SNF61U	SN54H101W	7
MC566L	SNF61J, N	SN54H101J, N	7
MC567F		SN54105W	6
MC567L		SN54105J, N	6
MC569F	SNG161U	SN5438W	6
MC569L	SNG161J, N	SN5438J, N	6
MC570F	SNG71U	SN5450W	6
MC570L	SNG71J, N	SN5450J, N	6
MC571F	SNF31U	SN54104W	6
MC571L	SNF31J, N	SN54104J, N	6
MC572F		SN5474W	6
MC572L		SN5474J, N	6
MC573F	SNF101U	SN5473W	6
MC573L	SNF101J, N	SN5473J, N	6
MC574F	SNF111U	SN5476W	6
MC574L	SNF111J, N	SN5476J, N	6
MC575F		SN5404W	6
MC575L		SN5404J, N	6
MC576F	SNG81U	SN5413W	6
MC576L	SNG81J, N	SN5413J, N	6
MC577F	SNG281U	SN54H52W	7
MC577L	SNG281J, N	SN54H52J, N	7

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DTL/TTL CIRCUITS

Motorola TTL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC578F		SN54H61W	7
MC578L		SN54H61J, N	7
MC2000F	SNG212U	SN74H55W	7
MC2000L, P	SNG212J, N	SN74H55J, N	7
MC2001F	SNG222U	SN74H00W	7
MC2001L, P	SNG222J, N	SN74H00J, N	7
MC2002F	SNG232U	SN74H62W	7
MC2002L, P	SNG232J, N	SN74H62J, N	7
MC2003F	SNG242U	SN74H20W	7
MC2003L, P	SNG242J, N	SN74H20J, N	7
MC2004F	SNG252U	SN74H53W	7
MC2004L, P	SNG252J, N	SN74H53J, N	7
MC2005F	SNG262U	SN74H30W	7
MC2005L, P	SNG262J, N	SN74H30J, N	7
MC2006F	SNG272U	SN74H60W	7
MC2006L, P	SNG272J, N	SN74H60J, N	7
MC2007F	SNG322U	SN74H10W	7
MC2007L, P	SNG322J, N	SN74H10J, N	7
MC2008F		SN74H04W	7
MC2008L, P		SN74H04J, N	7
MC2009F	SNF252U	SN74H102W	7
MC2009L, P	SNF252J, N	SN74H102J, N	7
MC2010F	SNF262U	SN74H101W	7
MC2010L, P	SNF262J, N	SN74H101J, N	7
MC2011F	SNG202U	SN74H30W	7
MC2011L, P	SNG202J, N	SN74H30J, N	7
MC2012F	SNG302U	SN74H53W	7
MC2012L, P	SNG302J, N	SN74H53J, N	7
MC2013F	SNG312U	SN74H50W	7
MC2013L, P	SNG312J, N	SN74H50J, N	7
MC2023F	SNF122U	SN74H103W	7
MC2023L, P	SNF122J, N	SN74H103J, N	7
MC2024F	SNF132U	SN74H108W	7
MC2024L, P	SNF132J, N	SN74H108J, N	7
MC2025F	SNF202U	SN74H102W	7
MC2025L, P	SNF202J, N	SN74H102J, N	7
MC2026F	SNF212U	SN74H101W	7
MC2026L, P	SNF212J, N	SN74H101J, N	7
MC2028F		SN74H101W	7
MC2028L, P		SN74H101J, N	7
MC2050F	SNG213U	SN74H55W	7
MC2050L, P	SNG213J, N	SN74H55J, N	7
MC2051F	SNG223U	SN74H00W	7
MC2051L, P	SNG223J, N	SN74H00J, N	7
MC2052F	SNG233U	SN74H62W	7
MC2052L, P	SNG233J, N	SN74H62J, N	7
MC2053F	SNG243U	SN74H20W	7
MC2053L, P	SNG243J, N	SN74H20J, N	7
MC2054F	SNG253U	SN74H53W	7
MC2054L, P	SNG253J, N	SN74H53J, N	7
MC2055F	SNG263U	SN74H30W	7
MC2055L, P	SNG263J, N	SN74H30J, N	7
MC2056F	SNG273U	SN74H60W	7
MC2056L, P	SNG273J, N	SN74H60J, N	7
MC2057F	SNG323U	SN74H10W	7
MC2057L, P	SNG323J, N	SN74H10J, N	7
MC2058F		SN74H04W	7
MC2058L, P		SN74H04J, N	7
MC2059F	SNF253U	SN74H102W	7
MC2059L, P	SNF253J, N	SN74H102J, N	7
MC2060F	SNF263U	SN74H101W	7
MC2060L, P	SNF263J, N	SN74H101J, N	7
MC2061F	SNG203U	SN74H30W	7
MC2061L, P	SNG203J, N	SN74H30J, N	7
MC2062F	SNG303U	SN74H53W	7
MC2062L, P	SNG303J, N	SN74H53J, N	7
MC2063F	SNG313U	SN74H50W	7
MC2063L, P	SNG313J, N	SN74H50J, N	7
MC2073F	SNF123U	SN74H103W	7
MC2073L, P	SNF123J, N	SN74H103J, N	7
MC2074F	SNF133U	SN74H108W	7
MC2074L, P	SNF133J, N	SN74H108J, N	7
MC2075F	SNF203U	SN74H102W	7
MC2075L, P	SNF203J, N	SN74H102J, N	7
MC2076F	SNF213U	SN74H101W	7
MC2076L, P	SNF213J, N	SN74H101J, N	7
MC2078F		SN74H101W	7
MC2078L, P		SN74H101J, N	7
MC2100F	SNG210U	SN54H55W	7
MC2100L	SNG210J, N	SN54H55J, N	7
MC2101F	SNG220U	SN54H00W	7
MC2101L	SNG220J, N	SN54H00J, N	7
MC2102F	SNG230U	SN54H62W	7
MC2102L	SNG230J, N	SN54H62J, N	7
MC2103F	SNG240U	SN54H20W	7
MC2103L	SNG240J, N	SN54H20J, N	7
MC2104F	SNG250U	SN54H53W	7
MC2104L	SNG250J, N	SN54H53J, N	7
MC2105F	SNG260U	SN54H30W	7
MC2105L	SNG260J, N	SN54H30J, N	7
MC2106F	SNG270U	SN54H60W	7
MC2106L	SNG270J, N	SN54H60J, N	7
MC2107F	SNG370U	SN54H10W	7
MC2107L	SNG320J, N	SN54H10J, N	7
MC2108F		SN54H04W	7
MC2108L		SN54H04J, N	7
MC2109F	SNF250U	SN54H102W	7
MC2109L	SNF250J, N	SN54H102J, N	7
MC2110F	SNF260U	SN54H101W	7
MC2110L	SNF260J, N	SN54H101J, N	7
MC2111F	SNG200U	SN54H30W	7
MC2111L	SNG200J, N	SN54H30J, N	7
MC2112F	SNG300U	SN54H53W	7
MC2112L	SNG300J, N	SN54H53J, N	7
MC2113F	SNG310U	SN54H50W	7
MC2113L	SNG310J, N	SN54H50J, N	7
MC2123F	SNF120U	SN54H103W	7
MC2123L	SNF120J, N	SN54H103J, N	7
MC2124F	SNF130U	SN54H108W	7
MC2124L	SNF130J, N	SN54H108J, N	7
MC2125F	SNF200U	SN54H102W	7
MC2125L	SNF200J, N	SN54H102J, N	7
MC2126F	SNF210U	SN54H101W	7
MC2126L	SNF210J, N	SN54H101J, N	7
MC2128F		SN54H101W	7
MC2128L		SN54H101J, N	7
MC2150F	SNG211U	SN54H55W	7
MC2150L	SNG211J, N	SN54H55J, N	7
MC2151F	SNG221U	SN54H00W	7
MC2151L	SNG221J, N	SN54H00J, N	7
MC2152F	SNG231U	SN54H62W	7
MC2152L	SNG231J, N	SN54H62J, N	7
MC2153F	SNG241U	SN54H20W	7
MC2153L	SNG241J, N	SN54H20J, N	7
MC2154F	SNG251U	SN54H53W	7
MC2154L	SNG251J, N	SN54H53J, N	7
MC2155F	SNG251U	SN54H30W	7
MC2155L	SNG261J, N	SN54H30J, N	7
MC2156F	SNG271U	SN54H60W	7
MC2156L	SNG271J, N	SN54H60J, N	7
MC2157F	SNG321U	SN54H10W	7
MC2157L	SNG321J, N	SN54H10J, N	7
MC2158F		SN54H04W	7
MC2158L		SN54H04J, N	7
MC2159F	SNF251U	SN54H102W	7
MC2159L	SNF251J, N	SN54H102J, N	7

DTL/TTL CIRCUITS

Motorola TTL, Cont.

B

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC2160F	SNF261U	SN54H101W	7
MC2160L	SNF261J, N	SN54H101J, N	7
MC2161F	SNG201U	SN54H30W	7
MC2161L	SNG201J, N	SN54H30J, N	7
MC2162F	SNG301U	SN54H53W	7
MC2162L	SNG301J, N	SN54H53J, N	7
MC2163F	SNG311U	SN54H50W	7
MC2163L	SNG311J, N	SN54H50J, N	7
MC2173F	SNF121U	SN54H103W	7
MC2173L	SNF121J, N	SN54H103J, N	7
MC2174F	SNF131U	SN54H108W	7
MC2174L	SNF131J, N	SN54H108J, N	7
MC2175F	SNF201U	SN54H102W	7
MC2175L	SNF201J, N	SN54H102J, N	7
MC2176F	SNF211U	SN54H101W	7
MC2176L	SNF211J, N	SN54H101J, N	7
MC2178F		SN54H101W	7
MC2178L		SN54H101J, N	7
MC3000F	SN74H00W	SN74H00W	7
MC3000L	SN74H00J, N	SN74H00J, N	7
MC3004F	SN74H01W	SN74H03W	7
MC3004L, P	SN74H01J, N	SN74H03J, N	7
MC3005F	SN74H10W	SN74H10W	7
MC3005L, P	SN74H10J, N	SN74H10J, N	7
MC3006F	SN74H11W	SN74H11W	7
MC3006L, P	SN74H11J, N	SN74H11J, N	7
MC3008F	SN74H04W	SN74H04W	7
MC3008F	SN74H04J, N	SN74H04J, N	7
MC3009F	SN74H05W	SN74H05W	7
MC3009L, P	SN74H05J, N	SN74H05J, N	7
MC3010F	SN74H20W	SN74H20W	7
MC3010L, P	SN74H20J, N	SN74H20J, N	7
MC3009F	SN74H05W	SN74H05W	7
MC3009L, P	SN74H05J, N	SN74H05J, N	7
MC3010F	SN74H20W	SN74H20W	7
MC3010L, P	SN74H20J, N	SN74H20J, N	7
MC3011F	SN74H21W	SN74H21W	7
MC3011L, P	SN74H21J, N	SN74H21J, N	7
MC3012F	SN74H22W	SN74H22W	7
MC3012L, P	SN74H22J, N	SN74H22J, N	7
MC3016F	SN74H30W	SN74H30W	7
MC3016L, P	SN74H30J, N	SN74H30J, N	7
MC3018F	SN74H62W	SN74H62W	7
MC3018L, P	SN74H62J, N	SN74H62J, N	7
MC3019F	SN74H61W	SN74H61W	7
MC3019L, P	SN74H61J, N	SN74H61J, N	7
MC3020F	SN74H50W	SN74H50W	7
MC3020L, P	SN74H50J, N	SN74H50J, N	7
MC3021F	SN7486W	SN7486W	9
MC3021L,	SN7486J, N	SN7486J, N	9
MC3023F	SN74H51W	SN74H51W	7
MC3023L, P	SN74H51J, N	SN74H51J, N	7
MC3024F	SN74H40W	SN74H40W	7
MC3024L, P	SN74H40J, N	SN74H40J, N	7
MC3025F	SN74H40W	SN74H40W	7
MC3025L, P	SN74H40J, N	SN74H40J, N	7
MC3030F	SN74H60W	SN74H60W	7
MC3030L, P	SN74H60J, N	SN74H60J, N	7
MC3031F	SN74H52W	SN74H52W	7
MC3031L, P	SN74H52J, N	SN74H52J, N	7
MC3032F	SN74H53W	SN74H53W	7
MC3032L, P	SN74H53J, N	SN74H53J, N	7
MC3033F	SN74H54W	SN74H54W	7
MC3033L, P	SN74H54J, N	SN74H54J, N	7
MC3034F	SN74H55W	SN74H55W	7
MC3034L, P	SN74H55J, N	SN74H55J, N	7
MC3050F		SN74H72W	7
MC3050L, P		SN74H72J, N	7

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC3051F		SN74H102W	7
MC3051L, P		SN74H102J, N	7
MC3052F		SN74H102W	7
MC3052L, P		SN74H102J, N	7
MC3054F	SN74H71W	SN74H71W	7
MC3054L, P	SN74H71J, N	SN74H71J, N	7
MC3055F	SN74H72W	SN74H72W	7
MC3055L, P	SN74H72J, N	SN74H72J, N	7
MC3060F	SN74H74W	SN74H74W	7
MC3060L, P	SN74H74J, N	SN74H74J, N	7
MC3061F	SN74S114W	SN74S114W	5
MC3061L, P	SN74S114J, N	SN74S114J, N	5
MC3062F	SN74S113W	SN74S113W	5
MC3062L, P	SN74S113J, N	SN74S113J, N	5
MC3100F	SN54H00W	SN54H00W	7
MC3100L	SN54H00J, N	SN54H00J, N	7
MC3104F	SN54H01W	SN54H01W	7
MC3104L	SN54H01J, N	SN54H01J, N	7
MC3105F	SN54H10W	SN54H10W	7
MC3105L	SN54H10J, N	SN54H10J, N	7
MC3106F	SN54H11W	SN54H11W	7
MC3106L	SM54H11J, N	SN54H11J, N	7
MC3108F	SN54H04W	SN54H04W	7
MC3108L	SN54H04J, N	SN54H04J, N	7
MC3109F	SN54H05W	SN54H05W	7
MC3109L	SN54H05J, N	SN54H05J, N	7
MC3110F	SN54H20W	SN54H20W	7
MC3110L	SN54H20J, N	SN54H20J, N	7
MC3111F	SN54H21W	SN54H21W	7
MC3111L	SN54H21J, N	SN54H21J, N	7
MC3112F	SN54H22W	SN54H22W	7
MC3112L	SN54H22J, N	SN54H22J, N	7
MC3116F	SN54H30W	SN54H30W	7
MC3116L	SN54H30J, N	SN54H30J, N	7
MC3118F	SN54H62W	SN54H62W	7
MC3118L	SN54H62J, N	SN54H62J, N	7
MC3119F	SN54H61W	SN54H61W	7
MC3119L	SN54H61J, N	SN54H61J, N	7
MC3120F	SN54H50W	SN54H50W	7
MC3120L	SN54H50J, N	SN54H50J, N	7
MC3121F	SN5486W	SN5486W	9
MC3121L	SN5486J, N	SN5486J, N	9
MC3123F	SN54H51W	SN54H51W	7
MC3123L	SN54H51J, N	SN54H51J, N	7
MC3124F	SN54H40W	SN54H40W	7
MC3124L	SN54H40J, N	SN54H40J, N	7
MC3125F	SN54H40W	SN54H40W	7
MC3125L	SN54H40J, N	SN54H40J, N	7
MC3130F	SN54H60W	SN54H60W	7
MC3130L	SN54H60J, N	SN54H60J, N	7
MC3131F	SN54H52W	SN54H52W	7
MC3131L	SN54H52J, N	SN54H52J, N	7
MC3132F	SN54H53W	SN54H53W	7
MC3132L	SN54H53J, N	SN54H53J, N	7
MC3133F	SN54H54W	SN54H54W	7
MC3133L	SN54H54J, N	SN54H54J, N	7
MC3134F	SN54H55W	SN54H55W	7
MC3134L	SN54H55J, N	SN54H55J, N	7
MC3150F		SN54H72W	7
MC3150L		SN54H72J, N	7
MC3151F		SN54H102W	7
MC3151L		SN54H102J, N	7
MC3152F		SN54H102W	7
MC3152L		SN54H102J, N	7
MC3154F	SN54H71W	SN54H71W	7
MC3154L	SN54H71J, N	SN54H71J, N	7
MC3155F	SN54H72W	SN54H72W	7
MC3155L	SN54H72J, N	SN54H72J, N	7

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Motorola TTL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC3160F	SN54H74W	SN54H74W	7
MC3160L	SN54H74J, N	SN54H74J, N	7
MC3161F	SN54S114W	SN54S114W	5
MC3161L	SN54S114J, N	SN54S114J, N	5
MC3162F	SN54S113W	SN54S113W	5
MC3162L	SN54S113J, N	SN54S113J, N	5
MC5400F	SN5400W	SN5400W	6
MC5400L	SN5400J, N	SN5400J, N	6
MC5401F	SN5401W	SN5401W	6
MC5401L	SN5401J, N	SN5401J, N	6
MC5402F	SN5402W	SN5402W	6
MC5402L	SN5402J, N	SN5402J, N	6
MC5403L	SN5403J, N	SN5403J, N	6
MC5404F	SN5404W	SN5404W	6
MC5404L	SN5404J, N	SN5404J, N	6
MC5405F	SN5405W	SN5405W	6
MC5405L	SN5405J, N	SN5405J, N	6
MC5410F	SN5410W	SN5410W	6
MC5410L	SN5410J, N	SN5410J, N	6
MC5420F	SN5420W	SN5420W	6
MC5420L	SN5420J, N	SN5420J, N	6
MC5430F	SN5430W	SN5430W	6
MC5430L	SN5430J, N	SN5430J, N	6
MC5440F	SN5440W	SN5440W	6
MC5440L	SN5440J, N	SN5440J, N	6
MC5442L	SN5442J, N	SN5442J, N	9
MC5443L	SN5443J, N	SN5443J, N	9
MC5444L	SN5444J, N	SN5444J, N	9
MC5445L	SN5445J, N	SN5445J, N	9
MC5446L	SN5446AJ, N	SN5446AJ, N	9
MC5447L	SN5447AJ, N	SN5447AJ, N	9
MC5450F	SN5450W	SN5450W	6
MC5450L	SN5450J, N	SN5450J, N	6
MC5451F	SN5451W	SN5451W	6
MC5451L	SN5451J, N	SN5451J, N	6
MC5453F	SN5453W	SN5453W	6
MC5453L	SN5453J, N	SN5453J, N	6
MC5454F	SN5454W	SN5454W	6
MC5454L	SN5454J, N	SN5454J, N	6
MC5460F	SN5460W	SN5460W	6
MC5460L	SN5460J, N	SN5460J, N	6
MC5472F	SN5472W	SN5472W	6
MC5472L	SN5472J, N	SN5472J, N	6
MC5473F	SN5473W	SN5473W	6
MC5473L	SN5473J, N	SN5473J, N	6
MC5480L	SN5480J, N	SN5480J, N	9
SN5483L	SN5483J, N	SN5483J, N	9
MC5490L	SN5490W	SN5490W	9
MC5490L	SN5490J, N	SN5490J, N	9
MC5491AL	SN5491AJ, N	SN5491AJ, N	9
MC5492F	SN5492W	SN5492W	9
MC5492L	SN5492J, N	SN5492J, N	9
MC5493L	SN5493J, N	SN5493J, N	9
MC5494L	SN5494J, N	SN5494J, N	9
MC5495F	SN5495AW	SN5495AW	9
MC5495L	SN5495AJ, N	SN5495AJ, N	9
MC5496L	SN5496J, N	SN5496J, N	9
MC15842L	SN5482J, N	SN5482J, N	9
MC54107L	SN54107J, N	SN54107J, N	6
MC54121F	SN54121W	SN54121W	6
MC54121L	SN54121J, N	SN54121J, N	6
MC54150L	SN54150J, N	SN54150J, N	9
MC54151L	SN54151J, N	SN54151J, N	9
MC54192L	SN54192J, N	SN54192J, N	9
MC54193L	SN54193J, N	SN54193J, N	9
MC7400F	SN7400W	SN7400W	6
MC7400L, P	SN7400J, N	SN7400J, N	6
MC7401F	SN7401W	SN7401W	6
MC7401L, P	SN7401J, N	SN7401J, N	6
MC7402F	SN7402W	SN7402W	6
MC7402L, P	SN7402J, N	SN7402J, N	6
MC7403L, P	SN7403J, N	SN7403J, N	6
MC7404F	SN7404W	SN7404W	6
MC7404L, P	SN7404J, N	SN7404J, N	6
MC7405F	SN7405W	SN7405W	6
MC7405L, P	SN7405J, N	SN7405J, N	6
MC7410F	SN7410W	SN7410W	6
MC7410L, P	MC7410J, N	SN7410J, N	6
MC7420F	SN7420W	SN7420W	6
MC7420L, P	SN7420J, N	SN7420J, N	6
MC7430F	SN7430W	SN7430W	6
MC7430L, P	SN7430J, N	SN7430J, N	6
MC7440F	SN7440W	SN7440W	6
MC7440L, P	SN7440J, N	SN7440J, N	6
MC7441AL, P	SN74141J, N	SN74141J, N	9
MC7442L, P	SN7442J, N	SN7442J, N	9
MC7443L, P	SN7443J, N	SN7443J, N	9
MC7444L, P	SN7444J, N	SN7444J, N	9
MC7445L, P	SN7445J, N	SN7445J, N	9
MC7446L, P	SN7446AJ, N	SN7446AJ, N	9
MC7447L, P	SN7447AJ, N	SN7447AJ, N	9
MC7450F	SN7450W	SN7450W	6
MC7450L, P	SN7450J, N	SN7450J, N	6
MC7451F	SN7451W	SN7451W	6
MC7451L, P	SN7451J, N	SN7451J, N	6
MC7453F	SN7453W	SN7453W	6
MC7453L, P	SN7453J, N	SN7453J, N	6
MC7454F	SN7454W	SN7454W	6
MC7454L, P	SN7454J, N	SN7454J, N	6
MC7460F	SN7460W	SN7460W	6
MC7460L, P	SN7460J, N	SN7460J, N	6
MC7472F	SN7472W	SN7472W	6
MC7472L, P	SN7472J, N	SN7472J, N	6
MC7473F	SN7473W	SN7473W	6
MC7473L, P	SN7473J, N	SN7473J, N	6
MC7480L, P	SN7480J, N	SN7480J, N	9
SN7483L, P	SN7483J, N	SN7483J, N	9
MC7490F	SN7490W	SN7490W	9
MC7490L, P	SN7490J, N	SN7490J, N	9
MC7491AL, P	SN7491AJ, N	SN7491AJ, N	9
MC7492F	SN7492W	SN7492W	9
MC7492L, P	SN7492J, N	SN7492J, N	9
MC7493L, P	SN7493J, N	SN7493J, N	9
SN7494L, P	SN7494J, N	SN7494J, N	9
SN7495F	SN7495AW	SN7495AW	9
SN7495L, P	SN7495AJ, N	SN7495AJ, N	9
SN7496L, P	SN7496J, N	SN7496J, N	9
MC17482L	SN7482J, N	SN7482J, N	9
MC74107L, P	SN74107J, N	SN74107J, N	6
MC74121F	SN74121W	SN74121W	6
MC74121L, P	SN74121J, N	SN74121J, N	6
MC74150L	SN74150J, N	SN74150J, N	9
MC74151L, P	SN74151J, N	SN74151J, N	9
MC74192L, P	SN74192J, N	SN74192J, N	9
MC74193L, P	SN74193J, N	SN74193J, N	9

DTL/TTL CIRCUITS

Motorola Complex Functions

B

Type Number	Direct Replacement	Recommended For New Designs	Sec.
MC4000F		SN74153W	9
MC4000L, P		SN74153J, N	9
MC4001L, P		SN74184J, N or	9
		SN74185A,J, N	9
MC4002F		SN74155W	9
MC4002L, P		SN74155J, N	9
MC4004F	SN7481W	SN7481W	9
MC4004L, P	SN7481J, N	SN7481J, N	9
MC4005F	SN7481W	SN7481W	9
MC4005L, P	SN7481J, W	SN7481J, N	9
MC4006F		SN74155W	9
MC4006L, P		SN74155J, N	9
MC4007L, P		SN74155J, N	9
MC4008F		SN74180W	9
MC4008L, P		SN74180J, N	9
MC4010F		SN74180W	9
MC4010L, P		SN74180J, N	9
MC4012F		SN7495AW	9
MC4012L, P		SN7495AJ, N	9
MC4015L, P		SN7475J, N	9
MC4016L, P		SN74190J, N	9
MC4018L, P		SN74191J, N	9
MC4023F		SN7492W	9
MC4023L, P		SN7492J, N	9
MC4026F		SN74H183W	9
MC4026L, P		SN74H183J, N	9
MC4027F		SN74H183W	9
MC4027L, P		SN74H183J, N	9
MC4028F		SN74181W	9
MC4028L, P		SN74181J, N	9
MC4029F		SN74181W	9
MC4029L, P		SN74181J, N	9
MC4030F		SN74181W	9
MC4030L, P		SN74181J, N	9
MC4031F		SN74181W	9
MC4031L, P		SN74181J, N	9
MC4032F		SN74182W	9
MC4032L, P		SN74182J, N	9
MC4035F		SN7475W	9
MC4035L, P		SN7475J, N	9
MC4037F		SN7475W	9

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC4037L, P		SN7415J, N	9
MC4039P		SN7448J, N	9
MC4304F	SN5481W	SN5481W	9
MC4304L	SN5481J, N	SN5481J, N	9
MC4305F	SN5481W	SN5481W	9
MC4305L	SN5481J, N	SN5481J, N	9
MC316L, P		SN54190J, N	9
MC4318L, P		SN54191J, N	9
MC4326F		SN54H183W	9
MC4326L		SN54H183J, N	9
MC4327F		SN54H183W	9
MC4327L		SN54H183J, N	9
MC4328F		SN54181W	9
MC4328L		SN54181J, N	9
MC4329F		SN54181W	9
MC4329L		SN54181J, N	9
MC4330F		SN54181W	9
MC4330L		SN54181J, N	9
MC4331F		SN54181W	9
MC4331L		SN54181J, N	9
MC4332F		SN54182W	9
MC4332L		SN54182J, N	9
MC4335F		SN5475W	9
MC4335L, P		SN5475J, N	9
MC4337F		SN5475W	9
MC4337L, P		SN5475J, N	9
MC8300L, P	SN74195J, N	SN74195J, N	9
MC8301L, P		SN7442J, N	9
MC8304L, P		SN7482J, N	9
MC8309L, P		SN74153J, N	9
MC8312L, P		SN74151J, N	9
MC8601F	SN74122W	SN74122W	6
MC8601L, P	SN74122J, N	SN74122J, N	6
MC9300L	SN54195J, N	SN54195J, N	9
MC9301L		SN5442J, N	9
MC9304L		SN5482J, N	9
MC9309L		SN54153J, N	9
MC9312L		SN54151J, N	9
MC9601F	SN54122W	SN54122W	6
MC9601L	SN54122J, N	SN54122J, N	6

National DTL

Type Number	Direct Replacement	Recommended For New Designs	Sec.
DM930N	SN15830J, N	SN7420J, N	6
DM932N	SN15832J, N	SN7440J, N	6
DM933N	SN15833J, N	SN7460J, N	6
DM935N	SN15840J, N	SN7405J, N	6
DM936N	SN15836J, N	SN7405J, N	6
DM937N	SN15837J, N	SN7405J, N	6
DM944N	SN15844J, N	SN7440J, N	6
DM945N	SN15845J, N	SN74110J, N	6
DM946N	SN15846J, N	SN7400J, N	6
DM948N	SN15848J, N	SN74110J, N	6
DM949N	SN15849J, N	SN7400J, N	6

Type Number	Direct Replacement	Recommended for New Designs	Sec.
DM957N	SN15857J, N	SN7437J, N	6
DM958N	SN15858J, N	SN7437J, N	6
DM961N	SN15861J, N	SN7420J, N	6
DM962N	SN15862J, N	SN7410J, N	6
DM963N	SN15863J, N	SN7410J, N	6
DM1800N	SN151800J, N	SN7420J, N	6
DM1801N	SN151801J, N	SN7420J, N	6
DM9093N	SN158093J, N	SN7473J, N	6
DM9094N	SN158094J, N	SN7473J, N	6
DM9097N	SN158097J, N	SN7476J, N	6
DM9099N	SN158099J, N	SN7476J, N	6

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DTL/TTL CIRCUITS

National TTL

Type Number†	Direct Replacement	Recommended for New Designs	Sec.
DM5400D, N (7000)	SN5400J, N	SN5400J, N	6
DM5401D, N (7001)	SN5401J, N	SN5401J, N	6
DM5402D, N (7002)	SN5402J, N	SN5402J, N	6
DM5403D, N (7003)	SN5403J, N	SN5403J, N	6
DM5404D, N (7004)	SN5404J, N	SN5404J, N	6
DM5405D, N (7005)	SN5405J, N	SN5405J, N	6
DM5408D, N (7008)	SN5408J, N	SN5408J, N	6
DM5409D, N (7009)	SN5409J, N	SN5409J, N	6
DM5410D, N (7010)	SN5410J, N	SN5410J, N	6
DM5420D, N (7020)	SN5420J, N	SN5420J, N	6
DM5430D, N (7030)	SN5430J, N	SN5430J, N	6
DM5440D, N (7040)	SN5440J, N	SN5440J, N	6
DM5442D, N (7842)	SN5442J, N	SN5442J, N	9
DM5446D, N (7846)	SN5446AJ, N	SN5446AJ, N	9
DM5447D, N (7847)	SN5447AJ, N	SN5447AJ, N	9
DM5448D, N (7848)	SN5448J, N	SN5448J, N	9
DM5450D, N (7050)	SN5450J, N	SN5450J, N	6
DM5451D, N (7051)	SN5451J, N	SN5451J, N	6
DM5453D, N (7053)	SN5453J, N	SN5453J, N	6
DM5454D, N (7054)	SN5454J, N	SN5454J, N	6
DM5460D, N (7060)	SN5460J, N	SN5460J, N	6
DM5472D, N (7540)	SN5472J, N	SN5472J, N	6
DM5473D, N (7501)	SN5473J, N	SN5473J, N	6
DM5474D, N (7510)	SN5474J, N	SN5474J, N	6
DM5475D, N (7550)	SN5475J, N	SN5475J, N	9
DM5476D, N (7500)	SN5476J, N	SN5476J, N	6
DM5483D, N (7283)	SN5483J, N	SN5483J, N	9
DM5486D, N (7086)	SN5486J, N	SN5486J, N	9
DM5488D, N (7588)	SN5488J, N	SN5488J, N	9
DM5490D, N (7530)	SN5490J, N	SN5490J, N	9
DM5491AD, N	SN5491AJ, N	SN5491AJ, N	9
DM5492D, N (7532)	SN5492J, N	SN5492J, N	9
DM5493D, N (7533)	SN5493J, N	SN5493J, N	9
DM5495D, N (7580)	SN5495AJ, N	SN5495AJ, N	9
DM54107D, N (7502)	SN54107J, N	SN54107J, N	6
DM54121D, N	SN54121J, N	SN54121J, N	6
DM54153D, N (7212)	SN54153J, N	SN54153J, N	9
DM54154D, N (7213)	SN54154J, N	SN54154J, N	9
DM7200D, N		SN5485J, N	9
DM7210D, N		SN54151J, N	9
DM7220D, N		SN54180J, N	9
DM7280D, N (8680)		SN54196J, N	9
DM7281D, N (8681)		SN54197J, N	9
DM7288D, N (8688)		SN54197J, N	9
DM7400D, N (8000)	SN7400J, N	SN7400J, N	6
DM7401D, N (8001)	SN7401J, N	SN7401J, N	6
DM7402D, N (8002)	SN7402J, N	SN7402J, N	6
DM7403D, N (8003)	SN7403J, N	SN7403J, N	6
DM7404D, N (8004)	SN7404J, N	SN7404J, N	6
DM7405D, N (8005)	SN7405J, N	SN7405J, N	6
DM7408D, N (8008)	SN7408J, N	SN7408J, N	6
DM7409D, N (8009)	SN7409J, N	SN7409J, N	6
DM7410D, N (8010)	SN7410J, N	SN7410J, N	6
DM7420D, N (8020)	SN7420J, N	SN7420J, N	6
DM7430D, N (8030)	SN7430J, N	SN7430J, N	6
DM7440D, N (8040)	SN7440J, N	SN7440J, N	6
DM7441D, N (8841)	SN74141J, N	SN74141J, N	9
DM7442D, N (8842)	SN7442J, N	SN7442J, N	9
DM7446D, N (8846)	SN7446AJ, N	SN7446AJ, N	9
DM7447D, N (8847)	SN7447AJ, N	SN7447AJ, N	9
DM7448D, N (8848)	SN7448J, N	SN7448J, N	9
DM7450D, N (8050)	SN7450J, N	SN7450J, N	6
DM7451D, N (8051)	SN7451J, N	SN7451J, N	6
DM7453D, N (8053)	SN7453J, N	SN7453J, N	6
DM7454D, N (8054)	SN7454J, N	SN7454J, N	6
DM7460D, N (8060)	SN7460J, N	SN7460J, N	6
DM7472D, N (8540)	SN7472J, N	SN7472J, N	6
DM7473D, N (8501)	SN7473J, N	SN7473J, N	6
DM7474D, N (8510)	SN7474J, N	SN7474J, N	6
DM7475D, N (8550)	SN7475J, N	SN7475J, N	9
DM7476D, N (8500)	SN7476J, N	SN7476J, N	6
DM7483D, N (8283)	SN7483J, N	SN7483J, N	9
DM7486D, N (8086)	SN7486J, N	SN7486J, N	9
DM7488D, N (8588)	SN7488J, N	SN7488J, N	9
DM7490D, N (8530)	SN7490J, N	SN7490J, N	9
DM7491AD, N	SN7491AJ, N	SN7491AJ, N	9
DM7492D, N (8532)	SN7492J, N	SN7492J, N	9
DM7493D, N (8533)	SN7493J, N	SN7493J, N	9
DM7495D, N (8580)	SN7495AJ, N	SN7495AJ, N	9
DM74107D, N (8502)	SN74107J, N	SN74107J, N	6
DM74121D, N	SN74121J, N	SN74121J, N	6
DM74153D, N (8212)	SN74153J, N	SN74153J, N	9
DM74154D, N (8213)	SN74154J, N	SN74154J, N	9
DM7520D, N		SN5497J, N	9
DM7551D, N		SN5475J, N	9
DM7560D, N	SN54192J, N	SN54192J, N	9
DM7563D, N	SN54193J, N	SN54193J, N	9
DM7570D, N	SN54164J, N	SN54164J, N	9
DM7588D, N	SN5488J, N	SN5488J, N	9
DM7590D, N	SN54165J, N	SN54165J, N	9
DM7598D, N		SN5488J, N	9
DM7599D, N		SN5489J, N	9
DM8200D, N		SN7485J, N	9
DM8210D, N		SN74151J, N	9
DM8220D, N		SN74180J, N	9
DM8280D, N (7680)		SN54196J, N	9
DM8281D, N (7681)		SN54197J, N	9
DM8288D, N (7688)		SN54197J, N	9
DM8300D, N (8600)	SN74195J, N	SN74195J, N	9
DM8311D, N (8213)	SN74154J, N	SN74154J, N	9
DM8520D, N		SN7497J, N	9
DM8551D, N		SN7475J, N	9
DM8560D, N	SN74192J, N	SN74192J, N	9
DM8563D, N	SN74193J, N	SN74193J, N	9
DM8570D, N	SN74164J, N	SN74164J, N	9
DM8588D, N	SN7488J, N	SN7488J, N	9
DM8590D, N	SN74165J, N	SN74165J, N	9
DM8598D, N		SN7488J, N	9
DM8599D, N		SN7489J, N	9
DM8601D, N (8850)	SN74122J, N	SN74122J, N	6
DM9300D, N (7600)	SN54195J, N	SN54195J, N	9
DM9311D, N (7213)	SN54154J, N	SN54154J, N	9
DM9601D, N (7850)	SN54122J, N	SN54122J, N	6

†Number in parentheses is an obsolete type number.

DTL/TTL CIRCUITS

Raytheon DTL

B

Type Number	Direct Replacement	Recommended For New Designs	Sec.
RC930D, P	SN15830J, N	SN7420J, N	6
RC930J	SN15830U	SN7420W	6
RC932D, P	SN15832J, N	SN7440J, N	6
RC932J	SN15832U	SN7440W	6
RC933D, P	SN15833J, N	SN7460J, N	6
RC933J	SN15833U	SN7460W	6
RC934D, P	SN15834J, N	SN7405J, N	6
RC934J	SN15834U	SN7405W	6
RC935D, P	SN15838J, N	SN7405J, N	6
RC935J	SN15838U	SN7405W	6
RC936D, P	SN15836J, N	SN7405J, N	6
RC936J	SN15836U	SN7405W	6
RC937D, P	SN15837J, N	SN7405J, N	6
RC937J	SN15837U	SN7405W	6
RC940D, P	SN15835J, N	SN7405J, N	6
RC940J	SN15835U	SN7405W	6
RC941D, P	SN15841J, N		11
RC941J	SN15841U		11
RC944D, P	SN15844J, N	SN7440J, N	6
RC944J	SN15844U	SN7440W	6
RC945D, P	SN15845J, N	SN74110J, N	6
RC945J	SN15845U	SN74110W	6
RC946D, P	SN15846J, N	SN7400J, N	6
RC946J	SN15846U	SN7400W	6
RC948D, P	SN15848J, N	SN74110J, N	6
RC948J	SN15848U	SN74110W	6
RC949D, P	SN15849J, N	SN7400J, N	6
RC949J	SN15849U	SN7400W	6
RC950D, P	SN15850J, N	SN74110J, N	6
RC950J	SN15850U	SN74110W	6
RC951D, P	SN15851J, N	SN74121J, N	6
RC951J	SN15851U	SN74121W	6
RC957J	SN15857J, N	SN7437J, N	6
RC957J	SN15857U	SN7437W	6
RC958D, P	SN15858J, N	SN7437J, N	6
RC958J	SN15858U	SN7437W	6
RC961D, P	SN15861J, N	SN7420J, N	6
RC961J	SN15861U	SN7420W	6
RC962D, P	SN15862J, N	SN7410J, N	6
RC962J	SN15862U	SN7410W	6
RC9630D, P	SN15863J, N	SN7410J, N	6
RC963J	SN15863U	SN7410W	6
RC993D, P	SN158093J, N	SN7473J, N	6
RC993J	SN158093U	SN7473W	6
RC994D, P	SN158094J, N	SN7473J, N	6
RC994J	SN158094U	SN7473W	6
RC997D, P	SN158097J, N	SN7476J, N	6
RC997J	SN158097U	SN7476W	6
RC999D, P	SN158099J, N	SN7476J, N	6
RC999J	SN158099U	SN7476W	6
RC1900D, P	SN151800J, N	SN7420J, N	6
RC1900J	SN151800U	SN7420W	6
RC1901D, P	SN151801J, N	SN7420J, N	6
RC1901J	SN151801U	SN7420W	6
RC1902D, P	SN151802J, N	SN7430J, N	6
RC1902J	SN151802U	SN7430W	6
RC1903D, P	SN151803J, N	SN7430J, N	6
RC1903J	SN151803U	SN7430W	6
RC1904D, P	SN151804J, N	SN7430J, N	6
RC1904J	SN151804U	SN7430J, N	6
RC1905D, P	SN151805J, N	SN7430J, N	6
RC1905J	SN151805U	SN7430W	6

Type Number	Direct Replacement	Recommended for New Designs	Sec.
RM930D, P	SN15930J, N	SN5420J, N	6
RM930J	SN15930U	SN5420J, N	6
RM932D, P	SN15932J, N	SN5440J, N	6
RM932J	SN15932U	SN5440W	6
RM933D, P	SN15933J, N	SN5460J, N	6
RM933J	SN15933U	SN5460W	6
RM934D, P	SN15934J, N	SN5405J, N	6
RM934J	SN15934U	SN5405W	6
RM935D, P	SN15938J, N	SN5405J, N	6
RM935J	SN15938U	SN5405W	6
RM936D, P	SN15936J, N	SN5405J, N	6
RM936J	SN15936U	SN5405W	6
RM937D, P	SN15937J, N	SN5405J, N	6
RM937J	SN15937U	SN5405W	6
RM940D, P	SN15935J, N	SN5405J, N	6
RM940J	SN15935U	SN5405W	6
RM941D, P	SN15941J, N		11
RM941J	SN15941U		11
RM944D, P	SN15944J, N	SN5440J, N	6
RM944J	SN15944U	SN5440W	6
RM945D, P	SN15945J, N	SN54110J, N	6
RM945J	SN15945U	SN54110W	6
RM946D, P	SN15946J, N	SN5400J, N	6
RM946J	SN15946U	SN5400W	6
RM948D, P	SN15948J, N	SN54110J, N	6
RM948J	SN15948U	SN54110W	6
RM949D, P	SN15949J, N	SN5400J, N	6
RM949J	SN15949U	SN5400W	6
RM950D, P	SN15950J, N	SN54110J, N	6
RM950J	SN15950U	SN54110W	6
RM951D, P	SN15951J, N	SN54121J, N	6
RM951J	SN15951U	SN54121W	6
RM957D, P	SN15957J, N	SN5437J, N	6
RM957J	SN15957U	SN5437W	6
RM958D, P	SN15958J, N	SN5437J, N	6
RM958J	SN15958U	SN5437W	6
RM961D, P	SN15961J, N	SN5420J, N	6
RM961J	SN15961U	SN5420W	6
RM962D, P	SN15962J, N	SN5410J, N	6
RM962J	SN15962U	SN5410W	6
RM963D, P	SN15963J, N	SN5410J, N	6
RM963J	SN15963U	SN5410W	6
RM993D, P	SN159093J, N	SN5473J, N	6
RM993J	SN159093U	SN5473W	6
RM994D, P	SN159094J, N	SN5473J, N	6
RM994J	SN159094U	SN5473W	6
RM997D, P	SN159097J, N	SN5476J, N	6
RM977J	SN159097U	SN5476W	6
RM999D, P	SN159099J, N	SN5476J, N	6
RM999J	SN159099U	SN5476W	6
RM1900D, P	SN151900J, N	SN5420J, N	6
RM1900J	SN151900U	SN5420W	6
RM1901D, P	SN151901J, N	SN5420J, N	6
RM1901J	SN151901U	SN5420W	6
RM1902D, P	SN151902J, N	SN5430J, N	6
RM1902J	SN151902U	SN5430W	6
RM1903D, P	SN151903J, N	SN5430J, N	6
RM1903J	SN151903U	SN5430W	6
RM1904D, P	SN151904J, N	SN5430J, N	6
RM1904J	SN151904U	SN5430W	6
RM1905D, P	SN151905J, N	SN5430J, N	6
RM1905J	SN151905U	SN5430W	6

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DTL/TTL CIRCUITS

Raytheon TTL

Type Number	Direct Replacement	Recommended for New Designs	Sec.
RF10D, P	SNF10J, N	SN5472J, N	6
RF10K	SNF10U	SN5472W	6
RF11D, P	SNF11J, N	SN5472J, N	6
RF11K	SNF11U	SN5472W	6
RF12D, P	SNF12J, N	SN7472J, N	6
RF12K	SNF12U	SN7472W	6
RF13D, P	SNF13J, N	SN7472J, N	6
RF13K	SNF13U	SN7472W	6
RF20D, P	SNF20J, N	SN5472J, N	6
RF20K	SNF20U	SN5472W	6
RF21D, P	SNF21J, N	SN5472J, N	6
RF21K	SNF21U	SN5472W	6
RF22D, P	SNF22J, N	SN7472J, N	6
RF22K	SNF22U	SN7472W	6
RF23D, P	SNF23J, N	SN7472J, N	6
RF23K	SNF23U	SN7472W	6
RF30D, P	SNF30J, N	SN54104J, N	6
RF30K	SNF30U	SN54104W	6
RF31D, P	SNF31J, N	SN54104J, N	6
RF31K	SNF31U	SN54104W	6
RF32D, P	SNF32J, N	SN74104J, N	6
RF32K	SNF32U	SN74104W	6
RF33D, P	SNF32J, N	SN74104J, N	6
RF33K	SNF32U	SN74104W	6
RF50D, P	SNF50J, N	SN5470J, N	6
RF50K	SNF50U	SN5470W	6
RF51D, P	SNF51J, N	SN5470J, N	6
RF51K	SNF51U	SN5470W	6
RF52D, P	SNF52J, N	SN7470J, N	6
RF52K	SNF52U	SN7470W	6
RF53D, P	SNF53J, N	SN7470J, N	6
RF53K	SNF53U	SN7470W	6
RF60D, P	SNF60J, N	SN54H101J, N	7
RF60K	SNF60U	SN54H101W	7
RF61D, P	SNF61J, N	SN54H101J, N	7
RF61K	SNF61U	SN54H101W	7
RF62D, P	SNF62J, N	SN74H101J, N	7
RF62K	SNF62U	SN74H101W	7
RF63D, P	SNF63J, N	SN74H101J, N	7
RF63K	SNF63U	SN74H101W	7
RF100D, P	SNF100J, N	SN54H103J, N	7
RF100K	SNF100U	SN54H103W	7
RF101D, P	SNF101J, N	SN54H103J, N	7
RF101K	SNF101U	SN54H103W	7
RF102D, P	SNF102J, N	SN74H103J, N	7
RF102K	SNF102U	SN74H103W	7
RF103D, P	SNF103J, N	SN74H103J, N	7
RF103K	SNF103U	SN74H103W	7
RF110D, P	SNF110J, N	SN54H108J, N	7
RF110K	SNF110U	SN54H108W	7
RF111D, P	SNF111J, N	SN54H108J, N	7
RF111K	SNF111U	SN54H108W	7
RF112D, P	SNF112J, N	SN74H108J, N	7
RF112K	SNF112U	SN74H108W	7
RF113K, P	SNF113J, N	SN74H108J, N	7
RF113K	SNF113U	SN74H108W	7
RF120D, P	SNF120J, N	SN54H103J, N	7
RF120K	SNF120U	SN54H103W	7
RF121D, P	SNF121J, N	SN54H103J, N	7
RF121K	SNF121U	SN54H103W	7
RF122D, P	SNF122J, N	SN74H103J, N	7
RF122K	SNF122U	SN74H103W	7
RF123D, P	SNF123J, N	SN74H103J, N	7
RF123K	SNF123U	SN74H103W	7
RF130D, P	SNF130J, N	SN54H108J, N	7
RF130K	SNF130U	SN54H108W	7
RF131D, P	SNF131J, N	SN54H108J, N	7
RF131K	SNF131U	SN54H108W	7
RF132D, P	SNF132J, N	SN74H108J, N	7
RF132K	SNG132U	SN74H108W	7
RF133D, P	SNF133J, N	SN74H108J, N	7
RF133K	SNF133U	SN74H108W	7
RF200D, P	SNF200J, N	SN54H102J, N	7
RF200K	SNF200U	SN54H102W	7
RF201D, P	SNF201J, N	SN54H102J, N	7
RF201K	SNF201U	SN54H102W	7
RF202D, P	SNF202J, N	SN74H102J, N	7
RF202K	SNF202U	SN74H102W	7
RF203D, P	SNF203J, N	SN74H102J, N	7
RF203K	SNF203U	SN74H102W	7
RF210D, P	SNF210J, N	SN54H101J, N	7
RF210K	SNF210U	SN54H101W	7
RF211D, P	SNF211J, N	SN54H101J, N	7
RF211K	SNF211U	SN54H101W	7
RF212D, P	SNF212J, N	SN74H101J, N	7
RF212K	SNF212U	SN74H101W	7
RF213D, P	SNF213J, N	SN74H101J, N	7
RF213K	SNF213U	SN74H101W	7
RF250D, P	SNF250J, N	SN54H102J, N	7
RF250K	SNF250U	SN54H102W	7
RF251D, P	SNF251J, N	SN54H102J, N	7
RF251K	SNF251U	SN54H102W	7
RF252D, P	SNF252J, N	SN74H102J, N	7
RF252K	SNF252U	SN74H102W	7
RF253D, P	SNF253J, N	SN74H102J, N	7
RF253K	SNF253U	SN74H102W	7
RF260D, P	SNF260J, N	SN54H101J, N	7
RF260K	SNF260U	SN54H101W	7
RF261D, P	SNF261J, N	SN54H101J, N	7
RF261K	SNF261U	SN54H101W	7
RF262D, P	SNF262J, N	SN74H101J, N	7
RF262K	SNF262U	SN74H101W	7
RF263D, P	SNF263J, N	SN74H101J, N	7
RF263K	SNF263U	SN74H101W	7
RF3120D, P		SN54S112J, N	5
RF3120K		SN54S112W	5
RF3122D, P		SN74S112J, N	5
RF3122K		SN74S112W	5
RF3130D, P		SN54S114J, N	5
RF3130K		SN54S114W	5
RF3132D, P		SN74S114J, N	5
RF3132K		SN74S114W	5
RF3200D, P		SN54S112J, N	5
RF3200K		SN54S112J, N	5
RF3202D, P		SN74S112J, N	5
RF3202K		SN74S112W	5
RF3210D, P		SN54S112J, N	5
RF3210K		SN54S112W	5
RF3212D, P		SN74S112J, N	5
RF3212K		SN74S112W	5
RF3220D, P		SN54S74J, N	5
RF3220K		SN54S74W	5
RF3222D, P		SN74S74J, N	5
RF3222K		SN74S74W	5
RG40D, P	SNG40J, N	SN5420J, N	6
RG40K	SNG40U	SN5420W	6
RG41D, P	SNG41J, N	SN5420J, N	6
RG41K	SNG41U	SN5420W	6
RG42D, P	SNG42J, N	SN7420J, N	6
RG42K	SNG42U	SN7420W	6
RG43D, P	SNG43J, N	SN7420J, N	6
RG43K	SNG43U	SN7420W	6
RG50D, P	SNG50J, N	SN5453J, N	6
RG50K	SNG50U	SN5453W	6

Raytheon TTL, Cont.

B

Type Number	Direct Replacement	Recommended for New Designs	Sec.
RG51D, P	SNG51J, N	SN5453J, N	6
RG51K	SNG51U	SN5453W	6
RG52D, P	SNG52J, N	SN7453J, N	6
RG52K	SNG52U	SN7453W	6
RG53D, P	SNG53J, N	SN7453J, N	6
RG53K	SNG53U	SN7453W	6
RG60D, P	SNG60J, N	SN5430J, N	6
RG60K	SNG60U	SN5430W	6
RG61D, P	SNG61J, N	SN5430J, N	6
RG61K	SNG61U	SN5430W	6
RG62D, P	SNG62J, N	SN7430J, N	6
RG62K	SNG62U	SN7430W	6
RG63D, P	SNG63J, N	SN7430J, N	6
RG63K	SNG63U	SN7430W	6
RG70D, P	SNG70J, N	SN5450J, N	6
RG70K	SNG70U	SN5450W	6
RG71D, P	SNG71J, N	SN5450J, N	6
RG71K	SNG71U	SN5450W	6
RG72D, P	SNG72J, N	SN7450J, N	6
RG72K	SNG72U	SN7450W	6
RG73D, P	SNG73J, N	SN7450J, N	6
RG73K	SNG73U	SN7450W	6
RG80D, P	SNG80J, N	SN5413J, N	6
RG80K	SNG80U	SN5413W	6
RG81D, P	SNG81J, N	SN5413J, N	6
RG81K	SNG81U	SN5413W	6
RG82D, P	SNG82J, N	SN7413J, N	6
RG82K	SNG82U	SN7413W	6
RG83D, P	SNG83J, N	SN7413J, N	6
RG83K	SNG83U	SN7413W	6
RG90D, P	SNG90J, N	SN5486J, N	9
RG90K	SNG90U	SN5486W	9
RG91D, P	SNG91J, N	SN5486J, N	9
RG91K	SNG91U	SN5486W	9
RG92D, P	SNG92J, N	SN7486J, N	9
RG92K	SNG92U	SN7486W	9
RG93D, P	SNG93J, N	SN7486J, N	9
RG93K	SNG93U	SN7486W	9
RG100D, P	SNG100J, N	SN5453J, N	6
RG100K	SNG100U	SN5453W	6
RG101D, P	SNG101J, N	SN5453J, N	6
RG101K	SNG101U	SN5453W	6
RG102D, P	SNG102J, N	SN5453J, N	6
RG102K	SNG102U	SN5453W	6
RG103D, P	SNG103J, N	SN7454J, N	6
RG103K	SNG103U	SN7453W	6
RG110D, P	SNG110J, N	SN54H55J, N	7
RG110K	SNG110U	SN54H55W	7
RG111D, P	SNG111J, N	SN54H55J, N	7
RG111K	SNG111U	SN54H55W	7
RG112D, P	SNG112J, N	SN74H55J, N	7
RG112K	SNG112U	SN74H55W	7
RG113D, P	SNG113J, N	SN74H55J, N	7
RG113K	SNG113U	SN74H55W	7
RG120D, P	SNG120J, N	SN5430J, N	6
RG120K	SNG120U	SN5430W	6
RG121D, P	SNG121J, N	SN5430J, N	6
RG121K	SNG121U	SN5430W	6
RG122D, P	SNG122J, N	SN7430J, N	6
RG122K	SNG122U	SN7430W	6
RG123D, P	SNG123J, N	SN7430J, N	6
RG123K	SNG123U	SN7430W	6
RG130D, P	SNG130J, N	SN54S140J, N	5
RG130K	SNG130U	SN54S140W	5
RG131D, P	SNG131J, N	SN54S140J, N	5
RG131K	SNG131U	SN54S140W	5
RG132D, P	SNG132J, N	SN74S140J, N	5
RG132K	SNG132U	SN74S140W	5
RG133D, P	SNG133J, N	SN74S140J, N	5
RG133K	SNG133U	SN74S140W	5
RG140D, P	SNG140J, N	SN5400J, N	6
RG140K	SNG140U	SN5400W	6
RG141D, P	SNG141J, N	SN5400J, N	6
RG141K	SNG141U	SN5400W	6
RG142D, P	SNG142J, N	SN7400J, N	6
RG142K	SNG142U	SN7400W	6
RG143D, P	SNG143J, N	SN7400J, N	6
RG143K	SNG143U	SN7400W	6
RG150D, P	SNG150J, N	SN54H62J, N	7
RG150K	SNG150U	SN54H62W	7
RG151D, P	SNG151J, N	SN54H62J, N	7
RG151K	SNG151U	SN54H62W	7
RG152D, P	SNG152J, N	SN74H62J, N	7
RG152K	SNG152U	SN74H62W	7
RG153D, P	SNG153J, N	SN74H62J, N	7
RG153K	SNG153U	SN74H62W	7
RG160D, P	SNG160J, N	SN5438J, N	6
RG160K	SNG160U	SN5438W	6
RG161D, P	SNG161J, N	SN5438J, N	6
RG161K	SNG161U	SN5438W	6
RG162D, P	SNG162J, N	SN7438J, N	6
RG162K	SNG162U	SN7438W	6
RG163D, P	SNG163J, N	SN7438J, N	6
RG163K	SNG153U	SN7438W	6
RG170D, P	SNG170J, N	SN5460J, N	6
RG170K	SNG170U	SN5460W	6
RG171D, P	SNG171J, N	SN5460J, N	6
RG171K	SNG171U	SN5460W	6
RG172D, P	SNG172J, N	SN7460J, N	6
RG172K	SNG172U	SN7460W	6
RG173D, P	SNG173J, N	SN7460J, N	6
RG173K	SNG173U	SN7460W	6
RG180D, P	SNG180J, N	SN5430J, N	6
RG180K	SNG180U	SN5430W	6
RG181D, P	SNG181J, N	SN5430J, N	6
RG181K	SNG181U	SN5430W	6
RG182D, P	SNG182J, N	SN7430J, N	6
RG182K	SNG182U	SN7430W	6
RG183D, P	SNG183J, N	SN7430J, N	6
RG183K	SNG183U	SN7430W	6
RG190D, P	SNG190J, N	SN5410J, N	6
RG190K	SNG191U	SN5410W	6
EG191D, P	SNG191J, N	SN5410J, N	6
RG191K	SNG191U	SN5410W	6
RG192D, P	SNG192J, N	SN7410J, N	6
RG192K	SNG192U	SN7410W	6
RG193D, P	SNG193J, N	SN7410J, N	6
RG193K	SNG193U	SN7410W	6
RG200D, P	SNG200J, N	SN54H30J, N	7
RG200K	SNG200U	SN54H30W	7
RG201D, P	SNG201J, N	SN54H30J, N	7
RG201K	SNG201U	SN54H30W	7
RG202D, P	SNG202J, N	SN74H30J, N	7
RG202K	SNG202U	SN74H30W	7
RG203D, P	SNG203J, N	SN74H30J, N	7
RG203K	SNG203U	SN74H30W	7
RG210D, P	SNG210J, N	SN54H55J, N	7
RG210K	SNG210U	SN54H55W	7
RG211D, P	SNG211J, N	SN54H55J, N	7
RG211K	SNG211U	SN54H55W	7
RG212D, P	SNG212J, N	SN74H55J, N	7
RG212K	SNG212U	SN74H55W	7
RG213D, P	SNG213J, N	SN74H55J, N	7
RG213K	SNG213U	SN74H55W	7
RG220D, P	SNG220J, N	SN54H00J, N	7
RG220K	SNG220U	SN54H00W	7

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Raytheon TTL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
RG221D, P	SNG221J, N	SN54H00J, N	7
RG221K	SNG221U	SN54H00W	7
RG222D, P	SNG222J, N	SN74H00J, N	7
RG222K	SNG222U	SN74H00W	7
RG223D, P	SNG223J, N	SN74H00J, N	7
RG223K	SNG223U	SN74H00W	7
RG230D, P	SNG230J, N	SN74H62J, N	7
RG230K	SNG230U	SN74H62W	7
RG231D, P	SNG231J, N	SN54H62J, N	7
RG231K	SNG231U	SN54H62W	7
RG232D, P	SNG232J, N	SN74H62J, N	7
RG232K	SNG232U	SN74H62W	7
RG233D, P	SNG233J, N	SN74H62J, N	7
RG233K	SNG233U	SN74H62W	7
RG240D, P	SNG240J, N	SN54H20J, N	7
RG240K	SNG240U	SN54H20W	7
RG241D, P	SNG241J, N	SN54H20J, N	7
RG241K	SNG241U	SN54H20W	7
RG242D, P	SNG242J, N	SN74H20J, N	7
RG242K	SNG242U	SN74H20W	7
RG243D, P	SNG243J, N	SN74H20J, N	7
RG243K	SNG243U	SN74H20W	7
RG250D, P	SNG250J, N	SN54H53J, N	7
RG250K	SNG250U	SN54H53W	7
RG251D, P	SNG251J, N	SN54H53J, N	7
RG251K	SNG251U	SN54H53W	7
RG252D, P	SNG252J, N	SN74H53J, N	7
RG252K	SNG252U	SN74H53W	7
RG253D, P	SNG253J, N	SN74H53J, N	7
RG253K	SNG253U	SN74H53W	7
RG260D, P	SNG260J, N	SN54H30J, N	7
RG260K	SNG260U	SN54H30W	7
RG261D, P	SNG261J, N	SN54H30J, N	7
RG261K	SNG261U	SN54H30W	7
RG262D, P	SNG262J, N	SN74H30J, N	7
RG262K	SNG262U	SN74H30W	7
RG263D, P	SNG263J, N	SN74H30J, N	7
RG263K	SNG263U	SN74H30W	7
RG270D, P	SNG270J, N	SN54H60J, N	7
RG270K	SNG270U	SN54H60W	7
RG271D, P	SNG271J, N	SN54H60J, N	7
RG271K	SNG271U	SN54H60W	7
RG272D, P	SNG272J, N	SN74H60J, N	7
RG272K	SNG272U	SN74H60W	7
RG273D, P	SNG273J, N	SN74H60J, N	7
RG273K	SNG273U	SN74H60W	7
RG280D, P	SNG280J, N	SN54H52J, N	7
RG280K	SNG280U	SN54H52J, N	7
RG281D, P	SNG281J, N	SN54H52J, N	7
RG281K	SNG281U	SN54H52W	7
RG282D, P	SNG282J, N	SN74H52J, N	7
RG282K	SNG282U	SN74H52W	7
RG283D, P	SNG283J, N	SN74H52J, N	7
RG283K	SNG283U	SN74H52W	7
RG290D, P	SNG290J, N	SN54H62J, N	7
RG290K	SNG290U	SN54H62W	7
RG291D, P	SNG291J, N	SN54H62J, N	7
RG291K	SNG291U	SN54H62W	7
RG292D, P	SNG292J, N	SN74H62J, N	7
RG292K	SNG292U	SN74H62W	7
RG293D, P	SNG293J, N	SN74H62J, N	7
RG293K	SNG293U	SN74H62W	7
RG300D, P	SNG300J, N	SN54H53J, N	7
RG300K	SNG300U	SN54H53W	7
RG301D, P	SNG301J, N	SN54H53J, N	7
RG301K	SNG301U	SN54H53W	7
RG302D, P	SNG302J, N	SN74H53J, N	7
RG302K	SNG302U	SN74H53W	7
RG303D, P	SNG303J, N	SN74H53J, N	7
RG303K	SNG303U	SN74H53W	7
RG310D, P	SNG310J, N	SN54H50J, N	7
RG310K	SNG310U	SN54H50W	7
RG311D, P	SNG311J, N	SN54H50J, N	7
RG311K	SNG311U	SN54H50W	7
RG312D, P	SNG312J, N	SN74H50J, N	7
RG312K	SNG312U	SN74H50W	7
RG313D, P	SNG313J, N	SN74H50J, N	7
RG313K	SNG313U	SN74H50W	7
RG320D, P	SNG320J, N	SN54H10J, N	7
RG320K	SNG320U	SN54H10W	7
RG321D, P	SNG321J, N	SN54H10J, N	7
RG321K	SNG321U	SN54H10W	7
RG322D, P	SNG322J, N	SN74H10J, N	7
RG322K	SNG322U	SN74H10W	7
RG323D, P	SNG323J, N	SN74H10J, N	7
RG323K	SNG323U	SN74H10W	7
RG370D, P	SNG370J, N	SN5404J, N	6
RG370K	SNG370U	SN5404W	6
RG371D, P	SNG371J, N	SN5404J, N	6
RG371K	SNG371U	SN5404W	6
RG372D, P	SNG372J, N	SN7404J, N	6
RG372K	SNG372U	SN7404W	6
RG373D, P	SNG373J, N	SN7404J, N	6
RG373K	SNG373U	SN7404W	6
RG380D, P	SNG380J, N	SN54H04J, N	7
RG380K	SNG380U	SN54H04W	7
RG381D, P	SNG381J, N	SN54H04J, N	7
RG381K	SNG381U	SN54H04W	7
RG382D, P	SNG382J, N	SN74H04J, N	7
RG382K	SNG382U	SN74H04W	7
RG383D, P	SNG383J, N	SN74H04J, N	7
RG383K	SNG383U	SN74H04W	7
RG3180D, P		SN54S15J, N	5
RG3180K		SN54S15W	5
RG3182D, P		SN74S15J, N	5
RG3182K		SN74S15W	5
RG3200D, P		SN54H30J, N	7
RG3200K		SN54H30W	7
RG3202D, P		SN74H30J, N	7
RG3202K		SN74H30W	7
RG3210D, P		SN54S65J, N	5
RG3210K		SN54S65W	5
RG3212D, P		SN74S65J, N	5
RG3212K		SN74S65W	5
RG3220D, P		SN54S00J, N	5
RG3220K		SN54SooW	5
RG3222D, P		SN74S00J, N	5
RG3222K		SN74S00W	5
RG3230D, P		SN54S65J, N	5
RG3230K		SN54S65W	5
RG3232D, P		SN74S65J, N	5
RG3232K		SN74S65W	5
RG3240D, P		SN54S20J, N	5
RG3240K		SN54S20W	5
RG3242D, P		SN74S20J, N	5
RG3242K		SN74S20W	5
RG3250D, P		SN54S65J, N	5
RG3250K		SN54S65W	5
RG3252D, P		SN74S65J, N	5
RG3252K		SN74S65W	5
RG3260D, P		SN54H30J, N	7
RG3260K		SN54H30W	7
RG3262D, P		SN74H30J, N	7
RG3262K		SN74H30W	7

DTL/TTL CIRCUITS

Raytheon TTL, Cont.

B

Type Number	Direct Replacement	Recommended for New Designs	Sec.
RG3270D, P		SN54S65J, N	5
RG3270K		SN54S65W	5
RG3272D, P		SN74S65J, N	5
RG3272K		SN74S65W	5
RG3310D, P		SN54S65J, N	5
RG3310K		SN54S65W	5
RG3312D, P		SN74S65J, N	5
RG3312K		SN74S65W	5
RG3320D, P		SN54S10J, N	5
RG3320K		SN54S10W	5
RG3322D, P		SN74S10J, N	5
RG3322K		SN74S10W	5
RG3380D, P		SN54S04J, N	5
RG3380K		SN54S04W	5
RG3382D, P		SN74S04J, N	5
RG3382K		SN74S04W	5
RG3390D, P		SN54S15J, N	5
RG3390K		SN54S15W	5
RG3392D, P		SN74S15J, N	5
RG3392K		SN74S15W	5
RG3400D, P		SN54S15J, N	5
RG3400K		SN54S15W	5
RG3402D, P		SN74S15J, N	5
RG3402K		SN74S15W	5
RG3420D, P		SN54S22J, N	5
RG3420K		SN54S22W	5
RG3422D, P		SN74S22J, N	5
RG3422K		SN74S22W	5
RG3440D, P		SN54S65J, N	5
RG3440K		SN54S65W	5
RG3442D, P		SN74S65J, N	5
RG3442K		SN74S65W	5
RL10D, P		SN54H183J, N	9
RL10K		SN54H183W	9
RL11D, P		SN54H183J, N	9
RL11K		SN54H183W	9
RL12D, P		SN74H183J, N	9
RL12K		SN74H183W	9
RL13D, P		SN74H183J, N	9
RL13K		SN74H183W	9
RL20D, P	SNG20J, N	SN54181J, N	9
RL20K	SNG20U	SN54181W	9
RL21D, P	SNG21J, N	SN54181J, N	9
RL21K	SNG21U	SN54181W	9

Type Number	Direct Replacement	Recommended for New Designs	Sec.
RL22D, P	SNG22J, N	SN74181J, N	9
RL22K	SNG22U	SN74181W	9
RL23D, P	SNG23J, N	SN74181J, N	9
RL23K	SNG23U	SN74181W	9
RL30D, P	SNG30J, N	SN54181J, N	9
RL30K	SNG30U	SN54181W	9
RL31D, P	SNG31J, N	SN54181J, N	9
RL31K	SNG31U	SN54181W	9
RL32D, P	SNG32J, N	SN74181J, N	9
RL32K	SNG32U	SN74181W	9
RL33D, P	SNG33J, N	SN74181J, N	9
RL33K	SNG33U	SN74181W	9
RL40D, P	SNG40J, N	SN54182J, N	9
RL40K	SNG40U	SN54182W	9
RL41D, P	SNG41J, N	SN54182J, N	9
RL41K	SNG41U	SN54182W	9
RL42D, P	SNG42J, N	SN74182J, N	9
RL42K	SNG42U	SN74182W	9
RL43D, P	SNG43J, N	SN74182J, N	9
RL43K	SNG43U	SN74182W	9
RL60D, P	SNG60J, N	SN5475J, N	9
RL60K	SNG60U	SN5475W	9
RL61D, P	SNG61J, N	SN5475J, N	9
RL61K	SNG61U	SN5475W	9
RL62D, P	SNG62J, N	SN7475J, N	9
RL62K	SNG62U	SN7475W	9
RL63D, P	SNG63J, N	SN7475J, N	9
RL63K	SNG63U	SN7475W	9
RL70D, P	SNG70J, N	SN5475J, N	9
RL70K	SNG70U	SN5475W	9
RL71D, P	SNG71J, N	SN5475J, N	9
RL71K	SNG71U	SN5475W	9
RL72D, P	SNG72J, N	SN7475J, N	9
RL72K	SNG72U	SN7475W	9
RL73D, P	SNG73J, N	SN7475J, N	9
RL73K	SNG73U	SN7475W	9
RL80D, P	SNG80J, N	SN5489J, N	9
RL80K	SNG80U	SN5489W	9
RL81D, P	SNG81J, N	SN5489J, N	9
RL81K	SNG81U	SN5489W	9
RL82D, P	SNG82J, N	SN7489J, N	9
RL82K	SNG82U	SN7489W	9
RL83D, P	SNG83J, N	SN7489J, N	9
RL83K	SNG83U	SN7489W	9

Signetics DCL

Type Number	Direct Replacement	Recommended for New Designs	Sec.
N8H16A	SN74H20J, N	SN74H20J, N	7
N8H16J		SN74H20W	7
N8H20Q		SN74H103W	7
N8H21A		SN74H108J, N	7
N8H21Q		SN74H108W	7
N8H22B		SN74H106J, N	7
N8H70A	SN74H11J, N	SN74H11J, N	7
N8H70J		SN74H11W	7
N8H80A	SN74H00J, N	SN74H00J, N	7
N8H80J		SN74H00W	7
N8H90A	SN74H04J, N	SN74H04J, N	7
N8H90J	SN74H04W	SN74H04W	7
N8T01B		SN74141J, N	9
N8T04B		SN7447AJ, N	9

Type Number	Direct Replacement	Recommended for New Designs	Sec.
N8T04R		SN7447AJ, N	9
N8T05B		SN7448J, N	9
N8T05R		SN7448W	9
N8T13B		SN74S140J, N	5
N8T13R		SN74S140W	5
N8T14B		SN7413J, N	6
N8T14R		SN7413W	6
N8T80A		SN7426J, N	6
N8T80J		SN7426W	6
N8T90A		SN7406J, N	6
N8T90J		SN7406W	6
N1283A		SN7484J, N	9
N8162A		SN74121J, N	6
N8162J		SN74121W	6

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Signetics DCL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
N8200P		SN74198W	9
N8200Y		SN74198J, N	9
N8201P		SN74198W	9
N8201Y		SN74198J, N	9
N8202P		SN74198W	9
N8202Y		SN74198J, N	9
N8203P		SN74198W	9
N8203Y		SN74198J, N	9
N8224B	SN7488AJ, N	SN7488AJ, N	9
N8224R	SN7488W	SN7488W	9
N8230B		SN74151J, N	9
N8231B		SN74151J, N	9
N8232B		SN74151J, N	9
N8233B		SN74153J, N	9
N8234B		SN74153J, N	9
N8235B		SN74153J, N	9
N8241A		SN7486J, N	9
N8241Q		SN7486W	9
N8242A		SN7485J, N	9
N8242Q		SN7485W	9
N8243P		SN74198W	9
N8243Y		SN74198J, N	9
N8250A		SN7442J, N	9
N8250J		SN7442W	9
N8251B		SN7442J, N	9
N8260P		SN74181W	9
N8261A		SN74182J, N	9
N8261Q		SN74182W	9
N8262A		SN74180J, N	9
N8262Q		SN74180W	9
N8263P		SN74153W	9
N8263Y		SN74153J, N	9
N8264P		SN74153W	9
N8264Y		SN74153J, N	9
N8266B		SN74153J, N	9
N8266R		SN74153J, N	9
N8267B		SN74153J, N	9
N8267R		SN74153W	9
N8268A	SN7480J, N	SN74181J, N	9
N8268Q	SN7480W	SN74181W	9
N8270A		SN74194J, N	9
N8270J		SN74194W	9
N8271B		SN74194J, N	9
N8275B		SN7475J, N	9
N8275R		SN7475W	9
N8276A		SN7491AJ, N	9
N8276Q		SN7491A, W	9
N8280A		SN74196J, N	9
N8280J		SN74196W	9
N8281A		SN74197J, N	9
N8281J		SN74197W	9
N8284A		SN74191J, N	9
N8284Q		SN74191W	9
N8285A		SN74190J, N	9
N8285Q		SN74190W	9
N8288A		SN74163J, N	9
N8288Q		SN74163W	9
N8290A	SN74196J, N	SN74196J, N	9
N8290Q	SN74196W	SN74196W	9
N8291A	SN74197J, N	SN74197J, N	9
N8291Q	SN74197W	SN74197W	9
N8292A		SN74L90J, N	9
N8292Q		SN74L90R	9
N8293A		SN74197J, N	9
N8293Q		SN74197R	9
N8415A	SN151800J, N	SN7420J, N	6
N8415J		SN7420W	6
N8416A	SN15830J, N	SN7420J, N	6
N8416J		SN7420J, N	6
N8417A		SN7410J, N	6
N8417J		SN7410W	6
N8424A		SN74111J, N	6
N8424J		SN74111W	6
N8425A		SN74111J, N	6
N8425J		SN74111W	6
N8440A		SN7450J, N	6
N8440J		SN7450W	6
N8455A	SN7440J, N	SN7440J, N	6
N8455J		SN7440W	6
N8470A, F	SN7410J, N	SN7410J, N	6
N8470J		SN7410J, N	6
N8471A	SN7412J, N	SN7412J, N	6
N8471J		SN7412W	6
N8480A	SN7400J, N	SN7400J, N	6
N8480J		SN7400J, N	6
N8481A	SN7403J, N	SN7403J, N	6
N8481J		SN7403W	6
N8490A	SN7404J, N	SN7404J, N	6
N8490J	SN7404W	SN7404W	6
N8706A		SN7460J, N	6
N8706J		SN7460W	6
N8731A		SN7460J, N	6
N8731J		SN7460W	6
N8806J	SN7460W	SN7460W	6
N8808A	SN7430J, N	SN7430J, N	6
N8808J	SN7430W	SN7430W	6
N8815A	SN7425J, N	SN7425J, N	6
N8815J		SN7425W	6
N8816A		SN7420J, N	6
N8816J	SN7420W	SN7420W	6
N8821J		SN7476W	6
N8822A		SN7473J, N	6
N8822J	SN7473W	SN7473W	6
N8824B		SN7476J, N	6
N8825A	SN7470J, N	SN7470J, N	6
N8825J	SN7470W	SN7470W	6
N8826A		SN74107J, N	6
N8826J		SN7473W	6
N8827A		SN7476J, N	6
N8827J		SN7476W	6
N8824A	SN7474J, N	SN7474J, N	6
N8824J	SN7474W	SN7474W	6
N8829A	SN74110J, N	SN74110J, N	6
N8829J		SN74110W	6
N8840A	SN7450J, N	SN7450J, N	6
N8840J	SN7450W	SN7450W	6
N8848A	SN74H54J, N	SN74H54J, N	7
N8848J	SN74H54W	SN74H54W	7
N8855A		SN7440J, N	6
N8855J	SN7440W	SN7440W	6
N8870A		SN7410J, N	6
N8870J		SN7410W	6
N8875A	SN7427J, N	SN7427J, N	6
N8875J		SN7427W	6
N8880A		SN7400J, N	6
N8880J	SN7400W	SN7400W	6
N8881A	SN7401J, N	SN7401J, N	6
N8881J	SN7401W	SN7401W	6
N8885A		SN7402J, N	6
N8885J		SN7402W	6
N8890A	SN7404J, N	SN7404J, N	6
N8890Q	SN7404W	SN7404W	6
N8891A	SN7405J, N	SN7405J, N	6

Sginetics DCL, Cont.

B

Type Number	Direct Replacement	Recommended for New Designs	Sec.
N8891Q	SN7405W	SN7405W	6
S8H16A, F	SN54H20J, N	SN54H20J, N	7
S8H16J		SN54H20W	7
58H20Q		SN54H103W	7
S8H21A, F		SN54H108J, N	7
S8H21Q		SN54H108W	7
S8H22B, E		SN54H106J, N	7
S8H70A, F	SN54H11J, N	SN54H11J, N	7
S8H70J		SN54H11W	7
S8H80A, F	SN54H00J, N	SN54H00J, N	7
S8H80J		SN54H00W	7
S8H90A, F	SN54H04J, N	SN54H04J, N	7
S8H90J	SN54H04W	SN54H04W	7
S8T01B		SN74141J, N	9
S8T04B, E		SN5447AJ, N	9
S8T04R		SN5447AJ, N	9
S8T05B, E		SN5448J, N	9
S8T05R		SN5448W	9
S8T13B, E		SN54S140J, N	5
S8T13R		SN54S140W	5
S8T14B		SN5413J, N	6
S8T14R		SN5413W	6
S8T80A, F		SN5426J, N	6
S8T80J		SN5426W	6
S8T90A, F		SN5406J, N	6
S8T90J		SN5406W	6
S8162A, F		SN54121J, N	6
S8162J		SN54121W	6
S8200P		SN54198W	9
S8200Y		SN54198J, N	9
S8201P		SN54198W	9
S8201Y		SN54198J, N	9
S8202P		SN54198W	9
S8202Y		SN54198J, N	9
S8203P		SN54198W	9
S8203Y		SN54198J, N	9
S8224B	SN5488AJ, N	SN7488AJ, N	9
S8224R	SN5488W	SN5488W	9
S8230B, E		SN54151J, N	9
S8231B, E		SN54151J, N	9
S8232B, E		SN54151J, N	9
S8233B, E		SN54153J, N	9
S8234B, E		SN54153J, N	9
S8235B, E		SN54153J, N	9
S8241A, F		SN5486J, N	9
S8241Q		SN5486W	9
S8242A, F		SN5485J, N	9
S8242Q		SN5485W	9
S8243P		SN54198W	9
S8243Y		SN54198J, N	9
S8250A		SN5442J, N	9
S8250J		SN5442W	9
S8251B		SN5442J, N	9
S8260P		SN54181W	9
S8261A, F		SN54182J, N	9
S8261Q		SN54182W	9
S8262A, F		SN54180J, N	9
S8262Q		SN54180W	9
S8263P		SN54153W	9
S8263Y		SN54153J, N	9
S8264P		SN54153W	9
S8264Y		SN54153J, N	9
S8266B, E		SN54153J, N	9
S8267R		SN54153W	9
S8268A, F	SN5480J, N	SN54181J, N	9
S8268Q	SN5480W	SN54181W	9
S8270A		SN54194J, N	9
S8270J		SN54194W	9
S8271B		SN54194J, N	9
S8275B, E		SN5475J, N	9
S8275R		SN5475W	9
S8276A, F		SN5491J, N	9
S8276Q		SN5491A, W	9
S8280A		SN54196J, N	9
S8280J		SN54196W	9
S8281A		SN54197J, N	9
S8281J		SN54197W	9
S8284A		SN54191J, N	9
S8284Q		SN54191W	9
S8285A		SN54190J, N	9
S8285Q		SN54190W	9
S8288A		SN54163J, N	9
S8288Q		SN54163W	9
S8290A	SN54196J, N	SN54196J, N	9
S8290Q	SN54196W	SN54196W	9
S8291A	SN54197J, N	SN54197J, N	9
S8291Q	SN54197W	SN54197W	9
S8292A		SN54L90J, N	9
S8292Q		SN54L90R	9
S8293A		SN54197J, N	9
S8293Q		SN54197R	9
S8415A	SN151900J, N	SN5420J, N	6
S8415J		SN5420W	6
S8416A	SN15930J, N	SN5420J, N	6
S8416J		SN5420J, N	6
S8417A		SN5410J, N	6
S8417J		SN5410W	6
S8424A		SN54111J, N	6
S8424J		SN54111W	6
S8425A		SN54111J, N	6
S8425J		SN54111W	6
S8440A, F		SN5450J, N	6
S8440J		SN5450W	6
S8455A, F	SN5440J, N	SN5440J, N	6
S8455J		SN5440W	6
S8470A, F	SN5410J, N	SN5410J, N	6
S8470J		SN5410J, N	6
S8471A, F	SN5412J, N	SN5412J, N	6
S8471J		SN5412W	6
S8480A, F	SN5400J, N	SN5400J, N	6
S8480J		SN5400J, N	6
S8481A, F	SN5403J, N	SN5403J, N	6
S8481J		SN5403W	6
S8490A, F	SN5404J, N	SN5404J, N	6
S8490J	SN5404W	SN5404W	6
S8706A, F		SN5460J, N	6
S8706J		SN5460W	6
S8731A, F		SN5460J, N	6
S8731J		SN5460W	6
S8806A, F	SN5460J, N	SN5460J, N	6
S8806J	SN5460W	SN5460W	6
S8808A, F	SN5430J, N	SN5430J, N	6
S8808J	SN5430W	SN5430W	6
S8815A, F	SN5425J, N	SN5425J, N	6
S8815J		SN5425W	6
S8816A, F		SN5420J, N	6
S8816J	SN5420W	SN5420W	6
S8821J		SN5476W	6
S8822A, F		SN5473J, N	6
S8822J	SN5473W	SN5473W	6
S8824B		SN5476J, N	6
S8825A, F	SN5470J, N	SN5470J, N	6
S8825J	SN5470W	SN5470W	6
S8826A, F		SN54107J, N	6

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DTL/TTL CIRCUITS

Signetics DCL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
S8826J		SN5473W	6
S8827A, F		SN5476J, N	6
S8827J		SN5476W	6
S8824A, F	SN5474J, N	SN5474J, N	6
S8824J	SN5474W	SN5474W	6
S8829A, F	SN54110J, N	SN54110J, N	6
S8829J		SN54110W	6
S8840A, F	SN5450J, N	SN5450J, N	6
S8840J	SN5450W	SN5450W	6
S8848A, F	SN54H54J, N	SN54H54J, N	7
S8848J	SN54H54W	SN54H54W	7
S8855A, F		SN5440J, N	6
S8855J	SN5440W	SN5440W	6
S8870A, F		SN5410J, N	6
S8870J		SN5410W	6
S8875A, F	SN5427J, N	SN5427J, N	6
S8875J		SN5427W	6
S8880A, F		SN5400J, N	6
S8880J	SN5400W	SN5400W	6
S8881A, F	SN5401J, N	SN5401J, N	6
S8881J	SN5401W	SN5401W	6
S8885A, F		SN5402J, N	6
S8885J		SN5402W	6
S8890A, F	SN5404J, N	SN5404J, N	6
S8890Q	SN5404W	SN5404W	6
S8891A, F	SN5405J, N	SN5405J, N	6
S8891Q	SN5405W	SN5405W	6

Signetics TTL

Type Number	Direct Replacement	Recommended for New Designs	Sec.
N7400A	SN7400J, N	SN7400J, N	6
N7400J	SN7400W	SN7400W	6
N7401A	SN7401J, N	SN7401J, N	6
N7401J	SN7401W	SN7401W	6
N7402A	SN7402J, N	SN7402J, N	6
N7402Q	SN7402W	SN7402W	6
N7403A	SN7403J, N	SN7403J, N	6
N7404A	SN7404J, N	SN7404J, N	6
N7404Q	SN7404W	SN7404W	6
N7405A	SN7405J, N	SN7405J, N	6
N7405Q	SN7405W	SN7405W	6
N7408A	SN7408J, N	SN7408J, N	6
N7408Q	SN7408W	SN7408W	6
N7410A	SN7410J, N	SN7410J, N	6
N7410J	SN7410W	SN7410W	6
N7420A	SN7420J, N	SN7420J, N	6
N7420J	SN7420W	SN7420W	6
N7430A	SN7430J, N	SN7430J, N	6
N7430J	SN7430W	SN7430W	6
N7440A	SN7440J, N	SN7440J, N	6
N7440Q	SN7440W	SN7440W	6
N7441B	SN7441J, N	SN7441J, N	9
N7450A	SN7450J, N	SN7450J, N	6
N7450J	SN7450W	SN7450W	6
N7451A	SN7451J, N	SN7451J, N	6
N7451J	SN7451W	SN7451W	6
N7453A	SN7453J, N	SN7453J, N	6
N7453J	SN7453W	SN7453W	6
N7454A	SN7454J, N	SN7454J, N	6
N7454J	SN7454W	SN7454W	6
N7460A	SN7460J, N	SN7460J, N	6
N7460J	SN7460W	SN7460W	6
N7470A	SN7470J, N	SN7470J, N	6
N7470J	SN7470W	SN7470W	6
N7472A	SN7472J, N	SN7472J, N	6
N7472J	SN7472W	SN7472W	6
N7473A	SN7473J, N	SN7473J, N	6
N7473J	SN7473W	SN7473W	6
N7474A	SN7474J, N	SN7474J, N	6
N7474J	SN7474W	SN7474W	6
N7475B	SN7575J, N	SN7475J, N	9
N7476B	SN7476J, N	SN7476J, N	6
N4777Q	SN7477W	SN7477W	9
N7480A	SN7480J, N	SN7480J, N	9
N7480Q	SN7480W	SN7480W	9
N7490A	SN7490J, N	SN7490J, N	9
N7490Q	SN7490W	SN7490W	9
N7491A	SN7491J, N	SN7491J, N	9
N7491Q	SN7491W	SN7491W	9
N7492A	SN7492J, N	SN7492J, N	9
N7492Q	SN7492W	SN7492W	9
N7493A	SN7493J, N	SN7493J, N	9
N7493Q	SN7493W	SN7493W	9
N74107A	SN74107J, N	SN74107J, N	6
N74H00A	SN74H00J, N	SN74H00J, N	7
N74H00Q	SN74H00W	SN74H00W	7
N74H01A	SN74H01J, N	SN74H01J, N	7
N74H01Q	SN74H01W	SN74H01W	7
N74H04A	SN74H04J, N	SN74H04J, N	7
N74H04Q	SN74H04W	SN74H04W	7
N74H05A	SN74H05J, N	SN74H05J, N	7
N74H05Q	SN74H05W	SN74H05W	7
N74H10A	SN74H10J, N	SN74H10J, N	7
N74H10Q	SN74H10W	SN74H10W	7
N74H11A	SN74H11J, N	SN74H11J, N	7
N74H11Q	SN74H11W	SN74H11W	7
N74H20A	SN74H20J, N	SN74H20J, N	7
N74H20Q	SN74H20W	SN74H20W	7
N74H21A	SN74H21J, N	SN74H21J, N	7
N74H21Q	SN74H21W	SN74H21W	7
N74H22A	SN74H22J, N	SN74H22J, N	7
N74H22Q	SN74H22W	SN74H22W	7
N74H30A	SN74H30J, N	SN74H30J, N	7
N74H30J	SN74H30W	SN74H30W	7
N74H40A	SN74H40J, N	SN74H40J, N	7
N74H40Q	SN74H40W	SN74H40W	7
N74H50A	SN74H50J, N	SN74H50J, N	7
N74H50Q	SN74H50W	SN74H50W	7
N74H51A	SN74H51J, N	SN74H51J, N	7
N74H51Q	SN74H51W	SN74H51W	7
N74H52A	SN74H52J, N	SN74H52J, N	7
N74H52Q	SN74H52W	SN74H52W	7
N74H53A	SN74H53J, N	SN74H53J, N	7
N74H53J	SN74H53W	SN74H53W	7
N74H54A	SN74H54J, N	SN74H54J, N	7
N74H54J	SN74H54W	SN74H54W	7
N74H55A	SN74H55J, N	SN74H55J, N	7
N74H55J	SN74H55W	SN74H55W	7

DTL/TTL CIRCUITS

Signetics TTL, Cont.

B

Type Number	Direct Replacement	Recommended for New Designs	Sec.
N74H60A	SN74H60J, N	SN74H60J, N	7
N74H60J	SN74H60W	SN74H60W	7
N74H61A	SN74H61J, N	SN74H61J, N	7
N74H61J	SN74H61W	SN74H61W	7
N74H62A	SN74H62J, N	SN74H62J, N	7
N74H62J	SN74H62W	SN74H62W	7
N74H72A	SN74H72J, N	SN74H72J, N	7
N74H72Q	SN74H72W	SN74H72W	7
N74H73A	SN74H73J, N	SN74H73J, N	7
N74H73Q	SN74H73W	SN74H73W	7
N74H74A	SN74H74J, N	SN74H74J, N	7
N74H74Q	SN74H74W	SN74H74W	7
N74H76B	SN74H76J, N	SN74H76J, N	7
S5400A	SN5400J, N	SN5400J, N	6
S5400J	SN5400W	SN5400W	6
S5401A	SN5401J, N	SN5401J, N	6
S5401J	SN5401W	SN5401W	6
S5402A	SN5402J, N	SN5402J, N	6
S5402Q	SN5402W	SN5402W	6
S5403A	SN5403J, N	SN5403J, N	6
S5404A	SN5404J, N	SN5404J, N	6
S5404Q	SN5404W	SN5404W	6
S5405A	SN5405J, N	SN5405J, N	6
S5405Q	SN5405W	SN5405W	6
S5408A	SN5408J, N	SN5408J, N	6
S5408Q	SN5408W	SN5408W	6
S5410A	SN5410J, N	SN5410J, N	6
S5410J	SN5410W	SN5410W	6
S5420A	SN5420J, N	SN5420J, N	6
S5420J	SN5420W	SN5420W	6
S5430A	SN5430J, N	SN5430J, N	6
S5430J	SN5430W	SN5430W	6
S5440A	SN5440J, N	SN5440J, N	6
S5440J	SN5440W	SN5440W	6
S5450A	SN5450J, N	SN5450J, N	6
S5450J	SN5450W	SN5450W	6
S5451A	SN5451J, N	SN5451J, N	6
S5451J	SN5451W	SN5451W	6
S5453A	SN5453J, N	SN5453J, N	6
S5453J	SN5453W	SN5453W	6
S5454A	SN5453J, N	SN5454J, N	6
S5354J	SN5454W	SN5454W	6
S5460A	SN5460J, N	SN5460J, N	6
S5460J	SN5460W	SN5460W	6
S5470A	SN5470J, N	SN5470J, N	6
S5470J	SN5470W	SN5470W	6
S5472A	SN5472J, N	SN5472J, N	6
S5472J	SN5472W	SN5472W	6
S5473A	SN5473J, N	SN5473J, N	6
S5473J	SN5473W	SN5473W	6
S5474A	SN5474J, N	SN5474J, N	6
S5474J	SN5474W	SN5474W	6
S5475B	SN5475J, N	SN5475J, N	9
S5476B	SN5476J, N	SN5476J, N	6
S5477Q	SN5477W	SN5477W	9
S5480A	SN5480J, N	SN5480J, N	9
S5480Q	SN5480W	SN5480W	9
S5490A	SN5490J, N	SN5490J, N	9
S5490Q	SN5490W	SN5490W	9
S5491A	SN5491J, N	SN5491J, N	9
S5491Q	SN5491W	SN5491W	9
S5492A	SN5492J, N	SN5492J, N	9
S5492Q	SN5492W	SN5492W	9
S5493A	SN5493J, N	SN5493J, N	9
S5493Q	SN5493W	SN5493W	9
S54107A	SN54107J, N	SN54107J, N	7
S54H00A	SN54H00J, N	SN54H00J, N	7
S54H00Q	SN54H00W	SN54H00W	7
S54H01A	SN54H01J, N	SN54H01J, N	7
S54H01Q	SN54H01W	SN54H01W	7
S54H04A	SN54H04J, N	SN54H04J, N	7
S54H04Q	SN54H04W	SN54H04W	7
S54H05A	SN54H05J, N	SN54H05J, N	7
S54H05Q	SN54H05W	SN54H05W	7
S54H10A	SN54H10J, N	SN54H10J, N	7
S54H10Q	SN54H10W	SN54H10W	7
S54H11A	SN54H11J, N	SN54H11J, N	7
S54H11Q	SN54H11W	SN54H11W	7
S54H20A	SN54H20J, N	SN54H20J, N	7
S54H20Q	SN54H20W	SN54H20W	7
S54H21A	SN54H21J, N	SN54H21J, N	7
S54H21Q	SN54H21W	SN54H21W	7
S54H22A	SN54H22J, N	SN54H22J, N	7
S54H22Q	SN54H22W	SN54H22W	7
S54H30A	SN54H30J, N	SN54H30J, N	7
S54H30Q	SN54H30W	SN54H30W	7
S54H50A	SN54H50J, N	SN54H50J, N	7
S54H50Q	SN54H50W	SN54H50W	7
S54H51A	SN54H51J, N	SN54H51J, N	7
S54H51Q	SN54H51W	SN54H51W	7
S54H52A	SN54H52J, N	SN54H52J, N	7
S54H52Q	SN54H52W	SN54H52W	7
S54H53A	SN54H53J, N	SN54H53J, N	7
S54H53J	SN54H53W	SN54H53W	7
S54H54A	SN54H54J, N	SN54H54J, N	7
S54H54J	SN54H54W	SN54H54W	7
S54H55A	SN54H55J, N	SN54H55J, N	7
S54H55J	SN54H55W	SN54H55W	7
S54H60A	SN54H60J, N	SN54H60J, N	7
S54H60J	SN54H60W	SN54H60W	7
S54H61A	SN54H61J, N	SN54H61J, N	7
S54H61J	SN54H61W	SN54H61W	7
S54H62A	SN54H62J, N	SN54H62J, N	7
S54H62J	SN54H62W	SN54H62W	7
S54H72A	SN54H72J, N	SN54H72J, N	7
S54H72Q	SN54H72W	SN54H72W	7
S54H73A	SN54H73J, N	SN54H73J, N	7
S54H73Q	SN54H73W	SN54H73W	7
S54H74A	SN54H74J, N	SN54H74J, N	7
S54H74Q	SN54H74W	SN54H74W	7
S54H76B	SN54H76J, N	SN54H76J, N	7

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Sprague TTL

Type Number	Direct Replacement	Recommended for New Designs	Sec.
US5400A	SN5400J, N	SN5400J, N	6
US5400J	SN5400W	SN5400W	6
US5401A	US5401J, N	SN5401J, N	6
US5401J	US5401W	SN5401W	6
US5402A	SN5402J, N	SN5402J, N	6
US5402J	SN5402W	SN5402W	6
US5403A	SN5403J, N	SN5403J, N	6
US5404A	SN5404J, N	SN5404J, N	6
US5404J	SN5404W	SN5404W	6
US5405A	SN5405J, N	SN5405J, N	6
US5405J	SN5405W	SN5405W	6
US5408A	SN5408J, N	SN5408J, N	6
US5408J		SN5408W	6
US5409A	SN5409J, N	SN5409J, N	6
US5409J		SN5409W	6
US5410A	SN5410J, N	SN5410J, N	6
US5410J	SN5410W	SN5410W	6
US5420A	SN5420J, N	SN5420J, N	6
US5420J	SN5420W	SN5420W	6
US5426A	SN5426J, N	SN5426J, N	6
US5427A	SN5427J, N	SN5427J, N	6
US5427J		SN5427W	6
US5429A	SN5425J, N	SN5425J, N	6
US5429J		SN5425W	6
US5430A	SN5430J, N	SN5430J, N	6
US5430J	SN5430W	SN5430W	6
US5432A	SN5432J, N	SN5432J, N	6
US5432J		SN5432W	6
US5438A	SN5438J, N	SN5438J, N	6
US5438J		SN5438W	6
US5439A		SN5438J, N	6
US5439J		SN5438W	6
US5440A	SN5440J, N	SN5440J, N	6
US5440J	SN5440W	SN5440W	6
US5442A	SN5442J, N	SN5442J, N	9
US5442J	SN5442W	SN5442W	9
US5443A	SN5443J, N	SN5443J, N	9
US5443J	SN5443W	SN5443W	9
US5444A	SN5444J, N	SN5444J, N	9
US5444J	SN5444W	SN5444W	9
US5445A	SN5445J, N	SN5445J, N	9
US5445J	SN5445W	SN5445W	9
US5446A	SN5446AJ, N	SN5446AJ, N	9
US5446J	SN5446AW	SN5446AW	9
US5447A	SN5447AJ, N	SN5447AJ, N	9
US5447J	SN5447AW	SN5447AW	9
US5448A	SN5448J, N	SN5448J, N	9
US5448J	SN5448W	SN5448W	9
US5450A	SN5450J, N	SN5450J, N	6
US5450J	SN5450W	SN5450W	6
US5451A	SN5451J, N	SN5451J, N	6
US5451J	SN5451W	SN5451W	6
US5453A	SN5453J, N	SN5453J, N	6
US5453J	SN5453W	SN5453W	6
US5454A	SN5454J, N	SN5454J, N	6
US5454J	SN5454W	SN5454W	6
US5459A		SN5451J, N	6
US5459J		SN5451W	6
US5460A	SN5460J, N	SN5460J, N	6
US5460J	SN5460W	SN5460W	6
US5470A	SN5470J, N	SN5470J, N	6
US5470J	SN5470W	SN5470W	6
US5472A	SN5472J, N	SN5472J, N	6
US5472J	SN5472W	SN5472W	6
US5473A	SN5473J, N	SN5473J, N	6
US5473J	SN5473W	SN5473W	6
US5474A	SN5474J, N	SN5474J, N	6
US5474J	SN5474W	SN5474W	6

Type Number	Direct Replacement	Recommended for New Designs	Sec.
US5475A	SN5475J, N	SN5475J, N	9
US5476A	SN5476J, N	SN5476J, N	6
US5477J	SN5477W	SN5477W	9
US5480A	SN5480J, N	SN5480J, N	9
US5480J	SN5480W	SN5480W	9
US5481A	SN5481J, N	SN5481J, N	9
US5481J	SN5481W	SN5481W	9
US5482A	SN5482J, N	SN5482J, N	9
US5482J	SN5482W	SN5482W	9
US5483A	SN5483J, N	SN5483J, N	9
US5484A	SN5484J, N	SN5484J, N	9
US5484J	SN5484W	SN5484W	9
US5486A	SN5486J, N	SN5486J, N	9
US5486J	SN5486W	SN5486W	9
US5490A	SN5490J, N	SN5490J, N	9
US5490J	SN5490W	SN5490W	9
US5491A	SN5491AJ, N	SN5491AJ, N	9
US5491J	SN5491AW	SN5491AW	9
US5492A	SN5492J, N	SN5492J, N	9
US5492J	SN5492W	SN5492W	9
US5493A	SN5493J, N	SN5493J, N	9
US5493J	SN5493W	SN5493W	9
US5494A	SN5494J, N	SN5494J, N	9
US5494J	SN5494W	SN5494W	9
US5495A	SN5495AJ, N	SN5495AJ, N	9
US5495J	SN5495AW	SN5495AW	9
US5496A	SN5496J, N	SN5496J, N	9
US5496J	SN5496W	SN5496W	9
US54107A	SN54107J, N	SN54107J, N	6
US54121A	SN54121J, N	SN54121J, N	6
US54121J	SN54121W	SN54121W	6
US54122A	SN54122J, N	SN54122J, N	6
US54122J	SN54122W	SN54122W	6
US54123A	SN54123J, N	SN54123J, N	6
US54123J	SN54123W	SN54123W	6
US54145A	SN54145J, N	SN54145J, N	9
US54145J	SN54145W	SN54145W	9
US54150A	SN54150J, N	SN54150J, N	9
US54150J	SN54150W	SN54150W	9
US54151A	SN54151J, N	SN54151J, N	9
US54151J	SN54151W	SN54151W	9
US54153A	SN54153J, N	SN54153J, N	9
US54153J	SN54153W	SN54153W	9
US54154A	SN54154J, N	SN54154J, N	9
US54154J	SN54154W	SN54154W	9
US54164A	SN54164J, N	SN54164J, N	9
US54164J	SN54164W	SN54164W	9
US54165A	SN54165J, N	SN54165J, N	9
US54165J	SN54165W	SN54165W	9
US54180A	SN54180J, N	SN54180J, N	9
US54180J	SN54180W	SN54180W	9
US54181A	SN54181J, N	SN54181J, N	9
US54181J	SN54181W	SN54181W	9
US54182A	SN54182J, N	SN54182J, N	9
US54182J	SN54182W	SN54182W	9
US54192A	SN54192J, N	SN54192J, N	9
US54192J	SN54192W	SN54192W	9
US54193A	SN54193J, N	SN54193J, N	9
US54193J	SN54193W	SN54193W	9
US7400A	SN7400J, N	SN7400J, N	6
US7400J	SN7400W	SN7400W	6
US7401A	SN7401J, N	SN7401J, N	6
US7401J	SN7401W	SN7401W	6
US7402A	SN7402J, N	SN7402J, N	6
US7402J	SN7402W	SN7402W	6
US7403A	SN7403J, N	SN7403J, N	6
US7404A	SN7404J, N	SN7404J, N	6
US7404J	SN7404W	SN7404W	6

CROSS-REFERENCE GUIDE

DTL/TTL CIRCUITS

Sprague TTL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
US7405A	SN7405J, N	SN7405J, N	6
US7405J	SN7405W	SN7405W	6
US7408A	SN7408J, N	SN7408J, N	6
US7408J		SN7408W	6
US7409A	SN7409J, N	SN7409J, N	6
US7409J		SN7409W	6
US7410A	SN7410J, N	SN7410J, N	6
US7410J	SN7410W	SN7410W	6
US7420A	SN7420J, N	SN7420J, N	6
US7420J	SN7420W	SN7420W	6
US7426J	SN7426J, N	SN7426J, N	6
US7427A	SN7427J, N	SN7427J, N	6
US7427J		SN7427W	6
US7429A	SN7425J, N	SN425J, N	6
US7429J		SN425W	6
US7430A	SN7430J, N	SN7430J, N	6
US7430J	SN7430W	SN7430W	6
US7432A	SN7432J, N	SN7432J, N	6
US7432J		SN7432W	6
US7438A	SN7438J, N	SN7438J, N	6
US7438J		SN7438W	6
US7439A		SN7438J, N	6
US7439J		SN7438W	6
US7440A	SN7440J, N	SN7440J, N	6
US7440J	SN7440W	SN7440W	6
US7441A	SN74141J, N	SN74141J, N	9
US7442A	SN7442J, N	SN7442J, N	9
US7442J	SN7442W	SN7442W	9
US7443A	SN7443J, N	SN7443J, N	9
US7443J	SN7443W	SN7443W	9
US7444A	SN7444J, N	SN7444J, N	9
US7444J	SN7444W	SN7444W	9
US7445A	SN7445J, N	SN7445J, N	9
US7445J	SN7445W	SN7445W	9
US7446A	SN7446AJ, N	SN7446AJ, N	9
US7446J	SN7446AW	SN7446AW	9
US7447A	SN7447AJ, N	SN7447AJ, N	9
US7447J	SN7447AW	SN7447AW	9
US7448A	SN7448J, N	SN7448J, N	9
US7448J	SN7448W	SN7448W	9
US7450A	SN7450J, N	SN7450J, N	6
US7450J	SN7450W	SN7450W	6
US7451A	SN7451J, N	SN7451J, N	6
US7451J	SN7451W	SN7451W	6
US7453A	SN7453J, N	SN7453J, N	6
US7453J	SN7453W	SN7453W	6
US7454A	SN7454J, N	SN7454J, N	6
US7454J	SN7454W	SN7454W	6
US7459A		SN7451J, N	6
US7459J		SN7451W	6
US7460A	SN7460J, N	SN7460J, N	6
US7460J	SN7460W	SN7460W	6
US7470A	SN7470J, N	SN7470J, N	6
US7470J	SN7470W	SN7470W	6
US7472A	SN7472J, N	SN7472J, N	6
US7472J	SN7472W	SN7472W	6
US7473A	SN7473J, N	SN7473J, N	6
US7473J	SN7473W	SN7473W	6
US7474A	SN7474J, N	SN7474J, N	6
US7474J	SN7474W	SN7474W	6
US7475A	SN7475J, N	SN7475J, N	9
US7476A	SN7476J, N	SN7476J, N	6
US7477J	SN7477W	SN7477W	9
US7480A	SN7480J, N	SN7480J, N	9
US7480J	SN7480W	SN7480	9
US7481A	SN7481J, N	SN7481J, N	9
US7481J	SN7481W	SN7481W	9
US7482A	SN7482J, N	SN7482J, N	9
US7482J	SN7482W	SN7482W	9
US7483A	SN7483J, N	SN7483J, N	9
US7484A	SN7484J, N	SN7484J, N	9
US7484J	SN7484W	SN7484W	9
US7486A	SN7486J, N	SN7486J, N	9
US7486J	SN7486W	SN7486W	9
US7490A	SN7490J, N	SN7490J, N	9
US7490J	SN7490W	SN7490W	9
US7491A	SN7491AJ, N	SN7491AJ, N	9
US7491J	SN7491AW	SN7491AW	9
US7492A	SN7492J, N	SN7492J, N	9
US7492J	SN7492W	SN7492W	9
US7493A	SN7493J, N	SN7493J, N	9
US7493J	SN7493W	SN7493W	9
US7494A	SN7494J, N	SN7494J, N	9
US7494J	SN7494W	SN7494W	9
US7495A	SN7495AJ, N	SN7495AJ, N	9
US7495J	SN7495AW	SN7495AW	9
US7496A	SN7496J, N	SN7596J, N	9
US7496J	SN7496W	SN7496W	9
US74107A	SN74107J, N	SN74107J, N	6
US74121A	SN74121J, N	SN74121J, N	6
US74121J	SN74121W	SN74121W	6
US74122A	SN74122J, N	SN74122J, N	6
US75122J	SN74122W	SN74122W	6
US74123A	SN74123J, N	SN74123J, N	6
US74123J	SN74123W	SN74123W	6
US74145A	SN74145J, N	SN74145J, N	9
US74150A	SN74150J, N	SN74150J, N	9
US74150J	SN74150W	SN74150W	9
US74151A	SN74151J, N	SN74151J, N	9
US74151J	SN74151W	SN74151W	9
US74153A	SN74153J, N	SN74153J, N	9
US74153J	SN74153W	SN74153W	9
US74154A	SN74154J, N	SN74154J, N	9
US74154J	SN74154W	SN74154W	9
US74164A	SN74164J, N	SN74164J, N	9
US74164J	SN74164W	SN74164W	9
US74165A	SN74165J, N	SN74165J, N	9
US74165J	SN74165W	SN74165W	9
US74180A	SN74180J, N	SN74180J, N	9
US74180J	SN74180W	SN74180W	9
US74181A	SN74181J, N	SN74181J, N	9
US74181J	SN74181W	SN74181W	9
US74182A	SN74182J, N	SN74182J, N	9
US74182J	SN74182W	SN74182W	9
US74192A	SN74192J, N	SN74192J, N	9
US74192J	SN74192W	SN74192W	9
US74193A	SN74193J, N	SN74193J, N	9
US74193J	SN74193W	SN74193W	9
US54H00A	SN54H00J, N	SN54H00J, N	7
US54H00J	SN54H00W	SN54H00W	7
US54H01A	SN54H01J, N	SN54H01J, N	7
US54H01J	SN54H01W	SN54H01W	7
US54H04A	SN54H04J, N	SN54H04J, N	7
US54H04J	SN54H04W	SN54H04W	7
US54H05A	SN54H05J, N	SN54H05J, N	7
US54H05J	SN54H05W	SN54H05W	7
US54H10A	SN54H10J, N	SN54H10J, N	7
US54H10J	SN54H10W	SN54H10W	7
US54H11A	SN54H11J, N	SN54H11J, N	7
US54H11J	SN54H11W	SN54H11W	7
US54H20A	SN54H20J, N	SN54H20J, N	7
US54H20J	SN54H20W	SN54H20W	7
US54H21A	SN54H21J, N	SN54H21J, N	7
US54H21J	SN54H21W	SN54H21W	7
US54H22A	SN54H22J, N	SN54H22J, N	7
US54H22J	SN54H22W	SN54H22W	7

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DTL/TTL CIRCUITS

Sprague TTL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
US54H30A	SN54H30J, N	SN54H30J, N	7
US54H30J	SN54H30W	SN54H30W	7
US54H40A	SN54H40J, N	SN54H40J, N	7
US54H40J	SN54H40W	SN54H40W	7
US54H50A	SN54H50J, N	SN54H50J, N	7
US54H50J	SN54H50W	SN54H50W	7
US54H51A	SN54H51J, N	SN54H51J, N	7
US54H51J	SN54H51W	SN54H51W	7
US54H52A	SN54H52J, N	SN54H52J, N	7
US54H52J	SN54H52W	SN54H52W	7
US54H53A	SN54H53J, N	SN54H52J, N	7
US54H53J	SN54H53W	SN54H53W	7
US54H54A	SN54H54J, N	SN54H54J, N	7
US54H54J	SN54H54W	SN54H54W	7
US54H55A	SN54H55J, N	SN54H55J, N	7
US54H55J	SN54H55W	SN54H55W	7
US54H60A	SN54H60J, N	SN54H60J, N	7
US54H60J	SN54H60W	SN54H60W	7
US54H61A	SN54H61J, N	SN54H61J, N	7
US54H61J	SN54H61W	SN54H61W	7
US54H62A	SN54H62J, N	SN54H62J, N	7
US54H62J	SN54H62W	SN54H62W	7
US54H71A	SN54H71J, N	SN54H71J, N	7
US54H71J	SN54H71W	SN54H71W	7
US54H72A	SN54H72J, N	SN54H72J, N	7
US54H72J	SN54H72W	SN54H72W	7
US54H73A	SN54H73J, N	SN54H73J, N	7
US54H73J	SN54H73W	SN54H73W	7
US54H76A	SN54H76J, N	SN54H76J, N	7
US54H76J	SN54H76W	SN54H76W	7
US54H78A	SN54H78J, N	SN54H78J, N	7
US54H78J	SN54H78W	SN54H78W	7
US74H00A	SN74H00J, N	SN74H00J, N	7
US74H00J	SN74H00W	SN74H00W	7
US74H01A	SN74H01J, N	SN74H01J, N	7
US74H01J	SN74H01W	SN74H01W	7
US74H04A	SN74H04J, N	SN74H04J, N	7
US74H04J	SN74H04W	SN74H04W	7
US74H05A	SN74H05J, N	SN74H05J, N	7
US74H05J	SN74H05W	SN74H05W	7
US74H10A	SN74H10J, N	SN74H10J, N	7

Type Number	Direct Replacement	Recommended for New Designs	Sec.
US74H10J	SN74H10W	SN74H10W	7
US74H11A	SN74H11J, N	SN74H11J, N	7
US74H11J	SN74H11W	SN74H11W	7
US74H20A	SN74H20J, N	SN74H20J, N	7
US74H20J	SN74H20W	SN74H20W	7
US74H21A	SN74H21J, N	SN74H21J, N	7
US74H21J	SN74H21W	SN74H21W	7
US74H22A	SN74H22J, N	SN74H22J, N	7
US74H22J	SN74H22W	SN74H22W	7
US74H30A	SN74H30J, N	SN74H30J, N	7
US74H30J	SN74H30W	SN74H30W	7
US74H40A	SN74H40J, N	SN74H40J, N	7
US74H40J	SN74H40W	SN74H40W	7
US74H50A	SN74H50J, N	SN74H50J, N	7
US74H50J	SN74H50W	SN74H50W	7
US74H51A	SN74H51J, N	SN74H51J, N	7
US74H51J	SN74H51W	SN74H51W	7
US74H52A	SN74H52J, N	SN74H52J, N	7
US74H52J	SN74H52W	SN74H52W	7
US74H53A	SN74H53J, N	SN74H53J, N	7
US74H53J	SN74H53W	SN74H53W	7
US74H54A	SN74H54J, N	SN74H54J, N	7
US74H54J	SN74H54W	SN74H54W	7
US74H55A	SN74H55J, N	SN74H55J, N	7
US74H55J	SN74H55W	SN74H55W	7
US74H60A	SN75H60J, N	SN74H60J, N	7
US74H60J	SN74H60W	SN74H60W	7
US74H61A	SN74H61J, N	SN74H61J, N	7
US74H61J	SN74H61W	SN74H61W	7
US74H62A	SN74H62J, N	SN74H62J, N	7
US74H62J	SN74H62W	SN74H62W	7
US74H71A	SN74H71J, N	SN74H71J, N	7
US74H71J	SN74H71W	SN74H71W	7
US74H72A	SN74H72J, N	SN74H72J, N	7
US74H72J	SN74H72W	SN74H72W	7
US74H73A	SN74H73J, N	SN74H73J, N	7
US74H73J	SN74H73W	SN74H73W	7
US74H76A	SN74H76J, N	SN74H76J, N	7
US75H76J	SN74H76W	SN74H76W	7
US74H78A	SN74H78J, N	US74H78J, N	7
US74H78J	SN74H78W	US74H78W	7

Transitron TTL

Type Number	Direct Replacement	Recommended for New Designs	Sec.
SN5400F	SN5400W	SN5400W	6
SN5400J, N	SN5400J, N	SN5400J, N	6
SN5401F	SN5401W	SN5401W	6
SN5401J, N	SN5401J, N	SN5401J, N	6
SN5402F	SN5402W	SN5402W	6
SN5402J, N	SN5402J, N	SN5402J, N	6
SN5404F	SN5404W	SN5404W	6
SN5404J, N	SN5404J, N	SN5404J, N	6
SN5405F	SN5405W	SN5405W	6
SN5405J, N	SN5405J, N	SN5405J, N	6
SN5410F	SN5410W	SN5410W	6
SN5410J, N	SN5410J, N	SN5410J, N	6
SN5420F	SN5420W	SN5420W	6
SN5420J, N	SN5420J, N	SN5420J, N	6
SN5430F	SN5430W	SN5430W	6
SN5430J, N	SN5430J, N	SN5430J, N	6
SN5440F	SN5440W	SN5440W	6

Type Number	Direct Replacement	Recommended for New Designs	Sec.
SN5440J, N	SN5440J, N	SN5440J, N	6
SN5441AJ, N	SN54141J, N	SN54141J, N	9
SN5442J, N	SN5442J, N	SN5442J, N	9
SN5443J, N	SN5443J, N	SN5443J, N	9
SN5444J, N	SN5444J, N	SN5444J, N	9
SN5450F	SN5450W	SN5450W	6
SN5450J, N	SN5450J, N	SN5450J, N	6
SN5451F	SN5451W	SN5451J, N	6
SN5451J, N	SN5451J, N	SN5451J, N	6
SN5453F	SN5453W	SN5453W	6
SN5453J, N	SN5453J, N	SN5453J, N	6
SN5454F	SN5454W	SN5454W	6
SN5454J, N	SN5454J, N	SN5454J, N	6
SN5460F	SN5460W	SN5460W	6
SN5460J, N	SN5460J, N	SN5460J, N	6
SN5470F	SN5470W	SN5470W	6
SN5470J, N	SN5470J, N	SN5470J, N	6

CROSS-REFERENCE GUIDE

DTL/TTL CIRCUITS

Transitron TTL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
SN5472F	SN5472W	SN5472W	6
SN5472J, N	SN5472J, N	SN5472J, N	6
SN5473F	SN5473W	SN5473W	6
SN5473J, N	SN5473J, N	SN5473J, N	6
SN5474F	SN5474W	SN5474W	6
SN5474J, N	SN5474J, N	SN5474J, N	6
SN5475J, N	SN5475J, N	SN5475J, N	9
SN5476J, N	SN5476J, N	SN5476J, N	6
SN5480F	SN5480W	SN5480W	9
SN5480J, N	SN5480J, N	SN5480J, N	9
SN5482F	SN5482W	SN5482W	9
SN5482J, N	SN5482J, N	SN5482J, N	9
SN5483J, N	SN5483J, N	SN5483J, N	9
SN5490F	SN5490W	SN5490W	9
SN5490J, N	SN5490J, N	SN5490J, N	9
SN5491AF	SN5491AW	SN5491AW	9
SN5491AJ, N	SN5491AJ, N	SN5491AJ, N	9
SN5492F	SN5492W	SN5492W	9
SN5492J, N	SN5492J, N	SN5492J, N	9
SN5493F	SN5493W	SN5493W	9
SN5493J, N	SN5493J, N	SN5493J, N	9
SN5494J, N	SN5494J, N	SN5494J, N	9
SN5495F	SN5495AW	SN5495AW	9
SN5495J, N	SN5495AJ, N	SN5495AJ, N	9
SN5496J, N	SN5496J, N	SN5496J, N	9
SN54107J, N	SN54107J, N	SN54107J, N	6
SN54121F	SN54121W	SN54121W	6
SN54121J, N	SN54121J, N	SN54121J, N	6
SN542511F		SN54197W	9
SN542511J, N		SN54197J, N	9
SN542515F		SN54196W	9
SN542515J, N		SN54196J, N	9
SN542525F		SN54194W	9
SN542525J, N		SN54194J, N	9
SN543163F	SN5481W	SN5489W	9
SN543163J, N	SN5481J, N	SN5489J, N	9
SN545511F		SN5437W	6
SN545511J, N		SN5437J, N	6
SN545611F		SN5438W	6
SN545611J, N		SN5438J, N	6
SN548280F		SN54196W	9
SN548280J, N		SN54196J, N	9
SN548281F		SN54197W	9
SN548281J, N		SN54197J, N	9
SN7400F	SN7400W	SN7400W	6
SN7400J, N	SN7400J, N	SN7400J, N	6
SN7401F	SN7401W	SN7401W	6
SN7401J, N	SN7401J, N	SN7401J, N	6
SN7402F	SN7402W	SN7402W	6
SN7402J, N	SN7402J, N	SN7402J, N	6
SN7404F	SN7404W	SN7404W	6
SN7404J, N	SN7404J, N	SN7404J, N	6
SN7405F	SN7405W	SN7405W	6
SN7405J, N	SN7405J, N	SN7405J, N	6
SN7410F	SN7410W	SN7410W	6
SN7410J, N	SN7410J, N	SN7410J, N	6
SN7420F	SN7420W	SN7420W	6
SN7420J, N	SN7420J, N	SN7420J, N	6
SN7430F	SN7430W	SN7430W	6
SN7430J, N	SN7430J, N	SN7430J, N	6
SN7440F	SN7440W	SN7440W	6
SN7440J, N	SN7440J, N	SN7440J, N	6
SN7441AJ, N	SN74141J, N	SN74141J, N	9
SN7442J, N	SN7442J, N	SN7442J, N	9
SN7443J, N	SN7443J, N	SN7443J, N	9
SN7444J, N	SN7444J, N	SN7444J, N	9
SN7450F	SN7450W	SN7450W	6

Type Number	Direct Replacement	Recommended for New Designs	Sec.
SN7450J, N	SN7450J, N	SN7450J, N	6
SN7451F	SN7451W	SN7451W	6
SN7451J, N	SN7451J, N	SN7451J, N	6
SN7453F	SN7453W	SN7453W	6
SN7453J, N	SN7453J, N	SN7453J, N	6
SN7454F	SN7454W	SN7454W	6
SN7454J, N	SN7454J, N	SN7454J, N	6
SN7460F	SN7460W	SN7460W	6
SN7460J, N	SN7460J, N	SN7460J, N	6
SN7470F	SN7470W	SN7470W	6
SN7470J, N	SN7470J, N	SN7470J, N	6
SN7472F	SN7472W	SN7472W	6
SN7472J, N	SN7472J, N	SN7472J, N	6
SN7473F	SN7473W	SN7473W	6
SN7473J, N	SN7473J, N	SN7473J, N	6
SN7474F	SN7474W	SN7474W	6
SN7474J, N	SN7474J, N	SN7474J, N	6
SN7475J, N	SN7475J, N	SN7475J, N	9
SN7476J, N	SN7476J, N	SN7476J, N	6
SN7480F	SN7480W	SN7480W	9
SN7480J, N	SN7480J, N	SN7480J, N	9
SN7482F	SN7482W	SN7482W	9
SN7482J, N	SN7482J, N	SN7482J, N	9
SN7483J, N	SN7483J, N	SN7483J, N	9
SN7490F	SN7490W	SN7490W	9
SN7490J, N	SN7490J, N	SN7490J, N	9
SN7491AF	SN7491AW	SN7491AW	9
SN7491AJ, N	SN7491AJ, N	SN7491AJ, N	9
SN7492F	SN7492W	SN7492W	9
SN7492J, N	SN7492J, N	SN7492J, N	9
SN7493F	SN7493W	SN7493W	9
SN7493J, N	SN7493J, N	SN7493J, N	9
SN7494J, N	SN7494J, N	SN7494J, N	9
SN7495F	SN7495AW	SN7495AW	9
SN7495J, N	SN7495AJ, N	SN7495AJ, N	9
SN7496J, N	SN7496J, N	SN7496J, N	9
SN74107J, N	SN74107J, N	SN74107J, N	6
SN74121F	SN74121W	SN74121W	6
SN74121J, N	SN74121J, N	SN74121J, N	6
SN742512F		SN74197W	9
SN74212J, N		SN74197J, N	9
SN742516F		SN74196W	9
SN742516J, N		SN74196J, N	9
SN742526F		SN74194W	9
SN742526J, N		SN74194J, N	9
SN743162F	SN7481W	SN7489W	9
SN743162J, N	SN7481J, N	SN7489J, N	9
SN743164F	SN7481W	SN7489W	9
SN743164J, N	SN7481J, N	SN7489J, N	9
SN745512F		SN7437W	6
SN745512J, N		SN7437J, N	6
SN745612F		SN7438W	6
SN745612J, N		SN7438J, N	6
SN748280F		SN74196W	9
SN748280J, N		SN74196J, N	9
SN748281F		SN74197W	9
SN748281J, N		SN74197J, N	9
TA10E, J		SN54H183J, N	9
TA10F		SN54H183W	9
TA11E, J		SN54H183J, N	9
TA11F		SN54H183W	9
TA12E, J		SN74H183J, N	9
TA12F		SN74H183W	9
TA13E, J		SN74H183J, N	9
TA13F		SN74H183W	9
TA20E, J	SNE20J, N	SN54181J, N	9
TA20F	SNE20U	SN54181W	9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DTL/TTL CIRCUITS

Transitron TTL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
TA21E, J	SNE21J, N	SN54181J, N	9
TA21F	SNE21U	SN54181W	9
TA22E, J	SNE22J, N	SN74181J, N	9
TA22F	SNE22U	SN74181W	9
TA23E, J	SNE23J, N	SN74181J, N	9
TA23F	SNE23U	SN74181W	9
TA30E, J	SNE30J, N	SN54181J, N	9
TA30F	SNE30U	SN54181W	9
TA31E, J	SNE31J, N	SN54181J, N	9
TA31F	SNE31U	SN54181W	9
TA32E, J	SNE32J, N	SN74181J, N	9
TA32F	SNE32U	SN74181W	9
TA33E, J	SNE33J, N	SN74181J, N	9
TA33F	SNE33U	SN74181W	9
TC11E, J		SN54163J, N	9
TC11F		SN54163W	9
TC12E, J		SN74163J, N	9
TC12F		SN74163W	9
TC13E, J		SN54163J, N	9
TC13F		SN54163W	9
TC14E, J		SN74163J, N	9
TC14F		SN74163W	9
TC15E, J		SN54162J, N	9
TC15F		SN54162W	9
TC16E, J		SN74162J, N	9
TC16F		SN74162W	9
TC17E, J		SN54162J, N	9
TC17F		SN54162W	9
TC18E, J		SN74162J, N	9
TC18F		SN74162W	9
TD40E, J	SNE40J, N	SN54182J, N	9
TD40F	SNE40U	SN54182W	9
TD42E, J	SNE42J, N	SN74182J, N	9
TD42F	SNE42U	SN74182W	9
TF20E, J	SNF20J, N	SN5472J, N	6
TF20F	SNF20U	SN5472W	6
TF21E, J	SNF21J, N	SN5472J, N	6
TF21F	SNF21U	SN5472W	6
TF22E, J	SNF22J, N	SN7472J, N	6
TF22F	SNF22U	SN7472W	6
TF23E, J	SNF23J, N	SN7472J, N	6
TF23F	SNF23U	SN7472W	6
TF50E, J	SNF50J, N	SN5470J, N	6
TF50F	SNF50U	SN5470W	6
TF51E, J	SNF51J, N	SN5470J, N	6
TF51F	SNF51U	SN5470W	6
TF52E, J	SNF52J, N	SN7470J, N	6
TF52F	SNF52U	SN7470W	6
TF53E, J	SNF53J, N	SN7470J, N	6
TF53F	SNF53U	SN7470W	6
TF60E, J	SNF60J, N	SN54H101J, N	7
TF60F	SNF60U	SN54H101W	7
TF61E, J	SNF61J, N	SN54H101J, N	7
TF61F	SNF61U	SN54H101W	7
TF62E, J	SNF62J, N	SN74H101J, N	7
TF62F	SNF62U	SN74H101W	7
TF63E, J	SNF63J, N	SN74H101J, N	7
TF63F	SNF63U	SN74H101W	7
TF100E, J	SNF100J, N	SN54H103J, N	7
TF100F	SNF100U	SN54H103W	7
TF101E, J	SNF101J, N	SN54H103J, N	7
TF101F	SNF101U	SN54H103W	7
TF102E, J	SNF102J, N	SN74H103J, N	7
TF102F	SNF102U	SN74H103W	7
TF103E, J	SNF103J, N	SN74H103J, N	7
TF103F	SNF103U	SN74H103W	7

Type Number	Direct Replacement	Recommended for New Designs	Sec.
TF110E, J	SNF110J, N	SN54H108J, N	7
TF110F	SNF110U	SN54H108W	7
TF111E, J	SNF111J, N	SN54H108J, N	7
TF111F	SNF111U	SN54H108W	7
TF112E, J	SNF112J, N	SN74H108J, N	7
TF112F	SNF112U	SN74H108W	7
TF113E, J	SNF113J, N	SN74H108J, N	7
TF113F	SNF113U	SN74H108W	7
TF120E, J	SNF120J, N	SN54H103J, N	7
TF120F	SNF120U	SN54H103W	7
TF121E, J	SNF121J, N	SN54H103J, N	7
TF121F	SNF121U	SN54H103W	7
TF122E, J	SNF122J, N	SN74H103J, N	7
TF122F	SNF122U	SN74H103W	7
TF123E, J	SNF123J, N	SN74H103J, N	7
TF123F	SNF123U	SN74H103W	7
TF130E, J	SNF130J, N	SN54H108J, N	7
TF130F	SNF130U	SN54H108W	7
TF131E, J	SNF131J, N	SN54H108J, N	7
TF131F	SNF131U	SN54H108W	7
TF132E, J	SNF132J, N	SN74H108J, N	7
TF132F	SNF132U	SN74H108W	7
TF133E, J	SNF133J, N	SN74H108J, N	7
TF133F	SNF133U	SN74H108W	7
TF200E, J	SNF200J, N	SN54H102J, N	7
TF200F	SNF200U	SN54H102W	7
TF201E, J	SNF201J, N	SN54H102J, N	7
TF201F	SNF201U	SN54H102W	7
TF202E, J	SNF202J, N	SN74H102J, N	7
TF202F	SNF202U	SN74H102W	7
TF203E, J	SNF203J, N	SN74H102J, N	7
TF203F	SNF203U	SN74H102W	7
TF210E, J	SNF210J, N	SN54H101J, N	7
TF210F	SNF210U	SN54H101W	7
TF211E, J	SNF211J, N	SN54H101J, N	7
TF211F	SNF211U	SN54H101W	7
TF212E, J	SNF212J, N	SN74H101J, N	7
TF212F	SNF212U	SN74H101W	7
TF213E, J	SNF213J, N	SN74H101J, N	7
TF213F	SNF213U	SN74H101W	7
TF250E, J	SNF250J, N	SN54H102J, N	7
TF250F	SNF250U	SN54H102W	7
TF251E, J	SNF251J, N	SN54H102J, N	7
TF251F	SNF251U	SN54H102W	7
TF252E, J	SNF252J, N	SN74H102J, N	7
TF252F	SNF252U	SN74H102W	7
TF253E, J	SNF253J, N	SN74H102J, N	7
TF253F	SNF253U	SN74H102W	7
TF260E, J	SNF260J, N	SN54H101J, N	7
TF260F	SNF260U	SN54H101W	7
TF261E, J	SNF261J, N	SN54H101J, N	7
TF261F	SNF261U	SN54H101W	7
TF262E, J	SNF262J, N	SN74H101J, N	7
TF262F	SNF262U	SN74H101W	7
TF263E, J	SNF263J, N	SN74101J, N	7
TF263F	SNF263U	SN74H101W	7
TG40E, J	SNG40J, N	SN5420J, N	6
TG40F	SNG40U	SN5420W	6
TG41E, J	SNG41J, N	SN5420J, N	6
TG41F	SNG41U	SN5420W	6
TG42E, J	SNG42J, N	SN7420J, N	6
TG42F	SNG42U	SN7420W	6
TG43E, J	SNG43J, N	SN7420J, N	6
TG43F	SNG43U	SN7420W	6
TG50E, J	SN50J, N	SN5453J, N	6
TG50F	SNG50U	SN5453W	6

Transitron TTL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
TG51E, J	SNG51J, N	SN5453J, N	6
TG51F	SNG51U	SN5453W	6
TG52E, J	SNG52J, N	SN7453J, N	6
TG52F	SNG52U	SN7453W	6
TG53E, J	SNG53J, N	SN7453J, N	6
TG53F	SNG53U	SN7453W	6
TG60E, J	SNG60J, N	SN5430J, N	6
TG60F	SNG60U	SN5430W	6
TG61E, J	SNG61J, N	SN5430J, N	6
TG61F	SNG61U	SN5430W	6
TG62E, J	SNG62J, N	SN7430J, N	6
TG62F	SNG62U	SN7430W	6
TG63E, J	SNG63J, N	SN7430J, N	6
TG63F	SNG63U	SN7430W	6
TG70E, J	SNG70J, N	SN5450J, N	6
TG70F	SNG70U	SN5450W	6
TG71E, J	SNG71J, N	SN5450J, N	6
TG71F	SNG71U	SN5450W	6
TG72E, J	SNG72J, N	SN7450J, N	6
TG72F	SNG72U	SN7450W	6
TG73E, J	SNG73J, N	SN7450J, N	6
TG73F	SNG73U	SN7450W	6
TG80E, J	SNG80J, N	SN5413J, N	6
TG80F	SNG80U	SN5413W	6
TG81E, J	SNG81J, N	SN5413J, N	6
TG81F	SNG81U	SN5413W	6
TG82E, J	SNG82J, N	SN7413J, N	6
TG82F	SNG82U	SN7413W	6
TG83E, J	SNG83J, N	SN7413J, N	6
TG83F	SNG83U	SN7413W	6
TG90E, J	SNG90J, N	SN5486J, N	9
TG90F	SNG90U	SN5486W	9
TG91E, J	SNG91J, N	SN5486J, N	9
TG91F	SNG91U	SN5486W	9
TG92E, J	SNG92J, N	SN7486J, N	9
TG92F	SNG92U	SN7486W	9
TG93E, J	SNG93J, N	SN7486J, N	9
TG93F	SNG93U	SN7486W	9
TG100E, J	SNG100J, N	SN5453J, N	6
TG100F	SNG100U	SN5453W	6
TG101E, J	SNG101J, N	SN5453J, N	6
TG101F	SNG101U	SN5453W	6
TG102E, J	SNG102J, N	SN7453J, N	6
TG102F	SNG102U	SN7453W	6
TG103E, J	SNG103J, N	SN7453J, N	6
TG103F	SNG103U	SN7453W	6
TG110E, J	SNG110J, N	SN54H55J, N	7
TG110F	SNG110U	SN54H55W	7
TG111E, J	SNG111J, N	SN54H55J, N	7
TG111F	SNG111U	SN54H55W	7
TG112E, J	SNG112J, N	SN74H55J, N	7
TG112F	SNG112U	SN74H55W	7
TG113E, J	SNG113J, N	SN74H55J, N	7
TG113F	SNG113U	SN74H55W	7
TG120E, J	SNG120J, N	SN5430J, N	6
TG120F	SNG120U	SN5430W	6
TG121E, J	SNG121J, N	SN5430J, N	6
TG121F	SNG121U	SN5430W	6
TG122E, J	SNG122J, N	SN7430J, N	6
TG122F	SNG122U	SN7430W	6
TG123E, J	SNG123J, N	SN7430J, N	6
TG123F	SNG123U	SN7430W	6
TG130E, J	SNG130J, N	SN54S140J, N	5
TG130F	SNG130U	SN54S140W	5
TG131E, J	SNG131J, N	SN54S140J, N	5
TG131F	SNG131U	SN54S140W	5
TG132E, J	SNG132J, N	SN74S140J, N	5
TG132F	SNG132U	SN74S140W	5

Type Number	Direct Replacement	Recommended for New Designs	Sec.
TG133E, J	SNG133J, N	SN74S140J, N	5
TG133F	SNG133U	SN74S140W	5
TG140E, J	SNG140J, N	SN5400J, N	6
TG140F	SNG140U	SN5400W	6
TG141E, J	SNG141J, N	SN5400J, N	6
TG141F	SNG141U	SN5400W	6
TG142E, J	SNG142J, N	SN7400J, N	6
TG142F	SNG142U	SN7400W	6
TG143E, J	SNG143J, N	SN7400J, N	6
TG143F	SNG143U	SN7400W	6
TG150E, J	SNG150J, N	SN54H62J, N	7
TG150F	SNG150U	SN54H62W	7
TG151E, J	SNG151J, N	SN54H62J, N	7
TG151F	SNG151U	SN54H62W	7
TG152E, J	SNG152J, N	SN74H62J, N	7
TG152F	SNG152U	SN74H62W	7
TG153E, J	SNG153J, N	SN74H62J, N	7
TG153F	SNG153U	SN74H62W	7
TG160E, J	SNG160J, N	SN5438J, N	6
TG160F	SNG160U	SN5438W	6
TG161E, J	SNG161J, N	SN5438J, N	6
TG161F	SNG161U	SN5438W	6
TG162E, J	SNG162J, N	SN7438J, N	6
TG162F	SNG162U	SN7438W	6
TG163E, J	SNG163J, N	SN7438J, N	6
TG163F	SNG163U	SN7438W	6
TG170E, J	SNG170J, N	SN5460J, N	6
TG170F	SNG170U	SN5460W	6
TG171E, J	SNG171J, N	SN5460J, N	6
TG171F	SNG171U	SN5460W	6
TG172E, J	SNG172J, N	SN7460J, N	6
TG172F	SNG172U	SN7460W	6
TG173E, J	SNG173J, N	SN7460J, N	6
TG173F	SNG173U	SN7460W	6
TG180E, J	SNG180J, N	SN5430J, N	6
TG180F	SNG180U	SN5430W	6
TG181E, J	SNG181J, N	SN5430J, N	6
TG181F	SNG181U	SN5430W	6
TG182E, J	SNG182J, N	SN7430J, N	6
TG182F	SNG182U	SN7430W	6
TG183E, J	SNG183J, N	SN7430J, N	6
TG183F	SNG183U	SN7430W	6
TG190E, J	SNG190J, N	SN5410J, N	6
TG190F	SNG190U	SN5410W	6
TG191E, J	SNG191J, N	SN5410J, N	6
TG191F	SNG191U	SN5410W	6
TG192E, J	SNG192J, N	SN7410J, N	6
TG192F	SNG192U	SN7410W	6
TG193E, J	SNG193J, N	SN7410J, N	6
TG193F	SNG193U	SN7410W	6
TG200E, J	SNG200J, N	SN54H30J, N	7
TG200F	SNG200U	SN54H30W	7
TG201E, J	SNG201J, N	SN54H30J, N	7
TG201F	SNG201W	SN54H30W	7
TG202E, J	SNG202J, N	SN74H30J, N	7
TG202F	SNG202U	SN74H30W	7
TG203E, J	SNG203J, N	SN74H30J, N	7
TG203F	SNG203U	SN74H30W	7
TG210E, J	SNG210J, N	SN5455J, N	7
TG210F	SNG210U	SN54H55W	7
TG211E, J	SNG211J, N	SN54H55J, N	7
TG211F	SNG211U	SN54H55W	7
TG212E, J	SNG212J, N	SN74H55J, N	7
TG212F	SNG212U	SN74H55W	7
TG213E, J	SNG213J, N	SN74H55J, N	7
TG213F	SNG213U	SN74H55W	7
TG220E, J	SNG220J, N	SN54H00J, N	7
TG220F	SNG220U	SN54H00W	7

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DTL/TTL CIRCUITS

Transitron TTL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
TG221E, J	SNG221J, N	SN54H00J, N	7
TG221F	SNG221U	SN54H00W	7
TG222E, J	SNG222J, N	SN74H00J, N	7
TG222F	SNG222U	SN74H00W	7
TG223E, J	SNG223J, N	SN74H00J, N	7
TG223F	SNG223U	SN74H00W	7
TG230E, J	SGN230J, N	SN54H62J, N	7
TG230F	SNG230U	SN54H62W	7
TG231E, J	SNG231J, N	SN54H62J, N	7
TG231F	SNG231U	SN54H62W	7
TG232E, J	SNG232J, N	SN74H62J, N	7
TG232F	SNG232U	SN74H62W	7
TG233E, J	SNG233J, N	SN74H62J, N	7
TG233F	SNG233W	SN74H62W	7
TG240E, J	SNG240J, N	SN54H20J, N	7
TG240F	SNG240U	SN54H20W	7
TG241E, J	SNG241J, N	SN54H20J, N	7
TG241F	SNG241U	SN54H20W	7
TG242E, J	SNG242J, N	SN74H20J, N	7
TG242F	SNG242U	SN74H20W	7
TG243E, J	SNG243J, N	SN74H20J, N	7
TG243F	SNG243U	SN74H20W	7
TG250E, J	SNG250J, N	SN54H53J, N	7
TG250F	SNG250U	SN54H53W	7
TG251E, J	SNG251J, N	SN54H53J, N	7
TG251F	SNG251U	SN54H53W	7
TG252E, J	SNG252J, N	SN74H53J, N	7
TG252F	SNG252U	SN74H53W	7
TG253E, J	SNG253J, N	SN74H53J, N	7
TG253F	SNG253U	SN74H53W	7
TG260E, J	SNG260J, N	SN54H30J, N	7
TG260F	SNG260U	SN54H30W	7
TG261E, J	SNG261J, N	SN54H30J, N	7
TG261F	SNG261U	SN54H30W	7
TG262E, J	SNG262J, N	SN74H30J, N	7
TG262F	SNG262U	SN74H30W	7
TG263E, J	SNG263J, N	SN74H30J, N	7
TG263F	SNG263U	SN74H30W	7
TG270E, J	SNG270J, N	SN54H60J, N	7
TG270F	SNG270U	SN54H60W	7
TG271E, J	SNG271J, N	SN54H60J, N	7
TG271F	SNG271W	SN54H60W	7
TG272E, J	SNG272J, N	SN74H60J, N	7
TG272F	SNG272U	SN74H60W	7
TG273E, J	SNG273J, N	SN74H60J, N	7
TG273F	SNG273U	SN74H60W	7
TG280E, J	SNG280J, N	SN54H52J, N	7
TG280F	SNG280U	SN54H52W	7
TG281E, J	SNG281J, N	SN54H52J, N	7
TG281F	SNG281U	SN54H52W	7
TG282E, J	SNG282J, N	SN74H52J, N	7
TG282F	SNG282U	SN74H52W	7
TG283E, J	SNG283J, N	SN74H52J, N	7
TG283F	SNG283U	SN74H52W	7
TG290E, J	SNG290J, N	SN54H62J, N	7
TG290F	SNG290U	SN54H62W	7
TG291E, J	SNG291J, N	SN54H62J, N	7
TG291F	SNG291U	SN54H62W	7
TG292E, J	SNG292J, N	SN74H62J, N	7
TG292F	SNG292U	SN74H62W	7
TG293E, J	SNG293J, N	SN74H62J, N	7
TG293F	SNG293U	SN74H62W	7
TG300E, J	SNG300J, N	SN54H53J, N	7
TG300F	SNG300U	SN54H53W	7
TG301E, J	SNG301J, N	SN54H53J, N	7
TG301F	SNG301U	SN54H53W	7
TG302E, J	SNG302J, N	SN74H53J, N	7
TG302F	SNG302U	SN74H53W	7
TG303E, J	SNG303J, N	SN74H53J, N	7
TG303F	SNG303U	SN74H53W	7
TG310E, J	SNG310J, N	SN54H50J, N	7
TG310F	SNG310U	SN54H50W	7
TG311E, J	SNG311J, N	SN54H50J, N	7
TG311F	SNG311U	SN54H50W	7
TG312E, J	SNG312J, N	SN74H50J, N	7
TG312F	SNG312U	SN74H50W	7
TG313E, J	SNG313J, N	SN74H50J, N	7
TG313F	SNG313U	SN74H50W	7
TG320E, J	SNG320J, N	SN54H10J, N	7
TG320F	SNG320U	SN54H10W	7
TG321E, J	SNG321J, N	SN54H10J, N	7
TG321F	SNG321U	SN54H10W	7
TG322E, J	SNG322J, N	SN74H10J, N	7
TG322F	SNG322U	SN74H10W	7
TG323E, J	SNG323J, N	SN74H10J, N	7
TG323F	SNG323U	SN74H10W	7
TG350E, J	SNG351J, N	SN54S140J, N	5
TG350F	SNG351U	SN54S140W	5
TG352E, J	SNG353J, N	SN74S140J, N	5
TG352F	SNG353U	SN74S140W	5

MOS/LSI CIRCUITS

AMI

Type Number	Direct Replacement	Recommended for New Designs	Sec.
RD55		TMS 3002 LR	14
RD57		TMS 3002 LR	14
RD58		TMS 3002 LR	14
RD60		TMS 3002 LR	14
RD62		TMS 3104 LC/NC	14
RD63	TMS 3304 LR	TMS 3304 LR	14
RD64		TMS 3114 JC/NC	14
RD65		TMS 3401 LC/NC	14
MA51	TMS 2300 JC/NC	TMS 2300 JC/NC	14
MB51		TMS 2600 JC/NC	14
MX52		TMS 6009 JC/NC	14
MX53		TMS 6000 JC/NC	14
MX54		TMS 6009 JC/NC	14

A.M.S.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
AMD 91600111		TMS 4023 NC	14

CMI

Type Number	Direct Replacement	Recommended for New Designs	Sec.
CM1101	TMS 1101 JC	TMS 1101 JC/NC	14

Electronic Arrays

Type Number	Direct Replacement	Recommended for New Designs	Sec.
EA1003		TMS 3112 JC/NC	14
EA1007		TMS 3112 JC/NC	14
EA1004		TMS 3101 LC/NC	14
EA1005		TMS 3101 LC/NC	14
EA1200		TMS 3112 JC/NC	14
EA1201		TMS 3112 JC/NC	14
EA1204		TMS 3114 JC/NC	14
EA1205		TMS 3114 JC/NC	14
EA1206		TMS 3413 LC/NC	14
EA1208		TMS 3016 LR	14
EA1210		TMS 3412 JC/NC	14
EA1212		TMS 3412 JC/NC	14
EA1221		TMS 3101 JC/NC	14
EA1400		TMS 1101 JC/NC	14
EA1800		TMS 2200 JC/NC	14
EA1801		TMS 2200 JC/NC	14
EA1804		TMS 2200 JN/NC	14
EA1806		TMJ 2200 JC/NC	14
EA3001		TMS 2500 JC/NC	14
EA3101		TMS 2602 JC/NC	14
EA3300		TMS 4400 JC/NC	14
EA3307		TMS 2604 JC/NC	14
EA3500		TMS 2500 JC/NC	14

Electronic Arrays, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
EA3501		TMS 2501 JC/NC	14
EA3700		TMS 4100 JC/NC	14
EA3701		TMS 4103 JC/NC	14
EA4000		TMS 4400 JC/NC	14

Fairchild

Type Number	Direct Replacement	Recommended for New Designs	Sec.
3250		TMS 2500 JC/NC	14
3251		TMS 4400 JC/NC	14
3254		TMS 2500 JC/NC	14
3255		TMS 4100 JC/NC	14
3256		TMS 4100 JC/NC	14
3257		TMS 4100 JC/NC	14
3258		TMS 2500 JC/NC	14
3300		TMS 3000 LR	14
3303		TMS 3000 LR	14
3304		TMS 3016 LR	14
3305		TMS 3016 LR	14
3306		TMS 3016 LR	14
3307		TMS 3101 LC/NC	14
3320		TMS 3103 LC/NC	14
3325		TMS 3417 JC/NC	14
3326	TMS 3304 LC	TMS 3304 LC/NC	14
3330		TMS 3403 LC	14
3331		TMS 3402 LC/NC	14
3332		TMS 3305 LC	14
3377		TMS 3401 LC	
3383		TMS 3412 JC/NC	14
3501		TMS 2800 JC/NC	14
3507		TMS 2600 JC/NC	14
3512		TMS 2500 JC/NC	14
3513		TMS 2500 JC/NC	14
3514		TMS 2500 JC/NC	14
3530		TMS 1101 JC/NC	14
3532		TMS 1101 JC/NC	14
3580	TMS 2600 JC	TMS 2600 JC/NC	14
3584	TMS 2600 JC	TMS 2600 JC/NC	14
3700		TMS 6005 JC/NC	14
3701		TMS 6005 JC/NC	14
3810		TMS 2700 JC/NC	14

GI

Type Number	Direct Replacement	Recommended for New Designs	Sec.
DL-5-0406	TMS 3406 LC	TMS 3101 LC/NC	14
DL-5-1200		TMS 3101 LC/NC	14
DL-7-1200		TMS 3101 LC/NC	14
DL-5-1512		TMS 3401 LC/NC	14
DL-7-1512		TMS 3401 LC/NC	14
SL-6-2050		TMS 3002 LR	
SL-6-2064		TMS 3103 LC/NC	14
DL-6-2100		TMS 3101 LC/NC	14
RO-1-2240		TMS 2500 JC/NC	14
MU-6-2281		TMS 6000 JC/NC	14
DL-0-3066	TMS 3304 LR	TMS 3304 LR	14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS/LSI CIRCUITS

GI, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
SL-7-4025		TMS 3000 LR	14
SL-7-4032		TMS 3112 JC/NC	14
SS-6-8211		TMS 3016 LR	14
SS-6-8211		TMS 3016 LR	14
MEM2009		TMS 6003 JC/NC	14
MEM2017		TMS 6009 JC/NC	14
MEM3016	TMS 3016 LR	TMS 3016 LR	14
MEM3021	TMS 3021 LR	TMS 3021 LR	14
MEM3032-D2		TMS 3112 JC/NC	14
MEM3032-D5		TMS 3112 JC/NC	14
MEM3025		TMS 3000 LR	
MEM3064		TMS 3103 LC/NC	14
MEM3064 LR	TMS 3027 JC	TMS 3027 JC	14
MEM3064-2B		TMS 3103 LC/NC	14
MEM3100		TMS 3002 LR	14
MEM3100A2		TMS 3002 LR	14
MEM3128		TMS 3114 JC/NC	14
MEM3128-2		TMS 3114 JC/NC	14
MEM5021		TMS 5700 JC/NC	14

Intel

Type Number	Direct Replacement	Recommended for New Designs	Sec.
1101	TMS 1101 JC	TMS 1101 JC/NC	14
11001	TMS 1101 JC	TMS 1101 JC/NC	14
1103	TMS 1103 NC	TMS 1103 JC/NC	14
1301		TMS 2600 JC/NC	14
1402	TMS 3412 JC/NC	TMS 3412 JC/NC	14
1403	TMS 3413 JC	TMS 3413 JC/NC	14
1404	TMS 3414 JC	TMS 3414 JC/NC	14
1405		TMS 3401 LC/NC	14
1406	TMS 3406 LC	TMS 3101 LC/NC	14
1407	TMS 3407 LC	TMS 3101 LC/NC	14
1506	TMS 3406 LM	TMS 3101 LC/NC	14
1507	TMS 3407 LM	TMS 3101 LC/NC	14

Mostek

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MK1001L	TMS 3304 LR	TMS 3304 LR	14
MK1002P	TMS 3414 JC	TMS 3414 JC/NC	14
MK1003P		TMS 3412 LC/NC	14
MK2000P		TMS 4100 JC/NC	14
MK2001P		TMS 4103 JC/NC	14
MK2100P		TMS 2500 JC/NC	14
MK2101P		TMS 2501 JC/NC	14
MKB2300P		TMS 4100 JC/NC	14
TMS2302P		TMS 4103 JC/NC	14
TMS2400P	TMS 2300 JC/NC	TMS 2300 JC/NC	14
MK3100P		TMS 2500 JC/NC	14
MK3101P		TMS 2501 JC/NC	14
MK4001P	TMS 4003 JC	TMS 4003 JC/NC	14
MK4003P		TMS 4024 JC/NC	14

Motorola

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MCM1110	TMS 2600 JC	TMS 2600 JC/NC	14
MCM1120	TMS 2400 JC	TMS 2500 JC/NC	14
MCM1121	TMS 2400 JC	TMS 2500 JC/NC	14
MCM1122	TMS 2403 JC	TMS 2501 JC/NC	14
MC1124L		TMS 3802 LC	14
MC1125L		TMS 3802 LC	14
MCM1130	TMS 4100 JC	TMS 4100 JC/NC	14
MCM1131	TMS 4100 JC	TMS 4100 JC/NC	14
MCM1132	TMS 4103 JC	TMS 4103 JC/NC	14
MC1141G	TMS 3305 LR	TMS 3305 LR	14
MC1142G		TMS 3401 LC/NC	14
MC1150L		TMS 6000 JC/NC	14
MCM1150	TMS 2300 JC	TMS 2300 JC/NC	14
MC1160G	TMS 3003 LR	TMS 3101 LC/NC	14
MC1161G	TMS 3002 LR	TMS 3002 LR	14
MCM1170		TMS 1101 JC/NC	14
MCM1173		TMS 4023 NC	
MC2244G		TMS 3401 LC/NC	14
MC2246		TMS 3417 JC/NC	14
MCM2340		TMS 4400 JC/NC	14
MC2360G		TMS 3101 LC/NC	14
MC2362G		TMS 3412 JC/NC	14
MC2363G		TMS 3114 JC/NC	14
MCM2372	TMS 1103 NC	TMS 1103 NC	14
MC2380G		TMS 3101 LC/NC	14
MC2381G		TMS 3101 LC/NC	14
MC2384L	TMS 3412 JC	TMS 3412 JC/NC	14
MC2385G	TMS 3413 JC	TMS 3414 LC/NC	14
MC2386G	TMS 3414 JC	TMS 3414 LC/NC	14

National

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MM400/500		TMS 3000 LR	14
MM403/503		TMS 3002 LR	14
MM404/504		TMS 3016 LR	14
MM405/505		TMS 3112 JC/NC	14
MM406/506	TMS 3406 LC	TMS 3101 LC/NC	14
MM410/510		TMS 3103 LC/NC	14
MM421/521	TMS 2800 JC	TMS 2800 JC/NC	14
MM422/522		TMS 2600 JC/NC	14
MM422/522AP		TMS 2605 JC/NC	14
MM422BL/522BL		TMS 2607 JC/NC	14
MM422BN/522BN		TMS 2608 JC/NC	14
MM422DE/522DE		TMS 2605 JC/NC	14
MM422EK/522EK		TMS 2606 JC/NC	14
MM423/523	TMS 2600 JC	TMS 2600 JC/NC	14
MM423BO/523BO	TMS 2609 JC	TMS 2609 JC/NC	14
MM423FE/523FE	TMS 2610 JC	TMS 2610 JC/NC	14
MM4001/5001		TMS 3102 LC/NC	14
MM4006/5006		TMS 3101 LC/NC	14
MM400GD/500GD		TMS 3101 LC/NC	14
MM4010/5010		TMS 3103 LC/NC	14
MM4015A/5015A		TMS 3314 JC/NC	14
MM4016/5016		TMS 3401 LC/NC	14
MM4016D/5016D		TMS 3401 LC/NC	14
MM4018/5018		TMS 3103 LC/NC	14
MM4040/5040		TMS 3016 LR	14

National, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MM4050/5050		TMS 3112 JC/NC	14
MM4051/5051		TMS 3112 JC/NC	14
MM4051D/5051D		TMS 3112 JC/NC	14
MM4052/5052		TMS 3102 LC/NC	14
MM4053/5053		TMS 3101 LC/NC	14
MM5105		TMS 3403 LC/NC	14
MM4210/5210		TMS 2800 JC/NC	14
MM4211/5211		TMS 2600 JC/NC	14
MM4230/5230		TMS 2500 JC/NC	14
MM4231/5231		TMS 2500 JC/NC	14
MM4232/5232		TMS 4400 JC/NC	14
MM4240/5240		TMS 2500 JC/NC	14
MM4241/5241		TMS 2700 JC/NC	14
MM4250/5250	TMS 1101 JC	TMS 1101 JC/NC	14

Signetics

Type Number	Direct Replacement	Recommended for New Designs	Sec.
2001	TMS 3016 LR	TMS 3016 LR	14
2002	TMS 3000 LR	TMS 3000 LR	14
2003	TMS 3000 LR	TMS 3112 JC/NC	14
2004	TMS 3002 LR	TMS 3002 LR	14
2005	TMS 3003 LR	TMS 3101 LC/NC	14
2501	TMS 1101 JC	TMS 1101 JC/NC	14
2502	TMS 3412 JC	TMS 3412 JC/NC	14
2503	TMS 3413 LC	TMS 3413 LC/NC	14
2504	TMS 3414 LC	TMS 3414 LC/NC	14
2505		TMS 3401 LC/NC	14
2506		TMS 3101 LC/NC	14
2507		TMS 3101 LC/NC	14
2508		TMS 1103 NC	14
2509		TMS 3002 LR	14
2510		TMS 3101 LC/NC	14
2511		TMS 3101 LC/NC	14
2512		TMS 3414 LC/NC	14
2513		TMS 2500 JC/NC	14
2514		TMS 2500 JC/NC	14

Solitron

Type Number	Direct Replacement	Recommended for New Designs	Sec.
UC6525/7525		TMS 2600 JC/NC	14
UC6548/7548		TMS 2600 JC/NC	14
UC6550/7550	TMS 4026 JC	TMS 4026 JC/NC	14
UC6572/7572	TMS 2700 JC	TMS 2700 JC/NC	14
UC6596/7596		TMS 4400 JC/NC	14
UC65965/7596		TMS 4400 JC/NC	14
UC6577/7577		TMS 2500 JC/NC	14
UC7310		TMS 3413 JC/NC	14
UC7315		TMS 3112 JC/NC	14
UC7316		TMS 3016 LR	14
UC7320		TMS 3002 LR	14
UC7350		TMS 3417 JC/NC	14

Unisem

Type Number	Direct Replacement	Recommended for New Designs	Sec.
UA2524/3524		TMS 1103 NC	14
UA2525/3525		TMS 2600 JC/NC	14
UA2548/3548		TMS 2600 JC/NC	14
UA2552/3552		TMS 3113 LC/NC	14
UA2556/3556	TMS 1101 JC	TMS 1101 JC/NC	14
UA2564/3564		TMS 4026 JC/NC	14
UA2572/3572	TMS 2700 JC/NC	TMS 2700 JC/NC	14
UA2596/3596		TMS 4400 JC/NC	14
UA2664/3664	TMS 4026 JC	TMS 4026 JC/NC	14
UA3540		TMS 2500 JC/NC	14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

C

Discrete Semiconductors and Components

C

DISCRETE SEMICONDUCTORS AND COMPONENTS MANUFACTURED BY TEXAS INSTRUMENTS

In addition to its leadership position in integrated circuits, Texas Instruments is the world's largest supplier of discrete semiconductors and components.

Devices shown below represent TI's standard discrete semiconductors beginning with the 1N series, followed by 2N, in-house, and the resistor product lines. Note that consecutive type numbers are shown in condensed form: e.g. 1N253, 1N254, 1N255, and 1N256 devices are listed as 1N253–1N256.

C

1N251
1N253–1N256
1N332–1N349
1N440B–1N445B
1N456–1N459
1N456A–1N459A
1N461–1N464
1N461A–1N464A
1N482–1N485
1N482A–1N485A
1N482B–1N485B
1N530–1N540
1N547
1N550–1N555
1N599–1N606
1N599A–1N606A
1N607–1N614
1N607A–1N614A
1N607R–1N614R
1N607AR–1N614AR
1N625–1N629
1N643
1N645
1N645A
1N646–1N649
1N568–1N663
1N702–1N716
1N702A–1N716A
1N746–1N759
1N746A–1N759A
1N761–1N766
1N914–1N916
1N914A–1N916A
1N914B–1N916B
1N917
1N957–1N961
1N957A–1N961A
1N957B–1N961B
1N1095–1N1096
1N1100–1N1105
1N1115–1N1120
1N1124A–1N1128A
1N1124AR–1N1128AR
1N1487–1N1492
1N1581–1N1587
1N1612–1N1616
1N1692–1N1697
1N1816–1N1836
1N1816A–1N1836A
1N1816C–1N1836C
1N1816CA–1N1836CA
1N2069–1N2071
1N2069A–1N2071A
1N2175
1N2970–1N3011
1N2970A–1N3011A
1N2970B–1N3011B
1N3064
1N3070
1N3506–1N3517
1N3518–1N3520
1N4001–1N4007
1N4099
1N4100–1N4106
1N4148–1N4154
1N4305
1N4360
1N4370–1N4372
1N4370A–1N4372A
1N4444
1N4446–1N4449
1N4454
1N4531–1N4534
1N4536
1N4606
1N4727
1N4938
2N117–2N120
2N122
2N243–2N244
2N250–2N251
2N250A–2N251A
2N263–2N264
2N315A
2N317A
2N332–2N336
2N332A–2N336A
2N337–2N341
2N342
2N342A
2N343
2N377
2N388–2N389
2N388A–2N389A
2N395–2N397
2N398
2N398A
2N398B
2N404
2N404A
2N424
2N424A
2N426–2N428
2N438
2N438A
2N439–2N440
2N456A–2N458A
2N456B–2N458B
2N470–2N480
2N489–2N493
2N489A–2N493A
2N489B–2N493B
2N494
2N494A
2N494B
2N494C
2N497–2N498
2N497A–2N498A
2N508
2N511–2N512
2N511A–2N512A
2N511B–2N512B
2N520
2N520A
2N522A
2N541–2N543
2N581–2N582
2N587
2N594–2N596
2N634A–2N636A
2N656–2N657
2N656A–2N657A
2N658–2N662
2N696–2N699
2N705
2N706
2N706A
2N706B
2N708–2N710
2N711
2N711A
2N711B
2N717
2N718–2N720
2N718A–2N720A
2N721–2N722
2N730–2N731
2N743–2N744
2N797
2N849–2N852
2N870–2N871
2N910–2N912
2N914
2N917–2N918
2N929–2N930
2N929A–2N930A
2N956
2N960–2N975
2N985
2N997
2N1021–2N1022
2N1021A-2N1022A
2N1038–2N1045
2N1046–2N1050
2N1046A–2N1050A
2N1046B–2N1050B
2N1131–2N1132
2N1141–2N1143
2N1141A–2N1143A
2N1149–2N1156
2N1195
2N1273–2N1274
2N1276–2N1279
2N1302–2N1309
2N1370–2N1383
2N1404
2N1420
2N1507
2N1529–2N1548
2N1586–2N1599
2N1605
2N1613
2N1671
2N1671A
2N1671B
2N1690–2N1691
2N1711
2N1714–2N1721
2N1722
2N1722A
2N1723
2N1724
2N1724A
2N1725
2N1889–2N1893
2N1907–2N1908
2N1936–2N1937
2N1973–2N1975
2N1993–2N2001
2N2060
2N2102
2N2102A
2N2150–2N2151
2N2160
2N2188–2N2191
2N2192–2N2194
2N2192A–2N2194A
2N2217
2N2218–2N2219
2N2218A–2N2219A
2N2220
2N2221–2N2223
2N2221A–2N2223A
2N2243
2N2243A
2N2270
2N2303
2N2322–2N2326
2N2369
2N2369A
2N2386
2N2386A
2N2387–2N2390
2N2393–2N2396
2N2411–2N2412
2N2415–2N2416
2N2432
2N2432A
2N2453
2N2481
2N2483–2N2484
2N2497–2N2500
2N2537–2N2540
2N2552–2N2567
2N2586
2N2604–2N2605
2N2608–2N2609
2N2635
2N2639–2N2644
2N2646–2N2647
2N2659–2N2670
2N2802–2N2807
2N2861–2N2862
2N2880
2N2894
2N2904–2N2907
2N2904A–2N2907A
2N2913–2N2914
2N2915–2N2916
2N2915A–2N2916A
2N2917–2N2918
2N2919–2N2920
2N2919A–2N2920A
2N2944–2N2946
2N2944A–2N2946A
2N2972–2N2979
2N2987–2N2994
2N2996–2N3008
2N3010–2N3015
2N3036–2N3040
2N3043–2N3053
2N3114
2N3117
2N3146–2N3147
2N3244–2N3245
2N3250–2N3251
2N3250A–2N3251A
2N3252–2N3253
2N3328–2N3336
2N3347–2N3352
2N3371
2N3375
2N3418–2N3421
2N3444
2N3458–2N3460
2N3467–2N3468
2N3485–2N3486
2N3485A–2N3486A
2N3494–2N3497
2N3502–2N3505
2N3551–2N3562
2N3570–2N3576
2N3632
2N3680
2N3702–2N3716
2N3724–2N3725
2N3724A–2N3725A
2N3733
2N3789–2N3792
2N3798–2N3799
2N3806–2N3811
2N3819–2N3824
2N3829
2N3833–2N3835
2N3838
2N3846–2N3847
2N3866
2N3903–2N3906
2N3909
2N3909A
2N3962–2N3966
2N3970–2N3972
2N3980
2N3993–2N3994
2N3993A–2N3994A
2N3996–2N4005
2N4040–2N4041
2N4058–2N4062
2N4091–2N4093
2N4104
2N4138
2N4220–2N4222
2N4220A–2N4222A
2N4223–2N4224
2N4252–2N4253
2N4300–2N4301
2N4391–2N4393
2N4398–2N4399
2N4416
2N4416A
2N4418–2N4423
2N4851–2N4855
2N4856–2N4861
2N4856A–2N4861A
2N4874–2N4876
2N4891–2N4894
2N4901–2N4906
2N4913–2N4915
2N4947–2N4949
2N4994–2N4997
2N5043–2N5047
2N5058–2N5059
2N5245–2N5248
2N5273–2N5275
2N5301–2N5303
2N5332–2N5333

C

DISCRETE SEMICONDUTORS AND COMPONENTS MANUFACTURED BY TEXAS INSTRUMENTS (Contd)

2N5384—2N5390
2N5399
2N5447—2N5451
2N5543—2N5549
2N5938—2N5940
2N5949—2N5953
3N34—3N35
3N74—3N79
3N108—3N111
3N160—3N161
3N174
3N201—3N203
600C—601C
604C
606C
608C
610C
612C
614C
616C
618C
620C
622C
624C
650—653
650C0—650C7
651
651C0—651C9
652
652C0—652C9
653
653C0—653C9
654C9
655C9
A3T918
A3T929
A3T930
A3T2221—A3T2222
A3T2221A—A3T2222A
A3T2484
A3T2894
A3T2906—A3T2907
A3T2906A—A3T2907A
A3T3011
A4T918
A4T930
A4T1893
A4T2219A
A4T2243
A4T2369
A4T2432
A4T2484
A4T2605
A4T2894
A4T2907A
A4T2945
A4T3013
A4T3015
A4T3251A
A4T3570
A4T3702—A4T3716
A4T3725
A4T3822—A4T3823
A4T3829
A4T3890
A4T3993
A4T4058—A4T4062
A4T4416
A4T4496—A4T4497
A4T4857
A5T2222
A5T2907
A5T3644—A5T3645
A5T3903—A5T3906
A5T5058—A5T5059
A516—A517
A600—A602
A610—A612
A706—A713
A900—A903
A905—A908
G129—G130
H11
H35
H38
H60—H62
LSX400
LSX600
LSX900
TI51—TI60
TI71—TI75
SERIES TI145
TI156
TI156L
TI159—TI162
TI363—TI365
TI390—TI391
TI395
TI397—TI403
TI480—TI484
TI486—TI487
TI492—TI496
TI550—TI551
TI1121—TI1126
TI1131—TI1136
TI1141—TI1146
TI1151—TI1156
TI3027—TI3031
TIC35—TIC36
TIC44—TIC47
SERIES TIC250
SERIES TIC252
SERIES TIC260
SERIES TIC262
SERIES TIC270
SERIES TIC272
TID17—TID20
TID21A—TID26A
TID29A—TID30A
TID31—TID45
TID121—TID126
TID129—TID134
TIL23—TIL24
TIL58
TIL63—TIL67
TIL102—TIL103
TIL107—TIL108
TIL201—TIL208
TIL601—TIL616
TIP29—TIP36
TIP29A—TIP36A
TIP29B—TIP36B
TIP29C—TIP36C
TIP41—TIP42
TIP41A—TIP42A
TIP41B—TIP42B
TIP41C—TIP42C
TIP3055
TIS05
TIS14
TIS25—TIS27
TIS37—TIS39
TIS43
TIS56—TIS59
TIS62—TIS64
TIS68—TIS70
TIS73—TIS75
TIS78—TIS79
TIS84
TIS86—TIS87
TIS90—TIS93
TIS90M—TIS93M
TIS97—TIS101
TIS104—TIS119
TIV306—TIV308
TIXL05—TIXL06
TIXL12—TIXL22
TIXL26—TIXL30
TIXL51—TIXL53
TIXL55—TIXL57
TIXL59
TIXL68—TIXL76
TIXL104—TIXL106
TIXL109
TIXL151—TIXL152
TIXL301—TIXL302
TIXM101
TIXS33
TIXS35—TIXS36
TIXS80—TIXS81
TIXV01—TIXV04
XD500-XD502

RESISTORS AND SENSISTOR® RESISTORS

CD1/2MR—RN20X
CD1/2MR—RN20X
CD1/2MR—RN20X
CG1/8—RN55G
CG1/8—RN550—G
CG1/8—RN550—G
CG1/4—RN60D—G
CG1/4—RN60D—G
CG1/2—RN65D—G
CG1/2—RN65D—G
CG1/2—RN65D—G
MC50C—RN50C
MC50D
MC50E
MC55C—RN55C
MC55D—RN55D
MC55D—RC07
MC55E—RN55E
MC58C
MC58D
MC58E
MC60C—RN60C
MC60D—RN60D
MC60E—RN60E
MC61C
MC61D
MC61D—RL20
MC61E
MC65C—RN65C
MC65D—RN65D
MC65E—RN65E
MC65F—RN65F
MC66C
MC66D
MC66D—RL32
MC66E
MM60C—RN60C
MM60D
MM60E
MM65C—RN65C
MM65D
MM65E—RN65E
MM70C—RN70C
MM70D
MM70E—RN70E
P100 10 PCT
P100 5 PCT
TG1/8 10 PCT
TG1/8 5 PCT
TM1/8 10 PCT
TM1/8 5 PCT
TM1/4 10 PCT
TM1/4 5 PCT

LISTING OF PREFERRED SEMICONDUCTORS AND COMPONENTS BY DEVICE CLASSIFICATION

SILICON LOW-POWER N-P-N

TIS62	1025*
TIS63	1025
TIS84	1033
TIS86	1041
TIS87	1041
TIS97	1053
TIS98	1053
TIS99	1053
TIS100	1061
TIS101	1061
TIS108	1033
2N697	1201
2N930	1263
2N1613	1201
2N2219	1305
A3T2221	1313
A3T2221A	1317
2N2222	1305
A3T2222	1313
A3T2222A	1317
2N2243A	1301
2N2369A	1327
2N2432	1337
2N2484	1349
A3T2484	1269
A3T3011	1405
2N3013	1409
2N3015	1413
2N3704	1433
2N3705	1433
2N3706	1433
2N3707	1435
2N3708	1435
2N3709	1435
2N3710	1435
2N3711	1435
2N3725	1437
2N4252	1445
2N4994	1503
2N4995	1503
2N4996	1511
2N4997	1511
2N5449	1701
2N5450	1701
2N5451	1701

SILICON LOW-POWER P-N-P

TIS37	2001
TIS38	2001
2N2605	2119
2N2894	2125
A3T2894	2127
2N2905	2131
A3T2906	2135
A3T2906A	2135
2N2907	2131
A3T2907	2135
A3T2907A	2135
2N2945	2139
2N3250	2209*
2N3702	2225
2N3703	2225
2N3829	2235
2N4058	2301
2N4059	2301
2N4060	2301
2N4061	2301
2N4062	2301
2N5447	2305
2N5448	2305

SILICON UHF TRANSISTORS

2N918	3201
A3T918	3203
2N3570	3401
2N3866	3501
2N4875	3701

SILICON MULTIPLE AND MULTI-ELEMENT TRANSISTORS

3N79	4101
TIS92	4015
TIS92M	4105
TIS93	4105
TIS93M	4105
3N111	4109
2N997	4301
2N2060	4401
2N2223	4401
2N2639	4405
2N2642	4405
2N2643	4405
2N2920	4409
2N2977	4409
2N2979	4409
2N3350	4507
2N3680	4509
2N3838	4517
2N4854	4701

SILICON FIELD-EFFECT TRANSISTORS

TIS58	6091
TIS59	6091
TIS73	6103
TIS74	6103
TIS75	6103
3N160	6201
2N2386	6301
2N2498	6303
2N3330	6305
2N3819	6401
2N3820	6403
2N3822	6405
2N3823	6407
2N3909	6413
2N3993A	6501
2N4416	6503
2N4857	6511
2N5045	6601
2N5245	6703*
2N5246	6703
2N5247	6703
2N5248	6711

SILICON UNIJUNCTION

2N491A	7101
2N492A	7101
2N1671B	7109
2N3980	7201

GERMANIUM LOW-POWER ALLOY-JUNCTION TRANSISTORS

2N398	9101
2N404	9105
2N1302	9205
2N1303	9205
2N1304	9205
2N1305	9205
2N1306	9205
2N1307	9205
2N1308	9205
2N1309	9205
2N1377	9213
2N1997	9301
2N2000	9307

GERMANIUM MESA AND PLANAR SWITCHING TRANSISTORS

2N797	12101
2N964	12105
2N2635	12301

GERMANIUM UHF/MICROWAVE TRANSISTORS

2N5043	14401

SILICON POWER TRANSISTORS

TIP29A,B,C	16101
TIP30A,B,C	16105
TIP31A,B,C	16109
TIP32A,B,C	16113
TIP33A,B,C	16117
TIP34A,B,C	16121
TIP35A,B,C	16125
TIP36A,B,C	16129
2N1724	16301
TIP3055	
2N2987	16401*
2N2988	16401
2N2989	16401
2N2990	16401
2N2991	16401
2N2992	16401
2N2993	16401
2N2994	16401
2N3418	16501
2N3419	16501
2N3420	16501
2N3421	16501
2N3551	16507
2N3552	16507
2N3713	16511
2N3714	16511
2N3715	16511
2N3716	16511
2N3789	16557
2N3790	16557
2N3791	16557
2N3792	16557
2N3846	16579
2N3847	16579
2N3996	16601
2N3997	16601
2N3998	16601
2N3999	16601
2N4000	16607
2N4001	16607
2N4002	16613
2N4003	16613
2N4300	16625
2N4301	16631
2N4398	16645
2N4399	16645
2N5301	16687
2N5302	16687
2N5303	16687
2N5333	16701
2N5384	16707
2N5385	16707
2N5386	16711
2N5387	16715
2N5388	16715

GERMANIUM POWER TRANSISTORS

2N456A	17101
2N1038	17201
2N1539	17223
2N1907	17231
TI3027	17301

GENERAL PURPOSE DIODES

1N456	18101
1N457	18101
1N458	18101
1N459	18101
1N482	18109

* Page number of Preferred Semiconductors and Components Catalog — CC201

LISTING OF PREFERRED SEMICONDUCTORS AND COMPONENTS BY DEVICE CLASSIFICATION (Cont'd.)

GENERAL PURPOSE DIODES (Cont'd.)

1N483	18109*
1N484	18109
1N485	18109
1N645	18113
1N646	18113
1N647	18113
1N648	18113
1N649	18113

SWITCHING DIODES

1N251	19101
1N661	19151
1N914	19201
1N914B	19201
1N3070	19303
1N4148	19401
1N4154	19403
1N4448	19401
1N4454	19405

MULTIPLE DIODES

TID21	20005
TID22	20005
TID23	20005
TID24	20005
TID25	20009
TID26	20009
TID29	20013
TID30	20013

TUNING DIODES

TIV306	21205
TIV307	21205
TIV308	21205

REGULATOR DIODES

1N746	23109
1N746A	23109
1N747	23109
1N747A	23109
1N748	23109
1N748A	23109
1N749	23109
1N749A	23109
1N750	23109
1N750A	23109
1N751	23109
1N751A	23109
1N752	23109
1N752A	23109
1N753	23109
1N753A	23109
1N754	23109
1N754A	23109
1N755	23109
1N755A	23109
1N756	23109
1N756A	23109*
1N757	23109
1N757A	23109
1N758	23109
1N758A	23109
1N759	23109
1N759A	23109
1N4370	23601
1N4370A	23601
1N4371	23601
1N4371A	23601
1N4372	23601
1N4372A	23601

THYRISTORS AND TRIGGER DIODES

TI42A	24105
TI43A	24105
TIC44	24109
TIC45	24109
TIC46	24109
TIC47	24109
2N3001	24401
2N3002	24401
2N3003	24401
2N3004	24401
2N3005	24407
2N3006	24407
2N3007	24407
2N3008	24407
2N3555	24417
2N3556	24417
2N3557	24417
2N3558	24417
2N3559	24425
2N3560	24425
2N3561	24425
2N3562	24425

SILICON RECTIFIERS

1N4001	25401
1N4002	25401
1N4003	25401
1N4004	25401
1N4005	25401
1N4006	25401
1N4007	25401

OPTOELECTRONIC DEVICES

TIL01	27001
TIL09	27009
LS400	27401
LS600	27501
TIL601	27503
TIL602	27503
TIL603	27503
TIL604	27503
TIL605	27503
TIL606	27503*
TIL607	27503
TIL608	27503
1N2175	27801

PRECISION FILM RESISTORS

CG1/8	28201
CG1/4	28201
CG1/2	28201
MC50	28401
MC55	28401
MC60	28401
MC65	28401

TEMPERATURE-SENSING SILICON RESISTORS

TG1/8	29001
TM1/8	29001
TM1/4	29001

* Page number of Preferred Semiconductors and Components Catalog — CC201

APPLICATIONS GUIDE TO PREFERRED SEMICONDUCTORS AND COMPONENTS

APPLICATION	DEVICE RECOMMENDATION							
	BIPOLAR				FET			
	N-P-N		P-N-P		N-CHANNEL		P-CHANNEL	
	Type No.	Page No.*	Type No.	Page No.*	Type No.	Page No.*	Type No.	Page No.*
Small-Signal Transistor:	•A3T2484	1269	•A3T2906	2135	TIS58	6091	2N2386	6301
Amplifier:	•TIS92	4105	•A3T2907	2135	TIS59	6091	•2N2498	6303
	•TIS92M	4105	•A3T2906A	2135	•2N3819	6401	•2N3330	6305
DC to 1 MHz	•TIS97	1053	•A3T2907A	2135	•2N3822	6405	•2N3820	6403
	•TIS98	1053	•TIS93	4105			2N3909	6413
	TIS99	1053	•TIS93M	4105				
	2N697	1201	2N404	9105				
	2N930	1263	2N1303	9205				
	•2N997	4301	2N1305	9205				
	•2N1302	9205	2N1307	9205				
	•2N1304	9205	2N1309	9205				
	•2N1306	9205	2N2000	9307				
	•2N1308	9205	2N2605	2119				
	•2N2484	1349	•2N2905	2131				
	2N3704	1433	•2N2907	2131				
	2N3705	1433	2N3702	2225				
	2N3706	1433	2N3703	2225				
	2N3707	1435	•2N4058-62	2301				
	2N3708	1435	•2N5447	2305				
	2N3709	1435	2N5448	2305				
	2N3710	1435						
	2N3711	1435						
	•2N5449	1701						
	•2N5450	1701						
	•2N5451	1701						
1 MHz to 10 MHz	•A3T2484	1269	•TIS37	2001	TIS58	6091	2N2386	6301
	2N697	1201	2N404	9105	TIS59	6091	•2N2498	6303
	2N930	1263	2N1303	9205	•2N3819	6401	•2N3330	6305
	2N1302	9205	2N1305	9205	•2N3822	6405	•2N3820	6403
	2N1304	9205	2N1307	9205	•2N3823	6407	2N3909	6413
	2N1306	9205	2N1309	9205	•2N4416	6503		
	2N1308	9205	2N1377	9213	•2N5245	6703		
	2N1613	1201	2N1997	9301	•2N5246	6703		
	•2N2484	1349	2N2605	2119	•2N5247	6703		
	2N3704	1433	•2N2905	2131	•2N5248	6711		
	2N3705	1433	2N3702	2225				
	2N3706	1433	2N3703	2225				
	2N4994	1503	2N5447	2305				
	•2N4995	1503	2N5448	2305				
	•2N4996	1511						
	•2N4997	1511						
	2N5449	1701						
	2N5450	1701						
	2N5451	1701						
10 MHz to 50 MHz	TIS63	1025	•TIS37	2001	TIS58	6091	•2N2498	6303
	•TIS84	1033	•2N5043	14401	TIS59	6091	•2N3330	6305
	•TIS86	1041			•2N3819	6401		
	•TIS87	1041			•2N3822	6405		
	•TIS108	1033			•2N3823	6407		
	2N918	3201			•2N4416	6503		
	•2N2219	1305			•2N5245	6703		
	•2N2222	1305			•2N5246	6703		
	•2N2243A	1301			•2N5247	6703		
	2N4252	1445			•2N5248	6711		
	•2N4996	1511						
	•2N4997	1511						
50 MHz to 100 MHz	•TIS63	1025	•2N2905	2131	•2N3823	6407	•2N2498	6303
	•TIS86	1041	•2N2907	2131	•2N4416	6503	•2N3330	6305
	•TIS87	1041	•2N5043	14401	•2N5245	6703		
	•TIS108	1033			•2N5246	6703		
	2N918	3201			•2N5247	6703		
	•2N2219	1305						
	•2N2222	1305						
	2N4252	1445						
	•2N4875	3701						
	•2N4996	1511						
	•2N4997	1511						

• Devices especially recommended for new design

* Preferred Semiconductors and Components Catalog

C

APPLICATIONS GUIDE TO PREFERRED SEMICONDUCTORS AND COMPONENTS (Cont'd.)

APPLICATION	DEVICE RECOMMENDATION							
	BIPOLAR				FET			
	N-P-N		P-N-P		N-CHANNEL		P-CHANNEL	
	Type No.	Page No.*	Type No.	Page No.*	Type No.	Page No.*	Type No.	Page No.*
100 MHz to 5 GHz	•TIS84	1033	•2N5043	14401	•2N3823	6407		
	2N918	3201			•2N4416	6503		
	•2N3570	3401			•2N5245	6703		
	2N4252	1445			•2N5246	6703		
	•2N4875	3701			•2N5247	6703		
Low-Noise Amplifier:	•A3T2484	1269	•TIS37	2001	•2N3822	6405	•2N2498	6303
	•TIS97	1053	2N2605	2119	•2N4416	6503	•2N3330	6305
0 to 10 MHz	2N930	1263	•2N4058-62	2301	•2N5248	6711		
	•2N2484	1349						
	2N3707	1435						
10 MHz to 50 MHz	•A3T918	3203	•TIS37	2001	•2N3822	6405		
	•TIS62	1025			•2N3823	6407		
	•TIS86	1041			•2N4416	6503		
	2N918	3201			•2N5245	6703		
	•2N4252	1445			•2N5246	6703		
	•2N4875	3701			•2N5247	6703		
	•2N4997	1511			•2N5248	6711		
50 MHz to 100 MHz	•A3T918	3203	•2N5043	14401	•2N3823	6407		
	•TIS62	1025			•2N4416	6503		
	•TIS86	1041			•2N5245	6703		
	2N918	3201			•2N5246	6703		
	•2N3570	3401			•2N5247	6703		
	2N4252	1445			•2N5248	6711		
	•2N4875	3701						
	•2N4997	1511						
100 MHz to 1 GHz	•A3T918	3203	•2N5043	14401	•2N3823	6407		
	•TIS86	1041			•2N4416	6503		
	2N918	3201			•2N5245	6703		
	•2N3570	3401			•2N5246	6703		
	•2N4875	3701			•2N5247	6703		
Mixer and Converter:	2N918	3201	•TIS37	2001	TIS58	6091	•2N2498	6303
0 to 10 MHz	•2N4995	1503			TIS59	6091	•2N3330	6305
					•2N3823	6407		
					•2N4416	6503		
10 MHz to 50 MHz	•TIS63	1025	•TIS37	2001	TIS58	6091	•2N3820	6403
	•TIS86	1041			TIS59	6091		
	2N4252	1445			•2N3823	6407		
	•2N4875	3701			•2N4416	6503		
	•2N4994	1503			•2N5245	6703		
	•2N4995	1503			•2N5246	6703		
					•2N5247	6703		
					•2N5248	6711		
50 MHz to 100 MHz	•TIS63	1025	•2N5043	14401	•2N3823	6407		
	•TIS86	1041			•2N4416	6503		
	•2N3570	3401			•2N5245	6703		
	2N4252	1445			•2N5246	6703		
	•2N4875	3701			•2N5247	6703		
	•2N4997	1511			•2N5248	6711		
100 MHz to 5 GHz	•A3T918	3203	•2N5043	14401	•2N3823	6407		
	•TIS86	1041			•2N4416	6503		
	2N918	3201			•2N5246	6703		
	•2N3570	3401			•2N5247	6703		
	2N4252	1445			•2N5248	6711		
	•2N4875	3701						
	•2N4997	1511						
Oscillator:	•TIS98	1053	•TIS38	2001	•2N3819	6401	•2N2498	6303
0 to 10 MHz	2N697	1201	•2N2905	2131	•2N3822	6405	•2N3330	6305
	2N1613	1201	2N3702	2225	•2N3823	6407		
	•2N2484	1349	•2N5447	2305	•2N4416	6503		
	2N3704	1433			•2N5248	6711		
	2N3711	1435						
	•2N5449	1701						

• Devices especially recommended for new design

* Preferred Semiconductors and Components Catalog

APPLICATIONS GUIDE TO PREFERRED SEMICONDUCTORS AND COMPONENTS (Cont'd.)

APPLICATION	DEVICE RECOMMENDATION							
	BIPOLAR				FET			
	N-P-N		P-N-P		N-CHANNEL		P-CHANNEL	
	Type No.	Page No.*	Type No.	Page No.*	Type No.	Page No.*		
10 MHz to 50 MHz	•A3T918	3203	•TIS38	2001	•2N3822	6405		
	•TIS63	1025	•2N2905	2131	•2N3823	6407		
	•TIS98	1053	•2N2907	2131	•2N4416	6503		
	2N918	3201	•2N5447	2305	•2N5245	6703		
	•2N2219	1305			•2N5246	6703		
	•2N2222	1305			•2N5247	6703		
	2N3704	1433			•2N5248	6711		
	•2N4875	3701						
	•2N4994	1503						
	•2N5449	1701						
50 MHz to 100 MHz	•A3T918	3203	2N3702	2225	•2N3823	6407		
	•TIS63	1025	•2N5043	14401	•2N4416	6503		
	•TIS86	1041	•2N5447	2305	•2N5245	6703		
	2N918	3201			•2N5246	6703		
	2N3704	1433			•2N5247	6703		
	•2N4875	3701			•2N5248	6711		
	•2N5449	1701						
100 MHz to 5 GHz	•A3T918	3203	•2N5043	14401	•2N3823	6407		
	•TIS63	1025			•2N4416	6503		
	•TIS86	1041			•2N5245	6703		
	2N918	3201			•2N5246	6703		
	•2N3570	3401			•2N5247	6703		
	•2N4875	3701						
	•2N4997	1511						
Power Oscillator:	•2N3866	3501						
Power Amplifier:	•2N3866	3501						
Radio Frequency	•2N4875	3701						
Audio Frequency	•TIP29	16101	•TIP30	16105	•2N4857	6511		
	•TIP29A,B,C	16101	•TIP30A,B,C	16105				
	•TIP31	16109	•TIP32	16113				
	•TIP31A,B,C	16109	•TIP32A,B,C	16113				
	•TIP33	16117	•TIP34	16121				
	•TIP33A,B,C	16117	•TIP34A,B,C	16121				
	•TIP35	16125	•TIP36	16129				
	•TIP35A,B,C	16125	•TIP36A,B,C	16129				
	2N697	1201	2N456A	17101				
	2N1613	1201	2N1038	17201				
	•2N5301	16687	•2N2905	2131				
	•2N5302	16687	•2N2907	2131				
	•2N5303	16687	TI3027	17301				
			•2N3789	16557				
			•2N3790	16557				
			•2N3791	16557				
			•2N3792	16557				
			•2N3846	16579				
			•2N4398	16645				

	BIPOLAR				OTHER DEVICES		
	N-P-N		P-N-P				
	Type No.	Page No.*	Type No.	Page No.*	Type No.	Page No.*	Classification
Switching:	•A3T2221	1313	•A3T2894	2127	•2N3980	7201	UJT
Multivibrator,	•A3T2221A	1317	•A3T2906	2135	•2N4416	6503	N-FET
Pulse Generator,	•A3T2222	1313	•A3T2906A	2135	•2N4857	6511	N-FET
Schmitt Trigger	•A3T2222A	1317	•A3T2907	2135			
	•A3T3011	1405	•A3T2907A	2135			
	2N1302	9205	2N404	9105			
	2N1304	9205	2N1303	9205			
	2N1306	9205	2N1305	9205			
	2N1308	9205	2N1307	9205			
	•2N2219	1305	2N1309	9205			
	•2N2222	1305	2N1997	9301			
	•2N2369A	1327	2N2000	9307			

• Devices especially recommended for new design

* Preferred Semiconductors and Components Catalog

C

APPLICATIONS GUIDE TO PREFERRED SEMICONDUCTORS AND COMPONENTS (Cont'd.)

APPLICATION	DEVICE RECOMMENDATION: BIPOLAR N-P-N Type No.	Page No.*	BIPOLAR P-N-P Type No.	Page No.*	OTHER DEVICES Type No.	Page No.	Classification
	•2N3013	1409	2N2635	12301			
	•2N3725	1437	•2N2894	2125			
			•2N2905	2131			
			•2N2907	2131			
			•2N3829	2235			
Ring Counter/ Latching Amplifier	2N930	1263	•2N2894	2125	•2N3001-4	24401	SCR
	•2N2369A	1327	•2N2905	2131	•2N3555-8	24417	SCR
	•2N3013	1409	•2N3250	2209	•2N4416	6503	N-FET
	2N3704	1433	2N3702	2225	•2N4857	6511	N-FET
	•2N5449	1701	•2N3829	2235	•TIS73	6103	N-FET
			•2N4058-62	2301	TIS74	6103	N-FET
			•2N5447	2305	TIS75	6103	N-FET
Relaxation Oscillator					•TI42A	24105	Trigger Diode
					•TI43A	24105	Trigger Diode
					2N1671B	7109	UJT
					•2N3980	7201	UJT
Pulse Amplifier	•2N2243A	1301	2N1907	17231	•2N4857	6511	N-FET
	•2N2369A	1327	•2N2894	2125			
			•2N2905	2131			
			•2N3829	2235			
			•2N5333	16701			
			•2N5384	16707			
			•2N5386	16711			
Chopper	•TIP29	16101	•TIP30	16105	2N3993A	6501	P-FET
	•TIP29A,B,C	16101	•TIP30A,B,C	16105	•2N4857	6511	N-FET
	•TIP31	16109	•TIP32	16113			
	•TIP31A,B,C	16109	•TIP32A,B,C	16113			
	•TIP33	16117	•TIP34	16121			
	•TIP33A,B,C	16117	•TIP34A,B,C	16121			
	•TIP35	16125	•TIP36	16129			
	•TIP35A,B,C	16125	•TIP36A,B,C	16129			
	•2N2432	1337	•2N2945	2139			
	•2N5301	16687	•2N3789	16557			
	•2N5302	16687	•2N3790	16557			
	•2N5303	16687	•2N3791	16557			
	•3N79	4101	•2N3792	16557			
			•2N4398	16645			
			•2N4399	16645			
			•3N111	4109			
Computer Memory Driver	•2N3013	1409			•TIS73	6103	N-FET
	•2N3015	1413			TIS74	6103	N-FET
	•2N3725	1437			TIS75	6103	N-FET
					•2N4857	6511	N-FET
Power Control/ Regulator (See Selection Guide on pages 11-14)	•TIP29	16101	•TIP30	16105	•TIC44-7	24109	SCR
	•TIP29A,B,C	16101	•TIP30A,B,C	16105	•2N3001-4	24401	SCR
	•TIP31	16109	•TIP32	16113	•2N3005-8	24407	SCR
	•TIP31A,B,C	16109	•TIP32A,B,C	16113	•2N3555-8	24417	SCR
	•TIP33	16117	•TIP34	16121	•2N3559-62	24425	SCR
	•TIP33A,B,C	16117	•TIP34A,B,C	16121			
	•TIP35	16125	•TIP36	16129			
	•TIP35A,B,C	16125	•TIP36A,B,C	16129			
	2N1724	16301	2N456A	17101			
	•2N2987-94	16401	2N1539	17223			
	•2N3418-21	16501	2N1907	17231			
	•2N3551,2	16507	TI3027	17301			
	•2N3713-16	16511	•2N3789	16557			
	•2N3996-9	16601	•2N3790	16557			
	•2N4000,1	16607	•2N3791	16557			
	•2N4002,3	16613	•2N3792	16557			
	•2N4300	16625	•2N4398	16645			
	•2N4301	16631	•2N4399	16645			
	•2N5301	16687	•2N5333	16701			

• Devices especially recommended for new design

* Preferred Semiconductors and Components Catalog

APPLICATIONS GUIDE TO PREFERRED SEMICONDUCTORS AND COMPONENTS (Cont'd.)

APPLICATION	DEVICE RECOMMENDATION: BIPOLAR N-P-N Type No.	Page No.*	BIPOLAR P-N-P Type No.	Page No.*	OTHER DEVICES Type No.	Page No.*	Classification
	•2N5302	16687	•2N5384	16707			
	•2N5303	16687	•2N5385	16707			
	•2N5387,8	16715	•2N5386	16711			
Computer Logic Switch	2N797	12101	2N404	9105	•TIS73	6103	N-FET
	2N1302	9205	2N964	12105	TIS74	6103	N-FET
	2N1304	9205	2N1303	9205	TIS75	6103	N-FET
	2N1306	9205	2N1305	9205	•2N4857	6511	N-FET
	2N1308	9205	2N1307	9205			
	•2N2369A	1327	2N1309	9205			
	•2N3013	1409	2N1997	9301			
			2N2635	12301			
			•2N2894	2125			
			•2N3250	2209			
			•2N3829	2235			
Series Shunt Regulator	•TIP29	16101	•TIP30	16105	•2N4857	6511	N-FET
	•TIP29A,B,C	16101	•TIP30A,B,C	16105			
	•TIP31	16109	•TIP32	16113			
	•TIP31A,B,C	16109	•TIP32A,B,C	16113			
	•TIP33	16117	•TIP34	16121			
	•TIP33A,B,C	16117	•TIP36	16125			
	•TIP35	16125	•TIP36A,B,C	16129			
	•TIP35A,B,C	16125	2N456A	17101			
	2N1724	16301	2N1038	17201			
	•2N2987-94	16401	2N1539	17223			
	•2N3418-21	16501	2N1907	17231			
	•2N3551,2	16507	TI3027	17301			
	•2N3713-16	16511	•2N5333	16701			
	•2N3996-9	16601	•2N5384	16707			
	•2N4000,1	16607	•2N5385	16707			
	•2N4002,3	16613	•2N5386	16711			
	•2N4300	16625					
	•2N4301	16631					
	•2N5387,8	16715					
Lamp Driver (Nixie Driver) High Voltage	•TIS100	1061	2N398	9101	•2N4857	6511	N-FET
	•TIS101	1061					
	•2N2243A	1301					
Linear Application: Demodulator	•3N79	4101	2N1907	17231	•2N4857	6511	N-FET
	•2N2432	1337					
Differential Amplifier	•2N2060	4401	•2N3350	4507	•2N5045	6601	N-FET
	•2N2642	4405					
	•2N3680	4509					
	•2N3838	4517					
	•2N2920	4409					
	•2N2977	4409					
	•2N2979	4409					
Operational Amplifier	•2N2060	4401	•2N3350	4507	•2N4854	4701	NPN-PNP
	•2N2223	4401			•2N5045	6601	N-FET
	•2N2642	4405					
	•2N3680	4509					
Servo Amplifier	•2N2060	4401	2N1038	17201	•2N5045	6601	N-FET
	•2N2223	4401	2N1907	17231			
	•2N2642	4405	•2N3350	4507			
	•2N3680	4509					
Sense Amplifier/ Comparator	•2N2060	4401	•2N3350	4507	•2N4416	6503	N-FET
	•2N2642	4405			•2N5045	6601	N-FET
	•2N3680	4509					
	•2N3838	4517					
	•2N2920	4409					
	•2N2977	4409					
	•2N2979	4409					
Waveform Generator/ Clipper/Compressor	2N930	1263	2N3702	2225	•2N4416	6503	N-FET
	2N3707	1435	•2N5447	2305	•2N4857	6511	N-FET

• Devices especially recommended for new design

* Preferred Semiconductors and Components Catalog

C

APPLICATIONS GUIDE TO PREFERRED SEMICONDUCTORS AND COMPONENTS (Cont'd.)

APPLICATION	DEVICE RECOMMENDATION						
	BIPOLAR				OTHER DEVICES		
	N-P-N		P-N-P				
	Type No.	Page No.*	Type No.	Page No.*	Type No.	Page No.*	Classification
	2N3704	1433					
	2N3708	1435			•2N5245	6703	N-FET
	2N3709	1435			•2N5246	6703	N-FET
	2N3711	1435			•2N5247	6703	N-FET
	•2N5449	1701			•2N5248	6711	N-FET
					•2N492A	7101	UJT
Diode: Mixer/Converter					1N456-9	18101	
					1N482-5	18109	
					1N914	19201	
Detector					1N456-8	18101	
					•1N459	18101	
					1N914	19201	
					•1N4148	19401	
					•1N4448	19401	
Switch					•1N251	19101	
					•1N661	19151	
					1N914	19201	
					•1N3070	19303	200 V
					•1N4148	19401	
					•1N4448	19401	
					•1N4154	19403	
Tuning					•TIV306-8	21205	Voltage Variable
Voltage Regulator					1N746-1N759	23109	
					•1N746A-1N759A	23109	
					1N4370	23601	
					•1N4370A	23601	
Rectifier					1N456-9	18101	
					1N482-5	18109	
					•1N645-9	18113	
					•1N4001-7	25401	
Computer					•TID21-24	20005	8-Diode Array
					•TID25-26	20009	16-Diode Array
					•TID29-30	20013	20-Diode Array
					1N914	19201	
Transistor Biasing					•1N746A-1N759A	23109	
TV "Color Killer"					•1N3070	19303	
Power Supply					•1N645-9	18113	
Logarithmic					•1N645-9	18113	
					•1N746A-1N759A	23109	
Light Sensor					•LS400	27401	
					•LS600	27501	
					•TIL601	27503	
					•TIL602	27503	
					•TIL603	27503	
					•TIL604	27503	
					•TIL605	27503	
					•TIL606	27503	
					•TIL607	27503	
					•TIL608	27503	
					•1N2175	27801	
Infrared Source					•TIL01	27001	
					•TIL09	27009	

• Devices especially recommended for new design

* Preferred Semiconductors and Components Catalog

The following curves, arranged in ascending order of rated power dissipation at 100°C case temperature, show typical h_{FE} versus collector current at 25°C case temperature. Listed above each curve are the standard open-base collector-emitter voltage ratings available from among the device types listed.

N-P-N
2N2987-2N2994
10 W at 100°C
15 W at 25°C
V_{CEO}: 80 V and 100 V

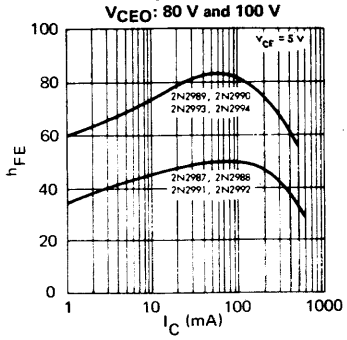


FIGURE 1

N-P-N
2N3418-2N3421
10 W at 100°C
15 W at 25°C
V_{CEO}: 60 V and 80 V

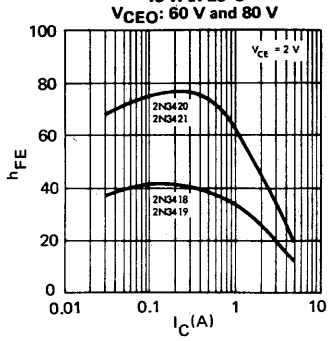


FIGURE 2

N-P-N
TIP29, TIP29A
12 W at 100°C
30 W at 25°C
V_{CEO}: 40 V and 60 V

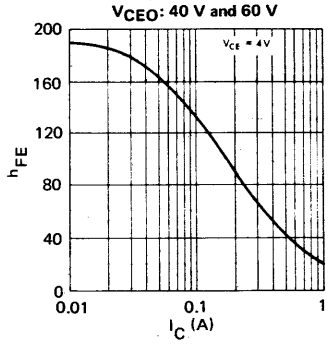


FIGURE 3

P-N-P
TIP30, TIP30A
12 W at 100°C
30 W at 25°C
V_{CEO}: 40 V and 60 V

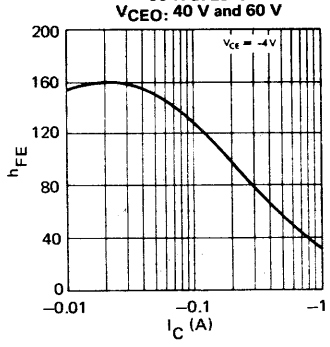


FIGURE 4

N-P-N
2N4000-2N4001
15 W at 100°C
V_{CEO}: 80 V and 100 V

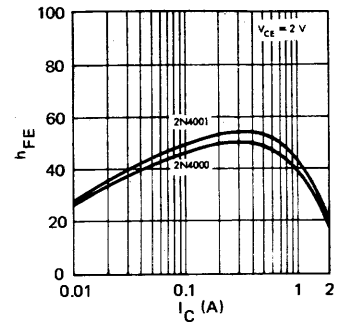


FIGURE 5

N-P-N
2N4300
15 W at 100°C
V_{CEO}: 80 V

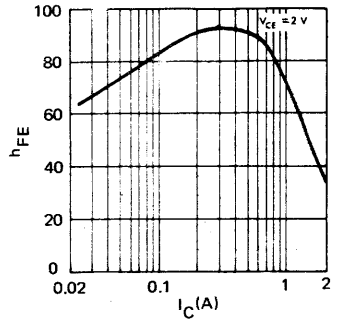


FIGURE 6

SELECTION GUIDE
SILICON POWER TRANSISTORS

C

P-N-P
2N5333
15 W at 100°C
V_{CEO}: 80 V

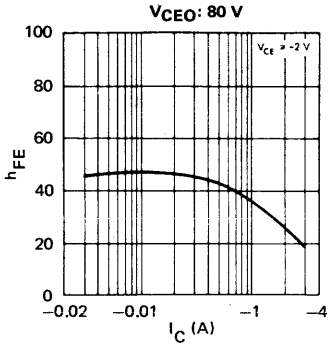


FIGURE 7

N-P-N
TIP31, TIP31A
16 W at 100°C
40 W at 25°C
V_{CEO}: 40 V and 60 V

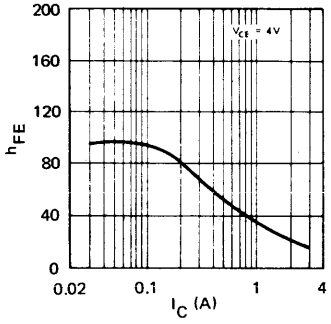


FIGURE 8

P-N-P
TIP32, TIP32A
16 W at 100°C
40 W at 25°C
V_{CEO}: 40 V and 60 V

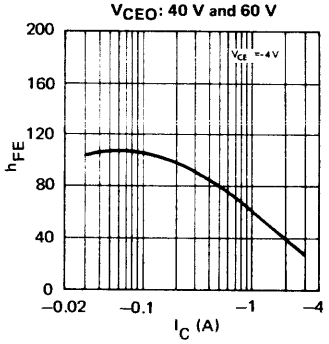


FIGURE 9

N-P-N
2N3996-2N3999
30 W at 100°C
V_{CEO}: 80 V

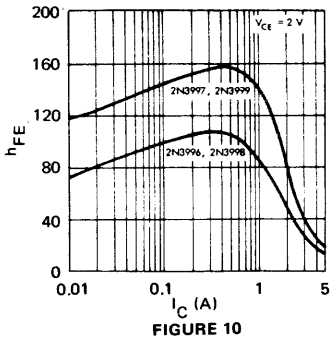


FIGURE 10

N-P-N
TIP33, TIP33A
32 W at 100°C
80 W at 25°C
V_{CEO}: 40 V and 60 V

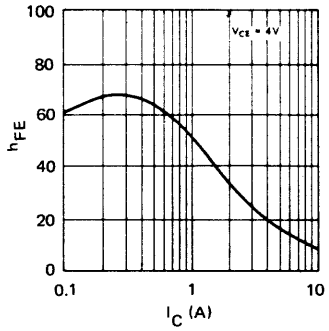


FIGURE 11

P-N-P
TIP34, TIP34A
32 W at 100°C
80 W at 25°C
V_{CEO}: 40 V and 60 V

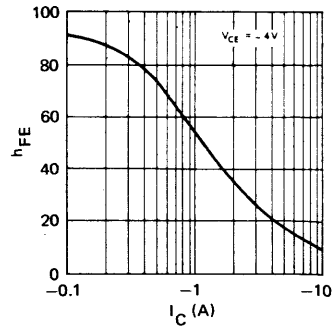


FIGURE 12

C

N-P-N
TIP35, TIP35A
36 W at 100°C
90 W at 25°C
V_{CEO}: 40 V and 60 V

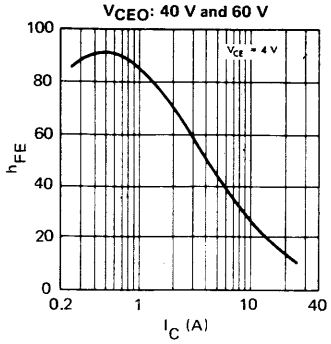


FIGURE 13

P-N-P
TIP36, TIP36A
36 W at 100°C
90 W at 25°C
V_{CEO}: 40 V and 60 V

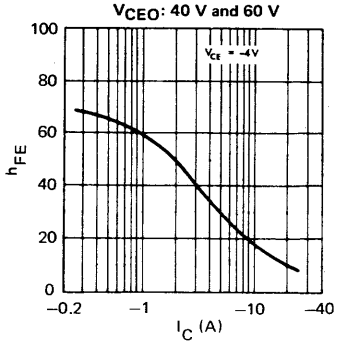


FIGURE 14

N-P-N
2N3551-2N3552
40 W at 100°C
V_{CEO}: 60 V and 80 V

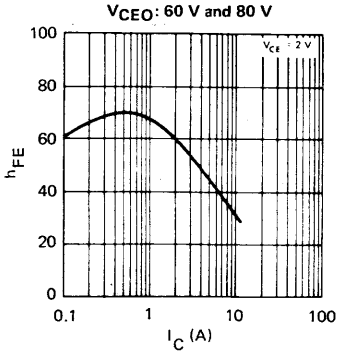


FIGURE 15

N-P-N
2N1724
50 W at 100°C
V_{CEO}: 80 V

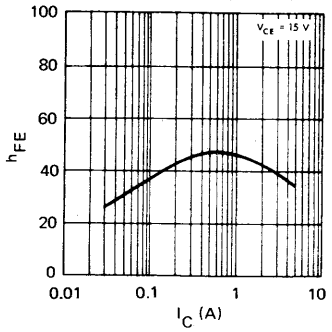


FIGURE 16

N-P-N
2N4301
50 W at 100°C
V_{CEO}: 80 V

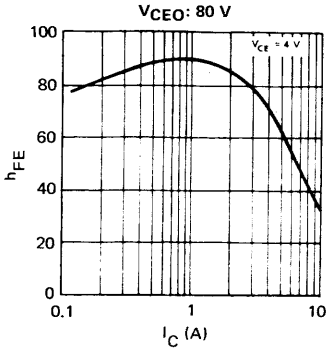


FIGURE 17

N-P-N
2N3713-2N3716
85 W at 100°C
150 W at 25°C
V_{CEO}: 60 V and 80 V

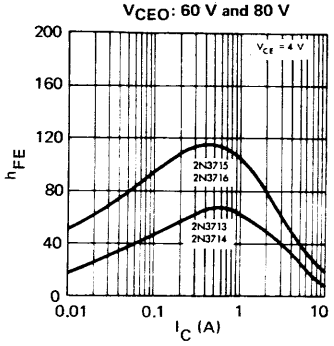


FIGURE 18

SELECTION GUIDE
SILICON POWER TRANSISTORS

C

P-N-P
2N3789-2N3792
85 W at 100°C
150 W at 25°C
V_{CEO}: 60 V and 80 V

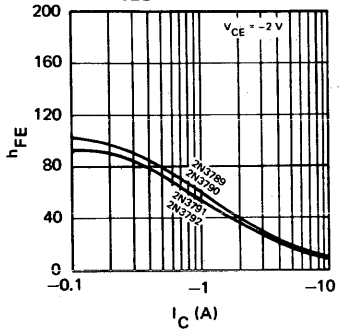


FIGURE 19

N-P-N
2N4002-2N4003
100 W at 100°C
V_{CEO}: 80 V and 100 V

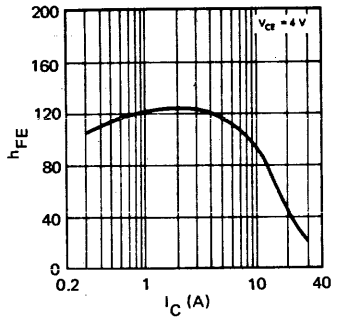


FIGURE 20

N-P-N
2N5387-2N5388
100 W at 100°C
V_{CEO}: 200 V and 250 V

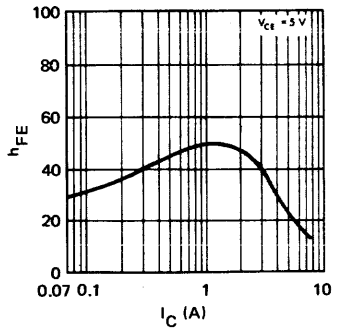


FIGURE 21

N-P-N
2N5301-2N5303
114 W at 100°C
200 W at 25°C
V_{CEO}: 40 V, 60 V, and 80 V

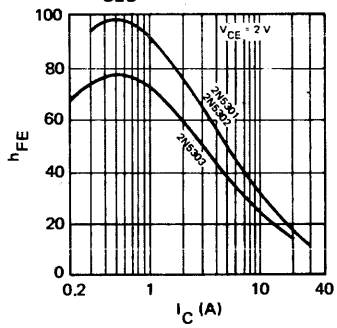


FIGURE 22

P-N-P
2N4398-2N4399
115 W at 100°C
200 W at 25°C
V_{CEO}: 40 V and 60 V

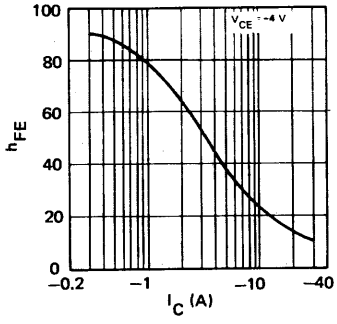


FIGURE 23

N-P-N
2N3846, 2N3847
150 W at 100°C
V_{CEO}: 200 V and 300 V

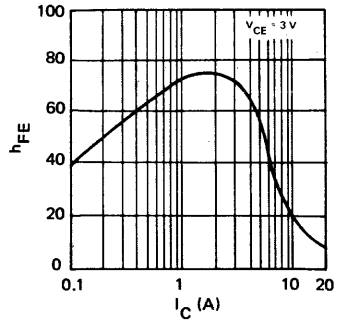


FIGURE 24

Ordering Instructions and Mechanical Data

ORDERING INSTRUCTIONS

Electrical characteristics presented in this catalog, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. Except for diode arrays, ECL, and MOS devices, the availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section. Other designations and packages are shown on individual data sheets.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

EXAMPLE: SN 54H72 N –00

1. Prefix

MUST CONTAIN TWO OR THREE LETTERS
(From Individual Data Sheet)

RSN	Radiation-Hardened Circuit
SN	Standard Prefix
SNM	Mach IV, Level I
SNA	Mach IV, Level II
SNC	Mach IV, Level III
SNH	Mach IV, Level IV
SNX	Experimental Circuit

2. Unique Circuit Description

MUST CONTAIN THREE TO SIX CHARACTERS
(From Individual Data Sheet)

Examples: F50, G50, 5410, 74H10, 54S112, 54L78, 15830, 75450A

3. Package

MUST CONTAIN A SINGLE LETTER
F, H, J, L, N, P, S, T, U, W, or Z
(From Pin-Connection Diagram on Individual Data Sheet)

4. Instructions (Dash No.)

MUST CONTAIN TWO NUMBERS
(From Dash No. Column of Following Table)

PACKAGES	FORMED LEADS	SOLDER-DIPPED LEADS	INSULATOR	CARRIER	ORDER DASH NO.
METAL FLAT PACKAGES					
F, S, T	No	No	No	†	00
F, S, T	Yes	No	Yes	†	01
F, S, T	No	No	No	Mech-Pak	02
F, S, T	No	No	Yes	Mech-Pak	03
F, S, T	Yes	No	No	Mech-Pak	04
F, S, T	Yes	No	Yes	Mech-Pak	05
F, S, T	No	No	Yes	†	06
F, S, T	Yes	No	No	†	07
F, S, T	No	Yes	No	†	10
F, S, T	Yes	Yes	Yes	†	11
F, S, T	No	Yes	No	Mech-Pak	12
F, S, T	No	Yes	Yes	Mech-Pak	13
F, S, T	Yes	Yes	No	Mech-Pak	14
F, S, T	Yes	Yes	Yes	Mech-Pak	15
F, S, T	No	Yes	Yes	†	16
F, S, T	Yes	Yes	No	†	17
CERAMIC FLAT PACKAGES					
H, U, W, Z	No	No	N/A	†	00
H	No	No	N/A	Mech-Pak	02
H, U, W, Z	No	Yes	N/A	†	10
DUAL-IN-LINE PACKAGES					
J, N, P	No	No	N/A	†	00
N	Yes	No	N/A	†	07
J, N, P	No	Yes	N/A	†	10
N	Yes	Yes	N/A	†	17
PLUG-IN PACKAGES					
L	No	No	N/A	†	00
L	No	Yes	N/A	†	10

†These circuits are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method which will best suit your particular needs.

Flat (F, H, S, T, U, W, Z)
- –Mech-Pakette
- –Barnes Carrier
- –Milton Ross Carrier

Dual-in-line (J, N, P)
- –Slide Magazines
- –A-Channel Plastic Tubing
- –Barnes Carrier
- –Sectioned Cardboard Box
- –Individual Plastic Box

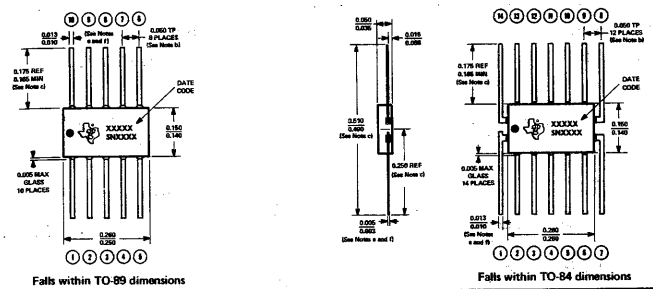
Plug-in (L)
- –Barnes Carrier
- –Sectioned Cardboard Box
- –Individual Plastic Box

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

F, S, and T flat packages

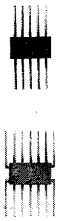
These hermetic packages feature glass-to-metal seals and welded construction. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram.

10- AND 14-PIN F AND S FLAT PACKAGE OUTLINES

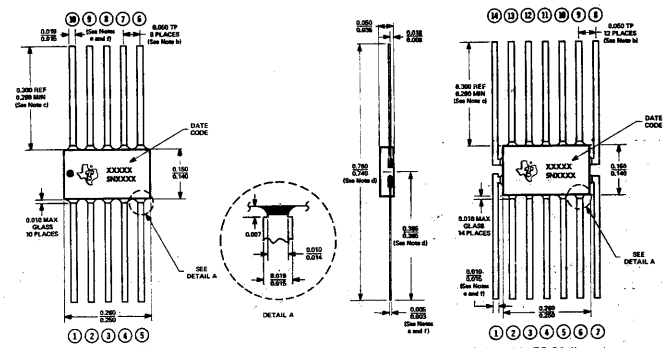


Falls within TO-89 dimensions

Falls within TO-84 dimensions



10- AND 14-PIN T FLAT PACKAGE OUTLINES



Falls within TO-89 dimensions

Falls within TO-84 dimensions

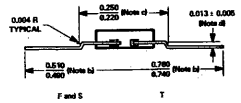
CIRCUIT SUBSTRATE IS ELECTRICALLY INSULATED FROM THE BODY OF THE F PACKAGE.
CIRCUIT SUBSTRATE IS IN ELECTRICAL CONTACT WITH THE BODY OF THE S AND T PACKAGES.

NOTES: a. All dimensions are in inches.
b. Lead centerlines are located within 0.005 of true position (TP) relative to body centerlines. This is measured along lines located within 0.030 from (and parallel to) the sides of the package.
c. Not applicable in Mech-Pak carrier.
d. Symbolization denotes orientation of package.
e. This dimension does not apply for solder-dipped leads.
f. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to within 0.050 of the package body.

F, S, and T package leads

Gold-plated F-15‡ leads require no additional cleaning or processing when used in soldered or welded assembly. Solder-dipped leads are also available. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Circuits can be removed from Mech-Pak carriers with lead lengths up to 0.175 inch for the F and S packages and up to 0.300 inch for the T package.

FORMED LEADS



F and S T

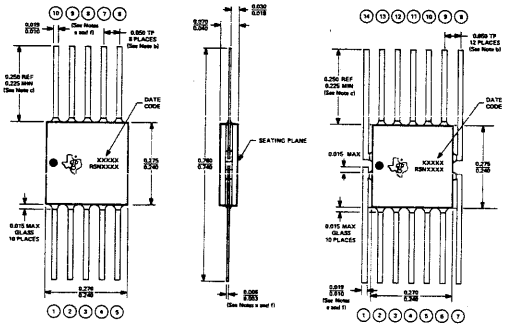
NOTES: a. All dimensions are in inches.
b. Not applicable in Mech-Pak carrier.
c. Measured from centerline of outside bends.
d. Measured from center of lead to bottom of package where lead emerges from body.
e. When solder-dipped leads are specified, dipped area of lead extends from lead tip to outside bend (minimum).

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

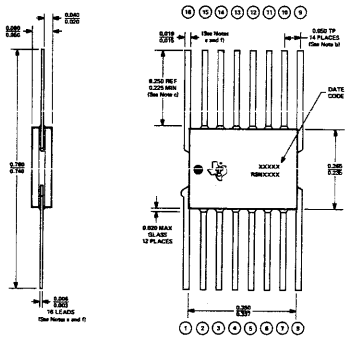
H flat packages

These packages each consist of a ceramic base, ceramic cap, and a 10- or 14-lead frame. Hermetic sealing is accomplished with glass. Gold-plated leads (–00) require no additional cleaning or processing when used in welded or soldered assembly.

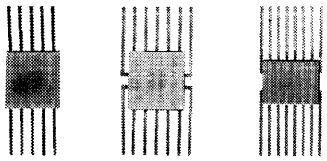
10- AND 14-PIN H CERAMIC FLAT PACKAGE OUTLINES



16-PIN H CERAMIC FLAT PACKAGE OUTLINE



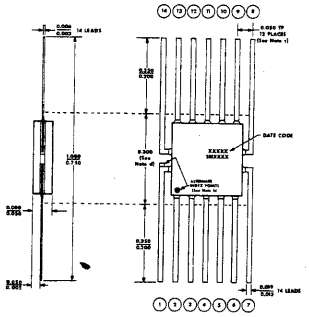
NOTES:
a. All dimensions are in inches.
b. Lead centerlines are located within 0.005 of true position (TP) relative to body centerlines. This is measured along lines located within 0.030 from (and parallel to) the sides of the package.
c. Not applicable in Mech-Pak carrier.
d. Symbolization denotes orientation of package.
e. This dimension does not apply for solder-dipped leads.
f. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to within 0.050 of the package body.



U and Z flat packages

These flat packages consist of a ceramic base, ceramic cap, and 14-lead frame. Circuit bars are alloy-mounted in the U package and glass-mounted in the Z package. Hermetic sealing is accomplished with glass. Tin-plated leads require no additional cleaning or processing when used in soldered assembly.

14-PIN U AND Z CERAMIC FLAT PACKAGE OUTLINES



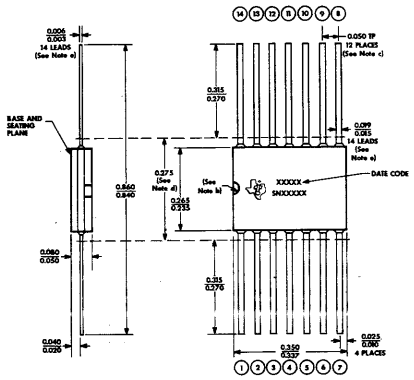
NOTES:
a. All dimensions are in inches.
b. Terminal identification is provided by either an index tab on pin 1 or an index dot.
c. Leads are within 0.005 radius of true position (TP) at maximum material condition.
d. This dimension determines a zone within which all body and lead irregularities lie.

Falls Within
MO-004AA Dimensions

W ceramic flat packages

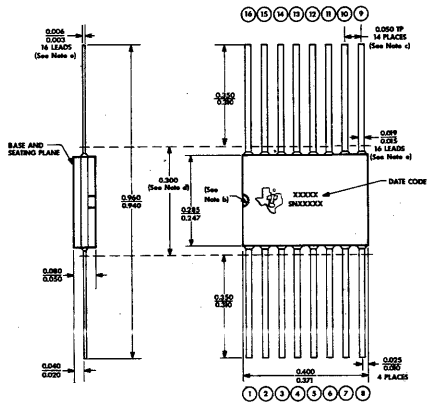
These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap, and a 14-, 16- or 24-lead frame. Hermetic sealing is accomplished with glass. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

14-PIN W CERAMIC
FLAT PACKAGE OUTLINE



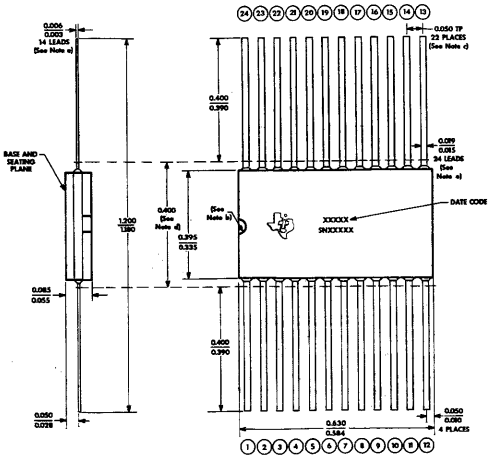
Falls Within
JEDEC MO-004AA Dimensions

16-PIN W CERAMIC
FLAT PACKAGE OUTLINE



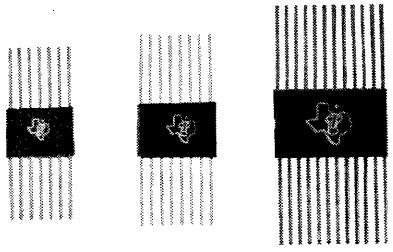
Falls Within
JEDEC MO-004AG Dimensions

24-PIN W CERAMIC
FLAT PACKAGE OUTLINE



Falls Within
JEDEC MO-019AA Dimensions

NOTES:
a. All dimensions are in inches.
b. Index point is provided on cap for terminal identification only.
c. Leads are within 0.005 radius of true position (TP) at maximum material condition.
d. This dimension determines a zone within which all body and lead irregularities lie.
e. Not applicable for solder-dipped leads.
f. When solder-dipped leads are specified, dipped area extends from lead tip to within 0.050 of package body.

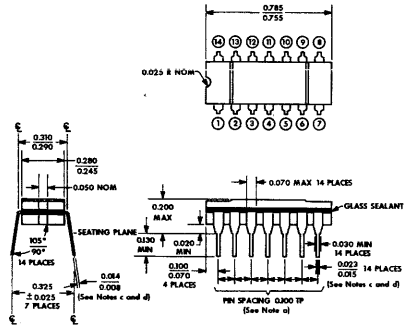


J ceramic dual-in-line packages

These hermetically-sealed, dual-in line packages consist of a ceramic base, ceramic cap, and a 14-, 16-, or 24-lead frame. The circuit bar is alloy-mounted to the base and hermetic sealing is accomplished with glass. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

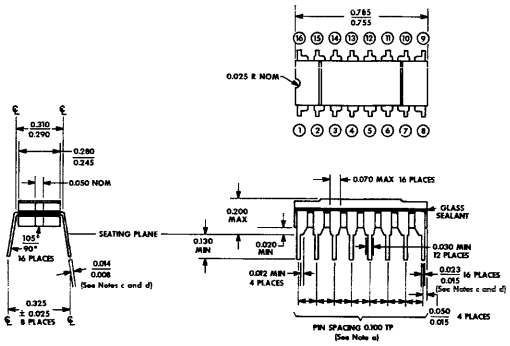
1

14-PIN J CERAMIC
DUAL-IN-LINE PACKAGE OUTLINE

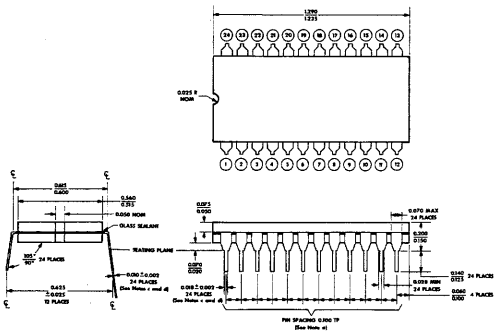


Falls Within JEDEC TO-116 and MO-001AA Dimensions

16-PIN J CERAMIC
DUAL-IN-LINE PACKAGE OUTLINE

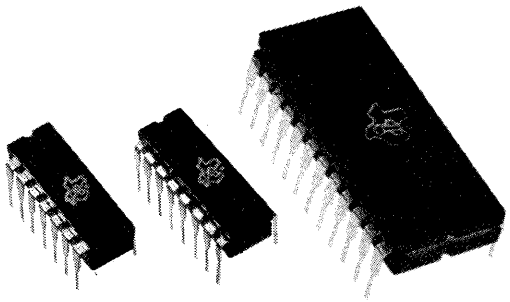


24-PIN J CERAMIC
DUAL-IN-LINE PACKAGE OUTLINE



Falls Within JEDEC MO-015AA Dimensions

NOTES:
a. Each pin centerline is located within 0.010 of its true longitudinal position.
b. All dimensions are in inches unless otherwise noted.
c. This dimension does not apply for solder-dipped leads.
d. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 above the seating plane.

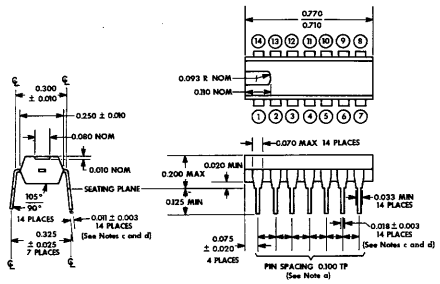


TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

N plastic dual-in-line packages

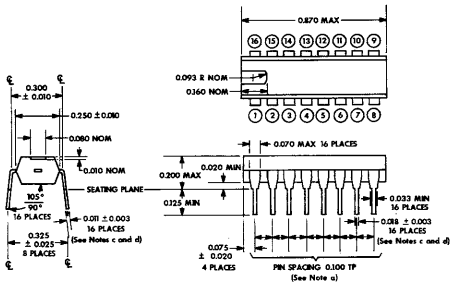
These dual-in-line packages consist of a circuit mounted on a 14-, 16-, or 24-lead frame and encapsulated within an electrically nonconductive, plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 0.300-inch (or 0.600-inch) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads (–00) require no additional cleaning or processing when used in soldered assembly.

14-PIN N PLASTIC
DUAL-IN-LINE PACKAGE OUTLINE

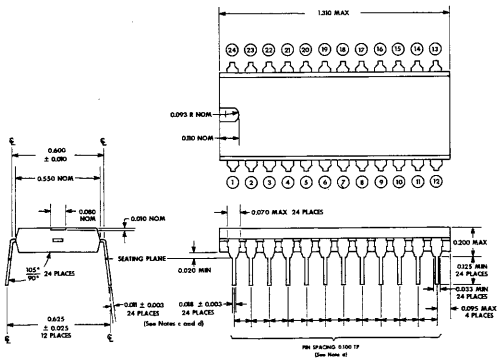


Falls Within JEDEC TO-116 and
MO-001AA Dimensions

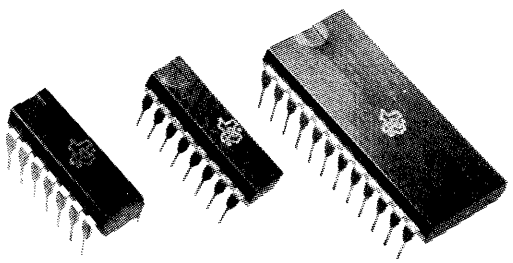
16-PIN N PLASTIC
DUAL-IN-LINE PACKAGE OUTLINE



24-PIN N PLASTIC
DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. Each pin centerline is located within 0.010 of its true longitudinal position.
b. All dimensions are in inches unless otherwise noted.
c. This dimension does not apply for solder-dipped leads.
d. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 above the seating plane.



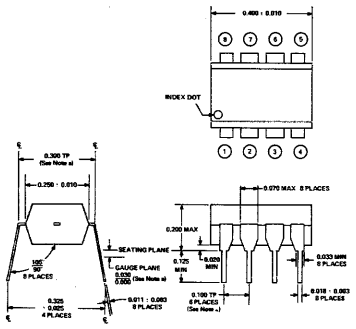
INTEGRATED CIRCUITS MECHANICAL DATA

P plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a 8-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

1

8-PIN P PLASTIC DUAL-IN-LINE PACKAGE OUTLINE

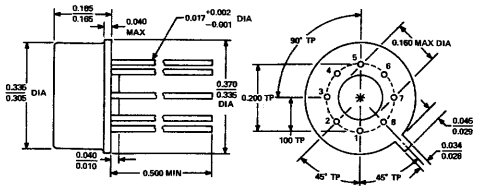


NOTES: a. Each pin is within 0.005 radius of true position (TP) at the guage plane with maximum material condition and unit installed.
b. All dimensions are in inches unless otherwise noted.

L plug-in packages

These hermetically sealed, plug-in packages each consist of a welded metal base and cap with individual leads secured by an insulating glass sealant. The gold-plated leads (–00) require no additional cleaning or processing when used in soldered assembly.

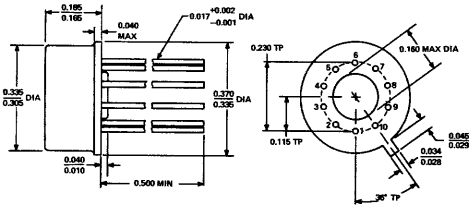
8-PIN L PLUG-IN PACKAGE OUTLINE



ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED.

Same as JEDEC TO-99 and MO-002AK except for diameter of standoff

10-PIN L PLUG-IN PACKAGE OUTLINE



ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED.

Same as JEDEC TO-100 and MO-006AD except for diameter of standoff

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Mach IV Procurement Specification

2

CONTENTS

MACH IV PROGRAM

1.0 SCOPE

1.1 This specification establishes standards for materials, workmanship, performance capabilities, identification and processing of high reliability, monolithic integrated circuits.

1.2 Intent

The intent of this document is such as to recognize that quality and reliability are *built* into, not *tested* into, a product. There is no specification or screening procedure that can substitute for inherent, built-in reliability. However, it must be realized that irrespective of lot quality, there will always be some small percentage of devices that are subject to early failure (infant mortality). A well engineered screening procedure will eliminate most, if not all, of these early failures. Secondly, the screening and acceptance testing described herein will also serve to demonstrate, with a high degree of statistical confidence, that the required levels of quality and reliability have, in fact, been built into the product.

2.0 APPLICABLE DOCUMENTS

2.1 The following specifications and standards, of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extend specified herein:

2.2 Specifications

Military

MIL-M-55565	Microcircuits, Packaging of
MIL-M-38510	Microcircuits Devices, General Specification for

2.3 Standards

Military

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-883	Test Methods and Procedures for Microelectronics (dated November 20, 1969)
MIL-STD-790	Reliability Assurance Program for Electronic Parts Specification
MIL-STD-1276	Leads, Weldable, for Electronic Components Parts
MIL-STD-1313	Microelectronics Terms and Definitions
MSFC-STD-355	Radiographic Inspection Standard for Electronic Parts

Detail Specifications

SNXXXX	Detail Specification for a Particular Part Type (e.g., Manufacturer's (Data Sheet)

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

2.4 Precedence of Documents

For the purpose of interpretation, in case of any conflicts, the following order of precedence shall apply:

a)	Purchase Order	—The purchase order shall have precedence over any referenced specification.
b)	Detail Specification	—The detail specification shall have precedence over this specification and other referenced specifications.
c)	This Specification	—This specification shall have precedence over all referenced specifications.
d)	Referenced Specifications	—Referenced Specifications shall apply to the extend specified herein.

2

2.5 Federal and/or military specifications and standards required shall be obtained from the usual government sources.

3.0 GENERAL REQUIREMENTS

The individual item requirements shall be as specified herein and in accordance with the applicable detail specification. In the event of any conflict between the requirements of this specification and the detail specification, the latter shall govern. The static and dynamic electrical performance requirements of the integrated circuits plus absolute maximum ratings and test methods shall be as specified in the detail specifications.

3.1.1 Definitions

a)	LTPD	Lot Tolerance Percent Defective shall be as defined by MIL-M-38510.
b)	λ	Lambda, stated in percent per 1000 hours as defined by MIL-M-38210.
c)	MRN	Minimum Reject Number as defined by MIL-M-38210
d)	Production Lot	For the purpose of this specification, a production lot shall be defined per MIL-M-38510.
f)	C	Acceptance number as defined by MIL-M-38510

3.1.2 Terms and Definitions

Terms and definitions shall be as defined in MIL-STD-1313.

3.1.3 Classification of Requirements

The requirements for the integrated circuits are classified herein as follows:

Requirement	Paragraph
Processing Conditioning, Testing and Screening	3.2
Qualification	3.3
Design and Construction	3.4
Marking of Integrated Circuits	3.5
Product Assurance	3.6
Workmanship	3.7
Performance Capabilities	3.8

3.2 Process Conditioning, Testing and Screening

Four levels of quality assurance for integrated circuits are provided for in this specification. Process conditioning, testing and screening shall be as specified in 4.3 and the applicable figure for the appropriate quality assurance level stated on the purchase order and defined as follows:

Prefix	Quality Assurance Process Level	Applicable Process Flow Chart
SNM	I	Figure 1
SNA	II	Figure 2
SNC	III	Figure 3
SNH	IV	Figure 4

3.3 Qualification

Vendor qualification for delivery of integrated circuits to this specification shall be as specified in paragraph 4.2.

3.4 Design and Construction

Integrated circuit design and construction shall be in accordance with the requirements specified herein and in the applicable detail specification.

3.4.1 Topography

Integrated circuits furnished under this specification shall have topography information available for review by procuring activity. The information made available shall provide sufficient data for thorough circuit design, application, performance, and failure analysis studies.

3.4.1.1 Monolithic Die Topography

An enlarged photograph or drawing (to scale) with a minimum magnification of 80 times the die (chip) size showning the topography of elements formed on the silicon monolithic die shall be available for review. This shall be identified with the specific detail integrated circuit part-type in which it is used and the applicable detail specification.

3.4.1.2 Die Intraconnection Pattern

An enlarged photograph or drawing (to scale) with a minimum magnification of 80 times the die (chip) size showing the specific intraconnection pattern utilized to intraconnect the elements in the circuit. This shall be in the same scale as the die topography 3.4.1.1 so that the elements utilized and those not being used can easily be determined.

3.4.2 Materials

Materials shall be inherently non-nutrient to fungus and shall not blister, crack, outgas, soften, flow or exhibit other immediate or latent defects that adversely affect storage, operation or environmental capabilities of integrated circuits.

3.4.2.1 Material Section

Materials selected for use in the construction of the integrated circuits shall be chosen for maximum suitability for the application. This shall include consideration of the best balance for:

a) Electrical performance

b) Thermal compatibility and conductivity

c) Chemical stability including resistance to deleterious interactions with other materials

d) Metallurgical stability with respect to adjacent materials and change in crystal configuration

e) Maximum stability with regard to continued uniform performance through the specified environmental conditions and life.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PROCESS FLOW CHART FOR LEVEL I (SNM)

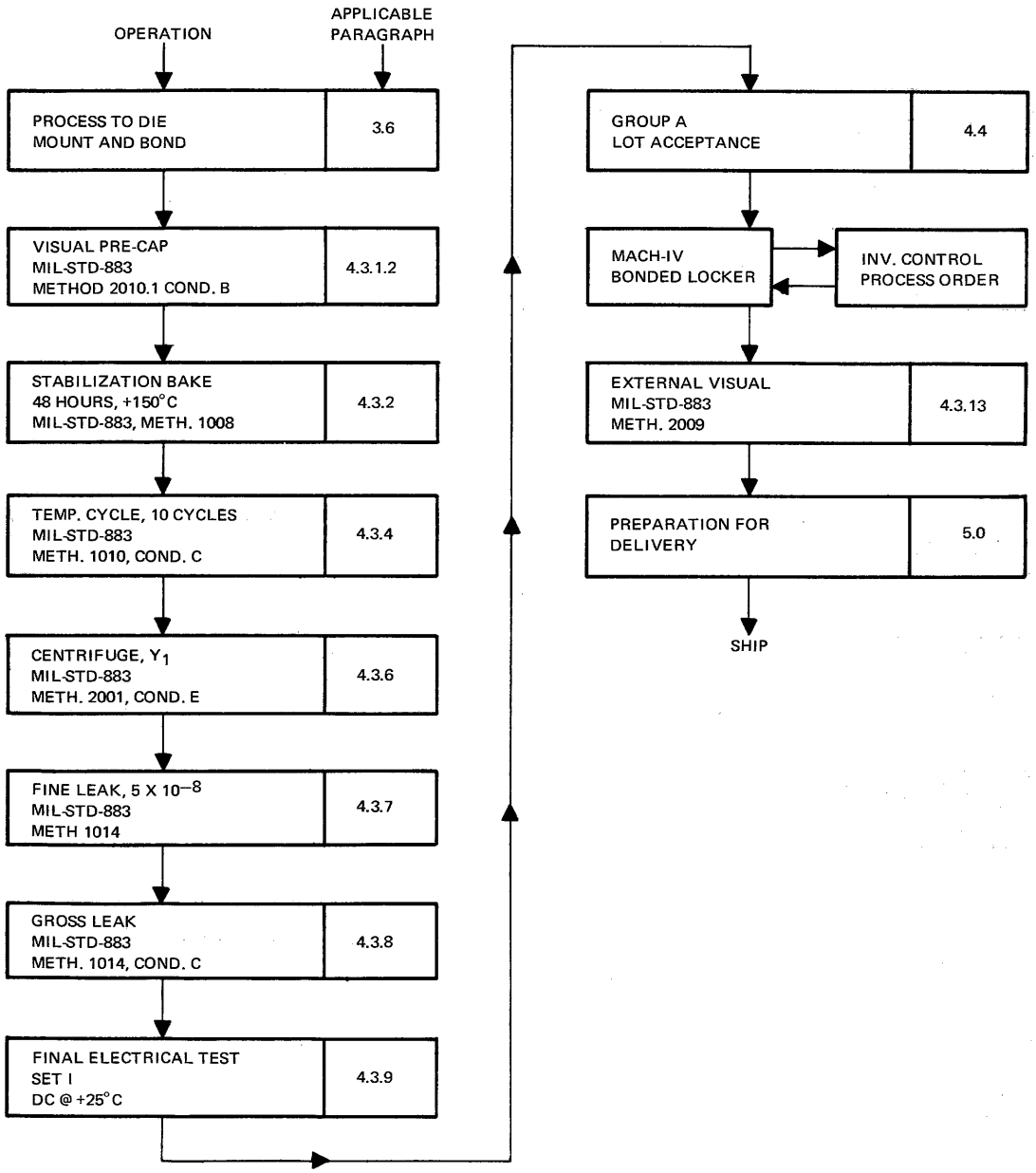


FIGURE 1

PROCESS FLOW CHART FOR LEVEL II (SNA)

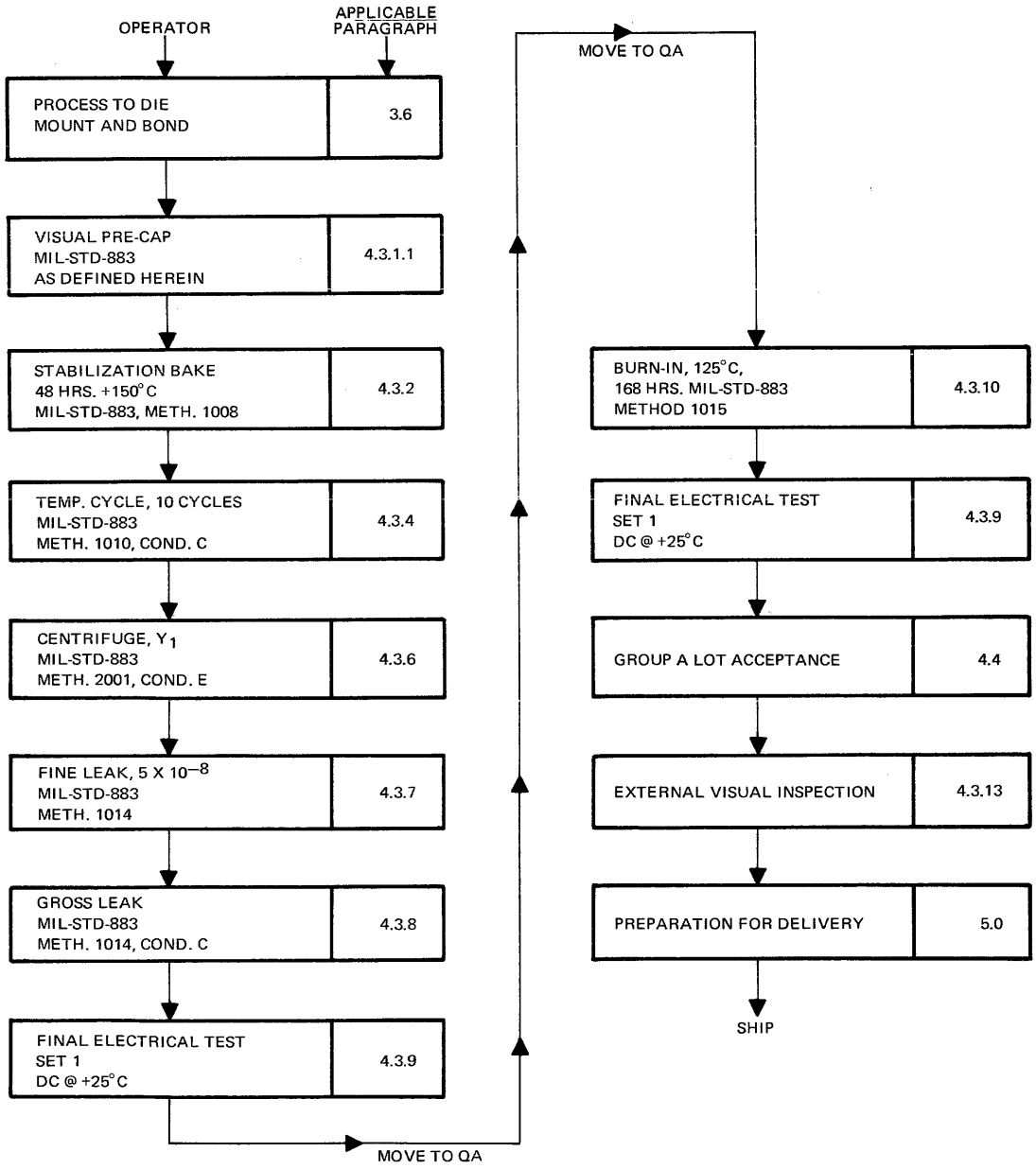


FIGURE 2

PROCESS FLOW CHART FOR LEVEL III (SNC)

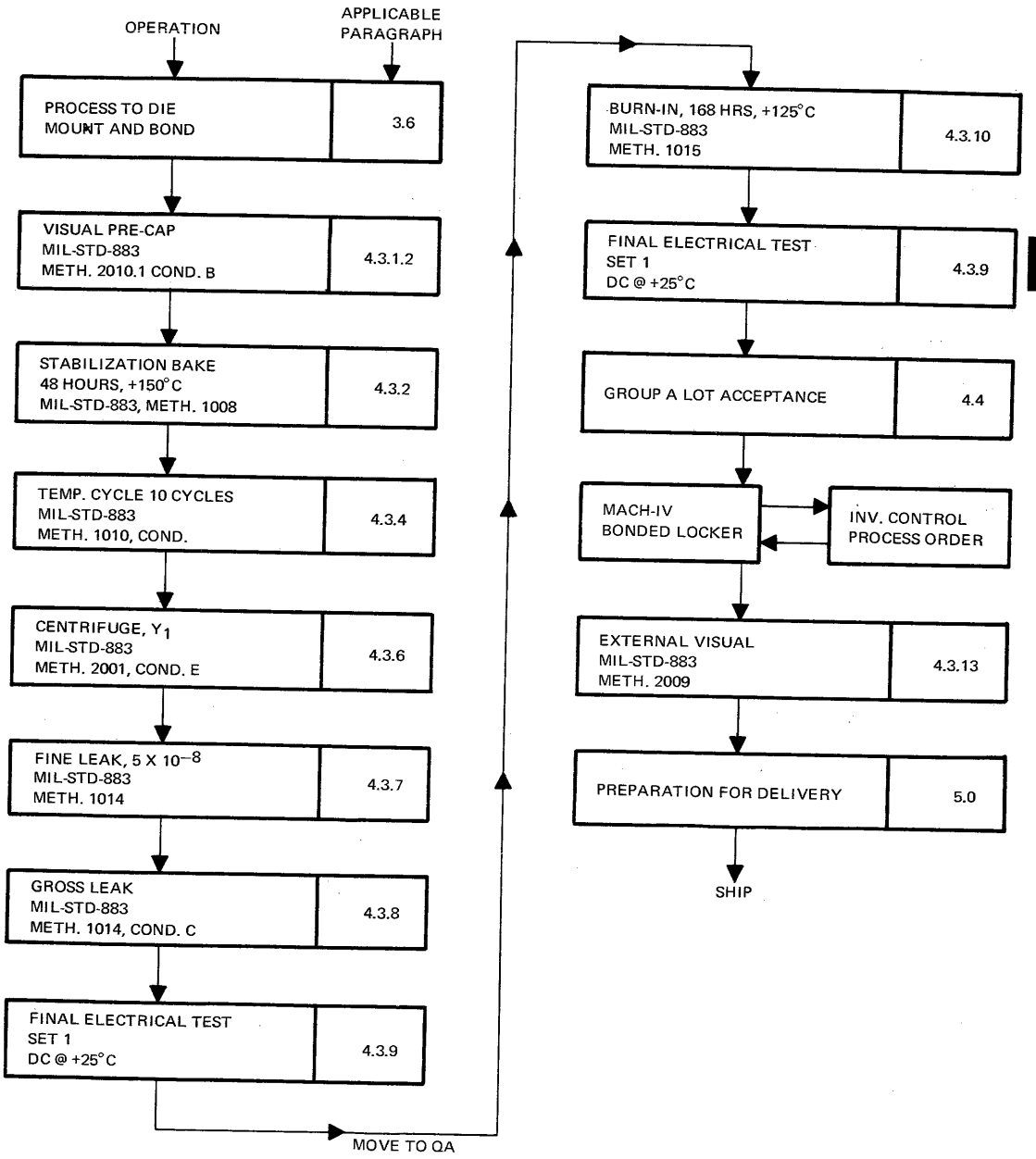


FIGURE 3

PROCESS FLOW CHART FOR LEVEL IV (SNH)

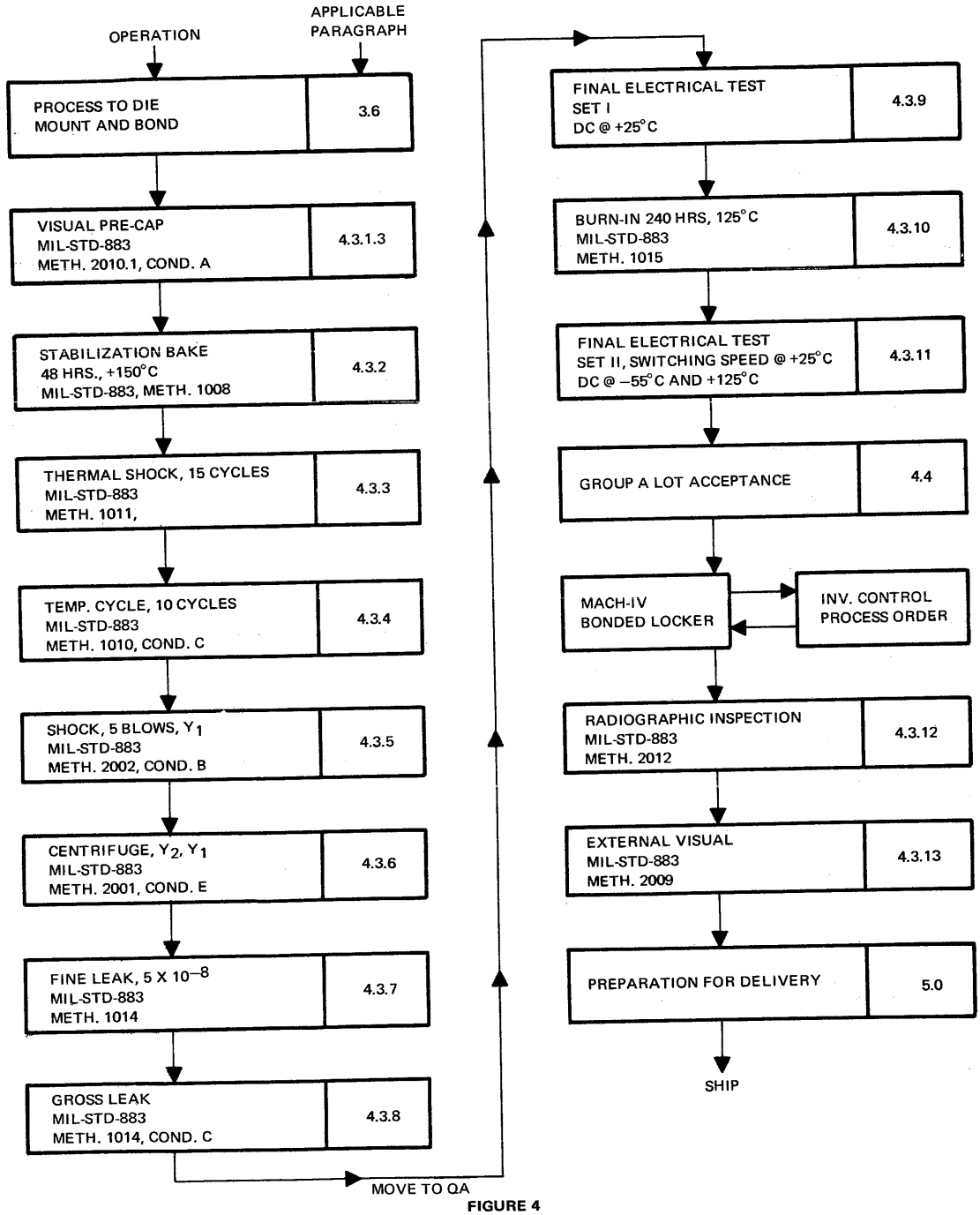


FIGURE 4

3.4.2.2 Foreign Materials

No lacquer, grease, paste, desiccant or other similar foreign encapsulant or coating material shall be included in the circuit enclosure nor applied to any part of the internal circuit assembly.

3.4.3 Mechanical

3.4.3.1 Case

Each integrated circuit shall be securely mounted and hermetically sealed within a case designed and constructed to conform to the outline and physical dimensions shown in the detailed specification. External surfaces of the integrated circuit case shall be unpainted except for markings.

3.4.3.2 Interconnections

Interconnections within the integrated circuit case shall be minimized and there shall be no wire crossovers. Circuit intraconnections by means of wire jumpers shall not be used. (See Note 6.2)

3.4.3.3 Leads

Lead material, construction, and outline shall be as specified on the detail specification and shall be capable of meeting the solderability test of MIL-STD-883, Method 20-3. (See Note 6.4).

3.4.3.3.1 Lead Size

Lead outline and dimensions shall be as specified in the detail specification.

3.4.3.3.2 Lead Surface Condition

Leads shall be free of the following defects over their entire length when inspected under a minimum of 4X magnification:

a) Foreign materials adhering to the leads such as paint, film, deposits and dust. Where adherence of such foreign materials is in question, leads may be subjected to a clean, contaminant-free (e.g., oil, dust, etc.), filtered air stream (suction or expulsion) or 88 feet per second maximum, or a wash/rinse as necessary and reinspected.

b) Nicks, cuts, scratches or other surface defacing defects which expose the base metal.

3.4.3.3.3 Lead Straightness

Leads shall be aligned within a 0.050-inch diameter, 0.050-inch length cylinder concentric to the point of lead emergence from the case and the X-axis (the axis parallel to the lead axis). Along the remaining lead length, there shall be no unspecified bend whose raduis is less than 0.10 inch and no twist whose angle is greater than 10° (ribbon leads, only).

3.4.3.3.4 Preformed Leads

Preformed leads, when specified, shall be in accordance with the detail specification. The part number of the integrated circuit shall remain as specified in the applicable detail specification or purchase order, the applicable suffix designation shall appear on the purchase order but shall not be marked on the device.

3.4.3.3.5 Carriers (Mech-Pak Carrier)

Carrier-matrix assemblies consisting of individually mounted integrated circuits shall be furnished when so specified by purchase order. The individual carrier shall have provisions for use with automatic test equipment contacts. Devices supplied "clipped-out" of the Mech-Pak Carrier shall be supplied in the Barnes Carrier type 029-188 or equivalent. (Applicable for Flat Packs only.)

3.5 Marking of Integrated Circuits

3.5.1 Legibility

All marking shall be permanent in nature and remain legible when subjected to specified operating, storage, and environmental requirements. All markings shall be insoluble in standard solvents such as trichlorethylene, water and xylene.

3.5.2 Marking Details

Marking of the integrated circuits shall be located as follows unless otherwise specified in the detail specification:

a) TO-100 (TO-5) and similar "can" cases shall be marked on the top of the case. Where space limitations exist, the side of the case may be used.

b) Flat Packs shall be marked on the top of the case. Where space limitation exists, the bottom of the package may be utilized as necessary. As a minimum the top of the package shall show the manufacturer's identification mark or symbol, the device part number, date code, and pin 1 orientation mark (where applicable).

c) Dual in-line plug-in packages shall be marked in the same manner as flat packs.

3.5.3 Required Device Marking

a) Index point indicating the starting point for numbering of leads shall be as indicated in the detail specification. The indexing point may be a tab, color dot, or other suitable indicator.

b) Manufacturer's identification mark or symbol.

c) A four or five digit alpha-numeric lot date code indicating the week of initial Group A acceptance. The date code shall be as follows:

1) EIA four digit date code, the first two numbers shall be the last two digits of the year, the last two numbers shall indicate the calendar week.

2) A Gothic letter which identifies separate lots of the same device type processed within the same calendar week. (If no more than one lot is processed through Lot Acceptance in a given calendar week, the Gothic letter may be omitted).

d) Manufacturer's part number.

e) Individual device serial number (if required)

f) A dot to indicate acceptance to Radiographic inspection

NOTE:

When a color dot is used to identify pin one, the radiographic inspection acceptance dot shall be placed on the bottom of the package.

3.6 Product Assurance

The manufacturer shall establish and maintain a reliability assurance program that complies with the basic intent of MIL-STD-790. Furthermore, it is intended that each integrated circuit delivered shall be free of any defect in design, material, manufacturing process, testing and handling, which would degrade or otherwise limit its performance when used within the specified limits.

3.6.1 Visual and Mechanical Examination

Integrated circuits shall be examined to verify that material, design, construction, physical dimensions, marking and workmanship are in accordance with the specified acceptance criteria.

3.6.2 Test Equipment

The manufacturer shall prepare and maintain a current list, by name and drawing number or other unique identification, of test equipment used in the manufacturing and testing of devices submitted for acceptance inspection under this specification. This list shall be made available to the procuring activity representative upon request.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

3.6.3 Process Control

Each integrated circuit shall be constructed by manufacturing processes which are under the surveillance of the manufacturer's Quality Control department. The processes shall be monitored and controlled by use of statistical techniques in accordance with published specifications and procedures. The manufacturer shall prepare and maintain suitable documentation (such as quality control manuals, inspection instructions, control charts, etc.) covering all phases of incoming part and material inspection and in-process inspections required to assure that product quality meets the requirements of this specification. The procuring activity may verify, with the permission of and in the company of the manufacturer's designated representative, that suitable documentation exists and is being applied. Information designated as proprietary by the manufacturer will be made available to the procuring activity or its representative only with the written permission of the manufacturer.

Process control is recognized as being vital to the concept of "built-in" quality. Appendix A defines an acceptable process-control system. Devices delivered to this specification shall be manufactured in a controlled system similar to that set forth in Appendix A.

3.6.4 Production Changes

The manufacturer shall advise the procuring activity of the time at which any major change(s) in production or QC methods or documentation become effective during the period of device production for delivery against any given purchase order referencing this specification.

3.7 Workmanship

Integrated circuits shall be manufactured and processed in a careful and workmanlike manner, in accordance with the production processes, workmanship instructions, inspection and test procedures, and training aids prepared by the manufacturer in fulfillment of the reliability assurance program established by paragraph 3.6.

3.7.1 Personnel Certification

The manufacturer shall be responsible for training, testing and certification of personnel involved in producing integrated circuits. Training shall be commensurate and consistent with the requirements of this specification and in conformance to the basic intent of MIL-STD-790. Training aids in the form of satifactory criteria shall be available for operator and inspector review at any time.

3.7.2 Personnel Evaluation

The supplier shall maintain a continuous evaluation of the proficiency of personnel concerned with production and inspection. Retraining of an operator or inspector shall be required when this evaluation establishes that a degree of proficiency necessary to meet the requirements of this specification is not being exercised.

3.7.3 Rework Provisions

3.7.3.1 Rework

All rework on microcircuits manufactured under this specification shall be accomplished in accordance with paragraph 3.7.1 of MIL-M-38510 except as defined herein.

3.7.3.2 Rebonding

Rebonding of integrated circuits shall be permitted with the following limitations:

a) No scratches, open or discontinuance metallization paths or conductor patterns shall be repaired by bridging with or addition of bonded wire or ribbon.

b) Rebonding at individual bonding pad locations shall be limited to a maximum of 3 rebonds for 14 pin devices, 4 rebonds for 16 pin devices, 7 rebonds for devices with more than 16 pins, and 2 rebonds for devices with less than 14 pins.

c) Rebonding shall be limited to not more than one rebond attempt at any single bond pad location.

d) Rebonding shall be limited to level I, II and III devices only. Rebonding of level IV (class A type) devices shall not be permitted.

3.8 Performance Capabilities

The integrated circuits delivered to this specification shall be designed to be capable of meeting the environmental requirements specified in Table II. The manufacturer need not perform these tests specifically for the contract or specification, but shall provide data which demonstrates the ability of the integrated circuits to pass the environmental tests. The data shall have been generated on devices from the same generic family as the circuits being supplied to this specification, and the package configuration shall be the same as for the delivered parts. (i.e., Flat Pack, TO-100, etc.).

3.9 Quality and Reliability Assurance Program Plan

The manufacturer shall establish and implement a Quality and Reliability Assurance Program Plan that meets the intent of MIL-M-38510, Appendix A. Submission of the program plan to the procuring activity shall not be a requirement of this specification; however, the program plan shall be maintained by the manufacturer and shall be available for review by the procuring activity.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for Inspection

Unless otherwise specified in the contract or purchase order, the manufacturer is responsible for the performance of all inspection requirements specified herein. Except as otherwise specified, the manufacturer may utilize his own facilities or any commercial laboratory acceptable to the procuring activity. The procuring activity may, at its discretion, perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements.

4.1.2 Inspection at Point of Delivery

The procuring activity may, at its discretion, reinspect any or all of the delivered parts. (Excluding Group B destructive samples as defined by MIL-STD-883). All parts found to be defective and/or lacking specified documentation (such as test documentation) may be returned to the manufacturer at the manufacturer's expense.

4.1.3 Inspection Records

The manufacturer shall maintain a reliability data and records library. This library shall have on file, for review by the procuring activity, records of examination, qualification test results, variables data (when required) and all other pertinent data generated on devices manufactured to this specification.

4.1.4 Control of Procurement Sources

The manufacturer shall be responsible for assuring that all supplies and services conform to this specification, the detail specification and the manufacturer's procurement requirements.

4.1.4.1 Manufacturer's Receiving Inspection

Purchased supplies shall be subjected to inspection after receipt as necessary to assure conformance to contract requirements. In selecting sampling plans, consideration shall be given to the controls exercised by the procurement source and evidence of sustained quality conformance.

4.1.4.2 The manufacturer shall provide procedures for withholding from use all incoming supplies pending completion of required tests or receipt of necessary certification or test records and their evaluation.

4.1.4.3 The manufacturer shall initiate corrective action with the procurement source depending upon the nature and frequency of receipt of nonconforming supplies.

4.1.5 Procuring Activity Quality Assurance Representative

The procuring activity, may, at its discretion, place quality assurance representatives in the manufacturer's plant as deemed necessary to assure conformance to contract requirements in any non-proprietary phase of design, fabrication, processing, inspection, testing, and reliability of the integrated circuits being produced. The manufacturer shall provide reasonable facilities and assistance for the safety and convenience of such personnel in the performance of their duties. Inspection and test procedures shall be made available for review by the quality assurance representative.

4.2 Qualification and Quality Conformance Inspection

4.2.1 Qualification

Manufacturer's qualification shall be based on compliance with the established reliability test program requirements of paragraph 4.2.1.1 herein. The manufacturer may, at his discretion, substitute the qualification test plan of paragraph 4.2.1.2 in order to establish initial qualification. However, the substitution of parapraph 4.2.1.2 does not relieve the manufacturer from the responsibility of establishing an in-house reliability evaluation program as defined by paragraph 4.2.1.1.

4.2.1.1 Established Reliability Test Program

The manufacturer shall have an established and well defined in-house reliability program. This program shall be so designed as to demonstrate that the manufacturer's product is capable of meeting, as a minimum, the environmental and minimum life requirements listed in Table I herein. The reliability program may be modeled after the test procedure of Table I or it may take the form of a step-stress testing program similar to that defined by MIL-STD-883, Method T5006. The program shall be on-going in nature; that is, at specified intervals the manufacturer shall randomly select product that is representative of current production techniques, and subject the devices to the specified tests. Sampling shall be done on each generic family.

4.2.1.2 Qualification Test Program

In lieu of meeting the requirements of 4.2.1.1, the manufacturer may establish qualification by performing an initial, one-time qualification test in accordance with Table I herein. Qualification testing shall be performed on each generic family supplied to this specification. Upon successful completion of the qualification program, the manufacturer shall remain qualified for a period not to exceed 12 calendar months. Continued qualification shall then be based on compliance with the requirements of paragraph 4.2.1.1.

4.2.1.3.1 Procedures and Definitions

4.2.1.3.1 Sampling Procedure

Device selection for the qualification procedure of 4.2.1.1 or 4.2.1.2 shall be based on a random sampling technique. Testing shall be done on a mixture of device types that adequately represent the entire generic family. The following is a recommended mix ratio:

Gates	:	65% of total sample
Flip-Flops	:	25% of total sample
MSI	:	10% of total sample

4.2.1.3.2 Generic Family

Electrically and structurally similar devices shall be said to comprise a generic family (e.g., TTL) if they meet the following criteria:

a) Are designed with the same basic circuit-element configuration such as TTL, DTL, ECL, or Linear, and differ only in the number or complexity of specified circuits which they contain.

b) Are designed for the same supply, bias and signal voltage, and for input/output capability with each other under an established set of loading rules.

c) Are enclosed in housing (packages) of the same basic construction (e.g., hermetically sealed flat packages, dual-in-line cermaic, dual-in-line plastic) and outline, differing only in the number of active housing terminals included and/or utilized.

4.2.2 Quality Conformance Inspection (Lot Inspection)

When specifically called out on the purchase order or contract, the manufacturer shall perform the lot qualification inspections, Group B and/or Group C in Table II.

4.2.2.1 Lot Acceptance Sampling

Statistical sampling for Group B and/or Group C lot acceptance inspections shall be in accordance with MIL-M-38510 Table B-1.

Group B samples shall be selected from sub-lots that have successfully completed all of the 100% processing steps, up to and including Group A Lot Acceptance, specified on the applicable process flow chart.

4.2.2.2 Resubmission/Failed Lots

Where a lot fails any one of the sub-group qualification requirements of Table II, it may be resubmitted a maximum of one time for qualification to that particular sub-group provided an analysis is performed to determine the failure mechanism for each reject device in the sub-group, and that it is determined that the failures are due to one of the following:

a) Testing error resulting in electrical damage to devices,

b) A defect that can effectively be removed by rescreening the lot,

c) Random defects which do not reflect poor basic device designs or poor workmanship.

4.2.2.3 Early Shipments

When lot qualification inspection is being performed for a specific contract or purchase order, the accepted Group A devices that are awaiting shipment pending successful completion of Group B and/or Group C, shall be stored in the MACH IV bonded locker. Under no circumstances shall such parts be shipped prior to the successful completion of the Group B tests.

4.2.2.4 Group B Test Data

All data generated by Group B and/or Group C testing shall accompany the initial shipment of devices. This data shall consist, at a minimum, of the following:

a) Attributes data for Group B. Endpoints for the subgroups are visual per the applicable MIL-STD-883 test method.

b) Variables data for Group C subgroups 1, 2, 4, and 5. Endpoints for these subgroups shall be "critical eletrical parameters" only. These parameters are designated by an asterisk (*) on the detail specification.

4.2.2.5 Procedure In Case Of Test Equipment Failure Or Operator Error

Where an integrated circuit is believed to have failed as a result of faulty test equipment or operator error, the failure shall be entered in the test record which shall be retained for review along with a complete explanation verifying why the failure is believed to be invalid. If it is determined that the failure is invalid, a replacement integrated circuit from the same inspection lot may be added to the sample. The replacement integrated circuit shall be subjected to all those tests to which the discarded integrated circuit was submitted prior to its failure, and any remaining specified test to which the discarded integrated circuit was not subjected prior to its failure.

4.3 Quality Assurance Processing, Methods and Procedures

This section establishes the test methods and conditions to be used for the 100% processing (screening) requirements specified by the applicable process flow chart.

4.3.1 Precap Visual Inspection

Each microcircuit shall be required to pass the appropriate precap visual inspection defined as follows. Precap Lot Acceptance shall be per paragraph 4.6.

4.3.1.1 Level II devices shall be visually inspected in accordance with the criteria listed in Section 6.1.3 of this specification. Inspection procedures and equipment requirements shall be as defined in MIL-STD-883.

4.3.1.2 Level I and III devices shall be visually inspected in accordance with MIL-STD-883, Method 2010.1, Condition B as defined by Revision Notice 2 dated November 20, 1969. (See Note 6.1.2.)

4.3.1.3 Level IV devices (designated for NASA type applications) shall be visually inspected in accordance with MIL-STD-883, Method 2010.1, Condition A as defined by Revision Notice 2 dated November 20, 1969. (See Note 6.1.1.)

4.3.2 Stabilization Bake

The purpose of this test is to determine the effect on microelectronic devices of baking at elevated temperatures without electrical stress applied. Test shall be performed in accordance with MIL-STD-883, Method 1008, Condition C.

4.3.3 Thermal Shock

The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in temperature. Test shall be performed in accordance with MIL-STD-883, Method 1011, Condition A.

4.3.4 Temperature Cycle

This test is conducted for the purpose of determining the resistance of a part to exposures at extremes of high and low temperatures, and to the effect of alternate exposures to these extremes, such as would be experienced when equipment or parts are transferred to and from heated shelters in arctic areas. Test shall be performed in accordance with MIL-STD-883, Method 1010, Condition C, minimum of 10 cycles.

4.3.5 Mechanical Shock

The shock test is intended to determine the suitability of the devices for use in electronic equipment which may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Test shall be performed in accordance with MIL-STD-883, Method 2002, Condition B, five blows minimum.

4.3.6 Centrifuge

The centrifuge test is used to determine the effects on microelectronic devices of a centrifugal force. This test is designed to indicate structural and mechanical weaknesses not necessarily detected in shock and vibration tests. Test shall be performed in accordance with MIL-STD-883, Method 2001, Condition E.

4.3.7 Fine Leak Test

Each integrated circuit shall be subject to a fine leak test in accordance with paragraph 4.3.7.1 or 4.3.7.2. The method shall be optional providing it is consistent with and capable of detecting the specified leak rate of the applicable process flow chart.

4.3.7.1 Helium Leak Test

Helium leak test shall be performed in accordance with MIL-STD-883, Method 1014, Condition A. Helium bomb pressure shall be 30 psig maximum, bomb time shall be 4 hours minimum.

4.3.7.2 Radiflo Leak Test

Radiflo leak test shall be performed in accordance with MIL-STD-883, Method 1014, Condition B. Krypton 85 bomb pressure and dwell time are a function of the radioactivity level and shall be selected so as to conform to the equations given in Condition B.

4.3.8 Gross Leak Test

Each integrated circuit shall be subjected to the appropriate gross-leak test of paragraphs 4.3.8.1 or 4.3.8.2. The manufacturer may, at his option, perform gross-leak testing after the Set I Final Electrical Tests of paragraph 4.3.9.

4.3.8.1 Glass to metal hermetic flat packs shall be tested in accordance with MIL-STD-883, Method 1014, Condition C, Step 2. Units will be bombed 4 hours minimum at 30 psi in FC-78. Units will then be immersed in FC-40 at +125°C ±5°C for 20 seconds minimum and observed for one large bubble or a continuous stream of small bubbles.

4.3.8.2 Glass to glass (ceramic) hermetic package shall be tested in accordance with MIL-STD-883, Method 1014, Condition C, Step 1.

4.3.9 Final Electrical Test (Set I)

Each integrated circuit shall be required to pass the electrical requirements of Subgroup 1 of the detail specification (DC @ +25°C). The manufacturer shall also perform such additional testing necessary to assure the parts will meet the temperature extreme limits.

4.3.10 Burn-In

2

The burn-in screen is performed for the purpose of eliminating marginal devices, those and early life failures evidenced as time and stress dependent. Test shall be in accordance with MIL-STD-883, Method 1015, Condition D or E at 125 ± 5°C for 168 hours minimum. The bias shall be removed from the devices prior to their return to 25°C. (See Note 6.3)

4.3.11 Final Electrical Test (Set II)

Each integrated circuit shall be required to pass the electrical requirements of the detail specifications. The following tests shall be performed as a minimum: d-c at maximum and minimum rated temperatures, and switching parameters at 25°C.

The manufacturer may, when deemed necessary, elect to perform additional electrical testing over and above the requirements stated herein.

4.3.12 Radiographic Inspection (X-ray)

Test shall be performed in accordance with MIL-STD-883, Method 2012. The integrated circuit shall be required to pass a radiographic inspection to these requirements. In addition, the acceptance criteria shall meet, as a minimum, the requirements of NASA MSFC specification MSFC-STD-355.

4.3.13 External Visual Inspection

The purpose of this examination is to verify that materials, construction, marking, and general workmanship are as specified. Examination shall be in accordance with MIL-STD-883, Method 2009.

4.4 Group A Lot Acceptance

Each lot of integrated circuits shall be sampled by Quality Control to the LTPD's given below:

GROUP A ACCEPTANCE

SUBGROUP	LTPD LEVEL I & II	LTPD LEVEL III & IV
Subgroup 1 25°C, d-c	7%	5%
Subgroup 2 +125°C, d-c	7%	5%
Subgroup 3 −55°C, d-c	7%	5%
Subgroup 4 Switching Speed @ +25°C	15%	10%

NOTE: Functional tests included in d-c tests.

TABLE I
MANUFACTURERS QUALIFICATION PROCEDURE

TEST	MIL-STD-883 METHOD	CONDITIONS	LTPD
Subgroup 1			
Physical Dimensions Visual and Mechanical	2008	Condition A & B	15
Subgroup 2†			
Solderability	2003		15
Subgroup 3†			
Thermal Shock	1011	Condition B	
Temperature Cycling	1010	Condition C	
Moisture Resistance	1004	Omit step 7B and Initial Conditioning	
Critical Electrical Parameters	5004	25°C, DC	15
Subgroup 4‡			
Mechanical Shock	2002	Condition B	
Vibration Variable Freq.	2007	Condition A	
Constant Acceleration	2001	Condition E	
Critical Electrical Parameters	5004	25°, DC	15
Subgroup 5†			
Lead Fatigue	2004	Condition B2	
Fine Leak	1014	Condition A, Per Para. 4.3.7 Herein	
Gross Leak	1014	Condition C, Per Para. 4.3.7 Herein	15
Subgroup 6†			
Salt Atmosphere	1009	Condition A, Omit Initial Conditioning	15
Subgroup 7‡			
Storage Life	1008	150°C, 1000 Hrs. Minimum	
Critical Electrical Parameters	5004	25°C, DC	10
Subgroup 8‡			
Operating Life	1005	125°C, 1000 Hrs. Minimum Return to 25°C without bias	
Critical Electrical Parameters	5004	25°C, DC	10
Subgroup 9†			
Bond Strength			10 devices not
a. Thermocompressions	2011	Condition B, D	greater than 1%
b. Ultrasonic	2011	Condition B, D	defective

†Visual and/or hermetic end points hence electrical or visual rejects may be used. Reference MIL-STD-883. Method 5005, Para. 3.4.

‡Electrical end points only.

TABLE II
LOT ACCEPTANCE/PERIODIC QUALIFICATION TEST
(GROUP B/GROUP C)

GROUP B

TEST	MIL-STD-883 METHOD	CONDITIONS	LTPD LEVEL I & II	LTPD LEVEL III & IV
Subgroup 1				
Physical Dimensions Visual and Mechanical	2008	Condition A	15	10
Subgroup 2				
Marking Permanency	2008	Condition B, para. 3.2.1		
Visual and Mechanical	2008	Condition B per applicable detail specification		
Bond Strength	2011	Condition B or D 2 grams for Au bonds 1 gram for Al bonds	15	5
Subgroup 3†				
Solderability	2003		15	10
Subgroup 4†				
Lead Fatigue	2004	Conditions B2		
Fine Leak	1014	Condition A, per para. 4.3.7 of this spec.		
Gross Leak	1014	Condition C, per para. 4.3.8 of this spec.	15	10

GROUP C

Subgroup 1‡				
Thermal Shock	1011	Condition B		
Temp. Cycle	1010	Condition C		
Moisture Resistance	1004	Omit Initial Cond. & step 7B		
Critical Electrical Parameters	5004	25°C, DC	15	10
Subgroup 2‡				
Mechanical Shock	2002	Condition B		
Vibration Variable Freq.	2007	Condition A		
Constant Acceleration	2001	Condition E		
Critical Electrical Parameters	5004	25°C, DC	15	10
Subgroup 3				
Salt Atmosphere	1009	Condition A Omit Initial Conditioning	15	10
Subgroup 4‡				
High Temp. Storage	1008	150°C, 1000 Hrs.		
Critical Electrical Parameters	5004	25°C, DC	10	7
Subgroup 5‡				
Operating Life Test	1005	125°C, 1000 Hrs. Minimum		
Critical Electrical Parameters		25°C, DC	10	7

†Visual and/or hermetic end points hence electrical or visual rejects may be used. Reference MIL-STD-883. Method 5005, Para. 3.4.

‡Electrical end points only.

4.5 Certification

The manufacturer shall include a certificate of compliance with each shipment of parts. This certificate shall indicate that all specified tests and requirements of this specification have been made or met, and that the lot of devices (identified by lot and/or batch number) are acceptable. The certificate shall bear the name and signature of the manufacturer's Quality Control representative, the date of acceptance or signing, and any pertinent notes as applicable.

4.6 Precap Lot Acceptance

After each precap inspection the lot of devices shall be sampled by quality control and inspected for the specified visual criteria. The sampling plan shall be:

40X criteria – 1.0% AQL
100X criteria – 1.0% AQL

5.0 PREPARATION FOR DELIVERY

5.1 Final Visual Shipping Inspection

Each lot of microcircuits and its associated documentation shall be sampled by Quality Control and visually inspected for the following:

a) Scratched, nicked or bent leads
b) Damaged header (packages)
c) All test data specified in section 4.0
d) Certificate of Compliance as specified in section 4.0
e) All other pertinent documentation required and specified by this specification.

5.2 Packing Requirements

Parts shall be packed in containers of the type, size, and kind commonly used which will ensure acceptance by common carriers and safe delivery at the destination and in accordance with MIL-M-55565, Level C. The containers shall be clearly marked with manufacturer's name or symbol. The manufacturer's FEDERAL SUPPLY CODE FOR MANUFACTURER (FSCM) shall be included if applicable.

5.3 Preservation and Package Identification

The package shall be marked with the following:

The country of origin if other and U.S.A.
Procuring activity parts number
Purchase order number
Material nomenclature
Quantity
Lot number
Date code

This information shall appear on the label or shall be directly marked on each container. Method is optional.

6.0 NOTES

6.1 Precap Visual Method 2010.1

The following precap criteria may be in conflict with the circuit design topology and construction techniques of some microcircuit manufacturers. Where such a conflict does exist, the inspection criteria listed herein may be waived. (Reference paragraph 3.0 of MIL-STD-883, Method 2010.1)

6.1.1 Preseal Visual Inspection, Test Condition A (Level IV)

6.1.1.1 Paragraph 3.1.6.3 is clarified as follows:

When the criteria of 3.1.6.3(b) is in conflict with 3.1.6.3(a), the criteria of 3.1.6.3(a) shall take precedence. (Note: This clarification is with respect to die symmetry only.)

6.1.1.2 Paragraphs 3.1.1.1(a) and 3.1.1.2(a) are clarified as follows:

"Any scratch or void in the metallization that leaves less than 50 (75) percent of the original metal width undisturbed" shall be rejected. When a bi-metallization system is used (e.g. Moly-Gold) the scratch or void must penetrate entirely through the gold and expose moly or oxide.

6.1.1.3 Paragraph 3.1.4.3(c) delete: (Applicable to gold ball bonds only) "Bonds in the fillet area (or the point where metallizations exits from the bonding pad) which reduces the major distance between the bond periphery and edge of fillet to less than 50 percent of the narrowest normal width of the interconnecting metallization."

6.1.2 Preseal Visual Inspection, Test Condition B (Levels I & III)

2

6.1.2.1 Paragraph 3.2.1.7(a) delete the 40 percent perimeter requirement. (Selected devices only)

6.1.2.2 Paragraph 3.2.4.3(a) substitute the following criteria: "Bonds placed so that the wire exiting from the bond appears to come closer than two wire diameters to another wire, bonding pad, or package land, after a distance of 10 mils from the die surface.

6.1.2.3 Paragraph 3.2.4.3(c) delete. "Bonds in the fillet area (or the point where metallizations exits from the bonding pad) which do not exhibit a line of undisturbed metallization visible between the periphery of the bond and at least one side of the fillet (or one side of the connecting stripe) when viewed from above."

6.1.3 Preseal Visual Inspection, Test Condition B (Level II)

The same comments of 6.1.2 are applicable here plus the following:

6.1.3.1 Paragraph 3.2.1.1(a) change to read as follows: "Scrathces or voids in metallization exposing oxide for more than 50 percent of the lead width or alternately, a scratch or void greater than 0.5 mils in length exposing oxide."

6.1.3.2 Paragraph 3.2.1.1(b) change to read as follows:

"Any scratch in the metallization over an oxide step which leaves less than 50 percent of the original metal width undisturbed."

6.1.3.3 Paragraph 3.2.1.2(b) change to read as follows:

"Any void in the metallization over an oxide step which leaves less than 50 percent of the remaining metal undisturbed."

6.1.3.4 Paragraph 3.2.3(d) delete.

"Any crack which exceeds 1.0 mil in length inside the scribe grid or scribe line that points toward active metallization or circuit area."

6.1.3.5 Paragraph 3.2.6.1(b) change to read as follows:

"Attached gold or silicon material that appears to bridge any two unpassivated metallization areas, two package leads, or any lead to package metallization."

6.2 Interconnections

Circuit intraconnections (metallization pattern) shall be designed so that no properly fabricated connection shall experience a current density greater than 5×10^5 amperes/cm2, including allowances for worst case conductor composition, normal production tolerances on design dimensions, and nominal thickness at critical areas such as contact windows.

6.3 Burn-in Method 1015

Condition D parallel excitation or Condition E ring oscillator burn-in circuits will be used. The requirement to return the device to 25°C room ambient temperature with bias still applied should be omitted. Indications are that for most saturated logic integrated circuits the high temperature bake after bias has been removed does not allow defective devices to recover and become good.

6.4 Salt Atmosphere Test, Method 1009.

Where package design consideration necessitate (such as .75" tip-to-tip metal flat packs), there may be a conformal coating applied prior to the salt atmosphere test.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

APPENDIX A

PROCESS CONTROL SYSTEM

INTEGRATED CIRCUITS PROCESS CONTROL

The integrated circuits industry has had over seven years experience in manufacturing and represents a high volume, mass production sector of electronics. We have overcome the usual new product growing pains and learned a great deal about process control systems from our experience. This article presents the philosophy and the basic elements of a process control system which has been found to be the most practical one for integrated circuits manufacturing. It should also be applicable to any semiconductor process which must produce devices for a high reliability market.

Integrated circuits were originally developed for the aerospace market and these are still the volume users. Hundreds of thousands of integrated circuits have already been delivered for use in Minuteman and Apollo alone. At the same time, the high volume commercial and consumer market for integrated circuits is developing very rapidly. Although most of the integrated circuits from a given manufacturer are built on a single production line, there are many different types and families: digital, linear, flip flops, choppers, gates, buffers, amplifiers, double epitaxial, monolithic, hybrids, TTL, DTL, ECL—hundreds of possibilities.

The key to success in today's integrated circuits business appears to be an efficient and effective process/product control system.

PRODUCT CONTROL VS. PROCESS CONTROL

Although it is not universally understood, *product* control is not the same as *process* control. They not only have different means, but their ends are entirely different. True, under the proper conditions, they can be interfaced and made more efficient, but let us first define the terminology.

PRODUCT CONTROL

Product control is the inspection and sorting of material (product) to cull unacceptable material from the acceptable. It is the age-old task of inspection, screening, detailing, or culling. With a state-of-the-art product such as integrated circuits, this inspection will usually take the form of go-no-go checking for various defects. The end result of product control is to eliminate from succeeding steps of the process that material which the preceding steps of the process have not constructed properly. The basic element of a product control system is where the inspection station is removing most of the product which was processed improperly by the preceding manufacturing operation.

It will be noted that this inspection has no control over the *process—only the product*. If the manufacturing operation should happen to start producing 100% bad product, the inspection station would remove this product, but would not correct the basic problem.

If the results of the inspection station, in the form of yield (or loss) data is monitored, analyzed, and compared to a standard set of circumstances, action can be taken to correct any degradation of the manufacturing operation. This feedback of information effects a degree of *process control* i.e., a control over the process which is not directly concerned with removing defective product.

The feedback of product control results for process control purposes helps achieve control over processes.

Product control in the manufacturing area is composed of:

1) Manufacturing Inspection
2) Quality Control Lot Acceptance Following Manufacturing Inspections.

1. Manufacturing Inspection

This inspection is performed by production personnel to go-no-go defect criteria. Even in this least severe level of product control, the closed loop feedback is utilized. The medium for this control is the product yield report and process control management system (PCMS), which has daily and weekly management, engineering, and quality control visibility.

Examples of these controls are diffusion, bar inspection, slice electrical probe, pre-encapsulation, hermetic seal, and electrical inspections performed in the manufacturing process.

2. Quality Control Lot Acceptance Following Manufacturing Inspection

In areas more critical in nature, the manufacturing inspection described in (1) is sometimes followed by Lot Acceptance. Here, decisions are made on lots of inspected product with regard to engineering specifications and predetermined quality levels.In this medium of control, feedback is two-fold: (1) Rejected lots are immediately identified for attention and manufacturing, engineering, and quality control are alerted as to whether process or inspection changes may have taken place, (2) PCMS shows trends of the quality control results and is distributed weekly to all levels of department management. Percentages are statistically compared to past averages and significant points are noted and corrective action implemented.

Examples of such control points are QC lot acceptance at epitaxial, bar inspection, pre-encapsulation, hermetic seal and electrical testing.

It should be pointed out that this "Product Control" concept is also an Inspection Control concept. The inspectors which are checked by a lot acceptance get instant feedback if the quality of their inspection degrades. Also, through the use of reject analysis and yield reporting, excessive losses are noted and thus both acceptable and rejectable material is monitored.

PROCESS CONTROL

Process control is the activity which controls the process itself and is not directly concerned with removing the defective product, but in preventing the manufacture of defective product which aids the subsequent product controls. It was noted previously that even in the case of pure *Product Control*, some process control can be effected by the proper use of feedback tools.

In integrated circuits manufacturing at Texas Instruments, *Process Control* is provided by the following:

1) Quality Control Surveillance Points During Manufacture
2) Engineering Evaluation of Manufacturing Process
3) Manufacturing Controls
4) Failure Analysis of Discrepant Devices

1. Quality Control Surveillance Points During Manufacture

Process Controls examines the manufacturing process to point out the problem areas. For example: If thirty operators are bonding, we inspect products from all thirty operators and point out the worst three bonders to the manufacturing supervisor daily. This concentrates the supervisor's effort on the quality problem operator each day. This type of control is called operator control.

A control where the worst machine or machines are pinpointed for corrective action by repair and maintenance personnel is called machine control. Examples of such controls are: $\bar{X}$–R chart control of diffusion furnaces, visual surveillance of product from each mounting operator, bond strength tests on bonded Integrated Circuits, hermetic seal checks on lid welders.

2. Engineering Evaluation of Manufacturing Process

Engineering maintains sample or pilot analysis at several critical points of manufacture. Here, electrical parameters are measured on a lot by lot basis to maintain control at that point. An example of this is the analysis performed in diffusion to control this portion of the manufacturing process.

3. Manufacturing Controls

Regular controls by manufacturing for operator performance, line balance, inventory control, and line comparison enhance the quality of the device.

4. **Failure Analysis of Discrepant Devices**

Another portion of the feedback loop is through the analysis of failed devices. Regular life testing with failure analysis of test failures is performed on representative device series. In addition, device failures from selected points in the process are given to the failure analysis lab on a routine basis. By this media, *Product* and *Process Controls* can be adjusted to correct mechanisms which might not be discovered until actual application of the devices.

An analysis of the complete QC process control system is shown in the attached flow charts. These charts describe the QC Process Control System and a brief description of each control point.

The PCMS is a computerized report of the control points on a weekly basis. These control points have their trends analyzed by comparing the current percentage to past averages and calculating significant differences. Points analyzed as significantly different are further detailed as to exact defect descriptions. These points are then analyzed and corrective action developed as necessary. This weekly analysis is circulated to all levels of department management. This reporting system plus the immediate feedback which occurs "on-line" provides an effective follow-up scheme.

It should be noted that the details of this system are flexible and not essential to the basic philosophy of a composite control system. As experience is gained in the various inspection areas and as process improvements are made, it will be found advantageous to suitably modify the system to keep pace with these changes. As time passes, sample sizes will be changed; inspection points will be added and deleted; defect criteria will be made less subjective, and new defect criteria will be added to the inspection procedure. But none of these affect the basic philosophy of the product/process control system.

ADVANTAGES OF THE SYSTEM

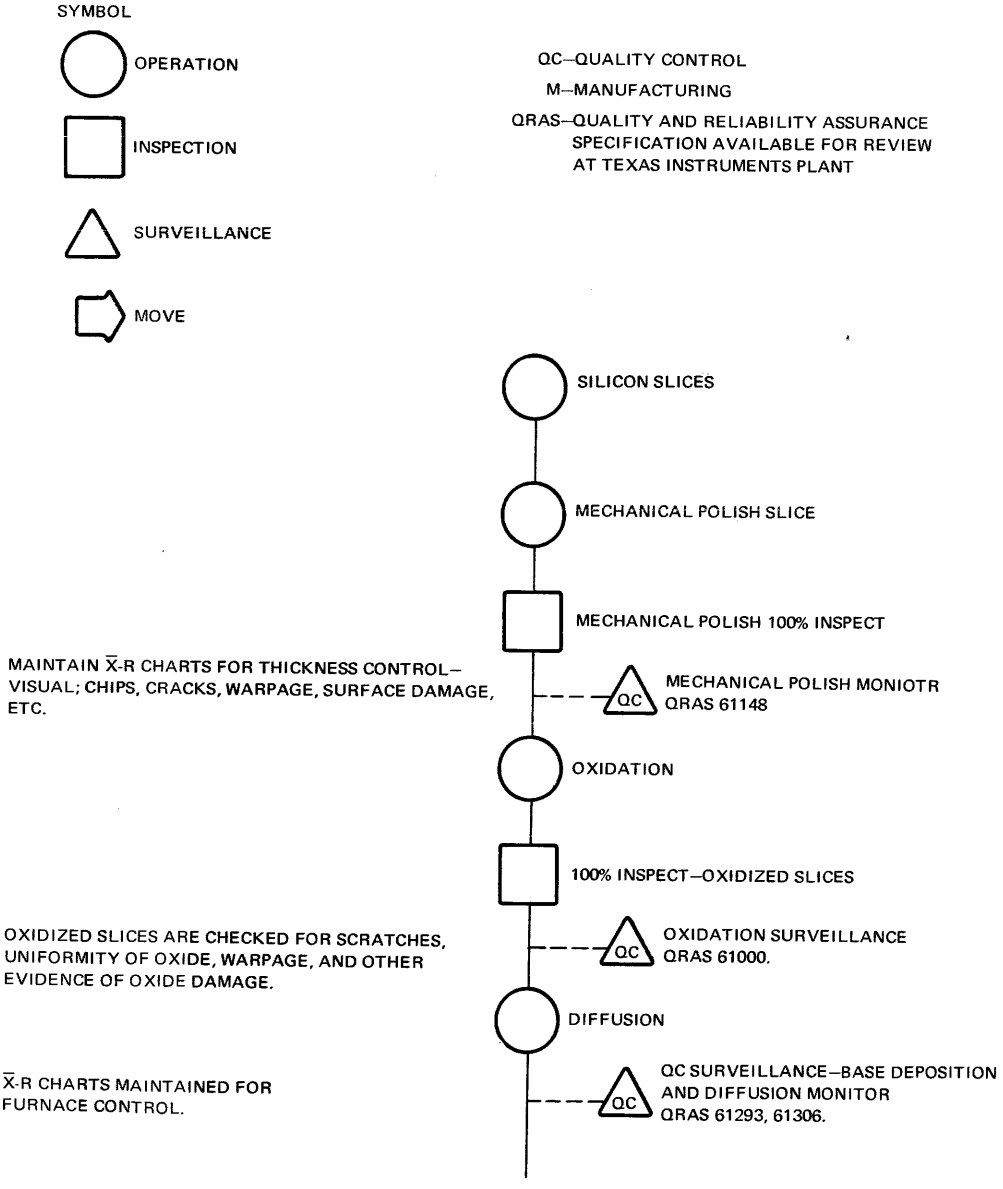
1) It is a flexible system easily adapted to changes brought about by technological improvements or by changes dictated by the system itself.
2) It is a cost optimized system in which the process or product can be stopped before unwarranted labor is expended. In addition, the system calls attention to the reason for defective product so that corrective action can be implemented.
3) The same general system can be utilized for different degrees of maturity of a product and for different degrees of criticality with regard to product requirements.
4) It combines the advantages of both the product and process control concepts.
5) There is maximum utilization of data by closing all the feedback loops with corrective action.

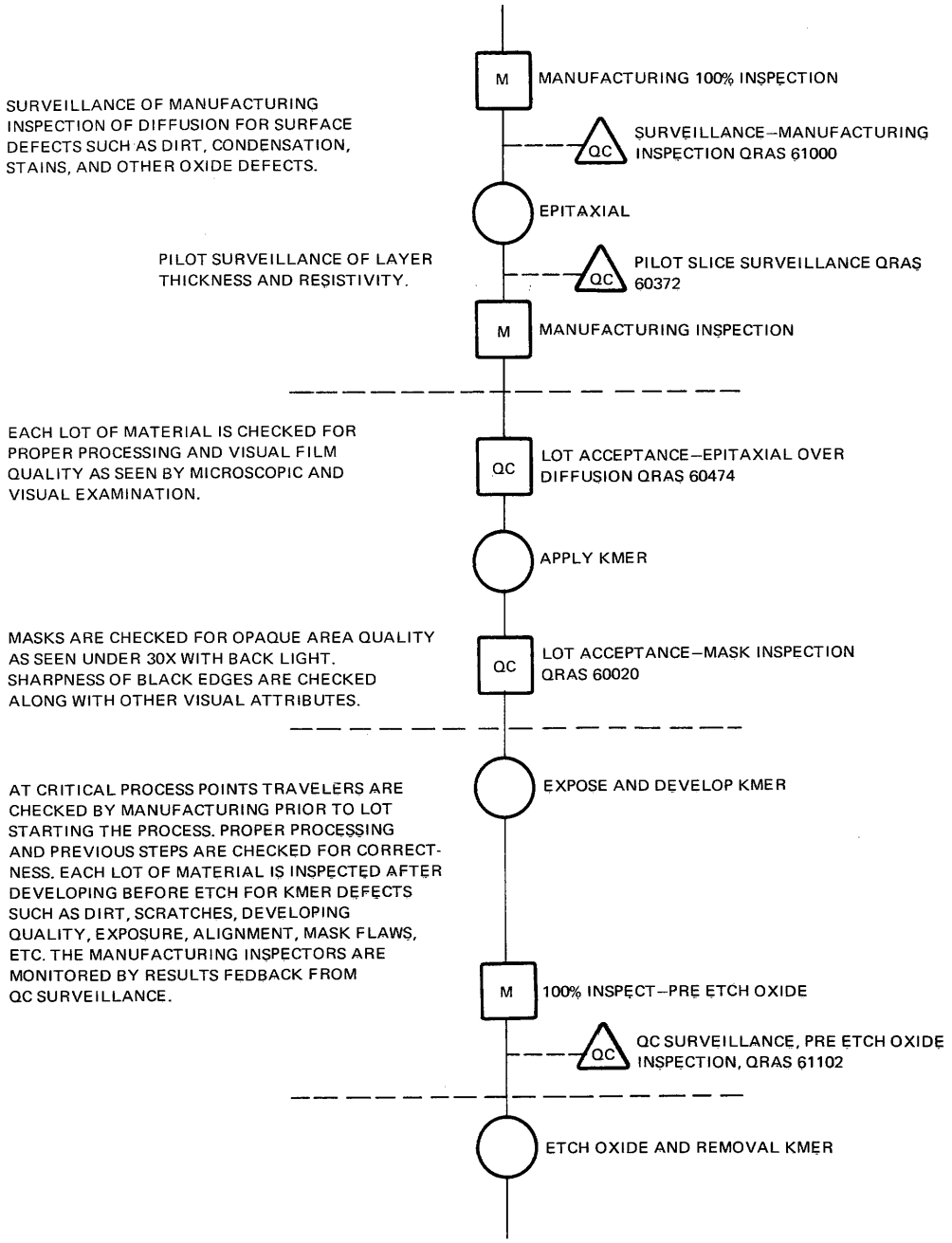
SUMMARY

Using the various elements described above to develop a composite control system for an integrated circuits process results in maximizing the efficiency of inspection and utilization of inspection data. In particular, the system offers a practical solution for interfacing these following features:

Product Control through 100% inspection and sorting.

Process Control through feedback of inspection data into the process.


SYMBOL
OPERATION
INSPECTION
SURVEILLANCE
MOVE
QC–QUALITY CONTROL
M–MANUFACTURING
QRAS–QUALITY AND RELIABILITY ASSURANCE SPECIFICATION AVAILABLE FOR REVIEW AT TEXAS INSTRUMENTS PLANT
SILICON SLICES
MECHANICAL POLISH SLICE
MECHANICAL POLISH 100% INSPECT
MAINTAIN X̄-R CHARTS FOR THICKNESS CONTROL–VISUAL; CHIPS, CRACKS, WARPAGE, SURFACE DAMAGE, ETC.
QC
MECHANICAL POLISH MONIOTR QRAS 61148
OXIDATION
100% INSPECT–OXIDIZED SLICES
OXIDIZED SLICES ARE CHECKED FOR SCRATCHES, UNIFORMITY OF OXIDE, WARPAGE, AND OTHER EVIDENCE OF OXIDE DAMAGE.
QC
OXIDATION SURVEILLANCE QRAS 61000.
DIFFUSION
X̄-R CHARTS MAINTAINED FOR FURNACE CONTROL.
QC
QC SURVEILLANCE–BASE DEPOSITION AND DIFFUSION MONITOR QRAS 61293, 61306.


M
MANUFACTURING 100% INSPECTION
SURVEILLANCE OF MANUFACTURING INSPECTION OF DIFFUSION FOR SURFACE DEFECTS SUCH AS DIRT, CONDENSATION, STAINS, AND OTHER OXIDE DEFECTS.
QC
SURVEILLANCE–MANUFACTURING INSPECTION QRAS 61000
EPITAXIAL
PILOT SURVEILLANCE OF LAYER THICKNESS AND RESISTIVITY.
QC
PILOT SLICE SURVEILLANCE QRAS 60372
M
MANUFACTURING INSPECTION
EACH LOT OF MATERIAL IS CHECKED FOR PROPER PROCESSING AND VISUAL FILM QUALITY AS SEEN BY MICROSCOPIC AND VISUAL EXAMINATION.
QC
LOT ACCEPTANCE–EPITAXIAL OVER DIFFUSION QRAS 60474
APPLY KMER
MASKS ARE CHECKED FOR OPAQUE AREA QUALITY AS SEEN UNDER 30X WITH BACK LIGHT. SHARPNESS OF BLACK EDGES ARE CHECKED ALONG WITH OTHER VISUAL ATTRIBUTES.
QC
LOT ACCEPTANCE–MASK INSPECTION QRAS 60020
EXPOSE AND DEVELOP KMER
AT CRITICAL PROCESS POINTS TRAVELERS ARE CHECKED BY MANUFACTURING PRIOR TO LOT STARTING THE PROCESS. PROPER PROCESSING AND PREVIOUS STEPS ARE CHECKED FOR CORRECTNESS. EACH LOT OF MATERIAL IS INSPECTED AFTER DEVELOPING BEFORE ETCH FOR KMER DEFECTS SUCH AS DIRT, SCRATCHES, DEVELOPING QUALITY, EXPOSURE, ALIGNMENT, MASK FLAWS, ETC. THE MANUFACTURING INSPECTORS ARE MONITORED BY RESULTS FEDBACK FROM QC SURVEILLANCE.
M
100% INSPECT–PRE ETCH OXIDE
QC
QC SURVEILLANCE, PRE ETCH OXIDE INSPECTION, QRAS 61102
ETCH OXIDE AND REMOVAL KMER

2

EACH LOT OF MATERIAL IS INSPECTED BY MANUFACTURING AFTER OXIDE REMOVAL FOR OXIDE DEFECTS SUCH AS UNDERCUT, ALIGNMENT, INCOMPLETE OXIDE REMOVAL, DIRT, ETC.

THE MANUFACTURING INSPECTORS ARE MONITORED BY RESULTS FEDBACK FROM THE QC SURVEILLANCE.

THIS CHECK IS A SURVEILLANCE OF TESTING EVAPORATION PILOT SLICES TO DETERMINE METAL THICKNESS. PILOTS ARE DOUBLE CHECKED TWICE PER WEEK PER SHIFT FROM EACH EVAPORATOR. THE TALYSURF (OR EQUIVALENT) WHICH MEASURES METAL FILM THICKNESS IS CHECKED FOR CALIBRATION ONCE PER SHIFT USING STANDARDS.

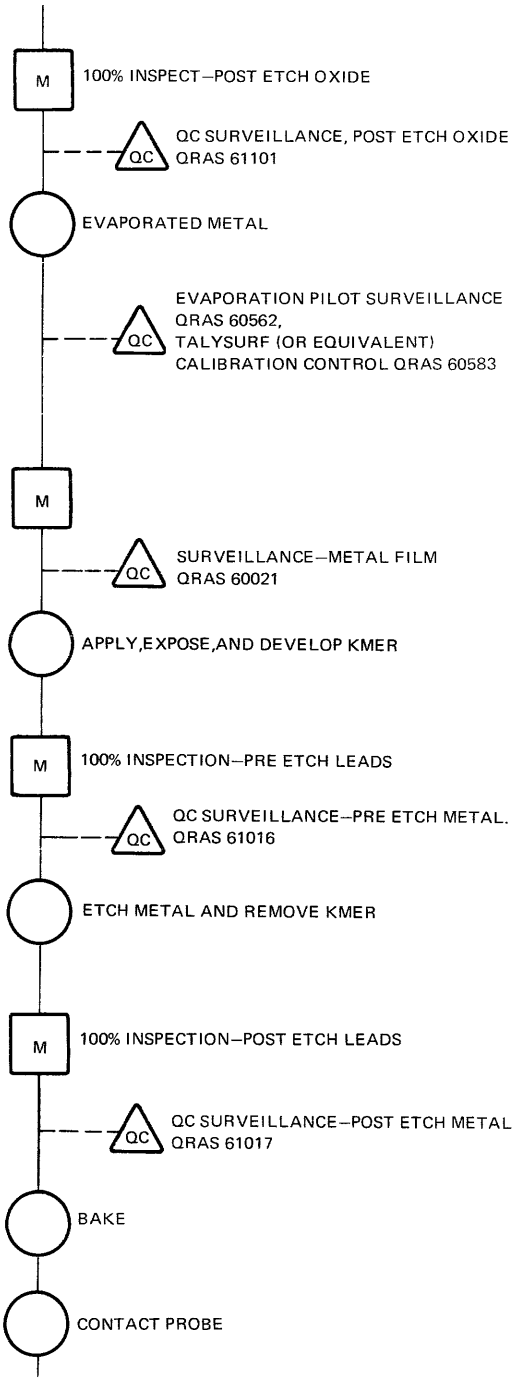
SAMPLES ARE PULLED ONCE PER EVAPORATOR PER SHIFT FOR EFFECTIVENESS OF MANUFACTURING 100% INSPECTION. DEFECTS SUCH AS CONTAMINATION, SPLATTERING, FOREIGN PARTICLES, ETC, ARE MONITORED

EACH LOT OF SLICES IS INSPECTED AT METAL ETCH FOR DEFECTS SUCH AS MISALIGNMENT, OVER AND UNDER EXPOSURE, WRONG PATTERN, RESIST PEELING, ETC. THIS KMER INSPECTION IS PERFORMED BY MANUFACTURING.

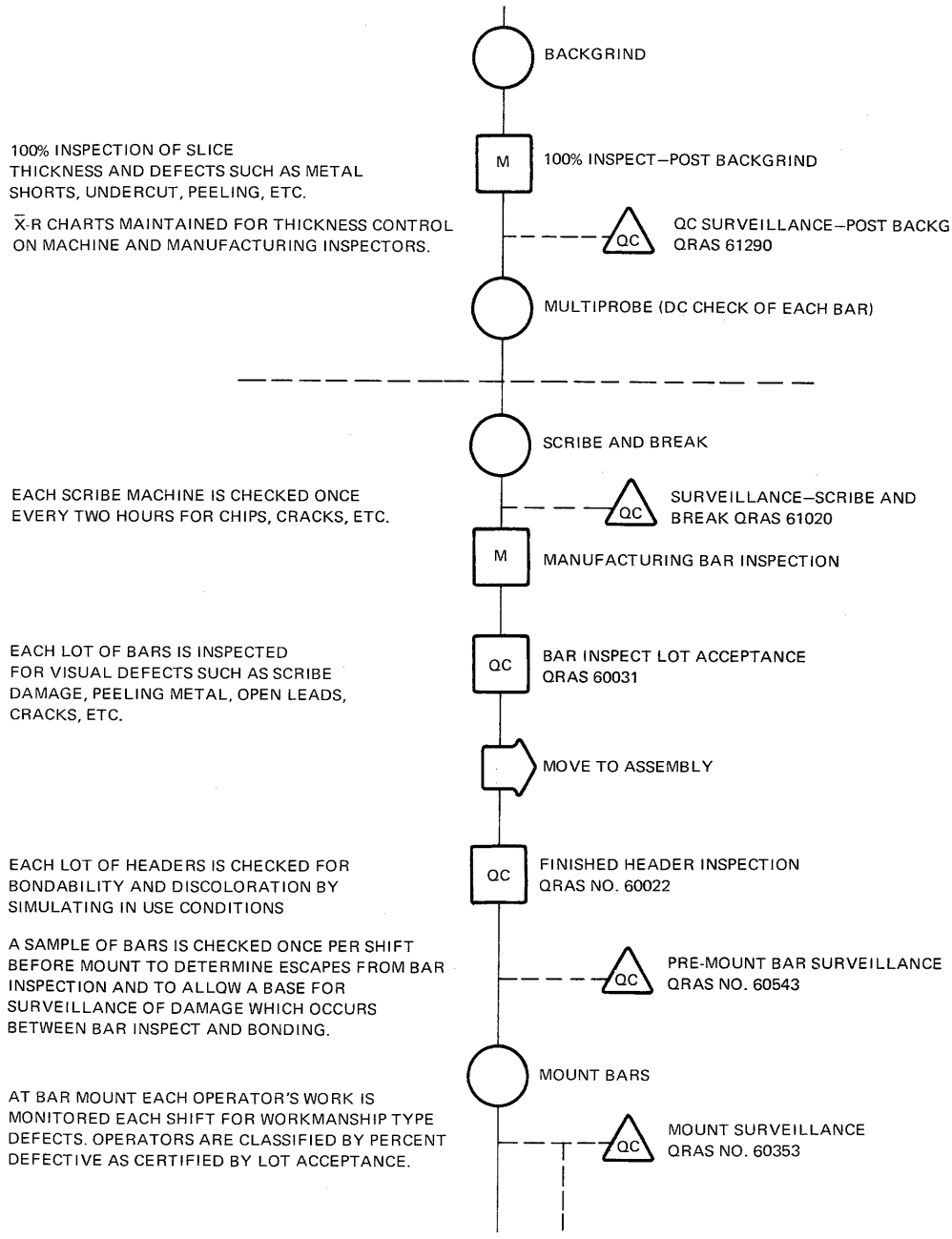
THE MANUFACTURING INSPECTORS ARE MONITORED BY RESULTS FEDBACK FROM THE QC SURVEILLANCE.

EACH LOT OF MATERIAL IS INSPECTED BY MANUFACTURING AFTER METAL REMOVAL FOR DEFECTS SUCH AS INCOMPLETE METAL REMOVAL, LEADS TOUCHING SILICON OUTSIDE CONTACTS, MISALIGNMENT, PEELING LEADS, ETC.

THE MANUFACTURING INSPECTORS ARE MONITORED BY RESULTS FEDBACK FROM THE QC SURVEILLANCE.



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222


BACKGRIND
100% INSPECTION OF SLICE THICKNESS AND DEFECTS SUCH AS METAL SHORTS, UNDERCUT, PEELING, ETC.
M
100% INSPECT–POST BACKGRIND
X̄-R CHARTS MAINTAINED FOR THICKNESS CONTROL ON MACHINE AND MANUFACTURING INSPECTORS.
QC
QC SURVEILLANCE–POST BACKGRIND QRAS 61290
MULTIPROBE (DC CHECK OF EACH BAR)
SCRIBE AND BREAK
EACH SCRIBE MACHINE IS CHECKED ONCE EVERY TWO HOURS FOR CHIPS, CRACKS, ETC.
QC
SURVEILLANCE–SCRIBE AND BREAK QRAS 61020
M
MANUFACTURING BAR INSPECTION
EACH LOT OF BARS IS INSPECTED FOR VISUAL DEFECTS SUCH AS SCRIBE DAMAGE, PEELING METAL, OPEN LEADS, CRACKS, ETC.
QC
BAR INSPECT LOT ACCEPTANCE QRAS 60031
MOVE TO ASSEMBLY
EACH LOT OF HEADERS IS CHECKED FOR BONDABILITY AND DISCOLORATION BY SIMULATING IN USE CONDITIONS
QC
FINISHED HEADER INSPECTION QRAS NO. 60022
A SAMPLE OF BARS IS CHECKED ONCE PER SHIFT BEFORE MOUNT TO DETERMINE ESCAPES FROM BAR INSPECTION AND TO ALLOW A BASE FOR SURVEILLANCE OF DAMAGE WHICH OCCURS BETWEEN BAR INSPECT AND BONDING.
QC
PRE-MOUNT BAR SURVEILLANCE QRAS NO. 60543
MOUNT BARS
AT BAR MOUNT EACH OPERATOR'S WORK IS MONITORED EACH SHIFT FOR WORKMANSHIP TYPE DEFECTS. OPERATORS ARE CLASSIFIED BY PERCENT DEFECTIVE AS CERTIFIED BY LOT ACCEPTANCE.
QC
MOUNT SURVEILLANCE QRAS NO. 60353

THE ALLOY MACHINES ARE CHECKED TWICE PER SHIFT FOR DEFECTS SUCH AS INCOMPLETE ALLOY, BAR ORIENTATION, SCRATCHES, ALLOY MATERIAL ON THE BAR, ETC.

EACH NEW FRIT MIXTURE HAS A USE TEST PERFORMED FROM IT BEFORE BEING RELEASED TO PRODUCTION. ONCE PER DAY A MICROSTRUCTURE ANALYSIS IS PERFORMED FROM EACH MOUNT FURNACE. TWICE PER SHIFT A SAMPLE FROM EACH FURNACE IS SUBJECTED TO TORQUE TEST FOR FURNACE CONTROL.

QC — ALLOY MOUNT QRAS 60413

QC — FRIT CONTROL QRAS NO. 60824

M — POST MOUNT INSPECTION

THE BONDING MACHINES ARE CHECKED FOR SUBSTRATE TEMPERATURE ONCE PER SHIFT. CAPILLARY PRESSURE IS CHECKED ONCE PER WEEK.

QC — BONDING MACHINE CONTROL QRAS NO. 60494

EACH BONDER IS CHECKED A MINIMUM OF TWICE PER SHIFT FOR WORKMANSHIP DEFECTS SUCH AS BONDS 50% OFF THE PAD, TIGHT WIRES, SHORTED WIRES, IMPROPER BOND SIZE, ETC. OPERATORS ARE CLASSIFIED DAILY INTO THREE CLASSIFICATIONS; CERTIFIED, MONITOR AND 100% INSPECT.

PULL AND SHEAR TESTS ARE PERFORMED EACH SHIFT TO MONITOR PROCESS BOND STRENGTH VARIABILITY.

ONCE PER SHIFT A SAMPLE OF BARS IS CHECKED AFTER BONDING TO DETERMINE PROCESS DAMAGE.

BONDING

QC — BONDING SURVEILLANCE QRAS NO. 60033

QC — BOND STRENGTH TESTS QRAS NOS. 60034 & 60543

QC — POST BOND BAR SURVEILLANCE QRAS NO. 60543

M — INSPECTING NETWORKS PRE-CAP 40X AND 100X INSPECTION.

EACH LOT OF DEVICES IS SAMPLED TO DETERMINE ACCEPTABILITY TO STANDARD DEFECT CRITERIA SUCH AS OPEN WIRES, SHORTED WIRES, EXTRANEOUS MATTER, ETC.

QC — PRE CAP LOT ACCEPTANCE QRAS NO. 60035

ENCAPSULATION

EACH WELDER IS CHECKED EVERY TWO HOURS TO DETERMINE PROPER OPERATION. BOTH FINE LEAK TESTS AND GROSS (BUBBLE) LEAK TESTS ARE PERFORMED. MOISTURE MONITORS ARE ALSO CHECKED AND VISUAL WELD QUALITY MONITORED.
A SAMPLE OF UNITS IS SUBJECTED TO A TORQUE TEST THAT DETERMINES THE STRENGTH OF THE PACKAGE TO LID SEAL.

QC — WELDER CONTROL QRAS NO. 60036

QC — C-DIP TORQUE TEST QRAS 61019

MOVE TO HIGH RELIABILITY FINAL TEST AREA.

PRINTED IN U.S.A.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

3

Linear Circuits

INDEX

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*					SEC.-PAGE
	–55°C to 125°C	0°C to 70°C	Dual-In-Line			Plug-In	Flat	
OPERATIONAL AMPLIFIERS								
General Purpose Operational Amplifiers	SN52702A			N		L	S	3-18
	SN52702	SN72702		N		L	S	3-18
High-Performance Operational Amplifiers	SN52101A	SN72301A	J	N	P	L	Z	3-5
	SN52107	SN72307	J	N	P	L	Z	3-9
	SN52709A			N	P	L	S	3-27
	SN52709	SN72709		N	P	L	S	3-27
	SN52741	SN72741	J	N	P	L	Z	3-34
	SN52748	SN72748	J	N	P	L	Z	3-43
	SN52770	SN72770	J	N	P	L	Z	3-47
	SN52771	SN72771	J	N	P	L	Z	3-53
Dual High-Performance Operational Amplifiers	SN52558	SN72558			P	L		3-13
	SN52747	SN72747	J	N				3-39
DIFFERENTIAL COMPARATORS								
Differential Comparators	SN52710	SN72710	J	N		L	S	3-68
	SN52810	SN72810	J	N	P	L	Z	3-79
Differential Comparators with Strobes	SN52510	SN72510	J	N	P	L	Z	3-60
Dual-Channel Differential Comparators with Strobes	SN52711	SN72711	J	N		L	S	3-72
	SN52811	SN72811	J	N		L		3-85
Dual Differential Comparators		SN72720		N				3-77
	SN52820	SN72820	J	N				3-91
Dual Differential Comparators with Strobes	SN52514	SN72514	J	N				3-66
VIDEO AMPLIFIERS								
Differential Video Amplifiers	SN52733	SN72733		N		L		3-94
	SN5510					L	F	3-101
		SN7510				L	F	3-108
	SN5511	SN7511		N		L	F	3-115
	SM5512	SM7512				L		3-121
	SN5514	SN7514				L		3-121
LINE CIRCUITS								
Dual Line Drivers	SN55109		J					3-130
		SN75109	J	N				3-130
	SN55110		J					3-130
		SN75110	J	N				3-130
Dual Line Receivers	SN55107A		J					3-130
		SN75107A	J	N				3-130
	SN55108A		J					3-130
		SN75108A	J	N				3-130
		SN75150	J	N	P			3-149
Dual Differential Line Receiver		SN75100L				L		3-126
Quadruple Line Receiver		SN75154	J	N				3-153

*For outline drawings of all packages, see Section 1.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*					SEC.-PAGE
	−55°C to 125°C	0°C to 70°C		Dual-In-Line		Plug-In	Flat	
SENSE AMPLIFIERS								
Dual-Channel Sense Amplifiers		SN7522	J	N				3-166
		SN7523	J	N				3-166
Dual-Channel Sense Amplifiers with Complementary Outputs		SN7520	J	N				3-164
		SN7521	J	N				3-164
Dual-Channel Sense Amplifiers with Output Registers		SN7526	J	N				3-172
		SN7527	J	N				3-172
Dual Sense Amplifiers		SN7524	J	N				3-170
		SN7525	J	N				3-170
		SN75234	J	N				3-176
		SN75235	J	N				3-176
Dual Sense Amplifiers with Preamplifier Test Points		SN7528	J	N				3-174
		SN7529	J	N				3-174
		SN75238	J	N				3-178
		SN75239	J	N				3-178
MEMORY AND PERIPHERAL DRIVERS								
2 X 4 Transistor Arrays		SN75303		N			S	3-212
		SN75308	J	N				3-217
Memory Driver		SN75325						3-230
Memory Driver with Decode Inputs		SN75324						3-222
Dual Peripheral Drivers		SN75450A		N				3-247
		SN75451A			P			3-249
		SN75452		P	P			3-250
		SN75453			P			3-251
		SN75454			P			3-252
Diode Arrays	TID21A Series			N			F	3-264
VOLTAGE REGULATOR								
Voltage Regulator		SN72400		N		L		3-270
COMMUNICATIONS CIRCUITS								
Logarithmic Amplifiers	SN56502	SN76502	J	N				3-277
Balanced Mixers	SN56514	SN76514	J	N		L		3-284
CONSUMER CIRCUITS								
Consumer Circuits Summary								3-289
Stereo Demodulator		SN76110		N				3-290

*For outline drawings of all packages, see Section 1.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

OPERATIONAL AMPLIFIER SELECTION GUIDE

Series 52

TYPE	SN52702	SN52709	SN52741	SN52747	SN52748	SN52770	SN52771	SN52558	SN52101A	SN52107	
FEATURES	Wide BW, General Purpose	General Purpose	Internally Compensated Gen. Pur.	Dual SN52741	Extended BW, Gen. Pur.	Super β	Super β	Dual 741 in 8-pin Package	Precision Op Amp	Internally Compensated	UNIT
Input Offset Voltage, Max	5	5	5	5	5	4	4	5	2	2	mV
Input Offset Current, Max	500	200	200	200	200	2	2	200	10	10	nA
Temperature Coefficient of Input Offset Voltage, Typ	10	6	7	7	7	10	10	7	3	3	μV/°C
Input Bias Current, Max	10,000	500	500	500	500	15	15	500	75	75	nA
Voltage Amplification, Min	1.4	25	50	50	50	50	50	50	50	50	V/mV
Slew Rate at Unity Gain, Typ	1.7	0.3	0.5	0.5	0.5	2.5	2.5	0.5	0.5	0.5	V/μs
Unity-Gain Bandwidth, Typ	30	5	1	1	1	1.3	1.3	1	1	1	MHz
Min Supply Voltage	+6, −3	±9	±5	±5	±5	±3	±3	±5	±3	±3	V
Max Supply Voltage	+14, −7	±18	±22	±22	±22	±22	±22	±22	±22	±22	V
Input Voltage Range, Min	0.5 to −4	±8	±12	±12	±12	±12	±12	±12	±15	±15	V
Differential Input Voltage Rating	±5	±5	±30	±30	±30	±30	±30	±30	±30	±30	V
Internal Compensation	No	No	Yes	Yes	No	No	Yes	Yes	No	Yes	
Offset Adjust	No	No	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	
Input Protection	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Output Protection	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	

Series 72

TYPE	SN72702	SN72709	SN72741	SN72747	SN72748	SN72770	SN72771	SN72558	SN72301A	SN72307	
FEATURES	Wide BW, General Purpose	General Purpose	Internally Compensated, Gen. Pur.	Dual SN72741	Extended BW, Gen. Pur.	Super β	Super β	Dual 741 in 8-pin Package	Precision Op Amp	Internally Compensated	UNIT
Input Offset Voltage, Max	5	7.5	6	6	6	10	10	6	7.5	7.5	mV
Input Offset Current, Max	500	500	200	200	200	10	10	200	50	50	nA
Temperature Coefficient of Input Offset Voltage, Typ	5	6	7	7	7	10	10	7	6	6	μV/°C
Input Bias Current, Max	15,000	1500	500	500	500	30	30	500	250	250	nA
Voltage Amplification, Min	1	15	20	20	20	35	35	20	25	25	V/mV
Slew Rate at Unity Gain, Typ	1.7	0.3	0.5	0.5	0.5	2.5	2.5	0.5	0.5	0.5	V/μs
Unity-Gain Bandwidth, Typ	30	5	1	1	1	1.3	1.3	1	1	1	MHz
Min Supply Voltage	+6, −3	±9	±5	±5	±5	±3	±3	±5	±3	±3	V
Max Supply Voltage	+14, −7	±18	±18	±18	±18	±18	±18	±18	±18	±18	V
Input Voltage Range, Min	0.5 to −4	±8	±12	±12	±12	±11	±11	±12	±12	±12	V
Differential Input Voltage Rating	±5	±5	±30	±30	±30	±30	±30	±30	±30	±30	V
Internal Compensation	No	No	Yes	Yes	No	No	Yes	Yes	No	Yes	
Offset Adjust	No	No	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	
Input Protection	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Output Protection	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN52101A, SN72301A
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

- Low Input Currents
- Low Input Offset Parameters
- Frequency and Transient Response Characteristics Adjustable
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Designed to be Interchangeable with National Semiconductor LM101A and LM301A
- No Latch-Up
- Large Common-Mode and Differential Voltage Ranges
- Same Pin Assignments as SN52709 and SN72709

description

The SN52101A and SN727301A are high-performance operational amplifiers, featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices.

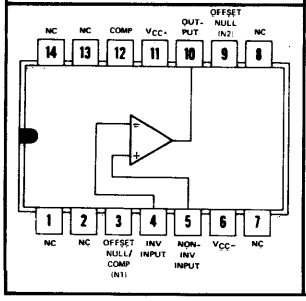
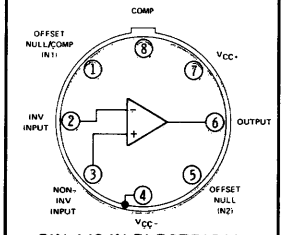
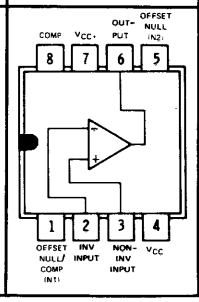
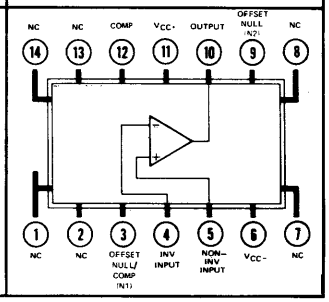
The high common-mode input voltage range and the absence of latch-up make the SN52101A and SN72301A ideal for voltage-follower applications. The devices are protected to withstand short-circuits at the output. The external compensation of the SN52101A and the SN72301A allows the changing of the frequency response (when the closed-loop gain is greater than unity) for applications requiring wider bandwidth or higher slew rate.

A potentiometer may be connected between the offset-null inputs (N1 and N2), as shown in Figure 8, to null out the offset voltage.

The SN52101A is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72301A is characterized for operation from 0°C to 70°C.

3

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	P DUAL-IN-LINE PACKAGE (TOP VIEW)	Z FLAT PACKAGE (TOP VIEW)
			

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52101A	SN72301A	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52101A only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

voltages specified

Throughout this data sheet, supply voltages are specified either as a range or as a specific value. A positive voltage within the specified range (or of the specified value) is applied to V_{CC+}, and an equal negative voltage is applied to V_{CC-}.

electrical characteristics at specified free-air temperature (see note 6)

PARAMETER		TEST CONDITIONS†		SN52101A			SN72301A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 kΩ	25°C		0.6	2		2.0	7.5	mV
			Full range			3			10	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		3	15		6	30	μV/°C
I_{IO}	Input offset current		25°C		1.5	10		3	50	nA
			Full range			20			70	
α_{IIO}	Average temperature coefficient of input offset current	T_A = −55°C to 25°C			0.02	0.2				nA/°C
		T_A = 25°C to 125°C			0.01	0.1				
		T_A = 0°C to 25°C						0.02	0.6	
		T_A = 25°C to 70°C						0.01	0.3	
I_{IB}	Input bias current		25°C		30	75		70	250	nA
			Full range			100			300	
V_I	Input voltage range	See Note 7	Full range	±15			±12			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	25°C	20	26		20	26		
			Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, $R_L \geq$ 2 kΩ	25°C	50,000	200,000		25,000	200,000		
			Full range	25,000			15,000			
r_i	Input resistance		25°C	1.5	4		0.5	2		MΩ
CMRR	Common-mode rejection ratio	R_S = 50 kΩ	25°C	80	98		70	90		dB
			Full range	80			70			
$\Delta V_{CC}/\Delta V_{IO}$	Power supply rejection ratio	R_S = 50 kΩ	25°C	80	98		70	96		dB
			Full range	80			70			
I_{CC}	Supply current	No load, No signal, See Note 7	25°C		1.8	3		1.8	3	mA
			125°C		1.2	2.5				

†All characteristics are specified under open-loop operation. Full range for SN52101A is −55°C to 125°C and for SN72301A is 0°C to 70°C.

NOTES: 6. Unless otherwise noted, $V_{CC\pm}$ = ±5 V to ±20 V for SN52101A and $V_{CC\pm}$ = ±5 V to ±15 V for SN72301A. All typical values are at $V_{CC\pm}$ = ±15 V.
7. For SN52101A, $V_{CC\pm}$ = ±20 V. For SN72301A, $V_{CC\pm}$ = ±15 V.

For ordering instructions and mechanical data, see the SN52741/SN72741 data sheet dated November 1970.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Average Temperature Coefficient Of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which, if exceeded at either input terminal, will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) The ratio of the change in power supply voltages to the change in input offset voltage. For these devices, both supply voltages are varied symmetrically.

THERMAL INFORMATION

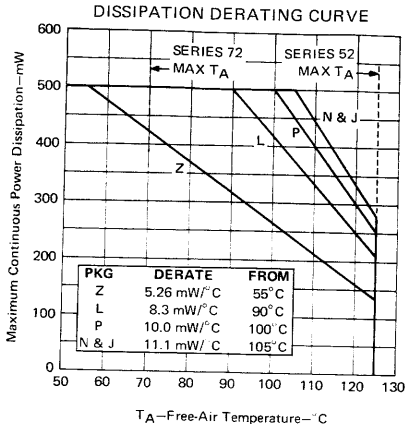


FIGURE 1

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

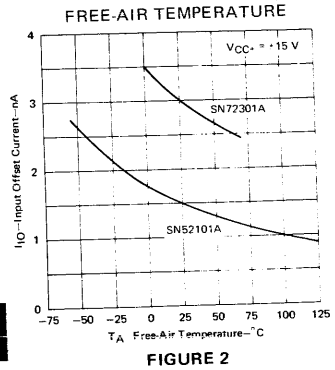


FIGURE 2

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

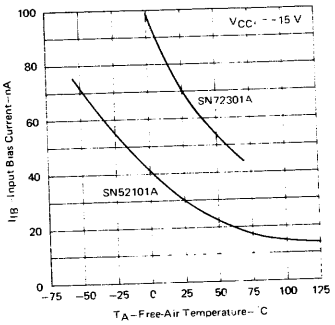


FIGURE 3

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (WITH
SINGLE-POLE COMPENSATION)
vs FREQUENCY

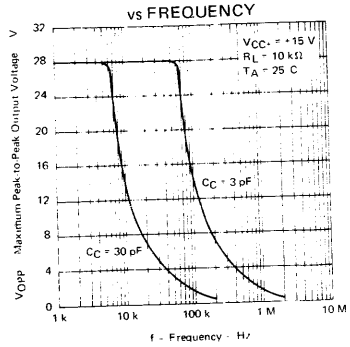


FIGURE 4

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

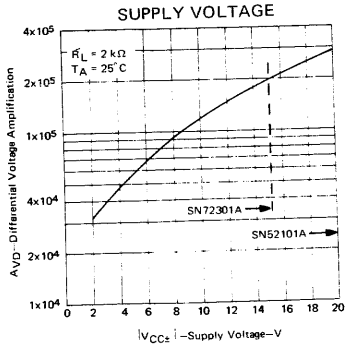


FIGURE 5

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

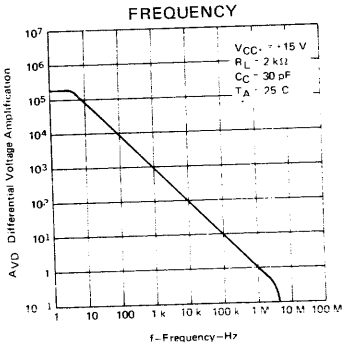


FIGURE 6

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

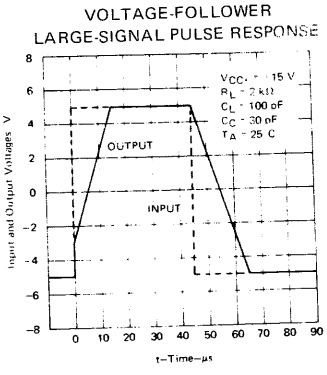
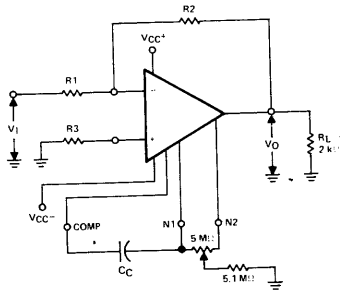


FIGURE 7

TYPICAL APPLICATION DATA



$$\frac{V_O}{V_I} = -\frac{R2}{R1}$$

$$C_C \geq \frac{R1 \cdot 30\ pF}{R1+R2}$$

$$R3 = \frac{R1 \cdot R2}{R1+R2}$$

FIGURE 8 – INVERTING CIRCUIT WITH ADJUSTABLE GAIN, SINGLE-POLE COMPENSATION, AND OFFSET ADJUSTMENT

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

LINEAR INTEGRATED CIRCUITS

CIRCUIT TYPES SN52107, SN72307 HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

- Low Input Currents
- No Frequency Compensation Required
- Offset-Voltage Null Capability
- Low Input Offset Parameters
- Designed to be Interchangeable with National Semiconductor LM107 and LM307
- Short-Circuit Protection
- No Latch-Up
- Large Common-Mode and Differential Voltage Ranges
- Same Pin Assignments as SN52741 and SN72741

description

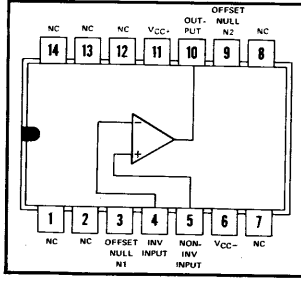
The SN52107 and SN72307 are high-performance operational amplifiers, featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices.

The high common-mode input voltage range and the absence of latch-up make the SN52107 and SN72307 ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset-null inputs, as shown in Figure 2, to null out the offset voltage.

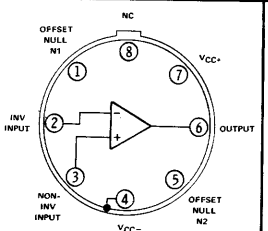
The SN52107 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72307 is characterized for operation from 0°C to 70°C.

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

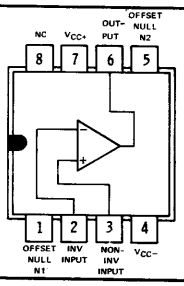


L PLUG-IN PACKAGE (TOP VIEW)

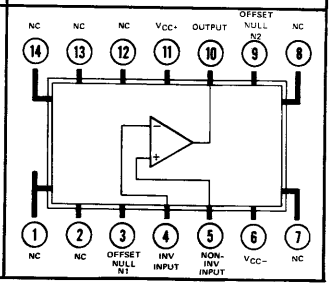


PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

P DUAL-IN-LINE PACKAGE (TOP VIEW)



Z FLAT PACKAGE (TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52107	SN72307	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52107 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

voltages specified

Throughout this data sheet, supply voltages are specified either as a range or as a specific value. A positive voltage within the specified range (or of the specified value) is applied to V_{CC+}, and an equal negative voltage is applied to V_{CC-}.

electrical characteristics at specified free-air temperature (see note 6)

PARAMETER		TEST CONDITIONS†		SN52107 MIN	SN52107 TYP	SN52107 MAX	SN72307 MIN	SN72307 TYP	SN72307 MAX	UNIT
V_{IO}	Input offset voltage	R_S = 50 kΩ	25°C		0.6	2		2	7.5	mV
			Full range			3			10	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		3	15		6	30	μV/°C
I_{IO}	Input offset current		25°C		1.5	10		3	50	nA
			Full range			20			70	
α_{IIO}	Average temperature coefficient of input offset current	T_A = −55°C to 25°C			0.02	0.2				nA/°C
		T_A = 25°C to 125°C			0.01	0.1				
		T_A = 0°C to 25°C						0.02	0.6	
		T_A = 25°C to 70°C						0.01	0.3	
I_{IB}	Input bias current		25°C		30	75		70	250	nA
			Full range			100			300	
V_I	Input voltage range	See Note 7	Full range	±15			±12			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	25°C	20	26		20	26		
			Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, $R_L \geq$ 2 kΩ	25°C	50,000	200,000		25,000	200,000		
			Full range	25,000			15,000			
r_i	Input resistance		25°C	1.5	4		0.5	2		MΩ
CMRR	Common-mode rejection ratio	R_S = 50 kΩ	25°C	80	98		70	90		dB
			Full range	80			70			
$\Delta V_{CC}/\Delta V_{IO}$	Power supply rejection ratio	R_S = 50 kΩ	25°C	80	98		70	96		dB
			Full range	80			70			
I_{CC}	Supply current	No load, No signal, See Note 7	25°C		1.8	3		1.8	3	mA
			125°C		1.2	2.5				

†All characteristics are specified under open-loop operation. Full range for SN52107 is −55°C to 125°C and for SN72307 is 0°C to 70°C.

NOTES: 6. Unless otherwise noted $V_{CC\pm}$ = ±5 V to ±20 V for SN52107 and $V_{CC\pm}$ = ±5 V to ±15 V for SN72307. All typical values are at $V_{CC\pm}$ = ±15 V.
7. For SN52107, $V_{CC\pm}$ = ±20 V. For SN72307, $V_{CC\pm}$ = ±15 V.

For ordering instructions and mechanical data, see the SN52741/SN72741 data sheet dated November 1970.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Average Temperature Coefficient Of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

3

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which, if exceeded at either input terminal, will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) The ratio of the change in power supply voltages to the change in input offset voltage. For these devices, both supply voltages are varied symmetrically.

THERMAL INFORMATION

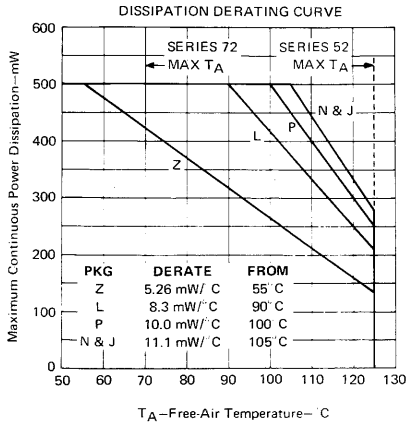


FIGURE 1

TYPICAL APPLICATION DATA

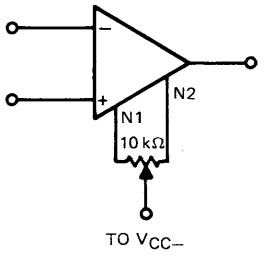


FIGURE 2–INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

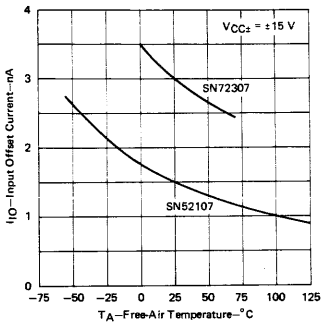


FIGURE 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

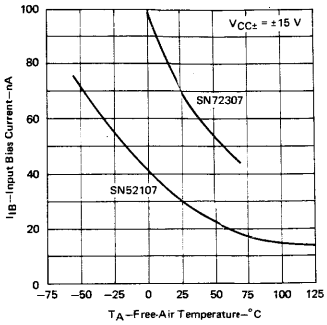


FIGURE 4

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

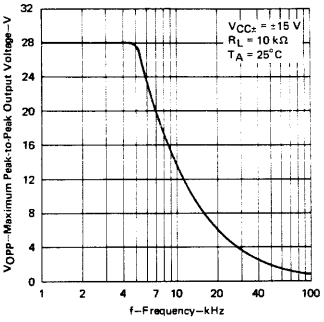


FIGURE 5

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

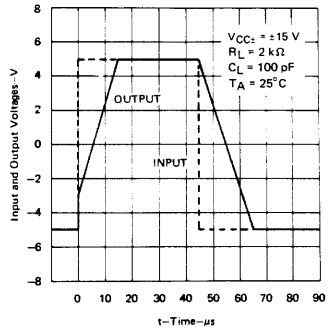


FIGURE 6

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

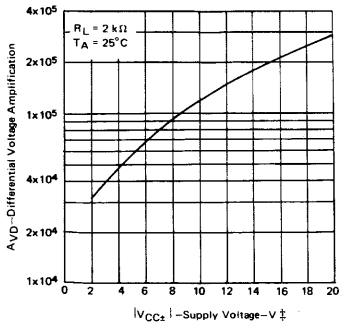


FIGURE 7

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

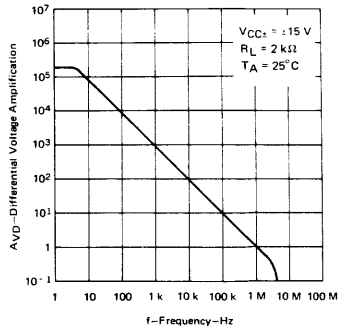


FIGURE 8

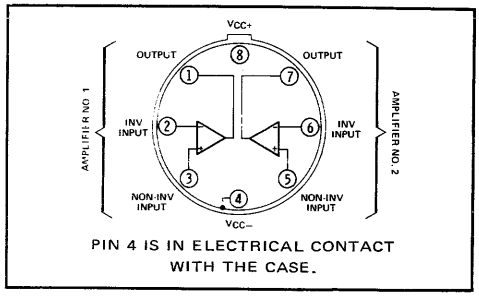
‡ Data for supply voltages greater than 15 V is applicable to SN52107 circuits only.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

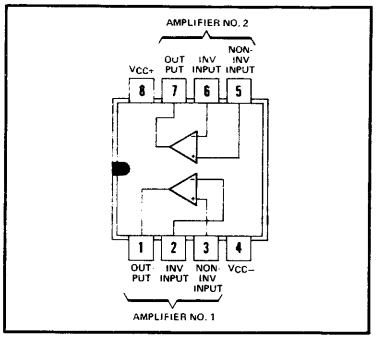
CIRCUIT TYPES SN52558, SN72558
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

- Short-Circuit Protection
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up
- Designed to be Interchangeable with Motorola MC1558/MC1458 and Signetics S5558/N5558

L PLUG-IN PACKAGE
(TOP VIEW)



P DUAL-IN-LINE PACKAGE
(TOP VIEW)



3

description

The SN52558 and SN72558 are dual high-performance operational amplifiers with each half electrically similar to SN52741/SN72741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensator ensures stability without external components.

The SN52558 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72558 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52558	SN72558	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 5)	Each amplifier	500	500	mW
	Total package	680	680	
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	L Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52558 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation of SN52558 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

CIRCUIT TYPES SN52558, SN72558
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52558			SN72558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10\ k\Omega$	25°C		1	5		1	6	mV
			Full range			6			7.5	
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	24	28		24	28		V
		$R_L \geq$ 10 kΩ	Full range	24			24			
		R_L = 2 kΩ	25°C	20	26		20	26		
		$R_L \geq$ 2 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ±10 V	25°C	50,000	200,000		20,000	200,000		
			Full range	25,000			15,000			
B_{OM}	Maximum-output-swing bandwidth (closed-loop)	R_L = 2 kΩ, $V_O \geq$ ±10 V, A_{VD} = 1, THD ≤ 5%	25°C		14			14		kHz
B_1	Unity-gain bandwidth		25°C		1			1		MHz
ϕ_m	Phase margin	A_{VD} = 1	25°C		65°			65°		
A_m	Gain margin		25°C		11			11		dB
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
z_{ic}	Common-mode input impedance	f = 20 Hz	25°C		200			200		MΩ
CMRR	Common-mode rejection ratio	$R_S \leq 10\ k\Omega$	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10\ k\Omega$	25°C		30	150		30	150	μV/V
			Full range			150			150	
e_n	Equivalent input noise voltage (closed-loop)	A_{VD} = 100, R_S = 0, f = 1 kHz, BW = 1 Hz	25°C		45			45		nV/√Hz
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current (Both amplifiers)	No load, No signal	25°C		3.4	5.6		3.4	5.6	mA
			Full range			6.6			6.6	
P_D	Total power dissipation (Both amplifiers)	No load, No signal	25°C		100	170		100	170	mW
			Full range			200			200	
V_{o1}/V_{o2}	Channel separation		25°C		120			120		dB

†All characteristics are specified under open-loop operation, unless otherwise noted. Full range for SN52558 is −55°C to 125°C and for SN72558 is 0°C to 70°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52558			SN72558			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 2		0.3			0.3		μs
	Overshoot			5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 2		0.5			0.5		V/μs

For mechanical data and ordering instructions, see the SN52741/SN72741 data sheet dated November 1970.

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Maximum-Output-Swing Bandwidth (B_{OM}) The range of frequencies within which the maximum output voltage swing is above a specified value.

Unity-Gain Bandwidth (B_1) The range of frequencies within which the voltage amplification is greater than unity.

Phase Margin (ϕ_m) A figure equal to 180° minus the absolute value of the phase shift measured around the loop at that frequency at which the magnitude of the loop gain is unity.

Gain Margin (A_m) The reciprocal of the differential voltage amplification at that frequency where the absolute value of the phase shift measured around the loop is 180°.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between the output terminal and ground.

Input Capacitance (C_i) The capacitance between the input terminals with either input grounded.

Common-Mode Input Impedance (z_{ic}) The parallel sum of the small-signal impedances between each input terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Power Supply Sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) The ratio of the change in input offset voltage to the change in supply voltages producing it. For these devices, both supply voltages are varied symmetrically.

Short-Circuit Output Current (I_{OS}) The maximum output current available from the amplifier with the output shorted to ground or to either supply.

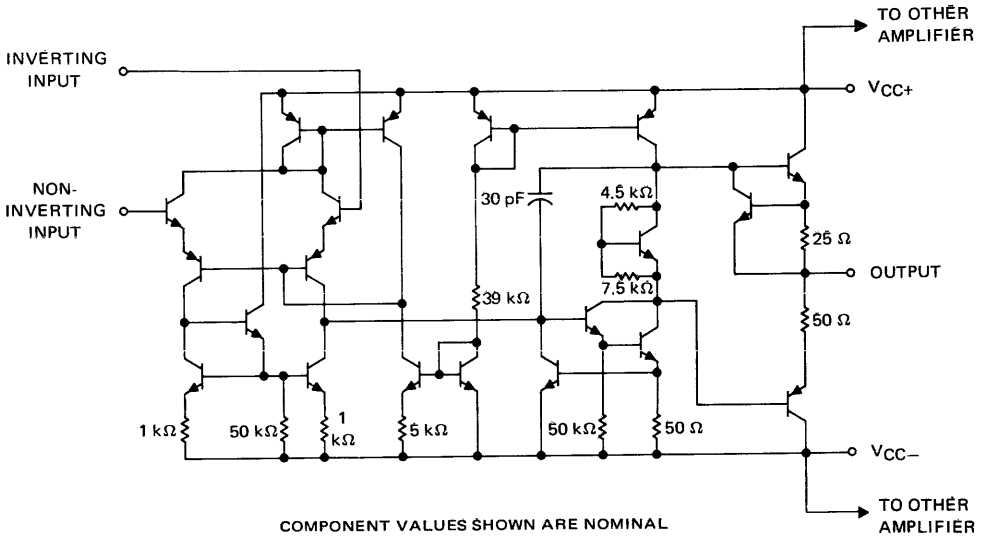
Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Overshoot The quotient of: (1) the largest deviation of the output signal value from its steady-state value after a step-function change of the input signal, and (2) the difference between the output signal values in the steady state before and after the step-function change of the input signal.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output voltage for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

schematic (each amplifier)



COMPONENT VALUES SHOWN ARE NOMINAL

3

THERMAL INFORMATION

DISSIPATION DERATING CURVE

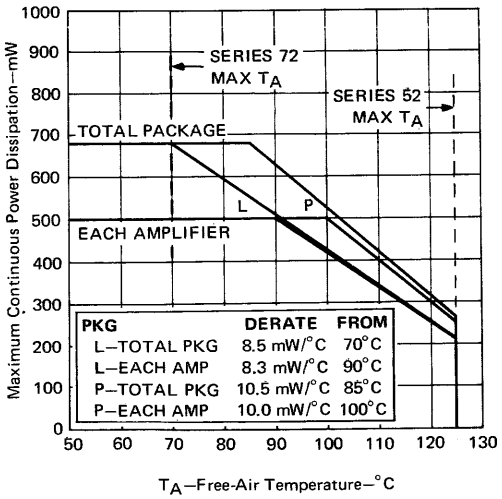
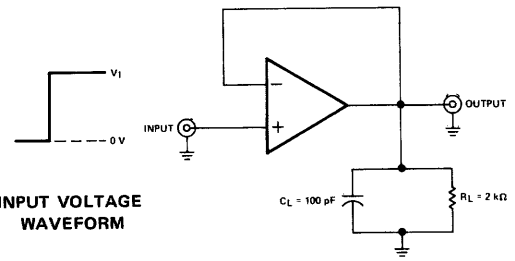


FIGURE 1

PARAMETER MEASUREMENT INFORMATION



INPUT VOLTAGE WAVEFORM

TEST CIRCUIT

FIGURE 2–RISE TIME, OVERSHOOT, AND SLEW RATE

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

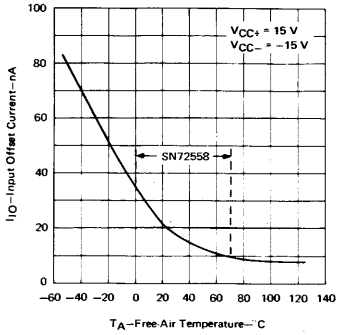


FIGURE 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

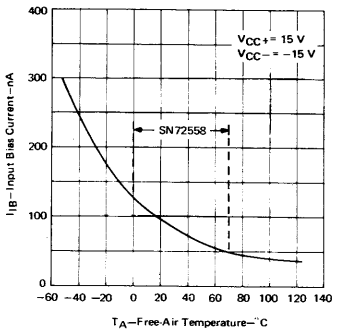


FIGURE 4

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

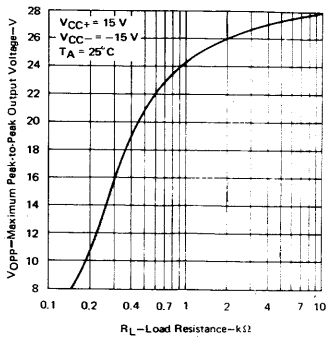


FIGURE 5

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

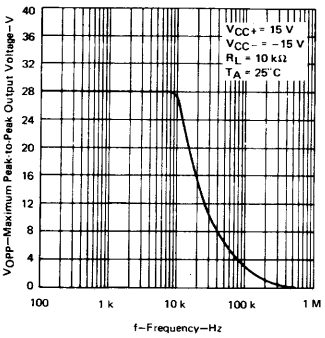


FIGURE 6

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

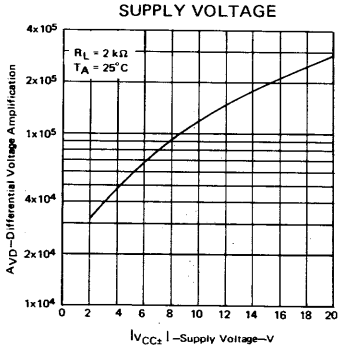


FIGURE 7

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

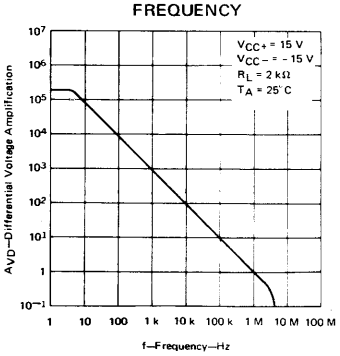


FIGURE 8

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

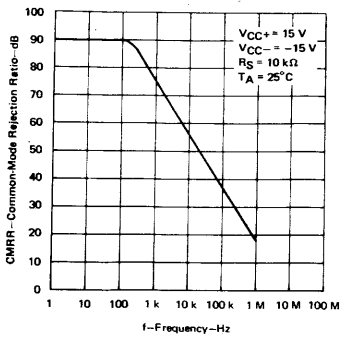


FIGURE 9

OUTPUT VOLTAGE
vs
ELAPSED TIME

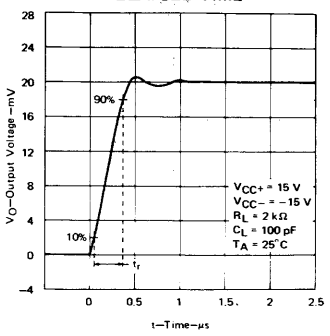


FIGURE 10

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

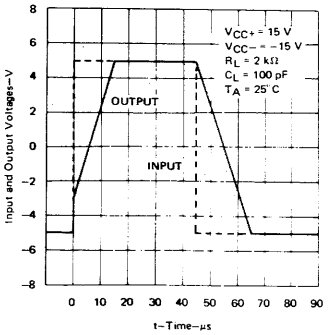


FIGURE 11

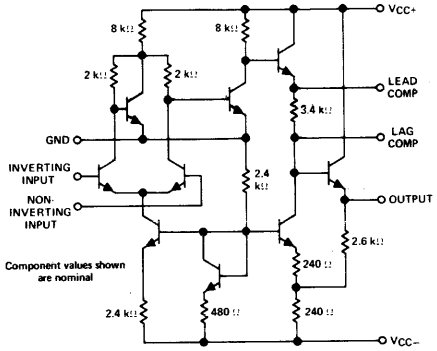
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN52702A, SN52702, SN72702 GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

SN52702A features

- Open-Loop Voltage Amplification . . . 3600 Typ
- Designed to be Interchangeable With Fairchild μA702A
- CMRR . . . 100 dB Typ

schematic

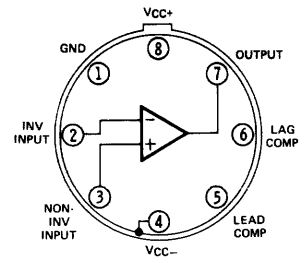
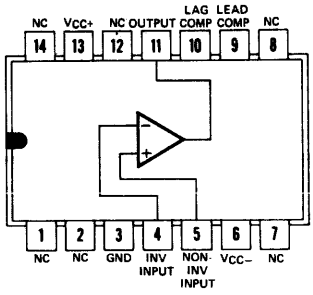
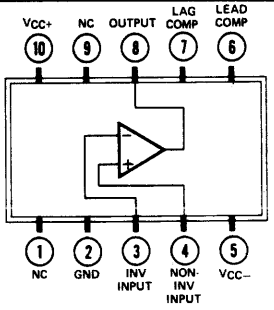


description

The SN52702A, SN52702 and SN72702 circuits are high-gain, wideband operational amplifiers, each having differential inputs and single-ended emitter-follower outputs. Provisions are incorporated within the circuit whereby external components may be used to compensate the amplifier for stable operation under various feedback or load conditions. Component matching, inherent in silicon monolithic circuit-fabrication techniques, produces an amplifier with low-drift and low-offset characteristics. The SN52702A is an improved version of the SN52702. These amplifiers are particularly useful for applications requiring transfer or generation of linear and non-linear functions up to a frequency of 30 MHz.

The SN52702A and SN52702 circuits are characterized for operation over the full military temperature range of −55°C to 125°C. The SN72702 circuit is characterized for operation over the temperature range of 0°C to 70°C.

terminal assignments

L PLUG-IN PACKAGE (TOP VIEW)	N DUAL-IN-LINE PACKAGE (TOP VIEW)	S FLAT PACKAGE (TOP VIEW)
		
PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE		PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52702A, SN52702	SN72702	UNIT
Supply voltage V_{CC+} (see Note 1)		14	14	V
Supply voltage V_{CC-} (see Note 1)		−7	−7	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Notes 1 and 3)		−6 to 1.5	−6 to 1.5	V
Peak output current ($t_w \leq 1$ S)		50	50	mA
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 4)		300	300	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	L or S Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the lesser of the two supply voltages.
4. For operation of SN52702A and SN52702 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 3.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SN52702A

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS†			SN52702A V_{CC+} = 12 V, V_{CC-} = −6 V MIN	SN52702A V_{CC+} = 12 V, V_{CC-} = −6 V TYP	SN52702A V_{CC+} = 12 V, V_{CC-} = −6 V MAX	SN52702A V_{CC+} = 6 V, V_{CC-} = −3 V MIN	SN52702A V_{CC+} = 6 V, V_{CC-} = −3 V TYP	SN52702A V_{CC+} = 6 V, V_{CC-} = −3 V MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 2\ k\Omega$		25°C		0.5	2		0.7	3	mV
				Full range			3			4	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$		−55°C to 25°C		2	10		3	15	µV/°C
				25°C to 125°C		2.5	10		3.5	15	
I_{IO}	Input offset current			25°C		0.2	0.5		0.12	0.5	µA
				−55°C		0.4	1.5		0.3	1.5	
				125°C		0.08	0.5		0.05	0.5	
α_{IIO}	Average temperature coefficient of input offset current			−55°C to 25°C		3	16		2	13	nA/°C
				25°C to 125°C		1	5		0.7	4	
I_{IB}	Input bias current			25°C		2	5		1.2	3.5	µA
				−55°C		4.3	10		2.6	7.5	
V_I	Input voltage range	Positive swing		25°C	0.5	1		0.5	1		V
		Negative swing			−4	−5		−1.5	−2		
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 100\ k\Omega$		25°C	10	10.6		5	5.4		V
				Full range	10			5			
		$R_L = 10\ k\Omega$		25°C	7	8		3	4		
		$R_L \geq 10\ k\Omega$		Full range	7			3			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 100\ k\Omega$	$V_O = \pm 5$ V	25°C	2500	3600	6000				
				Full range	2000		7000				
			$V_O = \pm 2.5$ V	25°C				600	900	1500	
				Full range				500		1750	
r_i	Input resistance			25°C	16	40		22	67		kΩ
				Full range	6			8			
r_o	Output resistance	V_O = 0,	See Note 3	25°C		200	500		300	700	Ω
CMRR	Common-mode rejection ratio	$R_S \leq 2\ k\Omega$		25°C	80	100		80	100		dB
				Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 2\ k\Omega$		25°C		75			75		µV/V
				Full range			200			200	
I_{CC}	Supply current	No load,	No signal	25°C		5	6.7		2.1	3.3	mA
				−55°C		5	7.5		2.1	3.9	
				125°C		4.4	6.7		1.7	3.3	
P_D	Total power dissipation	No load,	No signal	25°C		90	120		19	30	mW
				−55°C		90	135		19	35	
				125°C		80	120		15	30	

†All characteristics are specified under open-loop operation. Full range for SN52702A is −55°C to 125°C.

NOTE 3: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

SN52702

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS†			SN52702 V_{CC+} = 12 V, V_{CC-} = −6 V			SN52702 V_{CC+} = 6 V, V_{CC-} = −3 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 2\ k\Omega$		25°C		2	5		2	5	mV
				Full range			6			6	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$		−55°C to 25°C		10			10		μV/°C
				25°C to 125°C		5			5		
I_{IO}	Input offset current			25°C		0.5	2		0.3	2	μA
				−55°C		1	3			3	
				125°C		0.2	3			3	
α_{IIO}	Average temperature coefficient of input offset current			−55°C to 25°C		6			5		nA/°C
				25°C to 125°C		3			2		
I_{IB}	Input bias current			25°C		4	10		2.5	7	μA
				−55°C		6.5	20			14	
V_I	Input voltage range	Positive swing		25°C	0.5	1		0.5	1		V
		Negative swing			−4	−5		−1.5	−2		
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 100\ k\Omega$			10	10.6		5	5.4		V
		$R_L = 10\ k\Omega$				8			4		
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 100\ k\Omega$	$V_O = \pm 5$ V	25°C	1400	2600					
				Full range	1000						
			$V_O = \pm 2.5$ V	25°C				380	700		
r_i	Input resistance			25°C	8	25		12	40		kΩ
				Full range	3			4			
r_o	Output resistance	$V_O = 0$,	See Note 3	25°C		200	500		300	700	Ω
CMRR	Common-mode rejection ratio	$R_S \leq 2\ k\Omega$		25°C	70	80		70	80		dB
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 2\ k\Omega$		25°C		60	300		60	300	μV/V
I_{CC}	Supply current	No load,	No signal	25°C		5	6.7		2.1	3.9	mA
P_D	Total power dissipation	No load,	No signal	25°C		90	120		19	35	mW

†All characteristics are specified under open-loop operation. Full range for SN52702 is −55°C to 125°C.

NOTE 3: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SN72702

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V

PARAMETER		TEST CONDITIONS†			SN72702 MIN	SN72702 TYP	SN72702 MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 2\ k\Omega$		25°C		5	10	mV
				Full Range			15	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$		Full Range		5		μV/°C
I_{IO}	Input offset current			25°C		0.5	5	μA
				Full Range			7.5	
α_{IIO}	Average temperature coefficient of input offset current			0°C to 25°C		5		nA/°C
				25°C to 70°C		3		
I_{IB}	Input bias current			25°C		4	15	μA
				0°C		4.5	20	
V_I	Input voltage range	Positive swing		25°C	0.5	1		V
		Negative swing			−4	−5		
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 100\ k\Omega$		25°C	10	10.6		V
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 100\ k\Omega$,	$V_O = \pm 5$ V	25°C	1000	2600		
				Full Range	800			
r_i	Input resistance			25°C	6	25		kΩ
				Full Range	3.5			
r_o	Output resistance	$V_O = 0$,	See Note 3	25°C		200	600	Ω
CMRR	Common-mode rejection ratio	$R_S \leq 2\ k\Omega$		25°C	65	80		dB
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 2\ k\Omega$		25°C		60	300	μV/V
I_{CC}	Supply current	No load,	No signal	25°C		5	7	mA
P_D	Total power dissipation	No load,	No signal	25°C		90	125	mW

†All characteristics are specified under open-loop operation. Full range for SN72702 is 0°C to 70°C.

NOTE 3: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

SN52702A, SN52702, SN72702

operating characteristics V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	ALL TYPES MIN	ALL TYPES TYP	ALL TYPES MAX	UNIT
t_r	Rise time	1	V_I = 10 mV, C_L = 0		25	120	ns
		2	V_I = 1 mV		10	30	ns
	Overshoot	1	V_I = 10 mV, C_L = 100 pF		10%	50%	
		2	V_I = 1 mV		20%	40%	
SR	Slew rate	1	V_I = 6 V, C_L = 100 pF		1.7		V/μs
		2	V_I = 100 mV		11		

PARAMETER MEASUREMENT INFORMATION

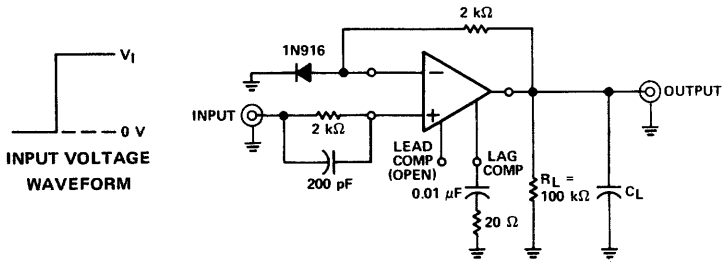


FIGURE 1–UNITY-GAIN AMPLIFIER

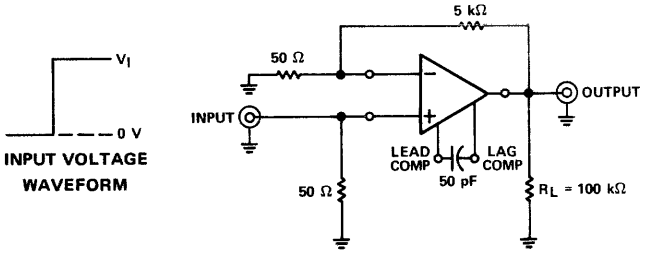


FIGURE 2–GAIN-OF-100 AMPLIFIER

THERMAL INFORMATION

SN52702A, SN52702
DISSIPATION DERATING CURVE

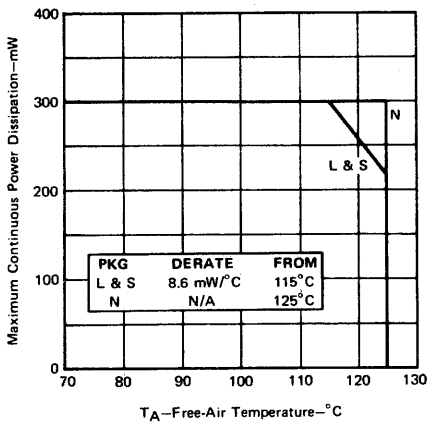


FIGURE 3

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Average Temperature Coefficient Of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Power Supply Sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) The ratio of the change in input offset voltage to the change in supply voltages producing it. For these devices, both supply voltages are varied symmetrically.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Overshoot The quotient of: (1) the largest deviation of the output signal value from its steady-state value after a step-function change of the input signal, and (2) the difference between the output signal values in the steady state before and after the step-function change of the input signal.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output voltage for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

TYPICAL CHARACTERISTICS

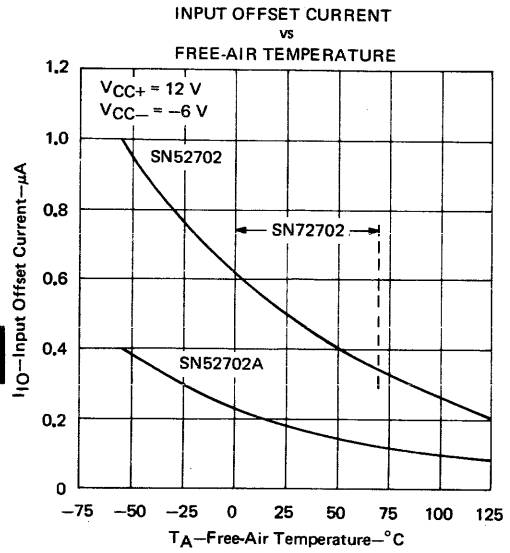


FIGURE 4

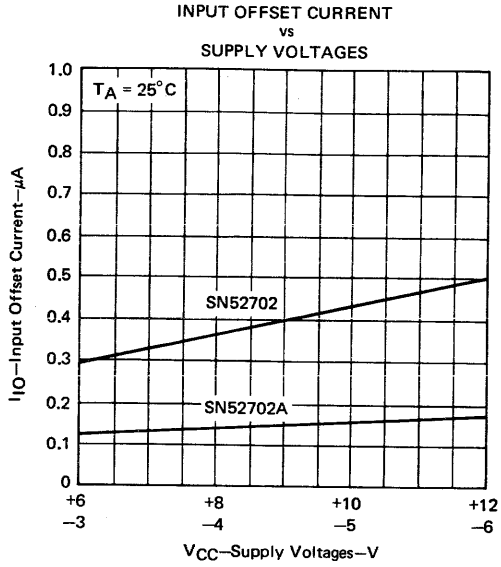


FIGURE 5

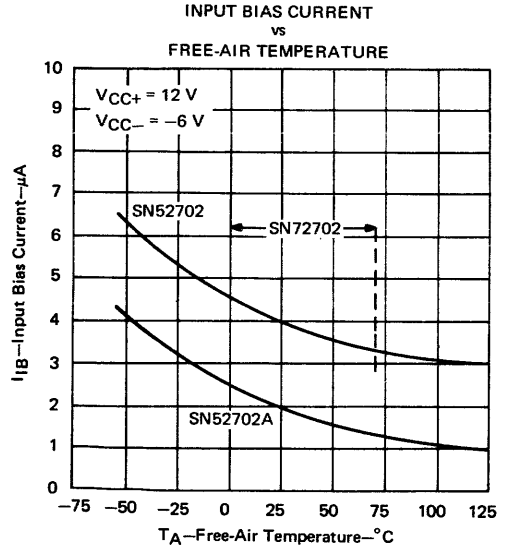


FIGURE 6

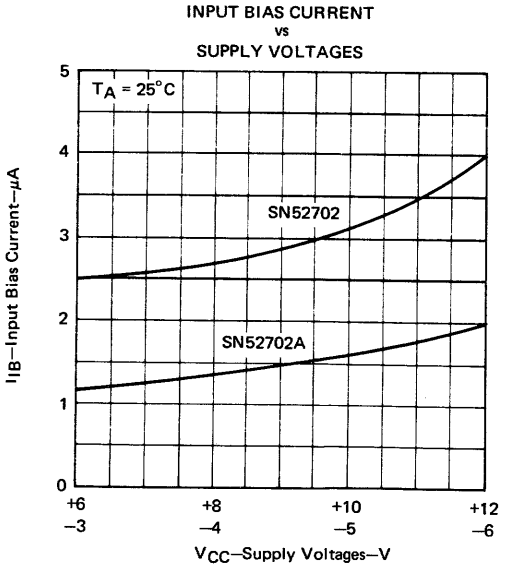


FIGURE 7

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY
(for various lag compensations)

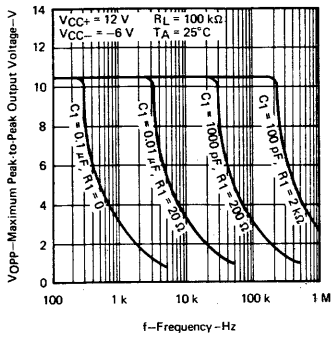
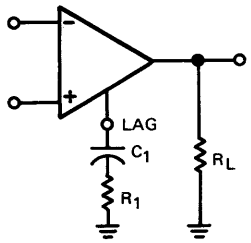


FIGURE 8



LAG COMPENSATION CIRCUIT FOR FIGURES 8, 9, AND 10

SN52709A
LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

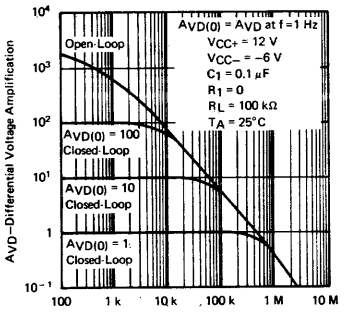


FIGURE 9

SN52702A
LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY
(for various lag compensations)

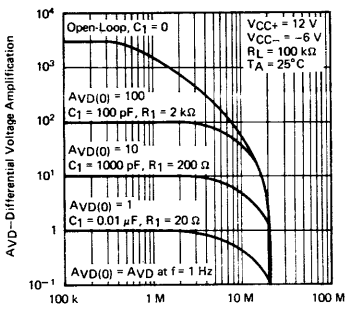


FIGURE 10

SN52702A
LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY
(for various lag compensations)

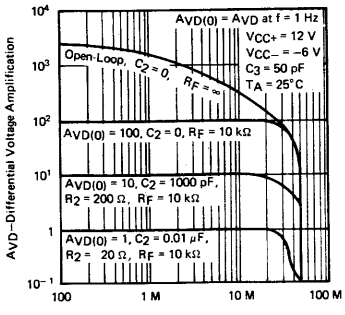
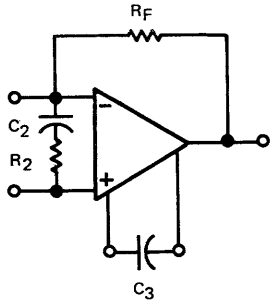


FIGURE 11



LEAD-LAG COMPENSATION CIRCUIT FOR FIGURE 11

3

TYPICAL CHARACTERISTICS

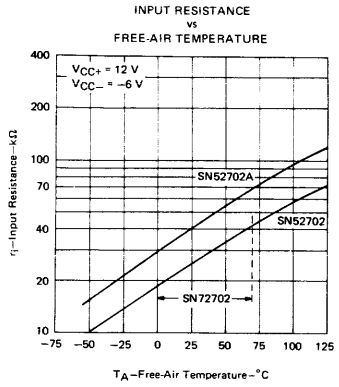


FIGURE 12

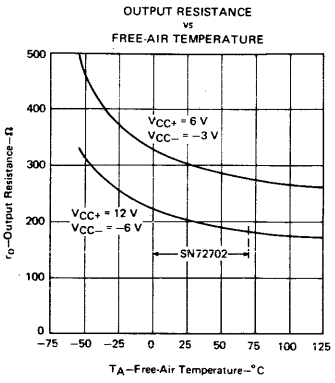


FIGURE 13

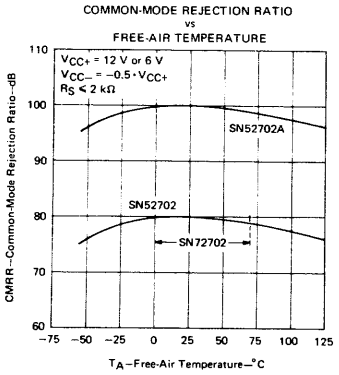


FIGURE 14

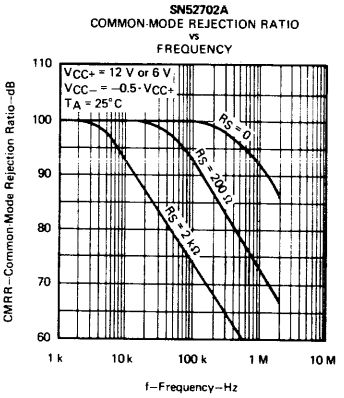


FIGURE 15

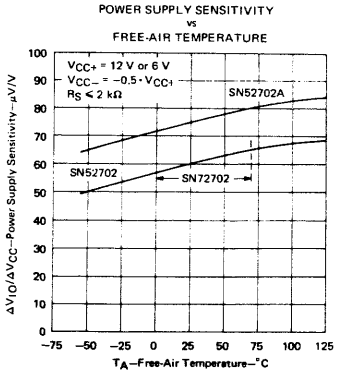


FIGURE 16

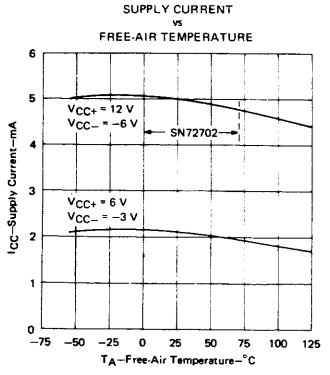


FIGURE 17

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN52709A, SN52709, SN72709 HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

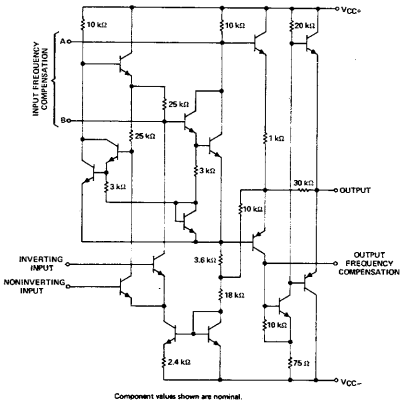
SERIES 52/72 OPERATIONAL AMPLIFIERS
featuring

- Common-Mode Input Range . . . ±10 V Typical
- Designed to be Interchangeable with Fairchild μA709A, μA709, and μA709C
- Maximum Peak-to-Peak Output Voltage Swing . . . 28 V Typical with 15 V Supplies

description

These circuits are high-performance operational amplifiers, each having high-impedance differential inputs and a low-impedance output. Component matching, inherent with silicon monolithic circuit-fabrication techniques, produces an amplifier with low-drift and low-offset characteristics. Provisions are incorporated within the circuit whereby external components may be used to compensate the amplifier for stable operation under various feedback or load conditions. These amplifiers are particularly useful for applications requiring transfer or generation of linear or nonlinear functions.

schematic

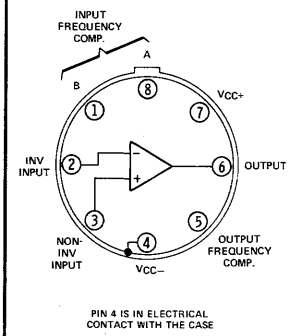


The SN52709A circuit features improved offset characteristics, reduced input-current requirements, and lower power dissipation when compared to the SN52709 circuit. In addition, maximum values of the average temperature coefficients of offset voltage and current are guaranteed.

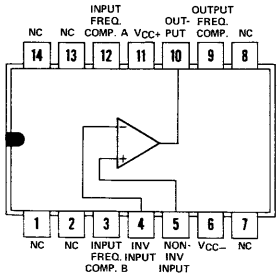
The SN52709A and SN52709 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN72709 is characterized for operation from 0°C to 70°C.

terminal assignments

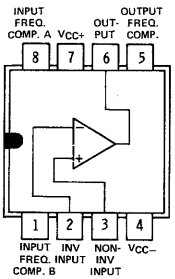
L — PLUG-IN PACKAGE (TOP VIEW)



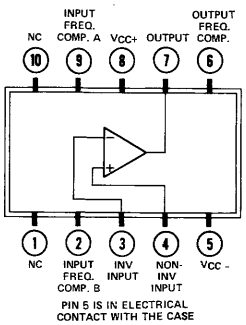
N — DUAL-IN-LINE PACKAGE (TOP VIEW)



P — DUAL-IN-LINE PACKAGE (TOP VIEW)



S — FLAT PACKAGE (TOP VIEW)



NC—No internal connection

voltages specified

Throughout this data sheet, supply voltages are specified either as a range or as a specific value. A positive voltage within the specified range (or of the specified value) is applied to V_{CC+}, and an equal negative voltage is applied to V_{CC-}.

CIRCUIT TYPES SN52709A, SN52709, SN72709
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52709A, SN52709	SN72709	UNIT
Supply voltage V_{CC+} (see Note 1)		18	18	V
Supply voltage V_{CC-} (see Note 1)		−18	−18	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Notes 1 and 3)		±10	±10	V
Duration of output short-circuit (see Note 4)		5	5	s
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 5)		300	300	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	L or S Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 10 volts, whichever is less.
4. The output may be shorted to ground or either power supply.
5. For operation of SN52709A and SN52709 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

3

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±9 V to ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN52709A			SN52709			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ		25°C		0.6	2		1	5	mV
				Full range			3			6	
α_{VIO}	Average temperature coefficient of input offset voltage	R_S = 50 Ω		Full range		1.8	10		3		μV/°C
		R_S = 10 kΩ		−55°C to 25°C		4.8	25		6		
				25°C to 125°C		2	15		6		
I_{IO}	Input offset current			25°C		10	50		50	200	nA
				−55°C		40	250		100	500	
				125°C		3.5	50		20	200	
α_{IIO}	Average temperature coefficient of input offset current			−55°C to 25°C		0.45	2.8				nA/°C
				25°C to 125°C		0.08	0.5				
I_{IB}	Input bias current			25°C		0.1	0.2		0.2	0.5	μA
				−55°C		0.3	0.6		0.5	1.5	
V_I	input voltage range	$V_{CC\pm}$ = ±15 V		25°C	±8	±10		±8	±10		V
				Full range	±8			±8			
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V,	$R_L \geqslant 10$ kΩ	25°C	24	28		24	28		V
				Full range	24			24			
		$V_{CC\pm}$ = ±15 V,	R_L = 2 kΩ	25°C	20	26		20	26		
		$V_{CC\pm}$ = ±15 V,	$R_L \geqslant 2$ kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V	$R_L \geqslant 2$ kΩ,	25°C		45,000			45,000		
				Full range	25,000		70,000	25,000		70,000	
r_i	Input resistance			25°C	350	750		150	400		kΩ
				−55°C	85	185		40	100		
r_o	Output resistance	V_O = 0,	See Note 6	25°C		150			150		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ		25°C	80	110		70	90		dB
				Full range	80			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10$ kΩ		25°C		40	100		25	150	μV/V
				Full range			100			150	
I_{CC}	Supply current	$V_{CC\pm}$ = ±15 V, No signal	No load,	25°C		2.5	3.6		2.6	5.5	mA
				−55°C		2.7	4.5				
				125°C		2.1	3				
P_D	Total power dissipation	$V_{CC\pm}$ = ±15 V, No signal	No load,	25°C		75	108		78	165	mW
				−55°C		81	135				
				125°C		63	90				

†All characteristics are specified under open-loop operation. Full range for SN52709A and SN52709 is −55°C to 125°C.

‡All typical values are at $V_{CC\pm}$ = ±15 V.

Note 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics at specified free-air temperature (unless otherwise noted $V_{CC\pm}$ = ±15 V)

PARAMETER		TEST CONDITIONS†			SN72709 MIN	SN72709 TYP	SN72709 MAX	UNIT
V_{IO}	Input offset voltage	$V_{CC\pm}$ = ±9 V to ±15 V, $R_S \leq 10$ kΩ		25°C		2	7.5	mV
				Full range			10	
I_{IO}	Input offset current	$V_{CC\pm}$ = ±9 V to ±15 V		25°C		100	500	nA
				Full range			750	
I_{IB}	Input bias current	$V_{CC\pm}$ = ±9 V to ±15 V		25°C		0.3	1.5	μA
				Full range			2	
V_I	Input voltage range			25°C	±8	±10		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 10$ kΩ		25°C	24	28		V
				Full range	24			
		R_L = 2 kΩ		25°C	20	26		
		$R_L \geq 2$ kΩ		Full range	20			
A_{VD}	Large-signal differential voltage amplification	$R_L \leq 2$ kΩ,	V_O = ±10 V	25°C	15,000	45,000		
				Full range	12,000			
r_i	Input resistance			25°C	50	250		kΩ
				Full range	35			
r_o	Output resistance	V_O = 0,	See Note 6	25°C		150		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ		25°C	65	90		dB
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10$ kΩ		25°C		25	200	μV/V
P_D	Total power dissipation	No load,	No signal	25°C		80	200	mW

†All characteristics are specified under open-loop operation. Full range for SN72709 is 0°C to 70°C.
NOTE 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics $V_{CC\pm}$ = ±9 V to ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			SN52709A SN52709 SN72709 MIN	SN52709A SN52709 SN72709 TYP	SN52709A SN52709 SN72709 MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ,	See Figure 2	C_L = 0		0.3	1	μs
	Overshoot			C_L = 100 pF		6%	30%	

THERMAL INFORMATION

SN52709A, SN52709
DISSIPATION DERATING CURVE

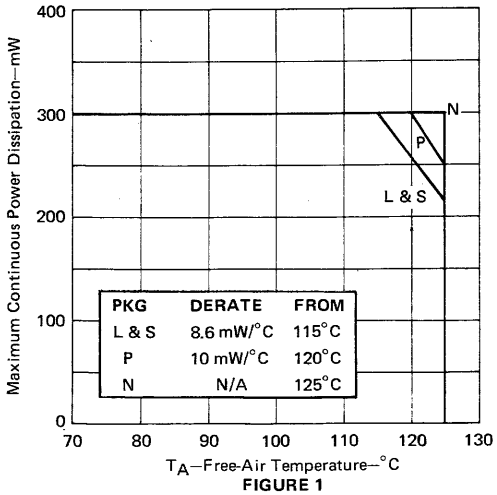


FIGURE 1

PARAMETER MEASUREMENT INFORMATION

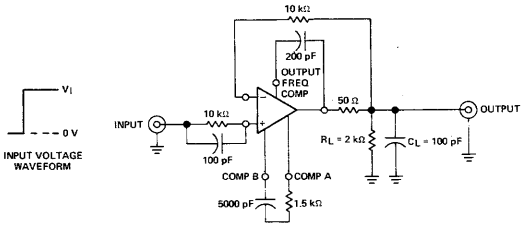


FIGURE 2—RISE TIME AND SLEW RATE

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left|\frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Average Temperature Coefficient Of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

3

$$\alpha_{IIO} = \left|\frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Power Supply Sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) The ratio of the change in input offset voltage to the change in supply voltages producing it. For these devices, both supply voltages are varied symmetrically.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Overshoot The quotient of: (1) the largest deviation of the output signal value from its steady-state value after a step-function change of the input signal, and (2) the difference between the output signal values in the steady state before and after the step-function change of the input signal.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS
(unless designated maximum or minimum)

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

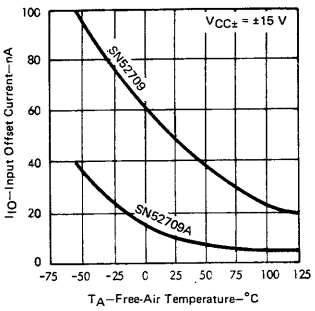


FIGURE 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

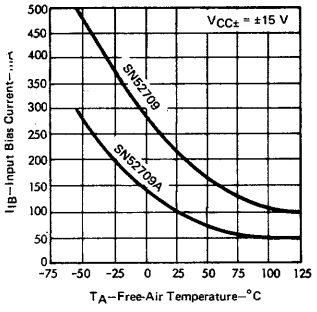


FIGURE 4

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

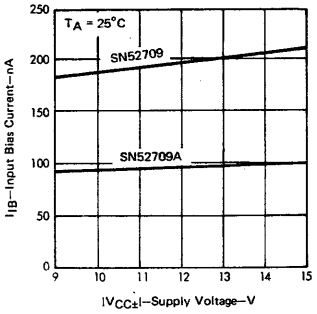


FIGURE 5

INPUT VOLTAGE RANGE
vs
SUPPLY VOLTAGE

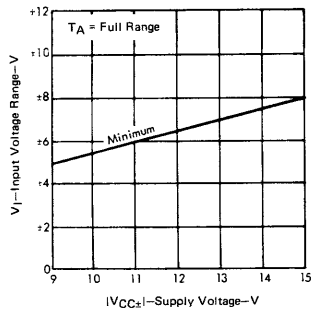


FIGURE 6

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

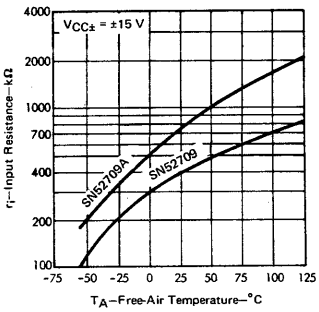


FIGURE 7

SN52709A
COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

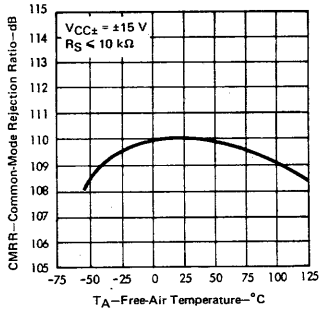


FIGURE 8

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

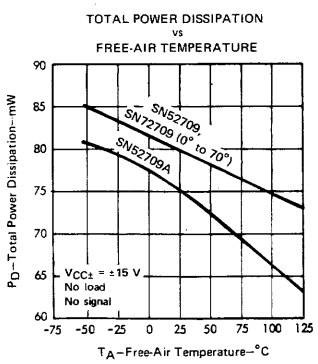


FIGURE 9

SN52709A
TOTAL POWER DISSIPATION
vs
SUPPLY VOLTAGE

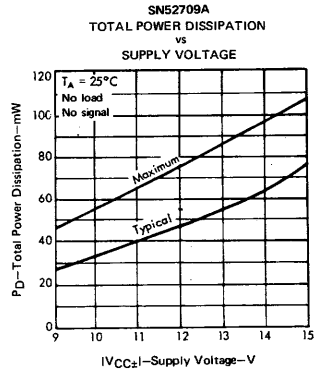


FIGURE 10

SN52709, SN72709
TOTAL POWER DISSIPATION
vs
SUPPLY VOLTAGE

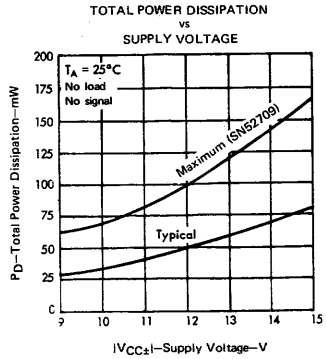


FIGURE 11

TYPICAL CHARACTERISTICS
(unless designated maximum or minimum)

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

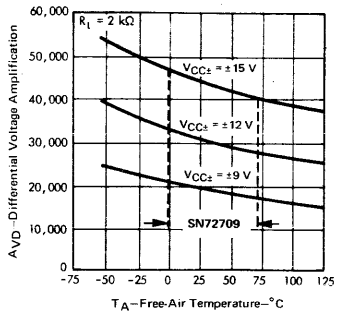


FIGURE 12

SN52709A, SN52709
OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

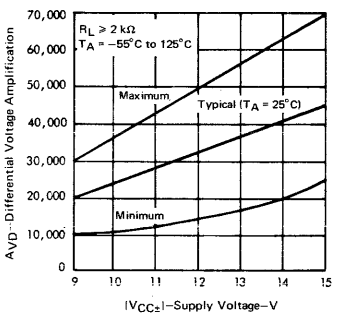


FIGURE 13

SN72709
OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

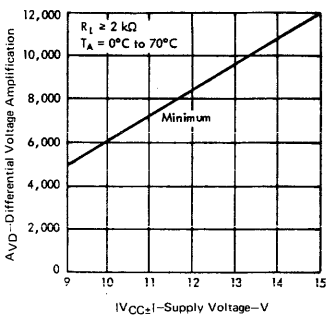


FIGURE 14

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

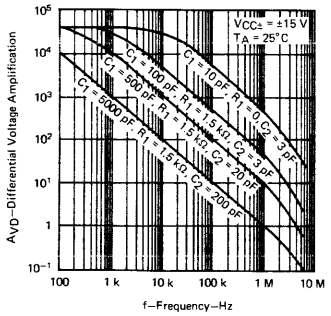


FIGURE 15

CLOSED-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

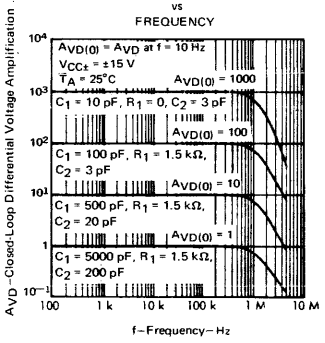
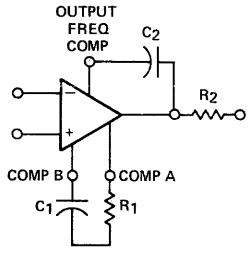


FIGURE 16



When the amplifier is operated with capacitive loading, R_2 = 50 Ω.

FREQUENCY COMPENSATION CIRCUIT FOR FIGURES 15, 16, AND 19

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

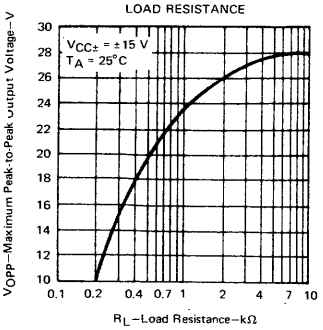


FIGURE 17

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

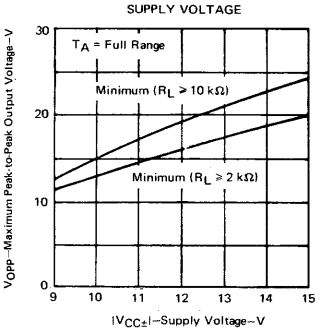


FIGURE 18

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

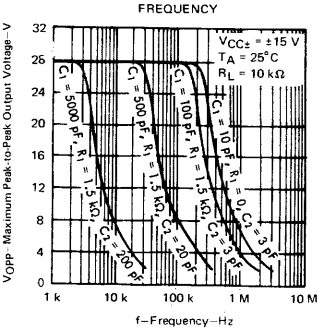


FIGURE 19

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

SN52709A, SN52709
VOLTAGE TRANSFER CHARACTERISTICS

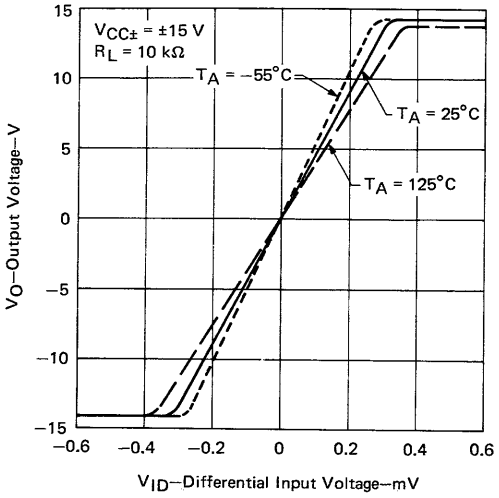


FIGURE 20

SN72709
VOLTAGE TRANSFER CHARACTERISTICS

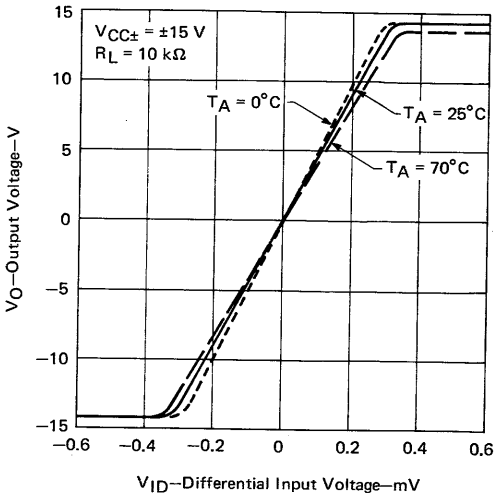


FIGURE 21

RELATIVE OUTPUT SWING vs ELAPSED TIME

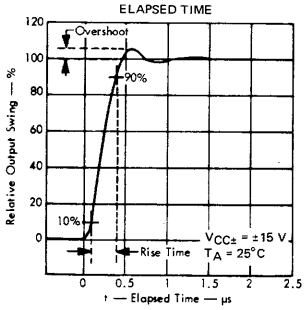


FIGURE 22

SLEW RATE vs CLOSED-LOOP DIFFERENTIAL VOLTAGE AMPLIFICATION

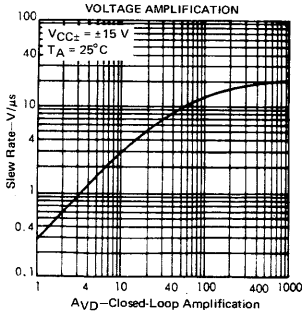


FIGURE 23

NORMALIZED FREQUENCY CHARACTERISTICS vs FREE-AIR TEMPERATURE

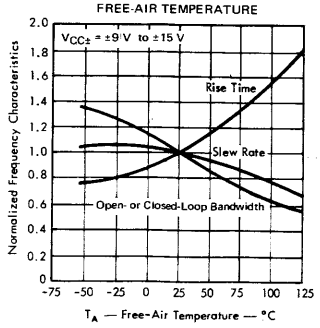


FIGURE 24

NORMALIZED FREQUENCY CHARACTERISTICS vs SUPPLY VOLTAGE

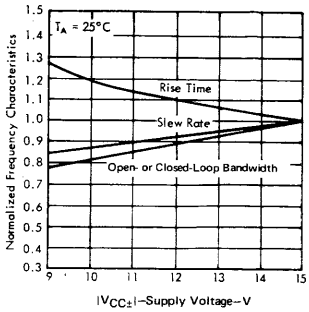


FIGURE 25

PRINTED IN U.S.A.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN52741, SN72741
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up
- Same Pin Assignments as SN52709/SN72709

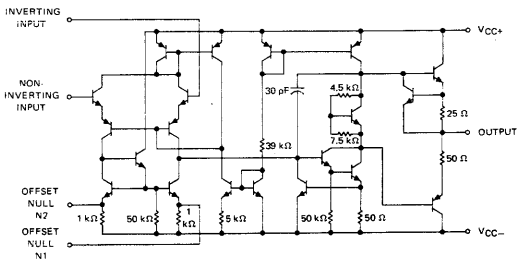
description

The SN52741 and SN72741 are high-performance operational amplifiers, featuring offset-voltage null capability.

The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 11.

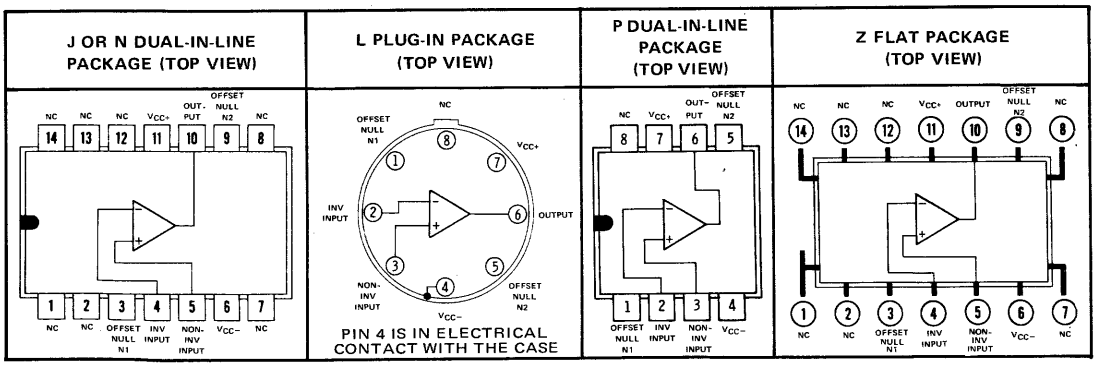
The SN52741 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72741 is characterized for operation from 0°C to 70°C.

schematic



COMPONENT VALUES SHOWN ARE NOMINAL

terminal assignments



NC—No internal connection

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52741	SN72741	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52741 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 12.

3

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52741			SN72741			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ	25°C		1	5		1	6	mV
			Full range			6			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range		25°C		±15			±15		mV
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	24	28		24	28		V
		$R_L \geq$ 10 kΩ	Full range	24			24			
		R_L = 2 kΩ	25°C	20	26		20	26		
		$R_L \geq$ 2 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ±10 V	25°C	50,000	200,000		20,000	200,000		
			Full range	25,000			15,000			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0 V, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10$ kΩ	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load, No signal	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	No load, No signal	25°C		50	85		50	85	mW
			Full range			100			100	

†All characteristics are specified under open-loop operation. Full range for SN52741 is −55°C to 125°C and for SN72741 is 0°C to 70°C.
NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52741			SN72741			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.3			0.3		μs
	Overshoot			5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5			0.5		V/μs

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

3

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which, if exceeded at either input terminal, will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between the output terminal and ground.

Input Capacitance (C_i) The capacitance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Power Supply Sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) The ratio of the change in input offset voltage to the change in supply voltages producing it. For these devices, both supply voltages are varied symmetrically.

Short-Circuit Output Current (I_{OS}) The maximum output current available from the amplifier with the output shorted to ground or to either supply.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Overshoot The quotient of: (1) the largest deviation of the output signal value from its steady-state value after a step-function change of the input signal, and (2) the difference between the output signal values in the steady state before and after the step-function change of the input signal.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output voltage for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

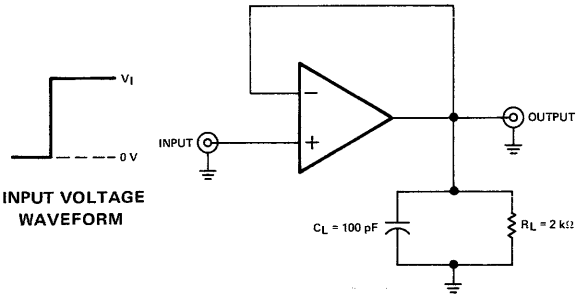


FIGURE 1–RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL CHARACTERISTICS

3

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

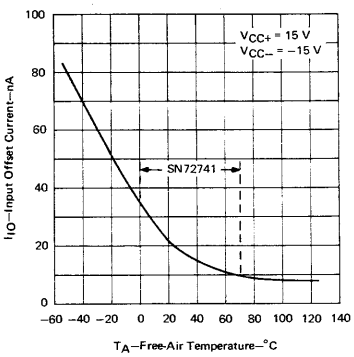


FIGURE 2

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

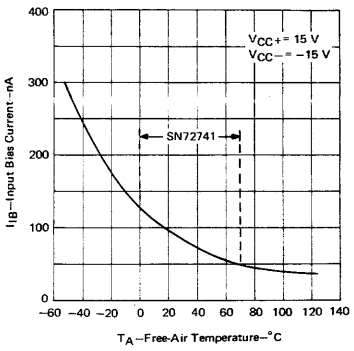


FIGURE 3

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

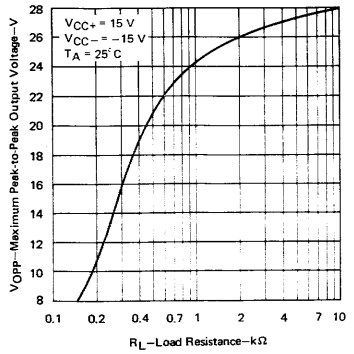


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

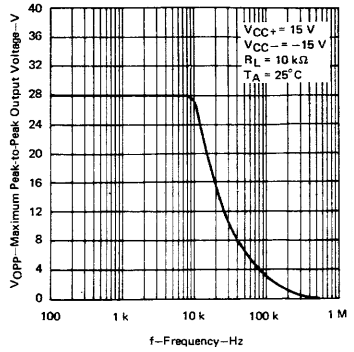


FIGURE 5

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

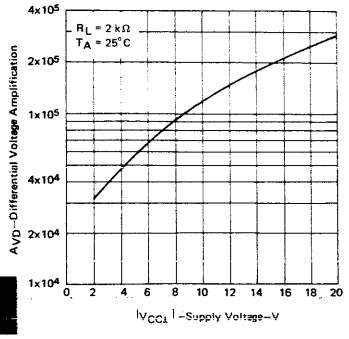


FIGURE 6

COMMON-MODE REJECTION RATIO vs FREQUENCY

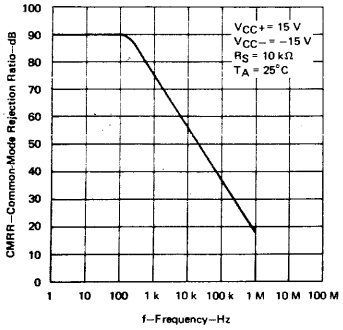


FIGURE 8

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

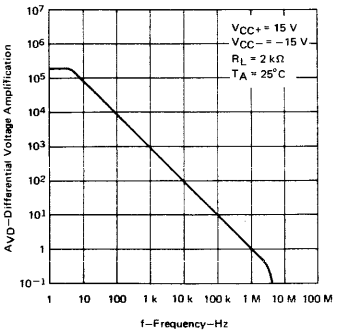


FIGURE 7

OUTPUT VOLTAGE vs ELAPSED TIME

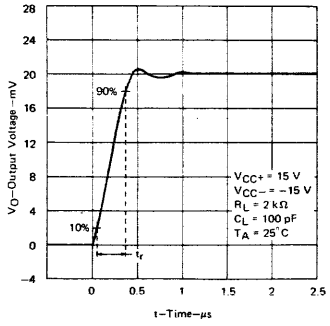


FIGURE 9

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

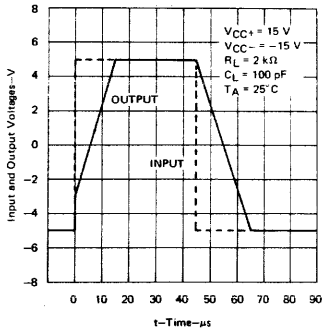


FIGURE 10

TYPICAL APPLICATION DATA

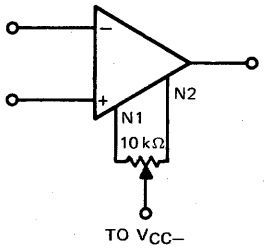
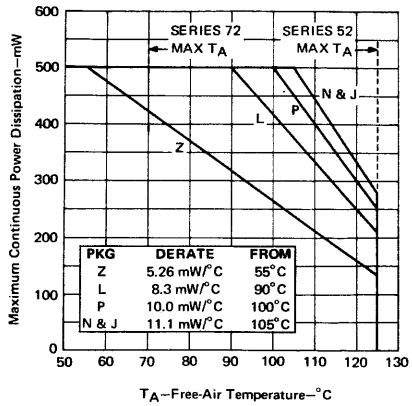


FIGURE 11–INPUT OFFSET VOLTAGE NULL CIRCUIT

THERMAL INFORMATION

DISSIPATION DERATING CURVE



PKG	DERATE	FROM
Z	5.26 mW/°C	55°C
L	8.3 mW/°C	90°C
P	10.0 mW/°C	100°C
N & J	11.1 mW/°C	105°C

FIGURE 12

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN52747, SN72747
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

- No frequency Compensation Required
- Low Power Consumption
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- No Latch-up
- Designed to be Interchangeable with Fairchild μA747 and μA747C

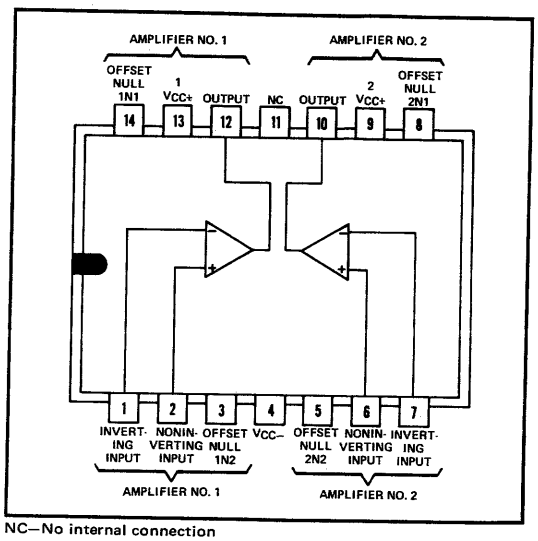
description

The SN52747 and SN72747 are dual high-performance operational amplifiers, featuring offset-voltage null capability. Each half is electrically similar to SN52741/SN72741.

The high common-mode input voltage range and the absence of latch-up make the amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 3.

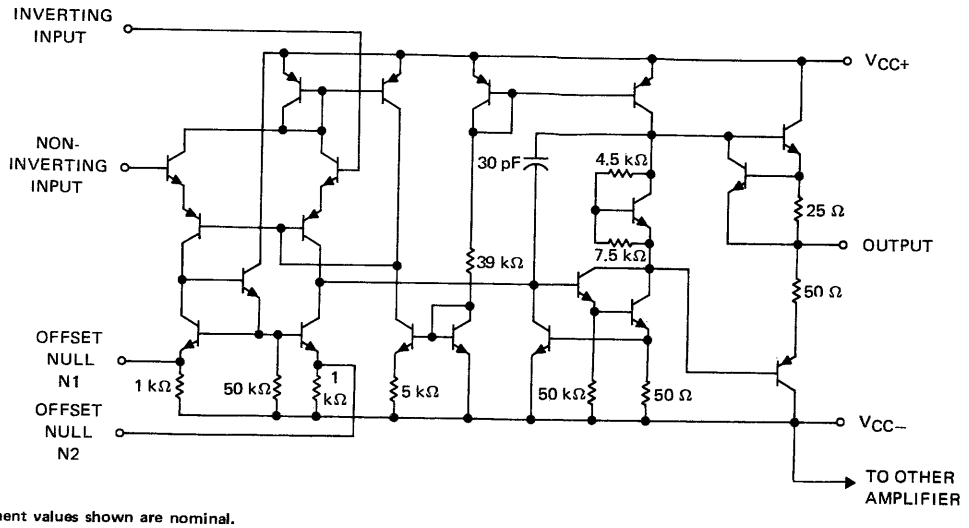
The SN52747 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72747 is characterized for operation from 0°C to 70°C.

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

schematic (each amplifier)



Component values shown are nominal.

CIRCUIT TYPES SN52747, SN72747
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52747	SN72747	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 5)	Each amplifier	500	500	mW
	Total package	800	800	
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52747 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation of SN52747 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 2.

3

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52747			SN72747			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10\ k\Omega$	25°C		1	5		1	6	mV
			Full range			6			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range		25°C		±15			±15		mV
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	24	28		24	28		V
		$R_L \geq$ 10 kΩ	Full range	24			24			
		R_L = 2 kΩ	25°C	20	26		20	26		
		$R_L \geq$ 2 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ±10 V	25°C	50,000	200,000		50,000	200,000		
			Full range	25,000			25,000			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0 V, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$R_S \leq 10\ k\Omega$	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10\ k\Omega$	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load, No signal	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Power dissipation (each amplifier)	No load, No signal	25°C		50	85		50	85	mW
			Full range			100			100	
V_{o1}/V_{o2}	Channel separation		25°C		120			120		dB

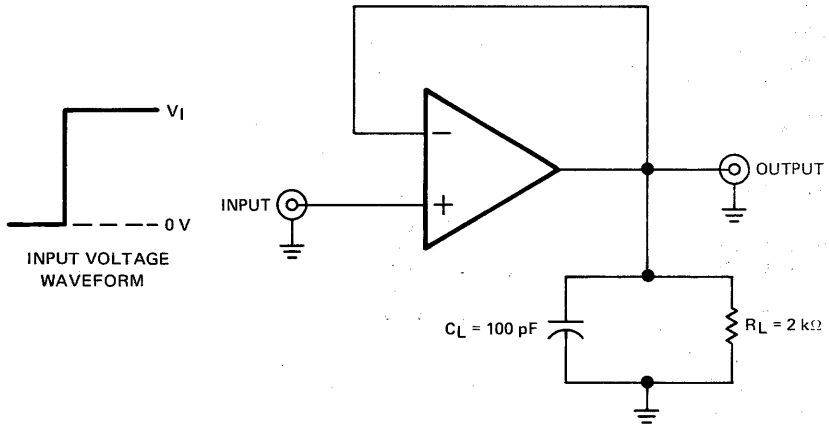
† All characteristics are specified under open-loop operation. Full range for SN52747 is −55°C to 125°C and for SN72747 is 0°C to 70°C.
NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.
For definitions of terms, mechanical data, and ordering instructions, see the SN52741/SN72741 data sheet dated November 1970.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52747			SN72747			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ,		0.3			0.3		μs
	Overshoot	C_L = 100 pF, See Figure 1		5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

FIGURE 1–RISE TIME, OVERSHOOT, AND SLEW RATE

THERMAL INFORMATION

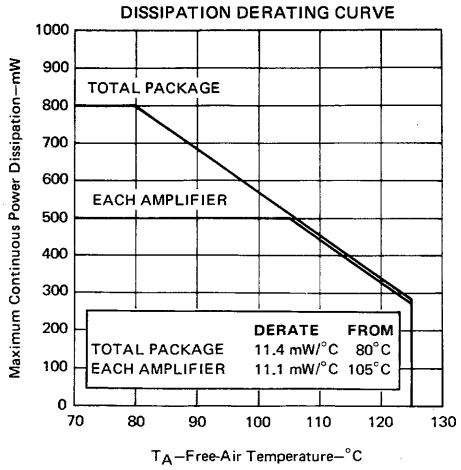


FIGURE 2

TYPICAL APPLICATION DATA

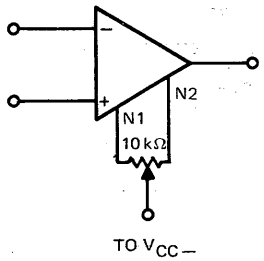


FIGURE 3–INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

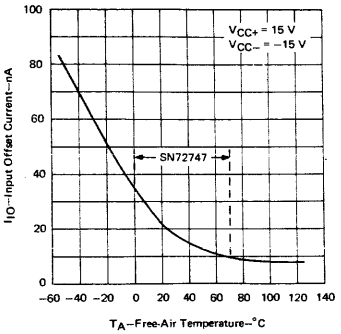


FIGURE 4

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

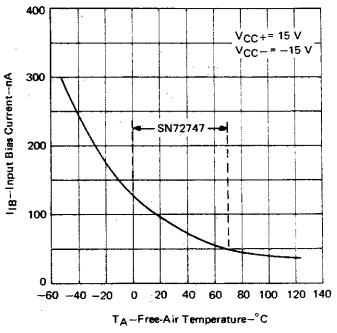


FIGURE 5

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

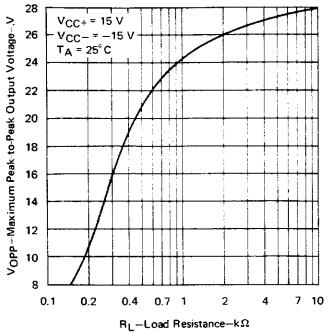


FIGURE 6

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

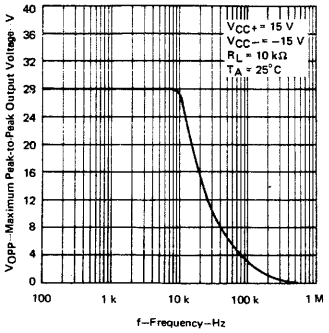


FIGURE 7

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

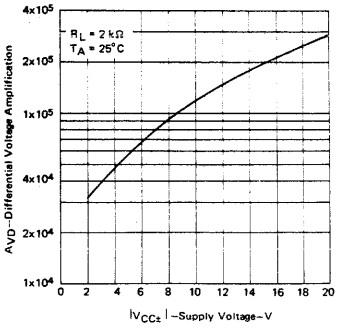


FIGURE 8

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

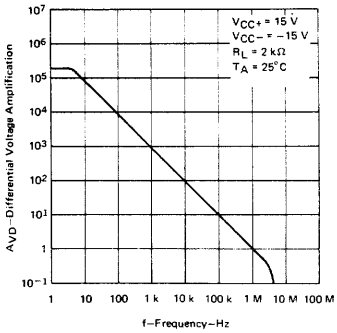


FIGURE 9

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

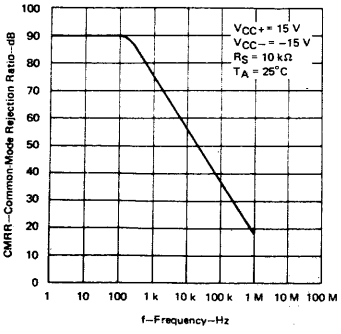


FIGURE 10

OUTPUT VOLTAGE
vs
ELAPSED TIME

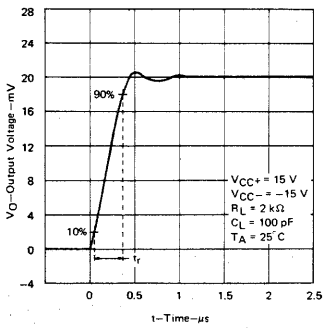


FIGURE 11

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

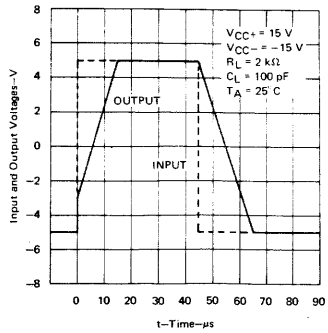


FIGURE 12

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN52748, SN72748
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

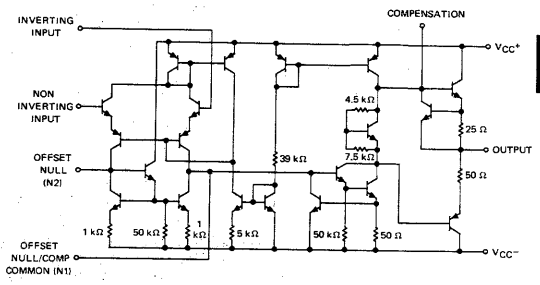
- Frequency and Transient Response Characteristics Adjustable
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-up
- Same Pin Assignments as SN52709/SN72709

description

The SN52748 and SN72748 are high-performance operational amplifiers. They offer the same advantages and desirable features as the SN52741 and SN72741 with the exception of internal compensation. The external compensation of the SN52748 and SN72748 allows the changing of the frequency response (when the closed-loop gain is greater than unity) for applications requiring wider bandwidth or higher slew rate. These circuits feature high gain, large differential and common-mode input voltage range, output short-circuit protection, and may be compensated under unity-gain conditions with a single 30-pF capacitor. A potentiometer may be connected between the offset null inputs, as shown in Figure 12, to null out the offset voltage.

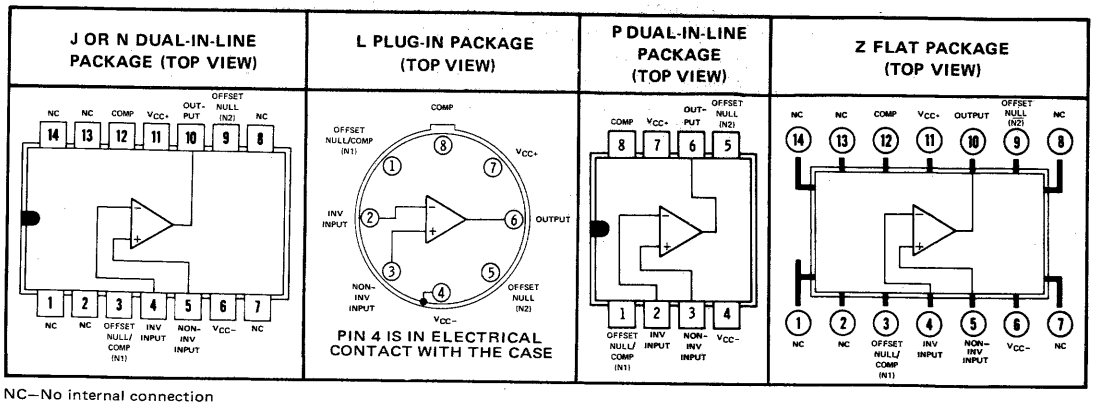
The SN52748 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72748 is characterized for operation from 0°C to 70°C.

schematic



COMPONENT VALUES SHOWN ARE NOMINAL

terminal assignments



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52748	SN72748	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52748 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 13.

3

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52748			SN72748			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ	25°C		1	5		1	6	mV
			Full range			6			7.5	
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	24	28		24	28		V
		$R_L \geq$ 10 kΩ	Full range	24			24			
		R_L = 2 kΩ	25°C	20	26		20	26		
		$R_L \geq$ 2 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ±10 V	25°C	50,000	200,000		50,000	200,000		
			Full range	25,000			25,000			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0 V, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10$ kΩ	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load, No signal	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	No load, No signal	25°C		50	85		50	85	mW
			Full range			100			100	

† All characteristics are specified under open-loop operation. Full range for SN52748 is −55°C to 125°C and for SN72748 is 0°C to 70°C.
NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

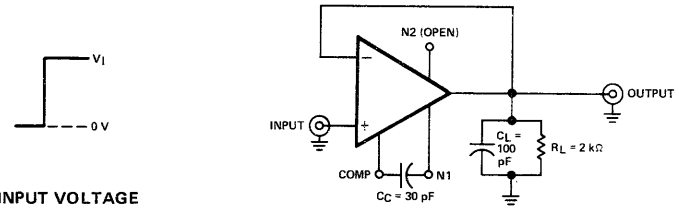
For definitions of terms, mechanical data, and ordering instructions, see SN52741/SN72741 data sheet dated November, 1970.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52748			SN72748			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, C_C = 30 pF, See Figure 1		0.3			0.3		μs
	Overshoot			5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, C_C = 30 pF, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION



INPUT VOLTAGE WAVEFORM

TEST CIRCUIT

FIGURE 1—RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

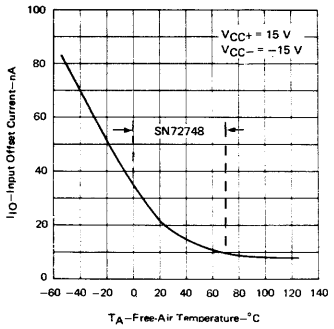


FIGURE 2

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

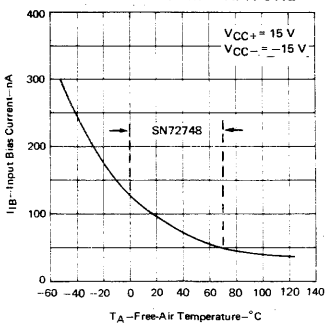


FIGURE 3

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

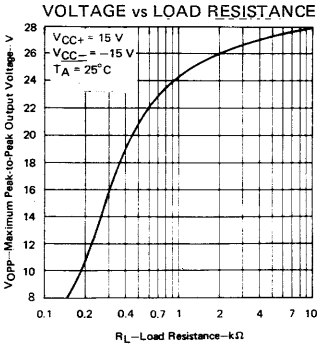


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

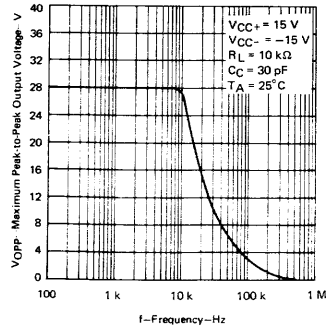


FIGURE 5

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

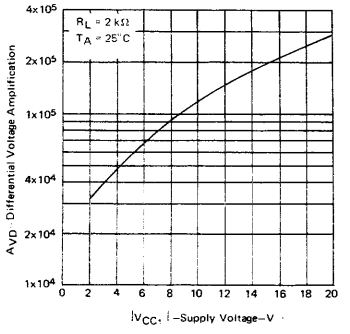


FIGURE 6

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

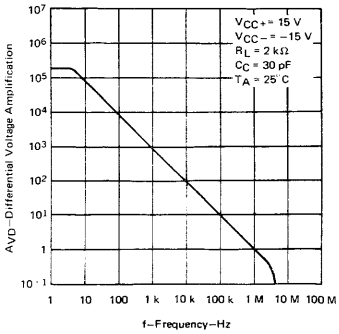


FIGURE 7

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREQUENCY

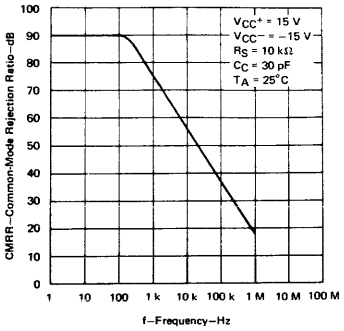


FIGURE 8

OUTPUT VOLTAGE vs ELAPSED TIME

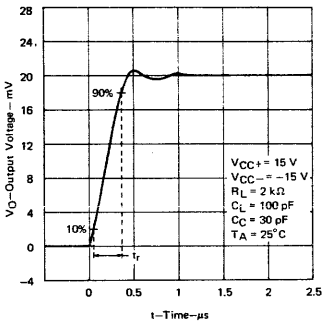


FIGURE 9

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

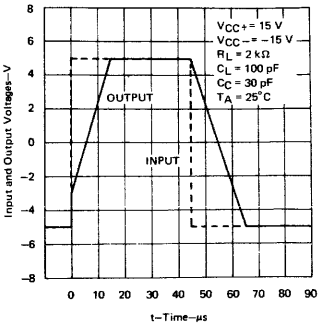
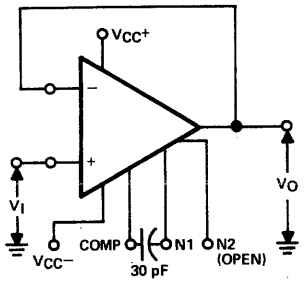


FIGURE 10

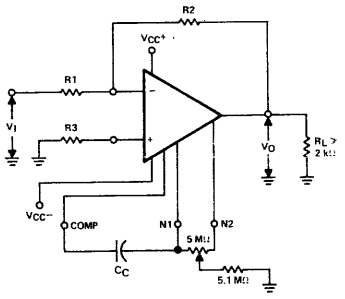
3

TYPICAL APPLICATION DATA



r_i = 400 MΩ, $r_o < 1\ \Omega$,
C_i = 1 pF, BW = 1 MHz

FIGURE 11—UNITY-GAIN VOLTAGE FOLLOWER



$$\frac{V_O}{V_I} = -\frac{R2}{R1}$$

$$C_C \geq \frac{R1 \cdot 30\ pF}{R1+R2}$$

$$R3 = \frac{R1 \cdot R2}{R1+R2}$$

FIGURE 12—INVERTING CIRCUIT WITH ADJUSTABLE GAIN, COMPENSATION, AND OFFSET ADJUSTMENT

THERMAL INFORMATION

DISSIPATION DERATING CURVE

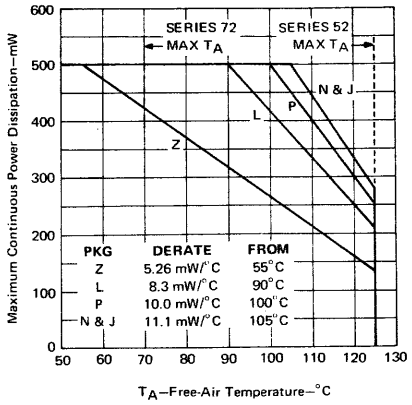


FIGURE 13

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN52770, SN72770
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

- Adjustable Frequency and Transient Response Characteristics
- Offset-Voltage Null Capability
- No Latch-Up
- Low Power Consumption
- High Slew Rates
- Very Low Input Bias Currents
- Very Low Input Offset Parameters
- Short-Circuit Protection
- Large Common-Mode and Differential Voltage Ranges

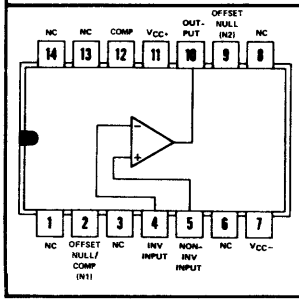
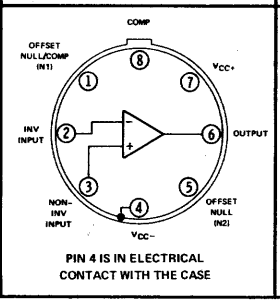
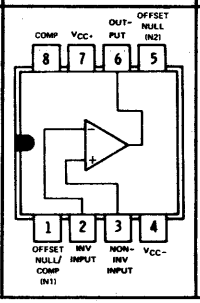
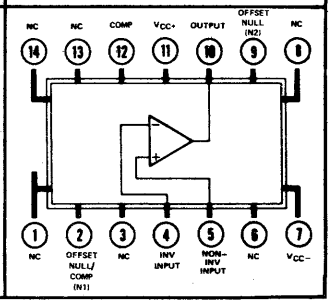
description

The SN52770 and SN72770 are high-performance general purpose integrated-circuit operational amplifiers. They offer the same advantages and desirable features as the SN52771 and SN72771 with the exception of internal compensation. The external compensation of the SN52770 and SN72770 allows the changing of the frequency response (when the closed-loop gain is greater than unity) for applications requiring wider bandwidth or higher slew rate. Unity-gain compensation is accomplished by means of a single 30-pF capacitor, and for higher gains, smaller capacitors may be used to obtain increased slew rate and bandwidth. High slew rate makes these amplifiers ideal for fast-rise-time signals, or large signals at high frequency. Very low input currents make them ideal for sample and hold, logarithmic amplifiers, and other low-level applications. A potentiometer may be connected between the offset null inputs, as shown in Figure 12, to null out the offset voltage.

The SN52770 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72770 is characterized for operation from 0°C to 70°C.

3

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	P DUAL-IN-LINE PACKAGE (TOP VIEW)	Z FLAT PACKAGE (TOP VIEW)
			

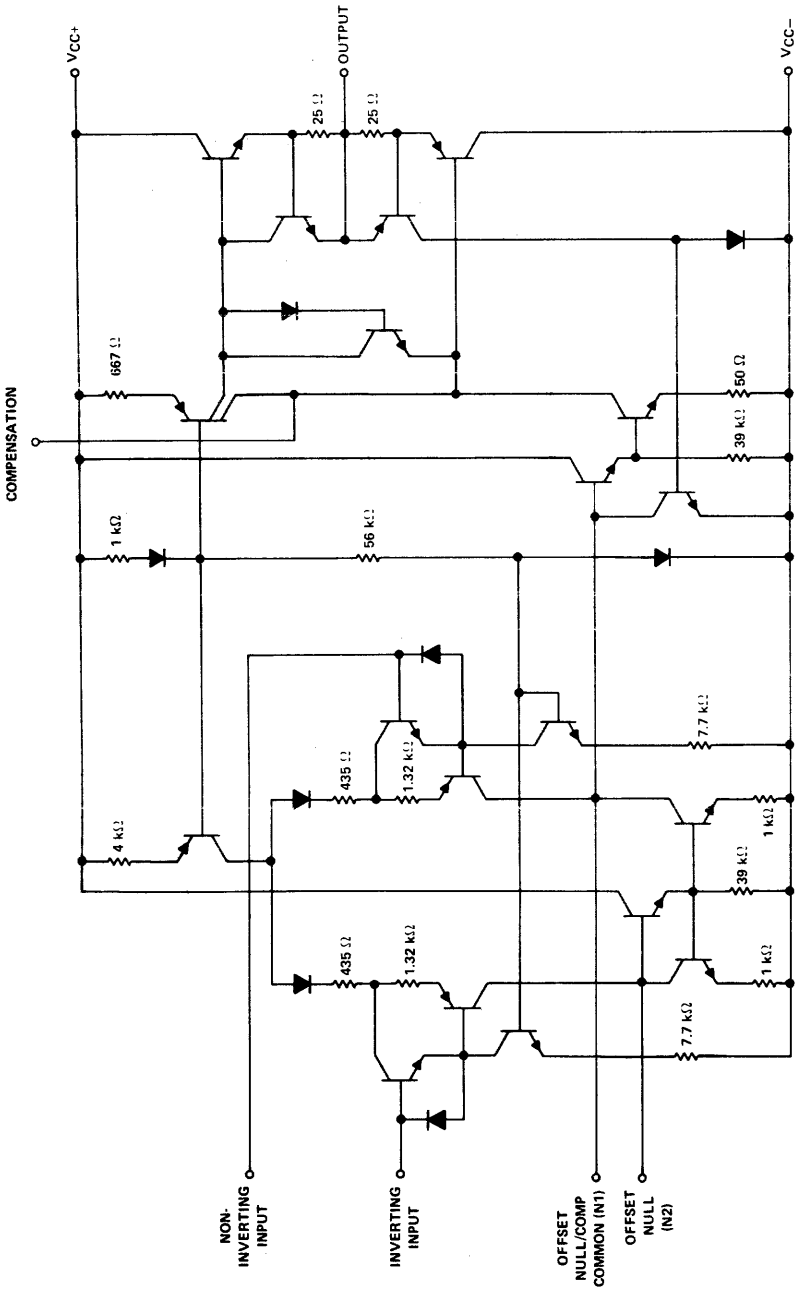
NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52770	SN72770	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52770 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

schematic



Component values shown are nominal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52770			SN72770			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ	25°C		2	4		5	10	mV
			Full range			7			14	
I_{IO}	Input offset current		25°C		1	2		5	10	nA
			Full range			5			14	
I_{IB}	Input bias current		25°C		8	15		15	30	nA
			Full range			35			40	
V_{ICR}	Common-mode input voltage range		25°C	±12	±14		±11			V
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 2 kΩ	25°C	24	26.5		22	26.5		
		$R_L \geq$ 2 kΩ	Full range	24			22			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, V_O = ±10 V	25°C	50,000	100,000		35,000	100,000		
		$R_L \geq$ 2 kΩ, V_O = ±10 V	Full range	25,000			25,000			
B_{OM}	Maximum-output-swing bandwidth (closed loop)	R_L = 2 kΩ, $V_O \geq$ ± 10 V, A_{VD} = 1, THD ≤ 5%	25°C		40			40		kHz
B_1	Unity-gain bandwidth		25°C		1.3			1.3		MHz
r_{id}	Differential input resistance		25°C		100			100		MΩ
z_{ic}	Common-mode input impedance	f = 10 Hz	25°C		500			500		MΩ
z_o	Output impedance	f = 10 Hz	25°C		2			2		kΩ
CMRR	Common-mode rejection ratio	$R_S \leq$ 10 kΩ	25°C	80	100		70	100		dB
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq$ 10 kΩ	25°C		80	150			200	μV/V
e_n	Equivalent input noise voltage (closed loop)	A_{VD} = 100, BW = 1 Hz, f = 1 kHz	25°C		40			40		nV/√Hz
I_{OS}	Short-circuit output current	To V_{CC+}	25°C		24			24		mA
		To V_{CC-}			−20			−20		
I_{CC}	Supply current	No load, No signal	25°C		1.3	2		1.7	4	mA
P_D	Total power dissipation	No load, No signal	25°C		40	60		50	120	mW

†All characteristics are specified under open-loop operation unless otherwise noted. Full range for SN52770 is −55°C to 125°C and for SN72770 is 0°C to 70°C.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52770			SN72770			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 200 mV, R_L = 2 kΩ, C_L = 200 pF, C_C = 30 pF, See Figure 2		130			130		ns
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 200 pF, C_C = 30 pF, See Figure 2		2.5			2.5		V/μs

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Common-Mode Input Voltage Range (V_{ICR}) The range of common-mode voltage which if exceeded will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

3

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Maximum-Output-Swing Bandwidth (B_{OM}) The range of frequencies within which the maximum output voltage swing is above a specified value.

Unity-Gain Bandwidth (B_1) The range of frequencies within which the voltage amplification is greater than unity.

Differential Input Resistance (r_{id}) The small-signal resistance between the two ungrounded input terminals.

Common-Mode Input Impedance (z_{ic}) The parallel sum of the small-signal impedances between each input terminal and ground.

Output Impedance (z_o) The small-signal impedance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Power Supply Sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) The ratio of the change in input offset voltage to the change in supply voltages producing it. For these devices, both supply voltages are varied symmetrically.

Short-Circuit Output Current (I_{OS}) The maximum output current available from the amplifier with the output shorted to the specified supply.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output voltage for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

THERMAL INFORMATION

DISSIPATION DERATING CURVE

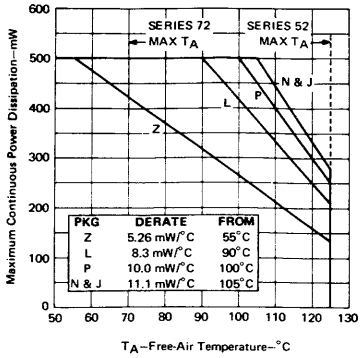
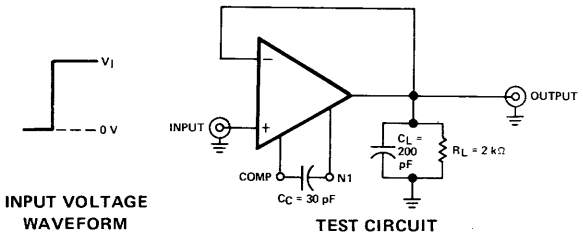


FIGURE 1

PARAMETER MEASUREMENT INFORMATION



INPUT VOLTAGE WAVEFORM

TEST CIRCUIT

FIGURE 2–BANDWIDTH, RISE TIME, AND SLEW RATE

3

TYPICAL CHARACTERISTICS

SN72770
COMMON-MODE INPUT VOLTAGE RANGE
vs
SUPPLY VOLTAGE

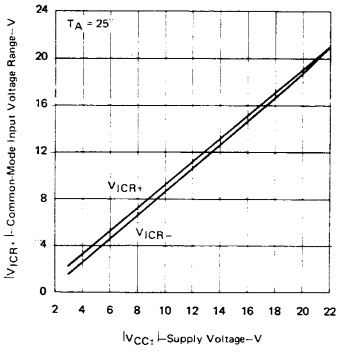


FIGURE 3

MAXIMUM OUTPUT VOLTAGE SWING
vs
SUPPLY VOLTAGE

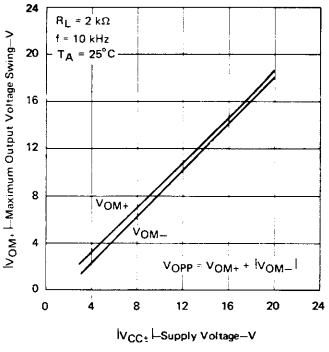


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE SWING
vs
FREQUENCY

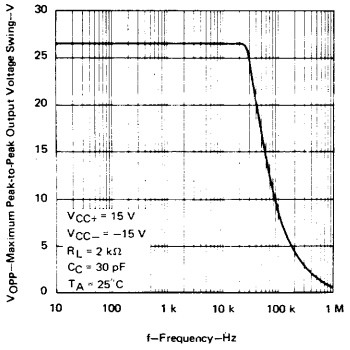


FIGURE 5

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

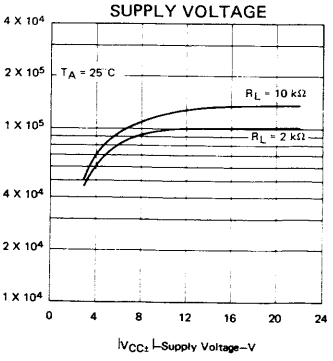


FIGURE 6

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

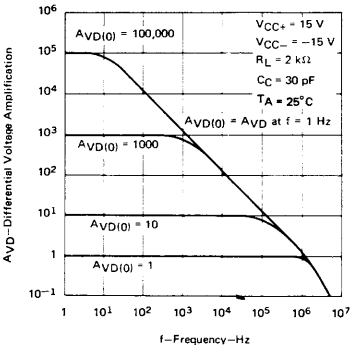


FIGURE 7

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

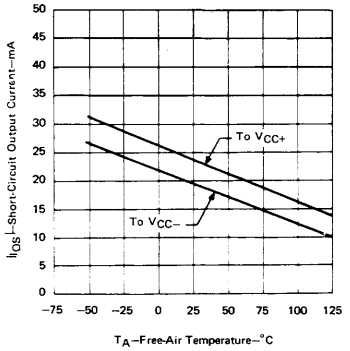


FIGURE 8

TYPICAL CHARACTERISTICS

TOTAL POWER DISSIPATION
vs
SUPPLY VOLTAGE

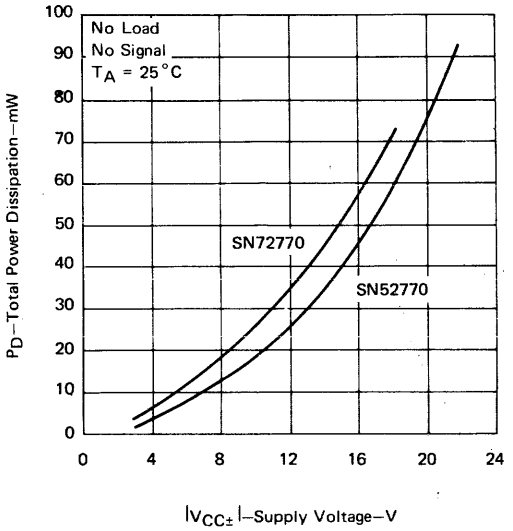


FIGURE 9

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

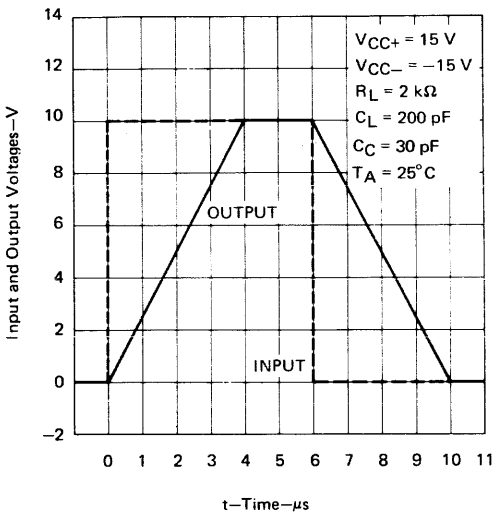
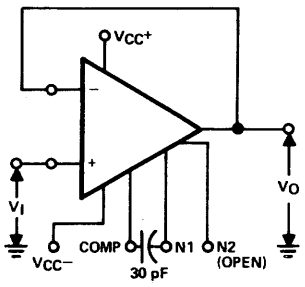


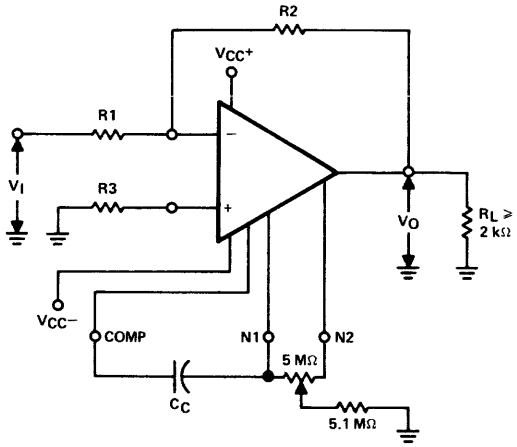
FIGURE 10

TYPICAL APPLICATION DATA



$r_i \approx 5{,}000$ MΩ at 10 Hz $r_o << 1$ Ω
$C_L \approx 1.5$ pF $B_1 \approx 1.3$ MHz

FIGURE 11–UNITY-GAIN VOLTAGE FOLLOWER



$$R3 = \frac{R1 \cdot R2}{R1 + R2} \qquad \frac{V_O}{V_1} = -\frac{R2}{R1} \qquad C_C \geq \frac{R1 \cdot 30\text{ pF}}{R1 + R2}$$

FIGURE 12–INVERTING CIRCUIT WITH ADJUSTABLE GAIN, COMPENSATION, AND OFFSET ADJUSTMENT

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN52771, SN72771
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

- Very Low Input Bias Currents
- 6-dB Roll-Off Insures Stability
- No Frequency Compensation Required
- Offset-Voltage Null Capability
- Low Power Consumption
- High Slew Rates
- Very Low Input Offset Parameters
- Short-Circuit Protection
- No Latch-Up
- Large Common-Mode and Differential Voltage Ranges

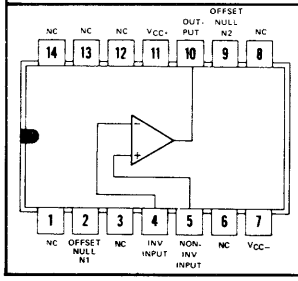
description

The SN52771 and SN72771 are high-performance general purpose integrated-circuit operational amplifiers. Very low input currents make these amplifiers ideal for sample and hold, logarithmic amplifiers, and other low-level applications. High slew rate makes them ideal for fast-rise-time signals, or large signals at high frequency. Internal compensation provides a 6-dB roll-off for stability under all closed-loop conditions. A potentiometer may be connected between the offset null inputs, as shown in Figure 11, to null out the offset voltage.

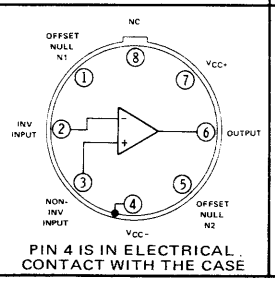
The SN52771 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72771 is characterized for operation from 0°C to 70°C.

terminal assignments

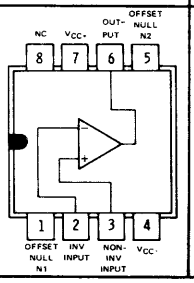
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



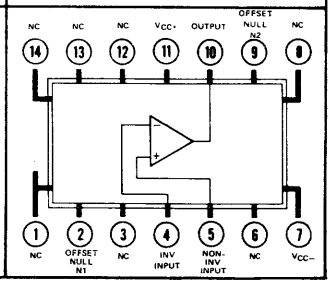
L PLUG-IN PACKAGE (TOP VIEW)



P DUAL-IN-LINE PACKAGE (TOP VIEW)



Z FLAT PACKAGE (TOP VIEW)



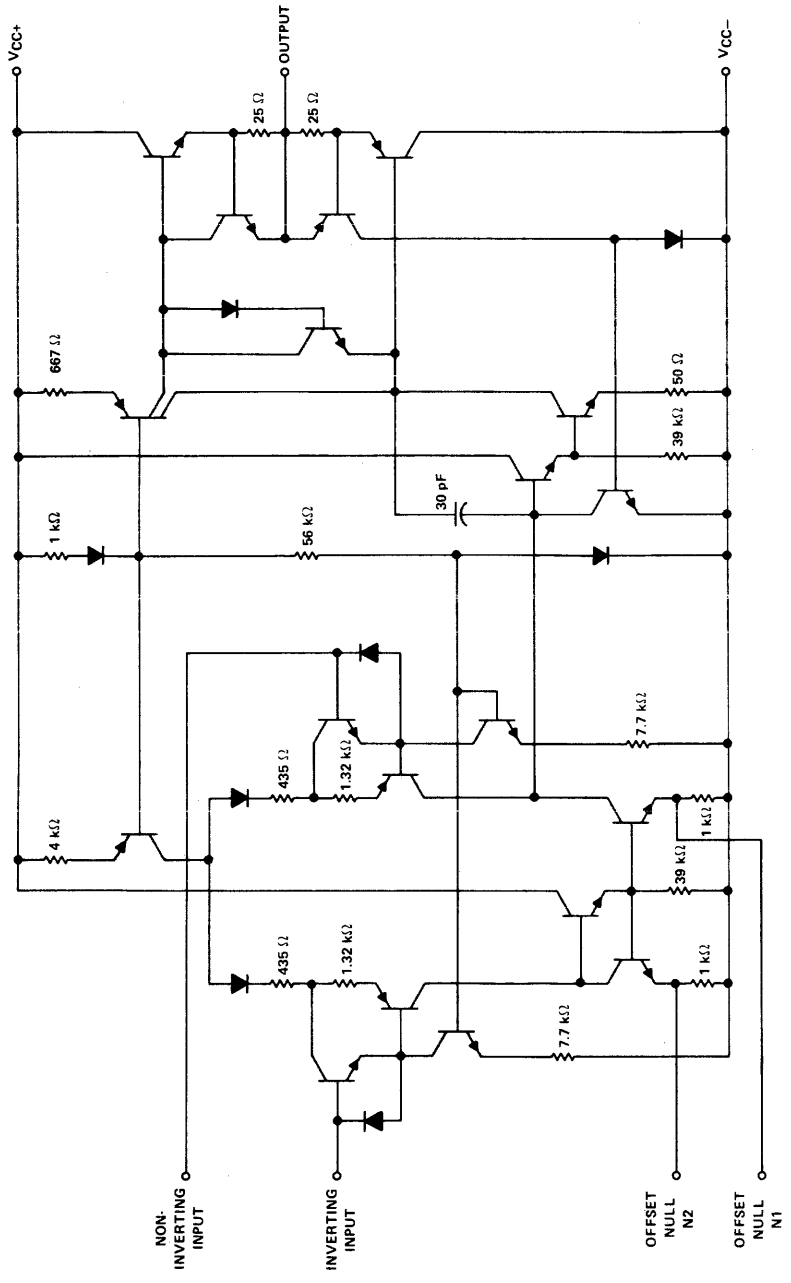
NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52771	SN72771	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52771 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

schematic



Component values shown are nominal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52771			SN72771			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ	25°C		2	4		5	10	mV
			Full range			7			14	
I_{IO}	Input offset current		25°C		1	2		5	10	nA
			Full range			5			14	
I_{IB}	Input bias current		25°C		8	15		15	30	nA
			Full range			35			40	
V_{ICR}	Common-mode input voltage range		25°C	±12	±14		±11			V
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 2 kΩ	25°C	24	26.5		22	26.5		
		$R_L \geq 2$ kΩ	Full range	24			22			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, V_O = ±10 V	25°C	50,000	100,000		35,000	100,000		
		$R_L \geq 2$ kΩ, V_O = ±10 V	Full range	25,000			25,000			
B_{OM}	Maximum-output-swing bandwidth (closed loop)	R_L = 2 kΩ, $V_O \geq$ ±10 V, A_{VD} = 1, THD ≤ 5%	25°C		40			40		kHz
B_1	Unity-gain bandwidth		25°C		1.3			1.3		MHz
r_{id}	Differential input resistance		25°C		100			100		MΩ
z_{ic}	Common-mode input impedance	f = 10 Hz	25°C		500			500		MΩ
z_o	Output impedance	f = 10 Hz	25°C		2			2		kΩ
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ	25°C	80	100		70	100		dB
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10$ kΩ	25°C		80	150			200	μV/V
e_n	Equivalent input noise voltage (closed loop)	A_{VD} = 100, BW = 1 Hz, f = 1 kHz	25°C		40			40		nV/√Hz
I_{OS}	Short-circuit output current	To V_{CC+}	25°C		24			24		mA
		To V_{CC-}			−20			−20		
I_{CC}	Supply current	No load, No signal	25°C		1.3	2		1.7	4	mA
P_D	Total power dissipation	No load, No signal	25°C		40	60		50	120	mW

†All characteristics are specified under open-loop operation unless otherwise noted. Full range for SN52771 is −55°C to 125°C and for SN72771 is 0°C to 70°C.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52771			SN72771			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 200 mV, R_L = 2 kΩ, C_L = 200 pF, C_C = 30 pF, See Figure 2		130			130		ns
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 200 pF, C_C = 30 pF, See Figure 2		2.5			2.5		V/μs

For ordering instructions and mechanical data, refer to Section 1.

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Common-Mode Input Voltage Range (V_{ICR}) The range of common-mode voltage which if exceeded will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

3

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Maximum-Output-Swing Bandwidth (B_{OM}) The range of frequencies within which the maximum output voltage swing is above a specified value.

Unity-Gain Bandwidth (B_1) The range of frequencies within which the voltage amplification is greater than unity.

Differential Input Resistance (r_{id}) The small-signal resistance between the two ungrounded input terminals.

Common-Mode Input Impedance (z_{ic}) The parallel sum of the small-signal impedances between each input terminal and ground.

Output Impedance (z_o) The impedance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Power Supply Sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) The ratio of the change in input offset voltage to the change in supply voltages producing it. For these devices, both supply voltages are varied symmetrically.

Short-Circuit Output Current (I_{OS}) The maximum output current available from the amplifier with the output shorted to the specified supply.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output voltage for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

THERMAL INFORMATION

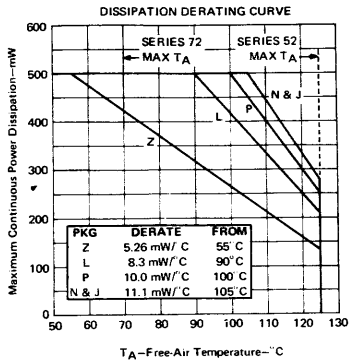


FIGURE 1

PARAMETER MEASUREMENT INFORMATION

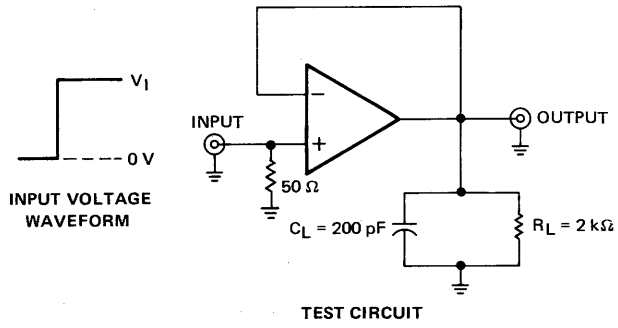


FIGURE 2–BANDWIDTH, RISE TIME, AND SLEW RATE

3

TYPICAL CHARACTERISTICS

SN52771

COMMON-MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

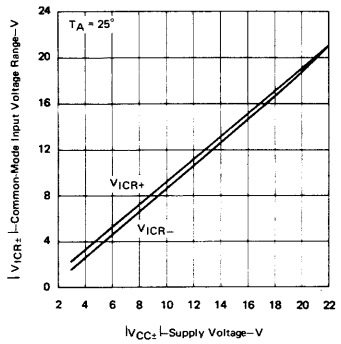


FIGURE 3

MAXIMUM OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

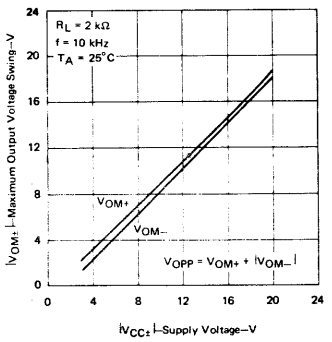


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE SWING vs FREQUENCY

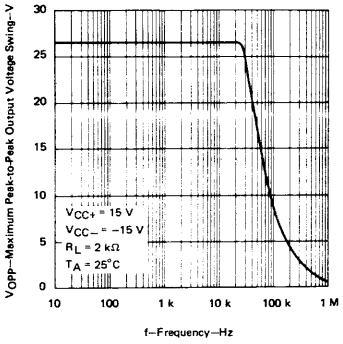


FIGURE 5

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

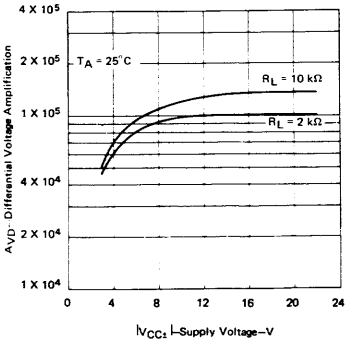


FIGURE 6

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

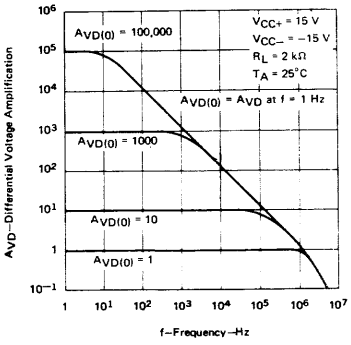


FIGURE 7

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

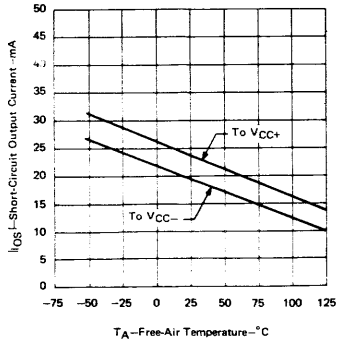


FIGURE 8

TYPICAL CHARACTERISTICS

TOTAL POWER DISSIPATION
vs
SUPPLY VOLTAGE

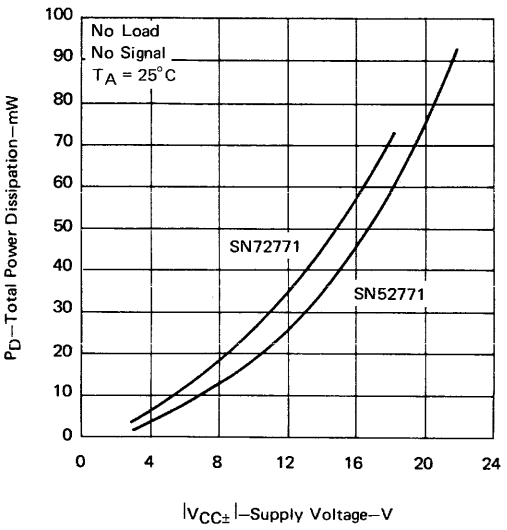


FIGURE 9

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

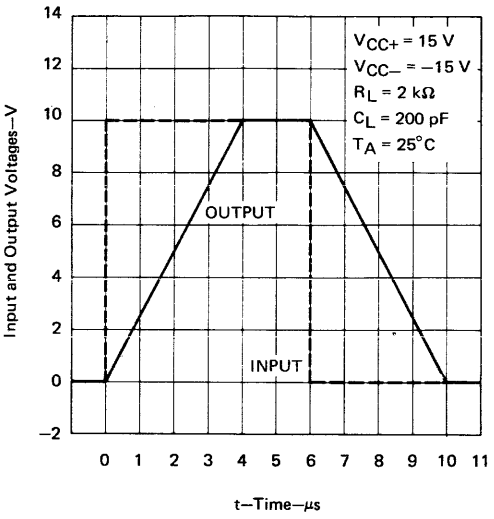
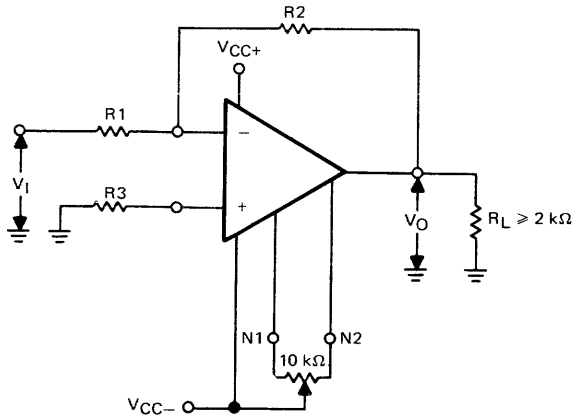


FIGURE 10

TYPICAL APPLICATION DATA



$$R3 = \frac{R1 \cdot R2}{R1 + R2} \qquad \frac{V_O}{V_I} = -\frac{R2}{R1}$$

FIGURE 11–INVERTING CIRCUIT WITH ADJUSTABLE GAIN, COMPENSATION, AND OFFSET ADJUSTMENT

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Series 52 and Series 55

TYPE	SINGLE				DUAL CHANNEL		DUAL				UNIT
	SN52710	SN52510	SN52810	SN52106*	SN52711	SN52811	SN52820	SN52514	SN52506*	SN55107A†	
Input Offset Voltage, Max	5	2	2	2	3.5	3.5	2	2	2	25	mV
Input Offset Current, Max	10	3	3	3	10	3	3	3	3	10	μA
Input Bias Current, Max	75	15	15	20	75	20	15	15	20	75	μA
Voltage Amplification, Min	750	12,500	12,500	40,000 Typ	750	12,500	12,500	12,500	40,000 Typ		
Common-Mode Input Voltage Range, Min	±5	±5	±5	±5	±5	±5	±5	±5	±5	±3	V
Output Sink Current, Min	1.6	2	2	100 Typ	0.5	0.5	2	2	100 Typ	16	mA
Input-Output Response Time, Typ	40	30	30	40	40	33	30	30	40	17	ns
Fan-Out to Series 54 TTL	1	1	1	10	1	1	1	1	10	10	
Power Supplies Required	12	12	12	12	12	12	12	12	12	5	V_{CC+}
	6	6	6	3 to 12	6	6	6	6	3 to 12	5	V_{CC-}
Packages	J, L, N, S	J, L, N, P, Z	J, L, N, P, Z	J, L, N, Z	J, L, N, S	J, L, N	J, N, Z	J, N, Z	N, J, Z	J, N	

3

Series 72 and Series 75

TYPE	SINGLE				DUAL CHANNEL		DUAL					UNIT
	SN72710	SN72510	SN72810	SN72306*	SN72711	SN72811	SN72720	SN72820	SN72514	SN72506*	SN75107A†	
Input Offset Voltage, Max	7.5	3.5	5	5	5	5	7.5	3.5	3.5	5	25	mV
Input Offset Current, Max	15	5	5	5	15	5	15	5	5	5	10	μA
Input Bias Current, Max	100	20	20	25	100	30	100	20	20	25	75	μA
Voltage Amplification, Min	700	10,000	10,000	40,000 Typ	700	10,000	700	10,000	10,000	40,000 Typ		
Common-Mode Input Voltage Range, Min	±5	±5	±5	±5	±5	±5	±5	±5	±5	±5	±3	V
Output Sink Current, Min	1.6	1.6	1.6	100 Typ	0.5	0.5		1.6	1.6	100	16	mA
Input-Output Response Time, Typ	40	30	30	40	40	33	40	30	30	40	17	ns
Fan-Out to Series 74 TTL	1	1	1	10	1	1	1	1	1	10	10	
Power Supplies Required	12	12	12	12	12	12	12	12	12	12	5	V_{CC+}
	6	6	6	3 to 12	6	6	6	6	6	3 to 12	5	V_{CC-}
Packages	J, L, N, S	J, L, N, P, Z	J, L, N, P, Z	J, L, N, Z	J, L, N, S	J, L, N	N	J, N, Z	J, N, Z	J, N, Z	J, N	

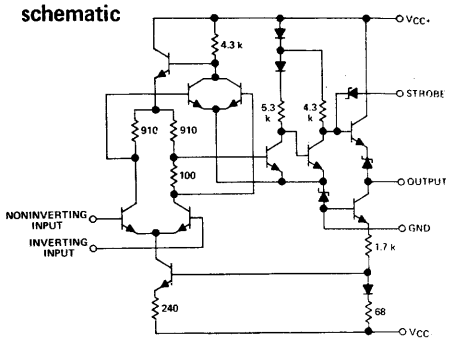
*To be announced soon

†Data sheet in the line circuits section.

CIRCUIT TYPES SN52510, SN72510 DIFFERENTIAL COMPARATORS WITH STROBE

- Low Offset Characteristics
- High Differential Voltage Amplification
- Fast Response Times
- Output Compatible with Most TTL and DTL Circuits

schematic



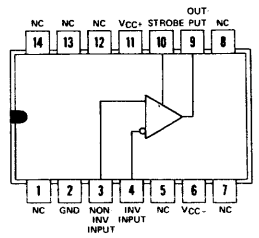
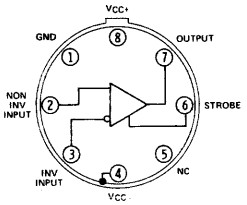
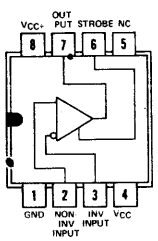
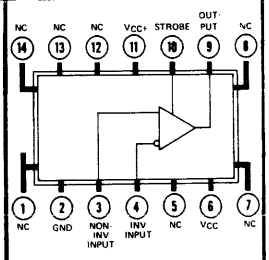
Resistor values are nominal in ohms.

description

The SN52510 and SN72510 monolithic high-speed voltage comparators are improved versions of the SN52710 and SN72710 with an extra stage added to increase voltage amplification and accuracy, and a strobe input for greater flexibility. Typical voltage amplification is 33,000. Since the output cannot be more positive than the strobe, a low-level input at the strobe will cause the output to go low regardless of the differential input. Component matching, inherent in integrated circuit fabrication techniques, produces a comparator with low-drift and low-offset characteristics. These circuits are particularly useful for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector.

The SN52510 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72510 is characterized for operation from 0°C to 70°C.

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	P DUAL-IN-LINE PACKAGE (TOP VIEW)	Z FLAT PACKAGE (TOP VIEW)
	 PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE		

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Strobe Voltage (see Note 1)	6 V
Peak output current ($t_w \leq 1$ s)	10 mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)	300 mW
Operating free-air temperature range: SN52510 Circuits	−55°C to 125°C
SN72510 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J, L, or Z package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N or P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the SN52510 above 70°C free-air temperature, refer to Dissipating Derating Curve, Figure 13.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52510 MIN	SN52510 TYP	SN52510 MAX	SN72510 MIN	SN72510 TYP	SN72510 MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		0.6	2		1.6	3.5	mV
			Full range			3			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage	R_S = 50 Ω, See Note 4	MIN to 25°C		3	10		3	20	μV/°C
			25°C to MAX		3	10		3	20	
I_{IO}	Input offset current	See Note 4	25°C		0.75	3		1.8	5	μA
			MIN		1.8	7			7.5	
			MAX		0.25	3			7.5	
α_{IIO}	Average temperature coefficient of input offset current	See Note 4	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	See Note 4	25°C		7	15		7	20	μA
			MIN		12	25		9	30	
I_{SH}	High-level strobe current	$V_{(strobe)}$ = 5 V, V_{ID} = −5 mV	25°C			±100			±100	μA
I_{SL}	Low-level strobe current	$V_{(strobe)}$ = −100 mV, V_{ID} = 5 mV	25°C		−1	−2.5		−1	−2.5	mA
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0 to 2.5 V	25°C	12,500	33,000		10,000	33,000		
			Full range	10,000			8,000			
V_{OH}	High-level output voltage	V_{ID} = 5 mV, I_{OH} = 0	Full range		4§	5		4§	5	V
		V_{ID} = 5 mV, I_{OH} = −5 mA	Full range	2.5	3.6§		2.5	3.6§		
V_{OL}	Low-level output voltage	V_{ID} = −5 mV, I_{OL} = 0	Full range	−1	−0.5§	0‡	−1	−0.5§	0‡	V
		$V_{(strobe)}$ = 0.3 V, V_{ID} = 5 mV, I_{OL} = 0	Full range	−1		0‡	−1		0‡	V
I_{OL}	Low-level output current	V_{ID} = −5 mV, V_O = 0	25°C	2	2.4		1.6	2.4		mA
			MIN	1	2.3		0.5	2.4		
			MAX	0.5	2.3		0.5	2.4		
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	Full range	80	100§		70	100§		dB
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 mV, No load	Full range		5.5§	9		5.5§	9	mA
I_{CC-}	Supply current from V_{CC-}		Full range		−3.5§	−7		−3.5§	−7	mA
P_D	Total power dissipation		Full range		90§	150		90§	150	mW

†Unless otherwise noted, all characteristics are measured with the strobe open. Full range (MIN to MAX) for SN52510 is −55°C to 125°C and for the SN72510 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

§These typical values are at T_A = 25°C.

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52510, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1V at T_A = 125°C; for SN72510, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Response time	R_L = ∞,	C_L = 5 pF,	See Note 5		30	80	ns
Strobe release time	R_L = ∞,	C_L = 5 pF,	See Note 6		5	25	ns

NOTES: 5. The response time specified is for a 100-mV input step with 5-mV overdrive.

6. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is then added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 50% point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4 V level.

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to the specified level. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at the specified level.

Average Temperature Coefficient of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

3

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at the specified level.

High-Level Strobe Current (I_{SH}) The current flowing into or out of the strobe at a high-level voltage.

Low-Level Strobe Current (I_{SL}) The current flowing out of the strobe at a low-level voltage.

Common-Mode Input Voltage Range (V_{ICR}) The range of common-mode voltage which if exceeded will cause the amplifier to cease functioning properly.

Differential Input Voltage Range (V_{ID}) The range of voltage between the two input terminals which if exceeded will cause the comparator to cease functioning properly.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in output voltage to the change in differential input voltage producing it.

High-Level Output Voltage (V_{OH}) The voltage at the output with the specified input conditions applied which should establish a high level at the output.

Low-Level Output Voltage (V_{OL}) The voltage at the output with the specified input conditions applied which should establish a low level at the output.

Low-Level Output Current (I_{OL}) The current flowing into the output at a specified low-level output voltage.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Response Time The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial condition sufficient to saturate the output to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Strobe Release Time The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the low logic level to the high logic level. Appropriate input conditions are assumed.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

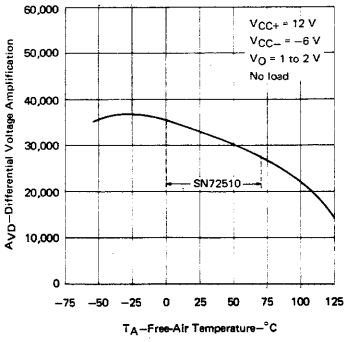


FIGURE 1

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

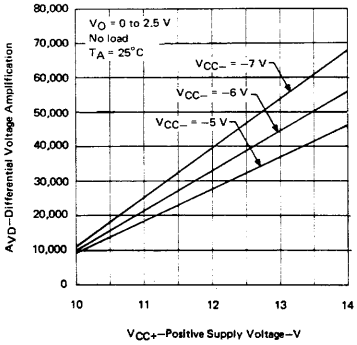


FIGURE 2

OUTPUT VOLTAGE LEVELS vs FREE-AIR TEMPERATURE

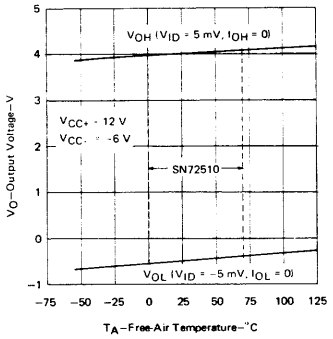


FIGURE 3

LOW-LEVEL OUTPUT CURRENT vs FREE-AIR TEMPERATURE

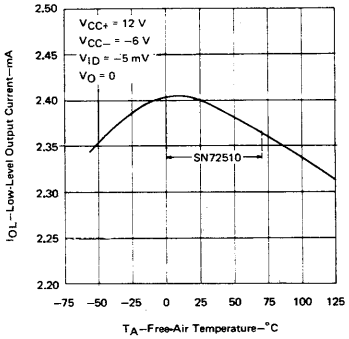


FIGURE 4

SN52510
VOLTAGE TRANSFER CHARACTERISTICS

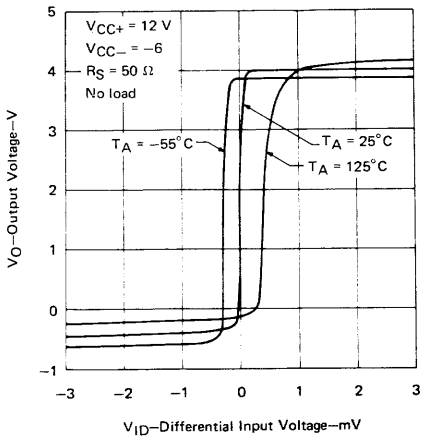


FIGURE 5

SN72510
VOLTAGE TRANSFER CHARACTERISTICS

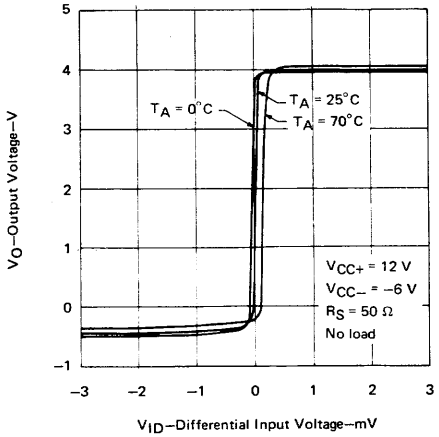


FIGURE 6

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

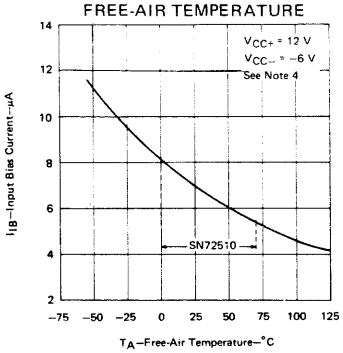


FIGURE 7

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

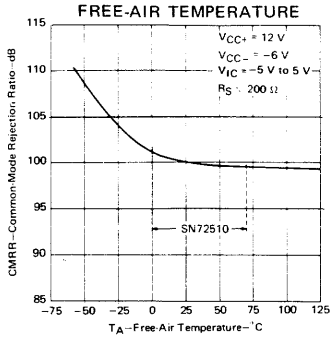


FIGURE 8

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

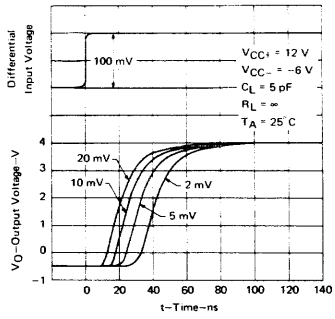


FIGURE 9

STROBE RELEASE TIME
FOR VARIOUS INPUT OVERDRIVES

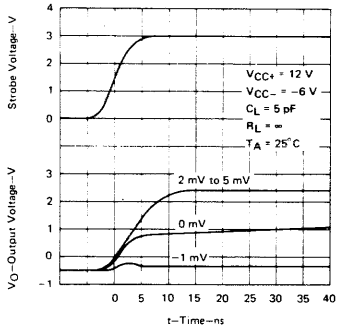


FIGURE 10

COMMON-MODE PULSE RESPONSE

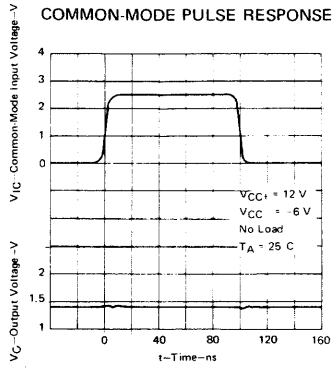
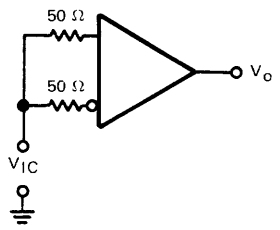


FIGURE 11



TEST CIRCUIT
FOR FIGURE 11

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52510, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1V at T_A = 125°C; for SN72510, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

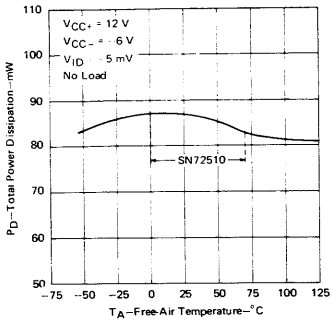


FIGURE 12

THERMAL INFORMATION

SN52510
DISSIPATION DERATING CURVE

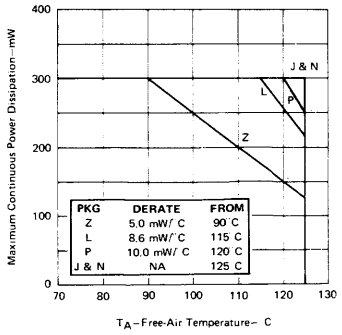


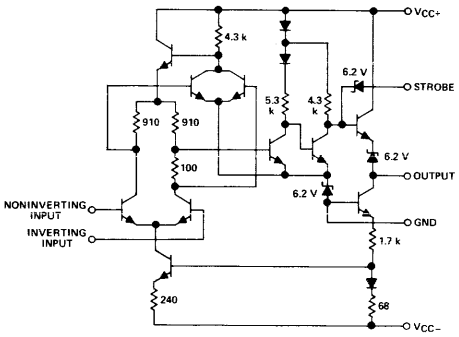
FIGURE 13

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN52514, SN72514
DUAL DIFFERENTIAL COMPARATORS WITH STROBES

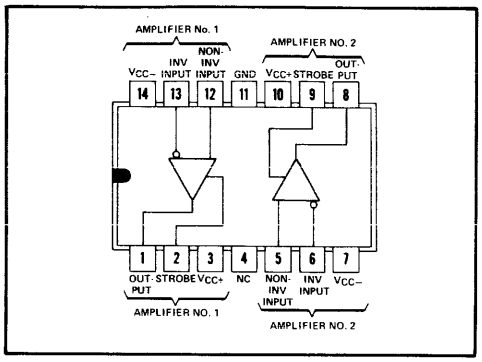
- Fast Response Times
- High Differential Voltage Amplification
- Low Offset Characteristics
- Outputs Compatible with Most TTL and DTL Circuits

schematic (each comparator)



Resistor values are in ohms.
Component values shown are nominal.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

description

The SN52514 and SN72514 are improved versions of the SN72720 dual high-speed voltage comparator. When compared with the SN72720, these circuits feature higher amplification (typically 33,000) due to an extra amplification stage, increased accuracy because of lower offset characterisitcs, and greater flexibility with the addition of a strobe to each comparator. Since the output cannot be more positive than the strobe, a low-level input at the strobe will cause the output to go low regardless of the differential input.

These circuits are especially useful in applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector. The SN52514 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72514 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Strobe voltage (see Note 1)	6 V
Peak output current ($t_w \leq 1$ s)	10 mA
Continuous total power dissipation: each comparator	300 mW
total package (see Note 3)	600 mW
Operating free-air temperature range: SN52514 Circuits	−55°C to 125°C
SN72714 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For SN52514, this rating applies at (or below) 95°C free-air temperature. For operation above this temperature, derate linearly at the rate of 10.9 mW/°C. For SN72514, this rating applies at (or below) 70°C free-air temperature without derating.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN52514, SN72514
DUAL DIFFERENTIAL COMPARATORS WITH STROBES

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52514			SN72514			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		0.6	2		1.6	3.5	mV
			Full range			3			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage	R_S = 50 Ω, See Note 4	MIN to 25°C		3	10		3	20	μV/°C
			25°C to MAX		3	10		3	20	
I_{IO}	Input offset current	See Note 4	25°C		0.75	3		1.8	5	μA
			MIN		1.8	7			7.5	
			MAX		0.25	3			7.5	
α_{IIO}	Average temperature coefficient of input offset current	See Note 4	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	See Note 4	25°C		7	15		7	20	μA
			MIN		12	25		9	30	
I_{SH}	High-level strobe current	$V_{(strobe)}$ = 5 V, V_{ID} = −5 mV	25°C			±100			±100	μA
I_{SL}	Low-level strobe current	$V_{(strobe)}$ = −100 mV, V_{ID} = 5 mV	25°C		−1	−2.5		−1	−2.5	mA
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0 to 2.5 V	25°C	12,500	33,000		10,000	33,000		
			Full range	10,000			8,000			
V_{OH}	High-level output voltage	V_{ID} = 5 mV, I_{OH} = 0	Full range		4§	5		4§	5	V
		V_{ID} = 5 mV, I_{OH} = −5 mA	Full range	2.5	3.6§		2.5	3.6§		
V_{OL}	Low-level output voltage	V_{ID} = −5 mV, I_{OL} = 0	Full range	−1	−0.5§	0‡	−1	−0.5§	0‡	V
		$V_{(strobe)}$ = 0.3 V, V_{ID} = 5 mV, I_{OL} = 0	Full range	−1		0‡	−1		0‡	V
I_{OL}	Low-level output current	V_{ID} = −5 mV, V_O = 0	25°C	2	2.4		1.6	2.4		mA
			MIN	1	2.3		0.5	2.4		
			MAX	0.5	2.3		0.5	2.4		
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	Full range	80	100§		70	100§		dB
I_{CC+}	Supply current from V_{CC+} ¶	V_{ID} = −5 mV, No load	Full range		5.5§	9		5.5§	9	mA
I_{CC-}	Supply current from V_{CC-} ¶		Full range		−3.5§	−7		−3.5§	−7	mA
P_D	Total power dissipation ¶		Full range		90§	150		90§	150	mW

†Unless otherwise noted, all characteristics are measured with the strobe open. Full range (MIN to MAX) for SN52514 is −55°C to 125°C and for the SN72514 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

§These typical values are at T_A = 25°C.

¶Suppy current and power dissipation limits apply for each comparator.

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52514, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1V at T_A = 125°C; for SN72514, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Response time	R_L = ∞,	C_L = 5 pF,	See Note 5		30	80	ns
Strobe release time	R_L = ∞,	C_L = 5 pF,	See Note 6		5	25	ns

NOTES: 5. The response time specified is for a 100-mV input step with 5-mV overdrive.

6. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is then added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 50% point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4 V level.

For definition of terms and typical characteristic curves, see the SN52510/SN72510 data sheet on page 3-60.

PRINTED IN U.S.A.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

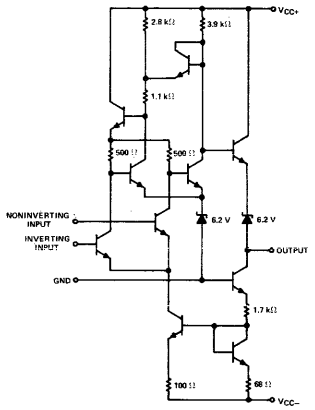
CIRCUIT TYPES SN52710, SN72710
DIFFERENTIAL COMPARATORS

- Fast Response Times
- Low Offset Characteristics
- Output Compatible with Most TTL and DTL Circuits

description

The SN52710 and SN72710 are monolithic high-speed comparators having differential inputs and a low-impedance output. Component matching, inherent in silicon integrated circuit fabrication techniques, produces a comparator with low-drift and low-offset characteristics. These circuits are especially useful for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed voltage comparator. The SN52710 is characterised for operation over the full military temperature range of −55°C to 125°C; the SN72710 is characterized for operation from 0°C to 70°C.

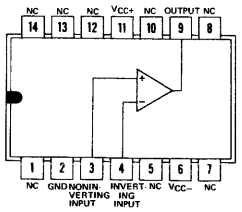
schematic



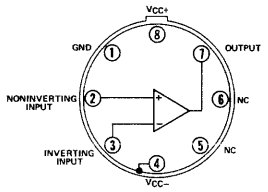
Component values shown are nominal.

terminal assignments

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

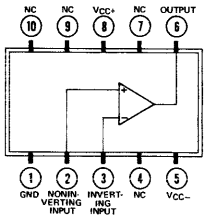


L
PLUG-IN PACKAGE (TOP VIEW)



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

S
FLAT PACKAGE (TOP VIEW)



PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52710	SN72710	UNIT
Supply voltage V_{CC+} (see Note 1)		14	14	V
Supply voltage V_{CC-} (see Note 1)		−7	−7	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Note 1)		±7	±7	V
Peak output current ($t_w \leq 1$ s)		10	10	mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)		300	300	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or S package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package	260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the SN52710 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 8.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52710			SN72710			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		2	5		2	7.5	mV
			Full range			6			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	Full range		5			7.5		μV/°C
I_{IO}	Input offset current	See Note 4	25°C		1	10		1	15	μA
			Full range			20			25	
I_{IB}	Input bias current	See Note 4	25°C		25	75		25	100	μA
			Full range			150			150	
V_I	Input voltage range	V_{CC-} = −7 V	25°C	±5			±5			V
V_{ID}	Differential input voltage range		25°C	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, See Note 4	25°C	750	1500		700	1500		
			Full range	500			500			
V_{OH}	High-level output voltage	V_{ID} = 15 mV, I_{OH} = −0.5 mA	25°C	2.5	3.2	4	2.5	3.2	4	V
V_{OL}	Low-level output voltage	V_{ID} = −15 mV, I_{OL} = 0	25°C	−1	−0.5	0‡	−1	−0.5	0‡	V
I_{OL}	Low-level output current	V_{ID} = −15 mV, V_O = 0	25°C	1.6	2.5					mA
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	25°C	70	90		65	90		dB
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 V to 5 V (−10 mV for typ), No load	25°C		5.4	10.1		5.4		mA
I_{CC-}	Supply current from V_{CC-}		25°C		−3.8	−8.9		−3.8		mA
P_D	Total power dissipation		25°C		88	175		88		mW

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52710, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for SN72710, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

†Full range for SN52710 is −55°C to 125°C and for SN72710 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	SN52710	SN72710	UNIT
		TYP	TYP	
Response time	No load, See Note 5	40	40	ns

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive.

For definitions of terms, mechanical data and ordering instructions, see SN52711/SN72711 data sheet dated February 1971.

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVES

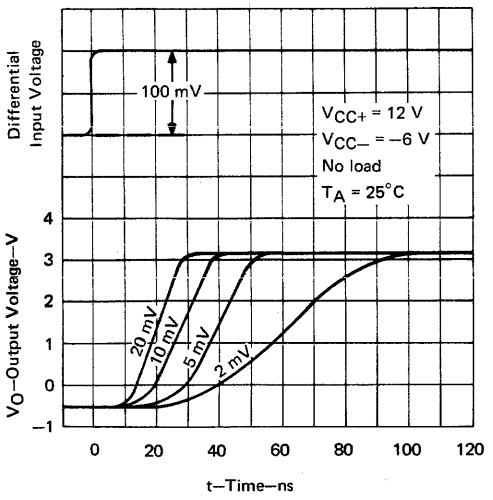


FIGURE 1

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVES

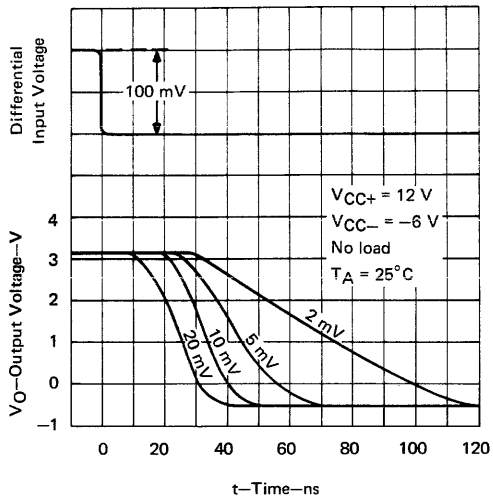


FIGURE 2

COMMON-MODE PULSE RESPONSE
vs
ELAPSED TIME

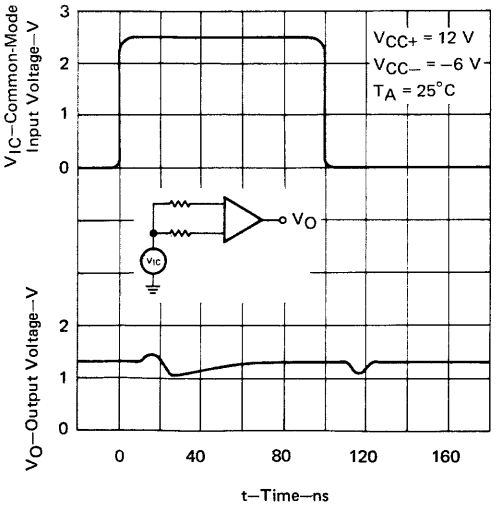


FIGURE 3

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

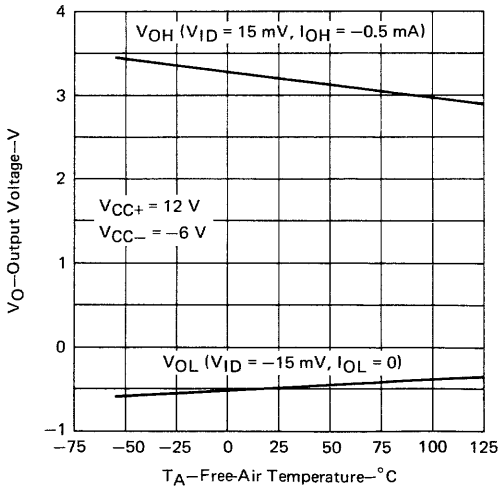


FIGURE 4

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

SN52710

VOLTAGE TRANSFER CHARACTERISTICS

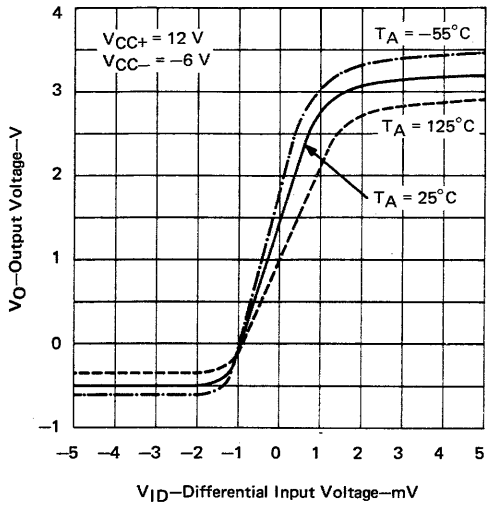


FIGURE 5

SN72710

VOLTAGE TRANSFER CHARACTERISTICS

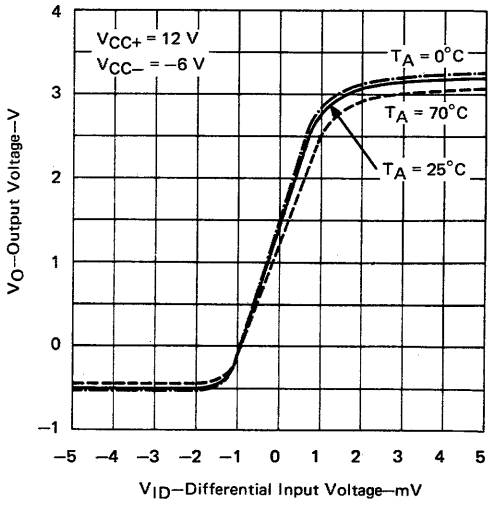


FIGURE 6

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

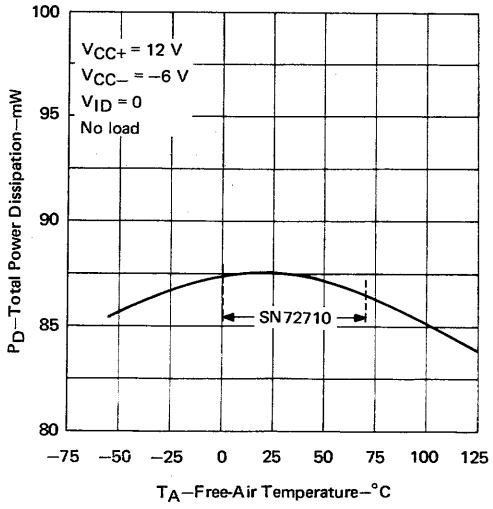


FIGURE 7

THERMAL INFORMATION

DISSIPATION DERATING CURVE

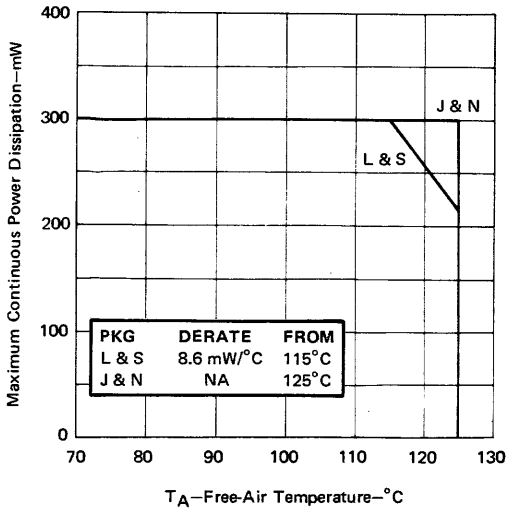


FIGURE 8

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

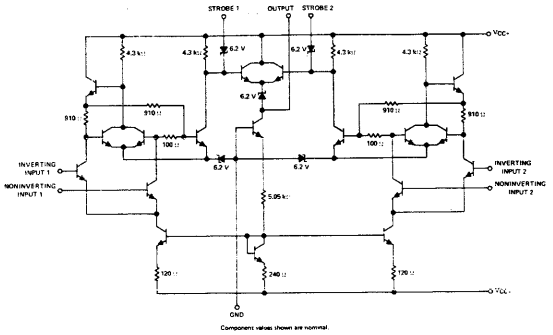
CIRCUIT TYPES SN52711, SN72711 DUAL-CHANNEL DIFFERENTIAL COMPARATORS WITH STROBES

- Fast Response Times
- Low Offset Characteristics
- Output Compatible with Most TTL and DTL Circuits
- Designed to be Interchangeable with Fairchild μA711 and μA711C

description

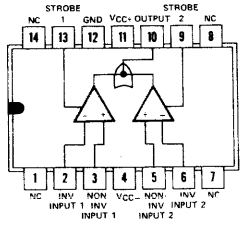
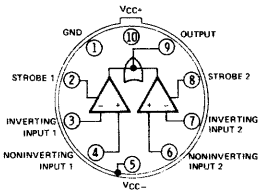
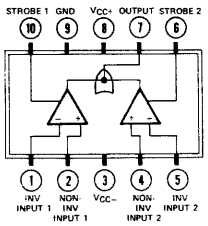
The SN52711 and SN72711 circuits are high-speed dual-channel comparators with differential inputs and a low-impedance output. Component matching, inherent with silicon monolithic circuit fabrication techniques, produces a comparator circuit with low-drift and low-offset characteristics. An independent strobe input is provided for each of the two channels, which when taken low, inhibits the associated channel. If both strobes are simultaneously low, the output will be low regardless of the conditions applied to the differential inputs. The comparator output puise width may be "stretched" by varying the capacitive loading. These dual comparators are particularly useful for applications requiring an amplitude-discriminating sense amplifier with an adjustable threshold voltage. The SN52711 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72711 is characterized for operation from 0°C to 70°C.

schematic



3

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	S FLAT PACKAGE (TOP VIEW)
		
	PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE	PIN 3 IS IN ELECTRICAL CONTACT WITH THE CASE

NC—No Internal Connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52711	SN72711	UNIT
Supply voltage V_{CC+} (see Note 1)		14	14	V
Supply voltage V_{CC-} (see Note 1)		−7	−7	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Note 1)		±7	±7	V
Strobe voltage (see Note 1)		6	6	V
Peak output current ($t_w \leq 1$ s)		50	50	mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)		300	300	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or S package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package	260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of SN52711 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 9.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52711			SN72711			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, V_{IC} = 0, See Note 4	25°C		1	3.5		1	5	mV
			Full range			4.5			6	
		$R_S \leq 200\ \Omega$, See Note 4	25°C		1	5		1	7.5	
			Full range			6			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leq 200\ \Omega$, V_{IC} = 0, See Note 4	Full range		5			5		μV/°C
I_{IO}	Input offset current	See Note 4	25°C		0.5	10		0.5	15	μA
			Full range			20			25	
I_{IB}	Input bias current	See Note 4	25°C		25	75		25	100	μA
			Full range			150			150	
I_{SL}	Low-level strobe current	$V_{(strobe)}$ = 0, V_{ID} = 10 mV	25°C		−1.2	−2.5		−1.2	−2.5	mA
V_I	Input voltage range	V_{CC-} = −7 V	25°C	±5			±5			V
V_{ID}	Differential input voltage range		25°C	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0 to 2.5 V	25°C	750	1500		700	1500		
			Full range	500			500			
V_{OH}	High-level output voltage	V_{ID} = 10 mV, I_{OH} = 0	25°C		4.5	5		4.5	5	V
		V_{ID} = 10 mV, I_{OH} = −5 mA	25°C	2.5	3.5		2.5	3.5		
V_{OL}	Low-level output voltage	V_{ID} = −10 mV, I_{OL} = 0	25°C	−1	−0.5	0‡	−1	−0.5	0‡	V
		V_{ID} = 10 mV, $V_{(strobe)}$ = 0.3 V, I_{OL} = 0	25°C	−1		0‡	−1		0‡	
I_{OL}	Low-level output current	V_{ID} = −10 mV, V_O = 0	25°C	0.5	0.8		0.5	0.8		mA
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	25°C	70	90		65	90		dB
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 V to 5 V (−10 mV for typ), Strobes alternately grounded, No load	25°C		9			9		mA
I_{CC-}	Supply current from V_{CC-}		25°C		−4			−4		mA
P_D	Total power dissipation		25°C		130	200		130	230	mW

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52711, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for SN72711, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

†Unless otherwise noted, all characteristics are measured with the strobe of the channel under test open. The strobe of the other channel is grounded. Full range for SN52711 is −55°C to 125°C and for the SN72711 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		SN52711			SN72711			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Response time	No load,	See Note 5		40	80		40		ns
Strobe release time	No load,	See Note 6		7	25		7		ns

NOTES: 5. The response time specified is for a 100-mV input step with 5-mV overdrive.

6. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is then added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 50% point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4 V level.

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to the specified level. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at the specified level.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at the specified level.

3

Low-Level Strobe Current (I_{SL}) The current flowing out of the strobe at a low-level voltage.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the comparator to cease functioning properly.

Differential Input Voltage Range (V_{ID}) The range of voltage between the two input terminals which if exceeded will cause the comparator to cease functioning properly.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in output voltage to the change in differential input voltage producing it.

High-Level Output Voltage (V_{OH}) The voltage at the output with the specified input conditions applied which should establish a high level at the output.

Low-Level Output Voltage (V_{OL}) The voltage at the output with the specified input conditions applied which should establish a low level at the output.

Low-Level Output Current (I_{OL}) The current flowing into the output at a specified low-level output voltage.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Response Time The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial condition sufficient to saturate the output to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Strobe Release Time The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the low logic level to the high logic level. Appropriate input conditions are assumed.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

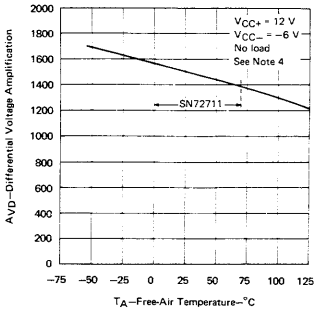


FIGURE 1

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

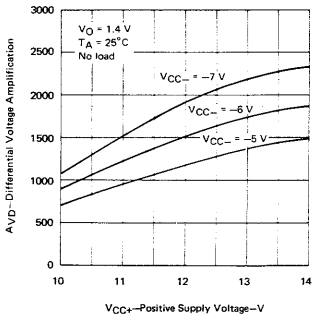


FIGURE 2

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

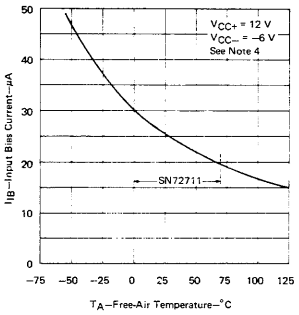


FIGURE 3

TOTAL POWER DISSIPATION vs FREE-AIR TEMPERATURE

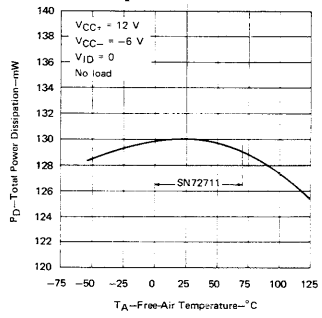


FIGURE 4

SN52711 VOLTAGE TRANSFER CHARACTERISTICS

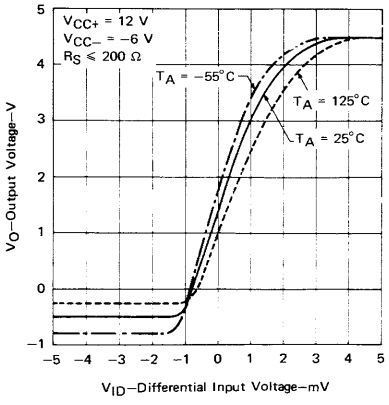


FIGURE 5

SN72711 VOLTAGE TRANSFER CHARACTERISTICS

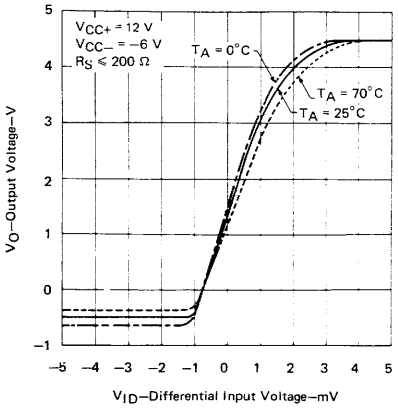


FIGURE 6

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52711, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for SN72711, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

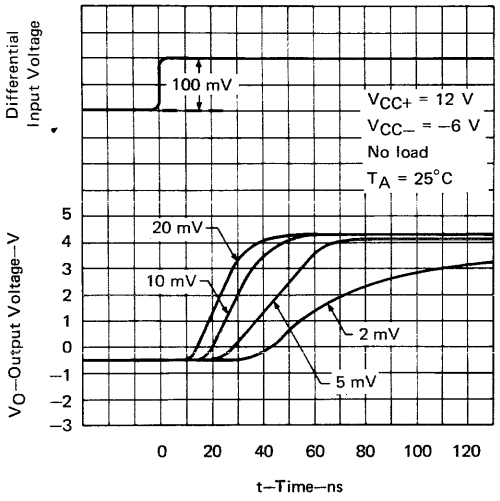


FIGURE 7

STROBE RELEASE TIME
FOR VARIOUS INPUT OVERDRIVES

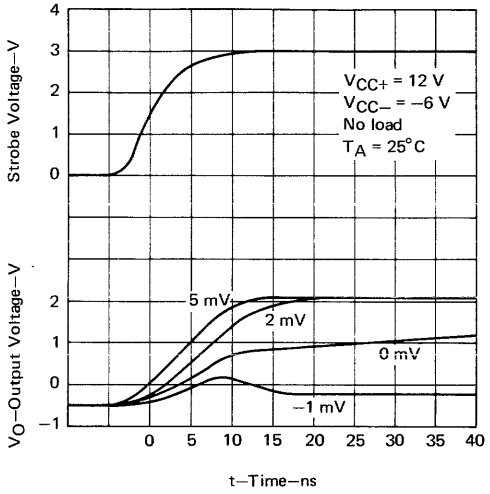


FIGURE 8

THERMAL INFORMATION

SN52711
DISSIPATION DERATING CURVE

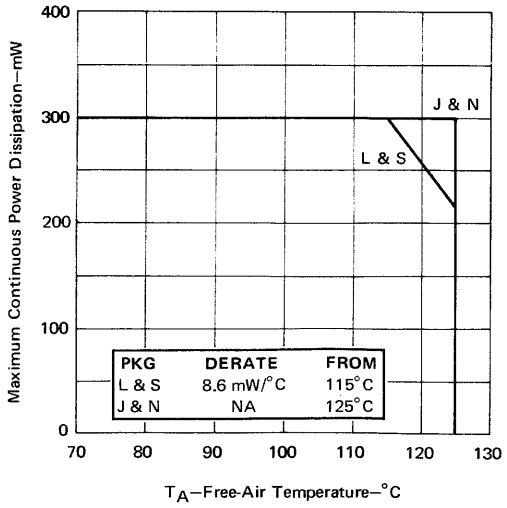


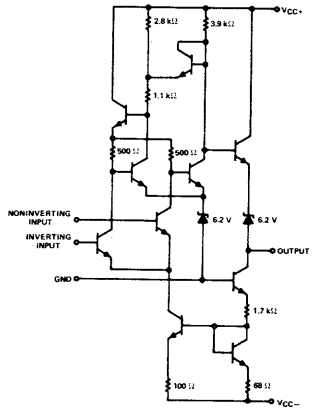
FIGURE 9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE SN72720
DUAL DIFFERENTIAL COMPARATORS

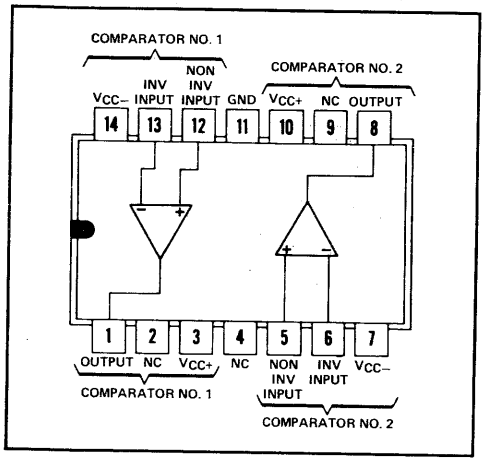
- Fast Response Times
- Low Offset Characteristics
- Output Compatible with Most TTL and DTL Circuits

schematic (each comparator)



Component values shown are nominal.

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

description

The SN72720 is two high-speed comparators in a single package, each electrically identical to the SN72710 and having differential inputs and a low-impedance output. Component matching, inherent in silicon monolithic circuit fabrication techniques, produces a comparator with low-drift and low-offset characteristics. This circuit is especially useful for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed voltage comparator. The SN72720 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Peak output current, each comparator ($t_w \leq 1$ s)	10 mA
Continuous total power dissipation: each comparator	300 mW
total package	600 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 10 seconds	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE SN72720
DUAL DIFFERENTIAL COMPARATORS

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 3	25°C		2	7.5	mV
			0°C to 70°C			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leq 200\ \Omega$, See Note 3	0°C to 70°C		7.5		μV/°C
I_{IO}	Input offset current	See Note 3	25°C		1	15	μA
			0°C to 70°C			25	
I_{IB}	Input bias current	See Note 3	25°C		25	100	μA
			0°C to 70°C			150	
V_I	Input voltage range	V_{CC-} = −7 V	25°C	±5			V
V_{ID}	Differential input voltage range		25°C	±5			V
A_{VD}	Large-signal differential voltage amplification	No load, See Note 3	25°C	700	1500		
			0°C to 70°C	500			
V_{OH}	High-level output voltage	V_{ID} = 15 mV, I_{OH} = −0.5 mA	25°C	2.5	3.2	4	V
V_{OL}	Low-level output voltage	V_{ID} = −15 mV, I_{OL} = 0	25°C	−1	−0.5	0‡	V
r_o	Output resistance	V_O = 1.4 V	25°C		200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	25°C	65	90		dB
I_{CC+}	Supply current from V_{CC+} (each comparator)	V_{ID} = −5 V to 5 V (−10 mV for typ), No load	25°C		5.4		mA
I_{CC-}	Supply current from V_{CC-} (each comparator)		25°C		−3.8		mA
P_D	Total power dissipation (each comparator)		25°C		88		mW

NOTE 3: These characteristics are verified by measurements at the following temperatures and output voltage levels: V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
Response time	No load, See Note 4	40	ns

NOTE 4: The response time specified is for a 100-mV input step with 5-mV overdrive.

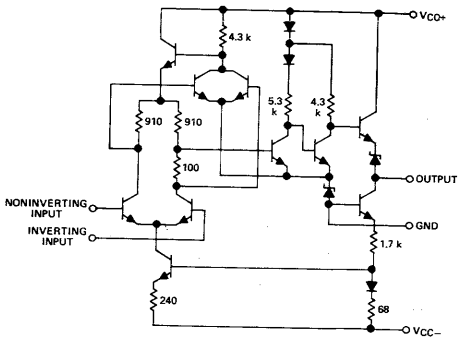
For definition of terms, refer to page of the SN52711/SN72711 data sheet. Typical characteristic curves on the SN72710 data sheet, pages 3-70 and 3-71, are applicable for the SN72720.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN52810, SN72810
DIFFERENTIAL COMPARATORS

- Low Offset Characteristics
- High Differential Voltage Amplification
- Fast Response Times
- Output Compatible with Most TTL and DTL Circuits

schematic



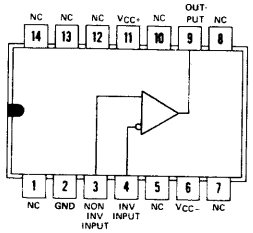
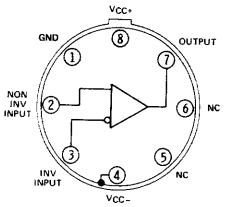
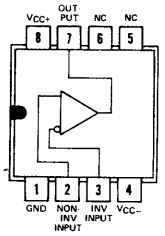
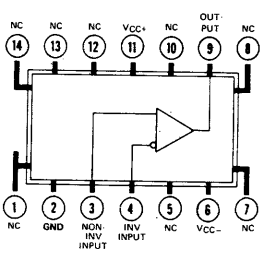
Resistor values are nominal in ohms.

description

The SN52810 and SN72810 are improved versions of the SN52710 and SN72710 high-speed voltage comparators with an extra stage added to increase voltage amplification and accuracy. Typical amplification is 33,000. Component matching, inherent in monolithic integrated circuit fabrication techniques, produces a comparator with low-drift and low-offset characteristics. These circuits are particularly useful for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector.

The SN52810 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72810 is characterized for operation from 0°C to 70°C.

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	P DUAL-IN-LINE PACKAGE (TOP VIEW)	Z FLAT PACKAGE (TOP VIEW)
	 PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE		

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Peak output current ($t_w \leq 1$ s)	10 mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)	300 mW
Operating free-air temperature range: SN52810 Circuits	−55°C to 125°C
SN72810 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J, L, or Z package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N or P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the SN52810 above 70°C free-air temperature, refer to Dissipating Derating Curve, Figure 1.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52810 MIN	SN52810 TYP	SN52810 MAX	SN72810 MIN	SN72810 TYP	SN72810 MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		0.6	2		1.6	3.5	mV
			Full range			3			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage	R_S = 50 Ω, See Note 4	MIN to 25°C		3	10		3	20	μV/°C
			25°C to MAX		3	10		3	20	
I_{IO}	Input offset current	See Note 4	25°C		0.75	3		1.8	5	μA
			MIN		1.8	7			7.5	
			MAX		0.25	3			7.5	
α_{IIO}	Average temperature coefficient of input offset current	See Note 4	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	See Note 4	25°C		7	15		7	20	μA
			MIN		12	25		9	30	
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0 to 2.5 V	25°C	12,500	33,000		10,000	33,000		
			Full range	10,000			8,000			
V_{OH}	High-level output voltage	V_{ID} = 5 mV, I_{OH} = 0	Full range		4§	5		4§	5	V
		V_{ID} = 5 mV, I_{OH} = −5 mA	Full range	2.5	3.6§		2.5	3.6§		
V_{OL}	Low-level output voltage	V_{ID} = −5 mV, I_{OL} = 0	Full range	−1	−0.5§	0‡	−1	−0.5§	0‡	V
I_{OL}	Low-level output current	V_{ID} = −5 mV, V_O = 0	25°C	2	2.4		1.6	2.4		mA
			MIN	1	2.3		0.5	2.4		
			MAX	0.5	2.3		0.5	2.4		
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	Full range	80	100§		70	100§		dB
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 mV, No load	Full range		5.5§	9		5.5§	9	mA
I_{CC-}	Supply current from V_{CC-}		Full range		−3.5§	−7		−3.5§	−7	mA
P_D	Total power dissipation		Full range		90§	150		90§	150	mW

†Full range (MIN to MAX) for SN52810 is −55°C to 125°C and for the SN72810 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

§These typical values are at T_A = 25°C.

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52810, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1V at T_A = 125°C; for SN72810, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Response time	$R_L = \infty$,	C_L = 5 pF,	See Note 5		30	80	ns

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to the specified level. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at the specified level.

Average Temperature Coefficient of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

3

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at the specified level.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the comparator to cease functioning properly.

Differential Input Voltage Range (V_{ID}) The range of voltage between the two input terminals which if exceeded will cause the comparator to cease functioning properly.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in output voltage to the change in differential input voltage producing it.

High-Level Output Voltage (V_{OH}) The voltage at the output with the specified input conditions applied which should establish a high level at the output.

Low-Level Output Voltage (V_{OL}) The voltage at the output with the specified input conditions applied which should establish a low level at the output.

Low-Level Output Current (I_{OL}) The current flowing into the output at a specified low-level output voltage.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Response Time The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial condition sufficient to saturate the output to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

THERMAL INFORMATION

SN52810
DISSIPATION DERATING CURVE

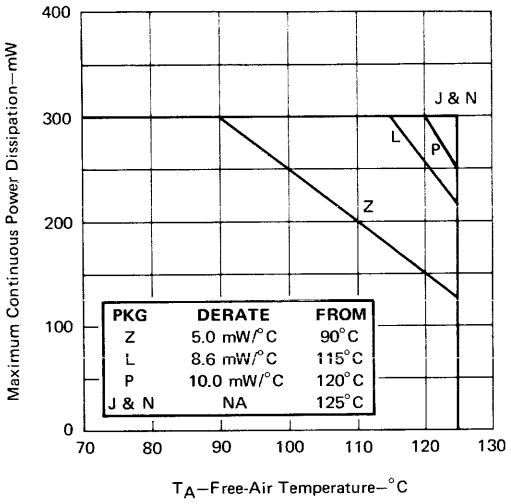


FIGURE 1

TYPICAL CHARACTERISTICS

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

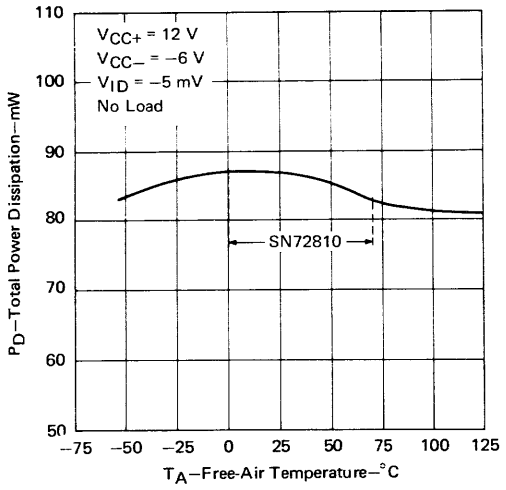


FIGURE 2

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

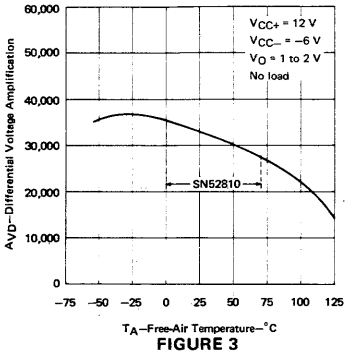


FIGURE 3

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

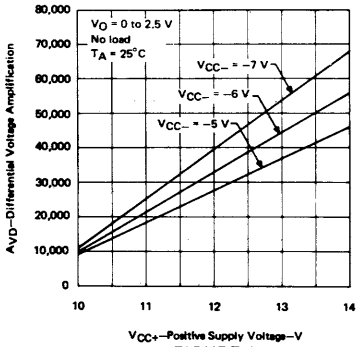


FIGURE 4

OUTPUT VOLTAGE LEVELS vs FREE-AIR TEMPERATURE

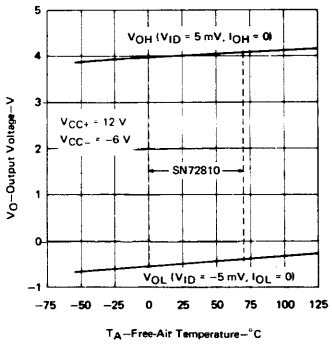


FIGURE 5

LOW-LEVEL OUTPUT CURRENT vs FREE-AIR TEMPERATURE

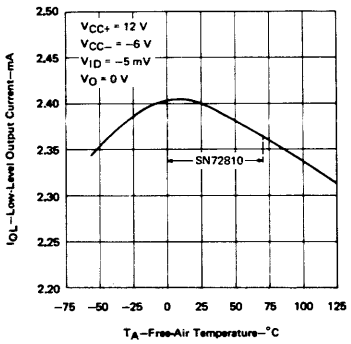


FIGURE 6

SN52810 VOLTAGE TRANSFER CHARACTERISTICS

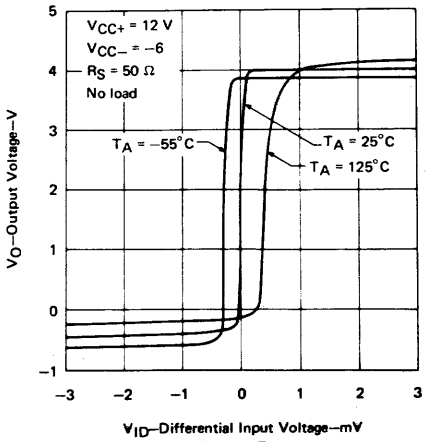


FIGURE 7

SN72810 VOLTAGE TRANSFER CHARACTERISTICS

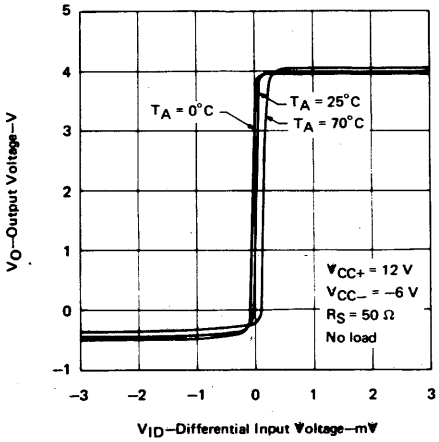


FIGURE 8

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

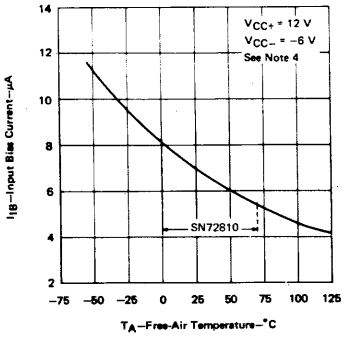


FIGURE 9

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

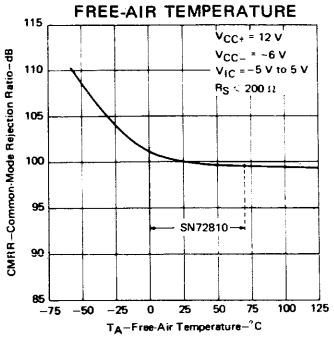


FIGURE 10

3

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

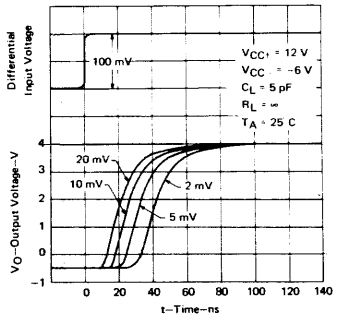


FIGURE 11

COMMON-MODE PULSE RESPONSE

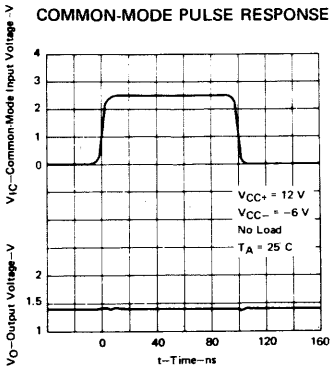
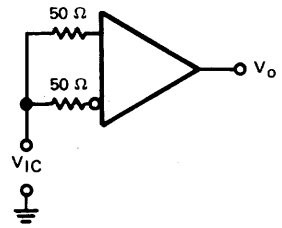


FIGURE 12



TEST CIRCUIT
FOR FIGURE 12

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52810, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1V at T_A = 125°C; for SN72810, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN52811, SN72811
DUAL-CHANNEL DIFFERENTIAL COMPARATORS WITH STROBES

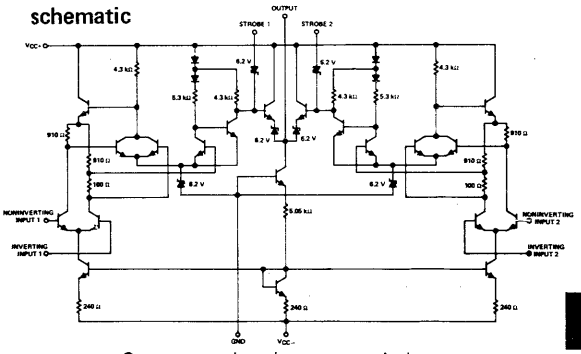
- Fast Response Times
- Improved Voltage Amplification and Offset Characteristics
- Output Compatible with Most TTL and DTL Circuits

description

The SN52811 and SN72811 are improved versions of the SN52711 and SN72711 high-speed dual-channel voltage comparators. Voltage amplification is higher (typically 17,500) due to an extra stage, increasing the comparator accuracy. The output pulse width may be "stretched" by varying the capacitive loading.

Each channel has differential inputs, a strobe input, and an output in common with the other channel. When either strobe is taken low, it inhibits the associated channel. If both strobes are simultaneously low, the output will be low regardless of the conditions applied to the differential inputs.

schematic



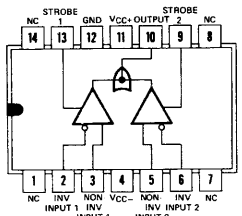
Component values shown are nominal.

These dual-channel voltage comparators are particularly attractive for applications requiring an amplitude-discriminating sense amplifier with an adjustable threshold voltage.

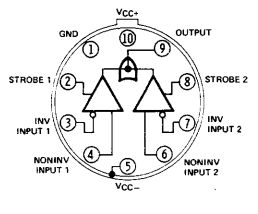
The SN52811 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72811 is characterized for operation from 0°C to 70°C.

terminal assignments

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

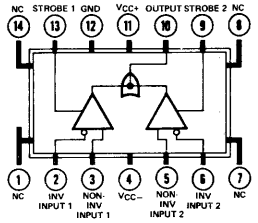


L
PLUG-IN PACKAGE (TOP VIEW)



PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

Z FLAT PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Strobe Voltage (see Note 1)	6 V
Peak output current ($t_w \leq 1$ s)	50 mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)	300 mW
Operating free-air temperature range: SN52811 Circuits	−55°C to 125°C
SN72811 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J, L, or Z package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the SN52811 above 70°C free-air temperature, refer to Dissipating Derating Curve, Figure 10.

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52811			SN72811			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, V_{IC} = 0, See Note 4	25°C		1	3.5		1	5	mV
			Full range			4.5			6	
		$R_S \leq 200\ \Omega$, See Note 4	25°C		1	5		1	7.5	
			Full range			6			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leq 200\ \Omega$, V_{IC} = 0, See Note 4	Full range		5			5		μV/°C
I_{IO}	Input offset current	See Note 4	25°C		0.5	3		0.5	5	μA
			Full range			5			10	
I_{IB}	Input bias current	See Note 4	25°C		7	20		7	30	μA
			Full range			30			50	
I_{SL}	Low-level strobe current	$V_{(strobe)}$ = −100 mV	25°C		−1.2	−2.5		−1.2	−2.5	mA
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V	25°C	±5			±5			V
V_{ID}	Differential input voltage range		25°C	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	V_O = 0 to 2.5 V, No load	25°C	12,500	17,500		10,000	17,500		
			Full range	8,000			5,000			
V_{OH}	High-level output voltage	V_{ID} = 10 mV, I_{OH} = 0	25°C		4	5		4	5	V
		V_{ID} = 10 mV, I_{OH} = −5 mA	25°C	2.5	3.6		2.5	3.6		
V_{OL}	Low-level output voltage	V_{ID} = −10 mV, I_{OL} = 0	25°C	−1	−0.4	0‡	−1	−0.4	0‡	V
		V_{ID} = 10 mV, $V_{(strobe)}$ = 0.3 V, I_{OL} = 0	25°C	−1		0‡	−1		0‡	
I_{OL}	Low-level output current	V_{ID} = −10 mV, V_O = 0	25°C	0.5	0.8		0.5	0.8		mA
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	25°C	70	90		65	90		dB
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 to 5 V (−10 mV for typ), No load, See Note 5	25°C		6.5			6.5		mA
I_{CC-}	Supply current from V_{CC-}		25°C		−2.7			−2.7		mA
P_D	Total power dissipation		25°C		94	150		94	200	mW

†Unless otherwise noted, all characteristics are measured with the strobe of the channel under test open, the strobe of the other channel is grounded. Full range for SN52811 is −55°C to 125°C and for the SN72811 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

NOTES: 4. These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52811, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for SN72811, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

5. The strobes are alternately grounded.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	SN52811			SN72811			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Response time	R_L = ∞, C_L = 5 pF, See Note 6		33	80		33		ns
Strobe release time	R_L = ∞, C_L = 5 pF, See Note 7		5	25		5		ns

NOTES: 6. The response time specified is for a 100-mV input step with 5-mV overdrive.

7. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is then added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 50% point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4 V level.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to the specified level. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} \text{ @ } T_{A(1)}) - (V_{IO} \text{ @ } T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at the specified level.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at the specified level.

Low-Level Strobe Current (I_{SL}) The current flowing out of the strobe at a low-level voltage.

Common-Mode Input Voltage Range (V_{ICR}) The range of common-mode voltage which if exceeded will cause the amplifier to cease functioning properly.

Differential Input Voltage Range (V_{ID}) The range of voltage between the two input terminals which if exceeded will cause the comparator to cease functioning properly.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in output voltage to the change in differential input voltage producing it.

High-Level Output Voltage (V_{OH}) The voltage at the output with the specified input conditions applied which should establish a high level at the output.

Low-Level Output Voltage (V_{OL}) The voltage at the output with the specified input conditions applied which should establish a low level at the output.

Low-Level Output Current (I_{OL}) The current flowing into the output at a specified low-level output voltage.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Response Time The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial condition sufficient to saturate the output to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Strobe Release Time The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the low logic level to the high logic level. Appropriate input conditions are assumed.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

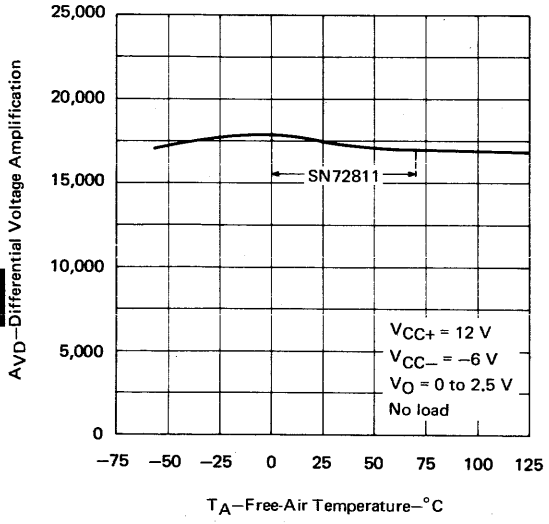


FIGURE 1

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

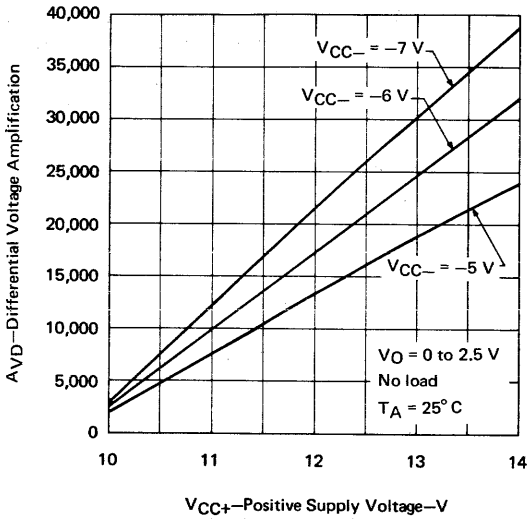


FIGURE 2

SN52811
VOLTAGE TRANSFER CHARACTERISTICS

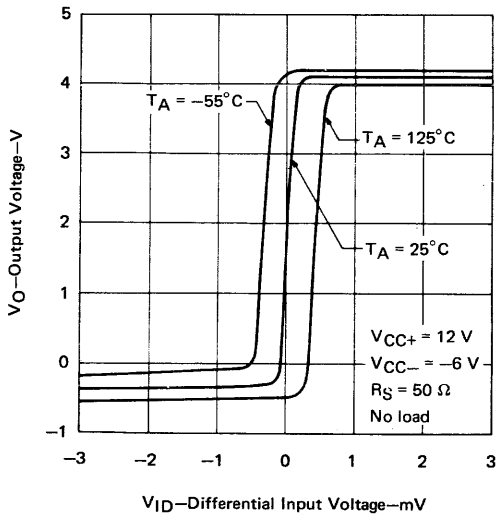


FIGURE 3

SN72811
VOLTAGE TRANSFER CHARACTERISTICS

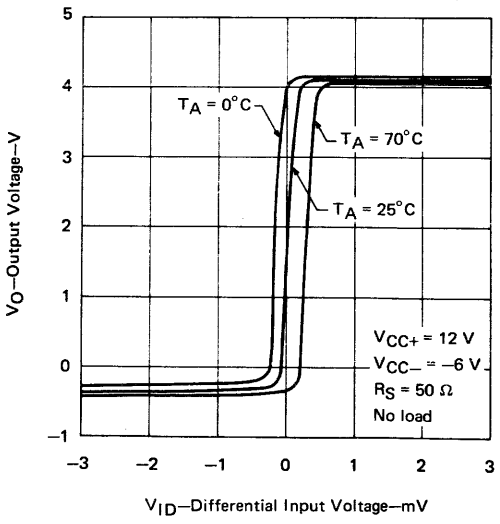


FIGURE 4

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

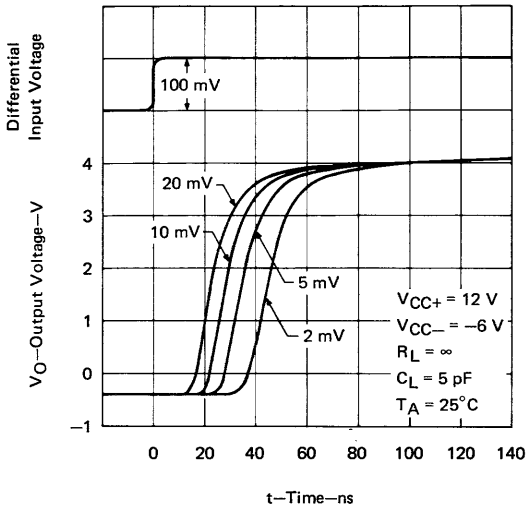


FIGURE 5

STROBE RELEASE TIME
FOR VARIOUS INPUT OVERDRIVES

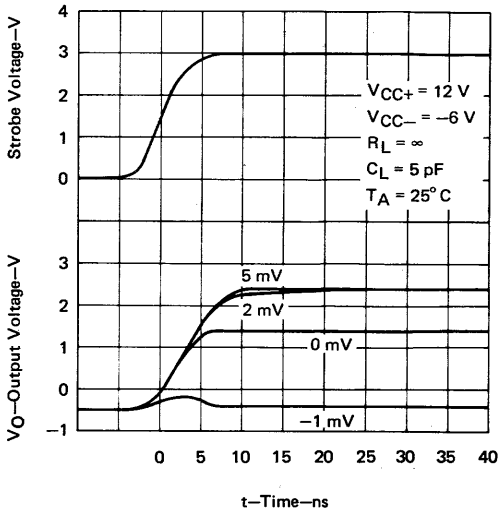


FIGURE 6

COMMON-MODE PULSE RESPONSE

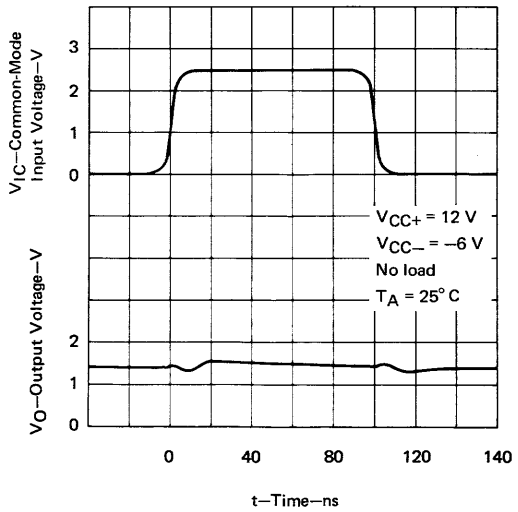
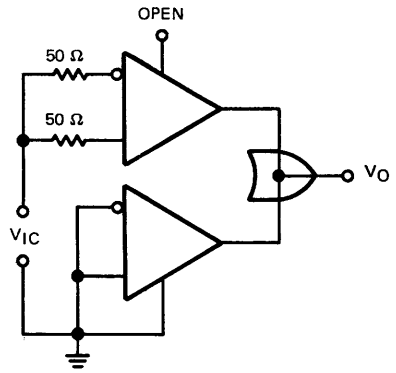


FIGURE 7



TEST CIRCUIT
FOR FIGURE 7

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

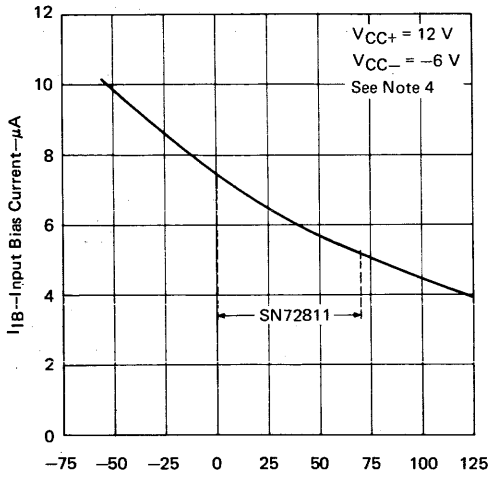


FIGURE 8

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

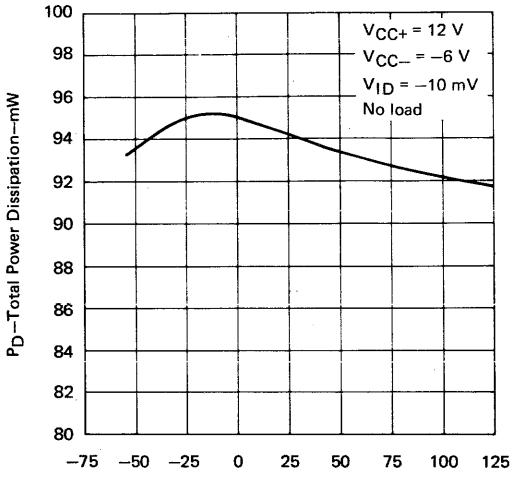


FIGURE 9

NOTE 4. These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52811, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for SN72811, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

THERMAL INFORMATION

SN52811
DISSIPATION DERATING CURVE

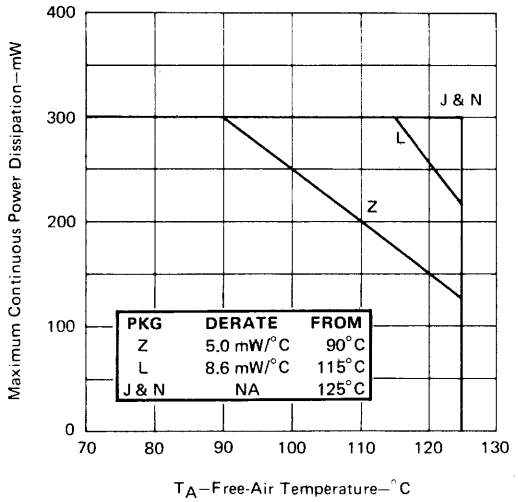


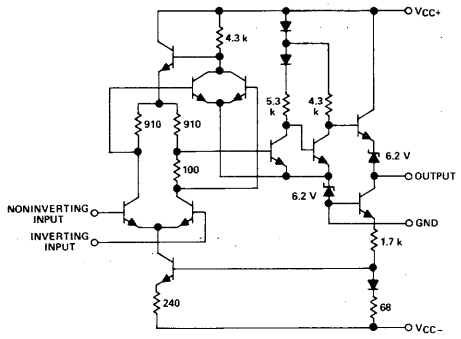
FIGURE 10

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN52820, SN72820
DUAL DIFFERENTIAL COMPARATORS

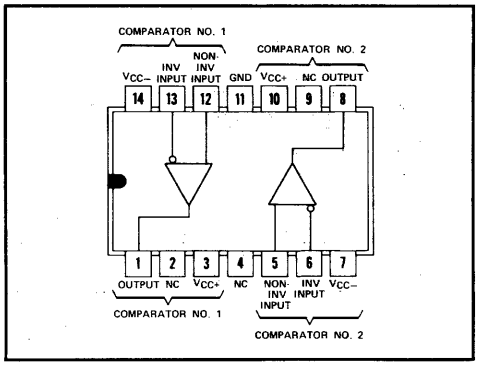
- Fast Response Times
- High Differential Voltage Amplification
- Low Offset Characteristics
- Outputs Compatible with Most TTL and DTL Circuits

schematic (each comparator)



Resistor values are in ohms.
Component values shown are nominal.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

description

The SN52820 and SN72820 are improved versions of the SN72720 dual high-speed voltage comparator. Each comparator has differential inputs and a low-impedance output. When compared with the SN72720, these circuits feature higher amplification (typically 33,000) due to an extra amplification stage and increased accuracy because of lower offset characteristics. They are particularly useful in applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector. The SN52820 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72820 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Peak output current ($t_w \leq 1$ s)	10 mA
Continuous total power dissipation: each comparator	300 mW
total package, (see Note 3)	600 mW
Operating free-air temperature range: SN52820 Circuits	−55°C to 125°C
SN72820 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For SN52820, this rating applies at (or below) 95°C free-air temperature. For operation above this temperature, derate linearly at the rate of 10.9 mW/°C. For SN72820, this rating applies at (or below) 70°C free-air temperature without derating.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN52820, SN72820
DUAL DIFFERENTIAL COMPARATORS

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52820			SN72820			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		0.6	2		1.6	3.5	mV
			Full range			3			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage	R_S = 50 Ω, See Note 4	MIN to 25°C		3	10		3	20	μV/°C
			25°C to MAX		3	10		3	20	
I_{IO}	Input offset current	See Note 4	25°C		0.75	3		1.8	5	μA
			MIN		1.8	7			7.5	
			MAX		0.25	3			7.5	
α_{IIO}	Average temperature coefficient of input offset current	See Note 4	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	See Note 4	25°C		7	15		7	20	μA
			MIN		12	25		9	30	
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0 to 2.5 V	25°C	12,500	33,000		10,000	33,000		
			Full range	10,000			8,000			
V_{OH}	High-level output voltage	V_{ID} = 5 mV, I_{OH} = 0	Full range		4§	5		4§	5	V
		V_{ID} = 5 mV, I_{OH} = −5 mA	Full range	2.5	3.6§		2.5	3.6§		
V_{OL}	Low-level output voltage	V_{ID} = −5 mV, I_{OL} = 0	Full range	−1	−0.5§	0‡	−1	−0.5§	0‡	V
I_{OL}	Low-level output current	V_{ID} = −5 mV, V_O = 0	25°C	2	2.4		1.6	2.4		mA
			MIN	1	2.3		0.5	2.4		
			MAX	0.5	2.3		0.5	2.4		
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	Full range	80	100§		70	100§		dB
I_{CC+}	Supply current from V_{CC+} (each comparator)	V_{ID} = −5 mV, No load	Full range		5.5§	9		5.5§	9	mA
I_{CC-}	Supply current from V_{CC-} (each comparator)		Full range		−3.5§	−7		−3.5§	−7	mA
P_D	Total power dissipation (each comparator)		Full range		90§	150		90§	150	mW

†Full range (MIN to MAX) for SN52820 is −55°C to 125°C and for the SN72820 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

§These typical values are at T_A = 25°C.

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52820, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1V at T_A = 125°C; for SN72820, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time	R_L = ∞, C_L = 5 pF, See Note 5		30	80	ns

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive.

For definition of terms and typical characteristic curves, see the SN52810/SN72810 data sheet on page 3-79.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPE	SN52733, SN72733	SN5510, SN7510	SN5511, SN7511	SN5512, SN7512	SN5514, SN7514	UNIT
Differential Voltage Amplification, Typ	10 to 400 (Adjustable)	93	3000	300	300	
Bandwidth (−3 dB), Typ	200 (Gain of 10)	40	3	80	80	MHz
Bandwidth (Unity-Gain), Typ	400	300	100	400	400	MHz
Input Offset Current, Typ	0.4	3	0.6	1	1	μA
Input Offset Voltage, Typ	1.5 (Gain of 400)	5	1	1 (can be nulled)	1	mV
Output Voltage Swing, Typ	4.7	4	5	3.4	3.4	V p-p
Packages	L, N	F, L	F, L, N	L	L	

CIRCUIT TYPES SN52733, SN72733
DIFFERENTIAL VIDEO AMPLIFIERS

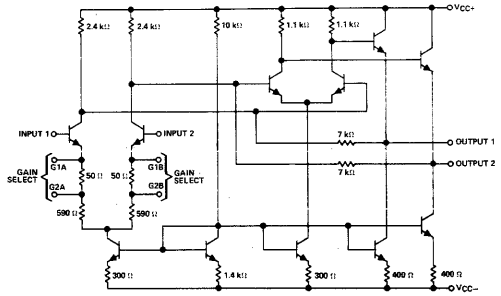
- 200 MHz Bandwidth
- 250 kΩ Input Resistance
- Selectable Nominal Amplification of 10, 100, or 400
- No Frequency Compensation Required

description

The SN52733 and SN72733 are monolithic two-stage video amplifiers with differential inputs and differential outputs.

Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

schematic



Component values shown are nominal

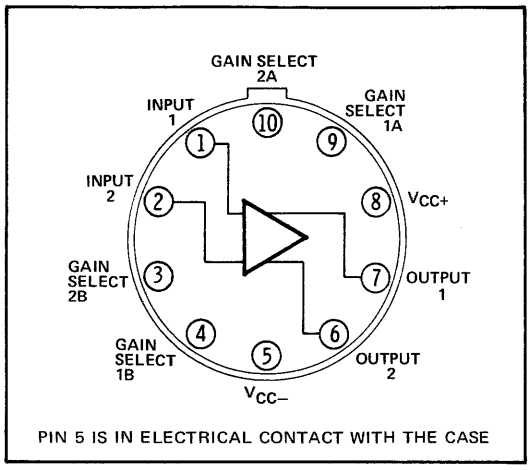
Fixed differential amplification of 10, 100, or 400 may be selected without external components, or amplification may be adjusted from 10 to 400 by the use of a single external resistor connected between G1A and G1B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disc-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

The SN52733 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72733 is characterized for operation from 0°C to 70°C.

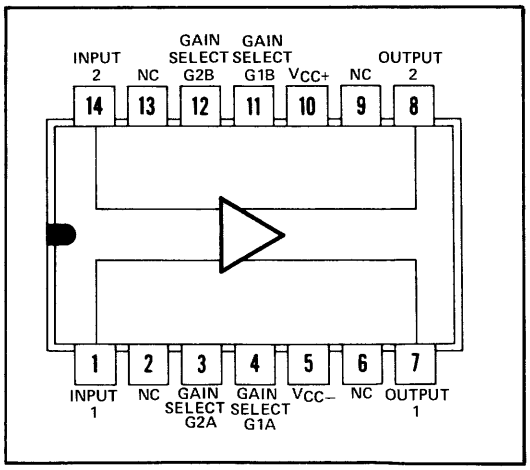
terminal assignments

L PLUG-IN-PACKAGE
(TOP VIEW)



PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52733	SN72733	UNIT
Supply voltage V_{CC+} (See Note 1)		8	8	V
Supply voltage V_{CC-} (See Note 1)		−8	−8	V
Differential input voltage		±5	±5	V
Common-mode input voltage		±6	±6	V
Output current		10	10	mA
Continuous total power dissipation (See Note 2 on the following page)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16" from case for 60 seconds	L package	300	300	°C
Lead temperature 1/16" from case for 10 seconds	N package	260	260	°C

NOTE 1: All voltage values, except differential input voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.

electrical characteristics, T_A = 25°C, V_{CC+} = 6 V, V_{CC-} = −6 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN† SELECT	SN52733 MIN	SN52733 TYP	SN52733 MAX	SN72733 MIN	SN72733 TYP	SN72733 MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OD} = 1 V	1	300	400	500	250	400	600	
				2	90	100	110	80	100	120	
				3	9	10	11	8	10	12	
BW	Bandwidth	2	R_S = 50 Ω	1		50			50		MHz
				2		90			90		
				3		200			200		
I_{IO}	Input offset current			Any		0.4	3		0.4	5	μA
I_{IB}	Input bias current			Any		9	20		9	30	μA
V_I	Input voltage range	1		Any	±1			±1			V
V_{OC}	Common-mode output voltage	1		Any	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1		1		0.6	1.5		0.6	1.5	V
				2 & 3		0.35	1		0.35	1.5	
V_{OPP}	Maximum peak-to-peak output voltage swing	1		Any	3	4.7		3	4.7		V
r_i	Input resistance	3	$V_{OD} \leq 1$ V	1		4			4		kΩ
				2	20	24		10	24		
				3		250			250		
r_o	Output resistance					20			20		Ω
C_i	Input capacitance	3	$V_{OD} \leq 1$ V	2		2			2		pF
CMRR	Common-mode rejection ratio	4	V_{IC} = ±1 V, f ≤ 100 kHz	2	60	86		60	86		dB
			V_{IC} = ±1 V, f = 5 MHz	2		70			70		
$\Delta V_{CC}/\Delta V_{IO}$	Supply voltage rejection ratio	1	ΔV_{CC+} = ± 0.5 V, ΔV_{CC-} = ± 0.5 V	2	50	70		50	70		dB
V_n	Broadband equivalent input noise voltage	5	BW = 1 kHz to 10 MHz	Any		12			12		μV
t_{pd}	Propagation delay time	2	R_S = 50 Ω, Output voltage step = 1 V	1		7.5			7.5		ns
				2		6.0	10		6.0	10	
				3		3.6			3.6		
t_r	Rise time	2	R_S = 50 Ω, Output voltage step = 1 V	1		10.5			10.5		ns
				2		4.5	10		4.5	12	
				3		2.5			2.5		
$I_{sink(max)}$	Maximum output sink current			Any	2.5	3.6		2.5	3.6		mA
I_{CC}	Supply current		No load, no signal	Any		16	24		16	24	mA

† The gain selection is made as follows:
Gain 1 . . . Gain Select pin G1A is connected to pin G1B, and pins G2A and G2B are open.
Gain 2 . . . Gain Select pin G1A and pin G1B are open, pin G2A is connected to pin G2B.
Gain 3 . . . All four gain-select pins are open.

DEFINITION OF TERMS

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in voltage between the output terminals to the change in voltage between the input terminals producing it.

Bandwidth (BW) The range of frequencies within which the differential gain of the amplifier is not more than 3 dB below its low-frequency value.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the inputs grounded.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the inputs grounded.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Common-Mode Output Voltage (V_{OC}) The average of the d-c voltages at the two output terminals.

Output Offset Voltage (V_{OO}) The difference between the d-c voltages at the two output terminals when the input terminals are grounded.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between either output terminal and ground.

Input Capacitance (C_i) The capacitance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in output offset voltage referred to the input.

Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) The ratio of the change in power supply voltages to the change in output offset voltage referred to the input. For these devices, both supply voltages are varied symmetrically.

Propagation Delay Time (t_{pd}) The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Maximum Output Sink Current ($I_{sink(max)}$) The maximum available current into either output terminal when that output is at its most negative potential.

Supply Current (I_{CC}) The average of the magnitudes of the two supply currents.

NOTE 2: For SN52733 in the L package, this rating applies at (or below) 90°C free-air temperature with derating above that temperature at the rate of 8.3 mW/°C. For SN52733 in the N package, this rating applies at (or below) 105°C free-air temperature with derating above that temperature at the rate of 11.1 mW/°C. For SN72733 in either package, this rating applies at (or below) 70°C free-air temperature without derating.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

test circuits

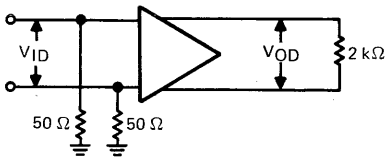


FIGURE 1

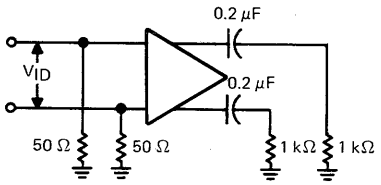


FIGURE 2

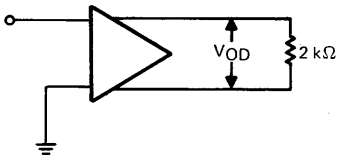


FIGURE 3

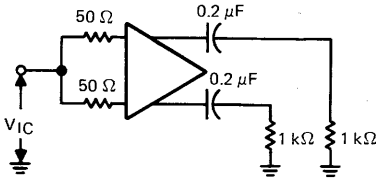


FIGURE 4

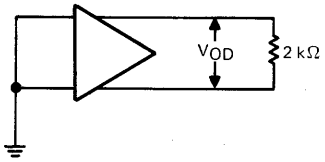
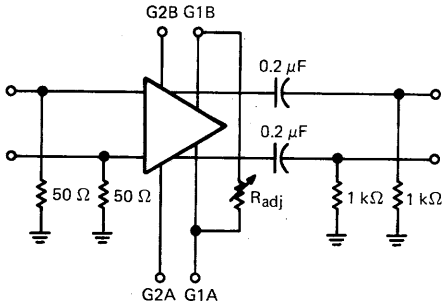


FIGURE 5



VOLTAGE AMPLIFICATION ADJUSTMENT

FIGURE 6

TYPICAL CHARACTERISTICS

PHASE SHIFT
vs
FREQUENCY

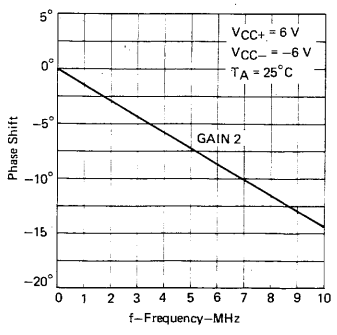


FIGURE 7

PHASE SHIFT
vs
FREQUENCY

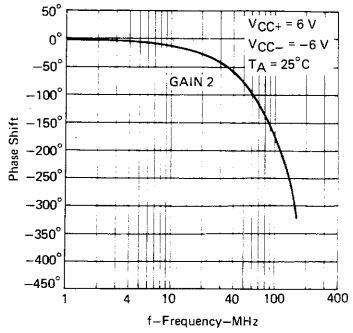


FIGURE 8

TYPICAL CHARACTERISTICS

VOLTAGE AMPLIFICATION
(SINGLE-ENDED OR DIFFERENTIAL)
vs
TEMPERATURE

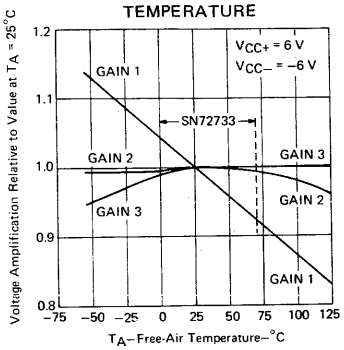


FIGURE 9

VOLTAGE AMPLIFICATION
(SINGLE-ENDED OR DIFFERENTIAL)
vs
SUPPLY VOLTAGE

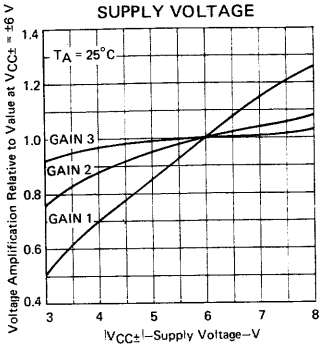


FIGURE 10

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
RESISTANCE BETWEEN G1A AND G1B

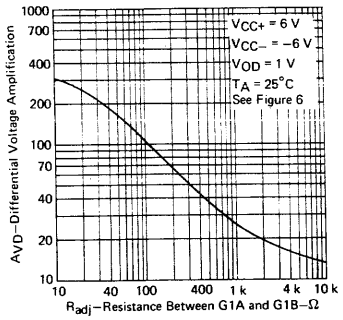


FIGURE 11

SINGLE-ENDED VOLTAGE AMPLIFICATION
vs
FREQUENCY

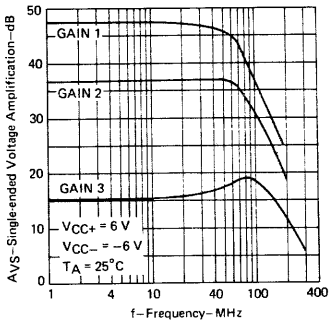


FIGURE 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

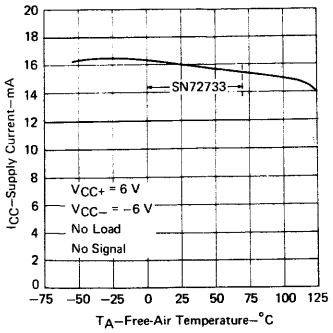


FIGURE 13

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

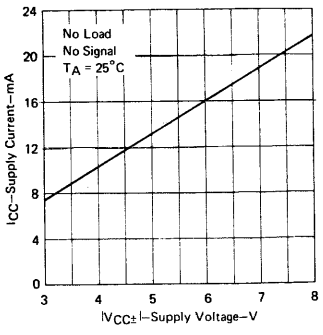


FIGURE 14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

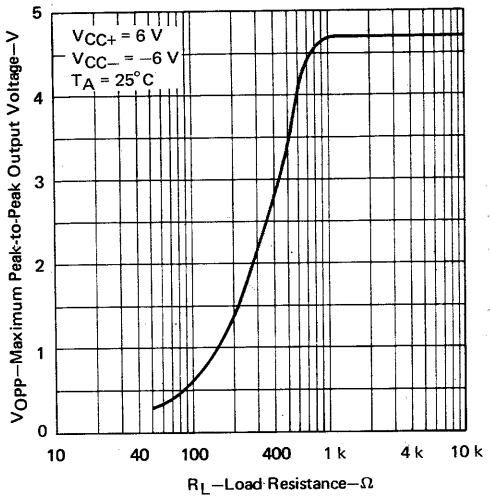


FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

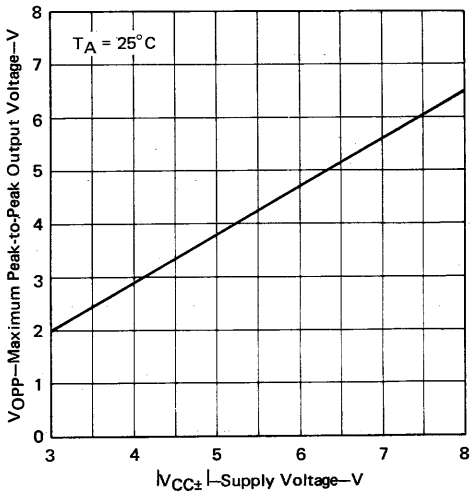


FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

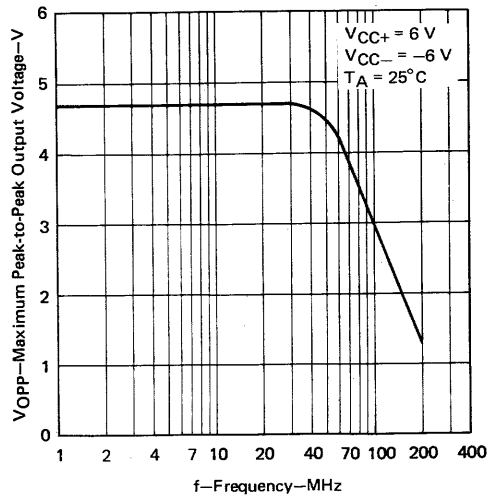


FIGURE 17

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

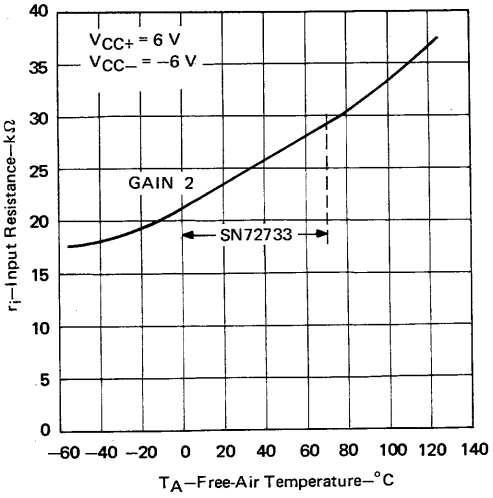


FIGURE 18

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

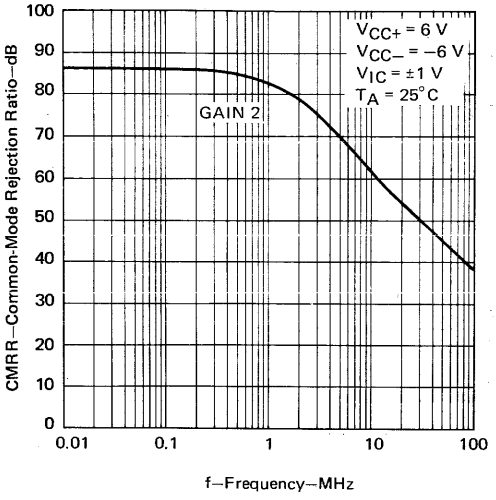


FIGURE 19

DIFFERENTIAL INPUT OVERLOAD RECOVERY TIME
vs
DIFFERENTIAL INPUT VOLTAGE

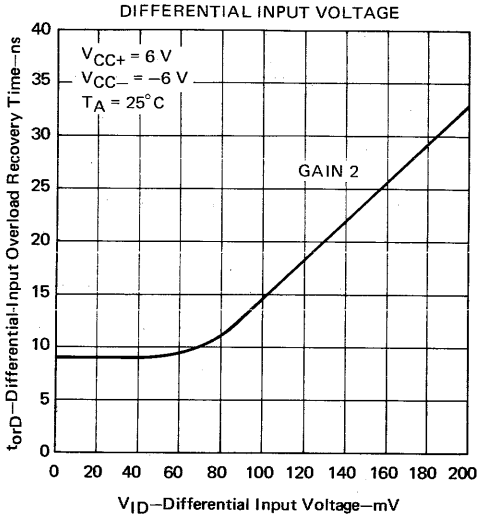


FIGURE 20

PULSE RESPONSE
AS A FUNCTION OF
SUPPLY VOLTAGE

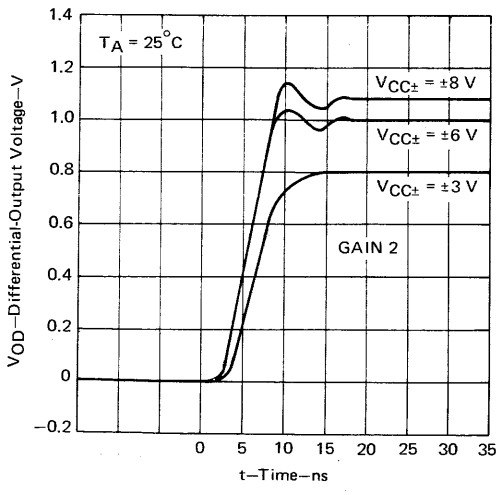


FIGURE 21

PULSE RESPONSE
AS A FUNCTION OF GAIN

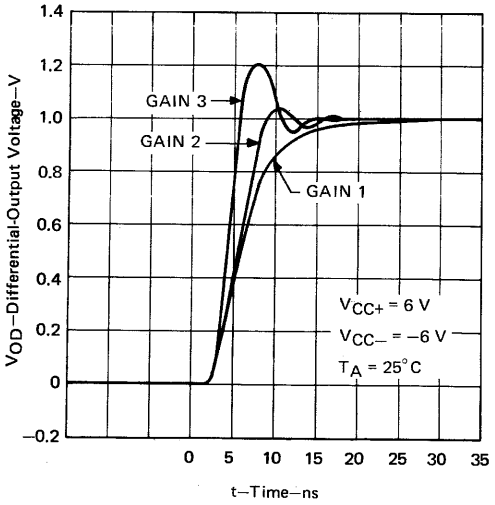


FIGURE 22

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE SN5510
DIFFERENTIAL VIDEO AMPLIFIER

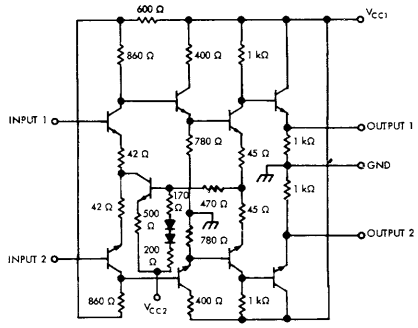
WIDE-BAND VIDEO AMPLIFIER
FEATURING
Flat Frequency Response with Low Phase-Shift from DC to 40 MHz

description

This wide-band video amplifier features a flat frequency response and low phase-shift from dc to 40 MHz. Differential inputs and outputs are provided which permit it to be used as a high-frequency differential amplifier.

Elements of the SN5510 video-amplifier bar include transistors with transition frequency as high as 1.2 GHz under low-current and low-V_{CE} conditions. Circuit frequency response from dc to greater than 100 MHz is possible.

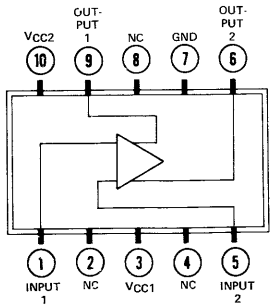
schematic



Component values shown are nominal.

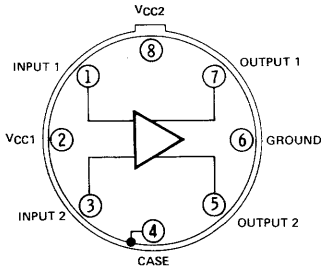
terminal assignments

F
FLAT PACKAGE (TOP VIEW)



THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

L
PLUG-IN PACKAGE (TOP VIEW)



THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

NC—No internal connection

CIRCUIT TYPE SN5510
DIFFERENTIAL VIDEO AMPLIFIER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (See Note 1): V_{CC1} . . . . . +8 V
V_{CC2} . . . . . −8 V
Differential input voltage . . . . . 5 V
Positive input voltage (See Note 1) . . . . . V_{CC1}
Negative input voltage (See Note 1) . . . . . V_{CC2}
Operating free-air temperature ranges: SN5510F . . . . . −55°C to 70°C
SN5510L . . . . . −55°C to 100°C
Operating case temperature ranges: SN5510F . . . . . −55°C to 100°C
SN5510L . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These voltage values are with respect to network ground.

3

electrical characteristics, T_A = 25°C, V_{CC1} = +6 V, V_{CC2} = −6 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DO}	Differential-output offset voltage	1			0.5	1.3	V
$V_{CMO(av)}$	Average common-mode output offset voltage	1		2.6	3.1	3.5	V
I_{in}	Input current	1			40	80	μA
I_{DI}	Differential-input offset current	1			3	20	μA
D_S	Single-ended output distortion	2	Load resistance = 5 kΩ, input distortion < 0.2%, V_{out} = 1 V rms, f = 10 kHz		1.5	5	%
$V_{N(in)}$	Equivalent average input noise voltage	3	Single-ended, R_S = 0, f = 10 Hz to 500 kHz		5		μV
V_{CMIM}	Maximum common-mode input voltage				±1		V
A_{vs}	Small-signal voltage gain	2	Single-ended, load resistance = 5 kΩ, f = 100 kHz	75	93	110	
A_{vcm}	Common-mode-input voltage gain	4	Single-ended, load resistance = 5 kΩ, V_{in} = 0.3 V rms, f = 100 kHz		−45	−30	dB
CMRR	Common-mode rejection ratio	4	Load resistance = 5 kΩ, f = 100 kHz		85		dB
BW	Bandwidth (−3 dB)	2			40		MHz
r_{in}	Input resistance	5	f = 100 kHz		6		kΩ
C_{in}	Input capacitance	5	f = 100 kHz		7		pF
z_{out}	Output impedance	5	f = 100 kHz		35		Ω
P_T	Total power dissipation	1	No input signal, no external load		165	220	mW
t_r	Rise time	6	Single-ended, V_{in} = 5 mV		9	12	ns
t_f	Fall time	6	Single-ended, V_{in} = 5 mV		9	12	ns

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

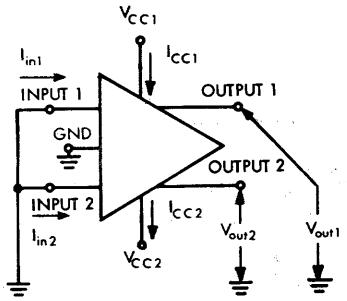
letter symbol and parameter definitions

V_{DO}	The d-c differential voltage that exists between the output terminals when the input terminals are at ground.
$V_{CMO(av)}$	The average of the d-c output voltages with respect to ground when the input terminals are grounded.
I_{DI}	The difference in the currents into the two input terminals.
V_{CMIM}	The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.
CMRR	The ratio of the differential-mode voltage gain to the common-mode voltage gain.
BW	The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.

3

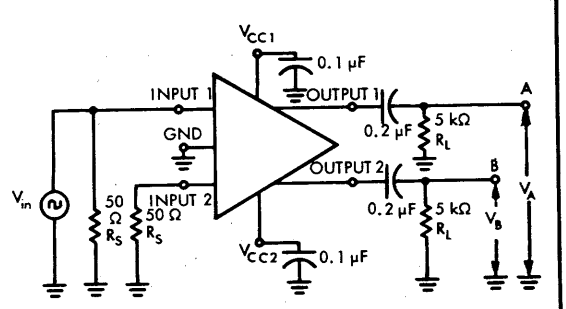
PARAMETER MEASUREMENT INFORMATION

test circuits



1. $V_{DO} = |V_{out1} - V_{out2}|$
2. $V_{CMO(av)} = \dfrac{V_{out1} + V_{out2}}{2}$
3. $I_{DI} = |I_{in1} - I_{in2}|$
4. $P_T = |V_{CC1} \bullet I_{CC1}| + |V_{CC2} \bullet I_{CC2}|$

FIGURE 1



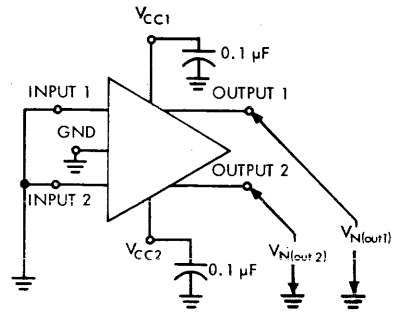
1. Single-ended output distortion is measured at A or B with V_A or V_B = 1 V rms, input distortion < 0.2%, and f = 10 kHz.
2. $A_{VS} = \left|\dfrac{V_A \text{ or } V_B}{V_{in}}\right|$

where: V_{in} = 1 mV rms and f = 100 kHz.

FIGURE 2

PARAMETER MEASUREMENT INFORMATION

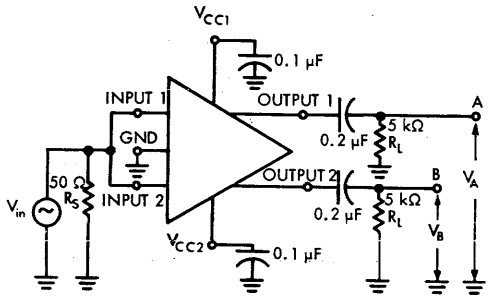
test circuits (continued)



1. $V_{\overline{N(in)}} = \dfrac{V_{\overline{N(out1)}} \text{ or } V_{\overline{N(out2)}}}{A_{VS}}$

where: $V_{\overline{N(out)}}$ = true rms broad-band noise voltage from 10 Hz to 500 kHz.

FIGURE 3



1. $A_{vcm} = 20 \text{ Log} \left| \dfrac{V_A \text{ or } V_B}{V_{in}} \right|$

where: V_{in} = 0.3 V rms and f = 100 kHz.

2. CMRR = 20 Log $A_{VS} - A_{vcm}$

FIGURE 4

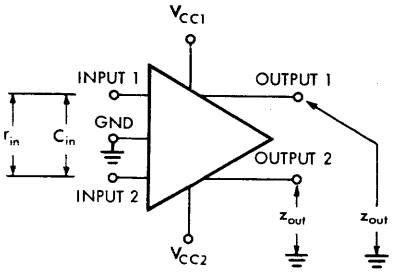
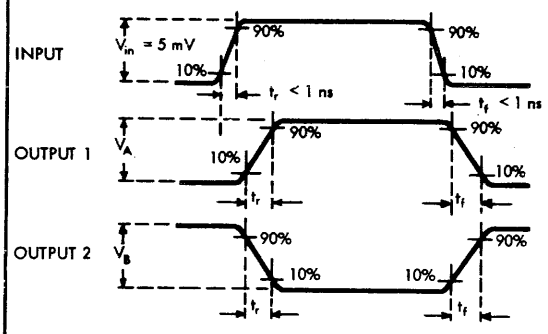


FIGURE 5



1. Test circuit is identical to that shown in Figure 2.

FIGURE 6 — t_r and t_f VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS†

AVERAGE COMMON-MODE OUTPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

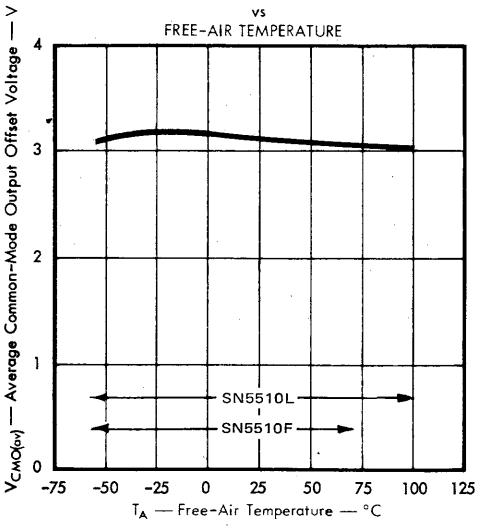


FIGURE 7

INPUT CURRENT
vs
FREE-AIR TEMPERATURE

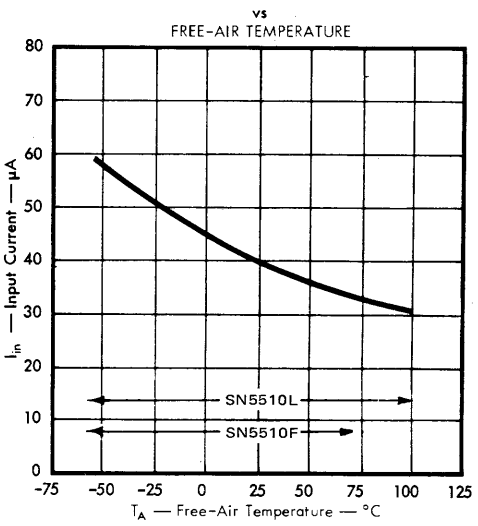


FIGURE 8

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

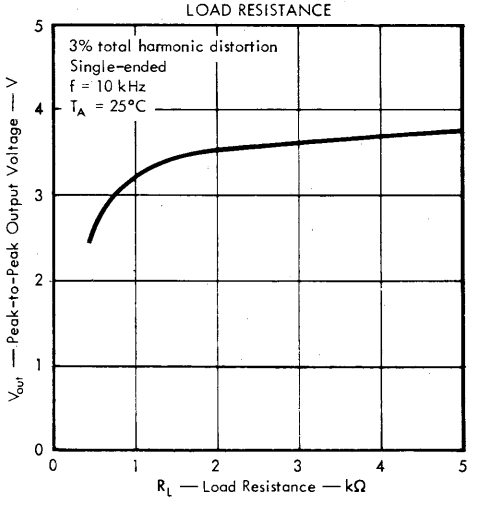


FIGURE 9

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

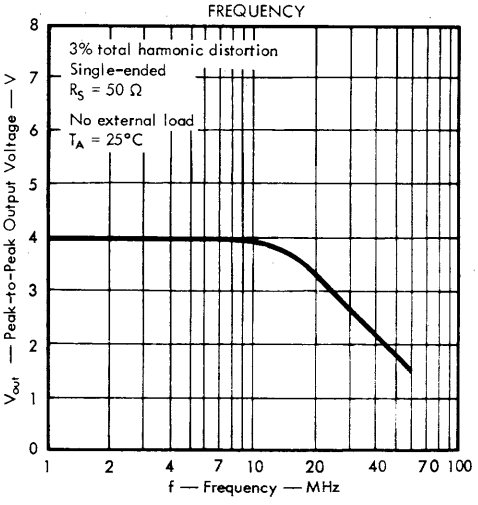


FIGURE 10

†Unless otherwise noted $V_{CC1} = +6$ V, $V_{CC2} = -6$ V.

TYPICAL CHARACTERISTICS†

SMALL-SIGNAL VOLTAGE GAIN
vs
FREE-AIR TEMPERATURE

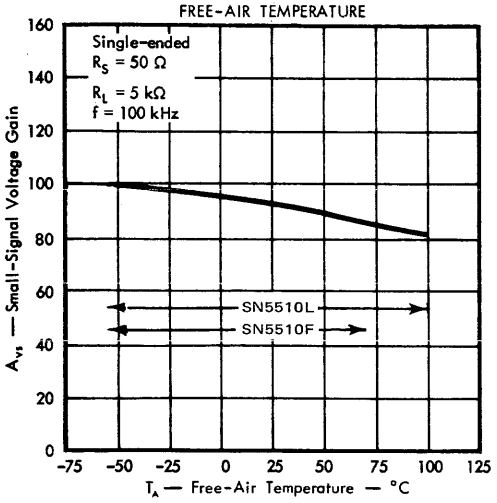


FIGURE 11

SMALL-SIGNAL VOLTAGE GAIN VARIATION
vs
SUPPLY VOLTAGE

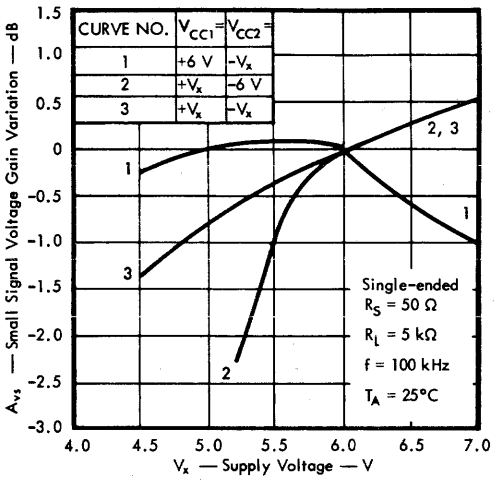


FIGURE 12

SMALL-SIGNAL VOLTAGE GAIN
vs
FREQUENCY

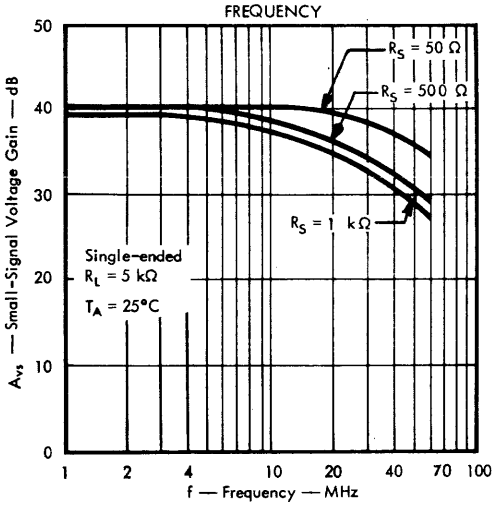


FIGURE 13

SMALL-SIGNAL VOLTAGE GAIN
vs
FREQUENCY

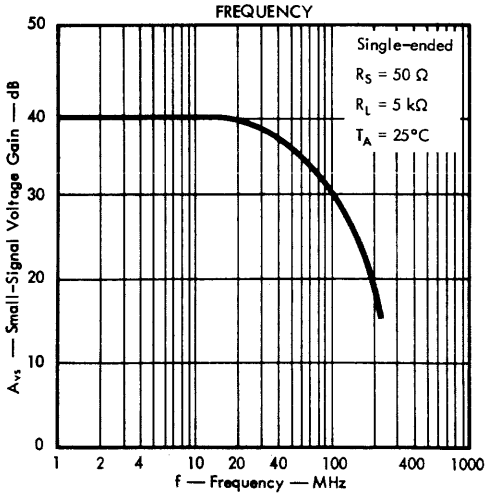


FIGURE 14

†Unless otherwise noted V_{CC1} = +6 V, V_{CC2} = −6 V.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS†

PHASE SHIFT
vs
FREQUENCY

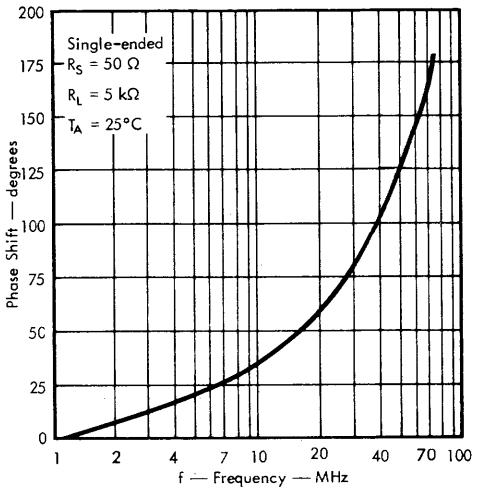


FIGURE 15

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

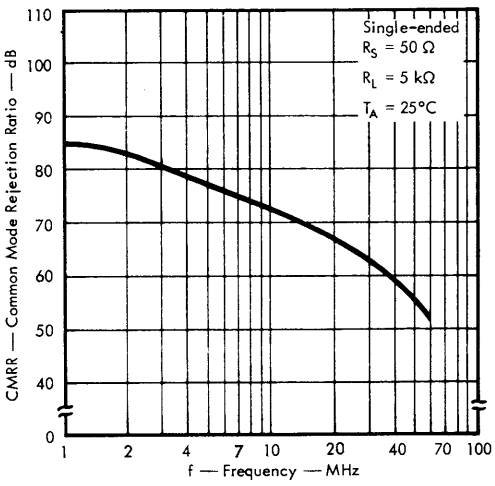
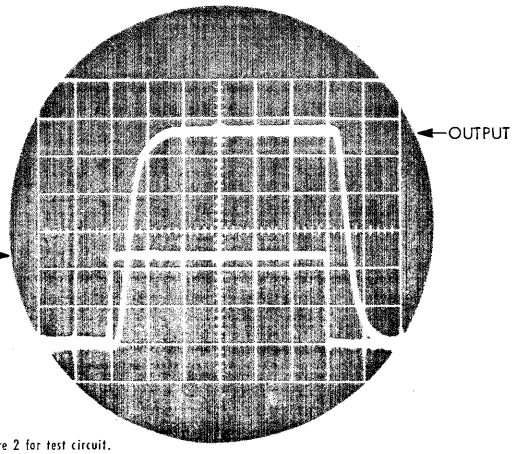


FIGURE 16

†V_{CC1} = +6 V and V_{CC2} = −6 V.



SCALES
Horizontal: 10 ns/division
Vertical: Output = 200 mV/division
Input = 5 mV/division

NOTE: See Figure 2 for test circuit.

FIGURE 17 — OSCILLOSCOPE PRESENTATION OF PULSE RESPONSE

CIRCUIT TYPE SN7510
DIFFERENTIAL VIDEO AMPLIFIER

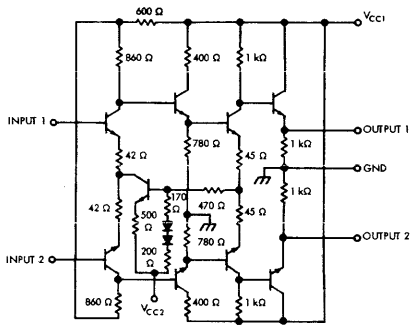
WIDE-BAND VIDEO AMPLIFIER
FEATURING
Flat Frequency Response with Low Phase-Shift from DC to 40 MHz

description

This wide-band video amplifier features a flat frequency response and low phase-shift from dc to 40 MHz. Differential inputs and outputs are provided which permit it to be used as a high-frequency differential amplifier.

Elements of the SN7510 video-amplifier bar include transistors with transition frequency as high as 1.2 GHz under low-current and low-V_{CE} conditions. Circuit frequency response from dc to greater than 100 MHz is possible.

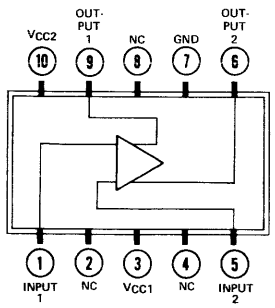
schematic



Component values shown are nominal.

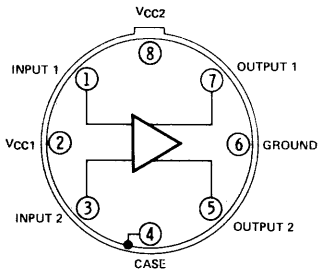
terminal assignments

F
FLAT PACKAGE (TOP VIEW)



THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

L
PLUG-IN PACKAGE (TOP VIEW)



THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

NC—No internal connection

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (See Note 1): V_{CC1} . . . . . +8 V
V_{CC2} . . . . . −8 V
Differential input voltage . . . . . 5 V
Positive input voltage (See Note 1) . . . . . V_{CC1}
Negative input voltage (See Note 1) . . . . . V_{CC2}
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These voltage values are with respect to network ground.

3

electrical characteristics, $T_A = 25°C$, $V_{CC1} = +6$ V, $V_{CC2} = -6$ V

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DO}	Differential-output offset voltage	1			0.5	2	V
$V_{CMO(av)}$	Average common-mode output offset voltage	1		2	3	4	V
I_{in}	Input current	1			50	100	μA
I_{DI}	Differential-input offset current	1			5	30	μA
V_{OM}	Maximum peak-to-peak output voltage	2	Single-ended, load resistance = 5 kΩ, f = 100 kHz, V_{in} = 20 mV rms		4.5		V
D_S	Single-ended output distortion	2	Load resistance = 5 kΩ, input distortion < 0.2%, V_{out} = 1 V rms, f = 10 kHz		2		%
$V_{\overline{N(in)}}$	Equivalent average input noise voltage	3	Single-ended, R_S = 0, f = 10 Hz to 500 kHz		5		μV
V_{CMIM}	Maximum common-mode input voltage				±1		V
A_{vs}	Small-signal voltage gain	2	Single-ended, load resistance = 5 kΩ, f = 100 kHz	60	90	120	
A_{vcm}	Common-mode-input voltage gain	4	Single-ended, load resistance = 5 kΩ, V_{in} = 0.3 V rms, f = 100 kHz		−40	−20	dB
CMRR	Common-mode rejection ratio	4	Load resistance = 5 kΩ, f = 100 kHz		85		dB
BW	Bandwidth (-3 dB)	2			40		MHz
r_{in}	Input resistance	5	f = 100 kHz		6		kΩ
C_{in}	Input capacitance	5	f = 100 kHz		7		pF
z_{out}	Output impedance	5	f = 100 kHz		35		Ω
P_T	Total power dissipation	1	No input signal, no external load		165	220	mW
t_r	Rise time	6	Single-ended, V_{in} = 5 mV		10	15	ns
t_f	Fall time	6	Single-ended, V_{in} = 5 mV		10	15	ns

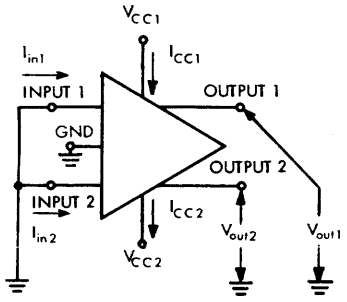
letter symbol and parameter definitions

V_{DO}	The d-c differential voltage that exists between the output terminals when the input terminals are at ground.
$V_{CMO(av)}$	The average of the d-c output voltages with respect to ground when the input terminals are grounded.
I_{DI}	The difference in the currents into the two input terminals.
V_{OM}	The maximum peak-to-peak output voltage swing that can be obtained without clipping.
V_{CMIM}	The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.
CMRR	The ratio of the differential-mode voltage gain to the common-mode voltage gain.
BW	The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.

3

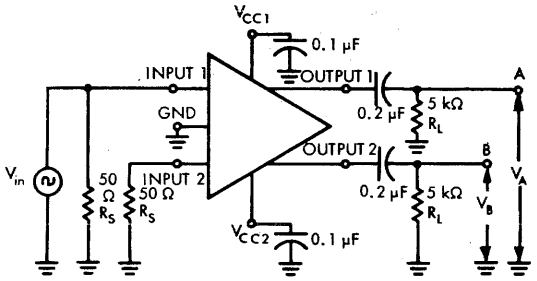
PARAMETER MEASUREMENT INFORMATION

test circuits



1. $V_{DO} = |V_{out1} - V_{out2}|$
2. $V_{CMO(av)} = \dfrac{V_{out1} + V_{out2}}{2}$
3. $I_{DI} = |I_{in1} - I_{in2}|$
4. $P_T = |V_{CC1} \cdot I_{CC1}| + |V_{CC2} \cdot I_{CC2}|$

FIGURE 1



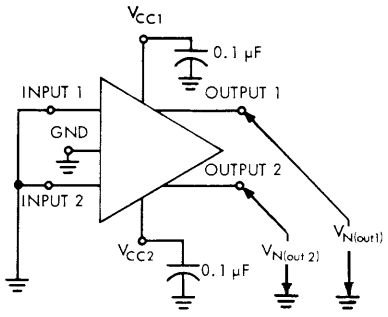
1. Single-ended output distortion is measured at A or B with V_A or V_B = 1 V rms, input distortion < 0.2%, and f = 10 kHz.
2. $A_{VS} = \left|\dfrac{V_A \text{ or } V_B}{V_{in}}\right|$
   where: V_{in} = 1 mV rms and f = 100 kHz.
3. $V_{OM} = V_A$ or V_B

FIGURE 2

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

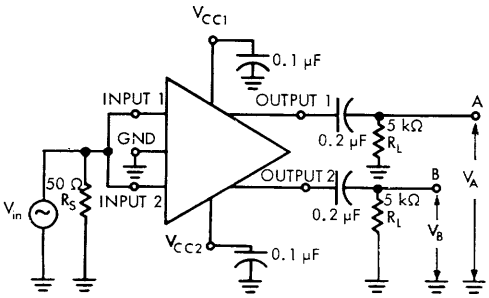
test circuits (continued)



1. $V_{\overline{N(in)}} = \dfrac{V_{\overline{N(out1)}} \text{ or } V_{\overline{N(out2)}}}{A_{VS}}$

where: $V_{\overline{N(out)}}$ = true rms broad-band noise voltage from 10 Hz to 500 kHz.

FIGURE 3



1. $A_{vcm} = 20 \text{ Log} \left| \dfrac{V_A \text{ or } V_B}{V_{in}} \right|$

where: V_{in} = 0.3 V rms and f = 100 kHz.

2. $CMRR = 20 \text{ Log } A_{VS} - A_{vcm}$

FIGURE 4

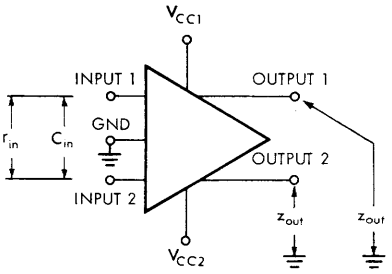
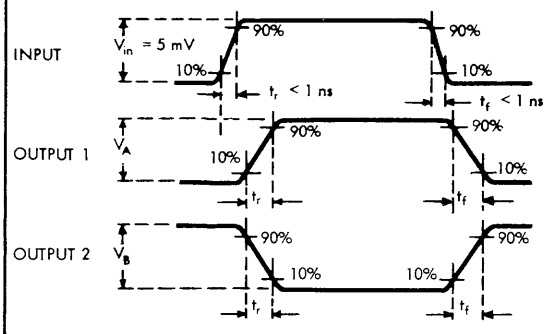


FIGURE 5



1. Test circuit is identical to that shown in Figure 2.

FIGURE 6 — t_r and t_f VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS†

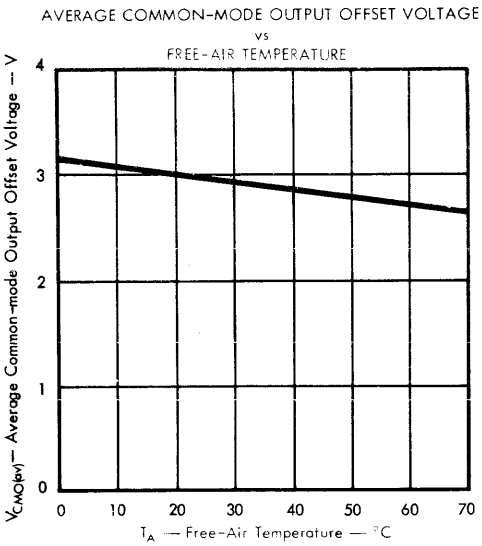


FIGURE 7

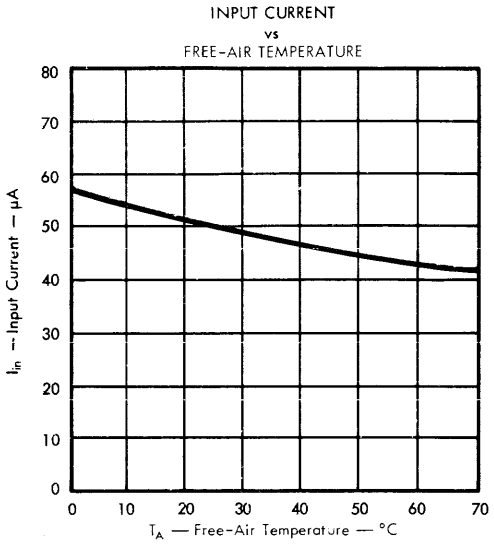


FIGURE 8

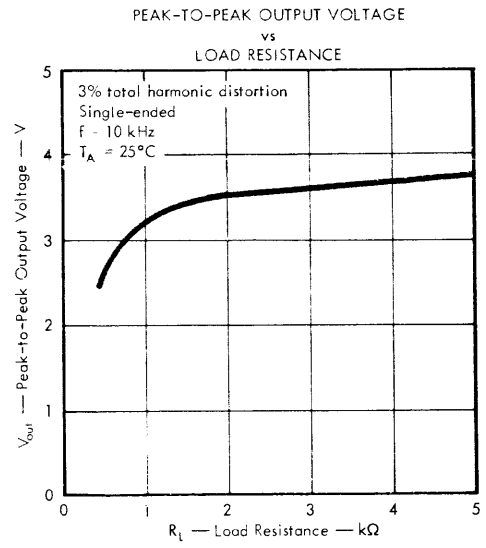


FIGURE 9

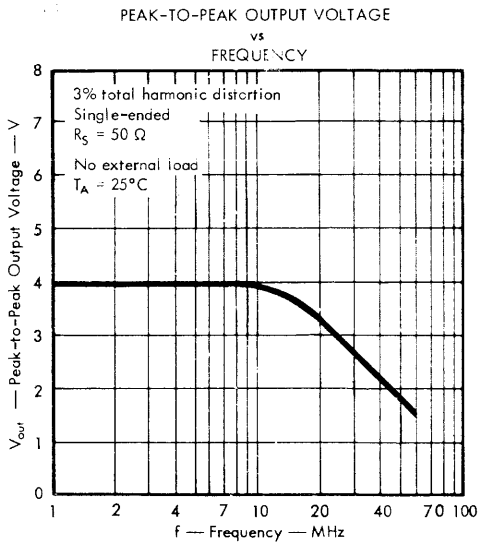


FIGURE 10

† Unless otherwise noted V_{CC1} = +6 V, V_{CC2} = −6 V.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS†

SMALL-SIGNAL VOLTAGE GAIN
vs
FREE-AIR TEMPERATURE

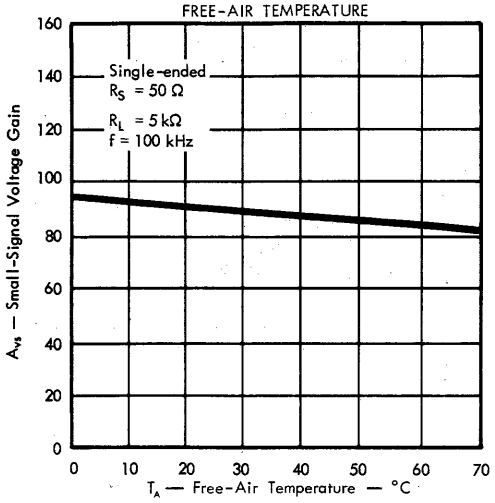


FIGURE 11

SMALL-SIGNAL VOLTAGE GAIN VARIATION
vs
SUPPLY VOLTAGE

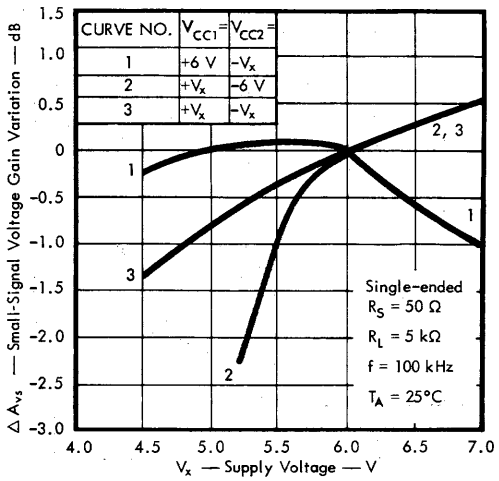


FIGURE 12

SMALL-SIGNAL VOLTAGE GAIN
vs
FREQUENCY

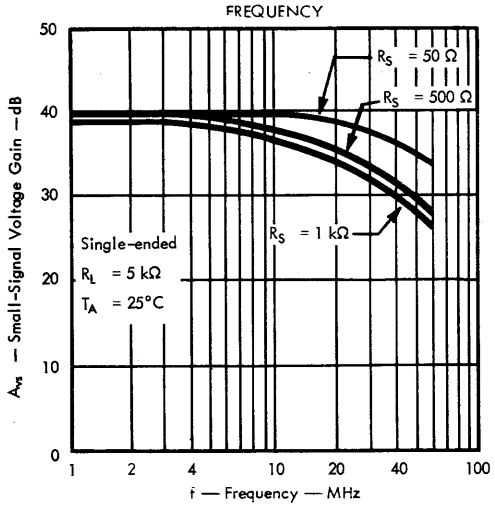


FIGURE 13

SMALL-SIGNAL VOLTAGE GAIN
vs
FREQUENCY

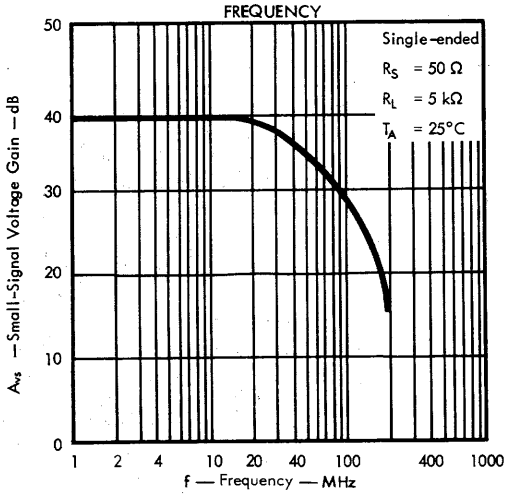


FIGURE 14

† Unless otherwise noted $V_{CC1} = +6$ V, $V_{CC2} = -6$ V.

TYPICAL CHARACTERISTICS†

PHASE SHIFT
vs
FREQUENCY

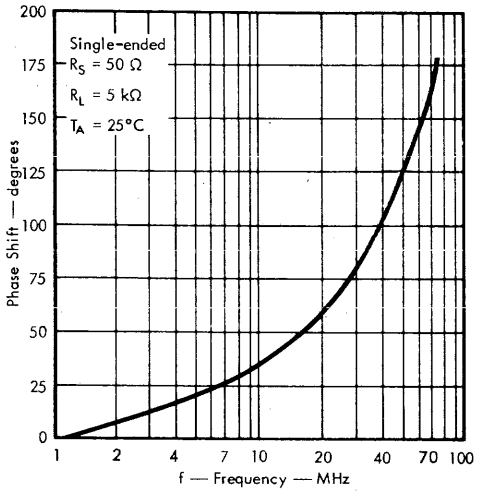


FIGURE 15

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

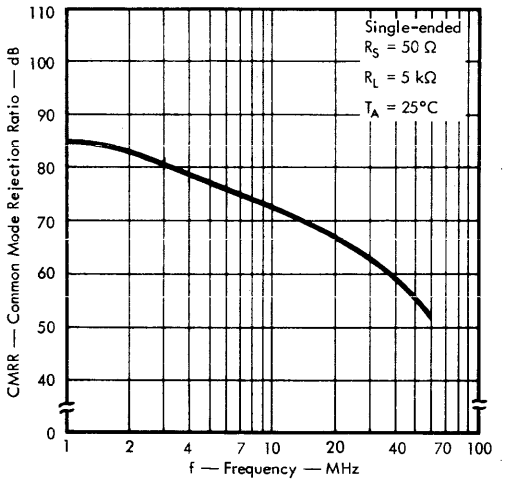


FIGURE 16

† V_{CC1} = +6 V and V_{CC2} = −6 V.

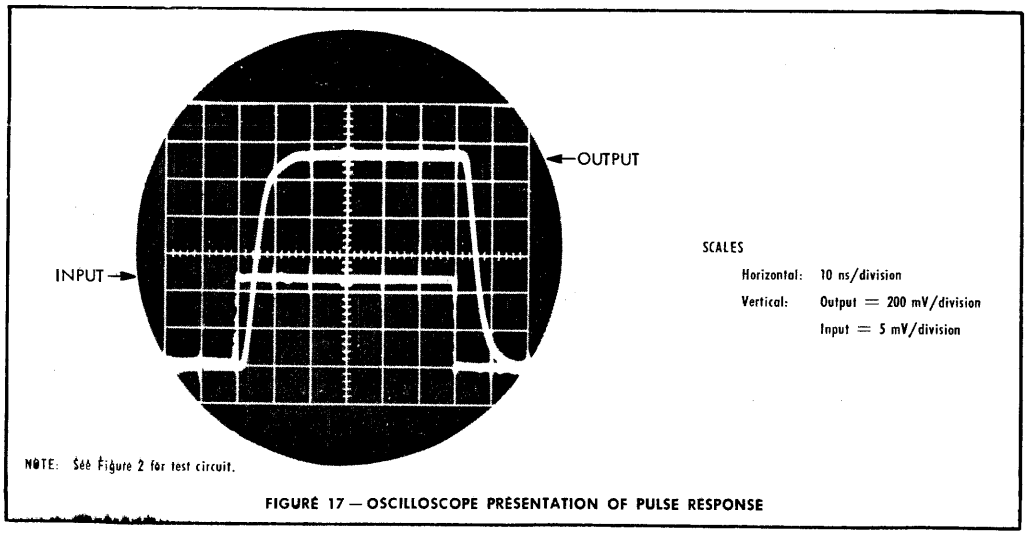


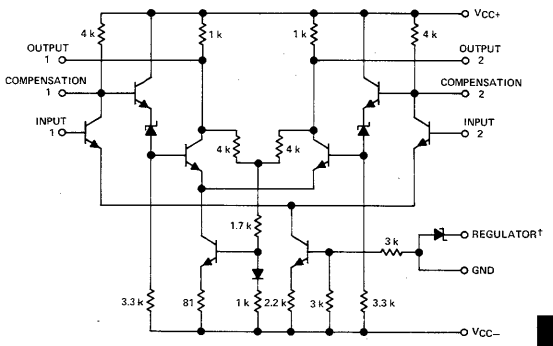
FIGURE 17 — OSCILLOSCOPE PRESENTATION OF PULSE RESPONSE

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5511, SN7511
DIFFERENTIAL VIDEO AMPLIFIERS

- Low Common-Mode Offset Voltage
- High Common-Mode Rejection Ratio
- High Gain-Bandwidth Product

schematic



Resistor values are nominal in ohms.

† Regulator terminal is used only with single supply. See description.

description

The SN5511 and SN7511 are wide-band amplifiers with differential inputs and outputs. High gain and low offset voltage permit use in applications requiring feedback. Frequency characteristics are such that a stable closed-loop configuration with 30-dB gain results in a 30-MHz bandwidth.

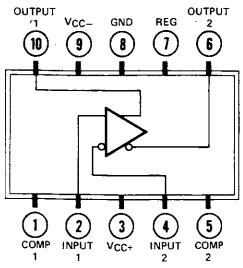
Accessibility to first-stage collectors makes offset balancing and frequency compensation possible with minimal effect on input and frequency characteristics.

The base of the first-stage current-source transistor is made available to permit operation from either a single 12-volt power supply or two 6-volt power supplies. For the latter, leave the regulator terminal open and connect the positive terminal of one supply to V_{CC+}, the negative terminal of the other supply to V_{CC-}, and the remaining terminals of the two supplies to the device ground terminal. For operation from a single 12-volt supply, connect the positive terminal of the supply to both the V_{CC+} and regulator terminals and connect the negative terminal to V_{CC-}. In either case, the device ground terminal is the reference for single-ended input and output voltages.

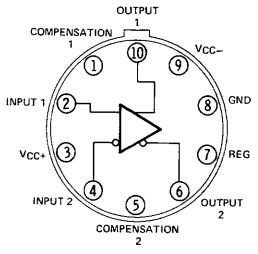
The wide bandwidth and high gain allow this amplifier to be used in a variety of applications where a stable differential video amplifier is required. Low common-mode offset voltage extends possible uses to comparators and direct-coupled amplifiers. The SN5511 is characterized for operation over the full military temperature range of –55°C to 125°C; the SN7511 is characterized for operation from 0°C to 70°C.

terminal assignments

F
FLAT PACKAGE (TOP VIEW)

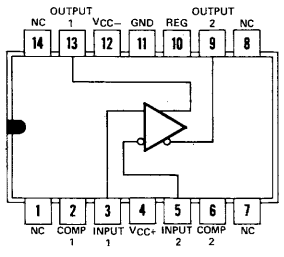


L
PLUG-IN PACKAGE (TOP VIEW)



ALL LEADS ARE ELECTRICALLY INSULATED FROM THE CASE

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC – No internal connection

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	8 V
Supply voltage V_{CC-} (see Note 1)	−8 V
Input voltage, either input to ground	±6 V
Differential input voltage	±6 V
Continuous total power dissipation at (or below) 55°C free-air temperature (see Note 2)	500 mW
Operating free-air temperature range: SN5511 Circuits	−55°C to 125°C
SN7511 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds, F and L packages	300°C
Lead temperature 1/16 inch from case for 10 seconds, N package	260°C

NOTES: 1. All voltage values, unless otherwise specified, are with respect to the network ground terminal.
2. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

3

electrical characteristics, V_{CC+} = 6 V, V_{CC-} = −6 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†	SN5511 MIN	SN5511 TYP	SN5511 MAX	SN7511 MIN	SN7511 TYP	SN7511 MAX	UNIT
A_{VD}	Large-signal differential voltage amplification		1	f ≤ 1 kHz, No load		3000					
				f ≤ 1 kHz, R_L = 5 kΩ		1200			600		
A_{VS}	Large-signal single-ended voltage amplification		2	f ≤ 1 kHz, R_L = 5 kΩ	400	600		250	300		
BW	Bandwidth	−3 dB		R_S = 500 Ω, No load		3			3		MHz
		Unity gain				100			100		
V_{IO}	Input offset voltage					1	5		1	5	mV
α_{VIO}	Average temperature coefficient of input offset voltage			T_A = −55°C to 25°C		4					μV/°C
				T_A = 25°C to 125°C		2					
				T_A = 0°C to 25°C					4		
				T_A = 25°C to 70°C					2		
I_{IO}	Input offset current					0.6	7		0.6	10	μA
I_{IB}	Input bias current					10	15		15	20	μA
V_I	Input voltage range		3		+2.5 −2			±1			V
V_{OO}	Output offset voltage			No load		0.35			0.35		V
				R_L = 500 Ω		0.17			0.17		
V_{OPP}	Maximum peak-to-peak output voltage swing		2	f ≤ 1 kHz, R_L = 5 kΩ	2.5	5		1.5	3		V
				f ≤ 1 kHz, R_L = 500 Ω		3			2		
z_{id}	Differential input impedance			f = 1 kHz		5			5		kΩ
z_{os}	Single-ended output impedance			f = 1 kHz		800			800		Ω
CMRR	Common-mode rejection ratio		3	f ≤ 100 kHz, No load, See Note 3	59	95		52	90		dB
P_D	Total power dissipation			No load, No signal		180			180		mW

NOTE 3: For SN5511, V_{IC} = +2.5 V to −2 V; for SN7511, V_{IC} = + 1 V to −1 V.

†Unless otherwise specified, V_{IO} is applied and the regulator terminal is open.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DEFINITION OF TERMS

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in voltage between the output terminals to the change in voltage between the input terminals producing it.

Large-Signal Single-Ended Voltage Amplification (A_{VS}) The ratio of the change in single-ended output voltage to the change in single-ended input voltage.

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c differential output voltage to zero.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left|\frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the inputs grounded.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the inputs grounded.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

3

Output Offset Voltage (V_{OO}) The difference between the d-c voltages at the two output terminals when the input terminals are grounded.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

Differential Input Impedance (z_{id}) The small-signal impedance between the two input terminals.

Single-Ended Output Impedance (z_{os}) The small-signal impedance between one output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in output offset voltage referred to the input.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load; $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

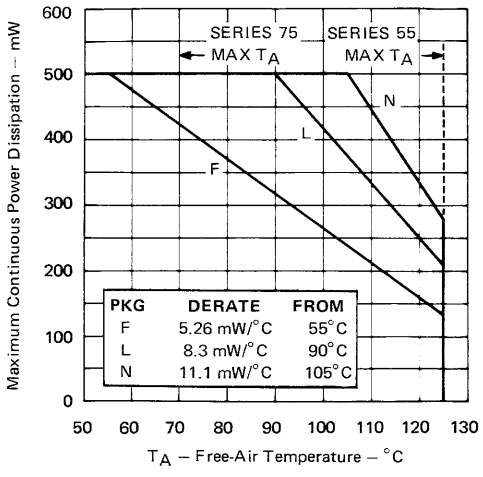


FIGURE 1

PARAMETER MEASUREMENT INFORMATION

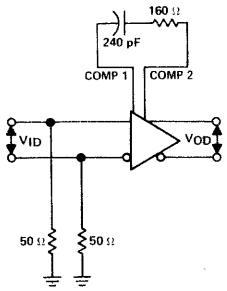


FIGURE 2 – A_{VD}

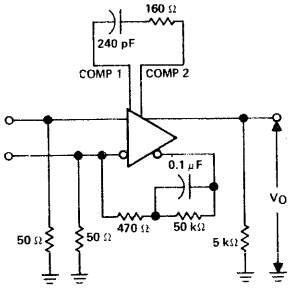


FIGURE 3 – A_{VS}, V_{OPP}

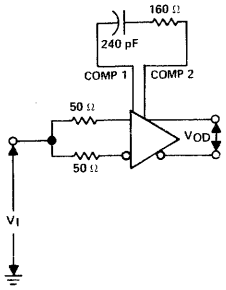


FIGURE 4 – V_I, CMRR

TYPICAL CHARACTERISTICS

3

SN5511
SINGLE-ENDED OPEN-LOOP
VOLTAGE AMPLIFICATION
vs
FREQUENCY

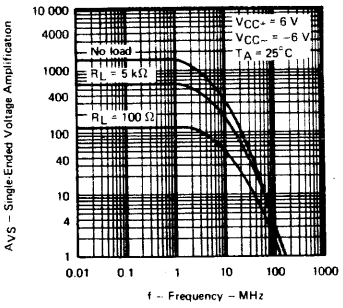


FIGURE 5

SN5511
SINGLE-ENDED OPEN-LOOP
VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

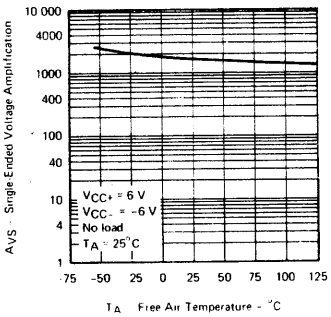


FIGURE 6

SN5511
SINGLE-ENDED OPEN-LOOP
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGES

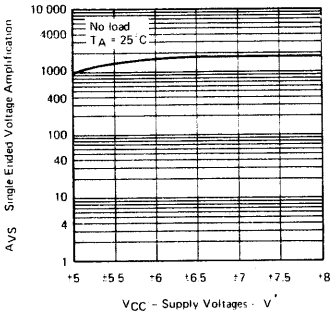


FIGURE 7

SN5511
INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

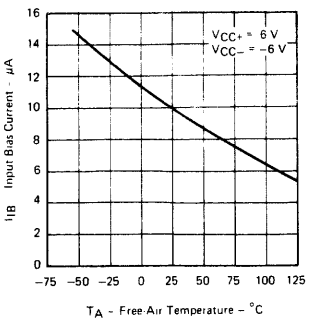


FIGURE 8

SN5511
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (OPEN-LOOP)
vs
LOAD RESISTANCE

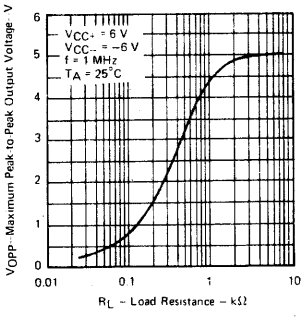


FIGURE 9

SN5511
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (OPEN-LOOP)
vs
FREQUENCY

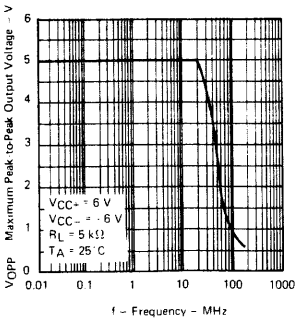


FIGURE 10

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

SN5511
SINGLE-ENDED CLOSED-LOOP
VOLTAGE AMPLIFICATION
vs
FREQUENCY

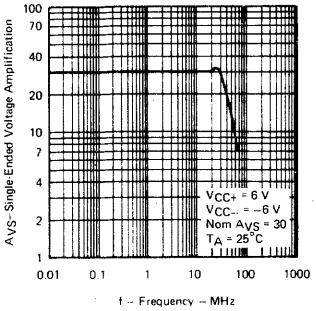
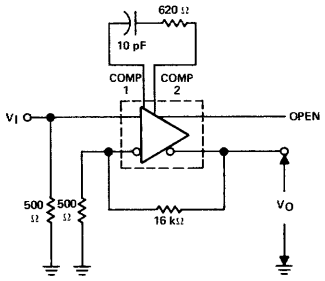


FIGURE 11

NOMINAL AMPLIFICATION OF 30



TEST CIRCUIT
FOR FIGURES 11 AND 12

SN5511
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (CLOSED-LOOP)
vs
FREQUENCY

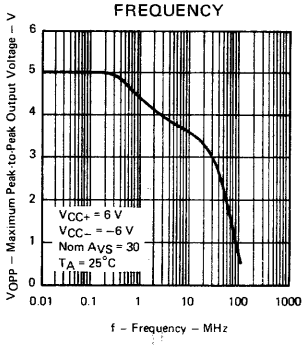


FIGURE 12

3

SN5511
SINGLE-ENDED CLOSED-LOOP
VOLTAGE AMPLIFICATION
vs
FREQUENCY

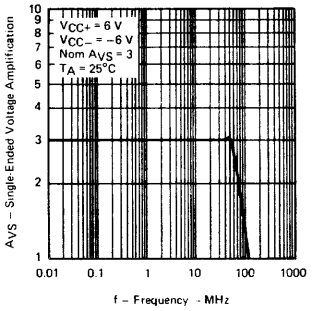
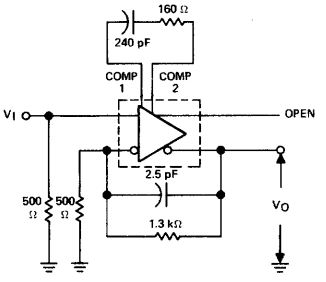


FIGURE 13

NOMINAL AMPLIFICATION OF 3



TEST CIRCUIT
FOR FIGURES 13 AND 14

SN5511
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (CLOSED-LOOP)
VS
FREQUENCY

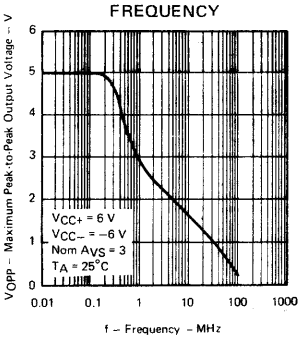


FIGURE 14

SN5511
SINGLE-ENDED CLOSED-LOOP
VOLTAGE AMPLIFICATION
vs
FREQUENCY

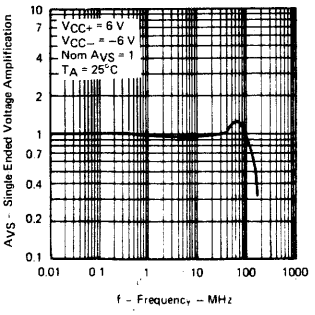
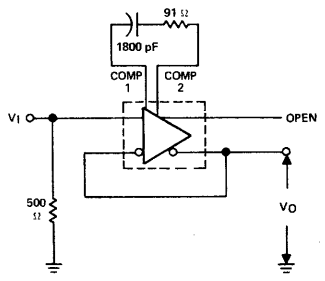


FIGURE 15

NOMINAL AMPLIFICATION OF 1



TEST CIRCUIT
FOR FIGURES 15 AND 16

SN5511
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (CLOSED-LOOP)
vs
FREQUENCY

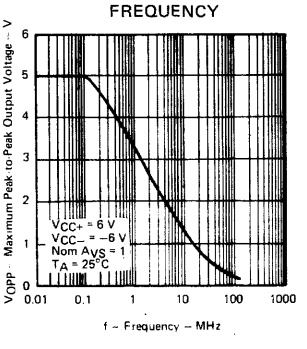


FIGURE 16

TYPICAL CHARACTERISTICS

INPUT IMPEDANCE
vs
FREE-AIR TEMPERATURE

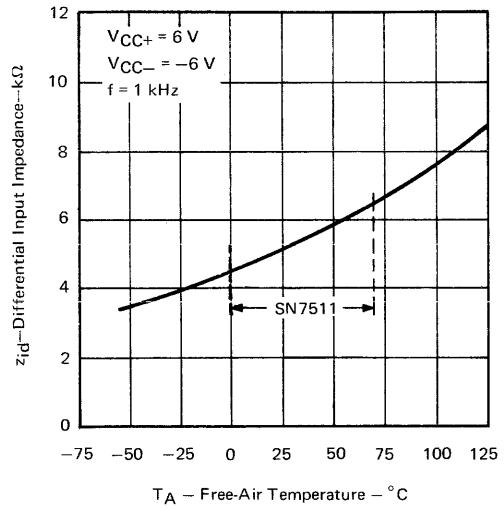


FIGURE 17

SN5511

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

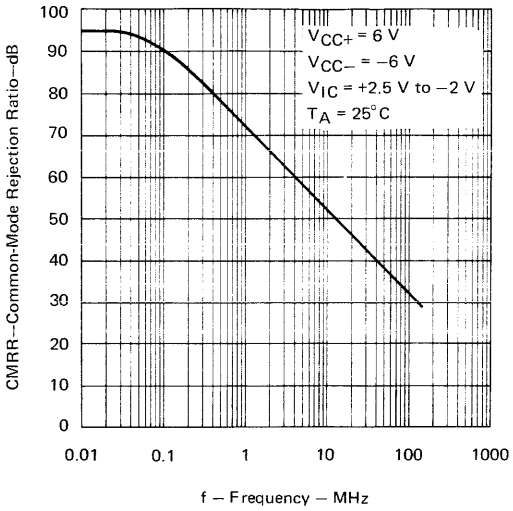


FIGURE 18

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

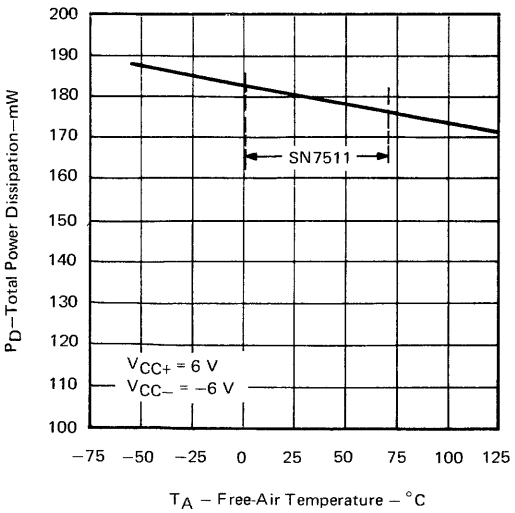


FIGURE 19

SPOT NOISE FIGURE
vs
FREQUENCY

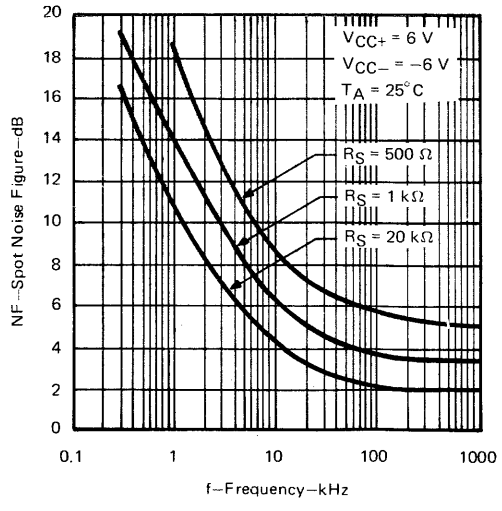


FIGURE 20

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5512, SN5514, SN7512, SN7514
DIFFERENTIAL VIDEO AMPLIFIERS

- 80-MHz Bandwidth
- No Frequency Compensation Required
- Typical Differential Voltage Amplification of 300
- SN5512 and SN7512 Have Offset-Voltage Null Capability

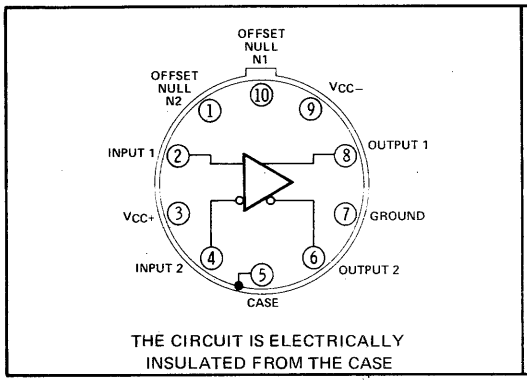
description

Each of these wide-band video amplifiers feature a flat frequency response and low phase distortion from dc to typically 80 MHz. Emitter-follower outputs enable the devices to drive capacitive loads. A low-value potentiometer may be connected between the offset null inputs of the SN5512 and SN7512, as shown in Figure 7, to null out the offset voltage.

These circuits are designed for use as sense amplifiers in high-speed thin-film or plated-wire memories, as magnetic tape-read amplifiers, or as general purpose pulse or video amplifiers.

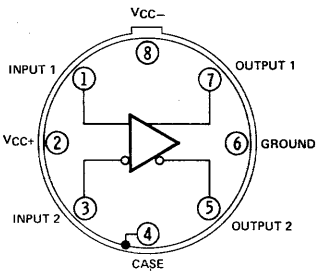
terminal assignments

SN5512, SN7512
L PLUG-IN PACKAGE
(TOP VIEW)



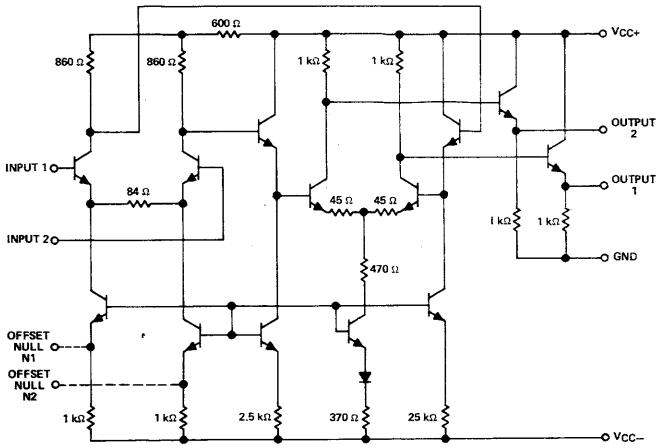
THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

SN5514, SN7514
L PLUG-IN PACKAGE
(TOP VIEW)



THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

schematic



NOTES: 1. Component values shown are nominal.
2. Offset null terminals (shown with dashed lines) are provided on the SN5512 and SN7512 only.

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5512, SN5514, SN7512, SN7514
DIFFERENTIAL VIDEO AMPLIFIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN5512 SN5514	SN7512 SN7514	UNIT
Supply voltage V_{CC+} (See Note 3)	8	8	V
Supply voltage V_{CC-} (See Note 3)	−8	−8	V
Differential input voltage	±5	±5	V
Common-mode input voltage	±6	±6	V
Voltage between either offset null terminal (N1/N2) and V_{CC-} (SN5512 and SN7512)	±0.5	±0.5	V
Output current	10	10	mA
Continuous total power dissipation at (or below) 65°C free-air temperature (See Note 4)	500	500	mW
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1/16" from case for 60 seconds	300	300	°C

NOTES: 3. All voltage values, except differential input voltages, are with respect to the network ground terminal.
4. For operation above 65°C free-air temperature, refer to Dissipation Derating Curve, Figure 6.

3

electrical characteristics, T_A = 25°C, V_{CC+} = 6 V, V_{CC-} = −6 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN5512 SN5514			SN7512 SN7514			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification	1	V_{OD} = 1 V	250	300	350	200	300	400	
BW	Bandwidth	2	R_S = 50 Ω		80			80		MHz
I_{IO}	Input offset current				1	3		1	5	μA
I_{IB}	Input bias current				50	80		50	80	μA
V_I	Input voltage range	1		±1			±1			V
V_{OC}	Common-mode output voltage	1		2.4	2.7	3.4	2.4	2.7	3.4	V
V_{OO}	Output offset voltage	1			0.5	1.3		0.5	1.3	V
V_{OPP}	Maximum peak-to-peak output voltage swing	3		3	5		3	5		V
r_i	Input resistance	3	$V_{OD} \leq$ 1 V		6			6		kΩ
r_o	Output resistance				35			35		Ω
C_i	Input capacitance	3	$V_{OD} \leq$ 1 V		7			7		pF
CMRR	Common-mode rejection ratio	4	V_{IC} = ± 1 V, f ≤ 100 kHz		84			84		dB
$\Delta V_{CC}/\Delta V_{IO}$	Supply voltage rejection ratio	1	ΔV_{CC+} = from 6 V to 5.5 V ΔV_{CC-} = from −6 V to −5.5 V	50	80		50	80		dB
V_n	Broadband equivalent input noise voltage	5	See Note 5		3			3		μV
t_{pd}	Propagation delay time	2	R_S = 50 Ω, Output voltage step = 0 to 1 V		6			6		ns
t_r	Rise time	2	R_S = 50 Ω, Output voltage step = 0 to 1 V		5			5		ns
$I_{sink(max)}$	Maximum output sink current			2.5	3.2		2.5	3.2		mA
I_{CC+}	Supply current from V_{CC+}		No load, No signal		19	25		19	25	mA
I_{CC-}	Supply current from V_{CC-}		No load, No signal		−13	−20		−13	−20	mA

NOTE 5: This parameter is measured in a system with response down 3 dB at 10 Hz and 500 kHz with a 6-dB/octave rolloff.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DEFINITION OF TERMS

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in voltage between the output terminals to the change in voltage between the input terminals producing it.

Bandwidth (BW) The range of frequencies within which the differential gain of the amplifier is not more than 3 dB below its low-frequency value.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the inputs grounded.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the inputs grounded.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Common-Mode Output Voltage (V_{OC}) The average of the d-c voltages at the two output terminals.

Output Offset Voltage (V_{OO}) The difference between the d-c voltages at the two output terminals when the input terminals are grounded.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between either output terminal and ground.

Input Capacitance (C_i) The capacitance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in output offset voltage referred to the input.

Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) The ratio of the change in power supply voltages to the change in output offset voltage referred to the input. For these devices, both supply voltages are varied symmetrically.

Propagation Delay Time (t_{pd}) The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Maximum Output Sink Current ($I_{sink(max)}$) The maximum available current into either output terminal when that output is at its most negative potential.

PARAMETER MEASUREMENT INFORMATION

test circuits

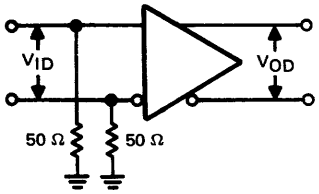


FIGURE 1

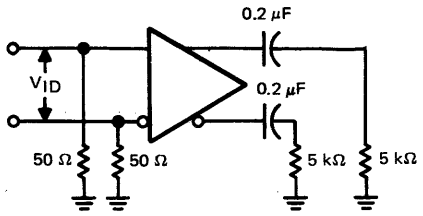


FIGURE 2

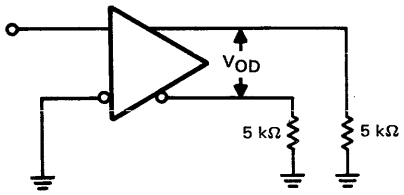


FIGURE 3

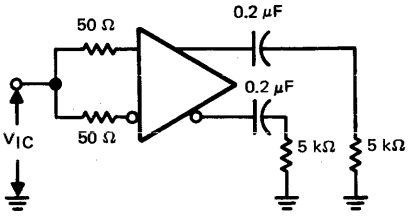


FIGURE 4

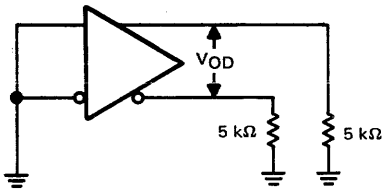


FIGURE 5

THERMAL INFORMATION

DISSIPATION DERATING CURVE

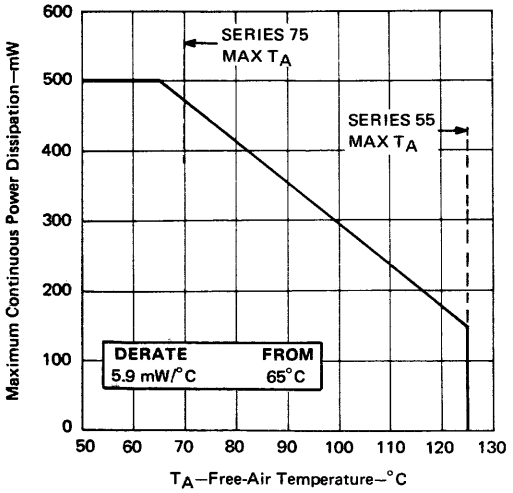


FIGURE 6

TYPICAL APPLICATION DATA

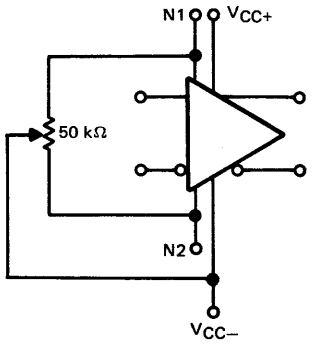


FIGURE 7—SN5512/SN7512
INPUT-OFFSET-VOLTAGE NULL CIRCUIT

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

line drivers

TYPE	SN55109, SN75109	SN55110, SN75110	SN75113*	SN75114*	SN75150†	SN75450A
• Operating Frequency	> 10 MHz	> 10 MHz	> 10 MHz	> 10 MHz	10 kHz at 2500-pF Load	< 1 MHz
• Type of Lines	Balanced or Single-Ended	Balanced or Single-Ended	Balanced or Single-Ended	Balanced or Single-Ended	Single-Ended	Balanced or Single-Ended
• Length of Line	Up to 5,000'	Up to 10,000'	Up to 1,000'	Up to 1,000'	Up to 500'	Up to 500'
• Input	TTL	TTL	TTL	TTL	TTL	TTL
• Output	Current Mode	Current Mode	Voltage Mode	Voltage Mode	Voltage Mode	Current Mode
• Party Line Operation	Yes	Yes	Yes	Yes	No	Yes
• Strobe Control	Yes	Yes	Yes	No	No	
• Power Supply	+5 V and −5 V	+5 V and −5 V	+5 V	+5 V	+12 V and −12 V	+5 V
Packages	J, N	J, N	J, N	J, N	J, N, P	N
Application Notes	CA130: Line Drivers and Receivers CA146: Data Transmission					CA150-Peripheral Interface Circuits

3

line receivers

TYPE	SN55107A, SN75107A	SN55108A, SN75108A	SN55115,* SN75115*	SN75154*
• Input Sensitivity, Max	25 mV	25 mV	0.5 V	
• Switching Time, Max	25 ns	25 ns	50 ns	50 ns
• Strobe Capability	Yes	Yes	Yes	No
• Output	TTL, Active Pull-Up	TTL, Open-Collector	TTL, Open-Collector With Active Pull-Up Option	TTL, Active Pull-Up
• Fan-Out to Series 54	10	10	10	10
• Power Supply	+5 V and −5 V	+5 V and −5 V	+5 V	+5 V or +12 V
Packages	J, N	J, N	J, N	J, N
Application Notes	CA130: Line Drivers and Receivers CA146: Data Transmission			

*To be announced soon

†Satisfies requirements of EIA standard RS-232-C

TYPE SN75100L
DUAL DIFFERENTIAL LINE RECEIVER

SERIES 75 LINE RECEIVER

featuring

- **High Input Impedance**
- **Fast Switching Speed**
- **Good Small-Signal Sensitivity**
- **TTL and DTL Compatible Outputs**
- **Wire-OR Output Capability**

description

The SN75100L is a monolithic, dual line receiver which consists of two independent discriminator/buffer circuits in a single package. Each line receiver is composed of a voltage-sensitive, differential-input comparator which drives an open-collector, saturated-logic buffer. This device is designed to operate throughout the temperature range of 0°C to 70°C with a maximum switching time of 40 nanoseconds. The buffer output is at a logical 1 voltage level when the voltage at the signal input is at least 100 millivolts more positive than the reference voltage applied at V_{ref}. The output is at a logical 0 level when the voltage at the signal input is at least 100 millivolts more negative than the reference voltage applied at V_{ref}.

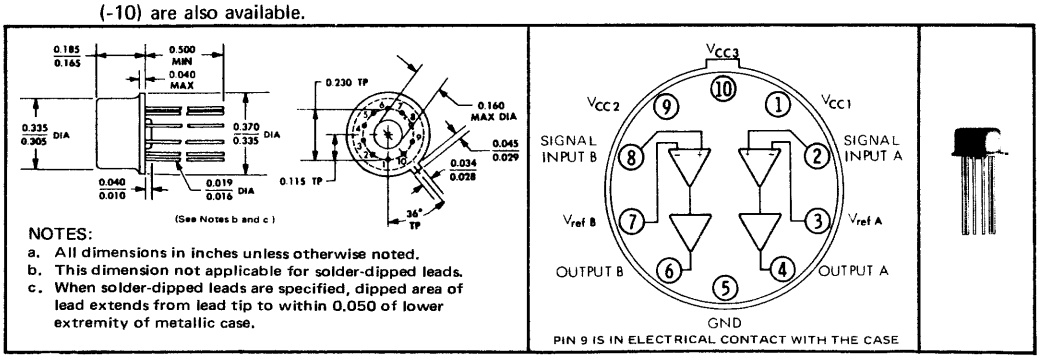
The line receiver has a common-mode input voltage range of -1.5 volts to 1.5 volts which means that both inputs can withstand common voltages of as much as 1.5 volts above or below ground. The buffer output will produce the correct logic-level output for a minimum difference in voltage of 100 millivolts between the differential inputs.

For normal single-ended operation, the data transmission line is connected to the signal input with a fixed d-c voltage between -1.5 volts and 1.5 volts applied at V_{ref}. For maximum noise immunity, the d-c voltage level at V_{ref} should be set midway between the logical 0 and logical 1 voltage levels of the input signal. Alternatively, the functions of the signal and reference-voltage inputs may be interchanged.

When the line receiver is used in a differential mode with balanced two-wire lines, one wire is connected to the signal input and the other wire is connected to V_{ref}. Since a maximum difference of 100 millivolts between the signal input and V_{ref} will assure a given logical level at the buffer output, a trade-off between input sensitivity and common-mode rejection can be made by using external voltage dividers at the inputs.

mechanical data

The SN75100L package outline is the same as JEDEC TO-100 except for diameter of standoff. Gold-plated leads (-00) require no additional cleaning or processing for use in soldered assembly. Solder-dipped leads (-10) are also available.



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (See Note 1): V_{CC1} . . . . . 10 V
V_{CC2} . . . . . -10 V
V_{CC3} . . . . . 6 V
Differential input voltage, V_{inD} (See Note 2) . . . . . ±5 V
Input voltage, V_{in} or V_{ref} (See Note 1) . . . . . ±5.5 V
Maximum current into the output, I_{sink} . . . . . 60 mA
Continuous power dissipation at (or below) 25°C free-air temperature (See Note 3) . . . . . 680 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . -65°C to 150°C

recommended operating conditions

Supply voltages (See Note 1): V_{CC1} . . . . . 8 V ± 10%
V_{CC2} . . . . . -8 V ± 10%
V_{CC3} . . . . . 4 V ± 10%
Reference voltage, V_{ref} . . . . . -1.5 V to 1.5 V

3

NOTES: 1. These voltage values are with respect to network ground terminal.
2. These voltage values are with respect to the other differential-input terminal.
3. Derate linearly to 435 mW at 70°C free-air temperature at the rate of 5.4 mW/°C.

electrical characteristics (unless otherwise noted, V_{CC1} = 8 V, V_{CC2} = -8 V, V_{CC3} = 4 V, T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{inD(0)}$	Logical 0 input voltage at the signal input, with respect to V_{ref}, required to ensure logical 0 level at the output	1	V_{ref} = -1.5 V to 1.5 V	-100			mV
$V_{inD(1)}$	Logical 1 input voltage at the signal input, with respect to V_{ref}, required to ensure logical 1 level at the output	1	V_{ref} = -1.5 V to 1.5 V	100			mV
$V_{out(0)}$	Logical 0 output voltage	2	V_{in} = -2 V to 1.4 V, V_{ref} = 1.5 V, I_{sink} = 40 mA		0.25	0.5	V
			V_{in} = -2 V to -1.6 V, V_{ref} = -1.5 V, I_{sink} = 40 mA		0.25	0.5	V
$I_{out(1)}$	Output reverse current	2	V_{in} = -1.4 V to 3.5 V, V_{ref} = -1.5 V, V_{out} = 5.5 V			250	μA
I_{in}	Input current into the signal input	3	V_{ref} = -1.5 V, See Note 4		20	50	μA
$I_{in(ref)}$	Input current into V_{ref}	3	V_{ref} = 1.5 V, See Note 4		20	50	μA
I_{CC1}	V_{CC1} supply current	4	V_{CC1} = 8.8 V		15	22	mA
I_{CC2}	V_{CC2} supply current	4	V_{CC2} = -8.8 V		-13	-17	mA
I_{CC3}	V_{CC3} supply current	4	V_{CC3} = 4.4 V		10	20	mA

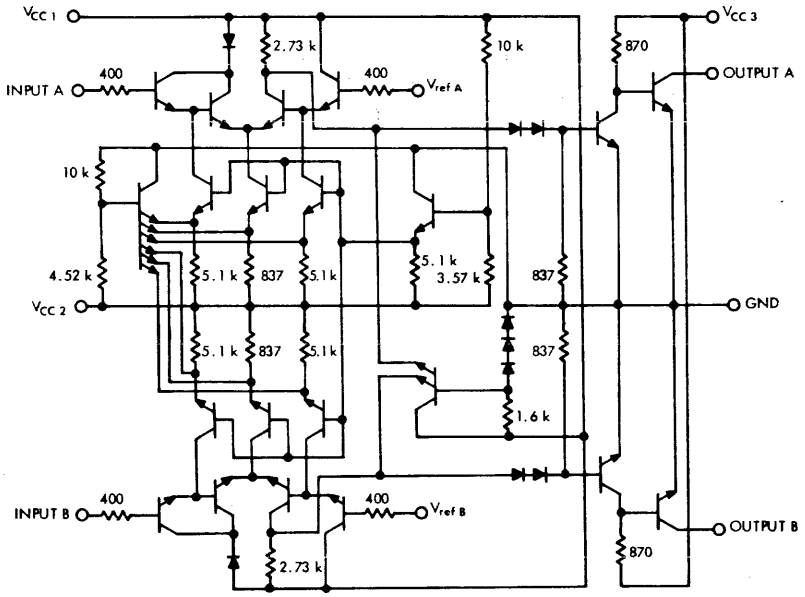
†All typical values are at 25°C.

NOTE: 4. The maximum value specified is also applicable under any combination of the following conditions:
a. V_{CC1} is open, grounded, or at 8 V ± 10%.
b. V_{CC2} is open, grounded, or at -8 V ± 10%.
c. V_{CC3} is open, grounded, or at 4 V.
d. V_{in} = 2 V to 4.4 V.

switching characteristics, V_{CC1} = 8 V, V_{CC2} = -8 V, V_{CC3} = 4 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd(1)}$	Propagation delay time to logical 1 level	5	R_L = 100 Ω, C_L = 20 pF, V_L = 4 V, f = 1 MHz		20	40	ns
$t_{pd(0)}$	Propagation delay time to logical 0 level	5			20	40	ns

schematic diagram



NOTE: All resistor values are in ohms.

PARAMETER MEASUREMENT INFORMATION †

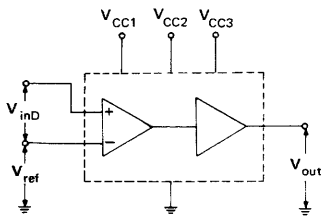


FIGURE 1– $V_{inD(0)}$ and $V_{inD(1)}$

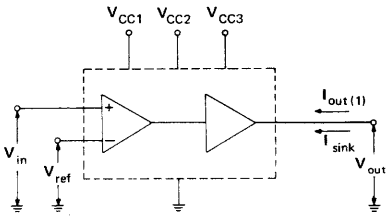


FIGURE 2– $V_{out(0)}$ and $I_{out(1)}$

†Arrows indicate direction of current flow.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION †

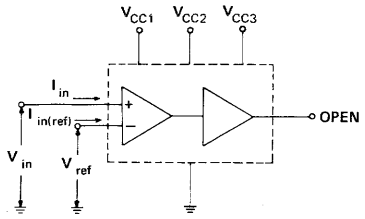


FIGURE 3—I_{in} and $I_{in(ref)}$

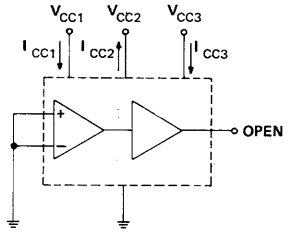
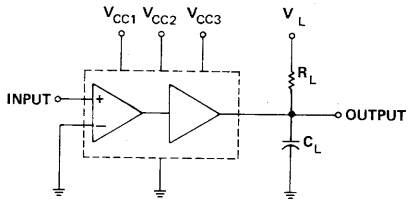
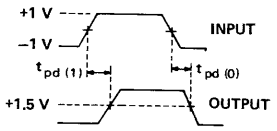


FIGURE 4—I_{CC1}, I_{CC2}, and I_{CC3}



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 5—$t_{pd(1)}$ and $t_{pd(0)}$

†Arrows indicate direction of current flow.

3

TYPICAL APPLICATION DATA

The SN75100L is ideally suited for use as a differential or single-ended line receiver. Maximum flexibility is ensured by the high-impedance inputs and open-collector outputs. The outputs are compatible for driving TTL or DTL digital circuits and may be combined to perform the wire-OR function.

When used in a single-ended "party line" data-transmission system, transmission lines may be either a twisted pair or coaxial cable. See Figure A.

By terminating the transmission line at each end, a two-way signal path may be utilized. The SN75100L provides very little loading to the transmission line due to its high input impedance. Therefore, transmitter/receiver pairs may be tied into the line anywhere along its length without disturbing the impedance level of the line.

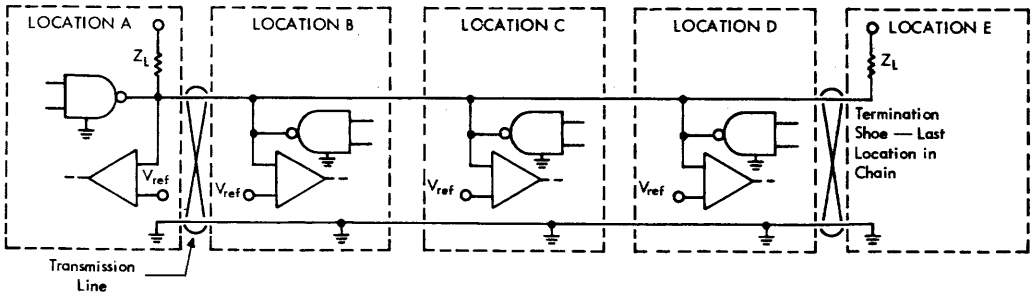


FIGURE A

CIRCUIT TYPES SN55107A, SN55108A, SN55109, SN55110, SN75107A, SN75108A, SN75109, SN75110 DUAL LINE RECEIVERS AND DRIVERS

SERIES 55/75107A LINE CIRCUITS
featuring

• High Speed • Standard Supply Voltages • Dual Channels

additional features of line receivers

- high common-mode rejection ratio
- high input impedance
- high input sensitivity
- differential input common-mode voltage range of ± 3 V
- differential input common-mode voltage range of more than ±15 V using external attenuator
- strobe inputs for receiver selection
- gate inputs for logic versatility
- TTL or DTL drive capability
- high d-c noise margins

−55°C to 125°C J Package	0°C to 70°C J or N Package	CIRCUIT FUNCTION	OUTPUT FUNCTION
SN55107A	SN75107A	Dual Line Receiver	Active Pull-Up
SN55108A	SN55108A	Dual Line Receiver	Open Collector
SN55109	SN75109	Dual Line Driver	6-mA Current Switch
SN55110	SN75110	Dual Line Driver	12-mA Current Switch

additional features of line drivers

- TTL input compatibility
- current-mode output (6 mA or 12 mA typical)
- high output impedance
- high common-mode output voltage range (-3 V to 10 V)
- inhibitor available for driver selection

description

The Series 55/75107 circuits are TTL/DTL compatible high-speed line receivers and drivers. Each is a monolithic dual circuit featuring two independent channels.

The SN55107A, SN55108A, SN75107A, and SN75108A line receivers are designed for general use as well as such specific applications as data comparators and balanced, unbalanced, and party-line transmission systems. These devices are unilaterally interchangeable with and replace SN55107, SN55108, SN75107, and SN75108, respectively, but offer diode-clamped inputs to simplify circuit design.

The SN55109, SN55110, SN75109, and SN75110 line drivers are designed to be used in many categories of applications in balanced, unbalanced, and party-line systems and as level converters.

The SN55107A, SN55108A, SN55109, and SN55110 are characterized for operation over the full military temperature range of −55°C to 125°C, and are available in the ceramic dual-in-line (J) package. The SN75107A, SN75108A, SN75109, and SN75110 are characterized for operation from 0°C to 70°C and are available either in the ceramic dual-in-line (J) package or in the plastic dual-in-line (N) package.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN55107A, SN55108A, SN55109, SN55110, SN75107A, SN75108A, SN75109, SN75110 DUAL LINE RECEIVERS AND DRIVERS

design characteristics

Series 55/75107A Line Circuits are TTL-compatible dual circuits intended for use in high-speed data-transmission systems. The drivers are designed to drive balanced, terminated transmission lines, such as twisted-pair, at normal line impedances without high power dissipation. The receivers are designed to detect low-level differential signals in the presence of common-mode noise and variations of temperature and supplies. Either driver may be used with either receiver. Specifications reflect worst-case conditions of temperature, supply voltages, and input voltages.

line receivers - SN55/75107A, SN55/75108A

The SN55/75107A and SN55/75108A are dual line receivers featuring independent channels with common voltage supply and ground terminals. The SN55/75107A circuit features a TTL-compatible active pull-up (totem-pole) output. The SN55/75108A circuit is also TTL-compatible, but features an open-collector output configuration that permits the dot-OR logic connection with similar outputs (such as the SN54/74101 TTL gate or other SN55/75108A line receivers). This permits a level of logic to be implemented without extra delay. All other features of the line receivers are identical.

The SN55/75107A and SN55/75108A line circuits are designed to detect input signals of 25 millivolts (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels.

The SN55/75107A and SN55/75108A feature high input impedance and low input currents which induce very little loading on the transmission line. This makes these devices especially useful in party-line systems. The excellent input sensitivity (3 millivolts typical) is particularly important when data is to be detected at the end of a long transmission line and the amplitude of the data has been deteriorated due to cable losses.

The receiver input common-mode voltage range is ±3 volts. This is adequate for application in most systems. In systems with requirements for greater common-mode voltage range, input attenuators may be used to decrease the noise to an acceptable level at the receiver-input terminals.

The receivers feature individual strobe inputs for each channel and a strobe input common to both channels for logic versatility. The strobe inputs are tested to guarantee 400 millivolts of d-c noise margin when interfaced with Series 54/74 TTL.

line drivers - SN55/75109, SN55/75110

The SN55/75109 and SN55/75110 are dual line drivers featuring independent channels with common voltage supply and ground terminals. The significant difference between the two drivers is in the output-current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by appropriate logic levels on the inhibit inputs. The output current is nominally 6 milliamperes for the SN55/75109 and 12 milliamperes for the SN55/75110. System design determines which driver is best suited to a particular application.

The inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high—the output impedance of a transistor biased to cutoff.

The driver outputs have a common-mode voltage range of −3 volts to +10 volts, allowing common-mode voltage on the line without affecting driver performance.

The logic and inhibit inputs of the drivers are designed to satisfy TTL-system requirements. The logic inputs are tested at 2.0 volts for high-logic-level conditions and 0.8 volt for low-logic-level conditions. These tests guarantee 400 millivolts of noise margin when interfaced with Series 54/74 TTL.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

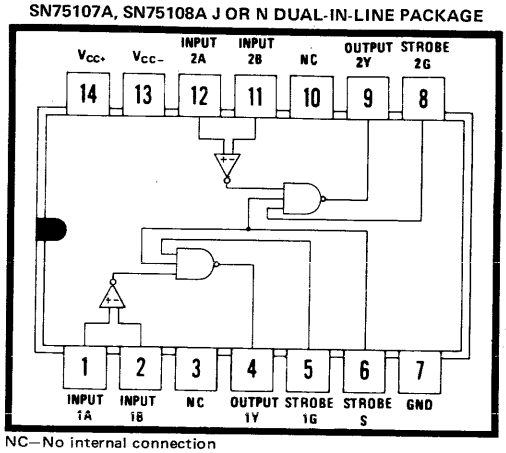
CIRCUIT TYPES SN55107A, SN55108A, SN75107A, SN75108A
DUAL LINE RECEIVERS

logic

TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} < 25$ mV	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

SN55107A, SN55108A J DUAL-IN-LINE PACKAGE
SN75107A, SN75108A J OR N DUAL-IN-LINE PACKAGE



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

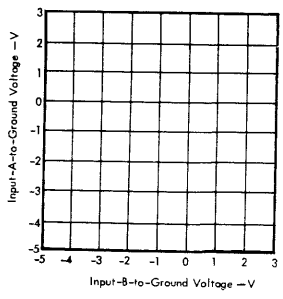
Supply voltage V_{CC+} (See Note 1) . . . . . 7 V
Supply voltage V_{CC-} (See Note 1) . . . . . −7 V
Differential input voltage (See Note 2) . . . . . ±6 V
Common-mode input voltage (See Note 1) . . . . . ±5 V
Strobe input voltage (See Note 1) . . . . . 5.5 V
Operating free-air temperature range, Series 55 . . . . . −55°C to 125°C
Series 75 . . . . . 0°C to 70°C
Storage temperature range, ceramic dual-in-line (J) package . . . . . −65°C to 150°C
plastic dual-in-line (N) package . . . . . −55°C to 150°C

recommended operating conditions (see note 3)

	SN55107A, SN55108A MIN	NOM	MAX	SN75107A, SN75108A MIN	NOM	MAX	UNIT
Supply voltage V_{CC+} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
Supply voltage V_{CC-} (See Note 1)	−4.5	−5	−5.5	−4.75	−5	−5.25	V
Output sink current			−16			−16	mA
Differential input voltage (See Notes 2 and 4)	−5†		5	−5†		5	V
Common-mode input voltage (See Notes 1 and 4)	−3†		3	−3†		3	V
Input voltage range, any differential input to ground (See Note 4)	−5†		3	−5†		3	V
Operating free-air temperature range	−55		125	0		70	°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. These voltage values are at the noninverting (+) terminal with respect to the inverting (−) terminal.
3. When using only one channel of the line receiver, the inputs of the other channel should be grounded.
4. The recommended combinations of input voltages fall within the shaded area of the figure at the right.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES FOR LINE RECEIVERS



†The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic voltage levels only.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

definition of input logic levels†

		TEST FIGURE	MIN	MAX	UNIT
V_{IDH}	High-level input voltage between differential inputs	1	0.025	5	V
V_{IDL}	Low-level input voltage between differential inputs	1	−5	−0.025	V
$V_{IH(S)}$	High-level input voltage at strobe inputs	3	2	5.5	V
$V_{IL(S)}$	Low-level input voltage at strobe inputs	3	0	0.8	V

†The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS‡		SN55107A, SN75107A			SN55108A, SN75108A			UNIT
					MIN	TYP§	MAX	MIN	TYP§	MAX	
I_{IH}	High-level input current into 1A or 2A	2	V_{CC+} = MAX, V_{ID} = 0.5 V,	V_{CC-} = MAX, V_{IC} = −3 V to 3 V		30	75		30	75	μA
I_{IL}	Low-level input current into 1A or 2A	2	V_{CC+} = MAX, V_{ID} = −2 V,	V_{CC-} = MAX, V_{IC} = −3 V to 3 V			−10			−10	μA
I_{IH}	High-level input current into 1G or 2G	4	V_{CC+} = MAX, $V_{IH(S)}$ = 2.4 V	V_{CC-} = MAX,			40			40	μA
			V_{CC+} = MAX, $V_{IH(S)}$ = MAX V_{CC+}	V_{CC-} = MAX,			1			1	mA
I_{IL}	Low-level input current into 1G or 2G	4	V_{CC+} = MAX, $V_{IL(S)}$ = 0.4 V	V_{CC-} = MAX,			−1.6			−1.6	mA
I_{IH}	High-level input current into S	4	V_{CC+} = MAX, $V_{IH(S)}$ = 2.4 V	V_{CC-} = MAX,			80			80	μA
			V_{CC+} = MAX, $V_{IH(S)}$ = MAX V_{CC+}	V_{CC-} = MAX,			2			2	mA
I_{IL}	Low-level input current into S	4	V_{CC+} = MAX, $V_{IL(S)}$ = 0.4 V	V_{CC-} = MAX,			−3.2			−3.2	mA
V_{OH}	High-level output voltage	3	V_{CC+} = MIN, I_{load} = −400 μA,	V_{CC-} = MIN, V_{IC} = −3 V to 3 V	2.4						V
V_{OL}	Low-level output voltage	3	V_{CC+} = MIN, I_{sink} = 16 mA,	V_{CC-} = MIN, V_{IC} = −3 V to 3 V			0.4			0.4	V
I_{OH}	High-level output current	3	V_{CC+} = MIN, V_{OH} = MAX V_{CC+}	V_{CC-} = MIN,						250	μA
I_{OS}	Short-circuit output current	5	V_{CC+} = MAX,	V_{CC-} = MAX	−18		−70				mA
I_{CCH+}	High-logic-level supply current from V_{CC+}	6	V_{CC+} = MAX, V_{ID} = 25 mV,	V_{CC-} = MAX, T_A = 25°C		18	30		18	30	mA
I_{CCH-}	High-logic-level supply current from V_{CC-}	6	V_{CC+} = MAX, V_{ID} = 25 mV,	V_{CC-} = MAX, T_A = 25°C		−8.4	−15		−8.4	−15	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

§ All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

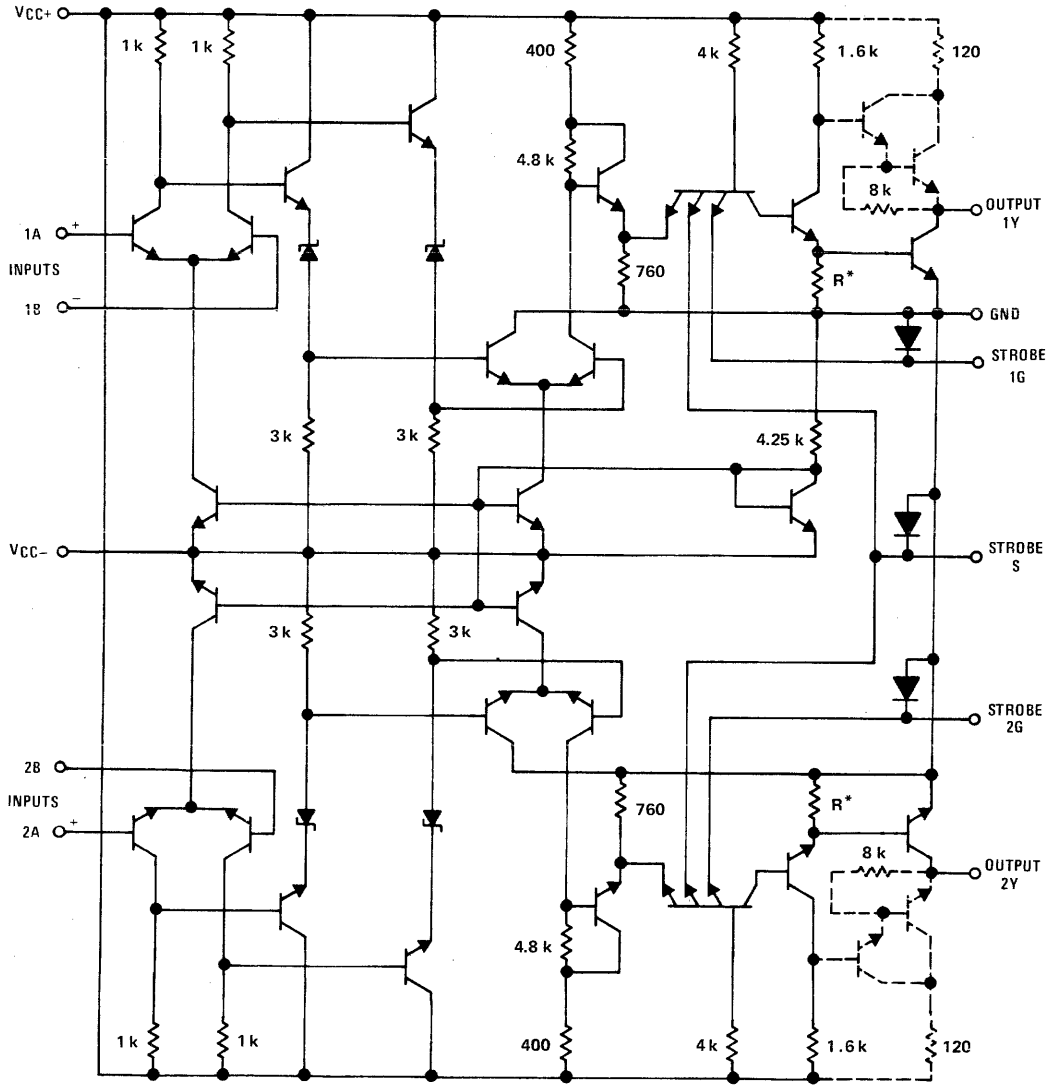
¶ Not more than one output should be shorted at a time.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		SN55107A, SN75107A			SN55108A, SN75108A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH(D)}$	Propagation delay time, low-to-high level, from differential inputs A and B to output	7	R_L = 390 Ω,	C_L = 50 pF		17	25				ns
			R_L = 390 Ω,	C_L = 15 pF					19	25	
$t_{PHL(D)}$	Propagation delay time, high-to-low level, from differential inputs A and B to output	7	R_L = 390 Ω,	C_L = 50 pF		17	25				ns
			R_L = 390 Ω,	C_L = 15 pF					19	25	
$t_{PLH(S)}$	Propagation delay time, low-to-high level, from strobe input G or S to output	7	R_L = 390 Ω,	C_L = 50 pF		10	15				ns
			R_L = 390 Ω,	C_L = 15 pF					13	20	
$t_{PHL(S)}$	Propagation delay time, high-to-low level, from strobe input G or S to output	7	R_L = 390 Ω,	C_L = 50 pF		8	15				ns
			R_L = 390 Ω,	C_L = 15 pF					13	20	

3

schematic



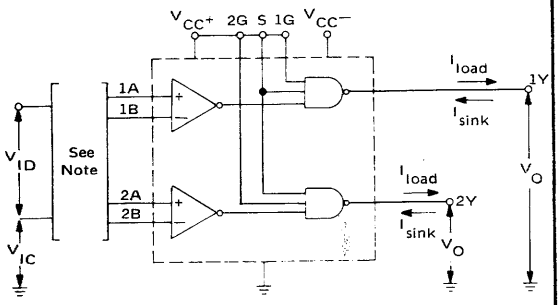
R* = 1 kΩ for SN55107A and SN75107A, 750 Ω for SN55108A and SN75108A.

NOTES: 1. Component values shown are nominal.
2. Resistance values are in ohms.
3. Components shown with dashed lines are applicable to the SN55107A and SN75107A only.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

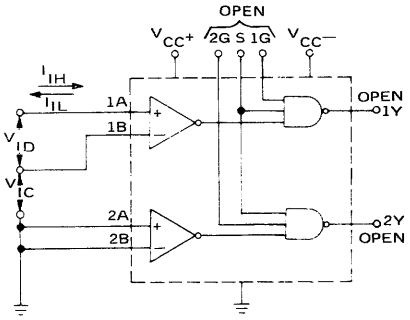
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



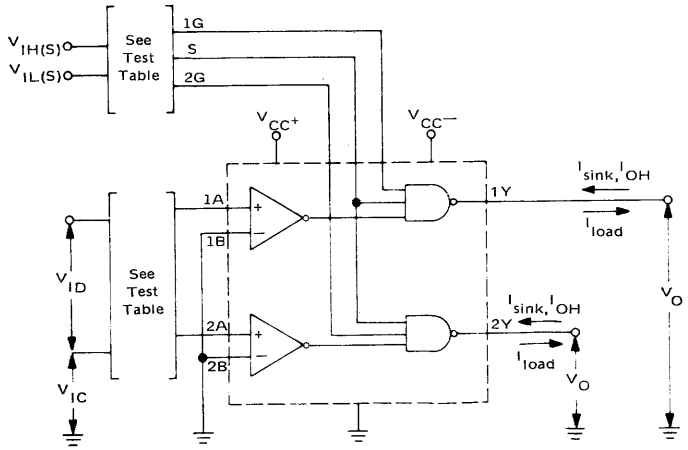
NOTE: When testing one channel, the inputs of the other channel are grounded.

FIGURE 1–V_{IDH} and V_{IDL}



NOTE: Each pair of differential inputs is tested separately. The inputs of the other pair are grounded.

FIGURE 2–I_{IH} and I_{IL}



TEST TABLE

SN55107A SN75107A	SN55108A SN75108A	V_{ID}	STROBE 1G or 2G	STROBE S
TEST		APPLY		
V_{OH}	I_{OH}	+25 mV	$V_{IH(S)}$	$V_{IH(S)}$
V_{OH}	I_{OH}	−25 mV	$V_{IL(S)}$	$V_{IH(S)}$
V_{OH}	I_{OH}	−25 mV	$V_{IH(S)}$	$V_{IL(S)}$
V_{OL}	V_{OL}	−25 mV	$V_{IH(S)}$	$V_{IH(S)}$

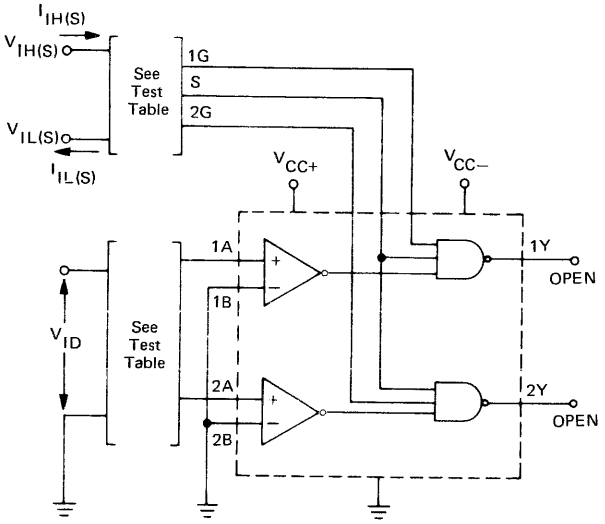
NOTES: 1. V_{IC} = −3 V to 3 V.
2. When testing one channel, the inputs of the other channel should be grounded.

FIGURE 3–$V_{IH(S)}$, $V_{IL(S)}$, V_{OH}, V_{OL}, and I_{OH}

† Arrows indicate actual direction of current flow.

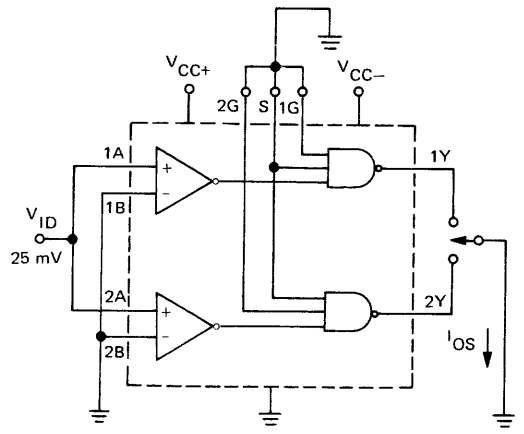
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST	INPUT 1A	INPUT 2A	STROBE 1G	STROBE S	STROBE 2G
I_{IH} at Strobe 1G	+25 mV	Gnd	$V_{IH(S)}$	Gnd	Gnd
I_{IH} at Strobe 2G	Gnd	+25 mV	Gnd	Gnd	$V_{IH(S)}$
I_{IH} at Strobe S	+25 mV	+25 mV	Gnd	$V_{IH(S)}$	Gnd
I_{IL} at Strobe 1G	−25 mV	Gnd	$V_{IL(S)}$	4.5 V	Gnd
I_{IL} at Strobe 2G	Gnd	−25 mV	Gnd	4.5 V	$V_{IL(S)}$
I_{IL} at Strobe S	−25 mV	−25 mV	4.5 V	$V_{IL(S)}$	4.5 V

FIGURE 4 – $I_{IH(G)}$, $I_{IL(G)}$, $I_{IH(S)}$, and $I_{IL(S)}$



NOTES: 1. Each channel is tested separately.
2. Not more than one output should be grounded at a time.

FIGURE 5–I_{OS}

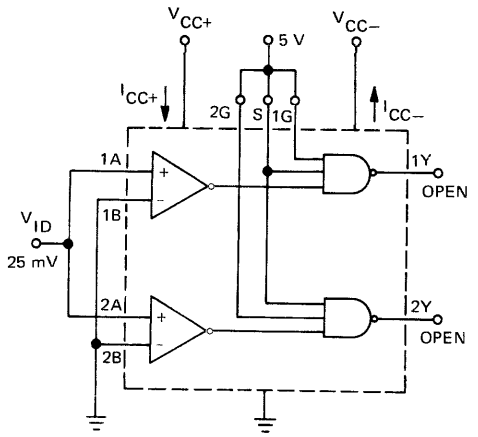
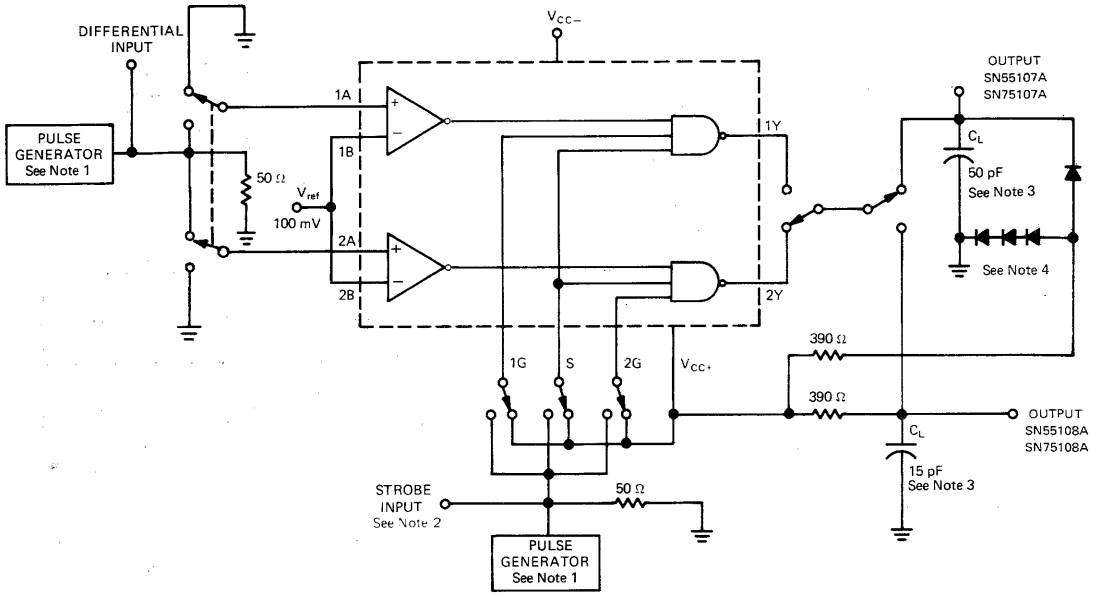


FIGURE 6–I_{CC+} and I_{CC-}

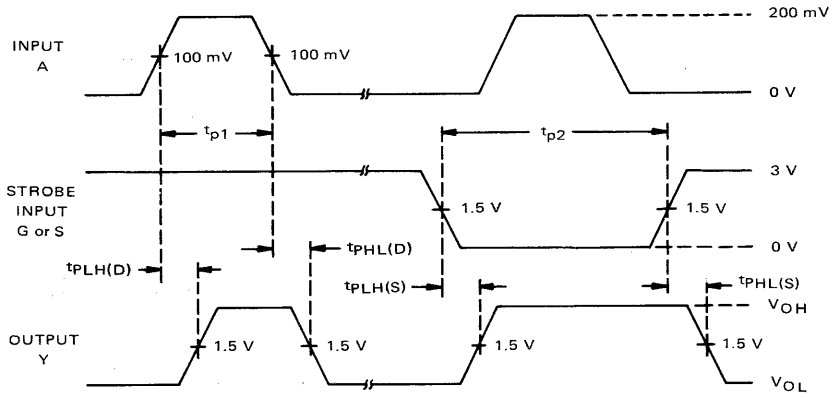
† Arrows indicate actual direction of current flow.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f = 10 \pm 5$ ns, t_{p1} = 500 ns, PRR = 1 MHz, t_{p2} = 1 ms, PRR = 500 kHz.
2. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916.

FIGURE 7—PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

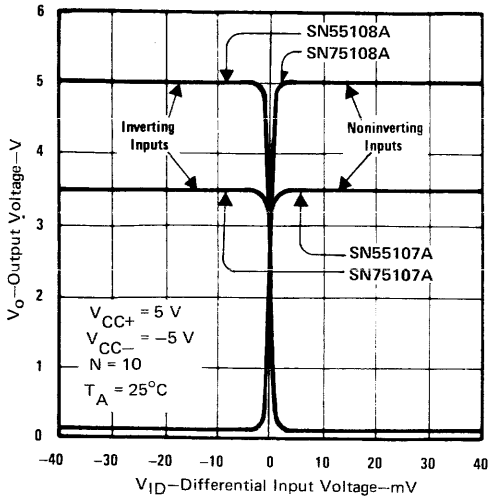


FIGURE 8

HIGH-LEVEL INPUT CURRENT
INTO 1A or 2A
vs
FREE-AIR TEMPERATURE

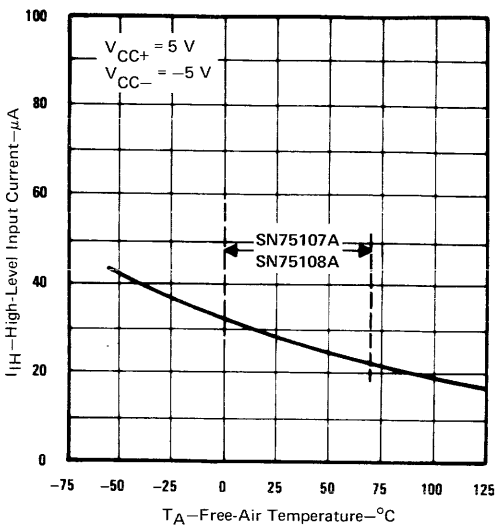


FIGURE 9

HIGH-LOGIC-LEVEL SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

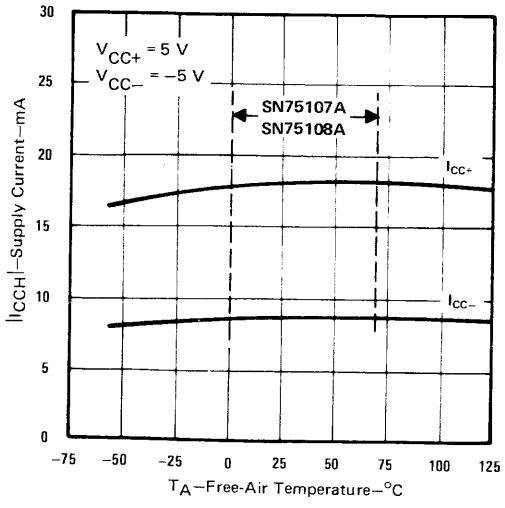


FIGURE 10

SN55107A, SN75107A
PROPAGATION DELAY TIME
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

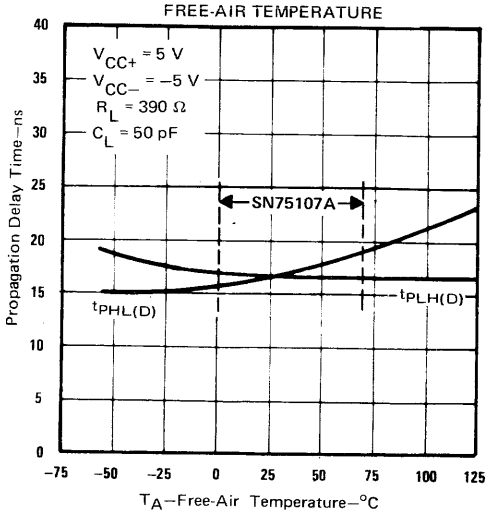


FIGURE 11

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

SN55108A, SN75108A
PROPAGATION DELAY TIME
LOW-TO-HIGH LEVEL
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

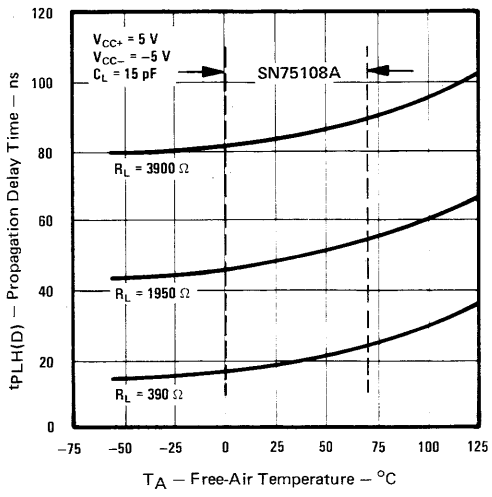


FIGURE 12

SN55108A, SN75108A
PROPAGATION DELAY TIME
HIGH-TO-LOW LEVEL
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

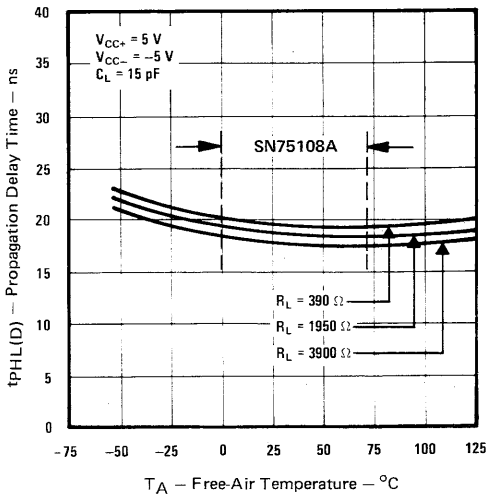


FIGURE 13

SN55107A, SN75107A
PROPAGATION DELAY TIME
(STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

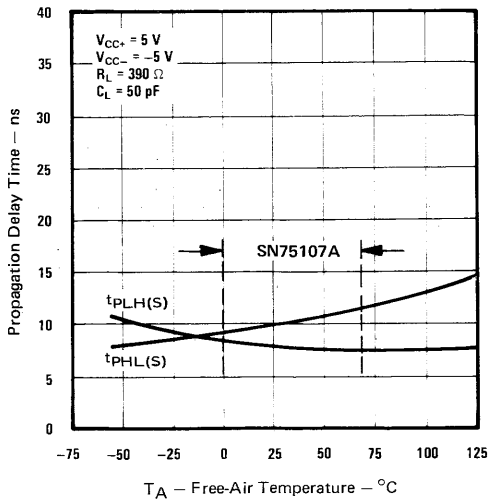


FIGURE 14

SN55108A, SN75108A
PROPAGATION DELAY TIME
(STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

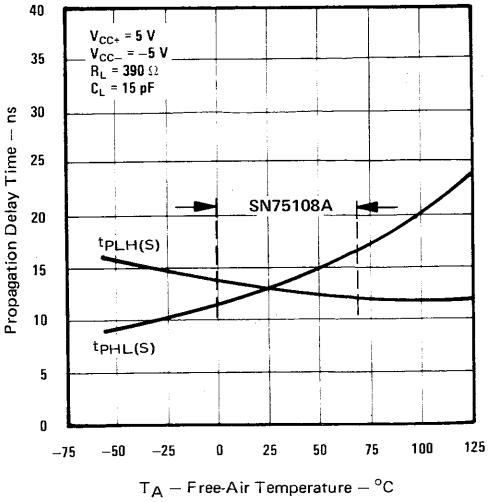
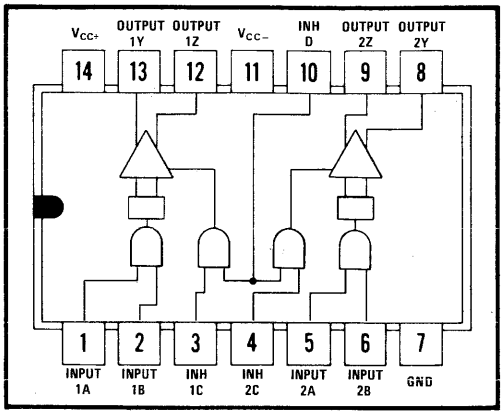


FIGURE 15

CIRCUIT TYPES SN55109, SN55110, SN75109, SN75110
DUAL LINE DRIVERS

SN55109, SN55110 J DUAL-IN-LINE PACKAGE
SN75109, SN75110 J OR N DUAL-IN-LINE PACKAGE



logic

TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the on state

High output represents the off state

3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (See Note 1) . . . . . 7 V
Supply voltage V_{CC-} (See Note 1) . . . . . −7 V
Logic and inhibitor input voltages (See Note 1) . . . . . 5.5 V
Common-mode output voltage (See Note 1) . . . . . −5 to 12 V
Operating free-air temperature range, Series 55 . . . . . −55°C to 125°C
Series 75 . . . . . 0°C to 70°C
Storage temperature range, ceramic dual-in-line (J) package . . . . . −65°C to 150°C
plastic dual-in-line (N) package . . . . . −55°C to 150°C

recommended operating conditions (see note 2)

	SN55109, SN55110			SN75109, SN75110			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC+} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
Supply voltage V_{CC-} (See Note 1)	−4.5	−5	−5.5	−4.75	−5	−5.25	V
Positive common-mode output voltage (See Note 1)	0		10	0		10	V
Negative common-mode output voltage (See Note 1)	0		−3	0		−3	V
Operating free-air temperature range	−55		125	0		70	°C

NOTES: 1. These voltage values are with respect to the network ground terminal.
2. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

definition of input logic levels†

		TEST FIGURE	MIN	MAX	UNIT
V_{IH}	High-level input voltage at any input	16, 17	2	5.5	V
V_{IL}	Low-level input voltage at any input	16, 17	0	0.8	V

†The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS‡	SN55109, SN75109 MIN	SN55109, SN75109 TYP§	SN55109, SN75109 MAX	SN55110, SN75110 MIN	SN55110, SN75110 TYP§	SN55110, SN75110 MAX	UNIT
$I_{IH(L)}$	High-level input current into 1A, 1B, 2A or 2B	16	V_{CC+} = MAX, V_{CC-} = MAX, $V_{IH(L)}$ = 2.4 V			40			40	μA
			V_{CC+} = MAX, V_{CC-} = MAX, $V_{IH(L)}$ = MAX V_{CC+}			1			1	mA
$I_{IL(L)}$	Low-level input current into 1A, 1B, 2A or 2B	16	V_{CC+} = MAX, V_{CC-} = MAX, $V_{IL(L)}$ = 0.4 V			−3			−3	mA
$I_{IH(I)}$	High-level input current into 1C or 2C	17	V_{CC+} = MAX, V_{CC-} = MAX, $V_{IH(I)}$ = 2.4 V			40			40	μA
			V_{CC+} = MAX, V_{CC-} = MAX, $V_{IH(I)}$ = MAX V_{CC+}			1			1	mA
$I_{IL(I)}$	Low-level input current into 1C or 2C	17	V_{CC+} = MAX, V_{CC-} = MAX, $V_{IL(I)}$ = 0.4 V			−3			−3	mA
$I_{IH(I)}$	High-level input current into D	17	V_{CC+} = MAX, V_{CC-} = MAX, $V_{IH(I)}$ = 2.4 V			80			80	μA
			V_{CC+} = MAX, V_{CC-} = MAX, $V_{IH(I)}$ = MAX V_{CC+}			2			2	mA
$I_{IL(I)}$	Low-level input current into D	17	V_{CC+} = MAX, V_{CC-} = MAX, $V_{IL(I)}$ = 0.4 V			−6			−6	mA
$I_{O(on)}$	On-state output current	18	V_{CC+} = MAX, V_{CC-} = MAX			−7			−15	mA
			V_{CC+} = MIN, V_{CC-} = MAX	−3.5			−6.5			mA
$I_{O(off)}$	Off-state output current	18	V_{CC+} = MIN, V_{CC-} = MIN			100			100	μA
$I_{CC+(on)}$	Supply current from V_{CC+} with driver enabled	19	$V_{IL(L)}$ = 0.4 V, $V_{IH(I)}$ = 2 V	18	30		23	35		mA
$I_{CC-(on)}$	Supply current from V_{CC-} with driver enabled	19	$V_{IL(L)}$ = 0.4 V, $V_{IH(I)}$ = 2 V	−18	−30		−34	−50		mA
$I_{CC+(off)}$	Supply current from V_{CC+} with driver inhibited	19	$V_{IL(L)}$ = 0.4 V, $V_{IL(I)}$ = 0.4 V		18			21		mA
$I_{CC-(off)}$	Supply current from V_{CC-} with driver inhibited	19	$V_{IL(L)}$ = 0.4 V, $V_{IL(I)}$ = 0.4 V		−10			−17		mA

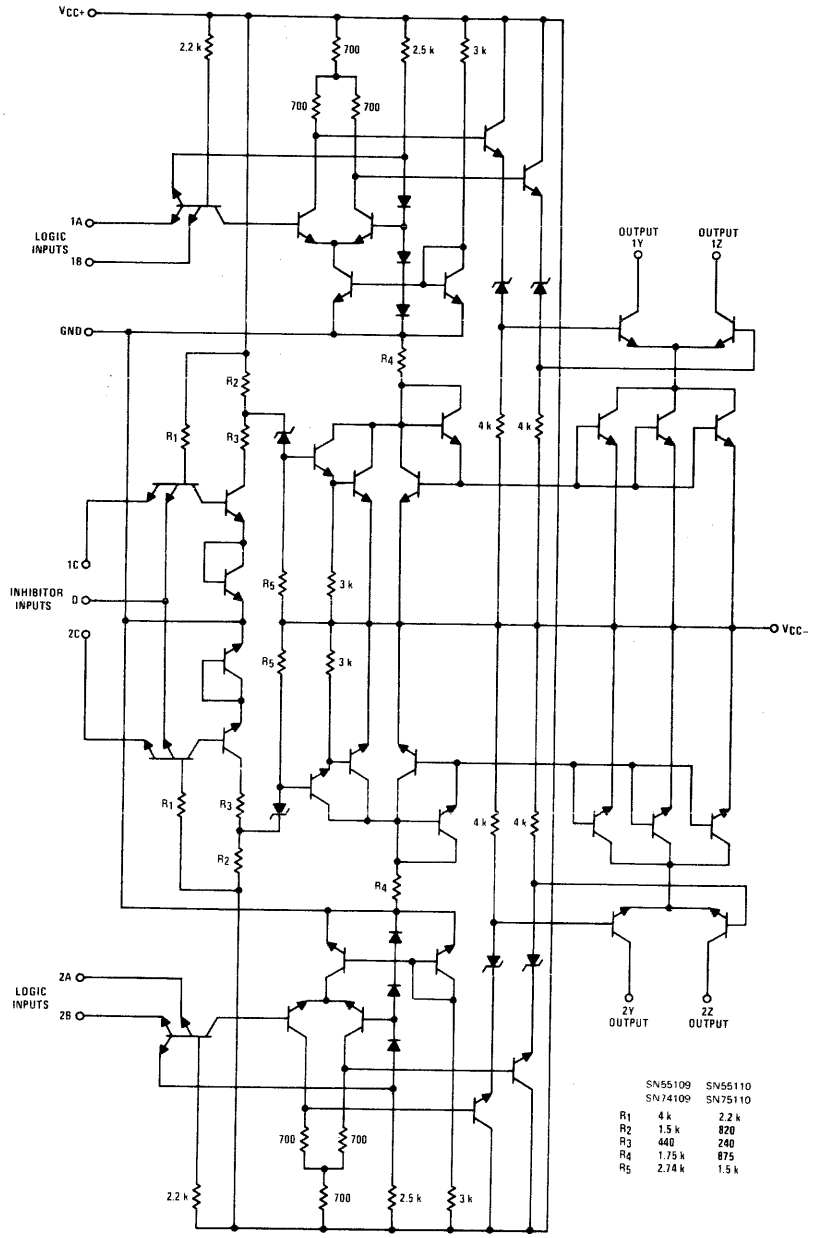
‡For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.
§All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(L)}$	Propagation delay time, low-to-high level, from logic input A or B to output Y or Z	20	R_L = 50 Ω, C_L = 40 pF		9	15	ns
$t_{PHL(L)}$	Propagation delay time, high-to-low level, from logic input A or B to output Y or Z	20	R_L = 50 Ω, C_L = 40 pF		9	15	ns
$t_{PLH(I)}$	Propagation delay time, low-to-high level, from inhibitor input C or D to output Y or Z	20	R_L = 50 Ω, C_L = 40 pF		16	25	ns
$t_{PHL(I)}$	Propagation delay time, high-to-low level, from inhibitor input C or D to output Y or Z	20	R_L = 50 Ω, C_L = 40 pF		13	25	ns

CIRCUIT TYPES SN55109, SN55110, SN75109, SN75110
DUAL LINE DRIVERS

schematic



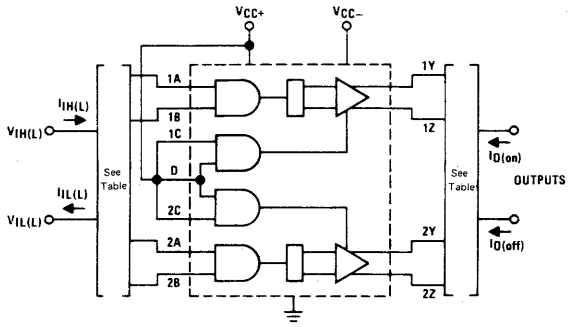
	SN55109 SN74109	SN55110 SN75110
R1	4 k	2.2 k
R2	1.5 k	820
R3	440	240
R4	1.75 k	875
R5	2.74 k	1.5 k

NOTES: 1. Component values shown are nominal.
2. Resistance values are in ohms.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits †

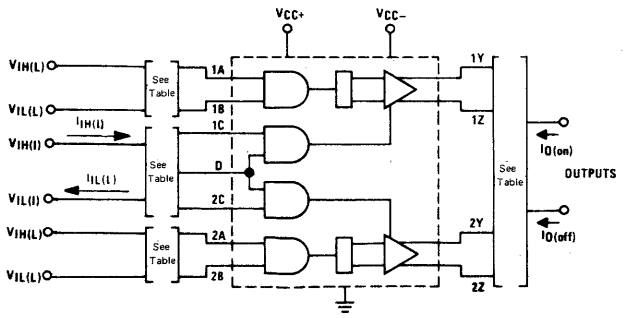


TEST TABLE

TEST AT ANY LOGIC INPUT	LOGIC INPUTS NOT UNDER TEST	ALL INHIBITOR INPUTS	OUTPUT 1Y or 2Y	OUTPUT 1Z or 2Z
$V_{IH(L)}$	Open	$V_{IH(I)}$	H (See Note 1)	L (See Note 1)
$V_{IL(L)}$	V_{CC+}	$V_{IH(I)}$	L (See Note 1)	H (See Note 1)
$I_{IH(L)}$	Gnd	$V_{IH(I)}$	Gnd	Gnd
$I_{IL(L)}$	4.5 V	$V_{IH(I)}$	Gnd	Gnd

NOTES: 1. Low output represents the on state, high output represents the off state.
2. Each input is tested separately.

FIGURE 16 – $V_{IH(L)}$, $V_{IL(L)}$, $I_{IH(L)}$, and $I_{IL(L)}$



TEST TABLE

TEST AT ANY INHIBITOR INPUT	ALL LOGIC INPUTS	INHIBITOR INPUTS NOT UNDER TEST	OUTPUT 1Y or 2Y	OUTPUT 1Z or 2Z
$V_{IH(I)}$	$V_{IH(L)}$	Open	H (See Note 1)	L (See Note 1)
	$V_{IL(L)}$	Open	L (See Note 1)	H (See Note 1)
$V_{IL(I)}$	$V_{IH(L)}$	V_{CC+}	H (See Note 1)	H (See Note 1)
	$V_{IL(L)}$	V_{CC+}	H (See Note 1)	H (See Note 1)
$I_{IH(I)}$	Gnd	Gnd	Gnd	Gnd
$I_{IL(I)}$	Gnd	4.5 V	Gnd	Gnd

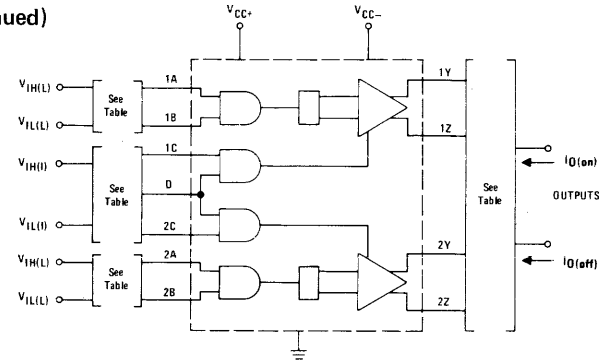
NOTES: 1. Low output represents the on state, high output represents the off state.
2. Each input is tested separately.

FIGURE 17 – $V_{IH(I)}$, $V_{IL(I)}$, $I_{IH(I)}$, $I_{IL(I)}$

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

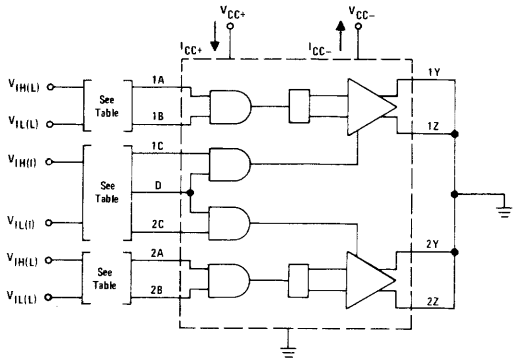
d-c test circuits† (continued)



TEST TABLE

TEST		LOGIC INPUTS		INHIBITOR INPUTS	
		1A or 2A	1B or 2B	1C or 2C	D
$I_{O(on)}$	at output 1Y or 2Y	$V_{IL(L)}$	$V_{IL(L)}$	$V_{IH(I)}$	$V_{IH(I)}$
		$V_{IL(L)}$	$V_{IH(L)}$		
		$V_{IH(L)}$	$V_{IL(L)}$		
$I_{O(on)}$	at output 1Z or 2Z	$V_{IH(L)}$	$V_{IH(L)}$	$V_{IH(I)}$	$V_{IH(I)}$
$I_{O(off)}$	at output 1Y or 2Y	$V_{IH(L)}$	$V_{IH(L)}$	$V_{IH(I)}$	$V_{IH(I)}$
$I_{O(off)}$	at output 1Z or 2Z	$V_{IL(L)}$	$V_{IL(L)}$	$V_{IH(I)}$	$V_{IH(I)}$
		$V_{IL(L)}$	$V_{IH(L)}$		
		$V_{IH(L)}$	$V_{IL(L)}$		
$I_{O(off)}$	at output 1Y, 2Y, 1Z, or 2Z	Either state	Either state	$V_{IL(I)}$	$V_{IL(I)}$
				$V_{IL(I)}$	$V_{IH(I)}$
				$V_{IH(I)}$	$V_{IL(I)}$

FIGURE 18 $-I_{O(on)}$ and $I_{O(off)}$



TEST TABLE

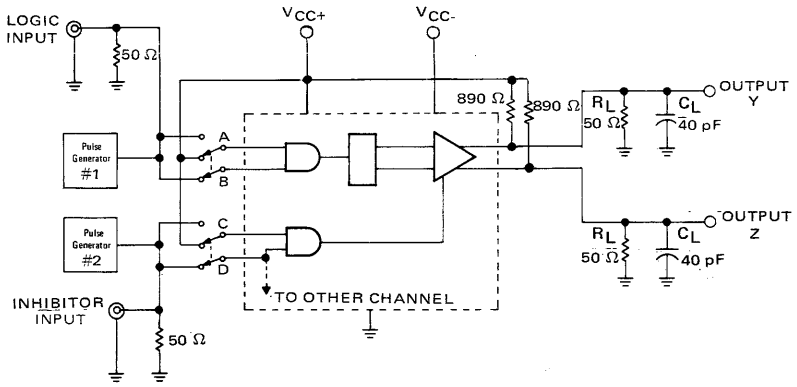
TEST		ALL LOGIC INPUTS	ALL INHIBITOR INPUTS
$I_{CC+(on)}$	Driver enabled	$V_{IL(L)}$	$V_{IH(I)}$
$I_{CC-(on)}$	Driver enabled	$V_{IL(L)}$	$V_{IH(I)}$
$I_{CC+(off)}$	Driver inhibited	$V_{IL(L)}$	$V_{IL(I)}$
$I_{CC-(off)}$	Driver inhibited	$V_{IL(L)}$	$V_{IL(I)}$

FIGURE 19 $-I_{CC+}$ and I_{CC-}

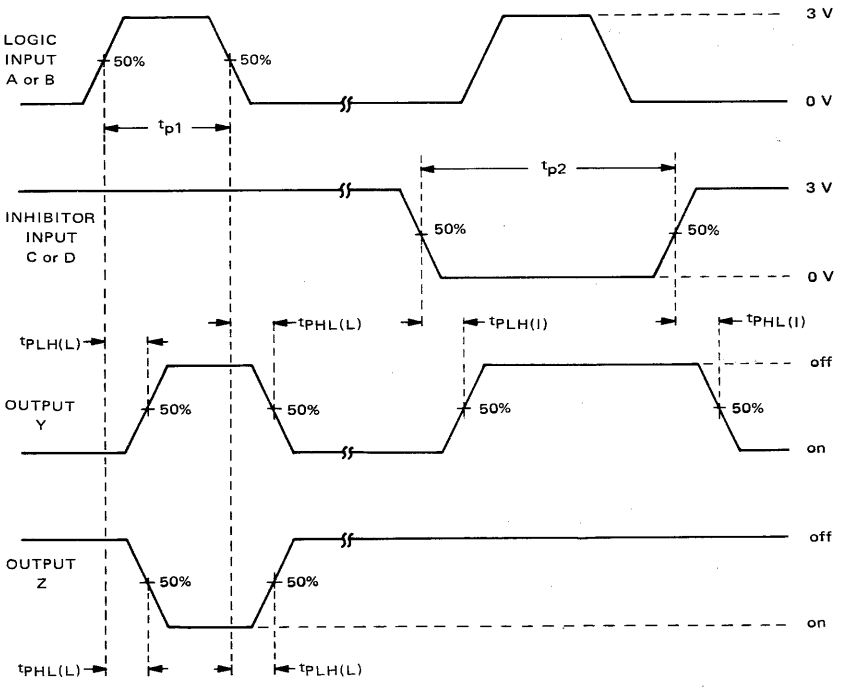
† Arrows indicate actual direction of current flow.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f = 10 \pm 5$ ns, t_{p1} = 500 ns, PRR = 1 MHz, t_{p2} = 1 ms, PRR = 500 kHz.
2. C_L includes probe and jig capacitance.
3. For simplicity, only one channel and the inhibitor connections are shown.

FIGURE 20–PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

SN55109, SN75109
OUTPUT CURRENT
vs
LOGIC INPUT VOLTAGE

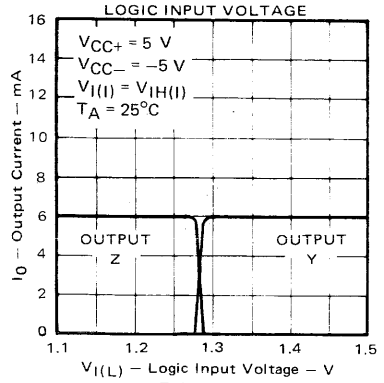


FIGURE 21

SN55110, SN75110
OUTPUT CURRENT
vs
LOGIC INPUT VOLTAGE

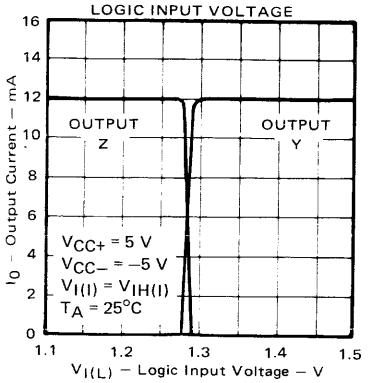


FIGURE 22

SN55109, SN75109
SUPPLY CURRENT WITH DRIVER ENABLED
vs
FREE-AIR TEMPERATURE

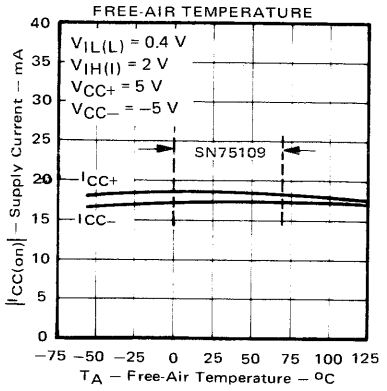


FIGURE 23

SN55110, SN75110
SUPPLY CURRENT WITH DRIVER ENABLED
vs
FREE-AIR TEMPERATURE

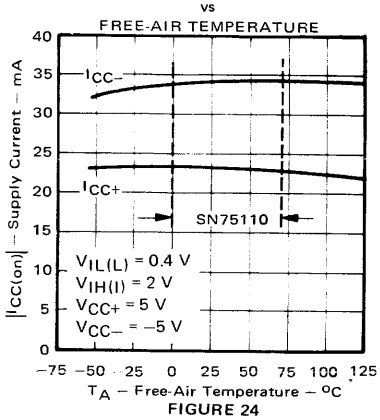


FIGURE 24

PROPAGATION DELAY TIME
(LOGIC INPUTS)
vs
FREE-AIR TEMPERATURE

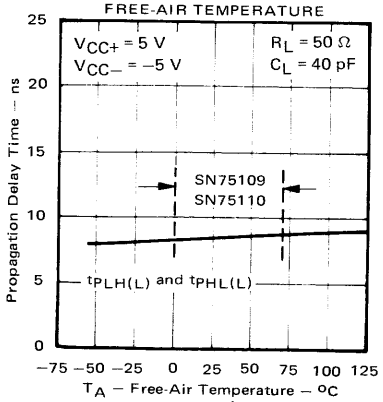


FIGURE 25

PROPAGATION DELAY TIME
(INHIBITOR INPUTS)
vs
FREE-AIR TEMPERATURE

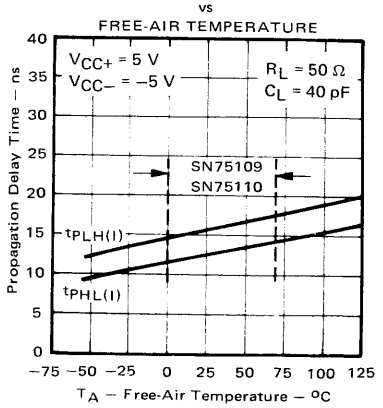


FIGURE 26

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATION DATA

BASIC BALANCED-LINE TRANSMISSION SYSTEM

Series 55/75107A dual line circuits are designed specifically for use in high-speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so that noise induced on one line is also induced on the other. The noise appears common-mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver-output circuit allows terminated transmission lines to be driven at normal line impedances. High-speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Cross-talk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately (30 + 1.3 L) nanoseconds, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

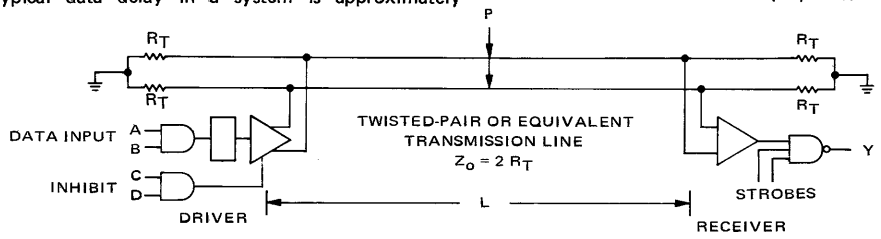
Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver-input logic levels. The voltage difference is approximately:

$$V_{DIFF} \simeq 1/2\ I_{O(on)} \cdot R_T.$$

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

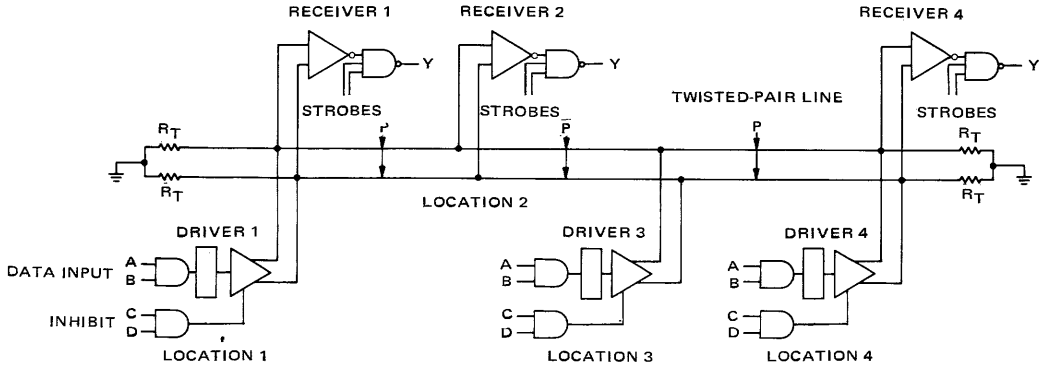
Line-termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

$$V_{DIFF} \simeq I_{O(on)} \cdot R_T.$$



DATA-BUS OR PARTY-LINE SYSTEM

The strobe feature of the receivers and the inhibit feature of the drivers allow the Series 55/75107A dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time-multiplexed on the transmission line. Series 55/75107A device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.



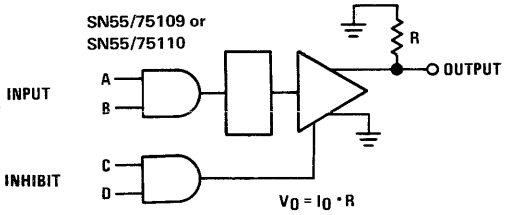
TYPICAL APPLICATION DATA

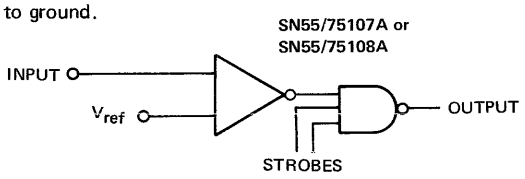
UNBALANCED OR SINGLE-LINE SYSTEMS

Series 55/75107A dual line circuits may also be used in unbalanced or single-line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environmental noise is not severe.

The receiver threshold level is established by applying a d-c reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of −3 volts to +3 volts. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

A single-ended output from a driver may be used in single-line systems. Coaxial or shielded line is preferred for minimum noise and cross-talk problems. For large signal swings, the high output current (12 mA) of the SN55/75110 is recommended. Drivers may be paralleled for higher current. The unused driver output must be tied to ground.





PRECAUTIONS IN THE USE OF SERIES 55/75107A LINE CIRCUITS

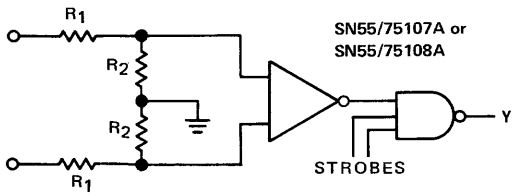
The following precautions should be observed when using or testing Series 55/75107A line circuits:

(1) Drivers, SN55/75109 and SN55/75110
When only one driver in a package is being used, the outputs of the other driver must either be grounded or inhibited in order to prevent excess power dissipation.

(2) Receivers, SN55/75107A and SN55/75108A
When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 volts and +3 volts, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers.

INCREASING COMMON-MODE INPUT VOLTAGE RANGE OF RECEIVER

The SN55/75107A and SN55/75108A line receivers feature a common-mode input voltage range of ±3 volts. This satisfies the requirements for all but the noisiest system applications. For these severe noise environments, the common-mode range can be extended by the use of external input attenuators. Common-mode input voltages can in this way be reduced to ±3 volts at the receiver input terminals. Differential data signals will be reduced proportionately. Input sensitivity, input impedance, and delay times will be adversely affected.

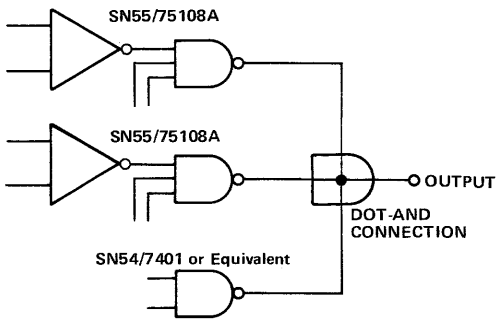


For balanced, terminated lines,
$Z_o = 2R_1 + 2R_2$

SN55/75108A DOT-AND OUTPUT CONNECTIONS

The SN55/75108A line receivers feature an open-collector-output circuit that can be connected in the DOT-AND logic configuration with other SN55/75108A outputs, SN5401/7401 outputs, or other similar outputs. This allows a level of logic to be implemented without additional logic delay.

For rules for such DOT-AND connections, refer to the SN5401 or SN7401 data sheet.



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

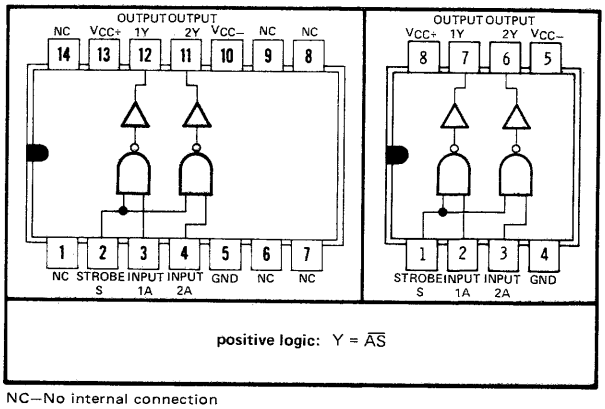
CIRCUIT TYPE SN75150
DUAL LINE DRIVER

SATISFIES REQUIREMENTS OF EIA STANDARD RS-232-C

- Withstands Sustained Output Short-Circuit to any Low-Impedance Voltage between −25 V and 25 V
- 2 μs Max Transition Time through the +3 V to −3 V Transition Region under Full 2500-pF Load
- Inputs Compatible with Most TTL and DTL Families
- Common Strobe Input
- Inverting Output
- Slew Rate can be Controlled with an External Capacitor at the Output
- Standard Supply Voltages . . . ±12 V

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)

P
DUAL-IN-LINE PACKAGE
(TOP VIEW)

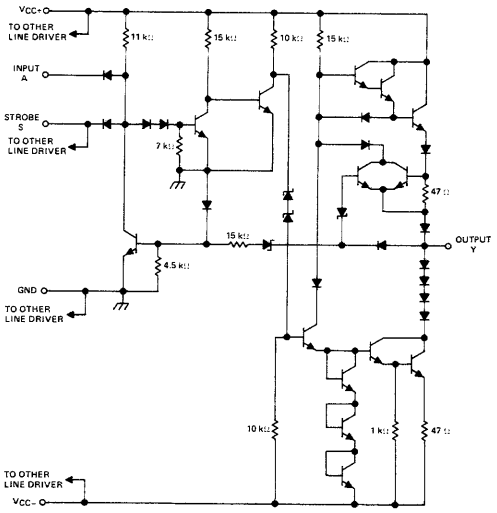


NC—No internal connection

description

The SN75150 is a monolithic dual line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500-pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and DTL families. Operation is from +12-volt and −12-volt power supplies. The SN75150 is characterized for operation from 0°C to 70°C.

schematic (each line driver)



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	15 V
Supply voltage V_{CC-} (see Note 1)	−15 V
Input voltage (see Note 1)	15 V
Applied output voltage (see Note 1)	±25 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

CIRCUIT TYPE SN75150
DUAL LINE DRIVER

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage V_{CC+}	10.8	12	13.2	V
Supply voltage V_{CC-}	−10.8	−12	−13.2	V
Input voltage, V_I	0		5.5	V
Applied output voltage, V_O			±15	V
Operating free-air temperature, T_A	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP†	MAX (SEE NOTE 2)	UNIT
V_{IH}	High-level input voltage	1			2			V
V_{IL}	Low-level input voltage	2					0.8	V
V_{OH}	High-level output voltage	2	V_{CC+} = 10.8 V, V_{IL} = 0.8 V,	V_{CC-} = −13.2 V, R_L = 3 kΩ to 7 kΩ	5	8		V
V_{OL}	Low-level output voltage	1	V_{CC+} = 10.8 V, V_{IH} = 2 V,	V_{CC-} = −10.8 V, R_L = 3 kΩ to 7 kΩ		−8	−5	V
I_{IH}	High-level input current	3	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 2.4 V	Data input		1	10	μA
				Strobe input		2	20	
I_{IL}	Low-level input current	3	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 0.4 V	Data input		−1	−1.6	mA
				Strobe input		−2	−3.2	
I_{OS}	Short-circuit output current	4	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V	V_O = 25 V		2		mA
				V_O = −25 V		−3		
				V_O = 0 V, V_I = 3 V		15		
				V_O = 0 V, V_I = 0 V		−15		
I_{CCH+}	Supply current from V_{CC+}, high-level output	5	V_{CC+} = 13.2 V, V_I = 0 V, T_A = 25°C	V_{CC-} = −13.2 V, R_L = 3 kΩ,		10	22	mA
I_{CCH-}	Supply current from V_{CC-}, high-level output					−1	−10	mA
I_{CCL+}	Supply current from V_{CC+}, low-level output	5	V_{CC+} = 13.2 V, V_I = 3 V, T_A = 25°C	V_{CC-} = −13.2 V, R_L = 3 kΩ,		8	17	mA
I_{CCL-}	Supply current from V_{CC-}, low-level output					−9	−20	mA

NOTE 2: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when −5 V is the maximum, the typical value is a more-negative voltage.

† All typical values are at V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low-to-high-level output	6	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ	0.2	1.4	2	μs
t_{THL}	Transition time, high-to-low-level output			0.2	1.5	2	μs
t_{TLH}	Transition time, low-to-high-level output	6	C_L = 15 pF, R_L = 7 kΩ		40		ns
t_{THL}	Transition time, high-to-low-level output				20		ns
t_{PLH}	Propagation delay time, low-to-high-level output	6	C_L = 15 pF, R_L = 7 kΩ		60		ns
t_{PHL}	Propagation delay time, high-to-low-level output				45		ns

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits‡

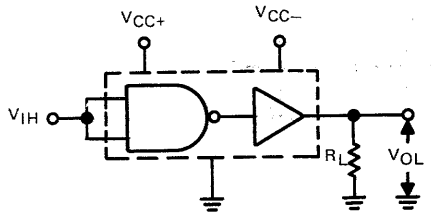
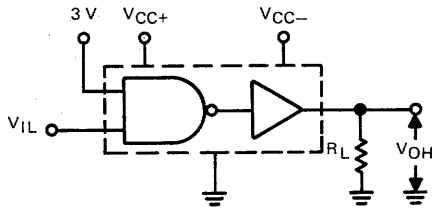


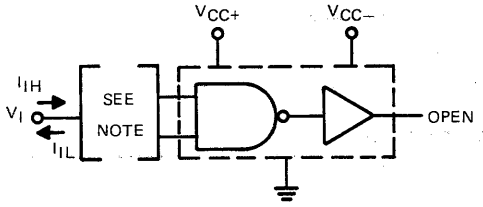
FIGURE 1–V_{IH}, V_{OL}



Each input is tested separately.

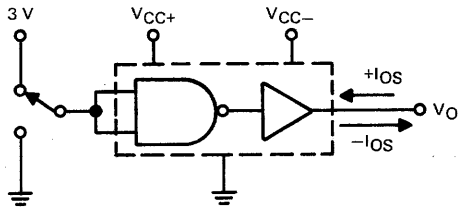
FIGURE 2–V_{IL}, V_{OH}

3



NOTE: When testing I_{IH}, the other input is at 3 V; when testing I_{IL}, the other input is open.

FIGURE 3–I_{IH}, I_{IL}



I_{OS} is tested for both input conditions at each of the specified output conditions.

FIGURE 4–I_{OS}

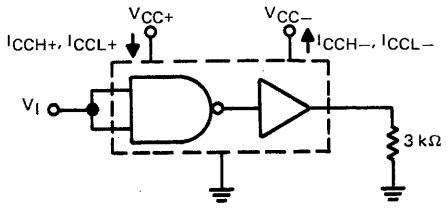
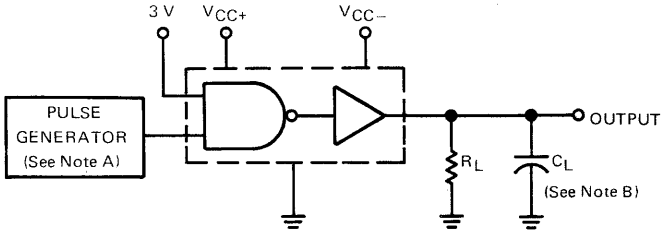


FIGURE 5–I_{CCH+}, I_{CCH-}, I_{CCL+}, I_{CCL-}

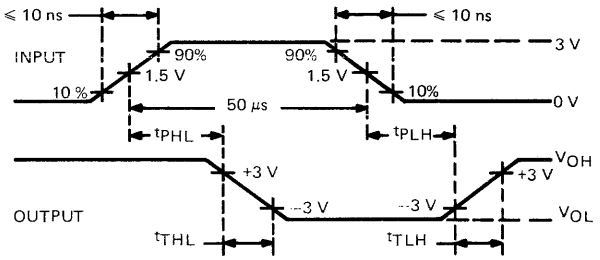
‡Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 6–SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
APPLIED OUTPUT VOLTAGE

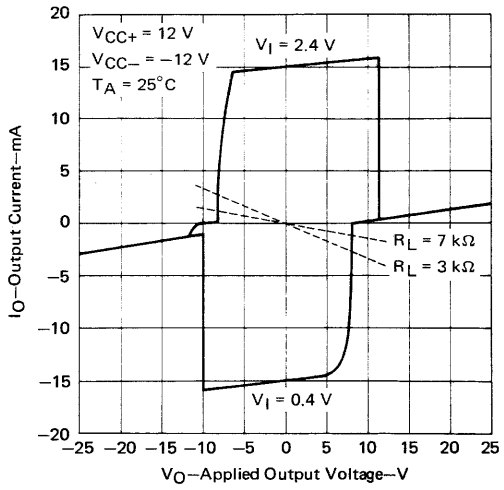


FIGURE 7

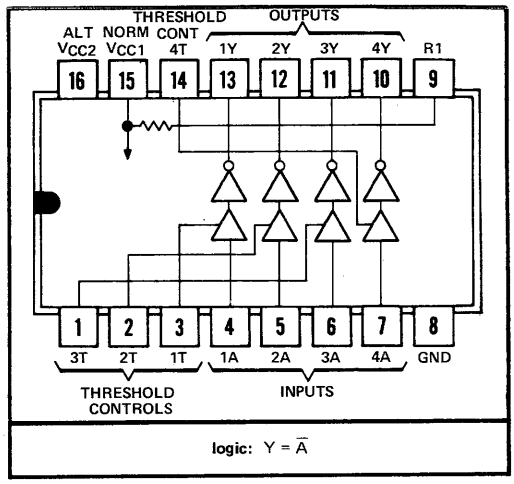
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE SN75154
QUADRUPLE LINE RECEIVER

SATISFIES REQUIREMENTS OF EIA STANDARD RS-232-C

- Input Resistance . . . 3 kΩ to 7 kΩ over Full RS-232-C Voltage Range
- Input Threshold Adjustable to Meet "Fail-Safe" Requirements Without Using External Components
- Built-In Hysteresis for Increased Noise Immunity
- Inverting Output Compatible with DTL or TTL
- Output with Active Pull-Up for Symmetrical Switching Speeds
- Standard Supply Voltages . . . 5 V or 12 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75154 is a monolithic quadruple line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are for relatively short, single-line, point-to-point data transmission and for level translators. Operation is normally from a single five-volt supply; however, a built-in option allows operation from a 12-volt supply without the use of additional components. The output is compatible with most TTL and DTL circuits when either supply voltage is used.

In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. See typical characteristics. In this mode of operation, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

The SN75154 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Normal supply voltage (pin 15), V_{CC1} (see Note 1)	7 V
Alternate supply voltage (pin 16), V_{CC2} (see Note 1)	14 V
Input voltage (see Note 1)	±25 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Normal supply voltage (pin 15), V_{CC1}	4.5	5	5.5	V
Alternate supply voltage (pin 16), V_{CC2}	10.8	12	13.2	V
Input voltage			±15	V
Normalized fan-out from each output, N			10	
Operating free-air temperature, T_A	0	25	70	°C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE SN75154
QUADRUPLE LINE RECEIVER

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX (SEE NOTE 2)	UNIT
V_{IH}	High-level input voltage		1		3			V
V_{IL}	Low-level input voltage		1				−3	V
V_{T+}	Positive-going threshold voltage	Normal operation	1		0.8	2.2	3	V
		Fail-safe operation			0.8	2.2	3	
V_{T-}	Negative-going threshold voltage	Normal operation	1		−3	−1.1	0	V
		Fail-safe operation			0.8	1.4	3	
$V_{T+}-V_{T-}$	Hysteresis	Normal operation	1		0.8	3.3	6	V
		Fail-safe operation			0	0.8	2.2	
V_{OH}	High-level output voltage		1	I_{OH} = −400 μA	2.4	3.5		V
V_{OL}	Low-level output voltage		1	I_{OL} = 16 mA		0.23	0.4	V
r_I	Input resistance		2	ΔV_I = −25 V to −14 V	3	5	7	kΩ
				ΔV_I = −14 V to −3 V	3	5	7	
				ΔV_I = −3 V to 3 V	3	6		
				ΔV_I = 3 V to 14 V	3	5	7	
				ΔV_I = 14 V to 25 V	3	5	7	
$V_{I(open)}$	Open-circuit input voltage		3	I_I = 0	0	0.2	2	V
I_{OS}	Short-circuit output current†		4	V_{CC1} = 5.5 V, V_I = −5 V	−10	−20	−40	mA
I_{CC1}	Supply current from V_{CC1}		5	V_{CC1} = 5.5 V, T_A = 25°C		20	35	mA
I_{CC2}	Supply current from V_{CC2}			V_{CC2} = 13.2 V, T_A = 25°C		23	40	

†Not more than one output should be shorted at a time.

‡ All typical values are at V_{CC1} = 5 V, T_A = 25°C.

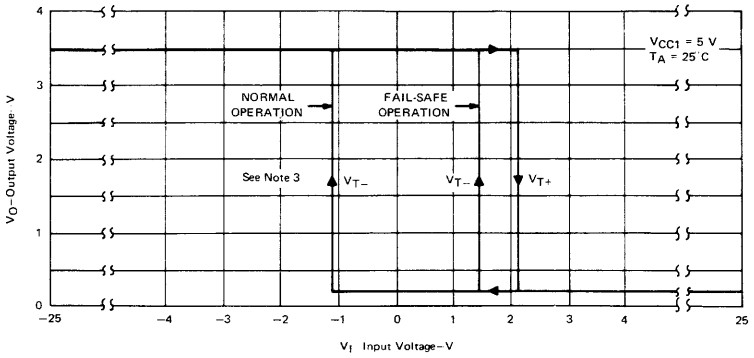
NOTE 2: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic and threshold levels only, e.g., when −3 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC1} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	6	C_L = 50 pF, R_L = 390 Ω		22		ns
t_{PHL}	Propagation delay time, high-to-low-level output				20		ns
t_{TLH}	Transition time, low-to-high-level output				9		ns
t_{THL}	Transition time, high-to-low-level output				6		ns

TYPICAL CHARACTERISTICS

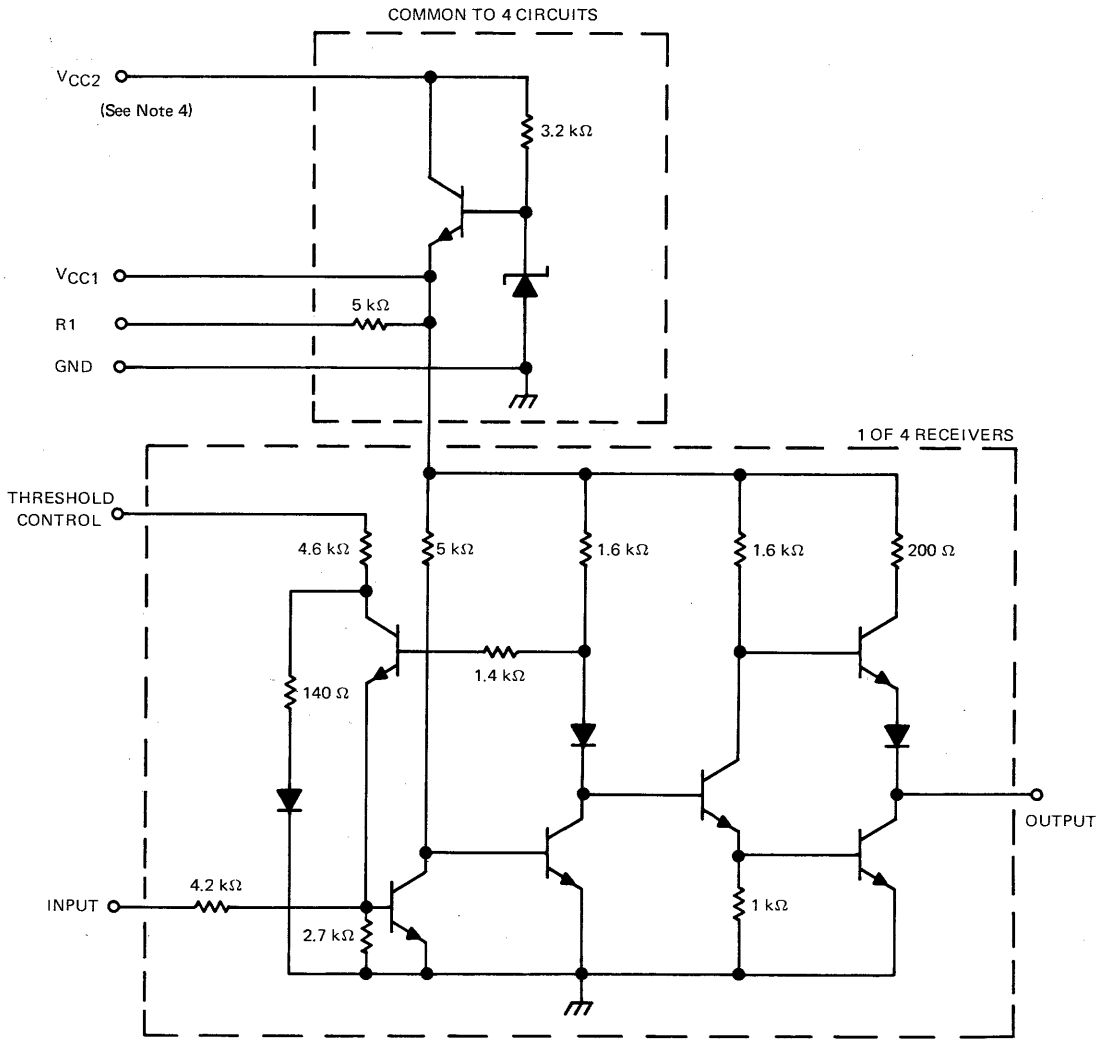
OUTPUT VOLTAGE vs INPUT VOLTAGE



NOTE 3: For normal operation, the threshold controls are connected to V_{CC1}, pin 15. For fail-safe operation, the threshold controls are open.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

schematic



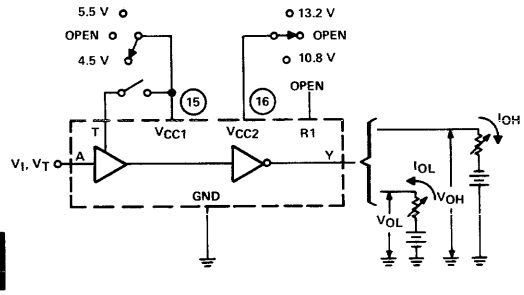
Component values shown are nominal

⏚ . . . Substrate

NOTE 4: When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

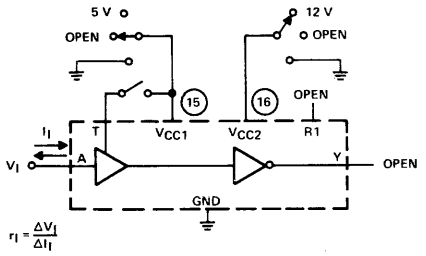


NOTES: A. Momentarily apply −5 V, then 0.8 V.
B. Momentarily apply 5 V, then ground.

TEST TABLE

TEST	MEASURE	A	T	Y	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open-circuit input (fail safe)	V_{OH}	Open	Open	I_{OH}	4.5 V	Open
	V_{OH}	Open	Open	I_{OH}	Open	10.8 V
V_{T+} min, V_{T-} min (fail safe)	V_{OH}	0.8 V	Open	I_{OH}	5.5 V	Open
	V_{OH}	0.8 V	Open	I_{OH}	Open	13.2 V
V_{T+} min (normal)	V_{OH}	Note A	Pin 15	I_{OH}	5.5 V and T	Open
	V_{OH}	Note A	Pin 15	I_{OH}	T	13.2 V
V_{IL} max, V_{T-} min (normal)	V_{OH}	−3 V	Pin 15	I_{OH}	5.5 V and T	Open
	V_{OH}	−3 V	Pin 15	I_{OH}	T	13.2 V
V_{IH} min, V_{T+} max, V_{T-} max (fail safe)	V_{OL}	3 V	Open	I_{OL}	4.5 V	Open
	V_{OL}	3 V	Open	I_{OL}	Open	10.8 V
V_{IH} min, V_{T+} max (normal)	V_{OL}	3 V	Pin 15	I_{OL}	4.5 V and T	Open
	V_{OL}	3 V	Pin 15	I_{OL}	T	10.8 V
V_{T-} max (normal)	V_{OL}	Note B	Pin 15	I_{OL}	5.5 V and T	Open
	V_{OL}	Note B	Pin 15	I_{OL}	T	13.2 V

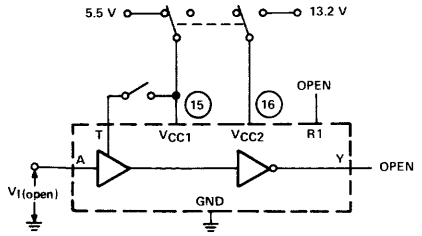
FIGURE 1 – V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}



TEST TABLE

T	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open	5 V	Open
Open	GND	Open
Open	Open	Open
Pin 15	T and 5 V	Open
GND	GND	Open
Open	Open	12 V
Open	Open	GND
Pin 15	T	12 V
Pin 15	T	GND
Pin 15	T	Open

FIGURE 2–r_I



TEST TABLE

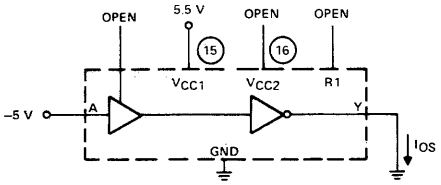
T	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open	5.5 V	Open
Pin 15	5.5 V	Open
Open	Open	13.2 V
Pin 15	T	13.2 V

FIGURE 3–$V_{I(open)}$

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

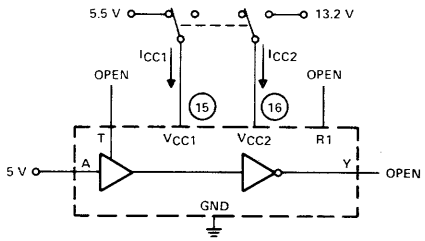
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



Each output is tested separately.

FIGURE 4–I_{OS}



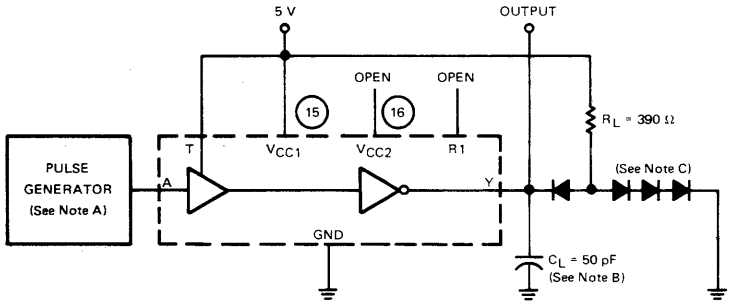
All four line receivers are tested simultaneously.

FIGURE 5–I_{CC}

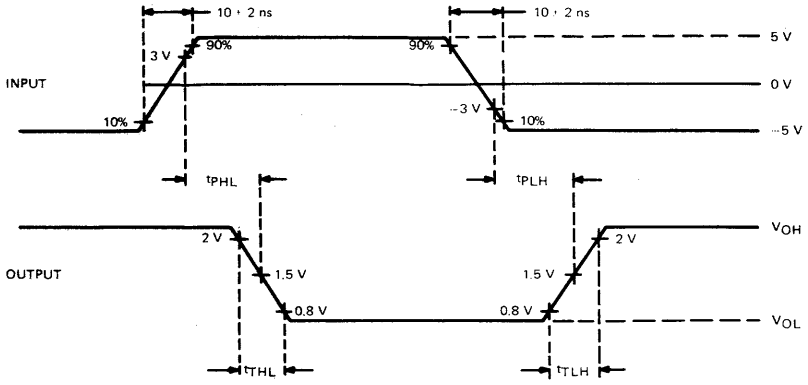
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

3

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

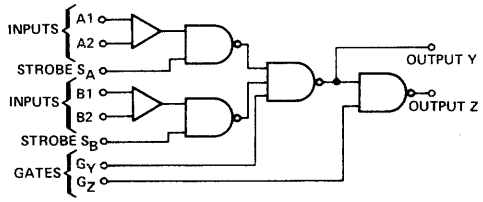
NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_w = 200 ns, duty cycle ≤ 20%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 6–SWITCHING TIMES

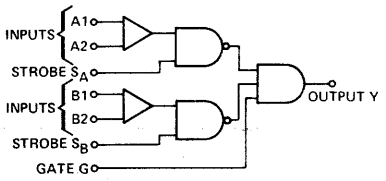
SENSE AMPLIFIER SELECTION GUIDE

TYPE	SN7520, SN7521	SN7522, SN7523	SN7524, SN7525 SN75234, SN75235†	SN7526, SN7527	SN7528, SN7529 SN75238, SN75239†
Features	• Provide Memory Data Register • Complementary Outputs	• Open-Collector Output Stage • High Fan-Out	• Dual Sense Channels • Independent Strobes	• Complete Memory Data Function • Effective Strobe Width of Less than 10 ns	• Test Points for Strobe Timing Adjustment • Dual Sense Channels
Packages	J, N	J, N	J, N	J, N	J, N
Applications	Large Memories	Large Memories	General Purpose Sense Amplifiers	High-Performance Sense Amplifiers	General Purpose Sense Amplifiers
Application Notes	CA-101: Operating and Use of Series 7520N Sense Amplifiers				

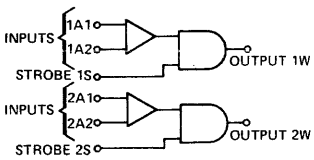
3 block diagrams



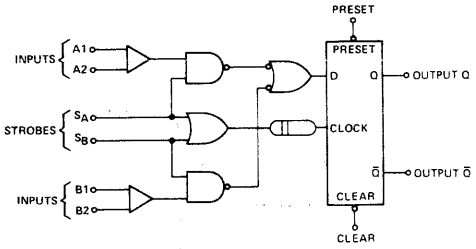
SN7520, SN7521



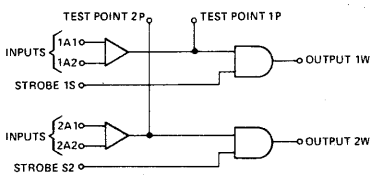
SN7522, SN7523



SN7524, SN7525
SN75234, SN75234†



SN7526, SN7527



SN7528, SN7529
SN75238, SN75239†

†Types SN75234, SN75235, SN75238, and SN75239 are indentical to types SN7524, SN7525, SN7528, and SN7529, respectively, except that an additional stage has been added to the output gate to provide an inverted output.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

HIGH-SPEED SENSE AMPLIFIERS FOR CONVERSION OF COINCIDENT-CURRENT MEMORY READOUT TO SATURATED DIGITAL-LOGIC LEVELS

performance features

- high speed and fast recovery time
- time and amplitude signal discrimination
- adjustable input threshold voltage levels
- narrow region of threshold voltage uncertainty
- multiple differential-input preamplifiers
- high d-c noise margin—typically one volt
- good fan-out capability

ease-of-design features

- choice of output circuit function
- TTL or DTL drive capability
- standard logic supply voltages
- plug-in configuration ideal for flow-soldering techniques
- pins on 100-mil grid spacings for industrial-type circuit boards

description

Series 7520 monolithic sense amplifiers are designed for use with high-speed memory systems. These sense amplifiers detect bipolar differential-input signals from the memory and provide the interface circuitry between the memory and the logic section. Low-level pulses originating in the memory are transformed into logic levels compatible with standard transistor-transistor-logic (TTL) and diode-transistor-logic (DTL) circuits.

These sense amplifiers feature multiple, differential-input preamplifiers and versatile gating and output circuits, permitting a significant reduction in the circuitry required to accomplish the sensing function. A unique circuit design provides inherent stability of the input threshold level over a wide range of power-supply voltage levels and temperature ranges. Independent strobing of each of the dual sense-input channels ensures maximum versatility and permits detection to occur when the signal-to-noise ratio is at a maximum. The gate and strobe inputs and the outputs are compatible with standard TTL and DTL digital logic circuits.

The SN7520 and SN7521 circuits may be used to perform the functions of a flip-flop or register which responds to the sense and strobe input conditions.

The SN7522 and SN7523 circuits feature a high-fan-out, single-ended, open-collector output stage. In addition, they may be used to expand the inputs to an SN7520 or SN7521 circuit, or to perform the wired-AND function.

The SN7524 and SN7525 circuits provide for independent, dual-channel sensing with separate outputs.

The SN7526 and SN7527 circuits have a D-type flip-flop output with external clear and preset inputs.

The SN7528 and SN7529 circuits are similar to the SN7524 and SN7525 except that the output of each preamplifier is available as a test point.

CONTENTS

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES 7520
SENSE AMPLIFIERS

design characteristics

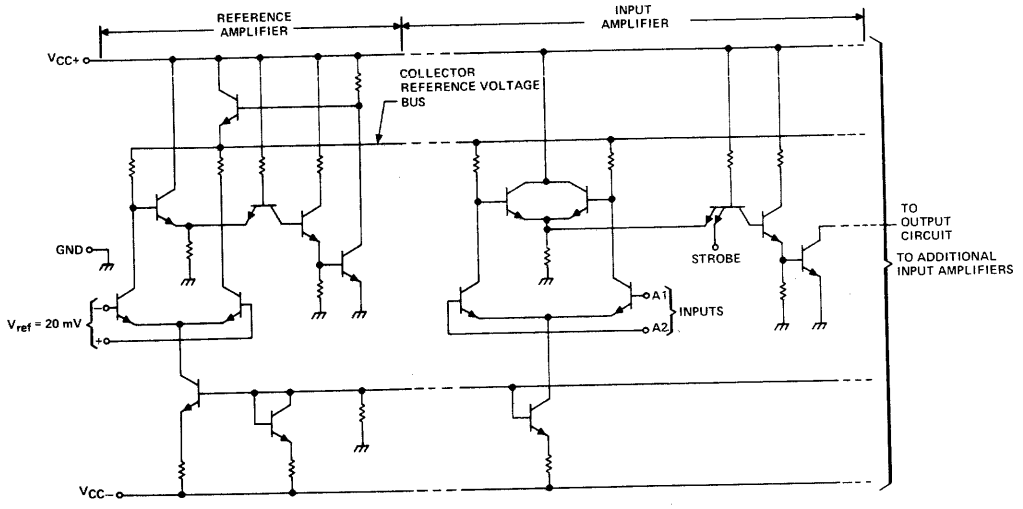
Series 7520 sense amplifiers are completely d-c coupled. Previous designs have resulted in circuits in which the threshold level could not be closely controlled because they were highly sensitive to changes in the d-c levels throughout the amplifier. This was due primarily to the required tolerances on the absolute value of resistors and the resistor temperature coefficients. The "matched-amplifier" design of Series 7520 circuits depends on resistor ratios rather than absolute values. In this design, excellent stability of the threshold level can be maintained despite component variations and changes in bias levels. The capability of multiple-input amplifiers increases the versatility of the design.

The basic circuit is used to implement several sense amplifier designs. Additional logic circuitry is added to the strobe-gate output to provide versatile sensing functions. The outputs of two or more input amplifiers can be combined to implement multiple-input amplifiers, a function not previously available in integrated form. The d-c coupled design eliminates many of the problems associated with overload recovery time and threshold shift (with high input repetition rates) usually encountered in sense amplifier designs that use reactive coupling components.

circuit operation

The basic Series 7520 sense amplifier strobe and threshold circuit is shown in Figure A. The design uses a "matched-amplifier" concept which takes advantage of the inherent excellent component matching and thermal tracking characteristics of monolithic integrated circuits. A reference amplifier is used to generate the collector reference voltage which is distributed to the input amplifiers. Application of an external reference voltage, V_{ref}, establishes the input-amplifier threshold voltage level, V_T. The design is such that there is 1:1 correspondence between the applied reference voltage, V_{ref}, and the nominal threshold voltage level, V_T. The reference and input amplifiers use identical circuit configurations; therefore, changes in bias levels introduced into the input amplifier, through changes in temperature or power-supply voltage levels, are compensated by similar changes in the reference amplifier.

The collector reference voltage, supplied by the reference amplifier, can be used to control the threshold-voltage level of more than one input amplifier, thereby establishing equal threshold levels to all of the input sense channels simultaneously.



Patent pending

FIGURE A—BASIC SERIES 7520 SENSE-AMPLIFIER CIRCUIT

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

circuit operation (continued)

The second stage of the input amplifier is a TTL gate. The gate provides the threshold action for the input sense channel and provides a convenient point in the circuit to accomplish the strobe function. The differential-input sense signal switches the output of the TTL gate only when the strobe input voltage is higher than the logic input threshold voltage. The strobe input, therefore, provides the sense amplifier with the capability of time discrimination, allowing the input signal to be detected when the signal-to-noise ratio is at a maximum.

The logic inputs (i.e., gate and strobe) of Series 7520 sense amplifiers are designed to be compatible with Series 74 TTL digital integrated circuits. The multiple-emitter transistors are utilized to provide inherent switching-time advantages over other saturated-logic schemes. The same guaranteed noise margin and logic threshold voltage as for Series 74 are assured each of the gate and strobe inputs. This is accomplished by testing each logic input under standard Series 74 test conditions, i.e., 2 volts for high-level input condition and 0.8 volt for low-level input conditions. Since the guaranteed minimum high-level output voltage is 2.4 volts and the guaranteed maximum low-level output voltage is 0.4 volt, a minimum noise margin of 0.4 volt is assured at each input.

SN7520 and SN7521 circuit

This circuit is a dual-channel sense amplifier with the preamplifiers connected to a common output stage and a complementary output stage. The output circuit is composed of two cascaded NAND gates, each with external gate inputs. External connection of the Z output and the G_Y input results in a flip-flop or register that is set by signals at the differential-input terminals. Reset of the register is performed at the G_Z input. Capacitive coupling from output Z to G_Y results in output pulse stretching. In either connection, complementary output levels are available. The gate and strobe inputs and the outputs are compatible with standard TTL logic. The input function of SN7520/SN7521 can be expanded by connecting the Y output of SN7522/SN7523 to the G_Y input of the circuit being expanded.

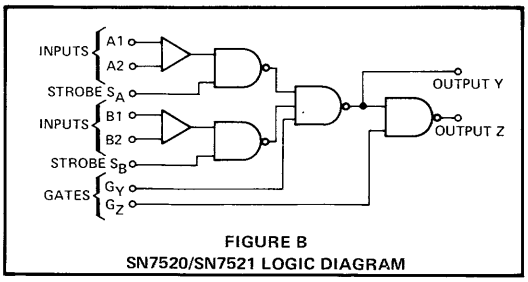


FIGURE B
SN7520/SN7521 LOGIC DIAGRAM

logic: $Y = \overline{G}_Y + A \cdot S_A + B \cdot S_B$
$Z = \overline{G}_Z + \overline{Y}$
$Z = \overline{G}_Z + G_Y (\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

SN7522 and SN7523 circuit

This circuit is a dual-channel sense amplifier with the preamplifiers connected to a common output stage. The output circuit features an open-collector output which permits two or more of these outputs to be connected in the wire-AND configuration. Each package includes a load resistor that may be used as the output pull-up resistor. High sink-current capability is a feature of this design, and a separate ground terminal is used for the output circuitry. These devices can also be used as input expanders for the SN7520/SN7521 circuit.

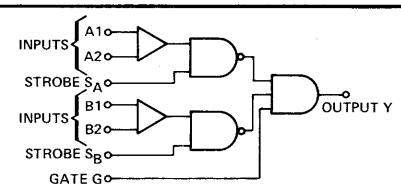


FIGURE C
SN7522/SN7523 LOGIC DIAGRAM

logic: $Y = G(\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

SN7524 and SN7525 circuit

This circuit features two completely independent sense amplifiers in a single package. Each channel features high fan-out capability.

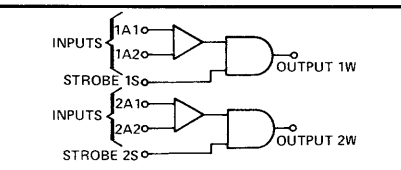


FIGURE D
SN7524/SN7525 LOGIC DIAGRAM
SN75234/SN75235 SAME EXCEPT INVERTED OUTPUT

logic: W = AS for SN7524 and SN7525
W = $\overline{AS}$ for SN75234 and SN75235

SN7526 and SN7527 circuit

This circuit is a dual-channel sense amplifier with the preamplifiers connected to a D-type flip-flop with external clear and preset inputs. A delay between the strobe input terminals and the clock input of the flip-flop ensures that data is set up at the D input of the flip-flop prior to clocking.

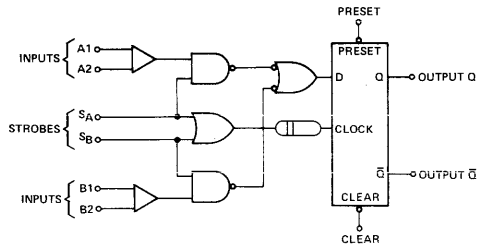


FIGURE E
SN7526/SN7527 LOGIC DIAGRAM

logic: See truth table on page 14.

SN7528 and SN7529 circuit

This circuit features two separate single-preamplifier sense amplifiers in a single package. The output of each preamplifier is available as a test point. These test points can be used to observe the amplified core signal to facilitate accurate strobe timing. When using this device, care should be taken to avoid coupling the strobe signal or other stray signals to the test point. Excessive loading of the test point is also to be avoided. The result of either coupling or loading will be a change in the threshold voltage of the device. The output circuit of each channel features a simple TTL gate configuration with a high fan-out capability.

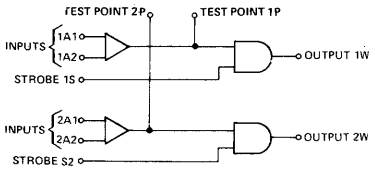


FIGURE F
SN7528/SN7529 LOGIC DIAGRAM
SN75238/SN75239 SAME EXCEPT INVERTED OUTPUT

logic: W = AS for SN7528 and SN7529
W = $\overline{AS}$ for SN75238 and SN75239

SN75234, SN75235, SN75238, SN75239 circuits

These dual sense amplifier circuits are the same as SN7524, SN7525, SN7528, and SN7529, respectively, except that an additional stage has been added to the output gate to provide an inverted output. Compared to using a separate gate for inversion, not only is package count reduced, but less propagation delay is added.

reference voltage considerations

These sense amplifiers feature a variable-threshold voltage level with simultaneous adjustment of both sense channels or both sense amplifiers by a single reference voltage. The operating threshold voltage level of the input amplifiers is established by and is approximately equal to the applied reference input voltage, V_{ref}. Several methods may be used to supply this reference voltage; however, methods given here will be limited to the discussion of fundamental design considerations. These sense amplifiers are recommended for use in systems requiring threshold voltage levels of ±15 to ±40 mV.

A simple method of generating the reference voltage is the use of a resistor voltage divider from either the positive (V_{CC+}) or negative (V_{CC-}) voltage supplies. See Figure G. This type of voltage divider may be used to supply an individual reference amplifier or to supply a number of paralleled reference amplifiers. The bias current required at the reference amplifier input is low (nominally 30 μA); therefore, voltage dividers of this type may normally be operated with very low current requirements. In noisy environments, the use of a filter capacitor across the inputs is recommended. By locating the capacitor as close to the device terminals as possible, noise and stray signals will be presented common-mode to the reference amplifier and thus be rejected.

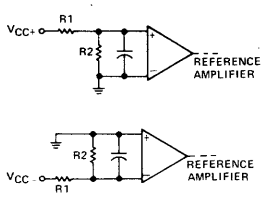


FIGURE G

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

input line layout considerations

Input sensitivity and device speed require adequate precautions in the routing of signal input and reference lines to prevent noise pickup. Bypassing of supply and reference inputs at the device with low-inductance disc ceramic capacitors, and use of a good ground plane to separate strobe and output lines from sense and reference input lines, is recommended.

sense-input termination resistor considerations

Termination resistors are intentionally omitted from the sense-input terminals so the designer may select resistor values which will be compatible with the particular application. Matched termination resistors, (R_T, Figure H), normally in the range of 25 Ω to 200 Ω each, are required not only to terminate the sense line in a desired impedance but also to provide a d-c path for the sense-input bias currents. Careful matching of the resistor pairs should be observed or effective common-mode rejection will be reduced.

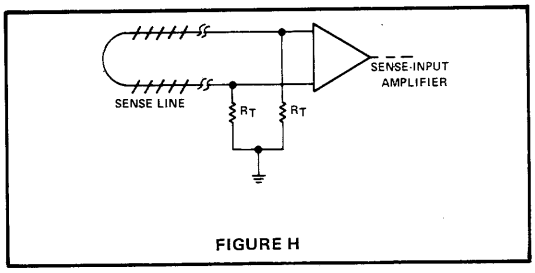


FIGURE H

3

output drive capability

The output circuits of these sense amplifiers feature the ability to sink or supply load current, This capability permits direct use with both TTL- and DTL-type loads. The open-collector output of the SN7522/SN7523 circuit may be connected to similar outputs to perform the wire-AND function. Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuit indicate the actual direction of current flow.

logic input current requirements

Logic input current requirements are specified at worst-case power-supply conditions over the operating free-air temperature range of 0°C to 70°C. The logic input currents are identical to and compatible with Series 74 TTL digital integrated circuits. Each logic input of the multiple-emitter input transistors requires no more than a 1.6-mA flow out of the input at a low logic level. Each input emitter requires current into the input when it is at a high-logic level. This current is 40 μA maximum. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

absolute maximum ratings (over free-air temperature range unless otherwise noted)

Supply voltages (see Note 1)	
V_{CC+}	7 V
V_{CC-}	−7 V
Differential input voltage, V_{ID} or V_{ref}	±5 V
Voltage from any input to ground (see Note 2)	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	−55°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC+} (see Note 1)	4.75	5	5.25	V
V_{CC-} (see Note 1)	−4.75	−5	−5.25	V
V_{ref}	15		40	mV

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Strobe and gate input voltages must be zero or positive with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

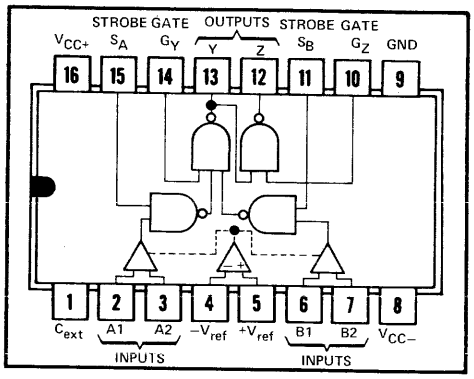
CIRCUIT TYPES SN7520,SN7521
DUAL-CHANNEL SENSE AMPLIFIERS WITH COMPLEMENTARY OUTPUTS

TRUTH TABLE

INPUTS						OUTPUTS	
A	B	G_Y	G_Z	S_A	S_B	Y	Z
X	X	L	X	X	X	H	$\overline{G}_Z$
H	X	X	X	H	X	H	$\overline{G}_Z$
X	H	X	X	X	H	H	$\overline{G}_Z$
L	L	H	X	X	X	L	H
L	X	H	X	X	L	L	H
X	L	H	X	L	X	L	H
X	X	H	X	L	L	L	H
X	X	X	L	X	X	X	H

J OR N

DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{G}_Y + A \cdot S_A + B \cdot S_B$

$Z = \overline{G}_Z + \overline{Y}$

$Z = \overline{G}_Z + G_Y(\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

3

definition of logic levels

INPUT	H	L	X
A or B†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
Any G or S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A and B are differential voltages (V_{ID}) between A1 and A2 or B1 and B2, respectively. For these circuits, V_{ID} is considered positive regardless of which terminal of each pair is positive with respect to the other.

electrical characteristics (unless otherwise noted V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential input threshold voltage (see Note 3, page 17)	1	V_{ref} = 15 mV	SN7520	11	15	19	mV
				SN7521	8	15	22	
			V_{ref} = 40 mV	SN7520	36	40	44	
				SN7521	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns			±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage (strobe and gate inputs)	3			2			V
V_{IL}	Low-level input voltage (strobe and gate inputs)	3					0.8	V
V_{OH}	High-level output voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4		V
V_{OL}	Low-level output voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	High-level input current (strobe and gate inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1	mA
I_{IL}	Low-level input current (strobe and gate inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1	−1.6	mA
$I_{OS(Y)}$	Short-circuit output current into Y	5	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−3		−5	mA
$I_{OS(Z)}$	Short-circuit output current into Z	5	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			28	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−14	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geqslant$ 100 pF, T_A = 25°C

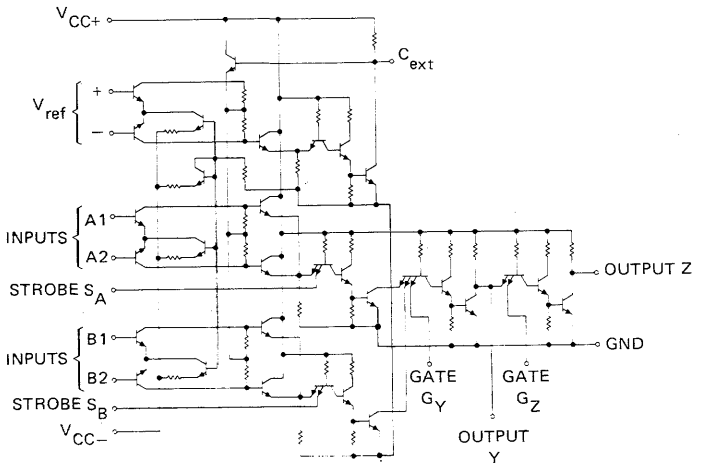
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(DY)}$	A1-A2 OR B1-B2	Y	32	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(DY)}$						20		
$t_{PLH(DZ)}$	A1-A2 OR B1-B2	Z	32	C_L = 15 pF, R_L = 288 Ω		30		ns
$t_{PHL(DZ)}$						35	55	
$t_{PLH(SY)}$	STROBE A OR B	Y	32	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(SY)}$						20		
$t_{PLH(SZ)}$	STROBE A OR B	Z	32	C_L = 15 pF, R_L = 288 Ω		30		ns
$t_{PHL(SZ)}$						35	55	
$t_{PLH(GY, Y)}$	GATE G_Y	Y	33	C_L = 15 pF, R_L = 288 Ω		15	25	ns
$t_{PHL(GY, Y)}$						10		
$t_{PLH(GY, Z)}$	GATE G_Y	Z	33	C_L = 15 pF, R_L = 288 Ω		15		ns
$t_{PHL(GY, Z)}$						20	30	
$t_{PLH(GZ, Z)}$	GATE G_Z	Z	34	C_L = 15 pF, R_L = 288 Ω		15		ns
$t_{PHL(GZ, Z)}$						10	20	

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geqslant$ 100 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic

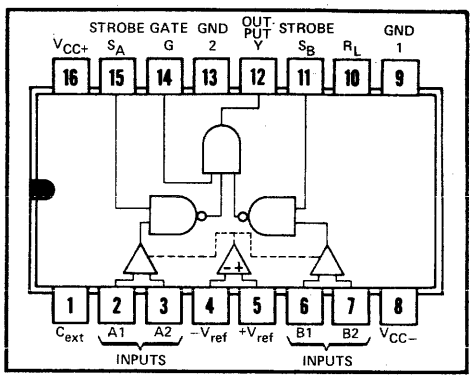


CIRCUIT TYPES SN7522, SN7523
DUAL-CHANNEL SENSE AMPLIFIERS

TRUTH TABLE

INPUTS					OUTPUT
A	B	G	S_A	S_B	Y
L	L	H	X	X	H
L	X	H	X	L	H
X	L	H	L	X	H
X	X	H	L	L	H
X	X	L	X	X	L
H	X	X	H	X	L
X	H	X	X	H	L

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



definition of logic levels

INPUT	H	L	X
A or B†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
Any G or S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A and B are differential voltages (V_{ID}) between A1 and A2 or B1 and B2, respectively. For these circuits, V_{ID} is considered positive regardless of which terminal of each pair is positive with respect to the other.

positive logic: $Y = G(\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

electrical characteristics (unless otherwise noted V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential input threshold voltage (see Note 3, page 17)	7	V_{ref} = 15 mV	SN7522	11	15	19	mV
				SN7523	8	15	22	
			V_{ref} = 40 mV	SN7522	36	40	44	
				SN7523	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns			±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage (strobe and gate inputs)	8			2			V
V_{IL}	Low-level input voltage (strobe and gate inputs)	8					0.8	V
V_{OH}	High-level output voltage	8	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4		V
V_{OL}	Low-level output voltage	8	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	High-level input current (strobe and gate inputs)	9	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1	mA
I_{IL}	Low-level input current (strobe and gate inputs)	9	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1	−1.6	mA
I_{OH}	High-level output current	10	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, V_O = 5.25 V				250	μA
I_{OS}	Short-circuit output current	11	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			27	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geqslant$ 100 pF, T_A = 25°C

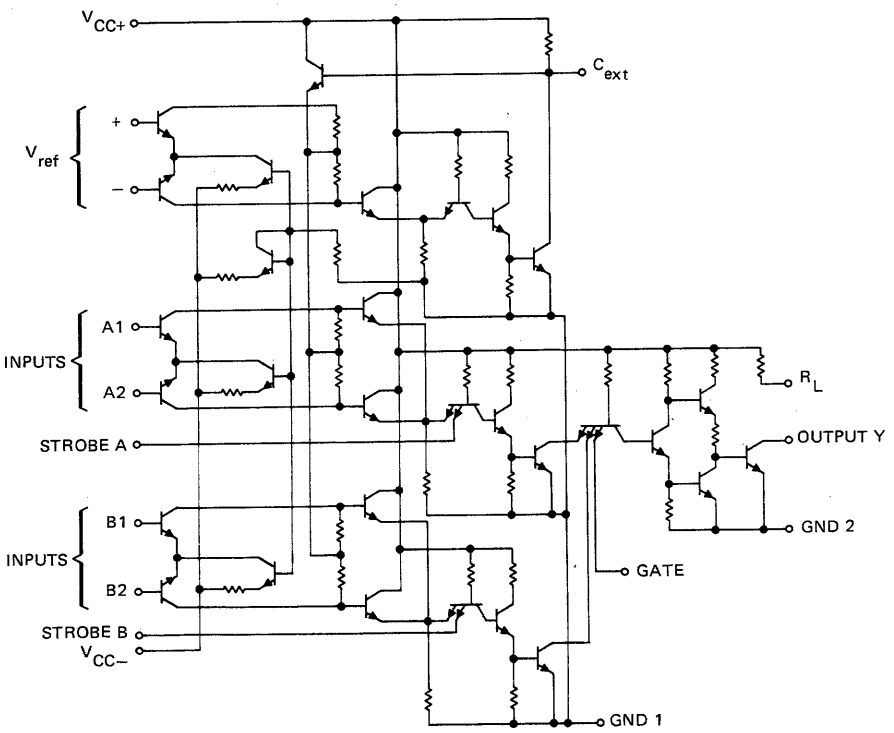
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1-A2 OR B1-B2	Y	35	C_L = 15 pF, R_L = 288 Ω		20		ns
$t_{PHL(D)}$						30	45	
$t_{PLH(S)}$	STROBE A OR B	Y	35	C_L = 15 pF, R_L = 288 Ω		20		ns
$t_{PHL(S)}$						20	40	
$t_{PLH(G)}$	GATE	Y	36	C_L = 15 pF, R_L = 288 Ω		10		ns
$t_{PHL(G)}$						15	25	

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geqslant$ 100 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential input-overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic



APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-AND function, and simultaneously, will drive from one to nine Series 54/74 loads. When no other open-collector gates are paralleled, this gate may be used to drive ten Series 54/74 loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available while the output is high. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the low level even if one of the paralleled outputs is sinking all the current.

In both conditions (low and high level) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

high-level (off-state) circuit calculations (see figure I)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the V_{OH} level required at the load:

$$V_{RL} = V_{CC} - V_{OH\ min}$$

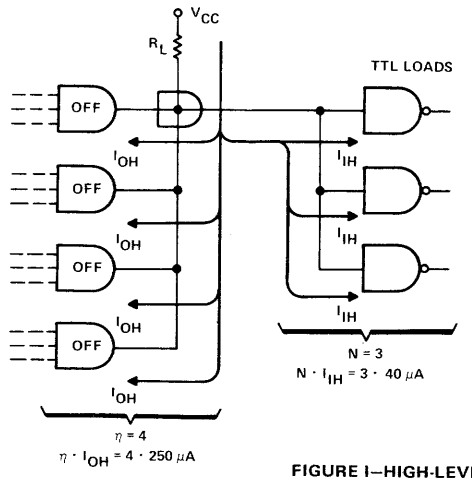
The total current through the load resistor (I_{RL}) is the sum of the load currents (I_{IH}) and off-state reverse currents (I_{OH}) through each of the wire-AND-connected outputs:

$$I_{RL} = \eta \cdot I_{OH} + N \cdot I_{IH} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\ min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

where η = number of gates wire-AND-connected, and N = number of TTL loads.



Calculation:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\ min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

$$R_{L(max)} = \frac{5 - 2.4}{0.001 + 0.00012}\,\Omega = \frac{2.6}{0.00112}\,\Omega = 2321\,\Omega$$

FIGURE I—HIGH-LEVEL CIRCUIT CONDITIONS

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

APPLICATION DATA

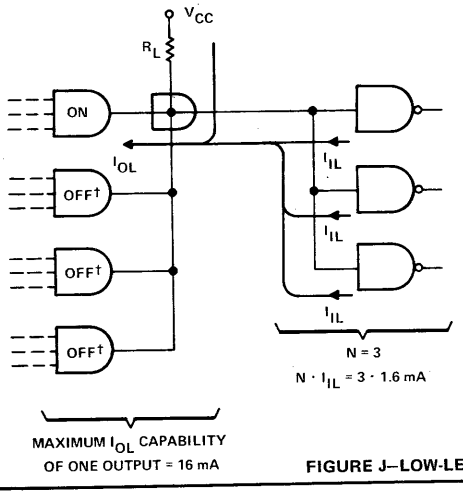
low-level (on-state) circuit calculations (see figure J)

The current through the resistor must be limited to the maximum sink-current of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during low-level periods, the current must be limited to 16 mA, the maximum current which will ensure a low-level maximum of 0.4 volt.

Also, fan-out must be considered. Part of the 16 mA will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{IL}}$$



Calculation:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{OL}}$$

$$R_{L(min)} = \frac{5 - 0.4}{0.016 - 0.0048}\ \Omega = \frac{4.6}{0.0112}\ \Omega = 410\ \Omega$$

†Current into OFF outputs is negligible at the low logic level.

FIGURE J–LOW-LEVEL CIRCUIT CONDITIONS

driving series 54/74 loads and combining outputs

Table 1 provides minimum and maximum resistor values, calculated from equations shown above, for driving one to ten Series 54/74 loads and wire-AND connecting two to seven parallel outputs. Each value shown for one wire-AND output is determined by the fan-out plus the cutoff current of a single output transistor. Extension beyond seven wire-AND connections is permitted with fan-outs of seven or less if a valid minimum and maximum R_L is possible. When fanning-out to ten Series 54/74 loads, the calculation for the minimum value of R_L indicates that an infinite resistance should be used ($V_{RL} \div 0 = \infty$); however, the use of a 4-kΩ resistor in this case will satisfy the high-level condition and limit the low level to less than 0.43 volt.

TABLE 1

FAN-OUT TO TTL LOADS	WIRE-AND OUTPUTS							
	1	2	3	4	5	6	7	1 to 7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000§
	MAXIMUM							MIN
	LOAD RESISTOR VALUE IN OHMS							

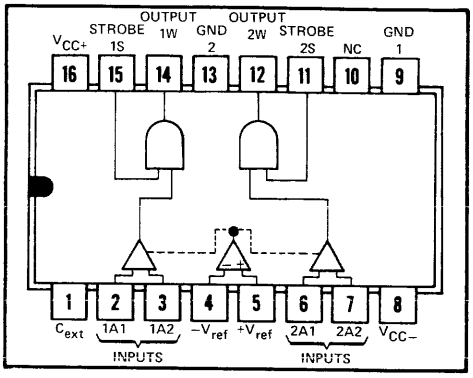
‡–All values shown in the table are based on:
High-level conditions: V_{CC} = 5 V, $V_{OH\ min}$ = 2.4 V
Low-level conditions: V_{CC} = 5 V, $V_{OL\ max}$ = 0.4 V
X–Not recommended or not possible.
§–The theoretical value is ∞. See explanation in text.

CIRCUIT TYPES SN7524, SN7525
DUAL SENSE AMPLIFIERS

TRUTH TABLE

INPUTS		OUTPUT
A	S	W
H	H	H
L	X	L
X	L	L

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: W = AS

NC—No internal connection

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_{T\ max}$	$V_{ID} \leq V_{T\ min}$	Irrelevant
S	$V_I \geq V_{IH\ min}$	$V_I \leq V_{IL\ max}$	Irrelevant

3

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

electrical characteristics (unless otherwise noted V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage (see Note 3, page 17)	12	V_{ref} = 15 mV	SN7524	11	15	19	mV
				SN7525	8	15	22	
			V_{ref} = 40 mV	SN7524	36	40	44	
				SN7525	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-Mode Input Pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns			±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	13			2			V
V_{IL}	Low-level input voltage (strobe inputs)	13					0.8	V
V_{OH}	High-level output voltage	13	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4		V
V_{OL}	Low-level output voltage	13	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	14	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1	mA
I_{IL}	Low-level input current (strobe inputs)	14	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1	−1.6	mA
I_{OS}	Short-circuit output current	15	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geqslant$ 100 pF, T_A = 25°C

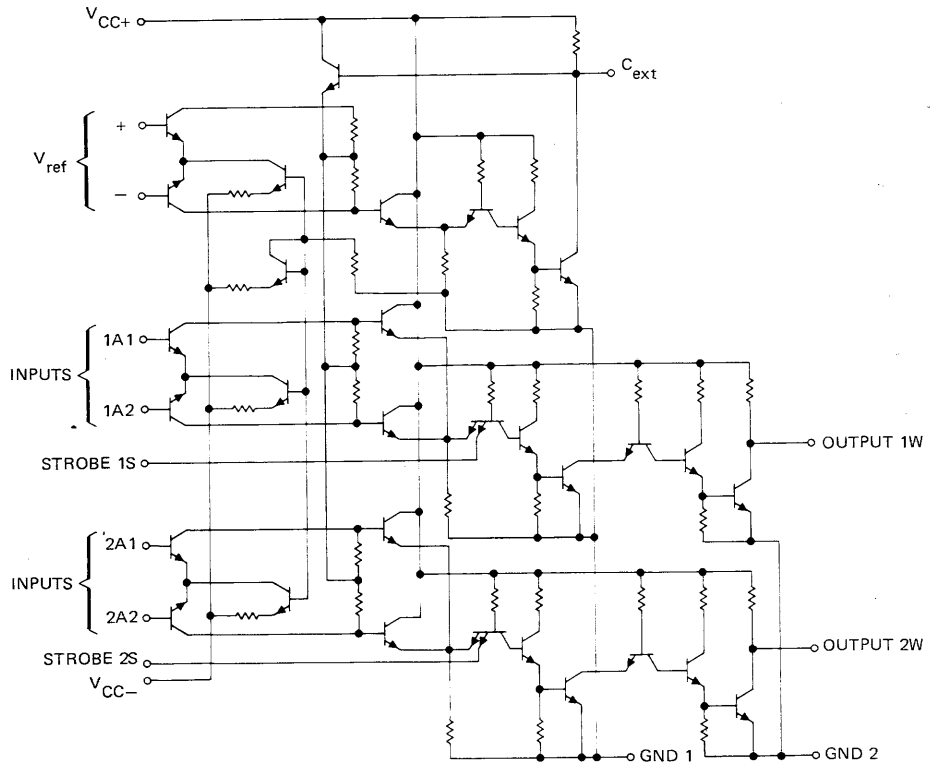
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	37	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(D)}$						20		
$t_{PLH(S)}$	STROBE	W	37	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(S)}$						20		

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geqslant$ 100 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic



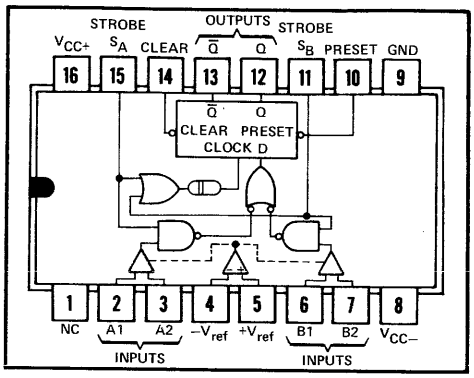
CIRCUIT TYPES SN7526, SN7527
DUAL-CHANNEL SENSE AMPLIFIERS WITH OUTPUT DATA REGISTERS

TRUTH TABLE

INPUTS AT TIME OF STROBE TRANSITION				OUTPUTS	
A	B	S_A	S_B	Q	$\overline{Q}$
H	X	↑	L	H	L
H	X	↑	↑	H	L
X	H	L	↑	H	L
X	H	↑	↑	H	L
L	L	↑	↑	L	H
L	X	↑	L	L	H
X	L	L	↑	L	H
X	X	H	↑	No Change	
X	X	↑	H	No Change	

NOTES: A. H = high level (steady state), L = low level (steady state), ↑ = transition from low level to high level, X = irrelevant.
B. Information at the inputs is transferred to the outputs on the positive-going edge of the strobe pulse.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to high level.
Low input to clear resets Q to low level.
Preset and clear dominate all other inputs.

NC—No internal connection

definition of logic levels

INPUT	H	L
A or B†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min
S_A or S_B	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max

†A and B are differential voltages (V_{ID}) between A1 and A2 or B1 and B2, respectively. For these circuits, V_{ID} is considered positive regardless of which terminal of each pair is positive with respect to the other.

recommended operating conditions¶

	MIN	MAX	UNIT
Width of clear or preset pulse, t_w	30		ns
Width of strobe pulse, t_w	30		ns
Input setup time, t_{setup}◇	20		ns
Input hold time, t_{hold}□	5		ns

electrical characteristics (unless otherwise noted V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 0°C to 70°C)

PARAMETER			TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential input threshold voltage (see Note 3, page 17)		16	V_{ref} = 15 mV	SN7526	11	15	19	mV
					SN7527	8	15	22	
				V_{ref} = 40 mV	SN7526	36	40	44	
					SN7527	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)		none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-Mode Input Pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns			±2.5		V
I_{IB}	Differential input bias current		2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential input offset current		2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage at strobe, preset, and clear inputs		17			2			V
V_{IL}	Low-level input voltage at strobe, preset, and clear inputs		17					0.8	V
V_{OH}	High-level output voltage		17	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	3.6		V
V_{OL}	Low-level output voltage		17	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.26	0.4	V
I_{IH}	High-level input current	clear and strobe inputs	19	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				80	μA
		preset input						120	
		clear and strobe inputs	19	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				2	mA
		preset input						3	
I_{IL}	Low-level input current	clear and strobe inputs	19	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−2	−3.2	mA
		preset input					−3	−4.8	
I_{OS}	Short-circuit output current§		18	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−18		−57	mA
I_{CC+}	Supply current from V_{CC+}		6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			27	40	mA
I_{CC-}	Supply current from V_{CC-}		6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−10	−20	mA

¶These are in addition to the conditions on Page 5. See waveforms in Figure 30.
◇Setup time is the interval immediately preceding the positive-going edge of the strobe pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
□Hold time is the interval immediately following the positive-going edge of the strobe pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.
‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

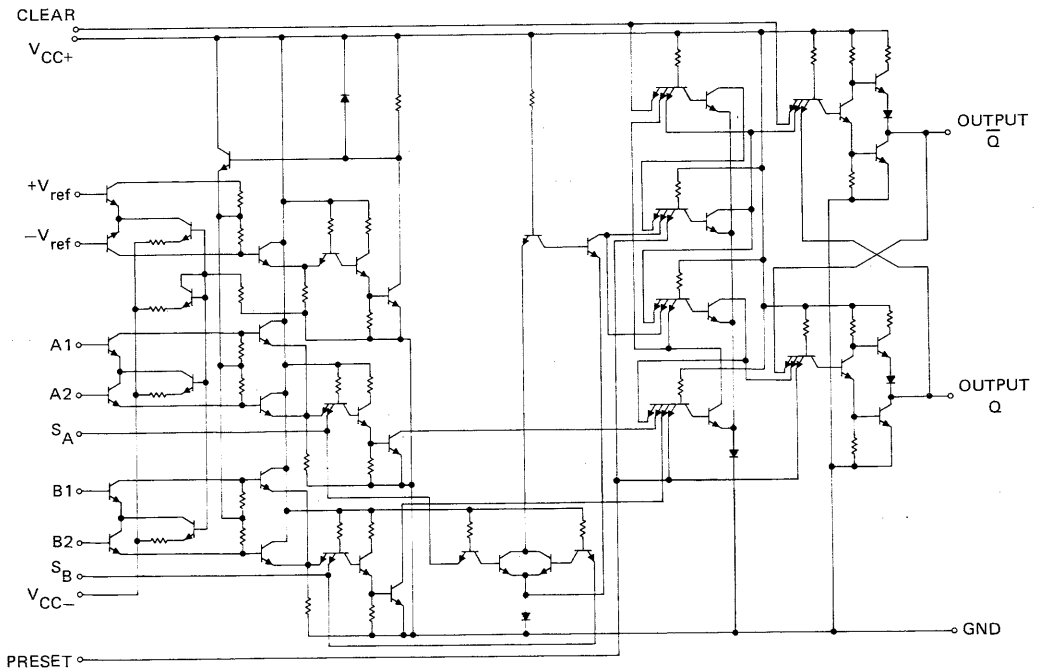
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(SQ)}$	STROBE S_A or S_B	Q	38	C_L = 15 pF, R_L = 288 Ω		25	45	ns
$t_{PHL(SQ)}$						30	45	
$t_{PLH(S\overline{Q})}$	STROBE S_A or S_B	$\overline{Q}$	38	C_L = 15 pF, R_L = 288 Ω		25	45	ns
$t_{PHL(S\overline{Q})}$						30	45	
$t_{PLH(CQ)}$	CLEAR	$\overline{Q}$	38	C_L = 15 pF, R_L = 288 Ω		15	25	ns
$t_{PHL(CQ)}$		Q				20	40	
$t_{PLH(PQ)}$	PRESET	Q	38	C_L = 15 pF, R_L = 288 Ω		15	25	ns
$t_{PHL(P\overline{Q})}$		$\overline{Q}$				20	40	

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic

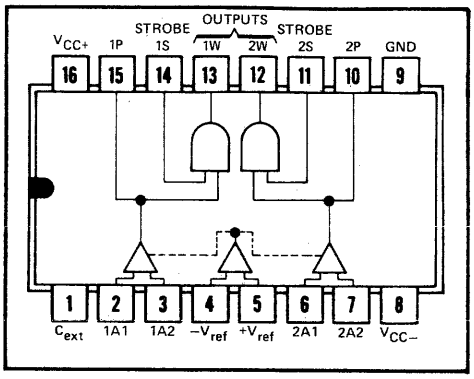


CIRCUIT TYPES SN7528, SN7529
DUAL SENSE AMPLIFIERS WITH PREAMPLIFIER TEST POINTS

TRUTH TABLE

INPUTS		OUTPUT
A	S	W
H	H	H
L	X	L
X	L	L

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: W = AS

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

3

electrical characteristics (unless otherwise noted V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage (see Note 3, page 17)	20	V_{ref} = 15 mV	SN7528	11	15	19	mV
				SN7529	8	15	22	
			V_{ref} = 40 mV	SN7528	36	40	44	
				SN7529	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-Mode Input Pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns			±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	21			2			V
V_{IL}	Low-level input voltage (strobe inputs)	21					0.8	V
V_{OH}	High-level output voltage	21	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4		V
V_{OL}	Low-level output voltage	21	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	22	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1	mA
I_{IL}	Low-level input current (strobe inputs)	22	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1	−1.6	mA
I_{OS}	Short-circuit output current	23	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	39	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(D)}$						20		ns
$t_{PLH(S)}$	STROBE	W	39	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(S)}$						20		ns

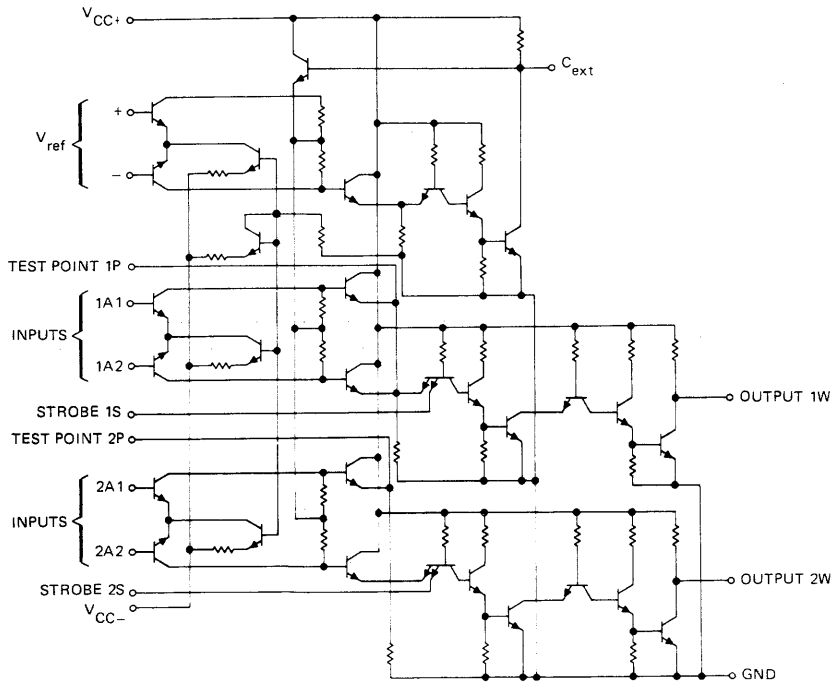
typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, t_f = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 3. The differential-input threshold voltage (V_T) is defined as the d-c differential-input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.

4. Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common-mode input signal is applied with a strobe-enable present.
5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic

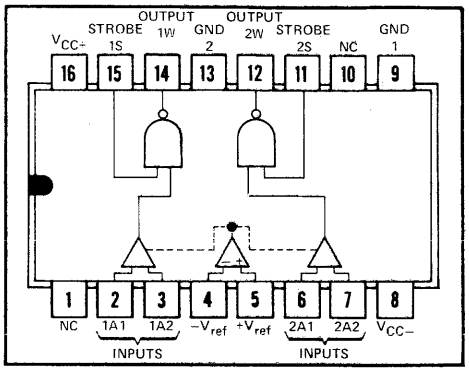


CIRCUIT TYPES SN75234, SN75235
DUAL SENSE AMPLIFIERS

TRUTH TABLE

INPUTS		OUTPUT
A	S	W
H	H	L
L	X	H
X	L	H

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $W = \overline{AS}$

NC—No internal connection

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_{T\ max}$	$V_{ID} \leq V_{T\ min}$	Irrelevant
S	$V_I \geq V_{IH\ min}$	$V_I \leq V_{IL\ max}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

3

electrical characteristics (unless otherwise noted $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 0°C$ to $70°C$)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage (see Note 3, page 17)	24	V_{ref} = 15 mV	SN75234	11	15	19	mV
				SN75235	8	15	22	
			V_{ref} = 40 mV	SN75234	36	40	44	
				SN75235	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-Mode Input Pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, $t_w = 50$ ns			±2.5		V
I_{IB}	Differential-input bias current	2	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{ID} = 0$			30	75	μA
I_{IO}	Differential-input offset current	2	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{ID} = 0$			0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	25			2			V
V_{IL}	Low-level input voltage (strobe inputs)	25					0.8	V
V_{OH}	High-level output voltage	25	$V_{CC+} = 4.75$ V, $V_{CC-} = -4.75$ V, $I_{OH} = -400$ μA		2.4	4		V
V_{OL}	Low-level output voltage	25	$V_{CC+} = 4.75$ V, $V_{CC-} = -4.75$ V, $I_{OL} = 16$ mA			0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	26	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IH} = 2.4$ V				40	μA
			$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IH} = 5.25$ V				1	mA
I_{IL}	Low-level input current (strobe inputs)	26	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IL} = 0.4$ V			−1	−1.6	mA
I_{OS}	Short-circuit output current	27	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $T_A = 25°C$			25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $T_A = 25°C$			−15	−20	mA

‡All typical values are at $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 25°C$.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics, V_{CC+} = 5 V, V_{CC-} = –5 V, T_A = 25°C

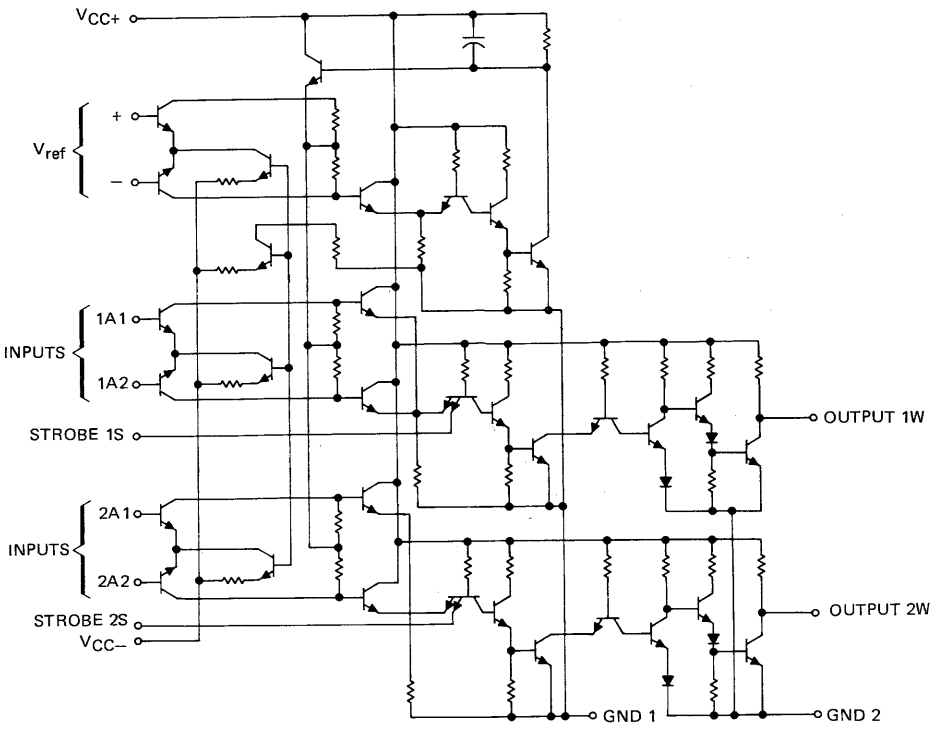
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	40	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(D)}$						25	40	
$t_{PLH(S)}$	STROBE	W	40	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(S)}$						15	30	

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = –5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic

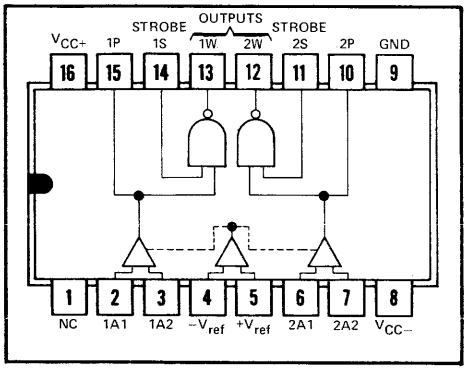


CIRCUIT TYPES SN75238, SN75239
DUAL SENSE AMPLIFIERS WITH PREAMPLIFIER TEST POINTS

TRUTH TABLE

INPUTS		OUTPUT
A	S	W
H	H	L
L	X	H
X	L	H

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $W = \overline{AS}$

NC—No internal connection

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

3

electrical characteristics (unless otherwise noted $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A =$ 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage (see Note 3, page 17)	28	V_{ref} = 15 mV	SN75238	11	15	19	mV
				SN75239	8	15	22	
			V_{ref} = 40 mV	SN75238	36	40	44	
				SN75239	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-Mode Input Pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, $t_w = 50$ ns			±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	29			2			V
V_{IL}	Low-level input voltage (strobe inputs)	29					0.8	V
V_{OH}	High-level output voltage	29	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4		V
V_{OL}	Low-level output voltage	29	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	30	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1	mA
I_{IL}	Low-level input current (strobe inputs)	30	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1	−1.6	mA
I_{OS}	Short-circuit output current	31	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics, V_{CC+} = 5 V, V_{CC-} = –5 V, T_A = 25°C

PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	41	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(D)}$						25	40	ns
$t_{PLH(S)}$	STROBE	W	41	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(S)}$						15	30	ns

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = –5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, t_f = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

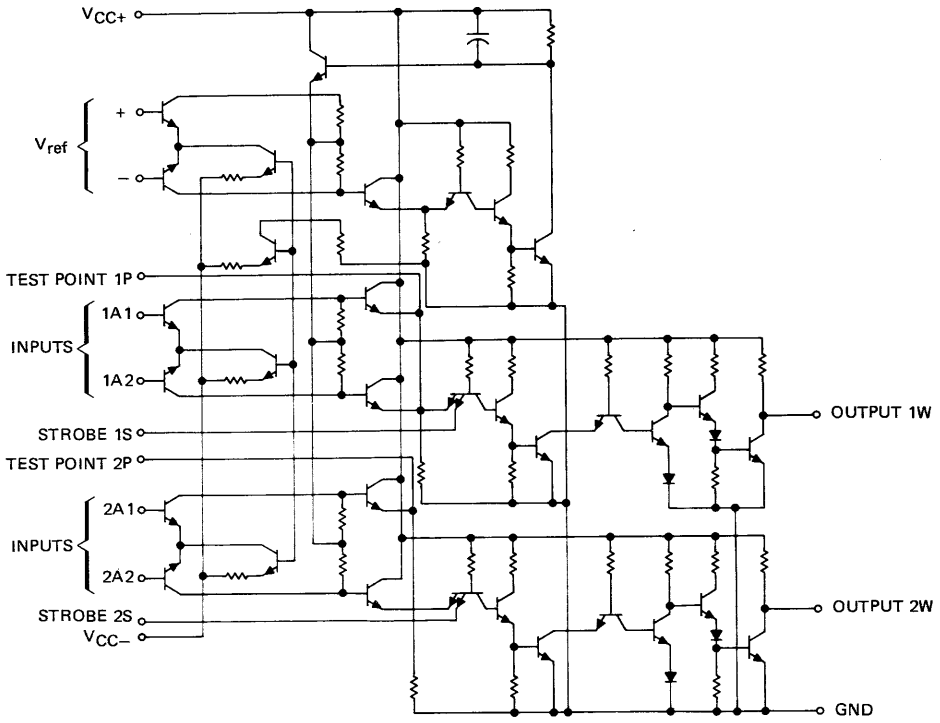
NOTES: 3. The differential-input threshold voltage (V_T) is defined as the d-c differential-input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.

4. Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common-mode input signal is applied with a strobe-enable present.

5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input overload signal prior to the strobe-enable signal.

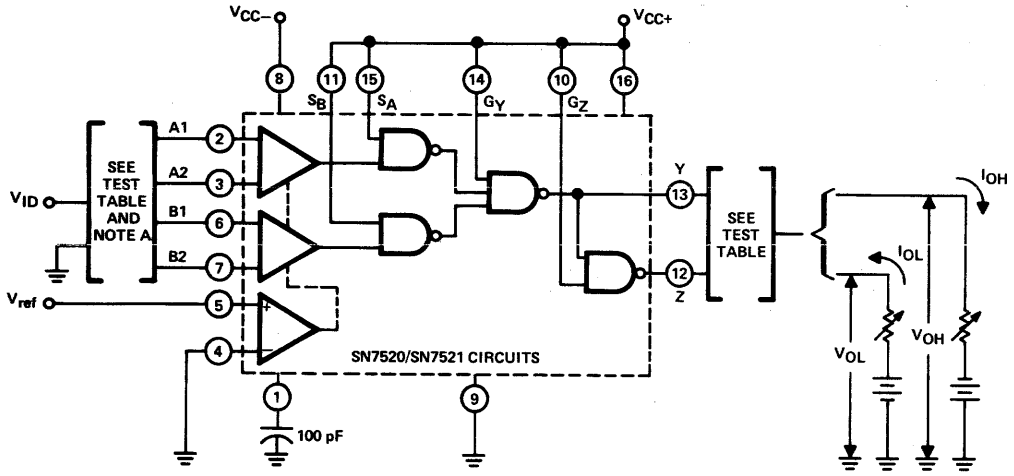
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic



PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT Y			OUTPUT Z		
				V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
SN7520	A1-A2 or B1-B2	15 mV	≤11 mV	≤0.4 V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	≥19 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤36 mV	≤0.4 V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≥44 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA
SN7521	A1-A2 or B1-B2	15 mV	≤ 8 mV	≤0.4 V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	≥22 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤33 mV	≤0.4 V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≥47 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with the other pair grounded.

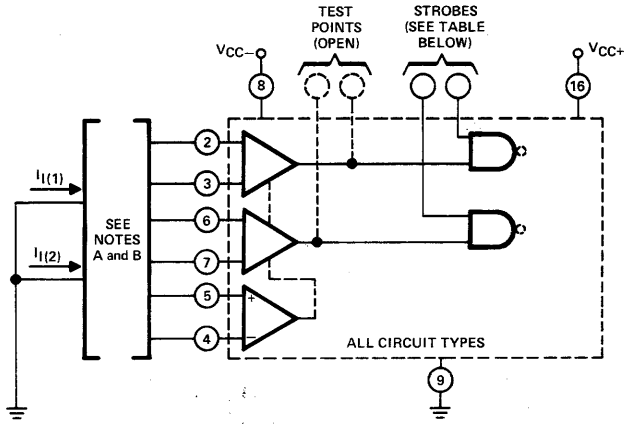
FIGURE 1–V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



NOTES: A. Each preamplifier is tested separately. Inputs not under test are grounded.
B. $I_{IB} = I_{I(1)}$ and/or $I_{I(2)}$; $I_{IO} = I_{I(1)} - I_{I(2)}$; $I_{I(1)}$ and $I_{I(2)}$ are the currents into the two inputs of the pair under test.

PIN CONNECTIONS (OTHER THAN THOSE SHOWN ABOVE)

CIRCUIT TYPES	100 pF to GND	APPLY V_{CC+}	APPLY GND	LEAVE OPEN	OTHER
SN7520, SN7521	C_{ext} (1)	G_Y, G_Z, S_A, S_B (14) (10) (15) (11)		Y, Z (13) (12)	
SN7522, SN7523	C_{ext} (1)	G, S_A, S_B (14) (15) (11)	GND 2 (13)		R_L, Y (10) (12)
SN7524, SN7525	C_{ext} (1)	1S, 2S (15) (11)	GND 2 (13)	1W, 2W (14) (12)	
SN7526, SN7527		PRESET, CLEAR, S_A, S_B (10) (14) (15) (11)		Q, $\bar{Q}$ (12) (13)	
SN7528, SN7529	C_{ext} (1)	1S, 2S (14) (11)		1P, 2P, 1W, 2W (15) (10) (13) (12)	
SN75234, SN75235		1S, 2S (15) (11)	GND 2 (13)	1W, 2W (14) (12)	
SN75238, SN75239		1S, 2S (14) (11)		1P, 2P, 1W, 2W (15) (10) (13) (12)	

FIGURE 2–I_{IB}, I_{IO}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

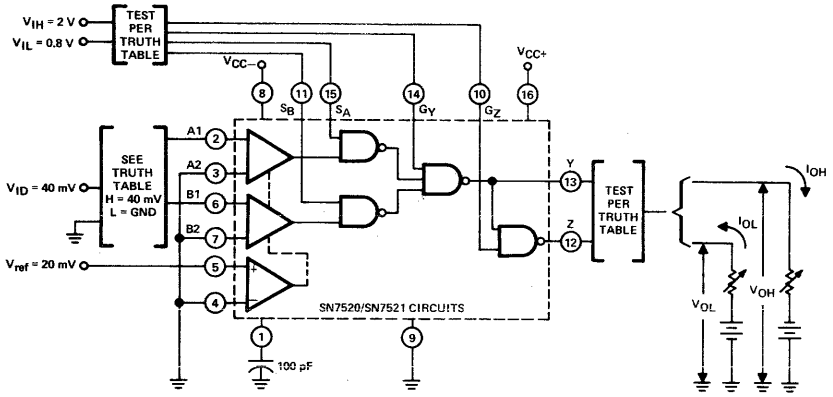
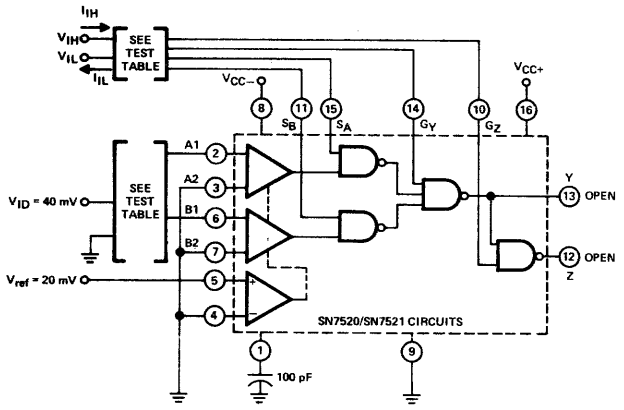


FIGURE 3–V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

TEST	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	GATE G_Y	GATE G_Z
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	V_{IL}	V_{IL}
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	V_{IL}	V_{IL}
I_{IH} at GATE G_Y	V_{ID}	V_{ID}	V_{IH}	V_{IH}	V_{IH}	V_{IL}
I_{IH} at GATE G_Z	GND	GND	V_{IL}	V_{IL}	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Y	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Z	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}

FIGURE 4–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

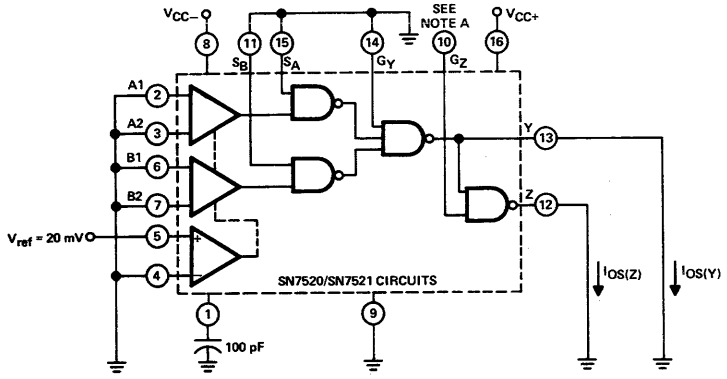
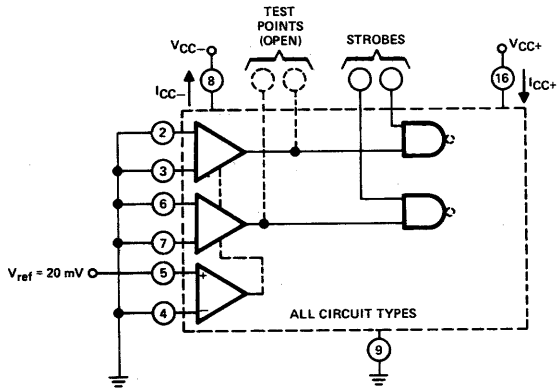


FIGURE 5–I_{OS}

NOTE A: When testing $I_{OS(Y)}$, Pin 10 is open; when testing $I_{OS(Z)}$, Pin 10 is grounded.



PIN CONNECTIONS (OTHER THAN THOSE SHOWN ABOVE)

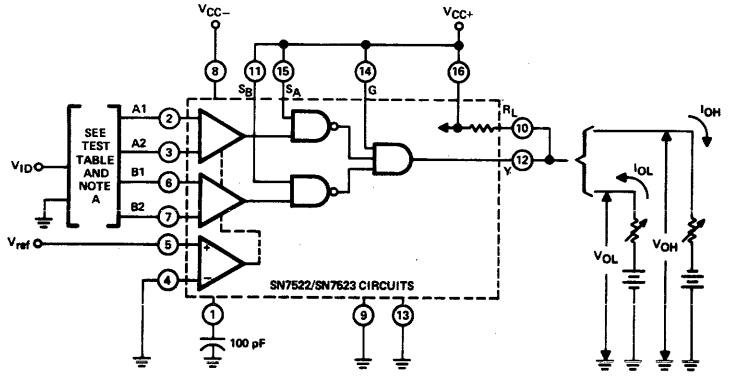
CIRCUIT TYPES	100 pF to GND	APPLY GND	LEAVE OPEN
SN7520, SN7521	C_{ext} (1)	G_Y, G_Z, S_A, S_B (14)(10)(15)(11)	Y, Z (13)(12)
SN7522, SN7523	C_{ext} (1)	G, S_A, S_B, GND 2 (14)(15)(11)(13)	R_L, Y (10)(12)
SN7524, SN7525	C_{ext} (1)	1S, 2S, GND 2 (15)(11)(13)	1W, 2W (14)(12)
SN7526, SN7527		S_A, S_B (15)(11)	PRESET, CLEAR, Q, $\overline{Q}$ (10)(14)(12)(13)
SN7528, SN7529	C_{ext} (1)	1S, 2S (14)(11)	1P, 2P, 1W, 2W (15)(10)(13)(12)
SN75234, SN75235		1S, 2S, GND 2 (15)(11)(13)	1W, 2W (14)(12)
SN75238, SN75239		1S, 2S (14)(11)	1P, 2P, 1W, 2W (15)(10)(13)(12)

FIGURE 6–I_{CC+}, I_{CC-}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN7522	A1-A2 or B1-B2	15 mV	≤11 mV	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	≥19 mV	≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤36 mV	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≥44 mV	≤0.4 V		16 mA
SN7523	A1-A2 or B1-B2	15 mV	≤ 8 mV	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	≥22 mV	≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤33 mV	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≥47 mV	≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with the other pair grounded.

FIGURE 7–V_T

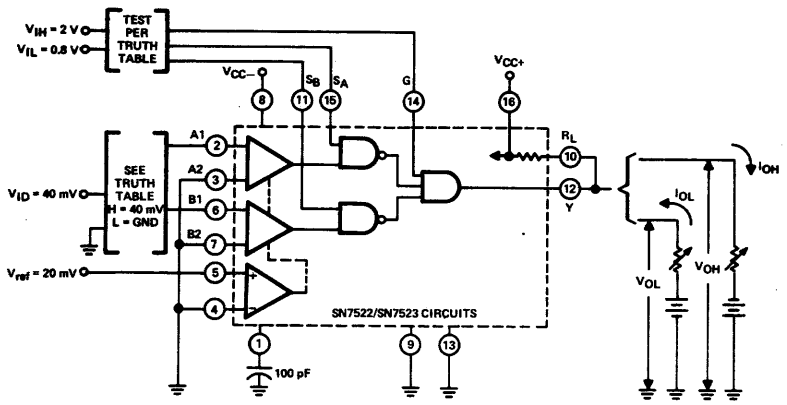


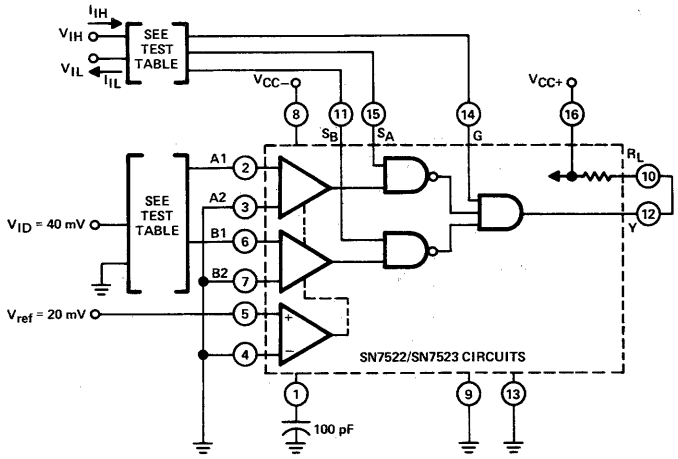
FIGURE 8–V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	GATE G
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	V_{IH}
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	V_{IH}
I_{IH} at GATE	V_{ID}	V_{ID}	V_{IH}	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IL}	V_{IH}
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IL}	V_{IL}	V_{IH}
I_{IL} at GATE	GND	GND	V_{IL}	V_{IL}	V_{IL}

FIGURE 9–I_{IH}, I_{IL}

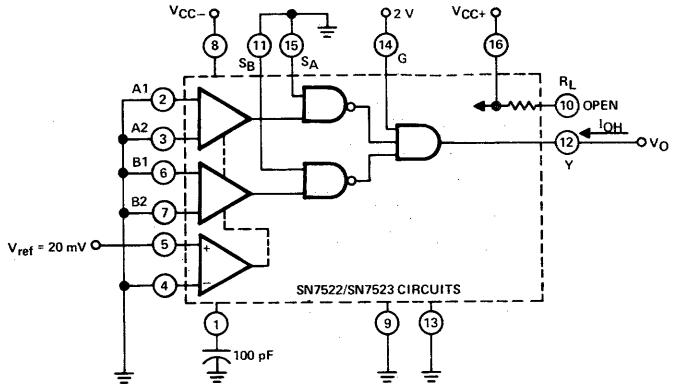


FIGURE 10–I_{OH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

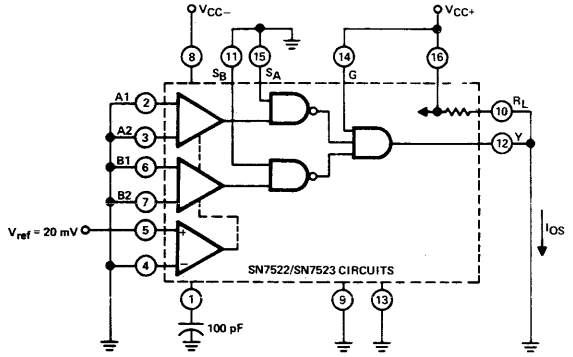
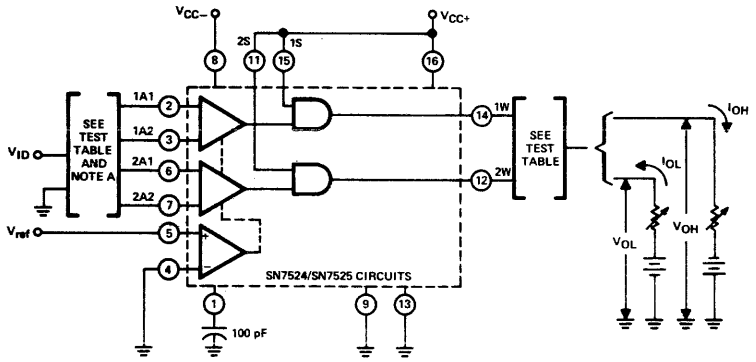


FIGURE 11–I_{OS}



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN7524	A1-A2	15 mV	≤11 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥19 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤36 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥44 mV	≥2.4 V	−400 μA	
SN7525	A1-A2	15 mV	≤ 8 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥22 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤33 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥47 mV	≥2.4 V	−400 μA	

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

FIGURE 12–V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

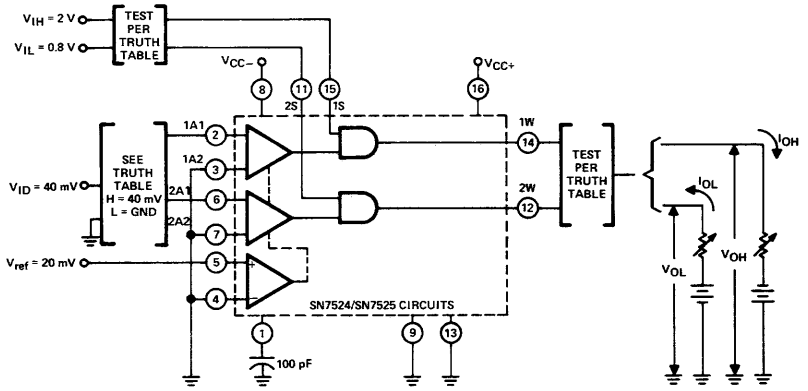
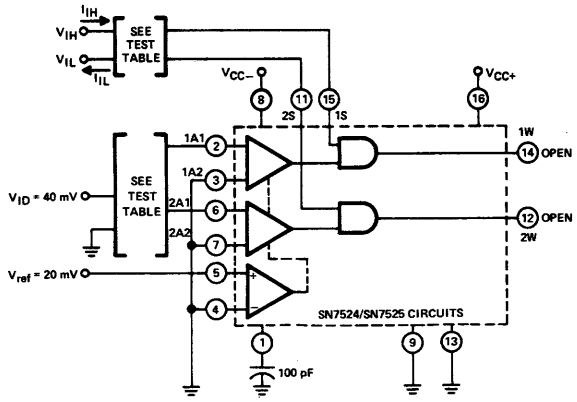


FIGURE 13–V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 14–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

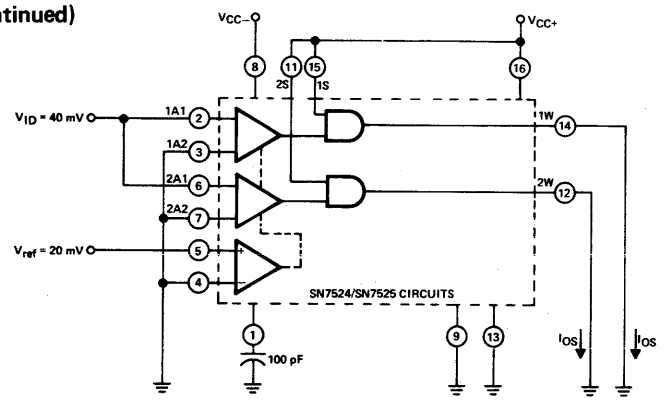
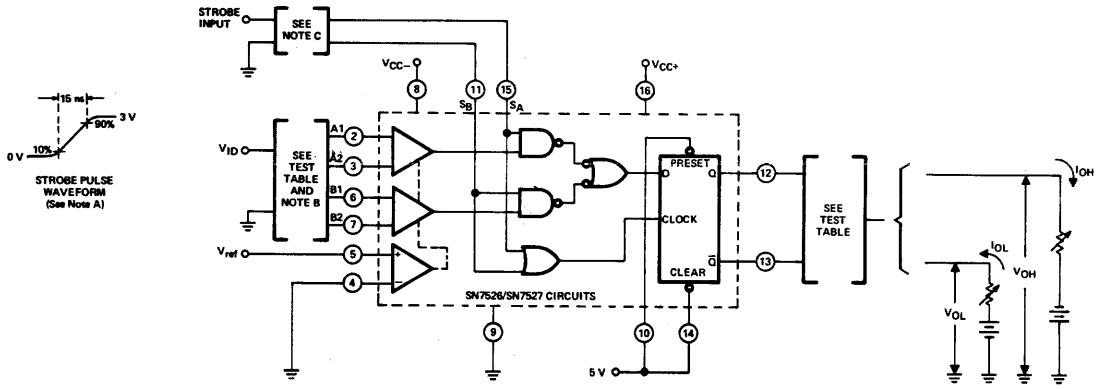


FIGURE 15–I_{OS}



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT Q			OUTPUT $\overline{Q}$		
				V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
SN7526	A1-A2 or B1-B2	15 mV	≤11 mV	≤0.4 V		16 mA	≥2.4 V		16 mA
	A1-A2 or B1-B2	15 mV	≥19 mV	≥2.4 V	−400 μA		≤0.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≤36 mV	≤0.4 V		16 mA	≥2.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≥44 mV	≥2.4 V	−400 μA		≤0.4 V	−400 μA	
SN7527	A1-A2 or B1-B2	15 mV	≤ 8 mV	≤0.4 V		16 mA	≥2.4 V		16 mA
	A1-A2 or B1-B2	15 mV	≥22 mV	≥2.4 V	−400 μA		≤0.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≤33 mV	≤0.4 V		16 mA	≥2.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≥47 mV	≥2.4 V	−400 μA		≤0.4 V	−400 μA	

NOTES: A. The strobe input pulse is supplied by a generator with the following characteristics: Z_O = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_w = 500 ns, PRR = 1 MHz.
B. Each pair of differential inputs is tested separately with the other pair grounded.
C. Strobe input pulse is applied to Strobe A when inputs A1-A2 are being tested and to Strobe B when inputs B1-B2 are being tested. In each case, the other strobe input is grounded.

FIGURE 16–V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

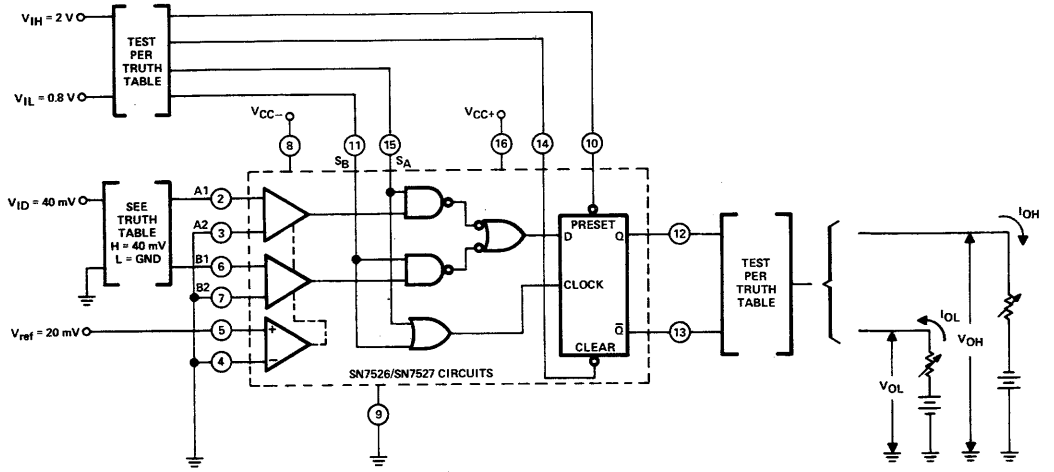
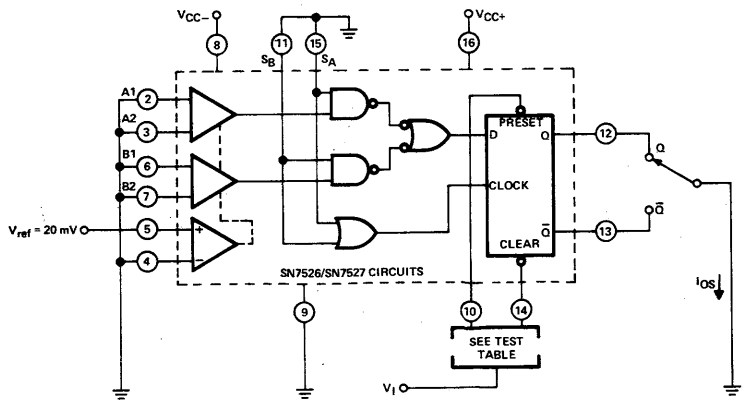


FIGURE 17–V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

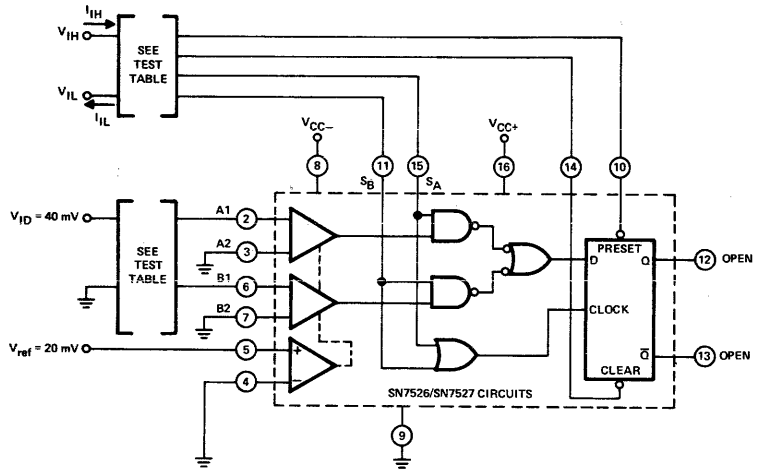
PARAMETER	PRESET	CLEAR
I_{OS} at OUTPUT Q	V_{IL}	V_{IH}
I_{OS} at OUTPUT $\bar{Q}$	V_{IH}	V_{IL}

FIGURE 18–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

PARAMETER	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	PRESET	CLEAR
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	OPEN	OPEN
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	OPEN	OPEN
I_{IH} at PRESET	GND	V_{ID}	V_{IL}	NOTE B	V_{IH}	V_{IH}
I_{IH} at CLEAR	GND	GND	V_{IL}	NOTE B	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IH}	OPEN	OPEN
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IH}	V_{IL}	OPEN	OPEN
I_{IL} at PRESET	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at PRESET	V_{ID}	GND	V_{IH}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at CLEAR	V_{ID}	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}

NOTES: A. Each input is tested separately.
B. Momentary ground, then V_{IH}.

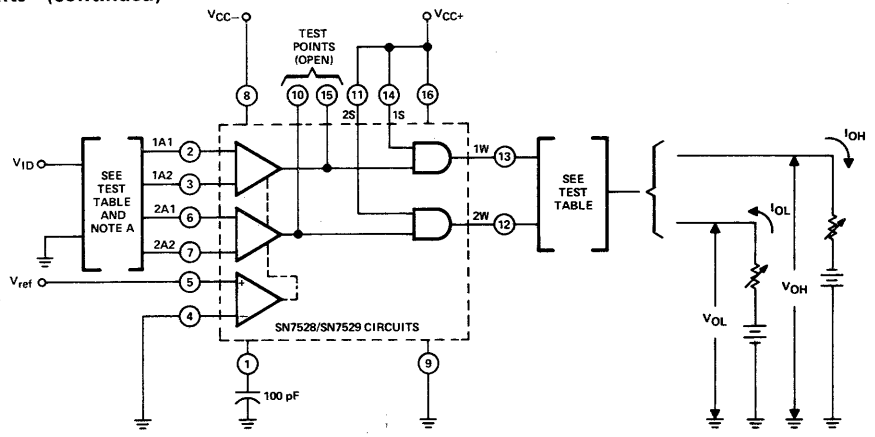
FIGURE 19–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN7528	A1-A2	15 mV	≤11 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥19 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤36 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥44 mV	≥2.4 V	−400 μA	
SN7529	A1-A2	15 mV	≤ 8 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥22 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤33 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥47 mV	≥2.4 V	−400 μA	

NOTE A: Each pair of inputs is tested separately with its corresponding output.

FIGURE 20–V_T

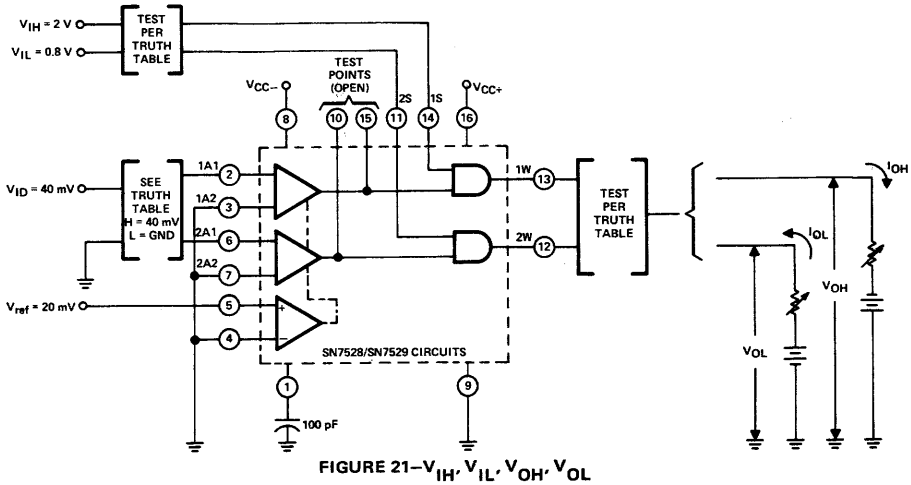
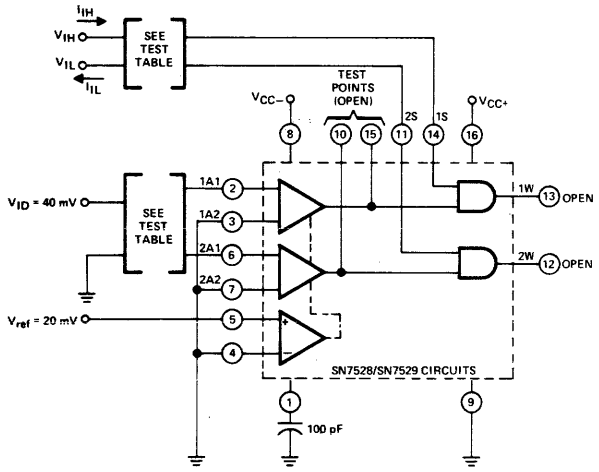


FIGURE 21–V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 22–I_{IH}, I_{IL}

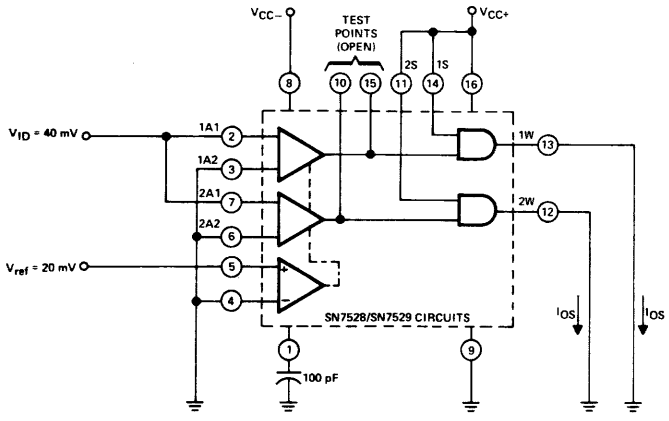


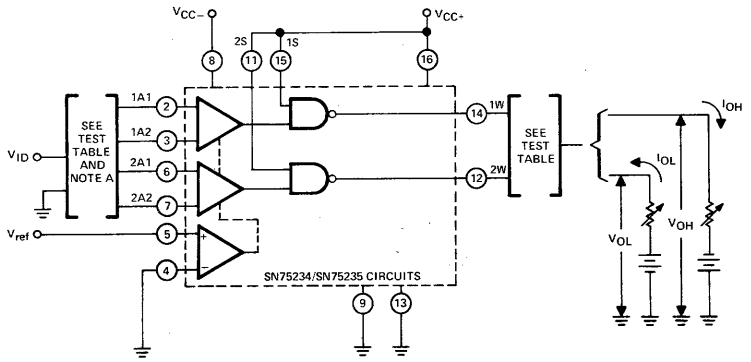
FIGURE 23–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN75234	A1-A2	15 mV	≤11 mV	≥2.4 V	−400 μA	
	A1-A2	15 mV	≥19 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≤36 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≥44 mV	≤0.4 V		16 mA
SN75235	A1-A2	15 mV	≤ 8 mV	≥2.4 V	−400 μA	
	A1-A2	15 mV	≥22 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≤33 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≥47 mV	≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

FIGURE 24–V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

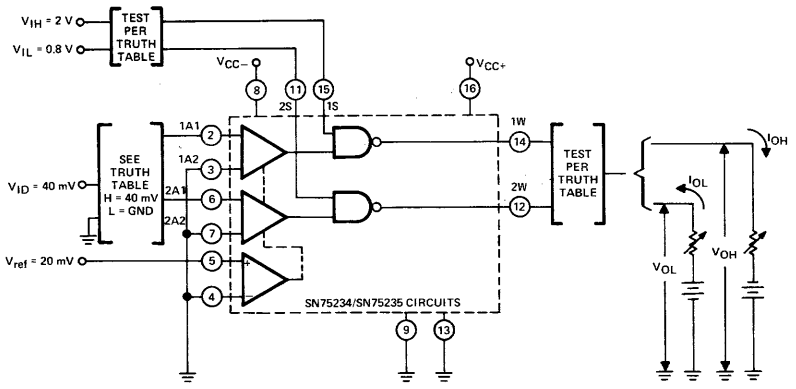
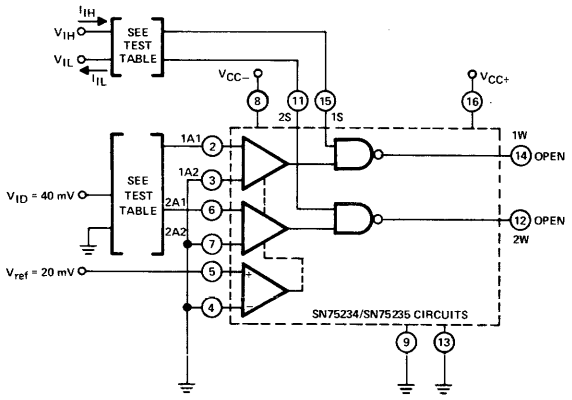


FIGURE 25–V_{IH}, V_{IL}, V_{OH}, V_{OL}

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 26–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

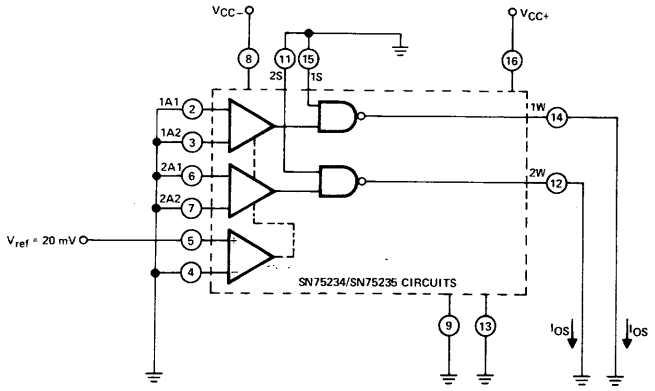
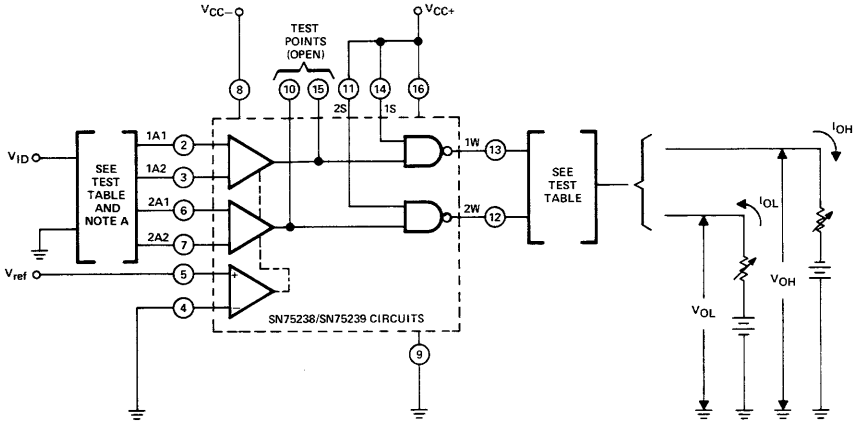


FIGURE 27–I_{OS}

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN75238	A1-A2	15 mV	⩽11 mV	⩾2.4 V	−400 μA	
	A1-A2	15 mV	⩾19 mV	⩽0.4 V		16 mA
	A1-A2	40 mV	⩽36 mV	⩾2.4 V	−400 μA	
	A1-A2	40 mV	⩾44 mV	⩽0.4 V		16 mA
SN75239	A1-A2	15 mV	⩽ 8 mV	⩾2.4 V	−400 μA	
	A1-A2	15 mV	⩾22 mV	⩽0.4 V		16 mA
	A1-A2	40 mV	⩽33 mV	⩾2.4 V	−400 μA	
	A1-A2	40 mV	⩾47 mV	⩽0.4 V		16 mA

NOTE A: Each pair of inputs is tested separately with its corresponding output.

FIGURE 28–V_T

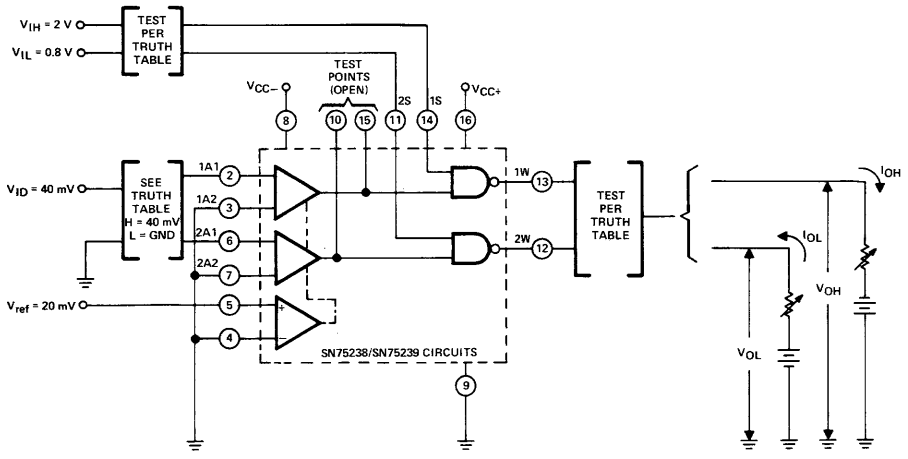
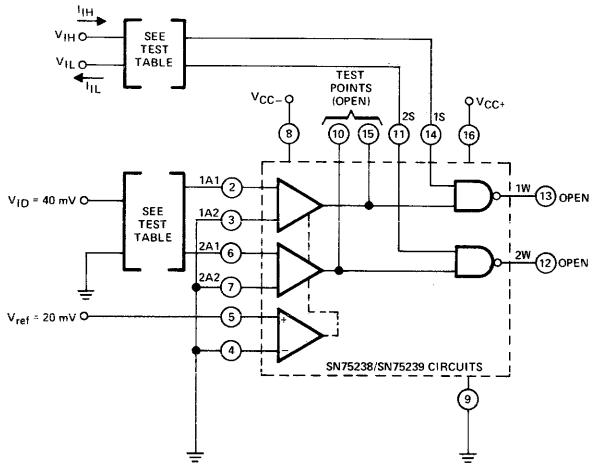


FIGURE 29–V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



3

TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 30–I_{IH}, I_{IL}

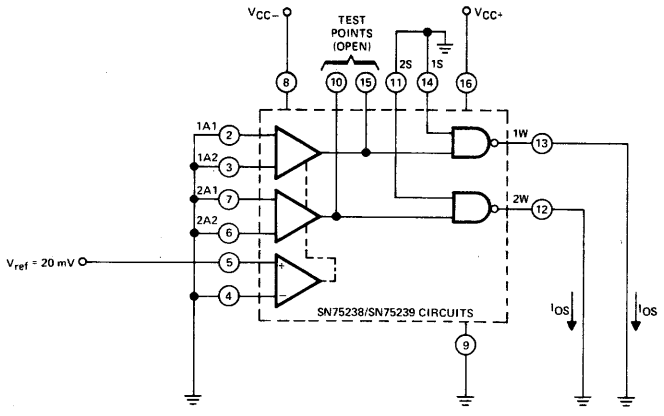


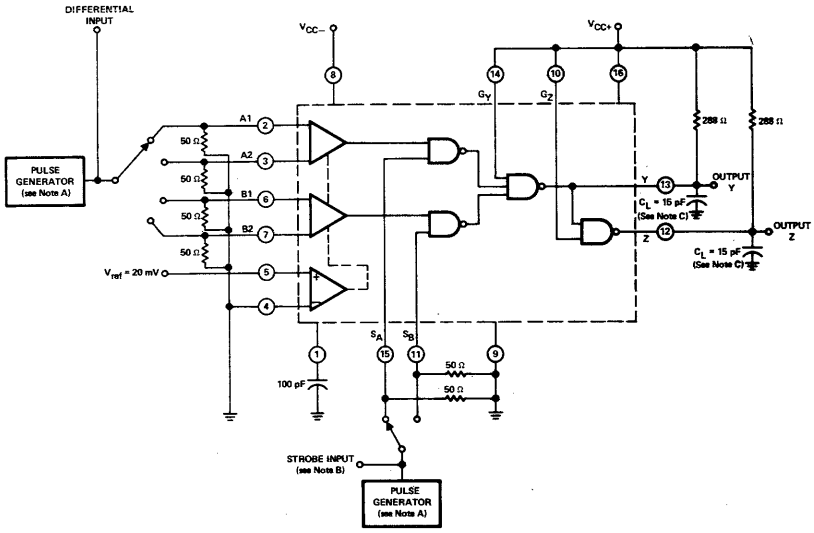
FIGURE 31–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

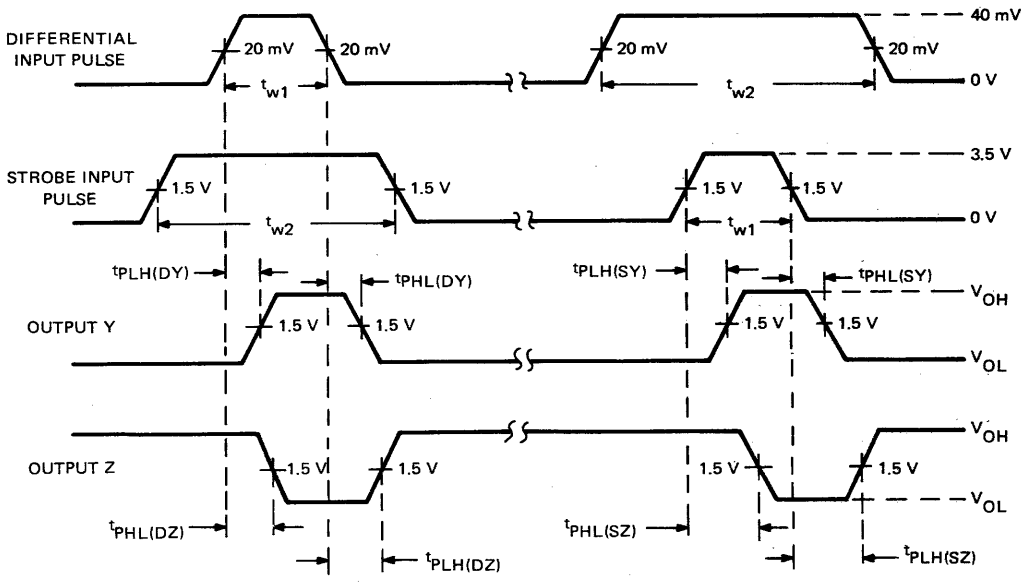
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

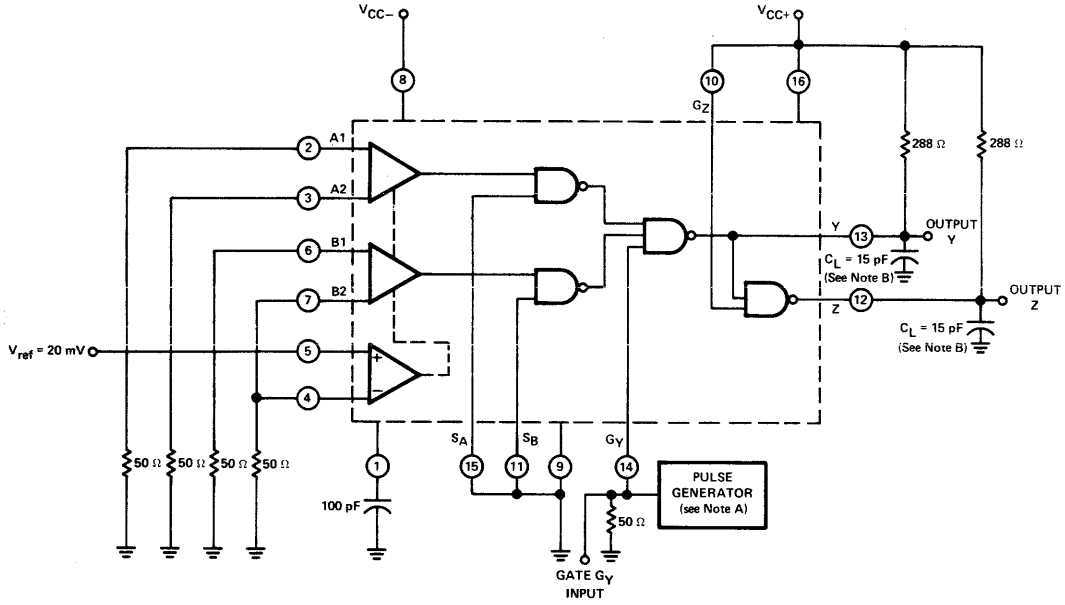
B. The strobe input pulse is applied to Strobe S_A when inputs A1-A2 are being tested and to Strobe S_B when inputs B1-B2 are being tested.

C. C_L includes probe and jig capacitance.

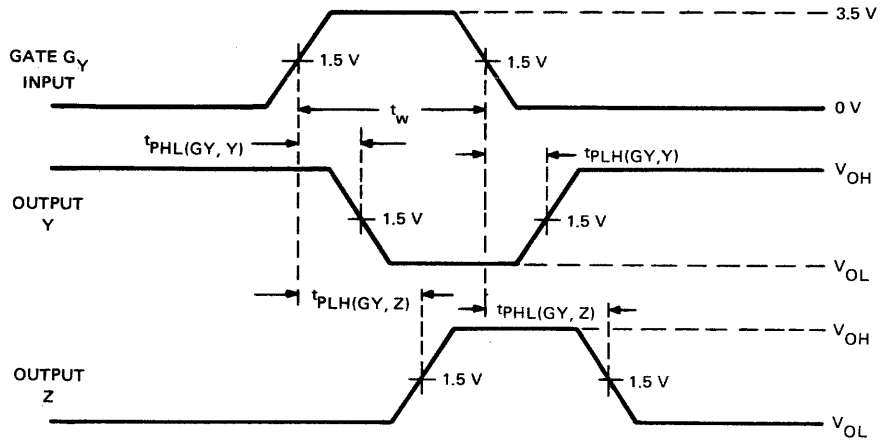
FIGURE 32–SN7520/SN7521 PROPAGATION DELAY TIMES FROM DIFFERENTIAL AND STROBE INPUTS

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

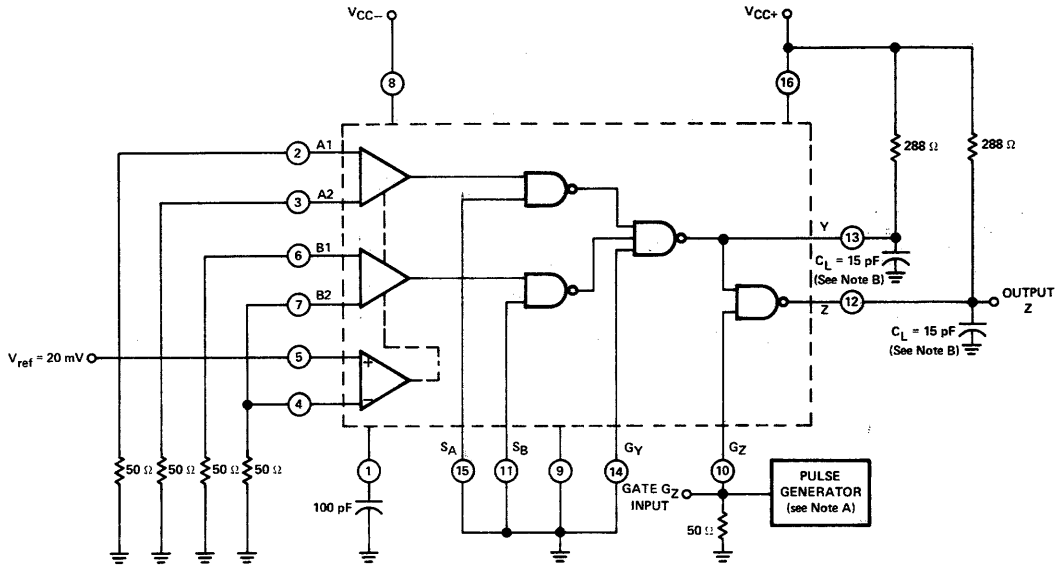
NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_w = 100 ns, and PRR = 1 MHz.
B. C_L includes probe and jig capacitance.

FIGURE 33–SN7520/SN7521 PROPAGATION DELAY TIMES FROM GATE GY

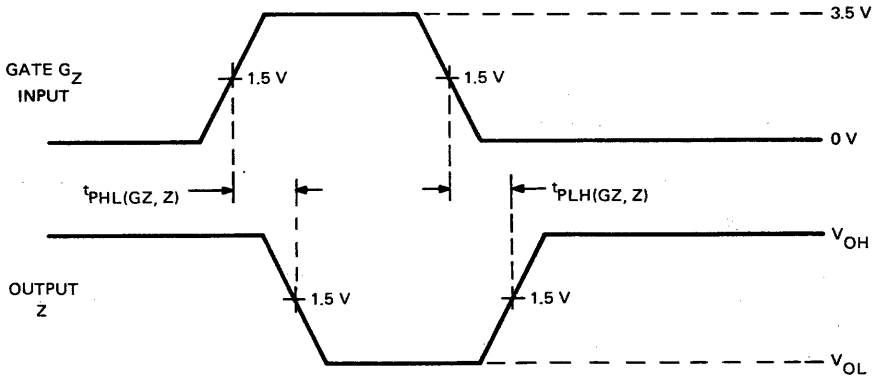
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



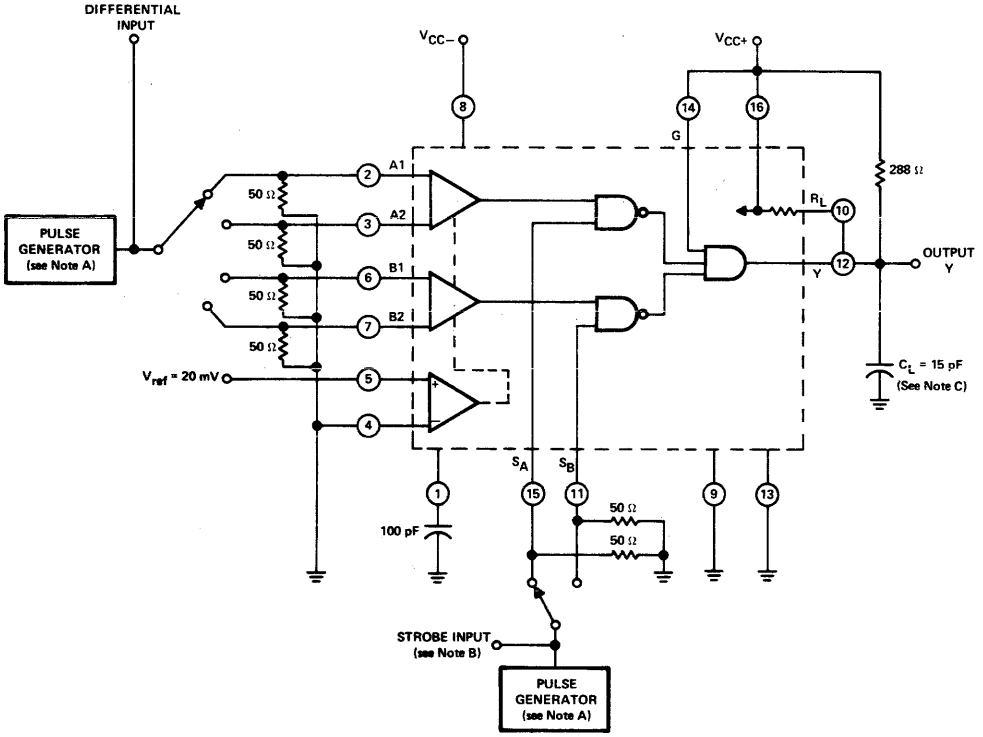
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_w = 100 ns, and PRR = 1 MHz.
B. C_L includes probe and jig capacitance.

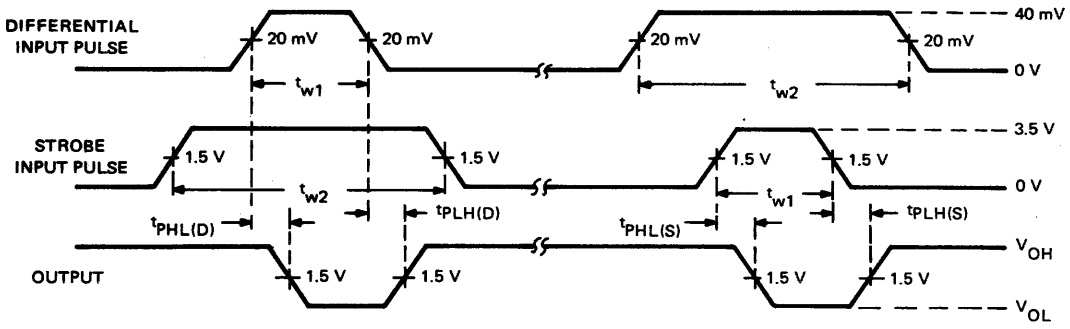
FIGURE 34–SN7520/SN7521 PROPAGATION DELAY TIMES FROM GATE G_Z

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

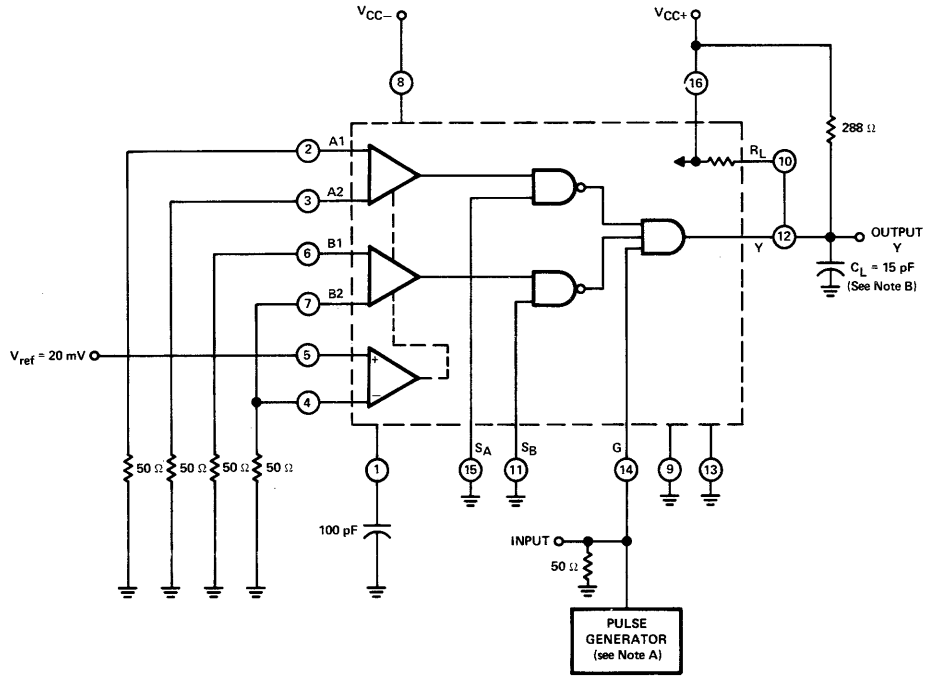
NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$, $t_r = t_f = 15 \pm 5$ ns, $t_{w1} = 100$ ns, $t_{w2} = 300$ ns, PRR = 1 MHz.
B. The strobe input pulse is applied to Strobe S_A when testing inputs A1-A2 and to Strobe S_B when testing inputs B1-B2.
C. C_L includes probe and jig capacitance.

FIGURE 35–SN7522/SN7523 PROPAGATION DELAY TIMES FROM DIFFERENTIAL AND STROBE INPUTS

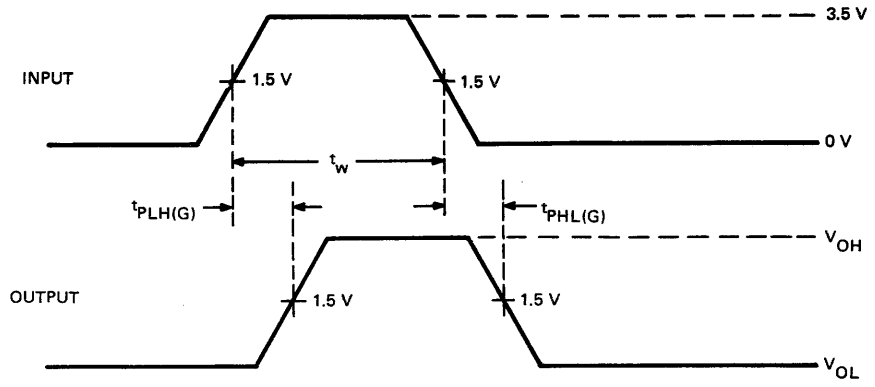
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

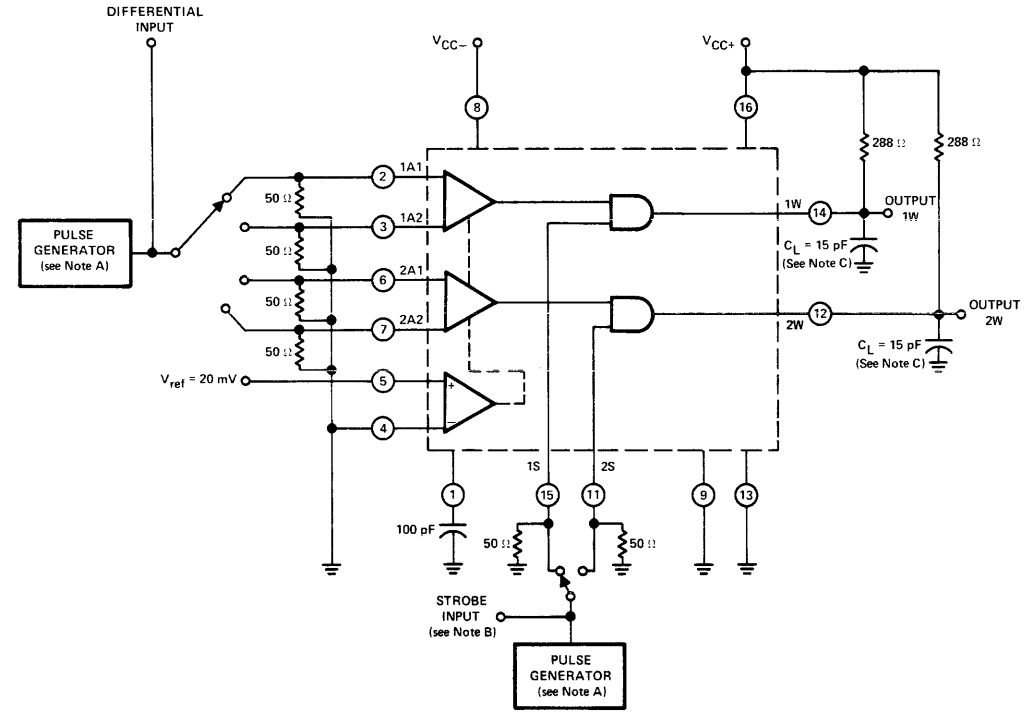
NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{p1} = 100 ns, t_{p2} = 300 ns, t_{p3} = 0.8 μs, PRR = 1 MHz.

B. C_L includes probe and jig capacitance.

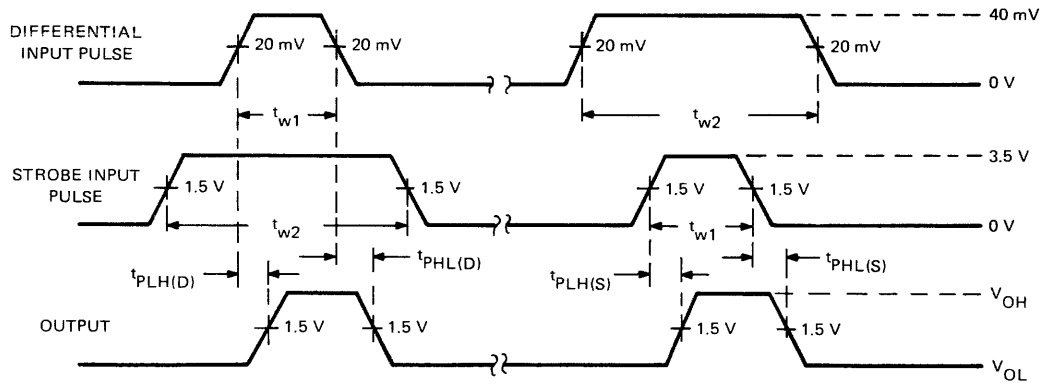
FIGURE 36–SN7522/SN7523 PROPAGATION DELAY TIMES FROM GATE INPUT

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2A2 are being tested.

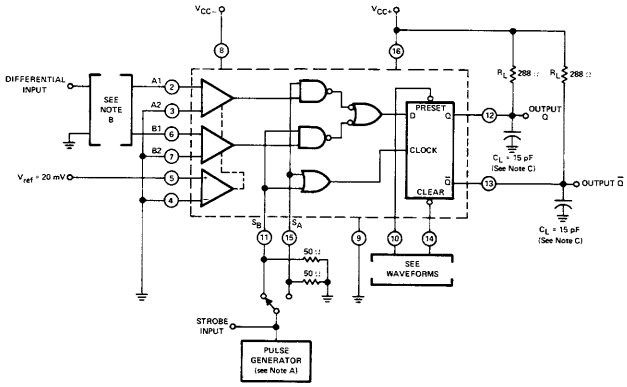
C. C_L includes probe and jig capacitance.

FIGURE 37—SN7524/SN7525 PROPAGATION DELAY TIMES

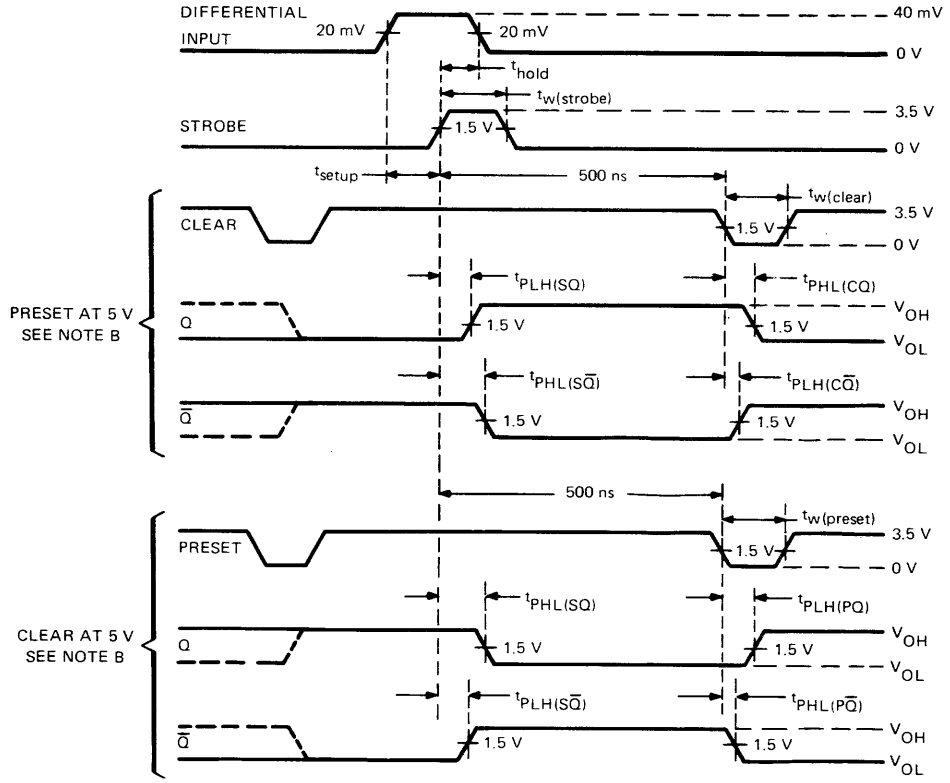
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



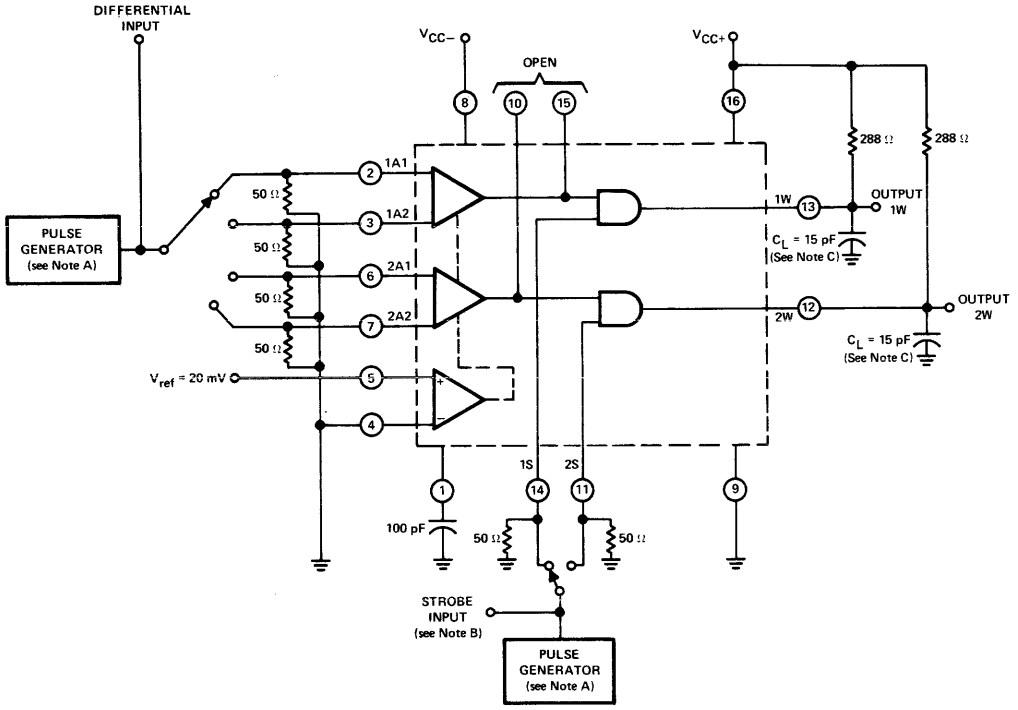
VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_w = 50 ns, and PRR = 1 MHz.
B. Each preamplifier is tested separately. Apply 40-mV pulse to input A1 when testing Strobe S_A and to B1 when testing Strobe S_B.
C. C_L includes probe and jig capacitance.

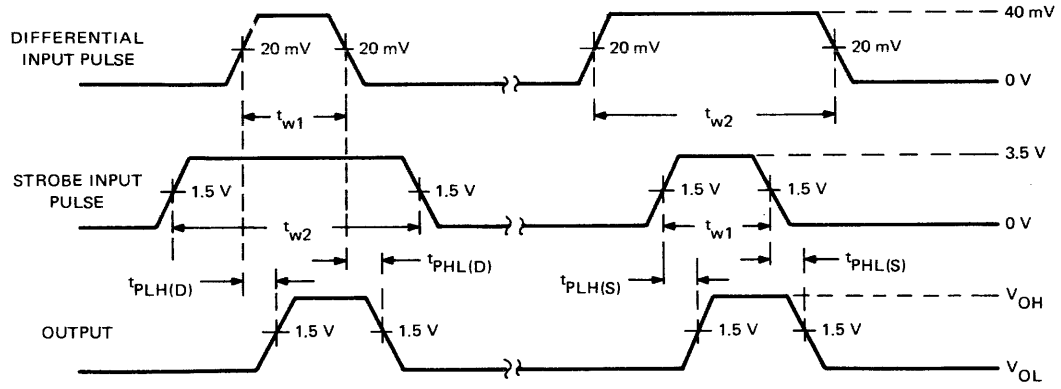
FIGURE 38–SN7526/SN7527 PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2S2 are being tested.

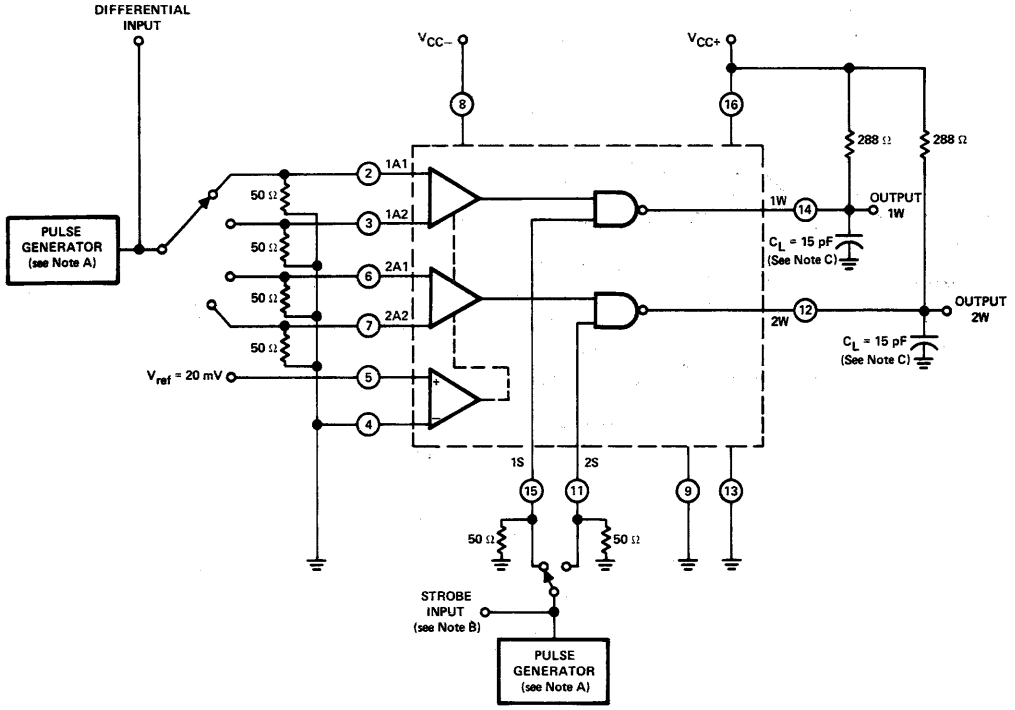
C. C_L includes probe and jig capacitance.

FIGURE 39—SN7528/SN7529 PROPAGATION DELAY TIMES

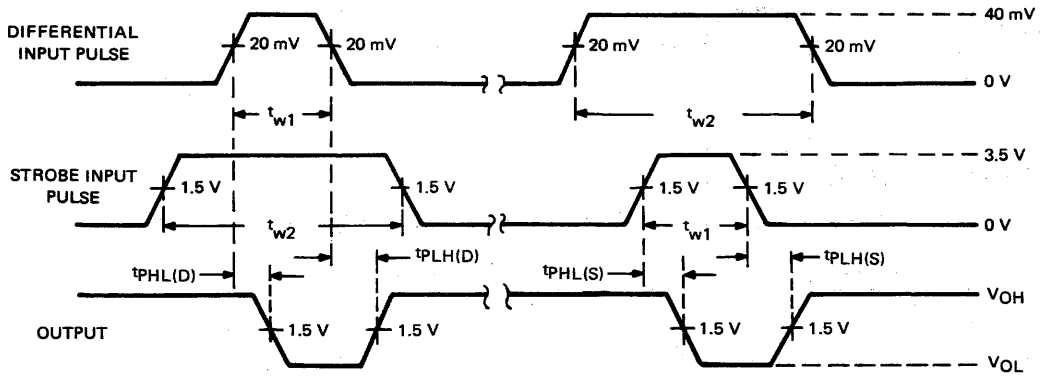
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

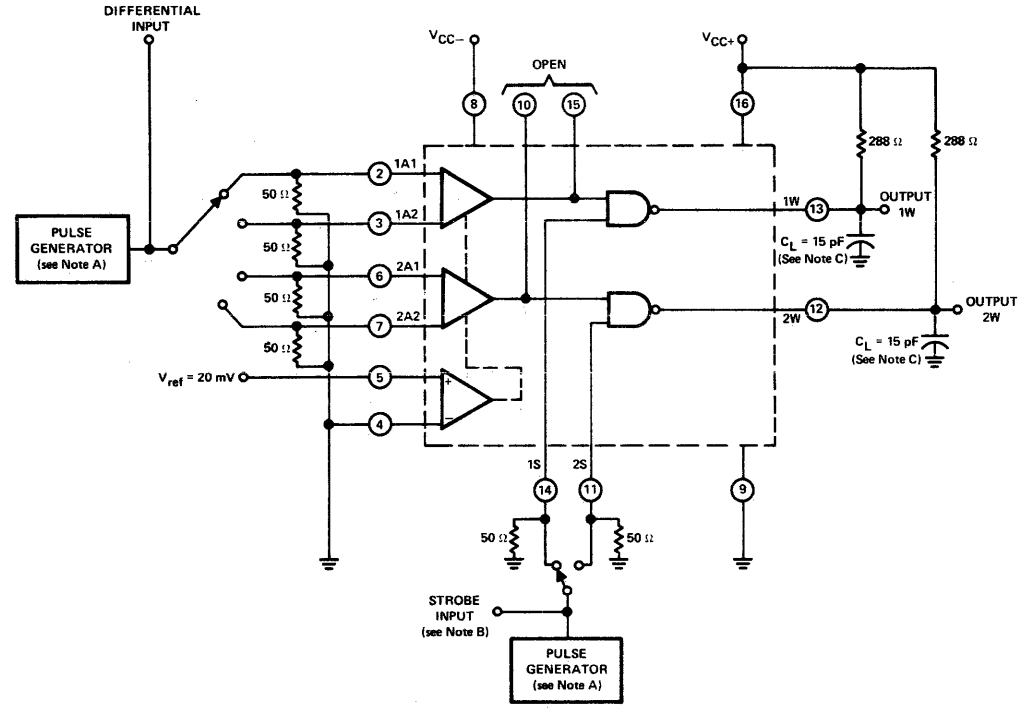
B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2A2 are being tested.

C. C_L includes probe and jig capacitance.

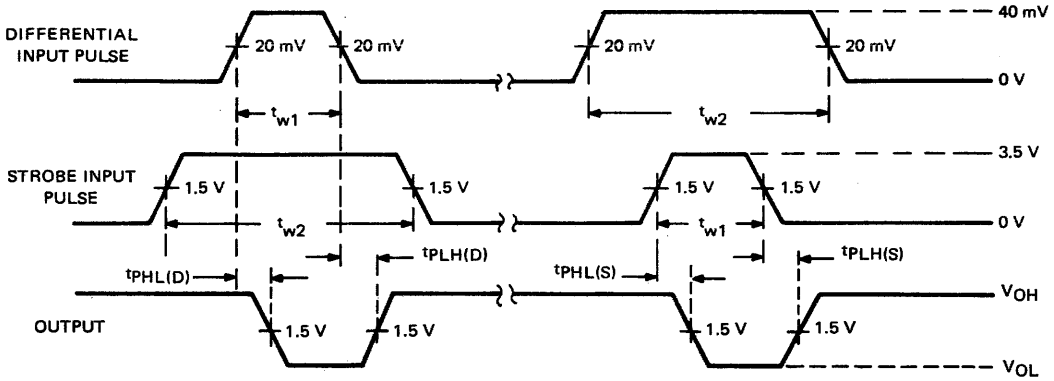
FIGURE 40–SN75234/SN75235 PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2S2 are being tested.

C. C_L includes probe and jig capacitance.

FIGURE 41—SN75238/SN75239 PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

THRESHOLD VOLTAGE
vs
REFERENCE VOLTAGE

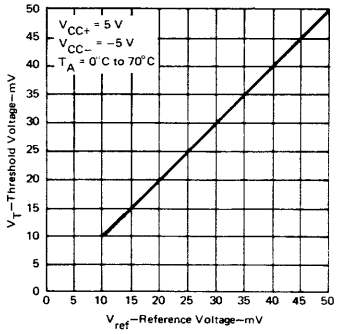


FIGURE 42

THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

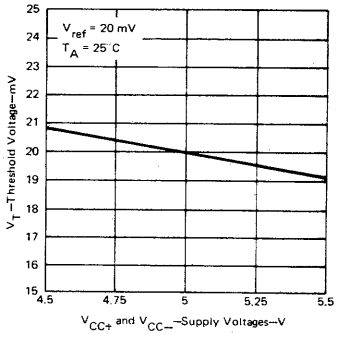


FIGURE 43

NORMALIZED THRESHOLD VOLTAGE
vs
PULSE REPETITION RATE

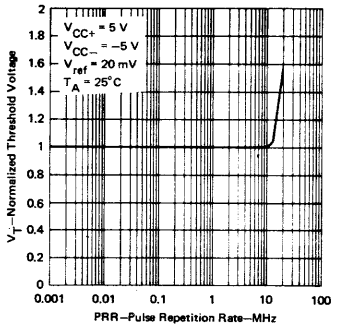


FIGURE 44

COMMON-MODE FIRING VOLTAGE
vs
FREE-AIR TEMPERATURE

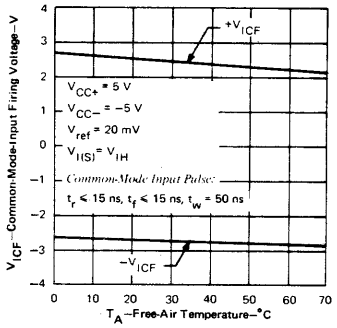


FIGURE 45

DIFFERENTIAL-INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

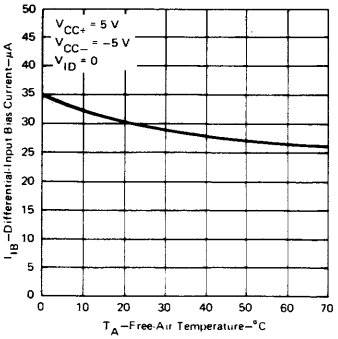


FIGURE 46

DIFFERENTIAL-INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

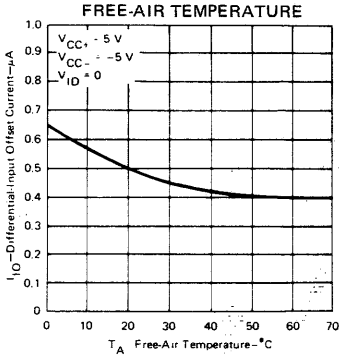


FIGURE 47

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

HIGH-LEVEL INPUT CURRENT
vs
INPUT VOLTAGE

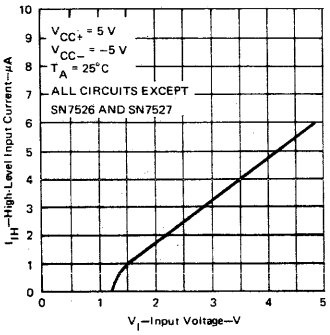


FIGURE 48

LOW-LEVEL INPUT CURRENT
vs
INPUT VOLTAGE

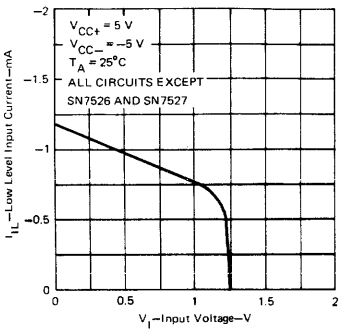


FIGURE 49

OUTPUT VOLTAGE
vs
DIFFERENTIAL-INPUT VOLTAGE

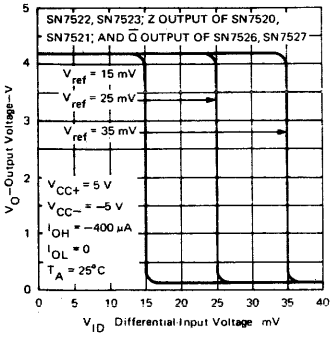


FIGURE 50

OUTPUT VOLTAGE
vs
DIFFERENTIAL-INPUT VOLTAGE

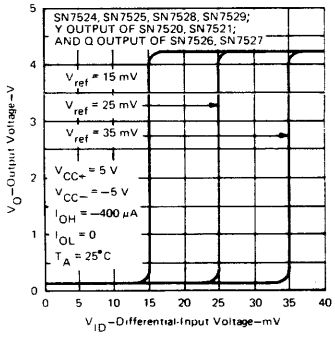


FIGURE 51

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

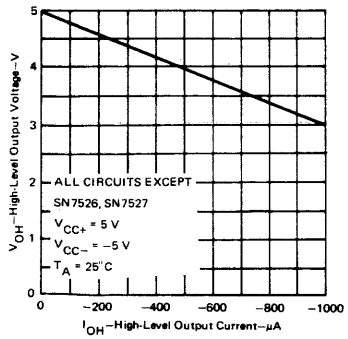


FIGURE 52

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

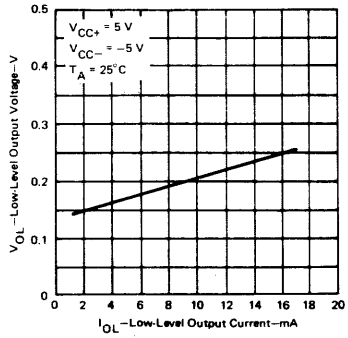


FIGURE 53

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATIONS

small memory systems

This application demonstrates an improved method of sensing data from relatively small memory systems. Two individual core planes, usually consisting of 4096 cores each, can be interfaced by each of the dual-channel SN7524 or SN7525 sense amplifiers, see Figure K. Standard TTL or DTL integrated circuits, driven directly from the compatible sense-amplifier outputs, may be selected to serve as the memory data register (MDR).

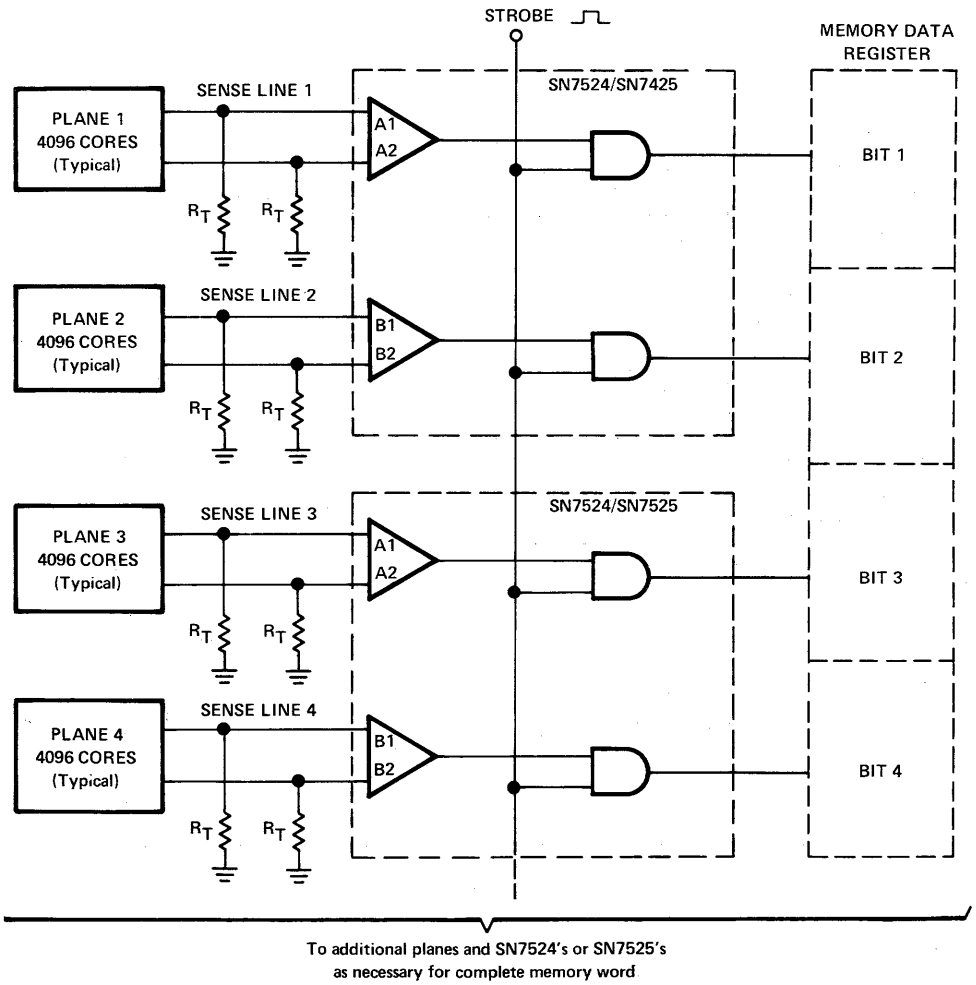


FIGURE K–SENSING SMALL MEMORY SYSTEMS

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATIONS (continued)

large memory systems

This application demonstrates an improved method of sensing data from large memory systems. The signal-to-noise ratio can be increased by sectioning the large core planes as illustrated in Figure L. Two segments, usually consisting of 4096 cores each, can be interfaced by each of the dual-input channels of the SN7420/SN7421 or SN7422/SN7423 sense amplifiers. The cascaded output gates of the SN7520/SN7521 circuits may be connected to serve as the memory data register (MDR). A number of SN7522/SN7523 sense amplifiers may be wire-AND connected to expand the input function of the MDR to interface all the segments of the plane. Complementary outputs, clear, and preset functions are provided for the MDR. Rules for combined fan-out and wire-AND capabilities must be observed.

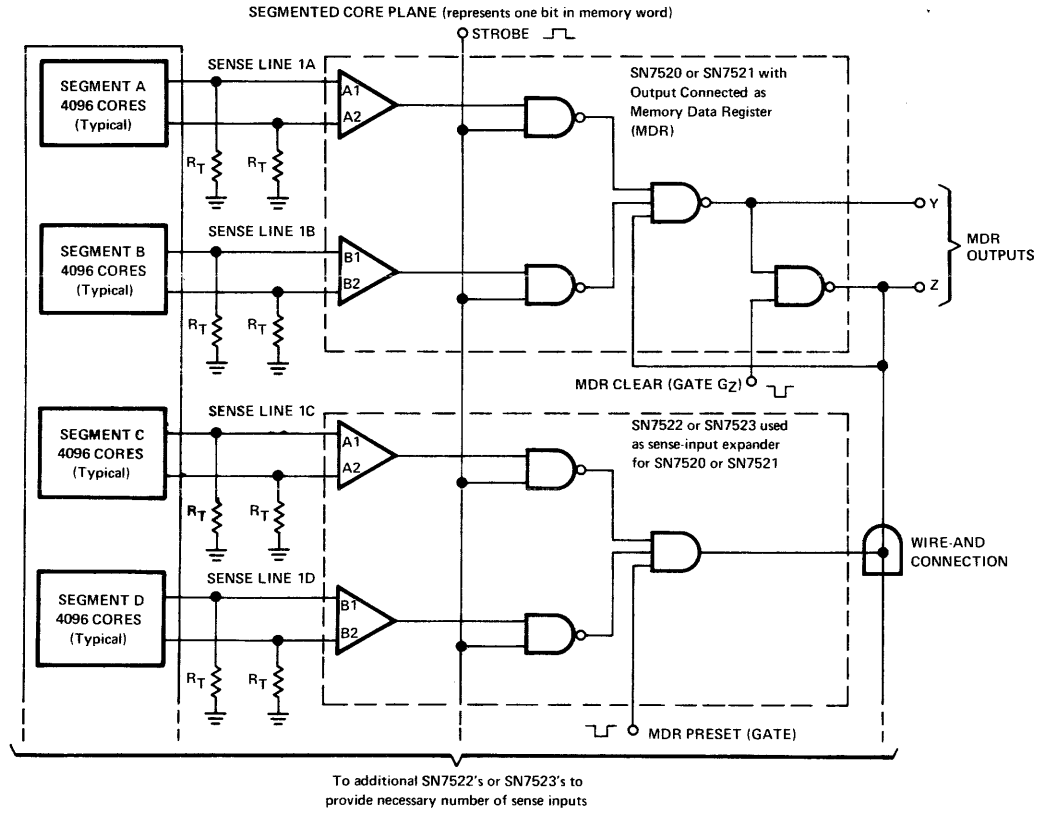
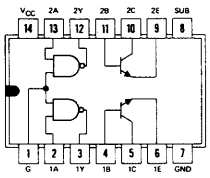
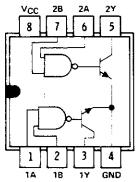
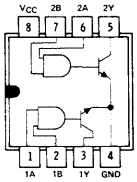
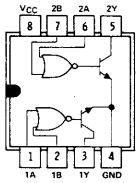
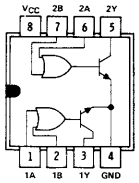


FIGURE L–SENSING LARGE MEMORY SYSTEMS

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

peripheral drivers

TYPE	SN75450A	SN75451A	SN75452	SN75453	SN75454
Block Diagrams		 Y = AB	 Y = $\overline{AB}$	 Y = A+B	 Y = $\overline{A+B}$
Features	Two TTL gates and two high current transistors on one chip. Each transistor sinks 300 mA of current and has a minimum collector-emitter breakdown voltage of 30 V. • Two Uncommitted Transistors	• 8-pin Package	• AND Gates	• NOR Gates	• OR Gates
Applications	• Lamp Driver • Relay Driver • MOS Driver • Line Driver	• Lamp Driver • Relay Driver	• Lamp Driver • Relay Driver	• Lamp Driver • Relay Driver	• Lamp Driver • Relay Driver
Package	N	P	P	P	P

3

memory drivers

TYPE	SN75303 4 X 2 TRANSISTOR ARRAY	SN75308 2 X 4 TRANSISTOR ARRAY	SN75324 DRIVER WITH DECODE INPUTS	SN75325 DRIVER WITH DECODE INPUT
Features	• Eight 150-mA Monolithic Transistors • $V_{(BR)CBO}$ = 25 V Min • $V_{(BR)CEO}$ = 18 V Min • $V_{CE(sat)}$ = 0.75 V Max at I_C = 150 mA • t_{PHL} = 14 ns Typ • t_{PLH} = 18 ns Typ	• Eight 600-mA Monolithic Transistors • $V_{(BR)CBO}$ = 25 V Min • $V_{(BR)CEO}$ = 10 V Min • $V_{CE(sat)}$ = 0.55 V Typ at I_C = 500 mA • t_{on} = 36 ns Typ • t_{off} = 23 ns Typ	• Four 400-mA Transistors • TTL-Compatible Inputs • Internal Decoding and Timing Gates • Single 14-V Supply	• Four 600-mA Transistors • TTL-Compatible Inputs • Internal Decoding • 5-V Supply
Application	• Core Memories • Read-Only Memories	• Core Memories • Read-Only Memories • Plated-Wire Memories	• Core Memories	• Core Memories • Plated-Wire Memories • Hammer Driver
Package	N, S	J, N	N, S	J, N
Application Notes			CA-107: SN75324 Monolithic Memory Driver	

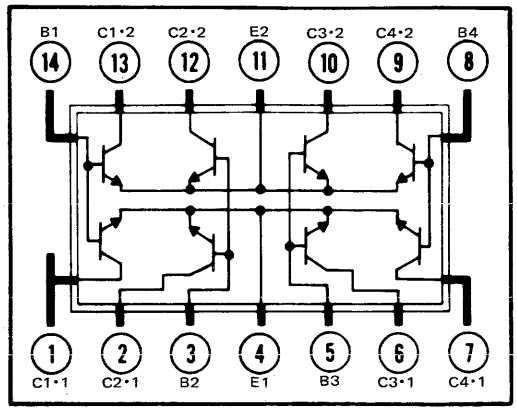
SYSTEMS INTERFACE CIRCUIT

CIRCUIT TYPE SN75303 2 X 4 TRANSISTOR ARRAY

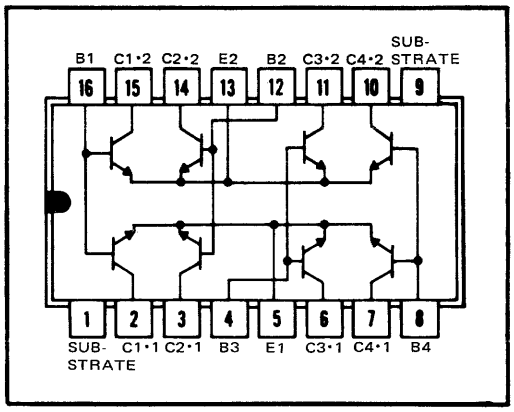
150-mA MEMORY DRIVER

- Maximum $V_{CE(sat)}$ of 750 mV at 150 mA I_C
- Maximum V_{BE} of 1.1 V at 150 mA I_C
- Minimum h_{FE} of 15 at 150 mA I_C

S FLAT PACKAGE (TOP VIEW)



N DUAL-IN-LINE PACKAGE (TOP VIEW)



3 **description**

Each SN75303 is a monolithic array of eight n-p-n transistors designed for use in core, thin-film, and plated-wire memories as a medium-current word-line driver. Selection is by base-emitter activation. The SN75303 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Collector-base voltage	25 V
Collector-emitter voltage (see Note 1)	18 V
Emitter-base voltage	5 V
Continuous collector current	200 mA
Continuous total package dissipation	250 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: This value applies when the base-emitter diode is open-circuited.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics at 25°C free-air temperature (unless otherwise noted)†

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)CBO}$	Collector-base breakdown voltage	I_C = 10 μA,	I_E = 0		25			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C = 10 mA,	I_B = 0,	See Note 2	18			V
$V_{(BR)CES}$	Collector-emitter breakdown voltage	I_C = 1 mA,	V_{BE} = 0		25			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E = 10 μA,	I_C = 0		5			V
h_{FE}	Static forward current transfer ratio	V_{CE} = 2 V,	I_C = 30 mA	See Note 2	20	35		
		V_{CE} = 2 V, T_A = 0°C	I_C = 30 mA,		15			
		V_{CE} = 2 V,	I_C = 150 mA		15	25		
V_{BE}	Base-emitter voltage	I_B = 3 mA,	I_C = 30 mA	See Note 2	0.7	0.8	0.9	V
		I_B = 3 mA, T_A = 0°C to 70°C	I_C = 30 mA,		0.65		0.95	
		I_B = 15 mA,	I_C = 150 mA		0.8	1	1.1	
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_B = 3 mA,	I_C = 30 mA	See Note 2		0.2	0.4	V
		I_B = 3 mA, T_A = 70°C	I_C = 30 mA,				0.45	
		I_B = 15 mA,	I_C = 150 mA			0.5	0.75	
C_{obo}	Common-base open-circuit output capacitance (1 transistor)	V_{CB} = 5 V, See Note 3	I_E = 0,	f = 140 kHz,		5		pF
C_{ibo}	Common-base open-circuit input capacitance (4 transistors in parallel)	V_{EB} = 0.5 V, See Note 4	I_C = 0,	f = 140 kHz,		40		pF

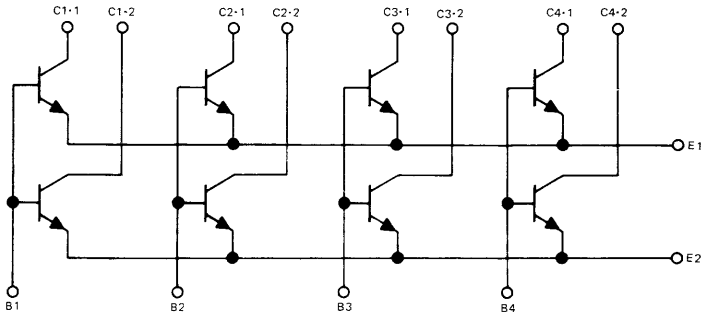
NOTES: 2. These parameters must be measured using pulse techniques, t_w = 300 μs, duty cycle ≤ 2%.
3. For measuring C_{obo}, the emitter of the transistor under test and all terminals of the other transistors are open.
4. For measuring C_{ibo}, the four base terminals are connected in parallel. The emitter terminal of the transistors not under test and all the collector terminals are open.

switching characteristics at 25°C free-air temperature†

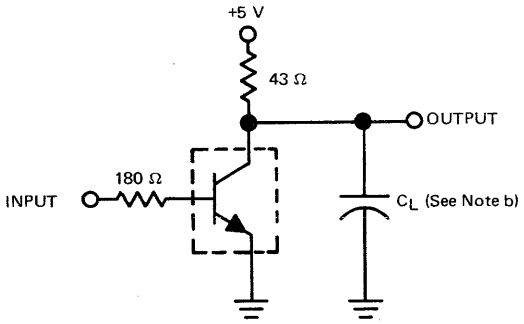
PARAMETER		TEST CONDITIONS‡		MIN	TYP	MAX	UNIT
t_{THL}	Transition time, high-to-low-level output	I_C = 100 mA,	$I_{B(1)}$ = 10 mA,		8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output	$V_{BE(off)}$ = 0, C_L ≤ 15 pF,	R_L = 43 Ω, See Figure 1		14	22	
t_{TLH}	Transition time, low-to-high-level output	I_C = 100 mA,	$I_{B(1)}$ = 10 mA,		6	12	ns
t_{PLH}	Propagation delay time, low-to-high-level output	$I_{B(2)}$ = −10 mA, C_L ≤ 15 pF,	R_L = 43 Ω, See Figure 2		18	30	

†Test conditions and limits apply separately to each transistor unless otherwise noted. The terminals of the transistors not under test are open during the measurement of these characteristics.
‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

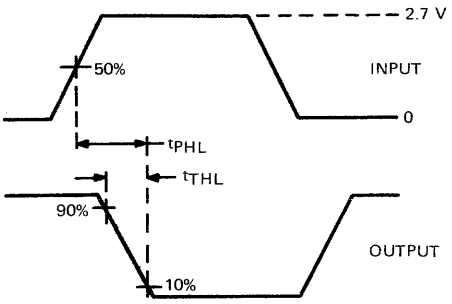
schematic



PARAMETER MEASUREMENT INFORMATION

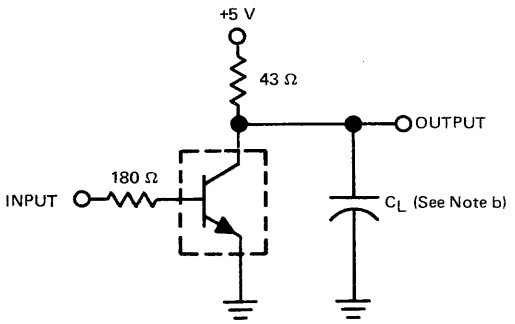


TEST CIRCUIT

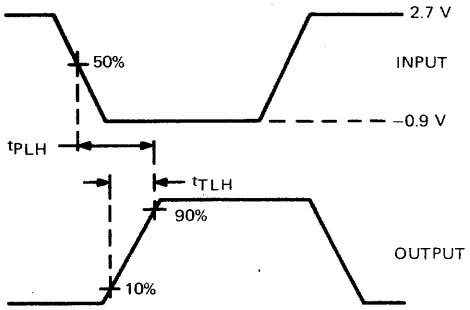


VOLTAGE WAVEFORMS

FIGURE 1–t_{THL} and t_{PHL}



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2–t_{TLH} and t_{PLH}

NOTES: a. The input waveforms are supplied by a generator with the following characteristics: $Z_{out} = 50\ \Omega$, $t_r \leq 2$ ns, $t_w \approx 70$ ns, duty cycle $\leq 2\%$.
b. C_L includes probe and jig capacitance.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

BASE-EMITTER VOLTAGE
vs
COLLECTOR CURRENT

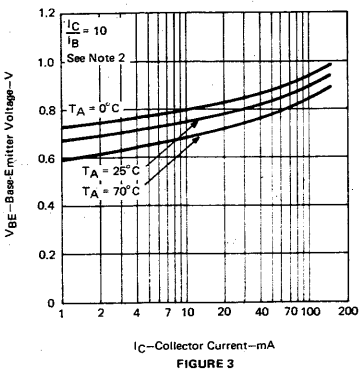


FIGURE 3

COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT

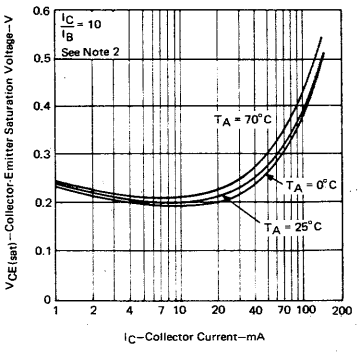


FIGURE 4

STATIC FORWARD
CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

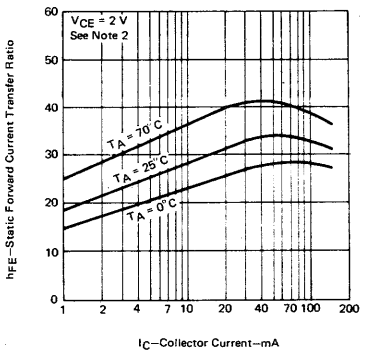


FIGURE 5

TURN-ON TIME
vs
FREE-AIR TEMPERATURE

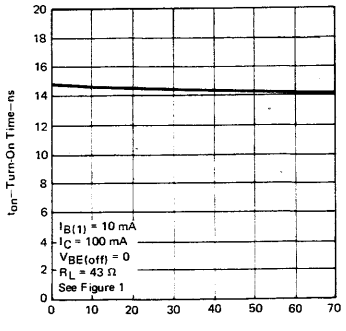


FIGURE 6

TURN-OFF TIME
vs
FREE-AIR TEMPERATURE

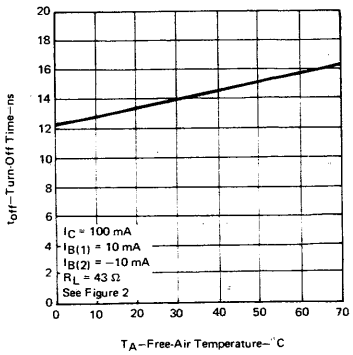


FIGURE 7

NOTE 2: These parameters must be measured using pulse techniques, t_w = 300 μs, duty cycle ≤ 2%.

CIRCUIT TYPE SN75303
2 X 4 TRANSISTOR ARRAY

TYPICAL APPLICATION DATA

Use of the SN75303 in High-Speed Read-Only Memories

Significant advantages result from the use of a high-speed, read-only memory (ROM) in computers and calculators. This ROM is used for control, as a function generator, or for performing highly repetitive routines such as multiplying, dividing , or calculating square roots. The read-only memory has permanently stored data and usually operates with a very fast cycle time. It can perform repetitive operations much more efficiently and faster than the larger and slower read-write memory in the computer or calculator.

The SN75303 two-by-four transistor array is designed to perform the word-line drive or select function for medium current, high-speed, read-only memories organized in the word-oriented (2D) or linear-select configuration. Such memories use magnetic memory elements such as plated wires, planar thin-films, transformers (as in a braided-wire memory), or ferrite switch cores. They also may utilize passive elements such as resistors, capacitors, or diodes. The typical organization of a word-oriented ROM is shown in the figure below.

3

Information is read from the ROM by selecting the desired word line. This is accomplished by appropriate activiation of one base-select and one emitter-select line. The transistor in the SN75303 array at the intersection of the selected base and emitter lines will be activated, thus sinking current from the word-line load resistor, R_L, connected to its collector. Energy is coupled from the selected word line to the sense lines by the memory elements (ME) located at the intersections of the word line and the sense lines. The presence of an ME can represent a stored logic 1 bit of information while the absence of an ME represents a stored logic 0 bit. (The desired information is stored in such a memory during fabrication and is not electrically alterable.)

The stored word is read out at the sense-amplifier outputs. The selection of a sense amplifier will depend on the type of ME used in the memory and may take the form of a special amplifier, a comparator, or a logic gate.

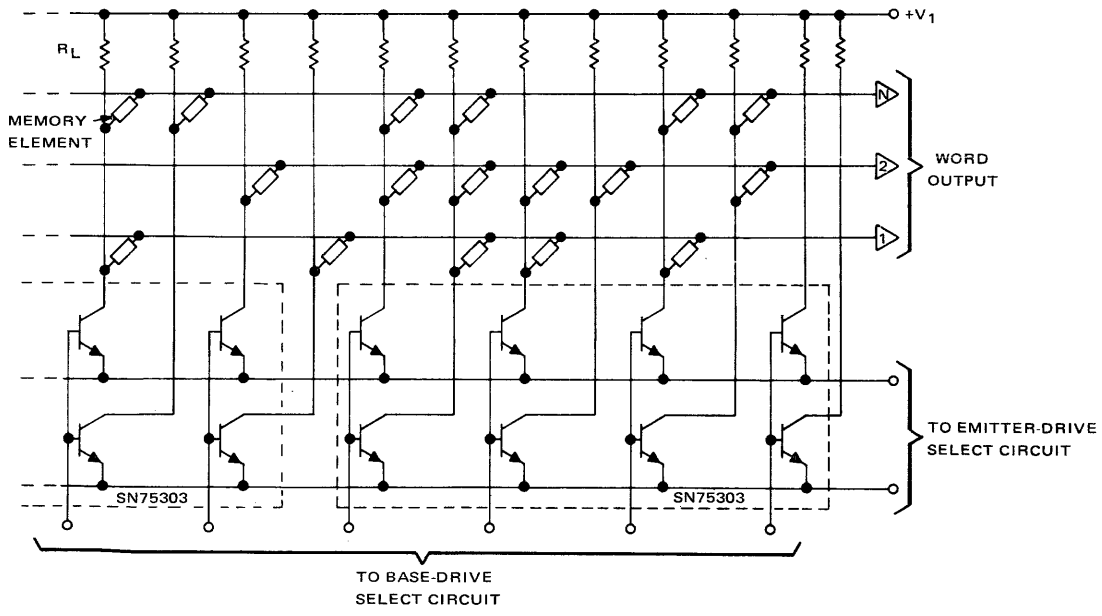


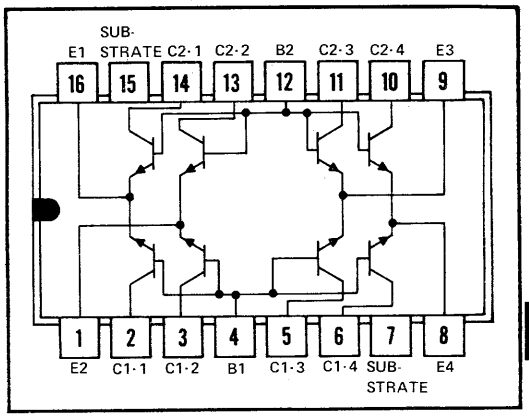
FIGURE 8

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE SN75308
2 X 4 TRANSISTOR ARRAY

- For High-Current Switching . . . to 600 mA Rated Collector Current
- Low Storage Time . . . 13 ns Typical
- Cross-Coupled Bases and Emitters Arranged for Selection

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75308 is an array of eight high-current (600 mA max) n-p-n transistors designed for use in linear select (2D) memory designs utilizing ferrite cores, plated wire, planar film, diodes, resistors, or other memory elements. One of eight transistors can be switched by selection of the appropriate base and emitter inputs. Drive of the base and emitter inputs can be provided by available circuits such as the SN7440, SN75450, and SN75451. The SN75308 transistors feature fast switching times.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Collector-base voltage	25 V
Collector-emitter voltage (see Note 1)	25 V
Collector-emitter voltage (see Note 2)	10 V
Emitter-base voltage	4.5 V
Continuous current, each collector	600 mA
Continuous total package dissipation (see Note 3)	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. This value applies when the base-emitter diode is short-circuited.
2. This value applies between 100 μA and 10 mA collector current when the base-emitter diode is open-circuited.
3. This value applies for any combination provided the ratings of single transistors are not exceeded.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE SN75308
2 X 4 TRANSISTOR ARRAY

electrical characteristics for each transistor at 25°C free-air temperature†

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)CBO}$	Collector-base breakdown voltage	I_C = 100 μA,	I_E = 0		25			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C = 10 mA,	I_B = 0,	See Note 4	10			V
$V_{(BR)CES}$	Collector-emitter breakdown voltage	I_C = 100 μA,	V_{BE} = 0		25			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E = 100 μA,	I_C = 0		5			V
$V_{(BR)CU}$	Collector-substrate breakdown voltage	I_C = 100 μA,	I_B = 0,	I_E = 0	25			V
h_{FE}	Static forward current transfer ratio	V_{CB} = 1 V,	I_E = 30 mA	See Note 4	15			
		V_{CB} = 1 V,	I_E = 100 mA		20			
		V_{CB} = 1 V,	I_E = 500 mA		20			
V_{BE}	Base-emitter voltage	I_B = 3 mA,	I_C = 30 mA	See Note 4		0.73	1	V
		I_B = 10 mA,	I_C = 100 mA			0.82	1.1	
		I_B = 30 mA,	I_C = 300 mA			1.0	1.2	
		I_B = 50 mA,	I_C = 500 mA			1.1	1.3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_B = 3 mA,	I_C = 30 mA	See Note 4		0.15	0.3	V
		I_B = 10 mA,	I_C = 100 mA			0.2	0.4	
		I_B = 30 mA,	I_C = 300 mA			0.36	0.6	
		I_B = 50 mA,	I_C = 500 mA			0.55	0.8	
$\lvert h_{fe} \rvert$	Small-signal common-emitter forward current transfer ratio	V_{CE} = 10 V,	I_C = 100 mA,	f = 100 MHz		2		
C_{obo}	Common-base open-circuit output capacitance (1 transistor)	V_{CB} = 10 V, See Note 5	I_E = 0,	f = 140 kHz,		18		pF
C_{ibo}	Common-base open-circuit input capacitance (2 transistors in parallel)	V_{EB} = 0.5 V, See Note 6	I_C = 0,	f = 140 kHz,		65		pF

NOTES: 4. These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ≤ 2%.
5. For measuring C_{obo}, the emitter terminal of the transistor under test and all terminals of the other transistors are open.
6. For measuring C_{ibo}, the base terminals are connected in parallel. The emitter terminals of the transistors not under test and all the collector terminals are open.

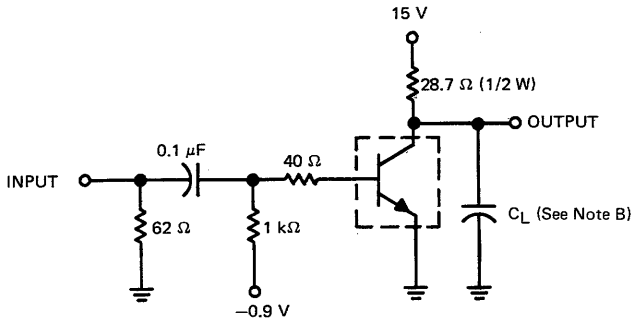
switching characteristics at 25°C free-air temperature†

PARAMETER		TEST CONDITIONS‡			TYP	UNIT
t_d	Delay time	I_C = 500 mA,	$I_{B(1)}$ = 50 mA,		16	ns
t_r	Rise time	$V_{BE(off)}$ = −0.9 V,	R_L = 28.7 Ω,		20	
t_{on}	Turn-on time	C_L = 15 pF,	See Figure 1		36	
t_s	Storage time	I_C = 500 mA,	$I_{B(1)}$ = 50 mA,		13	
t_f	Fall time	$I_{B(2)}$ = −50 mA,	R_L = 28.7 Ω,		10	
t_{off}	Turn-off time	C_L = 15 pF,	See Figure 1		23	

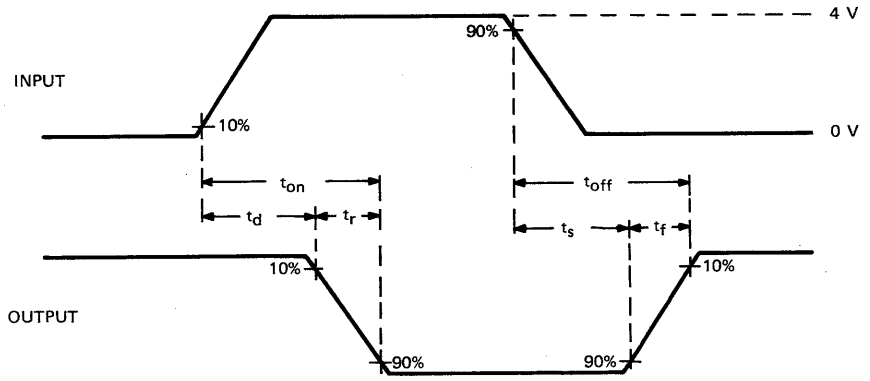
†Test conditions and limits apply separately to each transistor unless otherwise noted. The terminals of the transistors not under test are open during the measurement of these characteristics.

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns, $t_w \approx$ 100 ns, duty cycle ≤ 2%.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
EMITTER CURRENT

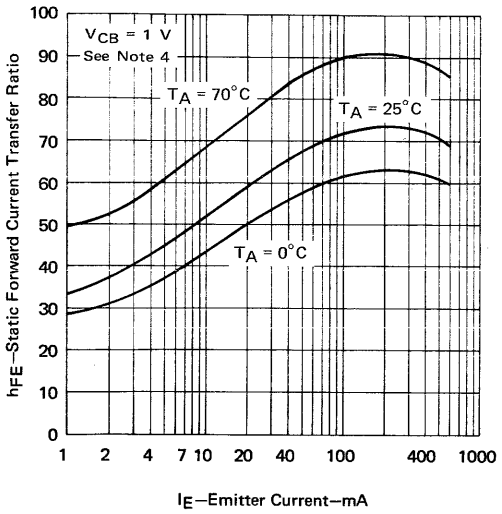


FIGURE 2

BASE-EMITTER VOLTAGE
vs
COLLECTOR CURRENT

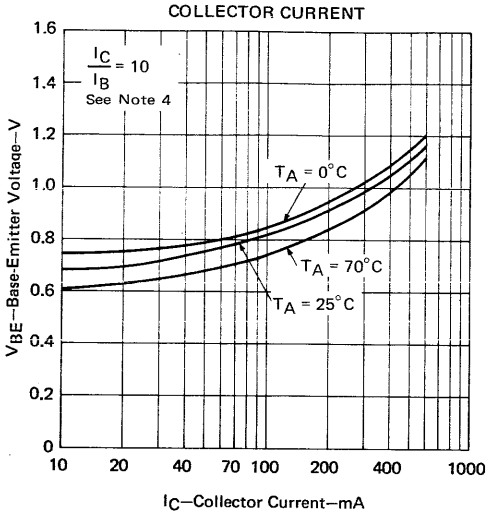


FIGURE 3

COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT

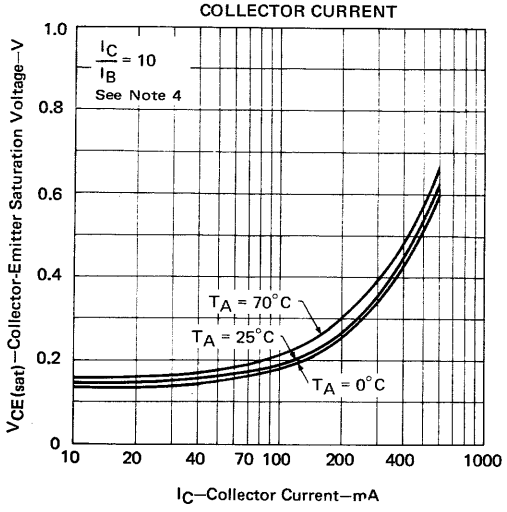


FIGURE 4

NORMALIZED COLLECTOR-EMITTER
BREAKDOWN VOLTAGE
vs
BASE-EMITTER RESISTANCE

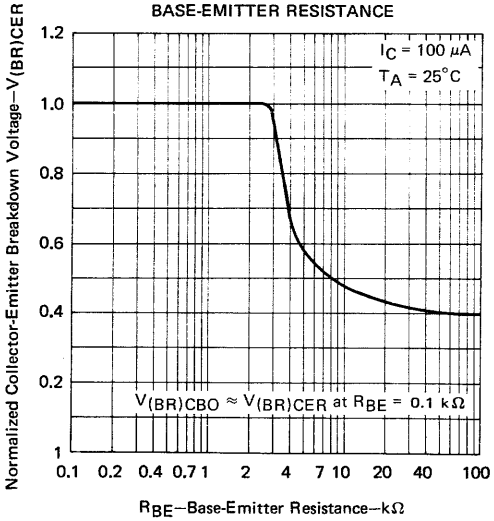


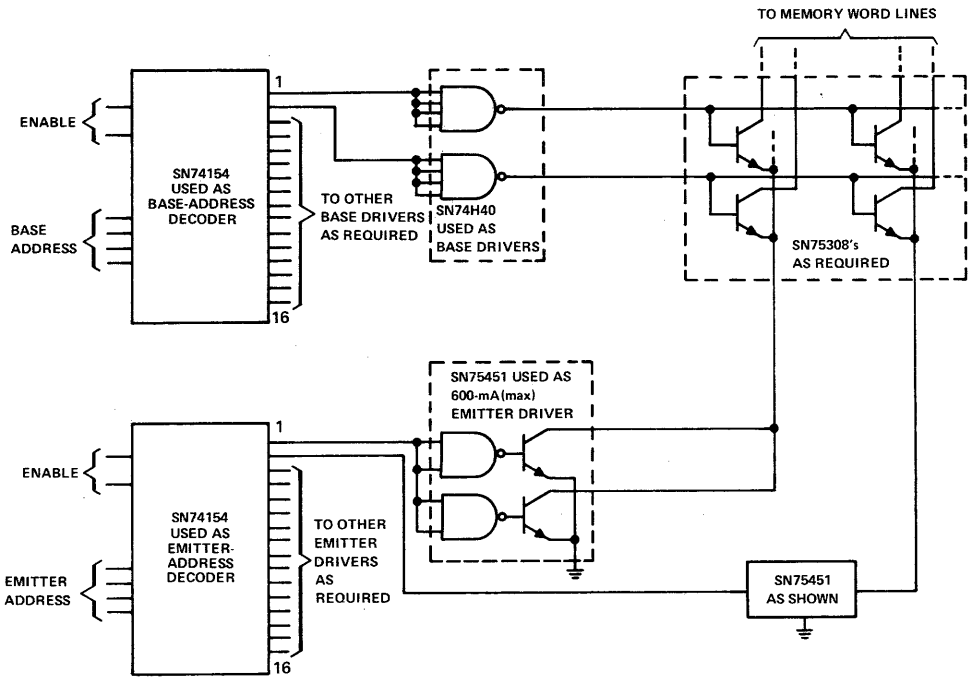
FIGURE 5

NOTE 4: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ⩽ 2%.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

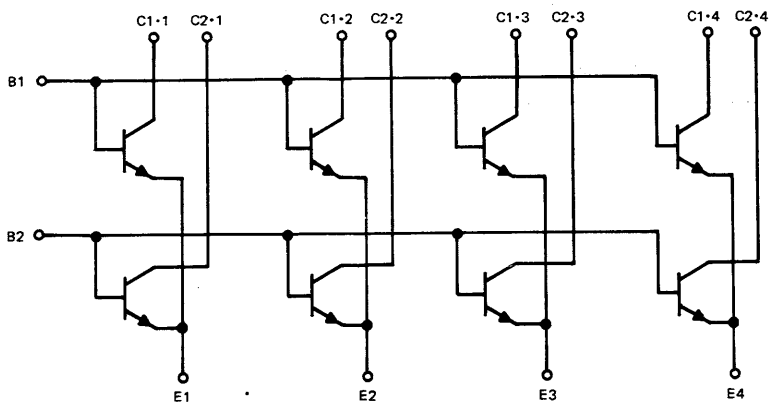
TYPICAL APPLICATION DATA

The SN75308 two-by-four transistor array is designed to perform the word-line drive or select function for medium current, high-speed, read-only memories organized in the word-oriented (2D) or linear-select configuration. Such memories use magnetic memory elements such as plated wires, planar thin-films, transformers (as in a braided-wire memory), or ferrite switch cores. They also may utilize passive elements such as resistors, capacitors, or diodes. The typical organization of a word-oriented ROM is shown on the SN75303 data sheet; a base and emitter selection technique is shown below. A similar selection circuit can be used with the SN75303 although with it the SN75451's need not be paralleled.



3

schematic



CIRCUIT TYPE SN75324
MEMORY DRIVER WITH DECODE INPUTS

SERIES 75 MEMORY DRIVER

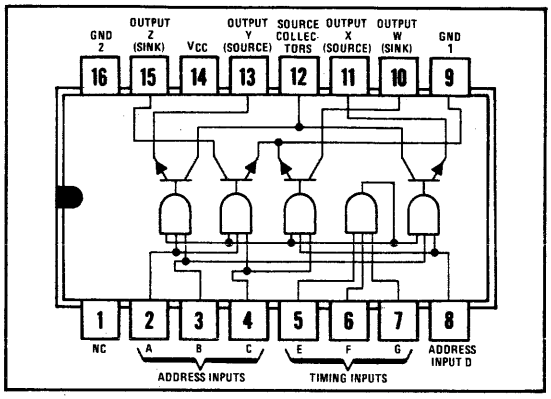
PERFORMANCE

- fast switching times
- 400-mA output capability
- internal decoding and timing circuitry
- dual sink/source outputs
- output short-circuit protection

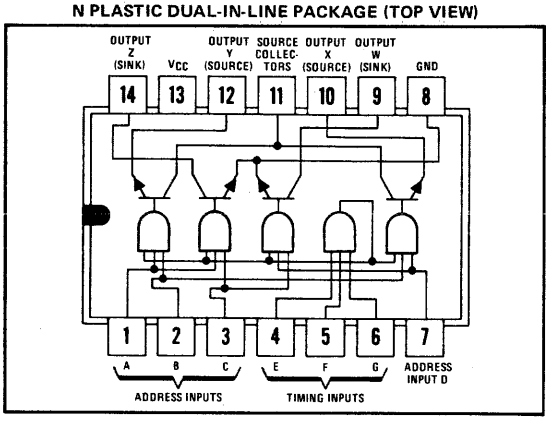
EASE OF DESIGN

- TTL or DTL compatibility
- eliminates transformer coupling
- reduces drive-line lengths
- increases reliability
- minimizes external components
- choice of flat or dual-in-line packages

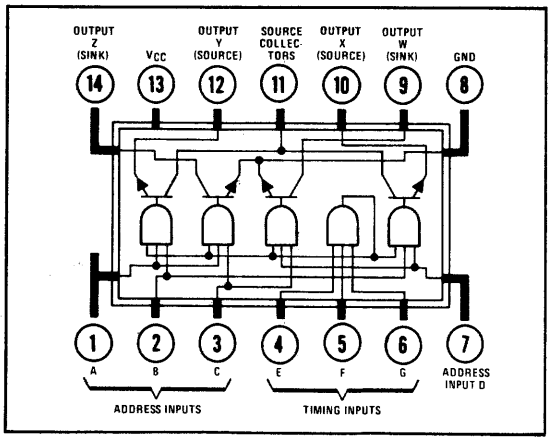
J CERAMIC DUAL-IN-LINE PACKAGE (TOP VIEW)



N PLASTIC DUAL-IN-LINE PACKAGE (TOP VIEW)



S FLAT PACKAGE (TOP VIEW)



NC—No internal connection
GND 1 and GND 2 are to be used in parallel

description

The SN75324 is a monolithic memory driver with decode inputs designed for use with magnetic memories. The device contains two 400-milliampere (source/sink) switch pairs, with decoding capability from four address lines. Two address inputs (B and C) are used for mode selection, i.e., source or sink. The other two address inputs (A and D) are used for switch-pair selection, i.e., output switch-pair Y/Z or W/X respectively.

The sink circuit is composed of an inverting switch with a transistor-transistor-logic (TTL) input. The source circuit is an emitter-follower driven from a TTL input stage.

The SN75324 is characterized for operation from 0°C to 70°C.

TRUTH TABLE

INPUTS							OUTPUTS			
ADDRESS			TIMING				SINK	SOURCES		SINK
A	B	C	D	E	F	G	W	X	Y	Z
0	0	1	1	1	1	1	ON	OFF	OFF	OFF
0	1	0	1	1	1	1	OFF	ON	OFF	OFF
1	1	0	0	1	1	1	OFF	OFF	ON	OFF
1	0	1	0	1	1	1	OFF	OFF	OFF	ON
X	X	X	X	0	X	X	OFF	OFF	OFF	OFF
X	X	X	X	X	0	X	OFF	OFF	OFF	OFF
X	X	X	X	X	X	0	OFF	OFF	OFF	OFF

NOTES: 1. X = Logical 1 or logical 0.
2. Not more than one output is to be allowed to be ON at one time: When all timing inputs are at a logical 1, two of the address inputs must be at a logical 0.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

logic definition

Standard positive logic applies with the following definitions used for specifying digital-level signals:

LOW VOLTAGE = LOGICAL 0
HIGH VOLTAGE = LOGICAL 1

absolute maximum ratings over operating case temperature range (unless otherwise noted)

Supply voltage V_{CC} (See Note 1) . . . . . 17 V
Input voltage (See Note 2) . . . . . 5.5 V
Operating case temperature range . . . . . 0°C to 70°C
Continuous total power dissipation at (or below) 70°C case temperature . . . . . 800 mW
Storage temperature range . . . . . -65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

3

electrical characteristics (unless otherwise noted, V_{CC} = 14 V, T_C = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input	1		3.5			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input	1				0.8	V
$I_{in(1)}$	Logical 1 level address input current	1	V_{in} = 5 V			200	μA
$I_{in(1)}$	Logical 1 level timing input current	1	V_{in} = 5 V			100	μA
$I_{in(0)}$	Logical 0 level address input current	1	V_{in} = 0 V			-6	mA
$I_{in(0)}$	Logical 0 level timing input current	1	V_{in} = 0 V			-12	mA
$V_{(sat)}$	Sink saturation voltage	2	$I_{sink} \simeq$ 420 mA, R_L = 53 Ω		0.75	0.85	V
$V_{(sat)}$	Source saturation voltage	2	$I_{source} \simeq$ -420 mA, R_L = 47.5 Ω		0.75	0.85	V
I_{off}	Output reverse current (off state)	1	V_{in} = 0 V		125	200	μA
I_{CC}	Supply current, all sources and sinks off	3	V_{in} = 0 V		12.5	15	mA
I_{CC}	Supply current, either sink selected	4			30	40	mA
I_{CC}	Supply current, either source selected	4			25	35	mA

†These typical values are at T_C = 25°C.

switching characteristics, V_{CC} = 14 V, T_C = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd(1)}$	Propagation delay time to logical 1 level, source output	5	R_{L1} = 53 Ω, R_{L2} = 500 Ω, C_L = 20 pF			90	ns
$t_{pd(0)}$	Propagation delay time to logical 0 level, source output	5				50	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level, sink output	6	R_L = 53 Ω, C_L = 20 pF			110	ns
$t_{pd(0)}$	Propagation delay time to logical 0 level, sink output	6				40	ns
t_s	Sink storage time	6				70	ns

3

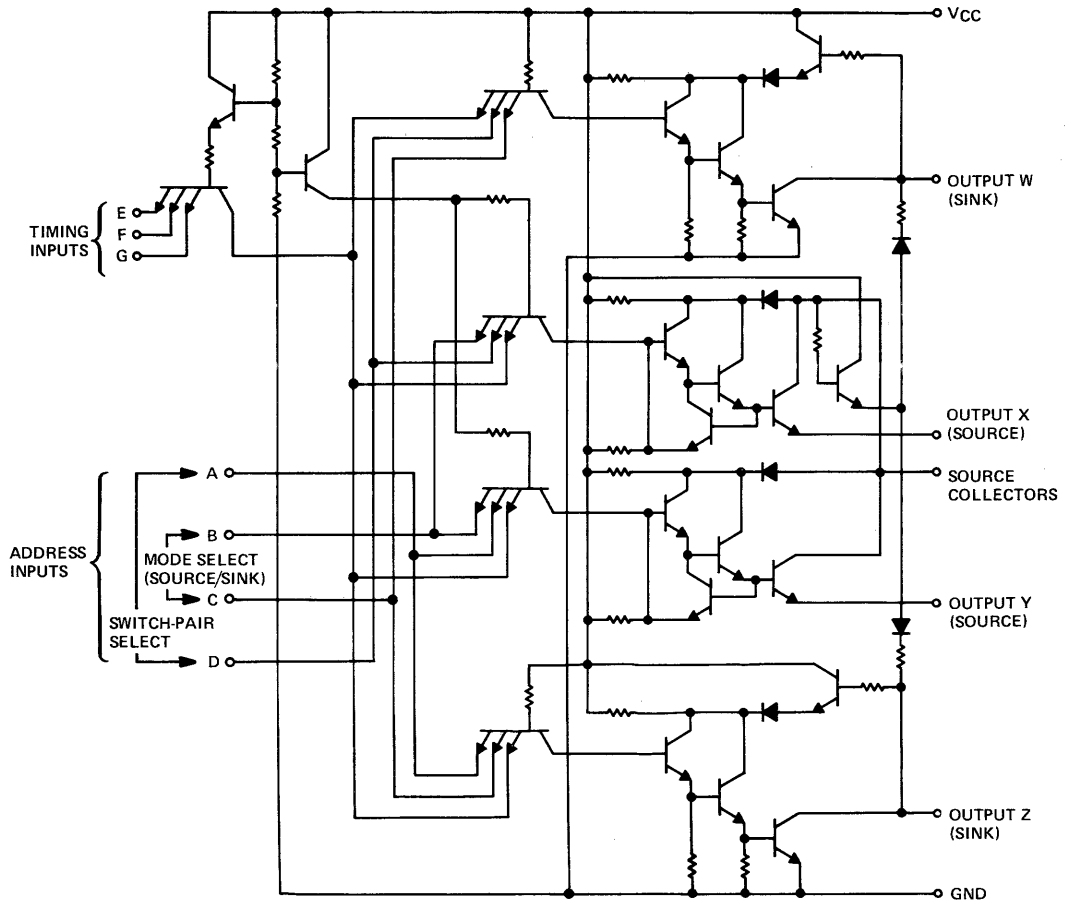
thermal information

The SN75324 is designed to be used at a case temperature not to exceed 70°C. Under this condition, infrared microradiometer and X-ray studies indicate that a safe junction temperature is maintained under specified worst-case conditions.

SN75324 circuits should be mounted so that minimum thermal resistance is achieved. A thermal compound should be used between the bottom of the flat S package and a heat sink. This, in conjunction with unrestricted forced-air flow across the heat sink and package, has been found to adequately satisfy thermal requirements. No thermal compound is required with the dual-in-line package. Air flow should be across the short dimension of either package.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

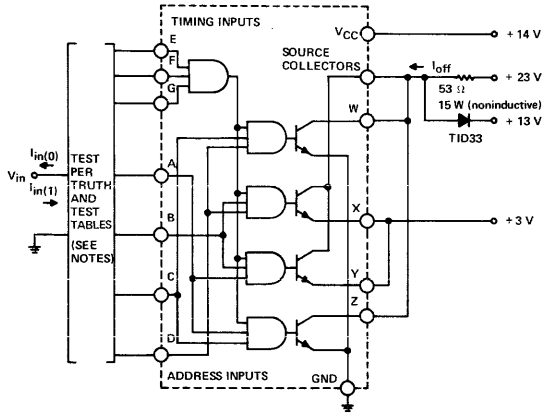
schematic


VCC
OUTPUT W
(SINK)
TIMING
INPUTS
E
F
G
OUTPUT X
(SOURCE)
SOURCE
COLLECTORS
A
B
ADDRESS
INPUTS
MODE SELECT
(SOURCE/SINK)
C
OUTPUT Y
(SOURCE)
SWITCH-PAIR
SELECT
D
OUTPUT Z
(SINK)
GND

CIRCUIT TYPE SN75324
MEMORY DRIVER WITH DECODE INPUTS

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

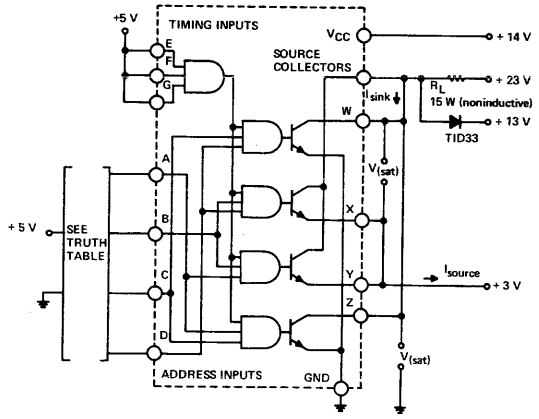


TEST TABLE FOR $I_{in(0)}$

APPLY 3.5 V	GROUND	TEST $I_{in(0)}$
B, C, E, F, and G	A and D	A
B, C, E, F, and G	A and D	D
A, D, E, F, and G	B and C	B
A, D, E, F, and G	B and C	C
A, B, C, D, F, and G	E	E
A, B, C, D, E, and G	F	F
A, B, C, D, E, and F	G	G

NOTES: 1. Check $V_{in(1)}$ and $V_{in(0)}$ per Truth Table.
2. Measure $I_{in(0)}$ per Test Table.
3. When measuring $I_{in(1)}$, all other inputs are at ground. Each input is tested separately.

FIGURE 1 – $V_{in(0)}$, $V_{in(1)}$, $I_{in(0)}$, $I_{in(1)}$, and I_{off}



NOTE: This parameter must be measured using pulse techniques. t_p = 500 ns, duty cycle ⩽ 1%.

FIGURE 2 – $V_{(sat)}$

† Arrows indicate actual direction of current flow.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits † (continued)

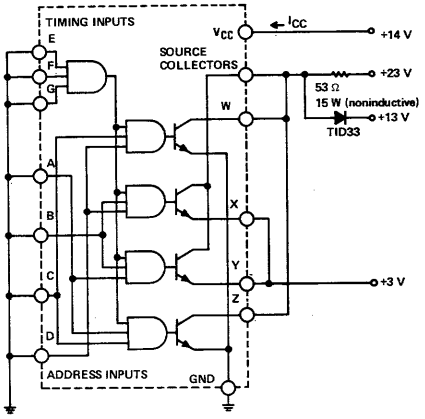
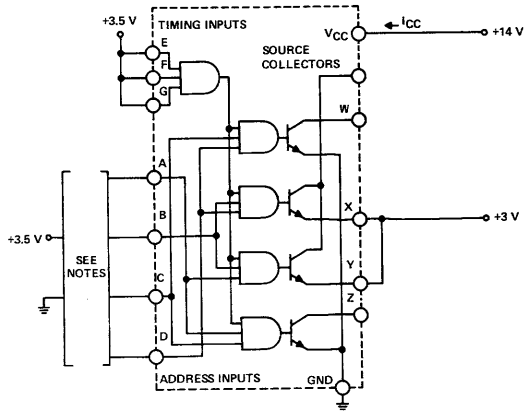


FIGURE 3 – I_{CC} (ALL OUTPUTS OFF)



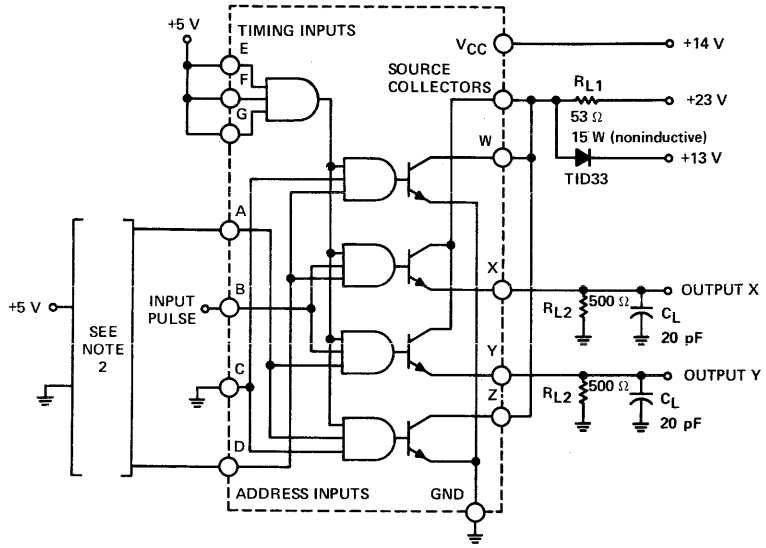
NOTES: 1. Ground A and B, apply 3.5 V to C and D, and measure I_{CC} (output W is on).
2. Ground B and D, apply 3.5 V to A and C, and measure I_{CC} (output Z is on).
3. Ground A and C, apply 3.5 V to B and D, and measure I_{CC} (output X is on).
4. Ground C and D, apply 3.5 V to A and B, and measure I_{CC} (output Y is on).

FIGURE 4 – I_{CC} (ONE OUTPUT ON)

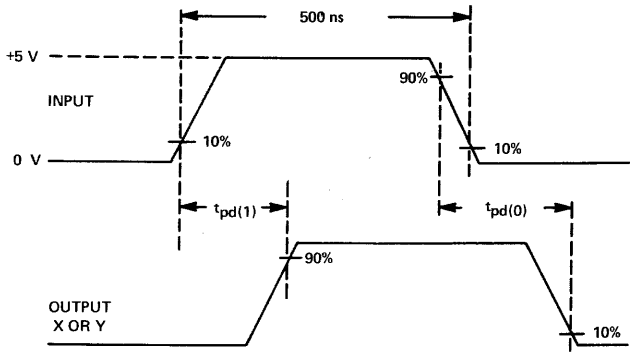
† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST TABLE



VOLTAGE WAVEFORMS

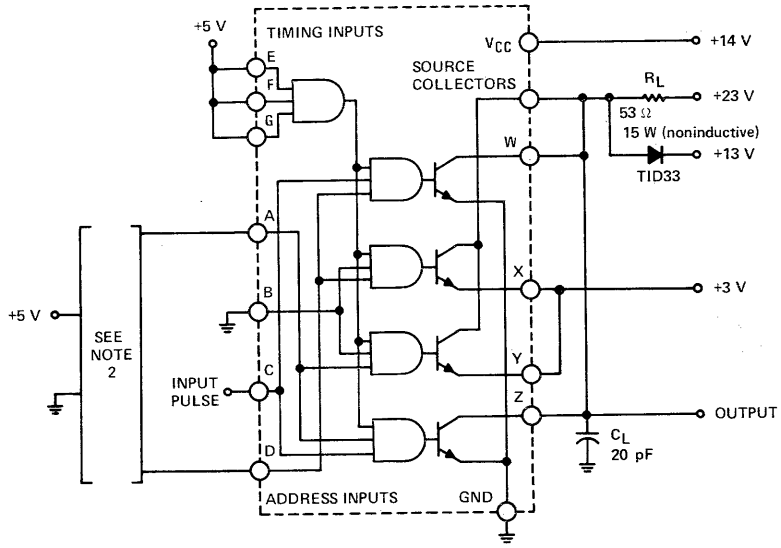
NOTES: 1. The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leqslant 1\%$, and $Z_{out} \approx 50\ \Omega$.
2. When measuring delay times at output X, apply +5 V to input D, and ground A. When measuring delay times at output Y, apply +5 V to input A, and ground D.
3. C_L includes probe and jig capacitance.
4. Unless otherwise noted all resistors are 0.5 W.

FIGURE 5 – SOURCE-OUTPUT SWITCHING TIMES

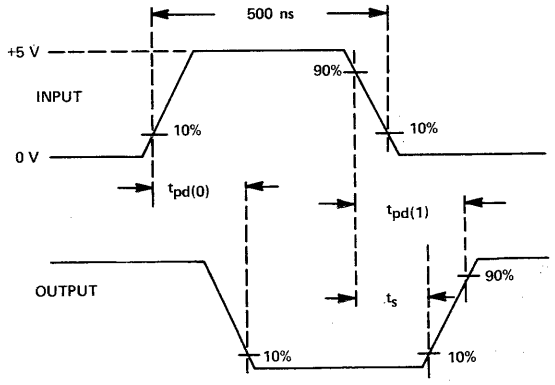
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leqslant 1\%$, $Z_{out} \approx 50\ \Omega$.
2. When measuring delay times at output W, apply +5 V to input D, and ground A. When measuring delay times at output Z, apply +5 V to input A, and ground D.
3. C_L includes probe and jig capacitance.

FIGURE 6 – SINK-OUTPUT SWITCHING TIMES

CIRCUIT TYPES SN55325, SN75325
MEMORY DRIVERS

SERIES 55/75 MEMORY DRIVER
featuring

PERFORMANCE

- 600-mA Output Capability
- Fast Switching Times
- Output Short-Circuit Protection
- Dual Sink and Dual Source Outputs
- Minimum Time Skew between Address and Output Current Rise
- 24-Volt Output Capability

EASE OF DESIGN

- Source Base Drive Externally Adjustable
- TTL or DTL Compatibility
- Input Clamping Diodes
- Transformer Coupling Eliminated
- Reliability Increased
- Drive-Line Lengths Reduced
- Use of External Components Minimized

3

description

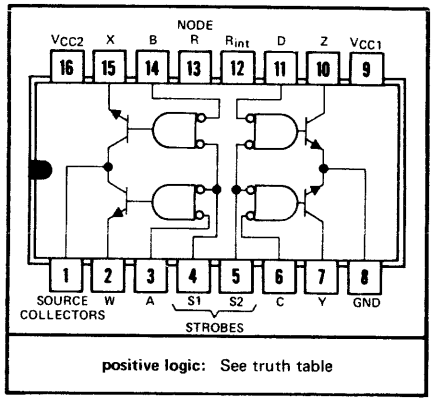
The SN55325 and SN75325 are monolithic integrated circuit memory drivers with logic inputs and are designed for use with magnetic memories.

The devices contain two 600-milliampere source-switch pairs and two 600-milliampere sink-switch pairs. Source selection is determined by one of two logic inputs, and source turn-on is determined by the source strobe. Likewise, sink selection is determined by one of two logic inputs, and sink turn-on is determined by the sink strobe. This arrangement allows selection of one of the four switches and its subsequent turn-on with minimum time skew of the output current rise.

When R_{int} and node R are connected together, the amount of base drive available for the source-1 or source-2 output transistor is set internally by a 575-ohm resistor. This method provides adequate base drive for source currents up to 375 mA with a V_{CC2} voltage of 15 volts or 600 mA with a V_{CC2} voltage of 24 volts.

When source currents greater than 375 mA are required, it is recommended that a resistor of the appropriate value be connected between V_{CC2} and node R and R_{int} must remain open. By using this method the source base current may usually be regulated within ±5%. An advantage of this method of setting the base drive is that the power dissipated by this resistor is external to the package and allows the integrated circuit to operate at higher source currents for a given junction temperature.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



TRUTH TABLE

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant
NOTE: Not more than one output is to be on at any one time.

Each sink-output collector has an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2}. This arrangement provides protection from voltage surges associated with switching inductive loads.

The SN55325 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN75325 is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55325	SN75325	UNIT
Supply voltage V_{CC1} (see Note 1)		7	7	V
Supply voltage V_{CC2} (see Note 1)		25	25	V
Input voltage (any address or strobe input)		5.5	5.5	V
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 2)		800	800	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N Package	260	260	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation of SN55325 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 20.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

3

PARAMETER			TEST FIGURE	TEST CONDITIONS		SN55325 MIN	SN55325 TYP†	SN55325 MAX	SN75325 MIN	SN75325 TYP†	SN75325 MAX	UNIT
V_{IH}	High-level input voltage		1 & 2			2			2			V
V_{IL}	Low-level input voltage		3 & 4					0.8			0.8	V
V_I	Input clamp voltage		5	V_{CC1} = 4.5 V, I_I = −10 mA,	V_{CC2} = 24 V, T_A = 25°C		−1.3	−1.7		−1.3	−1.7	V
$I_{(off)}$	Source-collectors terminal off-state current		1	V_{CC1} = 4.5 V, V_{CC2} = 24 V	Full range			500			200	μA
					T_A = 25°C		3	150		3	200	
V_{OH}	High-level sink output voltage		2	V_{CC1} = 4.5 V, I_O = 0	V_{CC2} = 24 V,	19	23		19	23		V
$V_{(sat)}$	Saturation voltage‡	Source outputs	3	V_{CC1} = 4.5 V, V_{CC2} = 15 V, R_L = 24 Ω, $I_{(source)}$ ≈ −600 mA, See Note 3	Full range			0.9			0.9	V
					T_A = 25°C		0.43	0.7		0.43	0.75	
		Sink outputs	4	V_{CC1} = 4.5 V, V_{CC2} = 15 V, R_L = 24 Ω, $I_{(sink)}$ ≈ 600 mA, See Note 3	Full range			0.9			0.9	
					T_A = 25°C		0.43	0.7		0.43	0.75	
I_I	Input current at maximum input voltage	address inputs	5	V_{CC1} = 5.5 V, V_I = 5.5 V	V_{CC2} = 24 V,			1			1	mA
		strobe inputs						2			2	
I_{IH}	High-level input current	address inputs	5	V_{CC1} = 5.5 V, V_I = 2.4 V	V_{CC2} = 24 V,		3	40		3	40	μA
		strobe inputs					6	80		6	80	
I_{IL}	Low-level input current	address inputs	5	V_{CC1} = 5.5 V, V_I = 0.4 V	V_{CC2} = 24 V,		−1	−1.6		−1	−1.6	mA
		strobe inputs					−2	−3.2		−2	−3.2	
$I_{CC(off)}$	Supply current, all sources and sinks off	from V_{CC1}	6	V_{CC1} = 5.5 V, T_A = 25°C	V_{CC2} = 24 V,		14	22		14	22	mA
		from V_{CC2}					7.5	20		7.5	20	
I_{CC1}	Supply current from V_{CC1}, either sink on		7	V_{CC1} = 5.5 V, $I_{(sink)}$ = 50 mA,	V_{CC2} = 24 V, T_A = 25°C		55	70		55	70	mA
I_{CC2}	Supply current from V_{CC2}, either source on		8	V_{CC1} = 5.5 V, $I_{(source)}$ = −50 mA,	V_{CC2} = 24 V, T_A = 25°C		32	50		32	50	mA

†All typical values are at T_A = 25°C.
‡Not more than one output is to be on at any one time.
NOTE 3: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ≤ 2%.

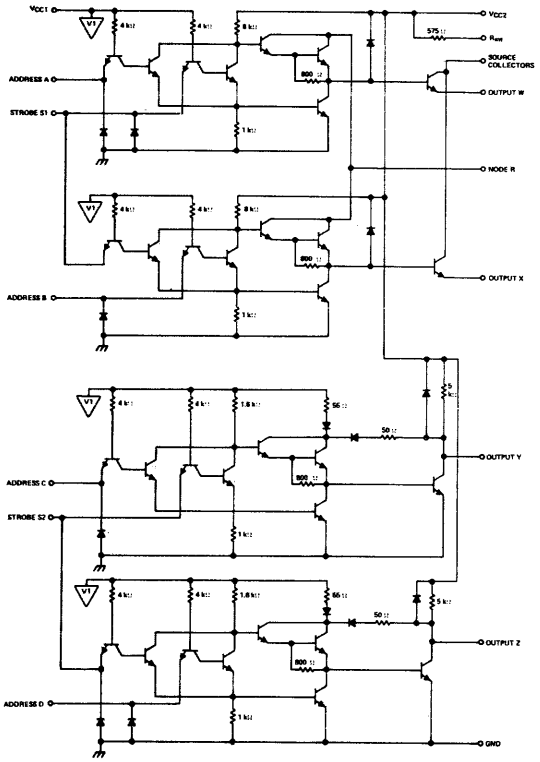
switching characteristics, V_{CC1} = 5 V, T_A = 25°C

PARAMETER¶	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Source collectors	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		25	50	ns
t_{PHL}					25	50	
t_{TLH}	Source outputs	10	V_{CC2} = 20 V, R_L = 1 kΩ, C_L = 25 pF		55		ns
t_{THL}					7		
t_{PLH}	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		20	45	ns
t_{PHL}					20	45	
t_{TLH}	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		7	15	ns
t_{THL}					9	20	
t_s	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		15	30	ns

3

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{TLH} = transition time, low-to-high-level output
t_{THL} = transition time, high-to-low-level output
t_s = storage time

schematic

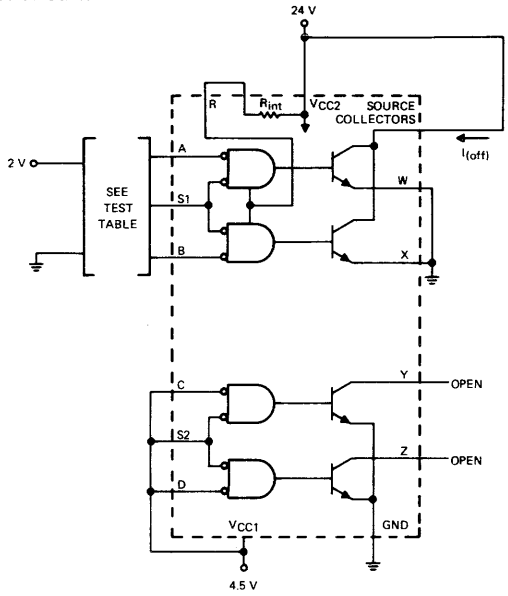


Component values shown are nominal.
V1 . . . V_{CC} bus

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

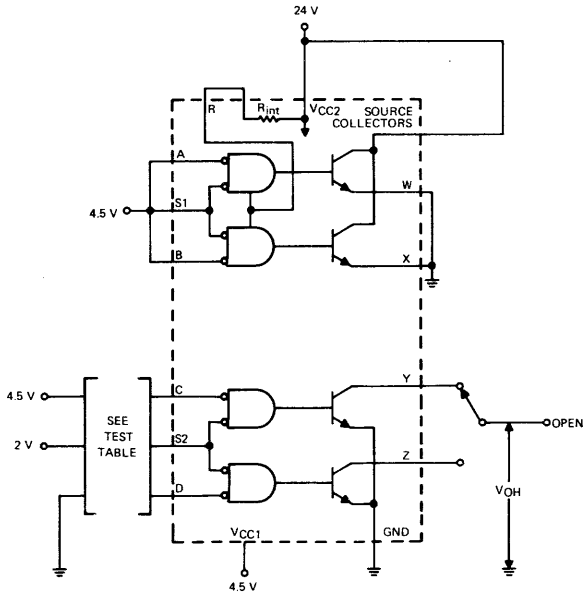
d-c test circuits†



TEST TABLE

A	B	S1
GND	GND	2 V
2 V	2 V	GND

FIGURE 1–$I_{(off)}$



TEST TABLE

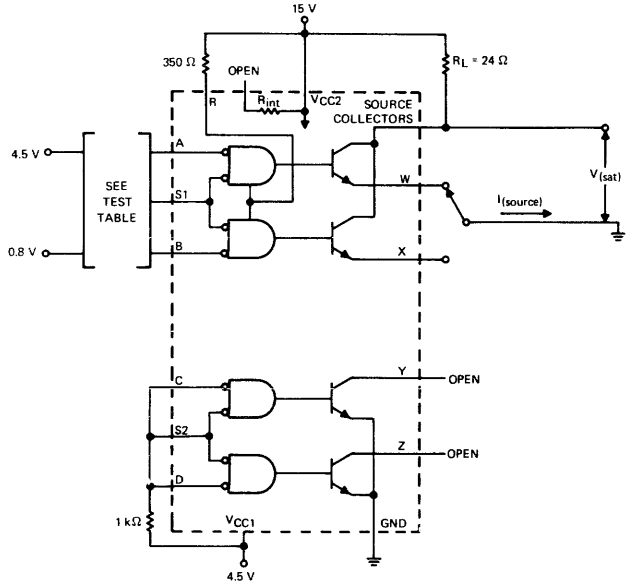
C	D	S2	Y	Z
2 V	4.5 V	GND	V_{OH}	OPEN
GND	4.5 V	2 V	V_{OH}	OPEN
4.5 V	2 V	GND	OPEN	V_{OH}
4.5 V	GND	2 V	OPEN	V_{OH}

FIGURE 2–V_{IH} AND V_{OH}

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)†

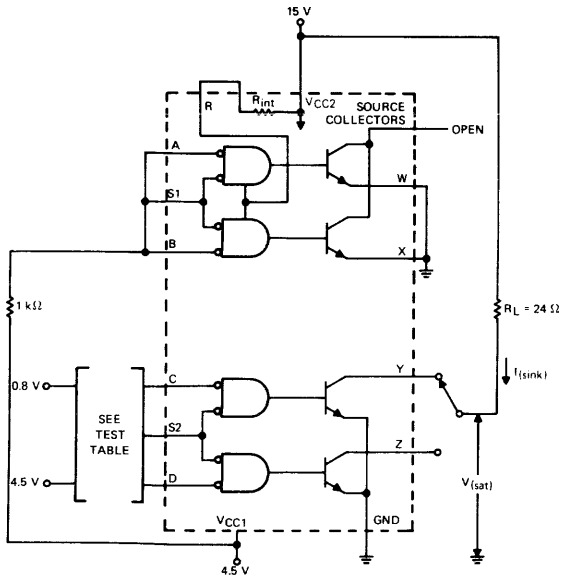


TEST TABLE

A	B	S1	W	X
0.8 V	4.5 V	0.8 V	GND	OPEN
4.5 V	0.8 V	0.8 V	OPEN	GND

NOTE A: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ⩽ 2%.

FIGURE 3–V_{IL} AND SOURCE $V_{(sat)}$



TEST TABLE

C	D	S2	Y	Z
0.8 V	4.5 V	0.8 V	R_L	OPEN
4.5 V	0.8 V	0.8 V	OPEN	R_L

NOTE A: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ⩽ 2%.

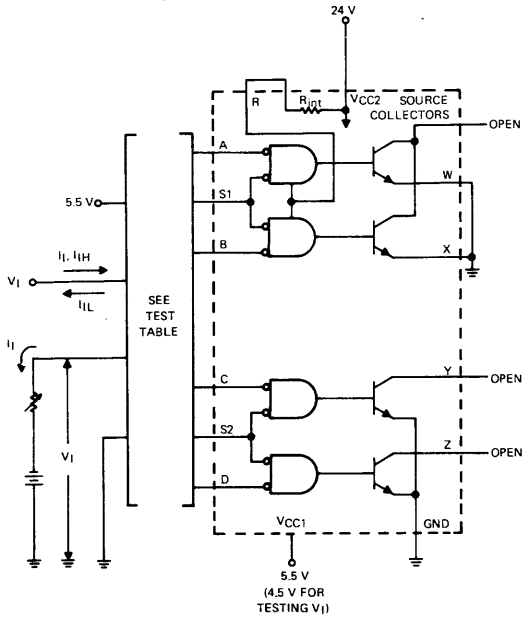
FIGURE 4–V_{IL} AND SINK $V_{(sat)}$

† Arrows indicate actual direction of current flow.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)†



TEST TABLES

I_I, I_{IH}

APPLY V_I = 5.5 V, MEASURE I_I APPLY V_I = 2.4 V, MEASURE I_{IH}	GROUND	APPLY 5.5 V
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

APPLY V_I = 0.4 V, MEASURE I_{IL} APPLY I_I = −10 mA MEASURE V_I	APPLY 5.5 V
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

FIGURE 5–V_I, I_I, I_{IH}, AND I_{IL}

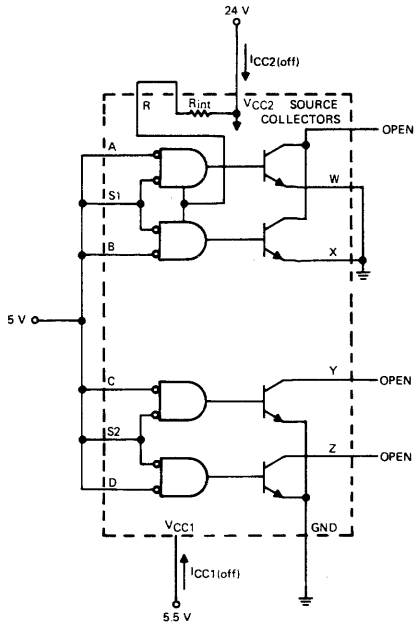
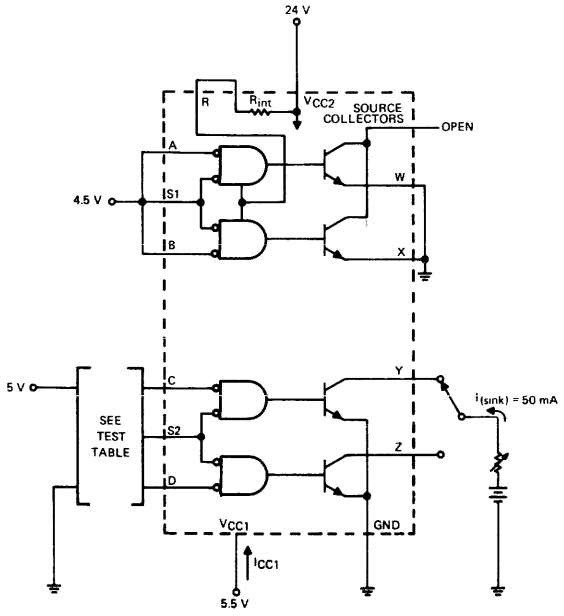


FIGURE 6–$I_{CC1(off)}$ AND $I_{CC2(off)}$

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

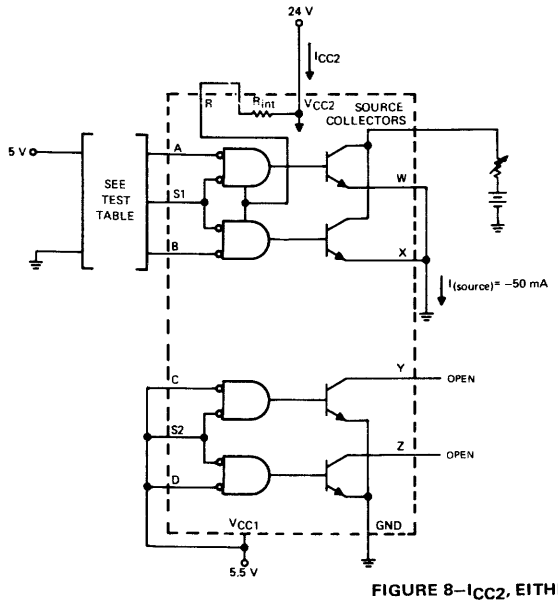
d-c test circuits (continued)†



TEST TABLE

C	D	S2	Y	Z
GND	5 V	GND	$I_{(sink)}$	OPEN
5 V	GND	GND	OPEN	$I_{(sink)}$

FIGURE 7–I_{CC1}, EITHER SINK ON



TEST TABLE

A	B	S1
GND	5 V	GND
5 V	GND	GND

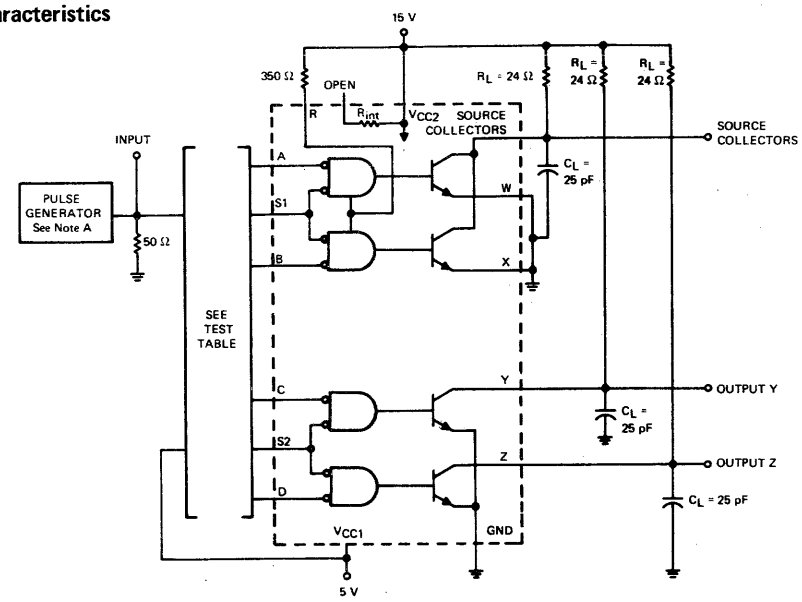
FIGURE 8–I_{CC2}, EITHER SOURCE ON

† Arrows indicate actual direction of current flow.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

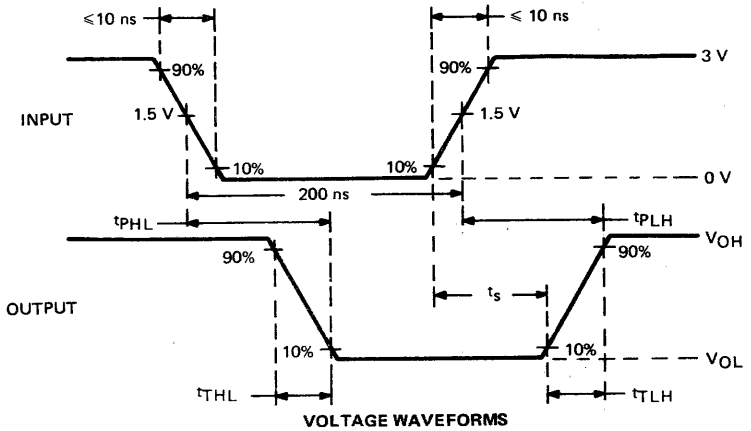
switching characteristics



TEST CIRCUIT

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t_{PLH} and t_{PHL}	Source collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, and t_s	Sink output Y	C and S2	A, B, D and S1
	Sink output Z	D and S2	A, B, C and S1



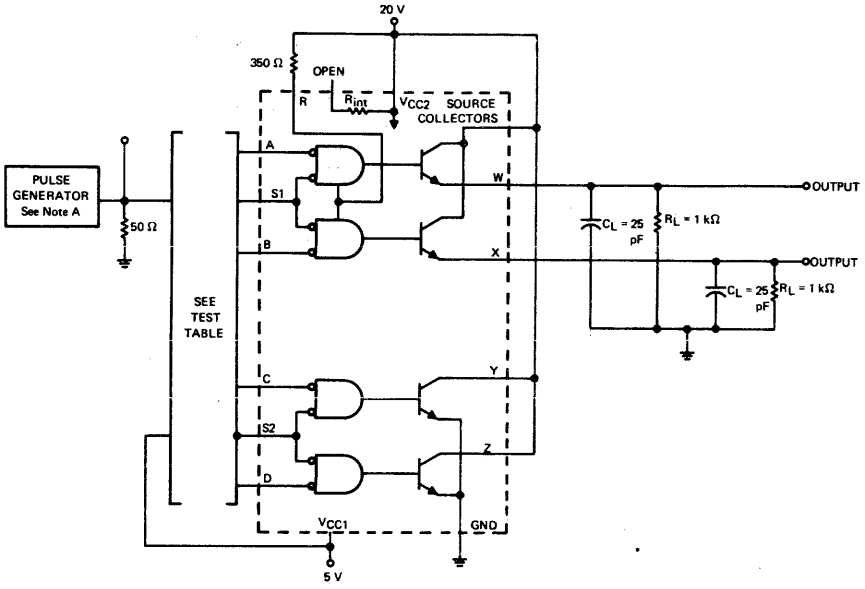
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 1%.
B. C_L includes probe and jig capacitance.

FIGURE 9–SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

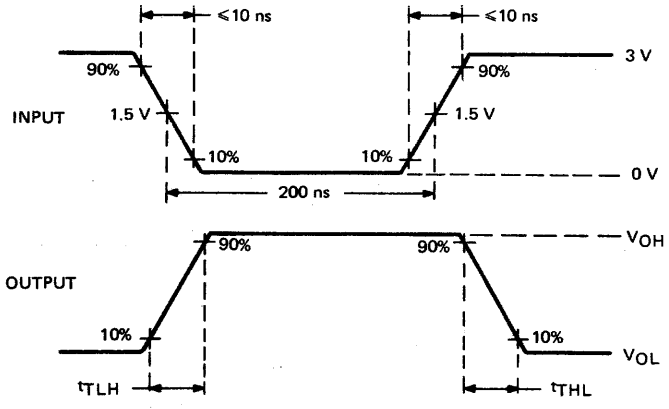
switching characteristics



TEST CIRCUIT

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t_{TLH} and t_{THL}	Source output W	A and S1	B, C, D, and S2
	Source output X	B and S1	A, C, D, and S2



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 1%.
B. C_L includes probe and jig capacitance.

FIGURE 10–TRANSITION TIMES OF SOURCE OUTPUTS

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

OFF-STATE CURRENT INTO SOURCE COLLECTORS
vs
FREE-AIR TEMPERATURE

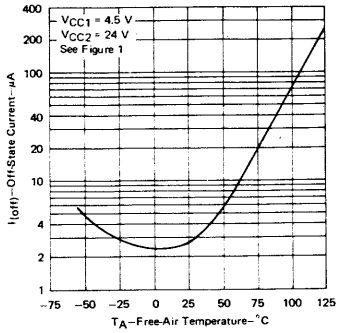


FIGURE 11

HIGH-LEVEL SINK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

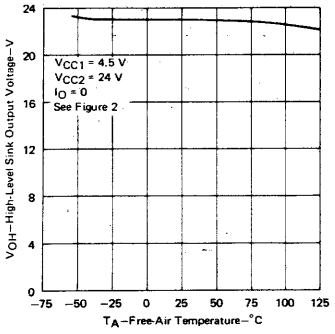


FIGURE 12

SOURCE OR SINK SATURATION VOLTAGE
vs
SOURCE CURRENT OR SINK CURRENT

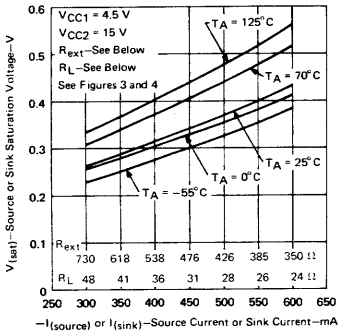


FIGURE 13

SOURCE OR SINK SATURATION VOLTAGE
vs
FREE-AIR TEMPERATURE

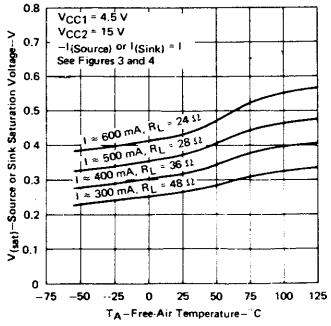


FIGURE 14

SUPPLY CURRENT, ALL SOURCES AND SINKS OFF
vs
FREE-AIR TEMPERATURE

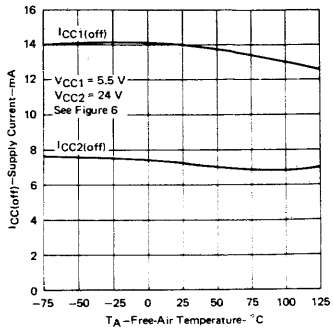
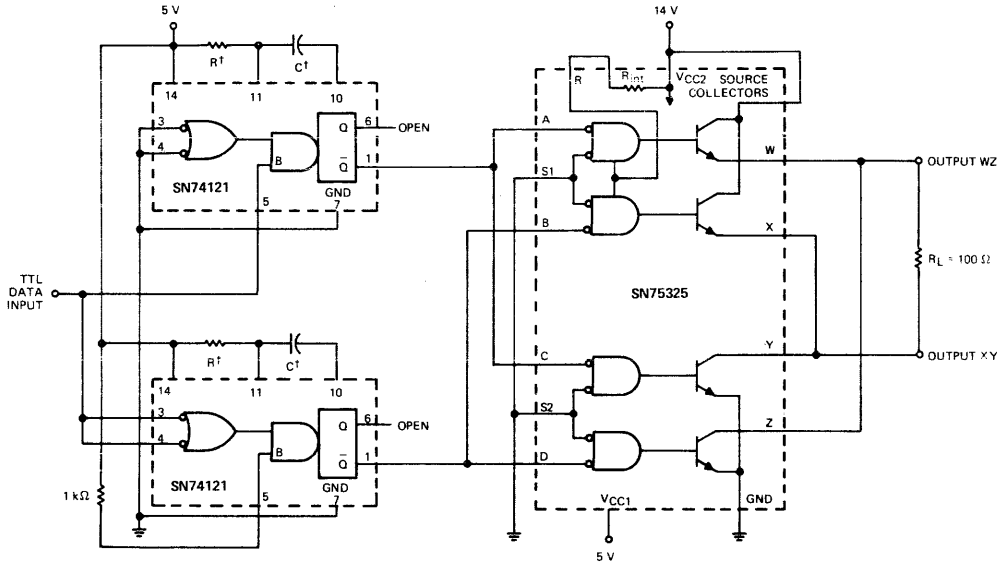


FIGURE 15

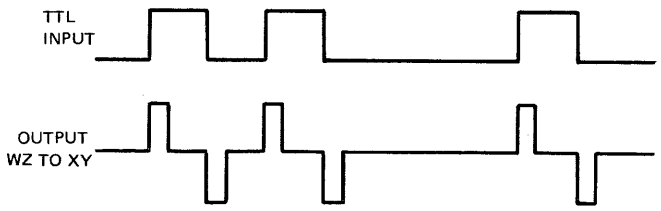
TYPICAL APPLICATION DATA

balanced bipolar logic-line driver

The circuit shown in Figure 16 converts standard TTL logic to bipolar logic. Bipolar logic is primarily used in transmitting data or clock pulses over long lines. This line-driver may be operated from a single 5-volt supply; however, the output drive may be increased by raising the supply voltage to the source collectors. The circuit features a tri-state output which is off during the absence of data, thus not dissipating high power. It provides a balanced drive circuit giving maximum noise immunity when used with the proper line receiver. Large drive levels can be used to further increase noise immunity. The circuit is capable of driving twisted-pair lines of several miles in length or low-impedance coaxial lines.



TEST CIRCUIT



VOLTAGE WAVEFORMS

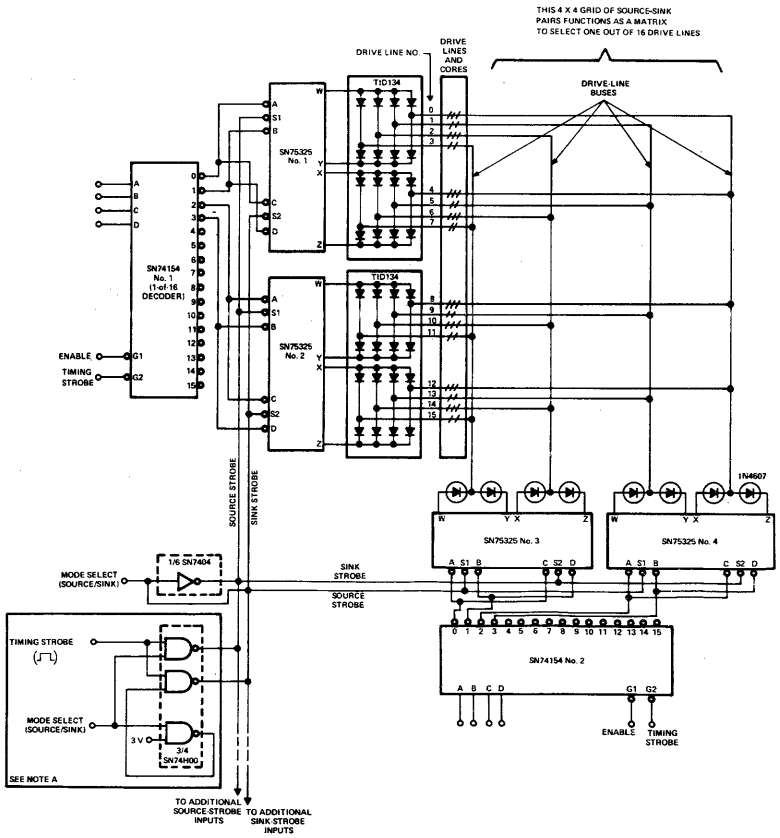
†R and C are adjusted to give the desired bipolar output pulse width.

FIGURE 16–BALANCED BIPOLAR LOGIC–LINE DRIVER

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATION DATA

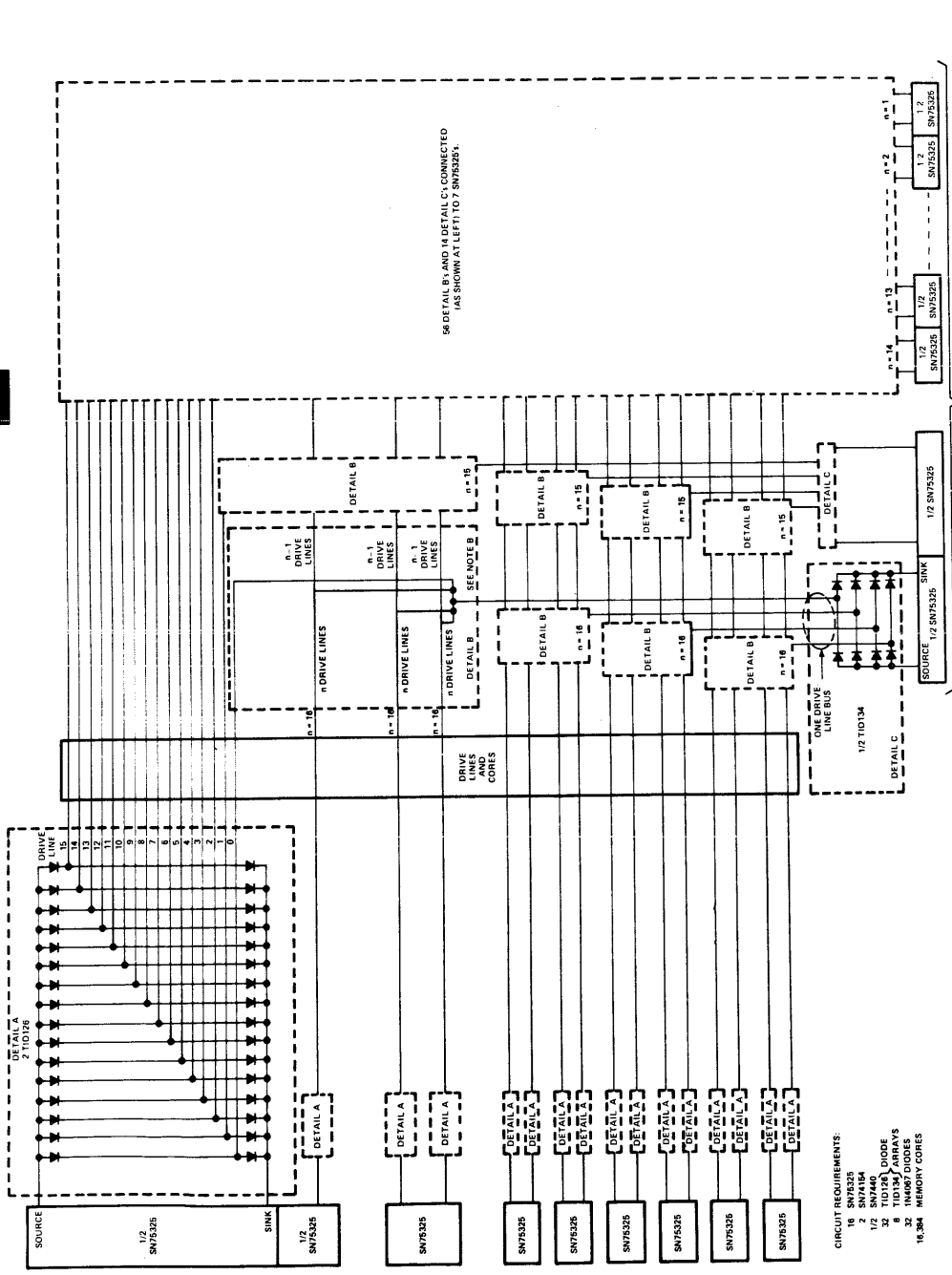
In memory-drive applications the SN75325 (or for full-temperature operation, the SN55325) can be connected in any of several ways. Typically, however, sources and sinks are arranged in pairs from which many drive-lines branch off as shown in Figure 17. Here each drive-line is served by a unique combination of two source/sink pairs so that a selection matrix is formed. To select drive-line 13, SN74154 No. 1 must be set to 3 (with mode select high), enabling source X of SN75325 No. 2 to drive lines 12 through 15, and SN74154 No. 2 must be set to 2, providing a sink at Y of SN75325 No. 4 for drive-line 13 only. Alternatively, to drive current in drive-line 13 in the opposite direction, only the mode-select voltage would be changed from high to low. The size of such a matrix is limited only by the number of drive-lines that a source/sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive-line of the particular system imposes on the driver. A 256-drive-line selection matrix is shown in Figure 18. These 256 drive-lines are sufficient to serve $(256/2)^2 = 16{,}384$ individual cores.



NOTE A: This optional mode-select and timing-strobe technique can be used in place of the SN7440 mode-select and SN74154 timing-strobe when minimum time skew is desired.

FIGURE 17–SN75325 USED AS A MEMORY DRIVER TO SELECT ONE OF SIXTEEN DRIVE LINES

TYPICAL APPLICATION DATA



NOTES: A. Outputs from one SN74154 decoder are connected to each SN75325 as shown in Figure 17. Source strobe and sink strobe from an SN7440 are connected to each SN75325 as shown in Figure 17.
B. The division of the drive-line bus into four segments reduces the capacitive load on the SN75325 driver.

FIGURE 18–SN75325 SERVING 256 DRIVE LINES IN A MAGNETIC MEMORY

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATION DATA

external resistor calculation

A typical magnetic-memory word-drive requirement is shown in Figure 19. A source-output transistor of one SN75325 delivers load current (I_L). The sink-output transistor of another SN75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,[V_{CC2(min)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(min)} - V_S - 2.9]} \qquad \text{(Equation 1)}$$

where: R_{ext} is in kΩ,
$V_{CC2(min)}$ is the lowest expected value of V_{CC2} in volts,
V_S is the source output voltage in volts with respect to ground,
I_L is in mA.

3

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2,

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(min)} - V_S - 2] \qquad \text{(Equation 2)}$$

where: P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3,

$$I_{CS} \approx 0.94\, I_L \qquad \text{(Equation 3)}$$

where: I_{CS} is in mA.

As an example, let $V_{CC2(min)} = 20$ V and $V_L = 3$ V while I_L of 500 mA flows.

Using Equation 1,

$$R_{ext} = \frac{16\ (20 - 3 - 2.2)}{500 - 1.6\ (20 - 3 - 2.9)} = 0.5\ k\Omega$$

and from Equation 2,

$$P_{Rext} \approx \frac{500}{16}\,[20 - 3 - 2] \approx 470\ mW$$

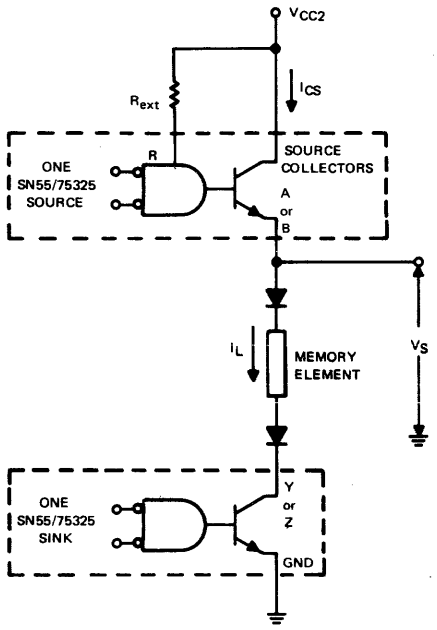
The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\ (500) \approx 470\ mA$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L.

TYPICAL APPLICATION DATA

external resistor calculation (continued)



NOTES: A. For clarity, partial logic diagrams of two SN75325's are shown.
B. Source and sink shown are in different packages.

FIGURE 19

THERMAL INFORMATION

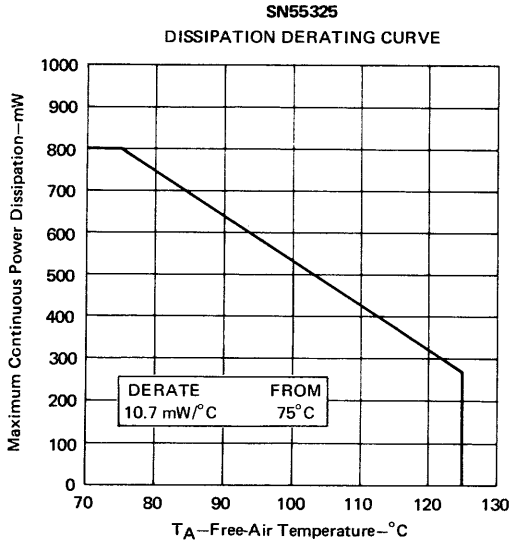


FIGURE 20

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SYSTEMS
INTERFACE CIRCUIT

SERIES 75450
DUAL PERIPHERAL DRIVERS

PERIPHERAL DRIVERS FOR HIGH-CURRENT SWITCHING AT HIGH SPEEDS

performance

- 300-mA Output Current Capability
- High-Voltage Outputs
- High-Speed Switching

ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL or DTL Compatible Diode-Clamped Inputs
- Standard Supply Voltages

SUMMARY OF DUAL DRIVERS

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGE
SN75450A	AND†	N
SN75451A	AND	P
SN75452	NAND	P
SN75453	OR	P
SN75454	NOR	P

†With transistor base connected directly to output of gate.

3

description

Series 75450 dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, and memory drivers. Additionally, the SN75450A may be used as a line driver. The SN75450A and SN75451A are functionally interchangeable with and are recommended for replacement of SN75450 and SN75451, respectively, in most applications which do not require the very high speed of the prototypes. The A-versions offer improved freedom from latch-up and diode-clamped inputs to simplify system design. They can drive lamps, relays, and memories to rated levels of voltage and current without external loading capacitors. Series 75450 drivers are monolithic circuits designed for operation over the temperature range of 0°C to 70°C.

The SN75450A is a unique general-purpose device featuring two standard Series 74 TTL gates and two uncommitted, high-current, high-voltage n-p-n transistors. The SN75450A offers the system designer the flexibility of tailoring the circuit to the application.

The SN75451A, SN75452, SN75453, and SN75454 are dual peripheral AND, NAND, OR, and NOR drivers respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

CONTENTS

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN75450A	SN75451A SN75452 SN75453 SN75454	UNIT
Supply voltage, V_{CC}	7	7	V
Input voltage (see Note 1)	5.5	5.5	V
Interemitter voltage (see Note 2)	5.5	5.5	V
V_{CC}-to-substrate voltage	35		V
Collector-to-substrate voltage	35		V
Collector-base voltage	35		V
Collector-emitter voltage (see Note 3)	30		V
Emitter-base voltage	5		V
Output voltage (see Notes 1 and 4)		30	V
Continuous collector current (see Note 5)	300		mA
Continuous output current (see Note 5)		300	mA
Continuous total power dissipation	800	800	mW
Operating free-air temperature range	0 to 70	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 10 seconds	260	260	°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously.

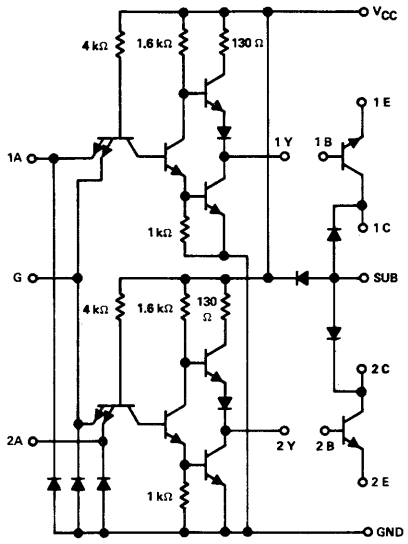
recommended operating conditions (see note 6)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Operating free-air temperature range, T_A	0	25	70	°C

NOTE 6: For the SN75450A only, the substrate (pin 8), must always be at the most-negative device voltage for proper operation.

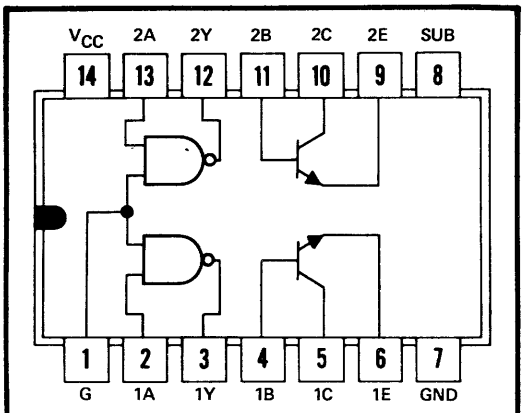
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

schematic



Component values shown are nominal

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TTL gates

PARAMETER			TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage		1		2			V
V_{IL}	Low-level input voltage		2				0.8	V
V_I	Input clamp voltage		3	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		2	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.3		V
V_{OL}	Low-level output voltage		1	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 16 mA		0.22	0.4	V
I_I	Input current at maximum input voltage	input A	4	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
		input G					2	
I_{IH}	High-level input current	input A	4	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
		input G					80	
I_{IL}	Low-level input current	input A	3	V_{CC} = 5.25 V, V_I = 0.4 V			−1.6	mA
		input G					−3.2	
I_{OS}	Short-circuit output current‡		5	V_{CC} = 5.25 V	−18		−55	mA
I_{CCH}	Supply current, high-level output		6	V_{CC} = 5.25 V, V_I = 0		2	4	mA
I_{CCL}	Supply current, low-level output			V_{CC} = 5.25 V, V_I = 5 V		6	11	mA

†All typical values at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE SN75450A
DUAL PERIPHERAL POSITIVE-AND DRIVER

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

output transistors

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA, I_E = 0		35			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C	See Note 7	25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C		30			
		V_{CE} = 3 V, I_C = 100 mA, T_A = 0°C		20			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 0°C		25			
V_{BE}	Base-Emitter Voltage	I_B = 10 mA, I_C = 100 mA	See Note 7		0.85	1	V
		I_B = 30 mA, I_C = 300 mA			1.05	1.2	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 10 mA, I_C = 100 mA	See Note 7		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA			0.5	0.7	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 7: These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TTL gates

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	12	C_L = 15 pF, R_L = 400 Ω		20		ns
t_{PHL}	Propagation delay time, high-to-low-level output				8		ns

output transistors

PARAMETER		TEST FIGURE	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
t_d	Delay time	13	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(off)}$ = −1 V, C_L = 15 pF, R_L = 50 Ω		8		ns
t_r	Rise time				12		ns
t_s	Storage time				7		ns
t_f	Fall time				6		ns

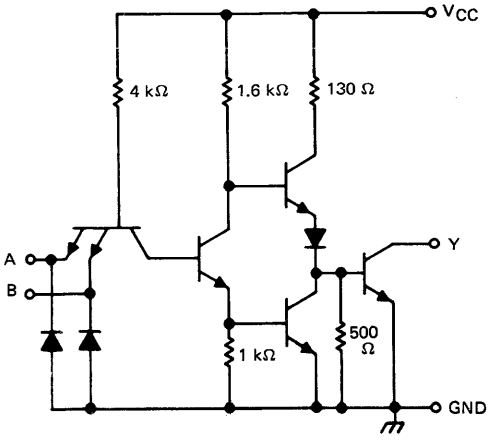
gates and transistors combined

PARAMETER		TEST FIGURE	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	I_C = 200 mA, C_L = 15 pF, R_L = 50 Ω		40		ns
t_{PHL}	Propagation delay time, high-to-low-level output				25		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

schematic (each driver)



Component values shown are nominal

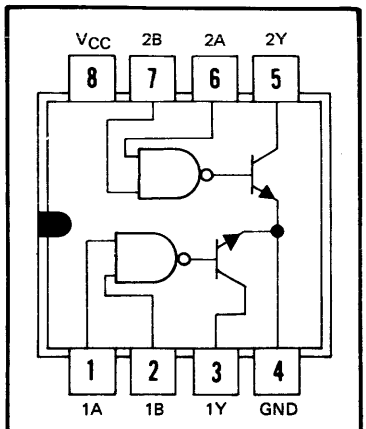
logic

TRUTH TABLE

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

H = high level, L = low level

P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = AB

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	7		2			V
V_{IL}	Low-level input voltage	7				0.8	V
V_I	Input clamp voltage	8	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	7	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 30 V			100	μA
V_{OL}	Low-level output voltage	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	8	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, high-level output	10	V_{CC} = 5.25 V, V_I = 5 V		7	11	mA
I_{CCL}	Supply current, low-level output		V_{CC} = 5.25 V, V_I = 0		52	65	mA

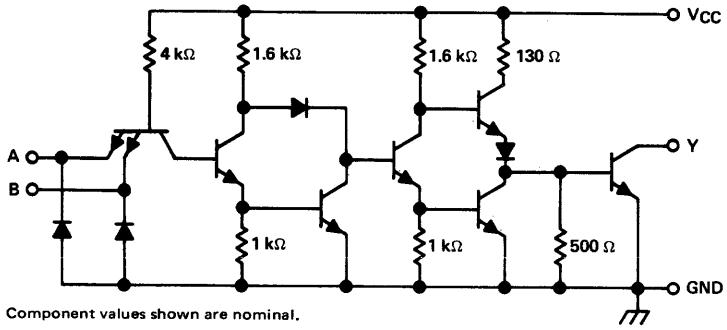
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		45		ns
t_{PHL}	Propagation delay time, high-to-low-level output				25		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

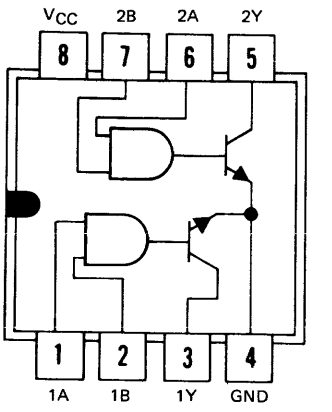
CIRCUIT TYPE SN75452
DUAL PERIPHERAL POSITIVE-NAND DRIVER

schematic (each driver)



Component values shown are nominal.

P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

logic

TRUTH TABLE

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

H = high level L = low level

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	7		2			V
V_{IL}	Low-level input voltage	7				0.8	V
V_I	Input clamp voltage	8	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{OH} = 30 V			100	μA
V_{OL}	Low-level output voltage	7	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	8	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, high-level output	10	V_{CC} = 5.25 V, V_I = 0 V		11	14	mA
I_{CCL}	Supply current, low-level output		V_{CC} = 5.25 V, V_I = 5 V		56	71	mA

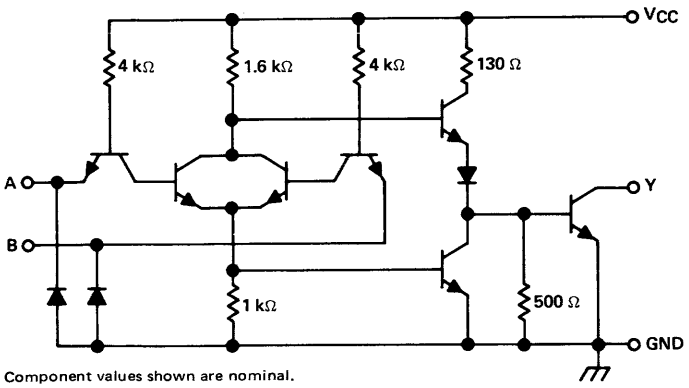
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50		ns
t_{PHL}	Propagation delay time, high-to-low-level output				35		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

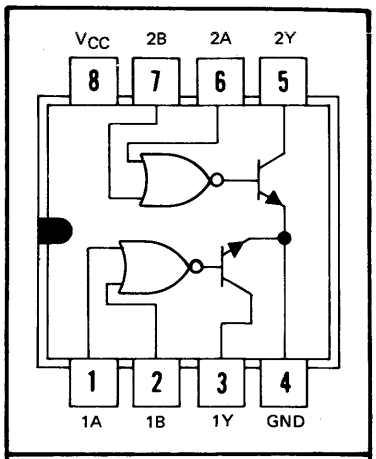
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

schematic (each driver)



Component values shown are nominal.

P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = A + B

logic

TRUTH TABLE

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

H = high level, L = low level

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	7		2			V
V_{IL}	Low-level input voltage	7				0.8	V
V_I	Input clamp voltage	8	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	7	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 30 V			100	μA
V_{OL}	Low-level output voltage	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	8	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, high-level output	11	V_{CC} = 5.25 V, V_I = 5 V		8	11	mA
I_{CCL}	Supply current, low-level output		V_{CC} = 5.25 V, V_I = 0		54	68	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

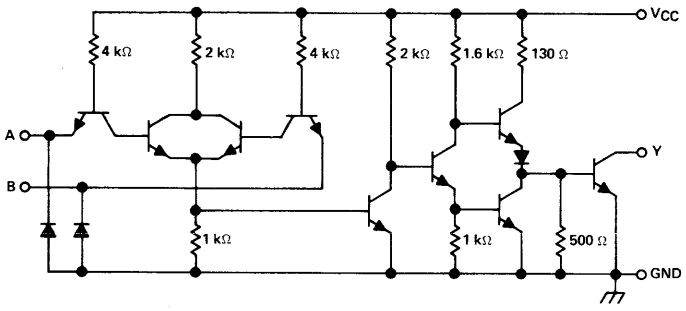
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		35		ns
t_{PHL}	Propagation delay time, high-to-low-level output				25		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

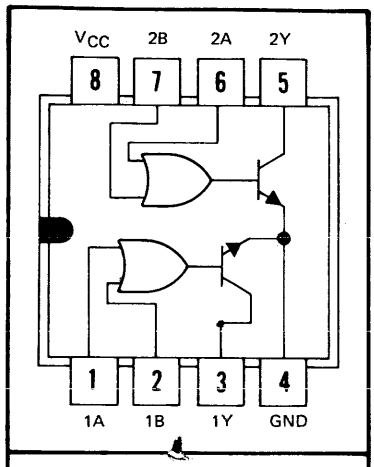
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE SN75454
DUAL PERIPHERAL POSITIVE-NOR DRIVER

schematic (each driver)



P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A + B}$

3

logic

TRUTH TABLE

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

H = high level, L = low level

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	7		2			V
V_{IL}	Low-level input voltage	7				0.8	V
V_I	Input clamp voltage	8	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output voltage	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{OH} = 30 V			100	μA
V_{OL}	Low-level output voltage	7	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	8	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, high-level output	11	V_{CC} = 5.25 V, V_I = 0 V		13	17	mA
I_{CCL}	Supply current, low-level output		V_{CC} = 5.25 V, V_I = 5 V		61	79	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

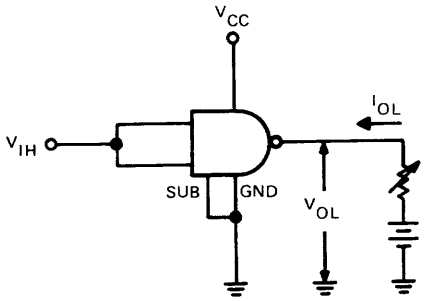
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50		ns
t_{PHL}	Propagation delay time, high-to-low-level output				25		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

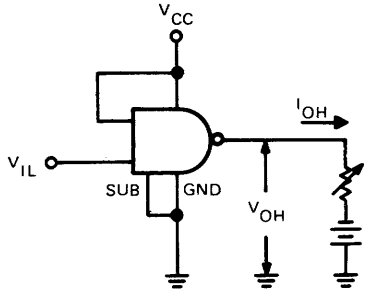
PARAMETER MEASUREMENT INFORMATION

d-c test circuits †



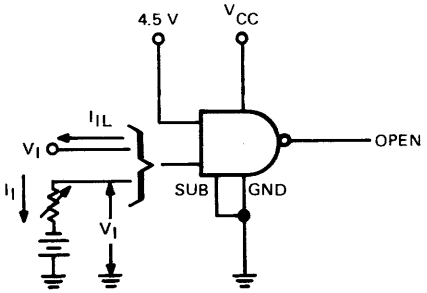
Both inputs are tested simultaneously.

FIGURE 1–V_{IH}, V_{OL}



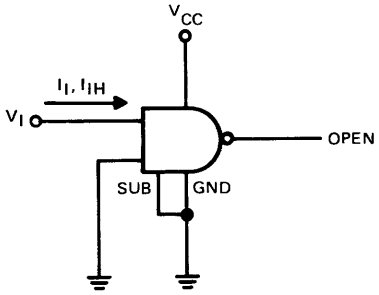
Each input is tested separately.

FIGURE 2–V_{IL}, V_{OH}



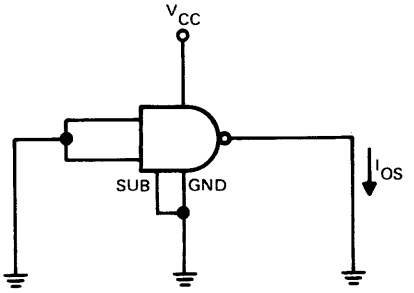
Each input is tested separately.

FIGURE 3–V_I, I_{IL}



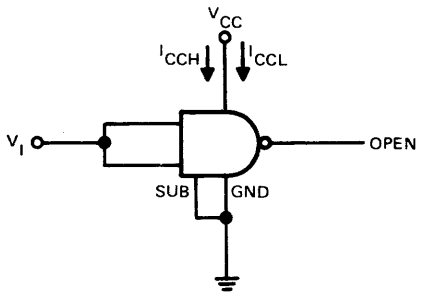
Each input is tested separately.

FIGURE 4–I_I, I_{IH}



Each gate is tested separately.

FIGURE 5–I_{OS}



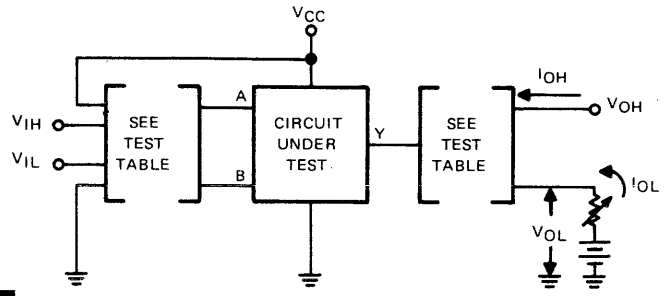
Both gates are tested simultaneously.

FIGURE 6–I_{CCH}, I_{CCL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

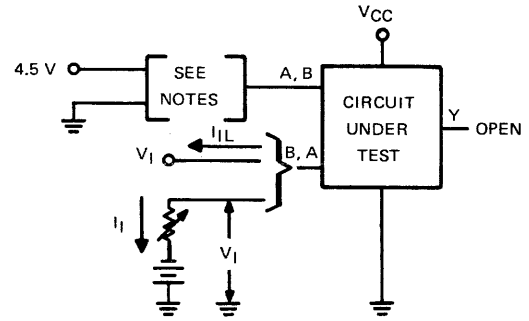


TEST TABLE

CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
SN75451A	V_{IH}	V_{IH}	V_{OH}	I_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
SN75452	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	V_{OH}	I_{OH}
SN75453	V_{IH}	GND	V_{OH}	I_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OL}
SN75454	V_{IH}	GND	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	V_{OH}	I_{OH}

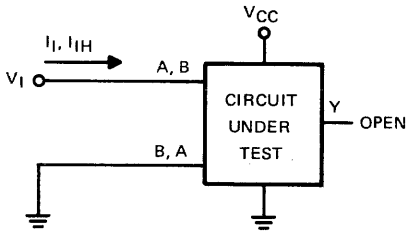
NOTE: Each input is tested separately.

FIGURE 7–V_{IH}, V_{IL}, I_{OH}, V_{OL}



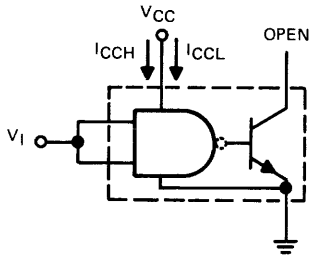
NOTES: A. Each input is tested separately.
B. When testing SN75453 and SN75454, input not under test is grounded. For all other circuits it is at 4.5 V.

FIGURE 8–V_I, I_{IL}



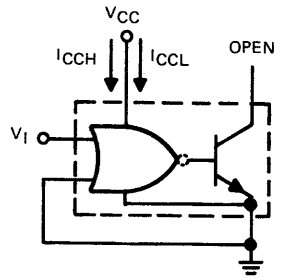
Each input is tested separately.

FIGURE 9–I_I, I_{IH}



Both gates are tested simultaneously.

FIGURE 10–I_{CCH}, I_{CCL} FOR AND, NAND CIRCUITS



Both gates are tested simultaneously.

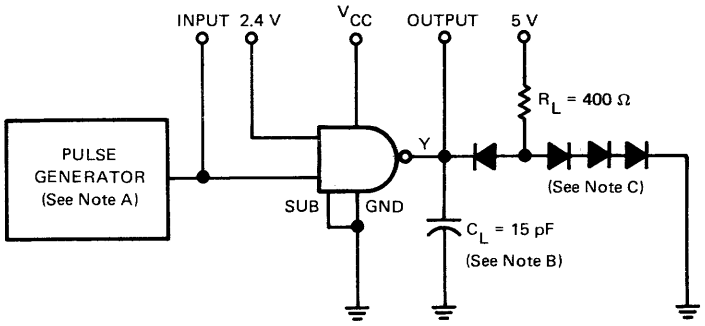
FIGURE 11–I_{CCH}, I_{CCL} FOR OR, NOR CIRCUITS

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

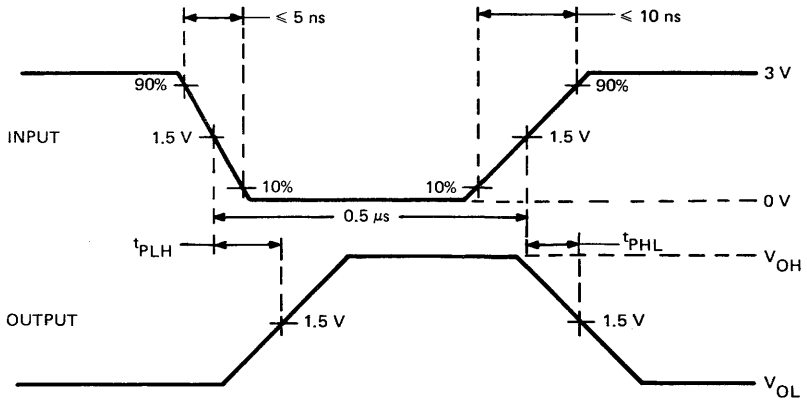
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



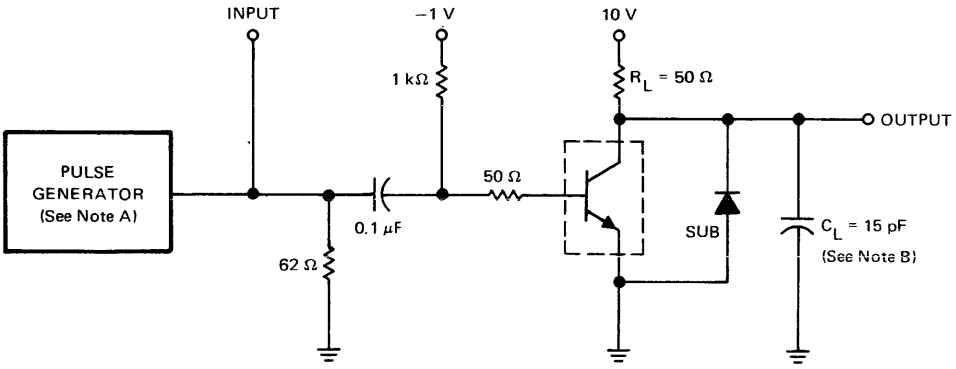
VOLTAGE WAVEFORMS

NOTES. A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. All diodes are 1N3064.

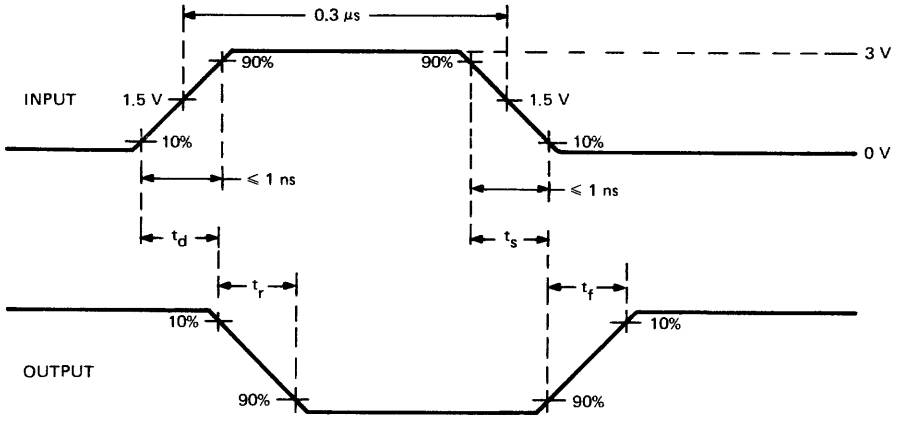
FIGURE 12–PROPAGATION DELAY TIMES, EACH GATE (SN75450A ONLY)

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



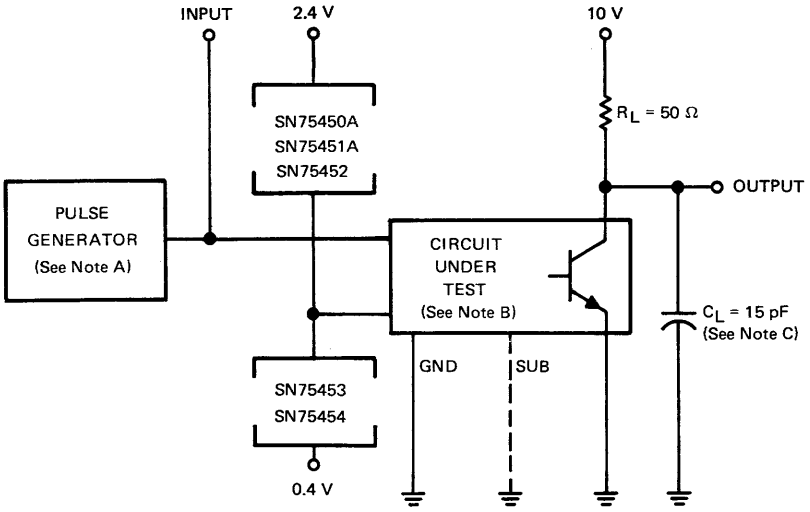
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, Z_{out} ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

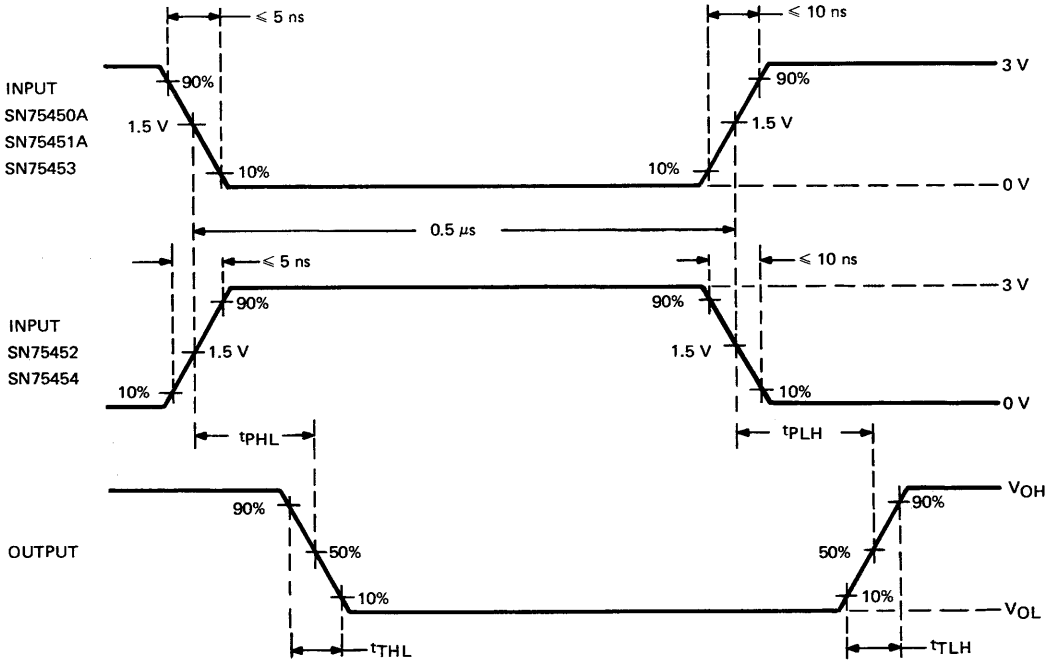
FIGURE 13–SWITCHING TIMES, EACH TRANSISTOR (SN75450A ONLY)

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. When testing SN75450A, connect output Y to transistor base and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

FIGURE 14–SWITCHING TIMES OF COMPLETE DRIVERS

TYPICAL CHARACTERISTICS

SN75450A
TTL GATE
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

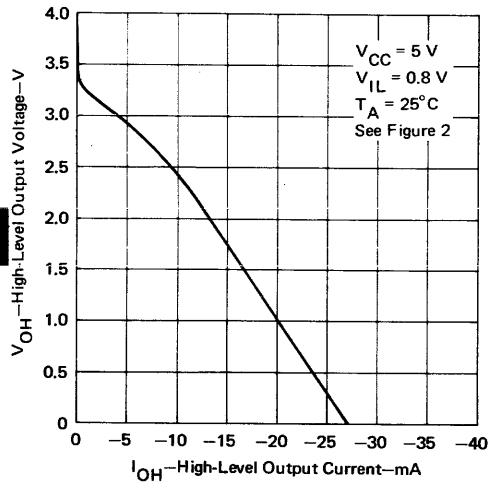


FIGURE 15

SN75450A
TRANSISTOR
STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

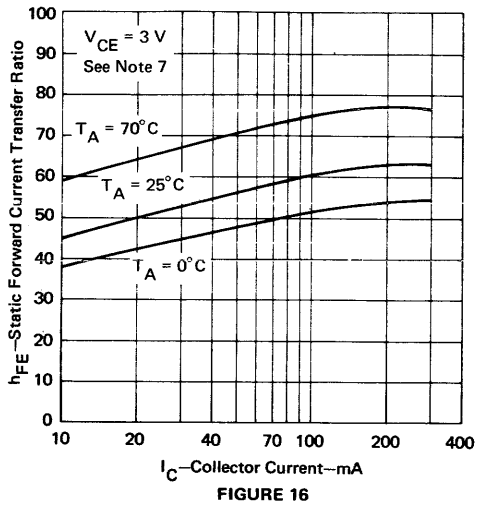


FIGURE 16

SN75450A
TRANSISTOR
BASE-EMITTER VOLTAGE
vs
COLLECTOR CURRENT

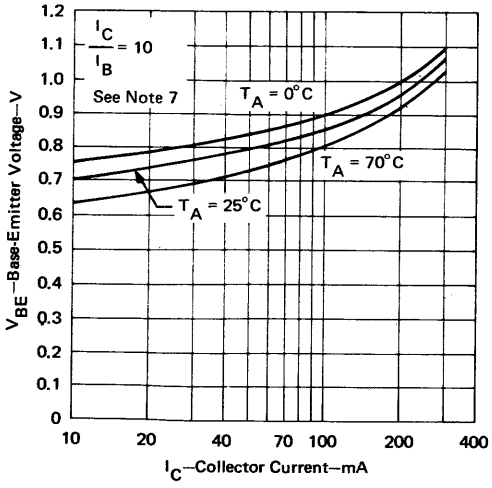


FIGURE 17

TRANSISTOR
COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT

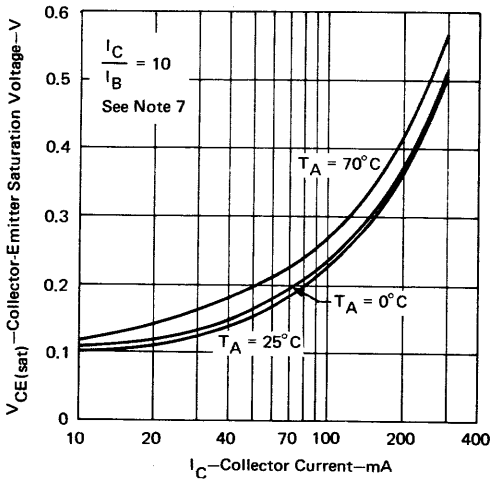
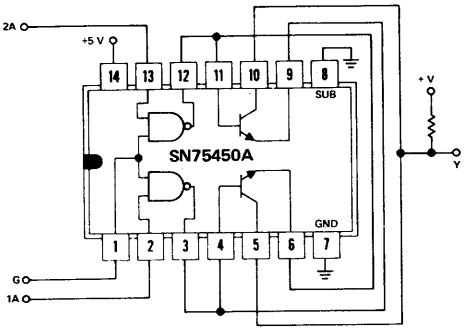


FIGURE 18

NOTE 7: These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATION DATA



$Y = \overline{G} + 1A \cdot 2A + 1\overline{A} \cdot 2\overline{A}$

FIGURE 19–GATED COMPARATOR

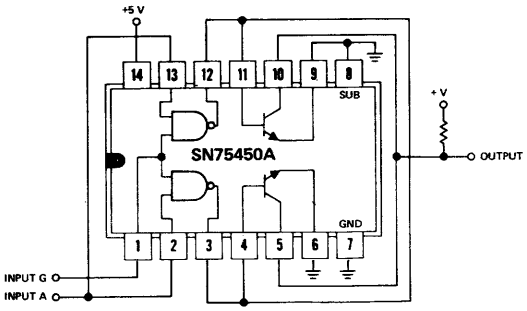


FIGURE 20–500-mA SINK

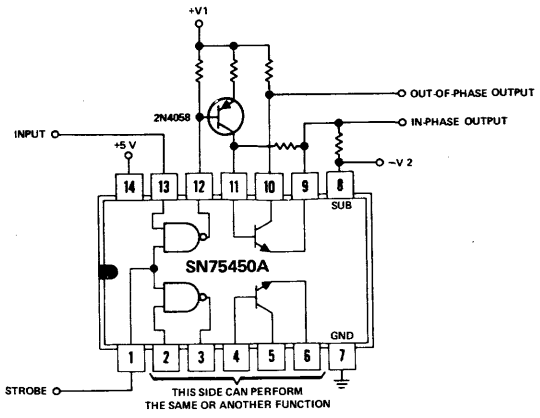


FIGURE 21–FLOATING SWITCH

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATION DATA

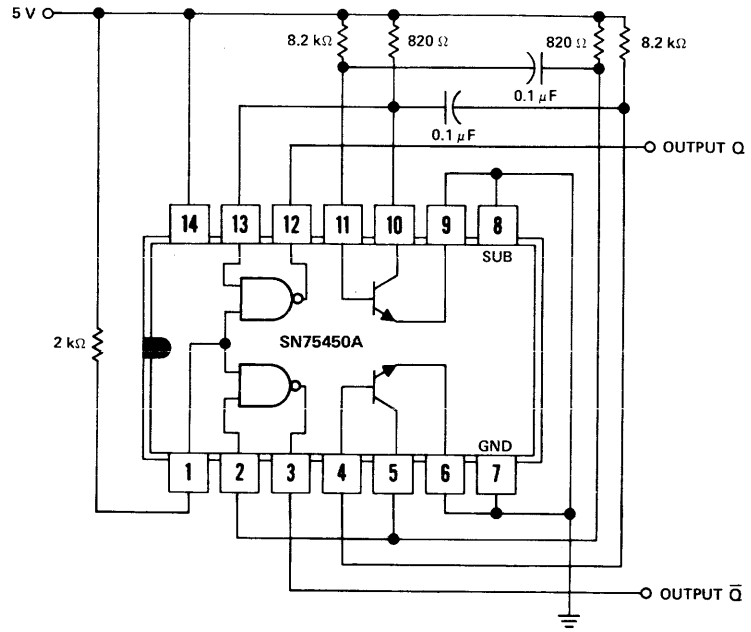
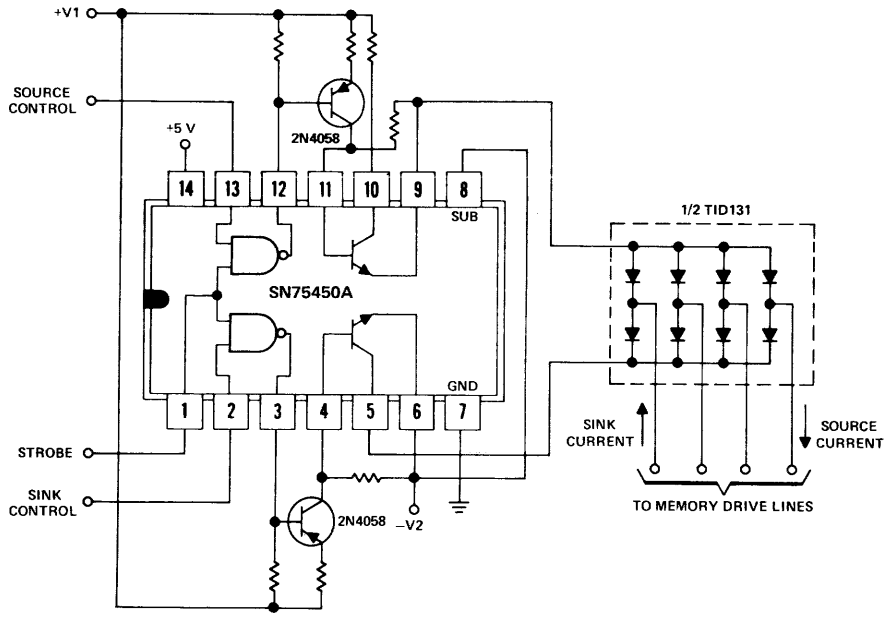


FIGURE 22–SQUARE-WAVE GENERATOR



Source and sink controls are activated by high-level input voltages ($V_{IH} \geq 2V$).

FIGURE 23–CORE MEMORY DRIVER

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATION DATA

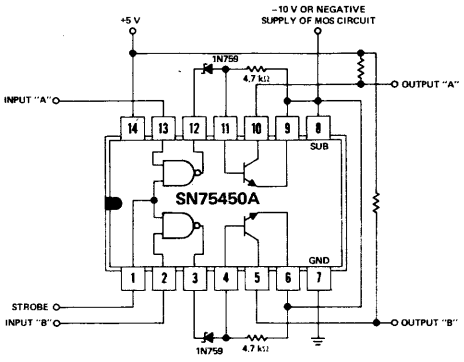


FIGURE 24—DUAL TTL-TO-MOS DRIVER

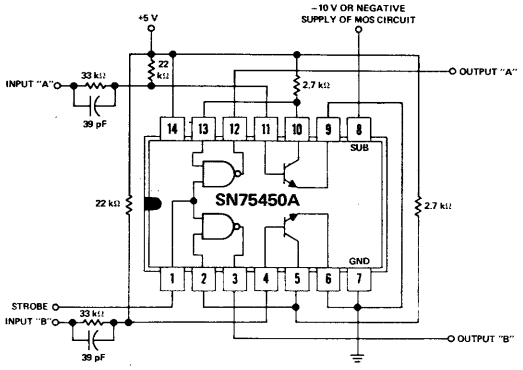
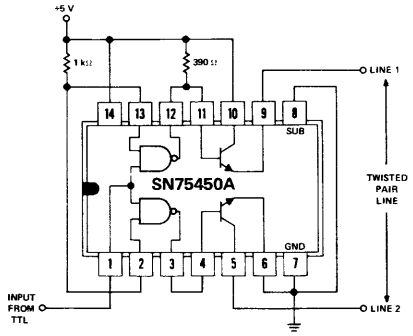
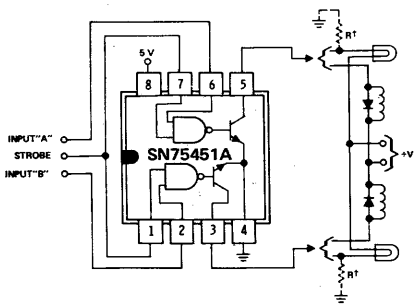


FIGURE 25—DUAL MOS-TO-TTL DRIVER



Termination is made at the receiving end as follows:
Line 1 is terminated to ground through $Z_O/2$;
Line 2 is terminated to +5 volts through $Z_O/2$;
where Z_O is the line impedence.

FIGURE 26—BALANCED LINE DRIVER



† Optional keep-alive resistors maintain off-state lamp current at ≈ 10% to reduce surge current.

FIGURE 27—DUAL LAMP OR RELAY DRIVER

TYPICAL APPLICATION DATA

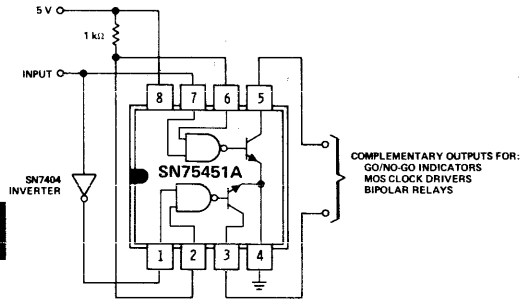


FIGURE 28–COMPLEMENTARY DRIVER

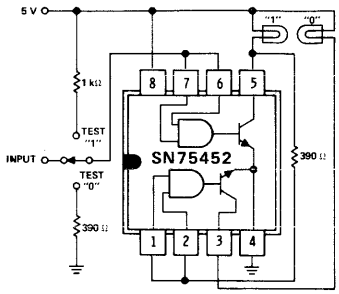
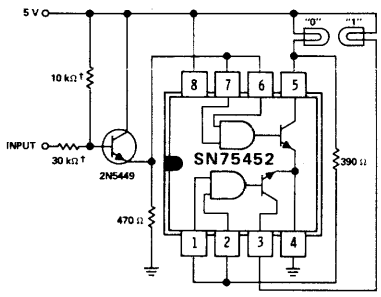


FIGURE 29–TTL OR DTL POSITIVE LOGIC-LEVEL DETECTOR



†The two input resistors must be adjusted for the level of MOS input.

FIGURE 30–MOS NEGATIVE-LOGIC-LEVEL DETECTOR

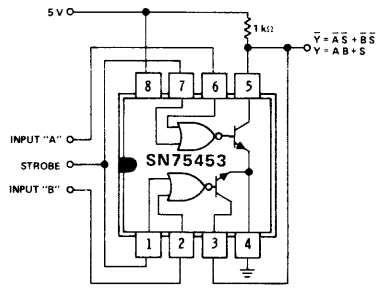
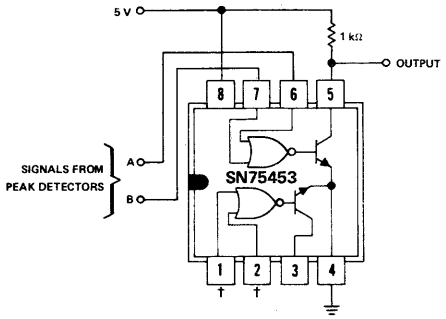
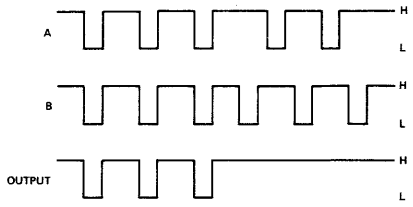


FIGURE 31–LOGIC SIGNAL COMPARATOR

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATION DATA





Low output occurs only when inputs are low simultaneously.

†If inputs are unused, they should be connected to +5 V through a 1 kΩ resistor.

FIGURE 32–IN-PHASE DETECTOR

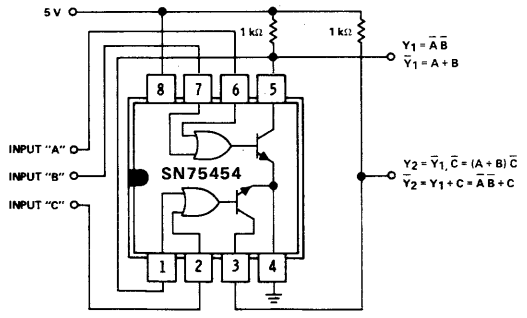


FIGURE 33–MULTIFUNCTION LOGIC-SIGNAL COMPARATOR

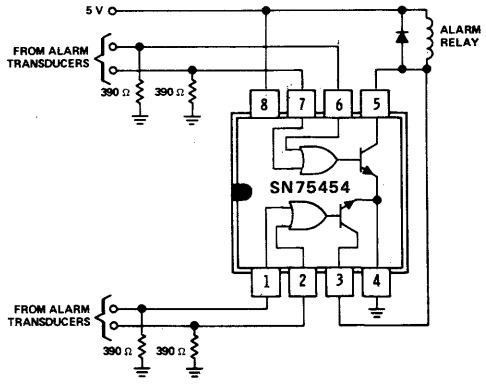


FIGURE 34–ALARM DETECTOR

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES TID21A THRU TID26A, TID29A, TID30A, TID121 THRU TID126, TID129 THRU TID134 EPITAXIAL PLANAR SILICON DIODE ARRAYS

CORE-DRIVER DIODE ARRAYS

For Application With

- Magnetic Cores
- Plated-Wire Memories
- Thin-Film Memories
- Decoding or Encoding Applications

For Use In

- Airborne Computers
- Military Computers
- Industrial Computers
- Peripheral Equipment

description

3

These diode arrays are multiple diode junctions fabricated by a planar process and mounted in integrated circuit packages for use in high-current, fast-switching core-driver applications. These arrays offer many of the advantages of integrated circuits such as high-density packaging and improved reliability. These advantages result from such factors as fewer connections, more uniform device parameters, smaller size, less weight, fewer glass-to-metal seals, and the elimination of pressure contacts and whiskers.

The arrays are available in hermetically sealed, welded flat packages or in dual-in-line plastic packages.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

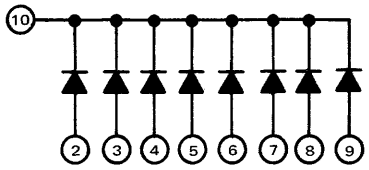
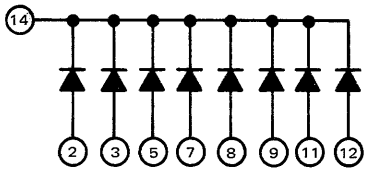
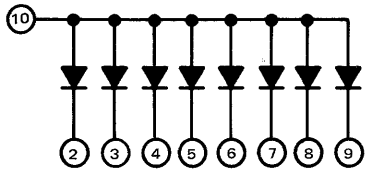
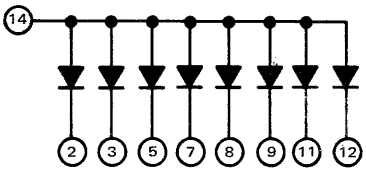
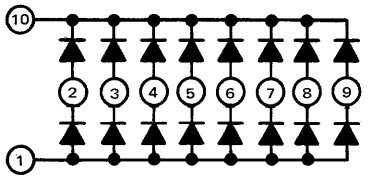
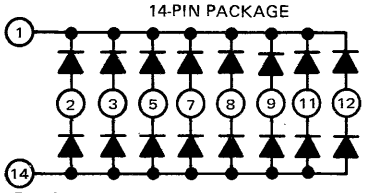
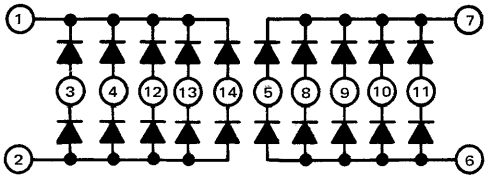
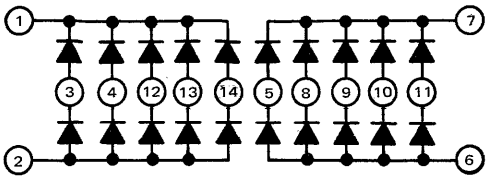
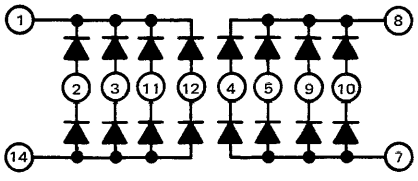
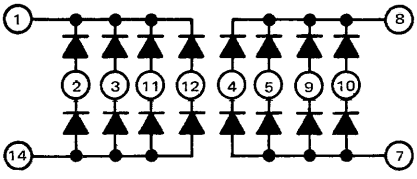
	FLAT PACKAGE			DUAL-IN-LINE PACKAGE			UNIT
	EACH DIODE		TOTAL DEVICE	EACH DIODE		TOTAL DEVICE	
8-DIODE ARRAYS (COMMON CATHODE) 8-DIODE ARRAYS (COMMON ANODE) 16-DIODE ARRAYS DUAL 10-DIODE ARRAYS DUAL 8-DIODE ARRAYS	TID21A TID23A TID25A TID29A TID131	TID22A TID24A TID26A TID30A TID132	ALL TYPES	TID121 TID123 TID125 TID129 TID133	TID122 TID124 TID126 TID130 TID134	ALL TYPES	
Peak Reverse Voltage (See Note 1)	60	40		60	40		V
Steady-State Reverse Voltage, V_R	40	25		40	25		V
Peak Forward Current at (or below) 25°C Free-Air Temperature (See Notes 1 and 2)	500†			500‡			mA
Continuous Forward Current at (or below) 25°C Free-Air Temperature (See Note 2)	300§			400¶			mA
Continuous Power Dissipation at (or below) 25°C Free-Air Temperature			500◇			600□	mW
Operating Free-Air Temperature Range	−65 to 150			−65 to 125			°C
Storage Temperature Range	−65 to 200			−65 to 150			°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	300			260			°C

NOTES: 1. These values apply for 100-μs pulses, duty cycle ⩽ 20%.
2. The values shown for total device apply for any combination provided the ratings of individual diodes are not exceeded.

†Derate linearly to 150°C free-air temperature at the rate of 4 mA/°C.
‡Derate linearly to 125°C free-air temperature at the rate of 5 mA/°C.
§Derate linearly to 150°C free-air temperature at the rate of 2.4 mA/°C.
¶Derate linearly to 125°C free-air temperature at the rate of 4 mA/°C.
◇Derate linearly to 150°C free-air temperature at the rate of 4 mW/°C.
□Derate linearly to 125°C free-air temperature at the rate of 6 mW/°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES TID21A THRU TID26A, TID29A, TID30A, TID121 THRU TID126, TID129 THRU TID134 EPITAXIAL PLANAR SILICON DIODE ARRAYS

FLAT PACKAGES	14-PIN PLASTIC DUAL-IN-LINE PACKAGES
TID21A, TID22A 8-DIODE ARRAY (COMMON CATHODE) 10-PIN PACKAGE  (1) No internal connection	**TID121, TID122** 8-DIODE ARRAY (COMMON CATHODE) 14-PIN PACKAGE  (1) (4) (6) (10) (13) No internal connection
TID23A, TID24A 8-DIODE ARRAY (COMMON ANODE) 10-PIN PACKAGE  (1) No internal connection	**TID123, TID124** 8-DIODE ARRAY (COMMON ANODE) 14-PIN PACKAGE  (1) (4) (6) (10) (13) No internal connection
TID25A, TID26A 16-DIODE ARRAY 10-PIN PACKAGE 	**TID125, TID126** 16-DIODE ARRAY 14-PIN PACKAGE  (4) (6) (10) (13) No internal connection
TID29A, TID30A DUAL 10-DIODE ARRAY 14-PIN PACKAGE 	**TID129, TID130** DUAL 10-DIODE ARRAY 14-PIN PACKAGE 
TID131, TID132 DUAL 8-DIODE ARRAY 14-PIN PACKAGE  (6) (13) No internal connection	**TID133, TID134** DUAL 8-DIODE ARRAY 14-PIN PACKAGE  (6) (13) No internal connection

3

electrical characteristics at 25°C free-air temperature

single-diode operation (see note 3)

PARAMETER		TEST CONDITIONS	TID21A TID121		TID22A TID122		TID23A TID25A TID29A TID123 TID125 TID129 TID131 TID133		TID24A TID26A TID30A TID124 TID126 TID130 TID132 TID134		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)}$	Reverse Breakdown Voltage	I_R = 10 μA	60		40		60		40		V
I_R	Static Reverse Current	V_R = 40 V, See Note 4		0.1				0.1			μA
		V_R = 25 V, See Note 4				0.1				0.1	μA
V_F	Static Forward Voltage	I_F = 100 mA		1		1.1		1		1.1	V
v_F	Instantaneous Forward Voltage	I_F = 500 mA, See Note 5		1.3		1.5		1.3		1.5	V
V_{FM}	Peak Forward Voltage	I_F = 500 mA, See Note 6		5		5		5		5	V
C_T	Total Capacitance†	V_R = 0, f = 1 MHz		4		4		8		8	pF

multiple-diode operation (see note 7)

PARAMETER		TEST CONDITIONS	ALL TYPES		UNIT
			MIN	MAX	
I_{R1}	Static Reverse Current	V_{R1} = rated V_R, I_{FN} = 25 mA		10	μA
V_{F1}	Static Forward Voltage	$I_{F1} = I_{FN}$ = 25 mA		1	V

switching characteristics at 25°C free-air temperature

single-diode operation (see note 3)

PARAMETER		TEST CONDITIONS	ALL TYPES		UNIT
			MIN	MAX	
t_{fr}	Forward Recovery Time	I_F = 500 mA, See Figure 3		40	ns
t_{rr}	Reverse Recovery Time	I_F = 200 mA, I_{RM} = 200 mA, R_L = 100 Ω, i_{rr} = 20 mA, See Figure 4		20	ns

NOTES: 3. Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics except for the measurement of I_R on arrays having both common-cathode and common-anode diodes (see Figures 1 and 2).

4. For arrays having both common-anode and common-cathode diodes see Figures 1 and 2, Parameter Measurement Information section.

5. This parameter is measured using pulse techniques. t_w = 300 μs, duty cycle = 2 %. Read time is 90 μs from the leading edge of the pulse.

6. The initial instantaneous value is measured using pulse techniques. t_w = 150 ns, duty cycle ⩽ 2%, pulse rise time ⩽ 10 ns. The total diode shunt capacitance is 19 pF maximum and the equipment bandwidth is 80 MHz.

7. Subscript numeral 1 refers to the diode under test; subscript N refers simultaneously to each of the other diodes in the section. Each diode is individually tested after the device reaches operating thermal equilibrium. Test conditions apply separately to common-anode and common-cathode sections.

†C_T is the total pin-to-pin capacitance measured across any of the diodes. For arrays having both common-anode and common-cathode sections, the interaction of the other diodes cannot easily be separated out unless three-terminal guarded measurement techniques are used. The actual capacitance of a single isolated diode will typically be 30% of the measured pin-to-pin value for the common-cathode diodes, and 75% of the measured value for the common-anode diodes.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

When measuring the reverse current of an individual diode of a device having both common-anode and common-cathode sections, the current meter must be placed so that the shunt current through the other diodes is bypassed around the meter to obtain accurate readings, the voltage drop across the current meter must be less than 10 mV.

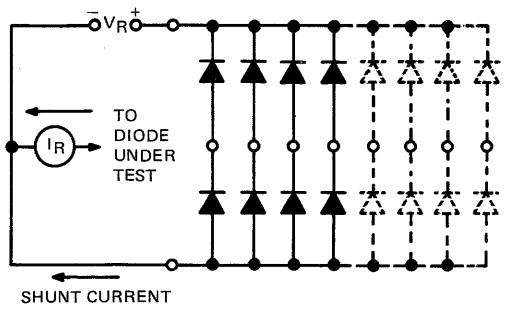


FIGURE 1–TEST CIRCUIT FOR COMMON-CATHODE DIODES

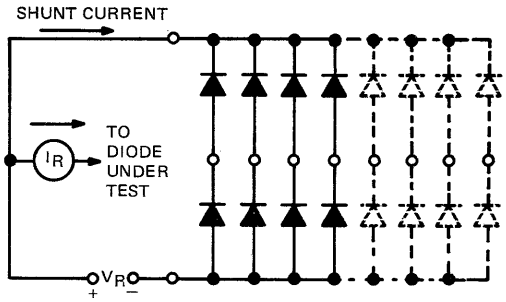
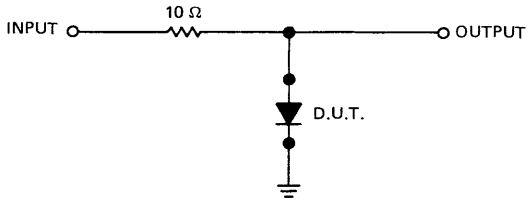
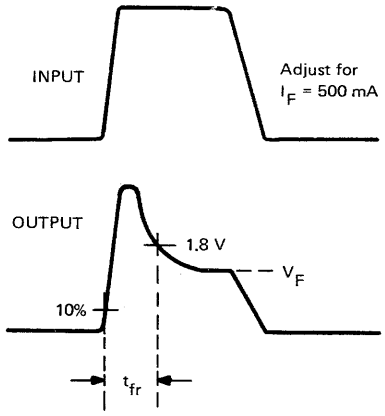


FIGURE 2–TEST CIRCUIT FOR COMMON-ANODE DIODES



TEST CIRCUIT



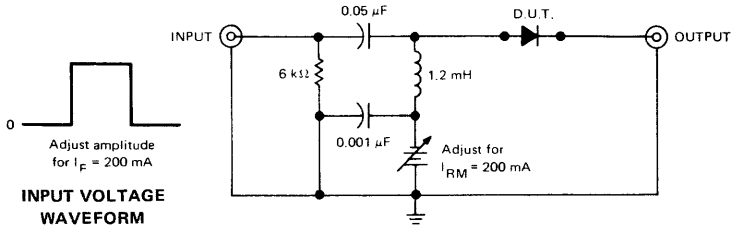
VOLTAGE WAVEFORMS

FIGURE 3–FORWARD RECOVERY TIME

NOTES: a. The input pulse is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $Z_{out} = 50\ \Omega$, $t_w = 150$ ns, duty cycle $\leq 2\%$.

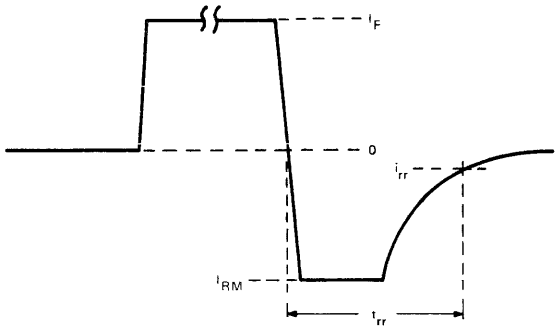
b. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq 4.5$ ns, $R_{in} \geq 1\ M\Omega$, $C_{in} \leq 5$ pF.

PARAMETER MEASUREMENT INFORMATION



INPUT VOLTAGE WAVEFORM

TEST CIRCUIT



OUTPUT CURRENT WAVEFORM

FIGURE 4—REVERSE RECOVERY TIME

NOTES: c. The input pulse is supplied by a generator with the following characteristics: $t_f \leq 1$ ns, $Z_{out} = 50\ \Omega$, $t_w = 200$ ns, duty cycle ≤ 1%.

d. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq 0.4$ ns, $R_{in} = 50\ \Omega$.

TYPICAL CHARACTERISTICS

FORWARD CONDUCTION CHARACTERISTICS

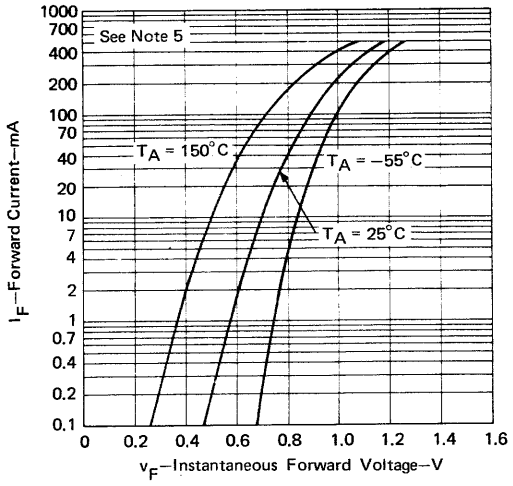


FIGURE 5

NOTE 5: This parameter is measured using pulse techniques. $t_w = 300\ \mu s$, duty cycle = 2%. Read time is 90 μs from the leading edge of the pulse.

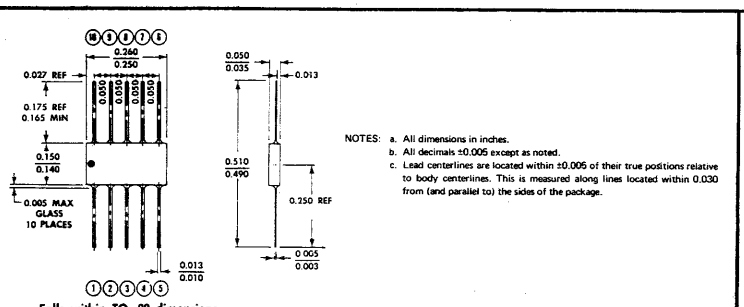
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MECHANICAL DATA

flat packages

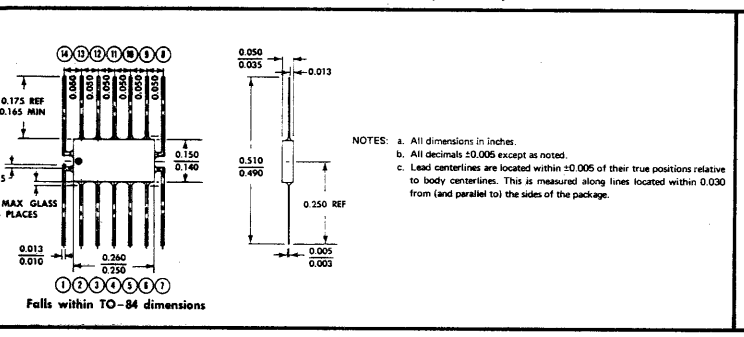
These hermetic packages feature glass-to-metal seals and welded construction in 10-pin and 14-pin configurations. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic.

TID21A, TID22A, TID23A, TID24A, TID25A, TID26A



NOTES: a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines. This is measured along lines located within 0.030 from (and parallel to) the sides of the package.

TID29A, TID30A, TID131, TID132

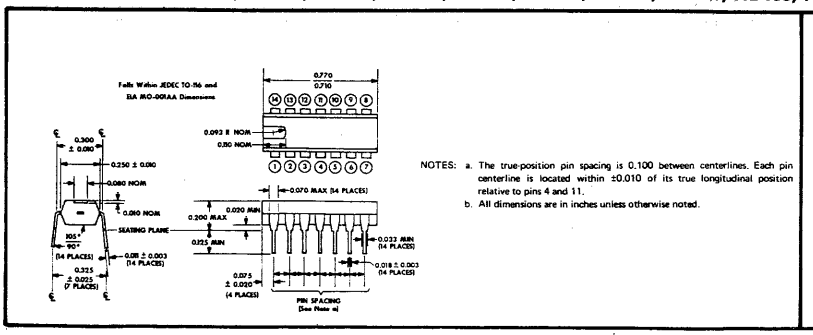


NOTES: a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines. This is measured along lines located within 0.030 from (and parallel to) the sides of the package.

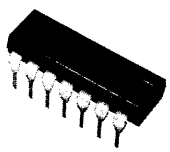
plastic dual-in-line package

The compound used to mold the dual-in-line package will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. The silver-plated leads require no additional cleaning or processing when used in soldered assembly.

TID121, TID122, TID123, TID124, TID125, TID126, TID129, TID130, TID133, TID134



NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 4 and 11.
b. All dimensions are in inches unless otherwise noted.



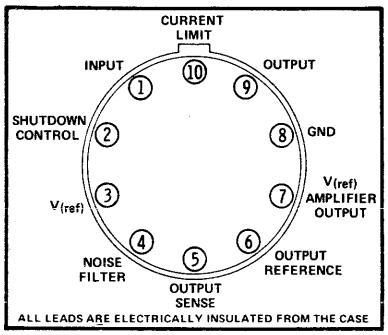
‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

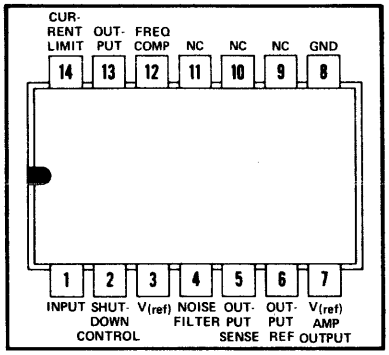
CIRCUIT TYPE SN72400
VOLTAGE REGULATOR

- 200-mA Load Current without External Power Transistor
- Remote Shutdown Control
- Adjustable Short-Circuit Current Limiter
- Input Voltages to 40 Volts
- Output Adjustable from 2 to 37 Volts

L
PLUG-IN PACKAGE (TOP VIEW)



N
DUAL-IN-LINE PACKAGE (TOP VIEW)



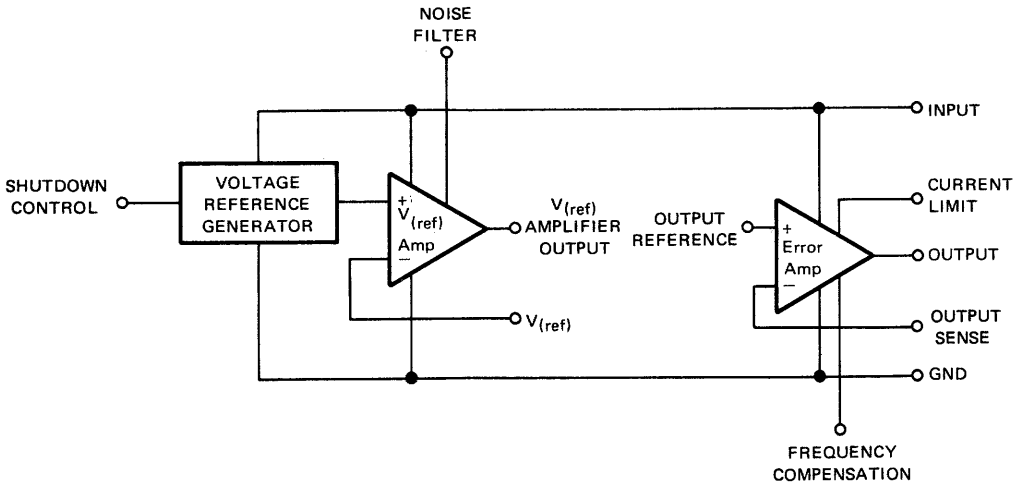
NC—No internal connection

description

The SN72400 voltage regulator is a monolithic integrated circuit featuring a versatile circuit configuration and excellent performance specifications. A temperature-compensated power supply may be constructed by the addition of only two resistors to set the desired output voltage and two capacitors.

The circuit consists of a temperature-compensated reference voltage generator, a reference voltage amplifier, an error amplifier, a 200-milliampere output transistor, a remote shutdown circuit, and an adjustable output current limiter. The device features high ripple rejection, excellent input and load regulation, low temperature sensitivity, and low standby current. The SN72400 is designed for use in positive or negative power supplies as a series, shunt, switching, or floating regulator.

functional block diagram



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input voltage (see Note 1)	40 V
Input-output voltage differential	40 V
Load current	200 mA
$V_{(ref)}$ amplifier output current	5 mA
Shutdown control voltage (see Notes 1 and 2)	V_I or 10 V
Power dissipation at (or below) 50°C free-air temperature (see Note 3)	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds, L package	300°C
Lead temperature 1/16 inch from case for 10 seconds, N package	260°C

NOTES: 1. Voltage values, except input-output voltage differential, are with respect to the network ground terminal.
2. The shutdown control voltage must never exceed the amount of the input voltage or 10 volts, whichever is less.
3. Power dissipation = $(I_I - I_O)\,V_I + (V_I - V_O)\,I_O$. For devices in the L package operating above 50°C free-air temperature, derate linearly at the rate of 8 mW/°C. No derating is required for devices in the N package.

3

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	8.5	40	V
Output voltage, V_O	2	37	V
Input-to-output voltage differential, $V_I - V_O$	3		V
Output current, I_O	1	200	mA
Operating free-air temperature, T_A	0	70	°C

electrical characteristics (unless otherwise noted, T_A = 25°C, see Note 4)

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input regulation	1	$V_O \approx 5$ V, I_O = 1 mA, V_I = 12 V to 15 V		0.03%	0.1%	
Ripple rejection	3	Ripple frequency = 50 Hz to 10 kHz		60		dB
Load regulation	4	V_I = 15 V, $V_O \approx 10$ V, I_O = 1 mA to 50 mA, T_A = 0°C to 70°C, See Note 5		−0.03%	−0.1%	
Reference voltage, $V_{(ref)}$	1 or 2		2.1	2.3	2.5	V
Standby current	1	V_I = 40 V, I_O = 0		3	8	mA
Temperature coefficient of output voltage	1	T_A = 0°C to 70°C		±0.002		%/°C
Short-circuit output current	1 or 2	R_L = 0, R_{SC} = 7 Ω		91		mA
Output impedance	5	V_I = 14 V, f = 10 kHz		0.02		Ω
Output noise voltage	1	R1 = 0 Ω ($V_O \approx V_{(ref)}$), BW = 10 Hz to 5 MHz		0.1		mV
Minimum shutdown control voltage	6	V_I = 40 V, $I_O \leq 150\,\mu$A			2.4	V
Shutdown control current	6	V_I = 40 V, Shutdown control at 2.4 V		0.8	1.5	mA

NOTES: 4. Unless otherwise specified, V_I = 12 V, V_O = 8 V, I_O = 10 mA, C_N = 0.1 μF.
5. Load regulation is measured using pulsed techniques (t_w = 150 μs, duty cycle = 5%) to limit changes in internal power dissipation. Output voltage drift due to large changes in internal power dissipation must be taken into account separately.

CIRCUIT TYPE SN72400
VOLTAGE REGULATOR

DEFINITION OF TERMS

Input Regulation The percentage change in the output voltage for a specified change in the input voltage.

$$\text{Input Regulation} = \left[\frac{\Delta V_O}{V_O \text{ at } V_I = 12\text{ V}}\right] 100\%$$

Ripple Rejection The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Load Regulation The percentage change in the output voltage for a specified change in output current.

$$\text{Load Regulation} = \left(\frac{V_O \text{ at } I_{O(2)} - V_O \text{ at } I_{O(1)}}{V_O \text{ at } I_{O(1)}}\right) 100\%$$

where $I_{O(1)}$ and $I_{O(2)}$ are the specified low and high current extremes, respectively.

Standby Current The input current to the regulator with no load current.

3

Temperature Coefficient of Output Voltage (αV_O) The ratio of the difference between the highest and lowest values of output voltage for the full temperature range to the output voltage at 25°C, expressed as a percentage and averaged over the full temperature range.

$$\alpha V_O = \pm \left[\frac{V_O \text{ max} - V_O \text{ min}}{V_O \text{ at } 25^\circ\text{C}}\right] \frac{100\%}{70^\circ\text{C}}$$

Short-Circuit Output Current The output current of the regulator with the output shorted to ground.

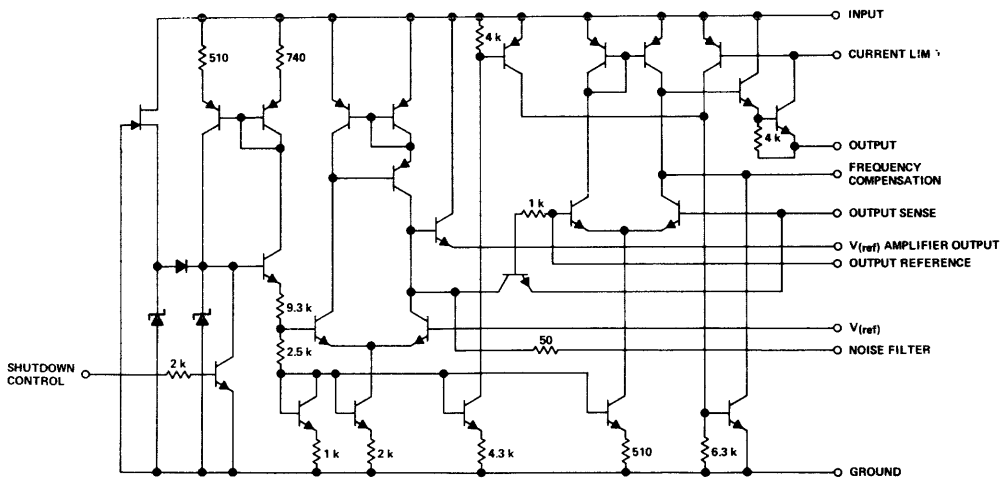
Output Impedance The ratio of a-c rms output voltage to the a-c rms output current.

Output Noise Voltage The rms output noise voltage with a constant load and no input ripple.

Minimum Shutdown Control Voltage The lowest voltage at the shutdown control terminal which will cause the regulator output current to decrease to below a specified value.

Shutdown Control Current The current into the shutdown control terminal.

schematic



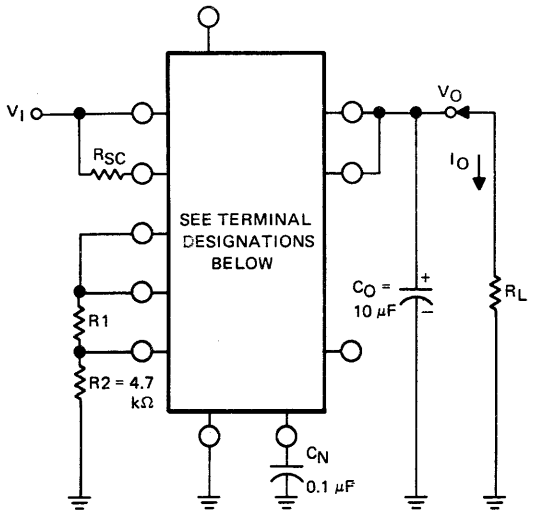
All resistor values are nominal in ohms.

NOTE: The frequency compensation terminal is not available on devices in the 10-pin plug-in package (outline L).

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

BASIC REGULATOR CONFIGURATION FOR $V_{(ref)} \leq V_O \leq 37$ V



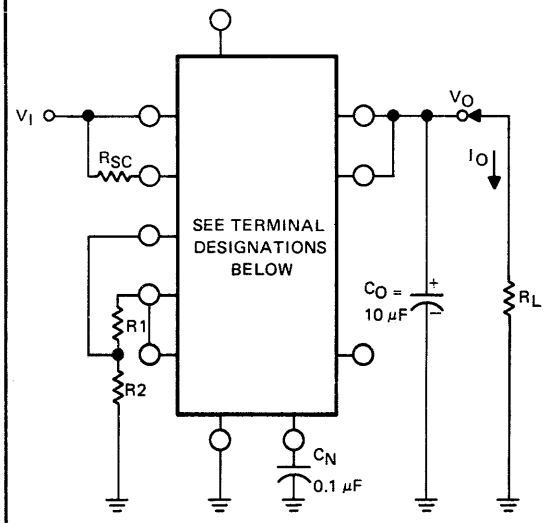
$$V_O = \frac{R1 + R2}{R2} V_{(ref)}$$

For $V_{(ref)}$ = 2.35 V and R2 = 4.7 kΩ:

$$R1 = (2 \frac{k\Omega}{V}) V_O - 4.7\ k\Omega$$

FIGURE 1

BASIC REGULATOR CONFIGURATION FOR 2 V $\leq V_O \leq V_{(ref)}$



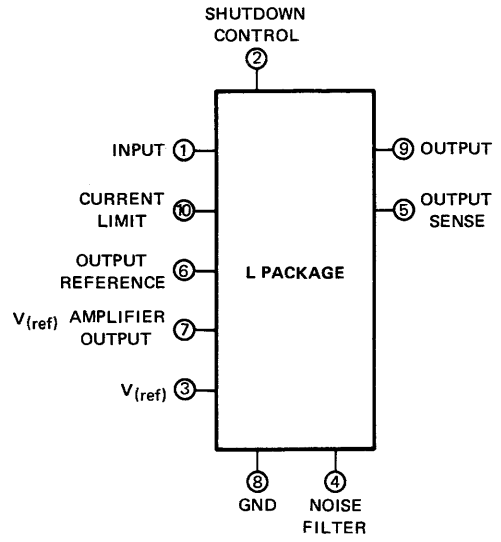
$$V_O = \frac{R2}{R1 + R2} V_{(ref)}$$

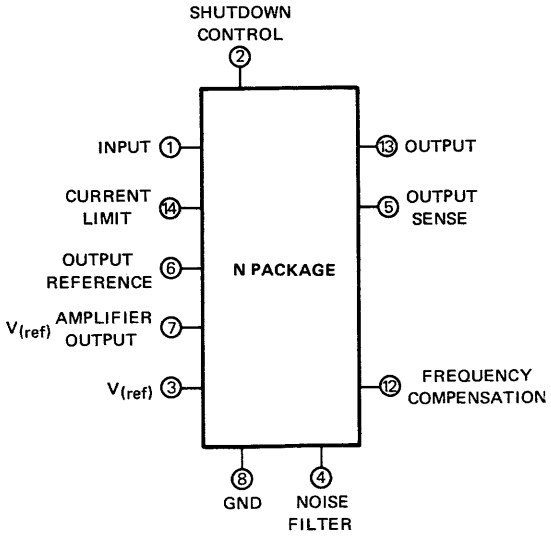
For $V_{(ref)}$ = 2.35 V:

$$R2 \approx (2\ V_O)\ k\Omega;\ R1 \approx 4.7\ k\Omega - R2$$

FIGURE 2

TERMINAL DESIGNATIONS





For basic regulator configurations, test circuits, and applications circuits appearing in this data sheet, terminal functions are defined by their relative positions as shown in the drawings above.

PARAMETER MEASUREMENT INFORMATION

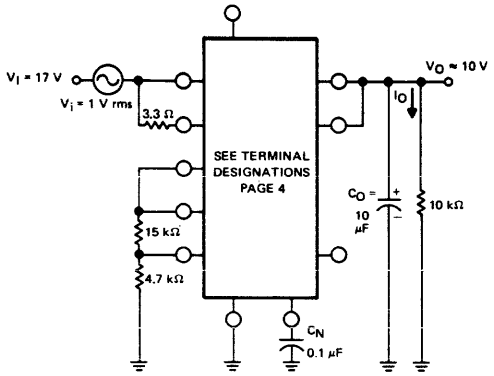


FIGURE 3–RIPPLE REJECTION

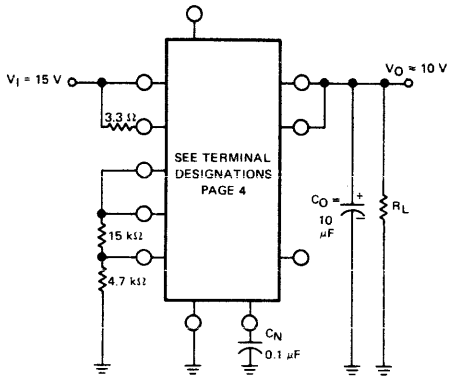


FIGURE 4–LOAD REGULATION

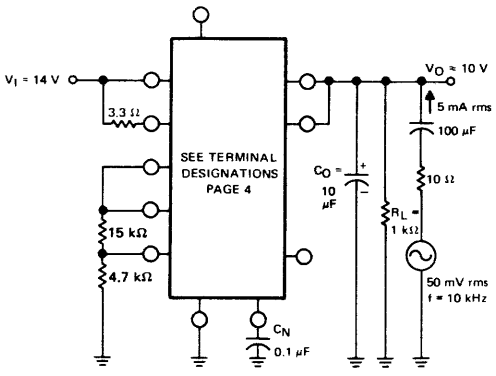


FIGURE 5–OUTPUT IMPEDANCE

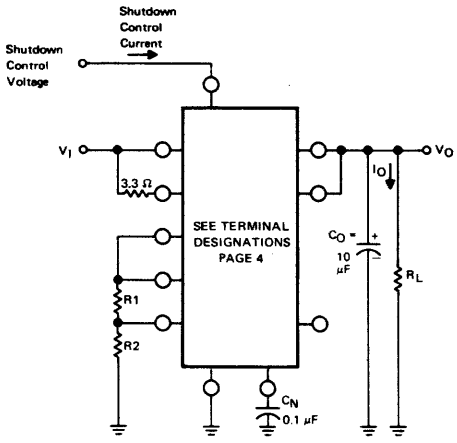


FIGURE 6–SHUTDOWN CONTROL VOLTAGE AND CURRENT

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

INPUT REGULATION
vs
INPUT-TO-OUTPUT
VOLTAGE DIFFERENTIAL

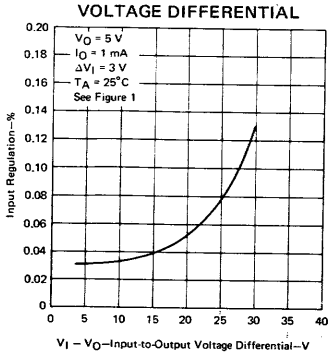


FIGURE 7

LOAD REGULATION
vs
INPUT-TO-OUTPUT
VOLTAGE DIFFERENTIAL

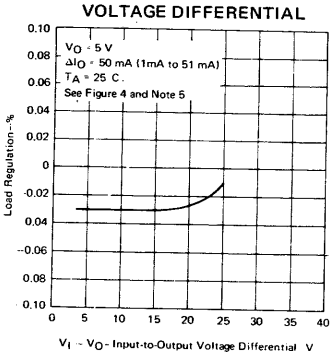


FIGURE 8

STANDBY CURRENT
vs
INPUT VOLTAGE

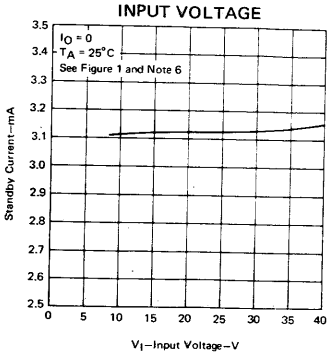


FIGURE 9

CURRENT LIMITING
CHARACTERISTICS

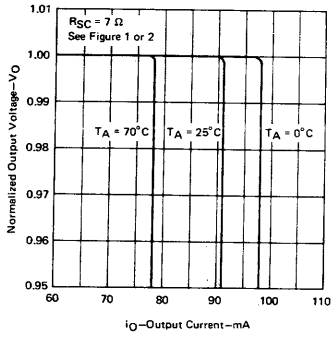


FIGURE 10

OUTPUT IMPEDANCE
vs
FREQUENCY

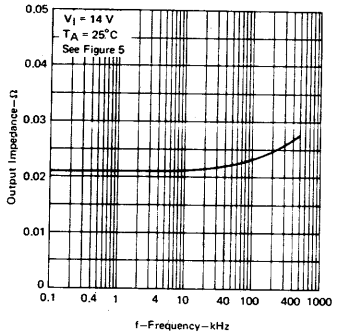


FIGURE 11

TRANSIENT RESPONSE
for
CHANGE IN INPUT VOLTAGE

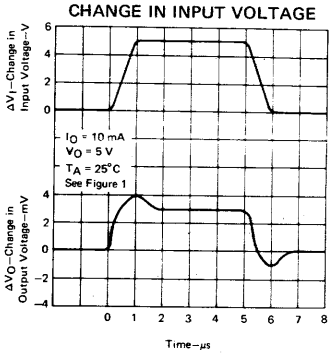


FIGURE 12

TRANSIENT RESPONSE
for
CHANGE IN OUTPUT CURRENT

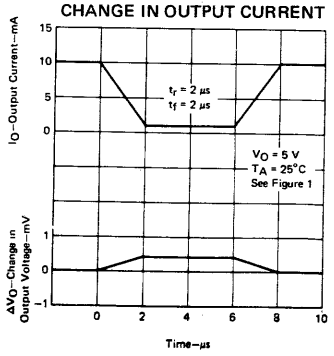


FIGURE 13

TRANSIENT RESPONSE
for
CHANGE IN OUTPUT CURRENT

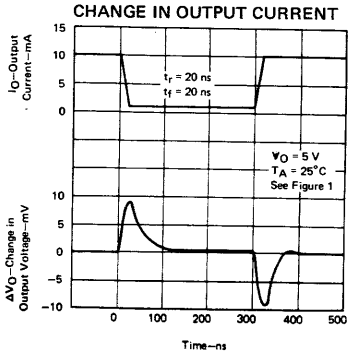


FIGURE 14

THERMAL CHARACTERISTICS

MAXIMUM OUTPUT CURRENT
vs
INPUT-TO-OUTPUT
VOLTAGE DIFFERENTIAL

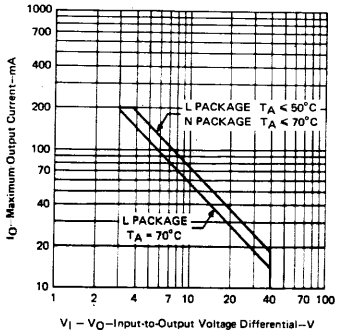


FIGURE 15

NOTES:

5. Load regulation is measured using pulsed techniques (t_W = 150 μs, duty cycle = 5%) to limit changes in internal power dissipation. Output voltage drift due to large changes in internal power dissipation must be taken into account separately.
6. $V_{(ref)}$ amplifier output current is 0.5 mA.

TYPICAL APPLICATION DATA

output voltage

Figures 1 and 2 show basic positive voltage regulator configurations for output voltages from 2 volts to 37 volts. For an adjustable output voltage, make R1 in Figure 1 a potentiometer with a maximum resistance of:

$$R1\ (max) \geq (2\frac{k\Omega}{V})\ (V_O\ max) - 4.7\ k\Omega$$

See Figure 16 for the basic negative voltage regulator connections.

short-circuit output current limiting

The maximum output current, I_{OS}, is determined by the magnitude of resistor R_{SC} which is connected between the input and current limit terminals. Select $R_{SC} \approx 0.63$ volts/I_{OS} in amperes.

noise filter capacitor, C_N

A 0.1-μF capacitor from the noise filter terminal to ground will reduce the output noise voltage to typically below 100 μV (rms). The capacitance value can be increased or decreased depending on the application requirements, but a minimum value of 0.001 μF is recommended.

frequency compensation

The compensation technique shown in Figures 1 through 6 (10-μF capacitor, C_O, from the output terminal to ground) is used for optimum transient response. The 14-pin N plastic package provides a separate frequency compensation terminal and, for most applications, a 0.001-μF capacitor from the frequency compensation terminal to the output sense terminal (C_C) is adequate compensation. Larger values of C_C will degrade pulse response and output impedance characteristics and smaller values will reduce stability.

shutdown control

A d-c voltage (2.4 V minimum) applied to the shutdown control terminal will effectively turn off the regulated output voltage, thereby eliminating power consumption by output loading circuitry and greatly reducing the regulator standby current. Standard TTL or DTL IC logic circuits driving the shutdown control terminal can be used to turn the regulator on and off.

CONNECTION FOR A NEGATIVE OUTPUT VOLTAGE

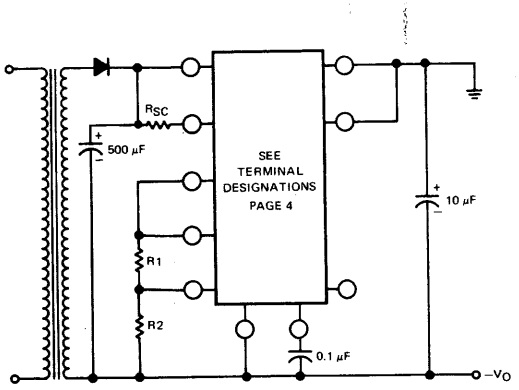


FIGURE 16

POSITIVE VOLTAGE REGULATOR WITH EXTERNAL N-P-N OUTPUT TRANSISTOR

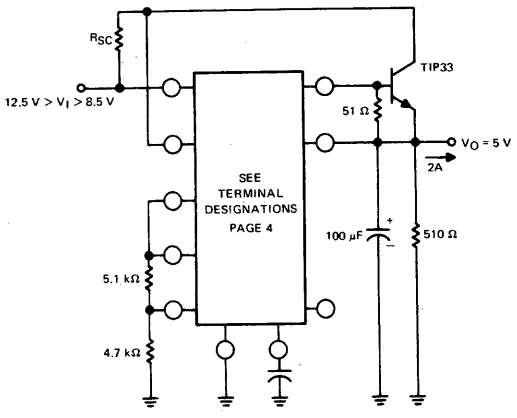


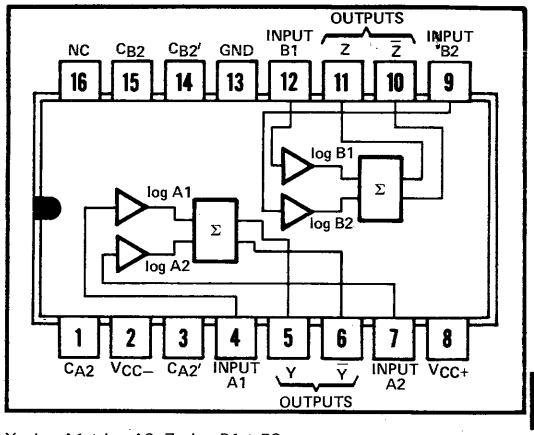
FIGURE 17

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN56502, SN76502 LOGARITHMIC AMPLIFIERS

- Excellent Dynamic Range
- Wide Bandwidth
- Built-In Temperature Compensation
- Log Linearity (30 dBV Sections) . . . 1 dBV
- Wide Input Voltage Range

J OR N
DUAL-IN-LINE PACKAGES (TOP VIEW)



3

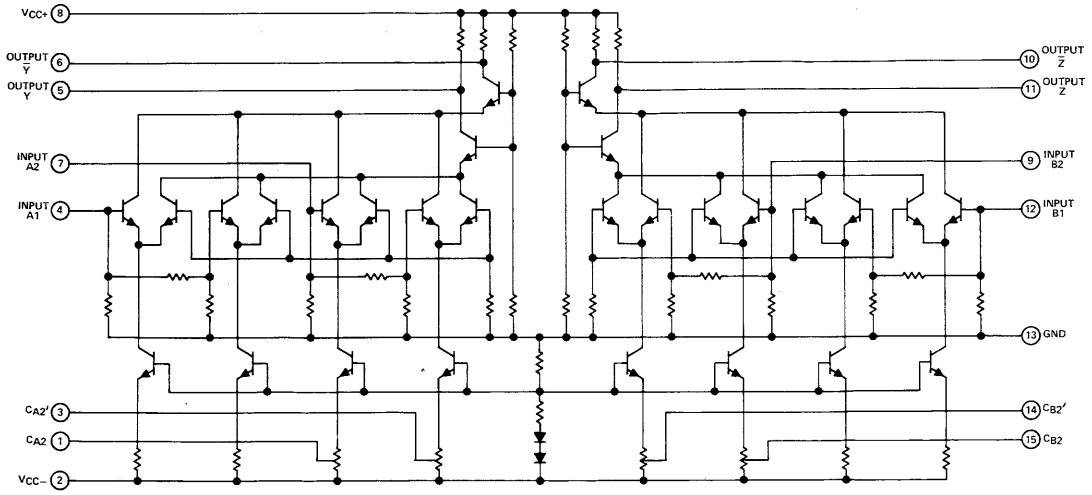
Y∝ log A1 + log A2; Z∝ log B1 + B2
where: A1, A2, B1, and B2 are in dBV, 0 dBV = 1 V.
C_{A2}, $C_{A2'}$, C_{B2}, and $C_{B2'}$, are detector compensation inputs.
NC—No internal connection

description

This monolithic logarithmic amplifier circuit contains four 30-dBV log stages. Gain in each stage is such that the output of each stage is proportional to the logarithm of the input voltage over the 30-dBV input voltage range. Each half of the circuit contains two of these 30-dBV stages summed together in one differential output which is proportional to the sum of the logs of the input voltages of the two stages. The four stages may be interconnected to obtain a theoretical input voltage range of 120 dBV. In practice, this permits the input voltage range to be typically greater than 80 dBV with log linearity of ±0.5 dBV (see application data). Bandwidth is from dc to 40 megahertz.

These circuits are useful in military weapons systems, broadband radar, and infrared reconnaissance systems. They serve for data compression and analog compensation. The logarithmic amplifiers are used in log IF circuitry as well as video and log amplifiers. The SN56502 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN76502 is characterized for operation from 0°C to 70°C.

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (see Note 1):
- V_{CC+} 8V
- V_{CC-} . . . . . −8V

Input voltage (see Note 1) 6V
Output sink current (any one output) . . . . . 30 mA
Continuous total power dissipation . . . . . 500 mW
Operating free-air temperature range: SN56502 Circuits . . . . . −55°C to 125°C
SN76502 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

Note 1: All voltage values, except differential output voltages, are with respect to network ground terminal.

recommended operating conditions

	SN56502			SN76502			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Input voltage for each 30-dBV stage	0.01		1	0.01		1	V_{p-p}
Operating free-air temperature, T_A	−55	25	125	0	25	70	°C

3

electrical characteristics, V_{CC+} = 6 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST FIGURE	SN56502			SN76502			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Differential output offset voltage	1		±25	±60		±40		mV
Quiescent output voltage	2	5.45	5.6	5.85	5.45	5.6	5.85	V
D-c scale factor (differential output), each 30-dBV stage, −35 dBV to −5 dBV	3	7	8	10	6	8	12	mV/dBV
A-c scale factor (differential output)			8			8		mV/dBV
D-c error at −20 dBV (midpoint of −35 dBV to −5 dBV range)	3		1	2		1		dBV
Input impedance			500			500		Ω
Output impedance			200			200		Ω
Rise time, 10% to 90% points, C_L = 24 pF	4		20	25		20	25	ns
Supply current from V_{CC+}	2	14.5	18.5	23	14.5	18.5	23	mA
Supply current from V_{CC-}	2	−6	−8.5	−10.5	−6	−8.5	−10.5	mA
Power dissipation	2	123	162	201	123	162	201	mW

PARAMETER MEASUREMENT INFORMATION

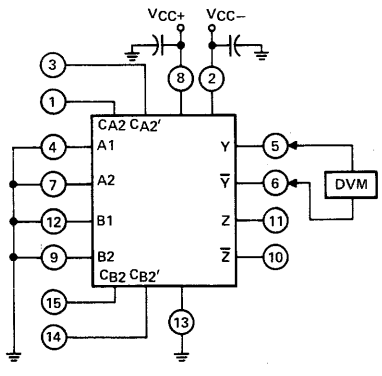


FIGURE 1

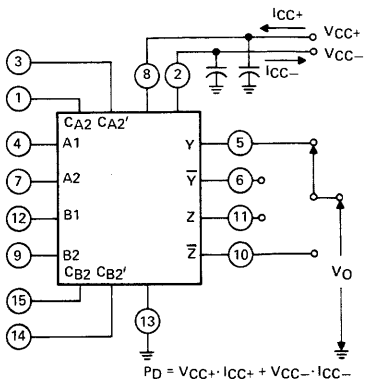
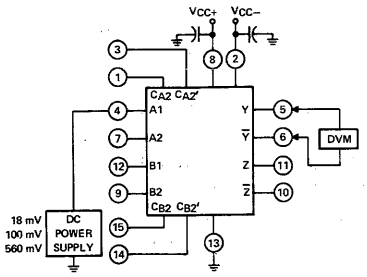


FIGURE 2

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

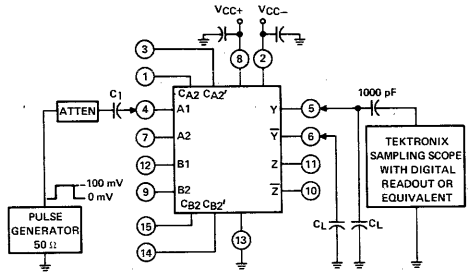
PARAMETER MEASUREMENT INFORMATION



$$\text{Scale Factor} = \frac{[V_{out(560\ mV)} - V_{out(18\ mV)}]\ mV}{30\ dBV}$$

$$\text{Error} = \frac{|V_{out(100\ mV)} - 0.5\ V_{out(560\ mV)} - 0.5\ V_{out(18\ mV)}|}{\text{Scale Factor}}$$

FIGURE 3



NOTES: A. The input pulse has the following characteristics: t_w = 50 ns, $t_r \leq 2$ ns, $t_f \leq 2$ ns, PRR = 10 MHz.

B. Capacitor C_1 consists of three capacitors in parallel: 1 μF, 0.1 μF, and 0.01 μF.

C. C_L includes probe and jig capacitance.

FIGURE 4

3

TYPICAL CHARACTERISTICS

SN56502
DIFFERENTIAL OUTPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

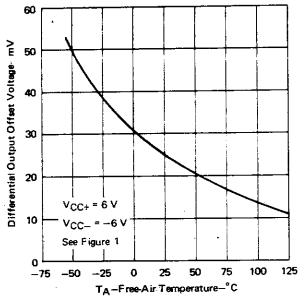


FIGURE 5

QUIESCENT OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

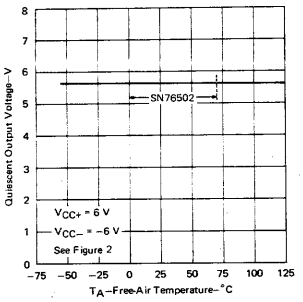


FIGURE 6

SN56502
D-C SCALE FACTOR
vs
FREE-AIR TEMPERATURE

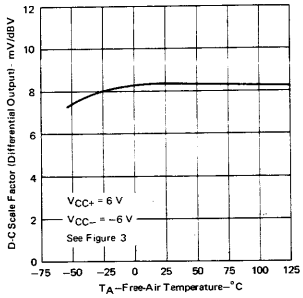


FIGURE 7

SN56502
D-C ERROR
vs
FREE-AIR TEMPERATURE

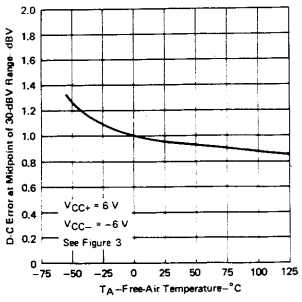


FIGURE 8

OUTPUT RISE TIME
vs
LOAD CAPACITANCE

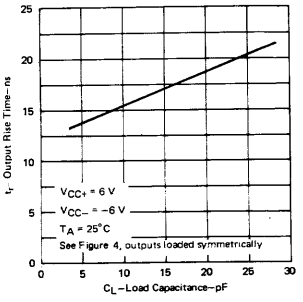


FIGURE 9

POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

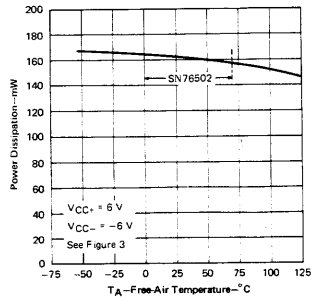


FIGURE 10

CIRCUIT TYPES SN56502, SN76502
LOGARITHMIC AMPLIFIERS

TYPICAL APPLICATION DATA

Although designed for high-performance applications such as broadband radar infrared detection, and weapons systems, this device has a wide range of applications in data compression and analog computation.

basic log function

The basic log response is derived from the exponential current-voltage relationship of collector current and base-emitter voltage. This relationship is given in the equation:

$$m \cdot V_{BE} = \ln [(I_C + I_{CES})/I_{CES}]$$

where: I_C = collector current
I_{CES} = collector current at $V_{BE} = 0$
$m = q/kT$ (in V^{-1})
V_{BE} = base-emitter voltage

The differential input amplifier allows dual-polarity inputs, is self-compensating for temperature variations, and is relatively insensitive to noise.

functional block diagram

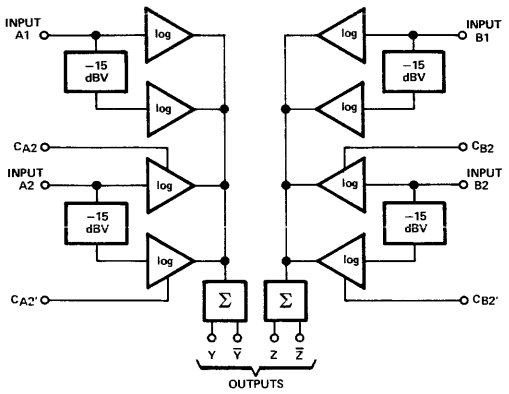


FIGURE 11

log sections

As can be seen from the schematic, there are eight differential pairs. Each pair is a 15-dBV log subsection, and each input feeds two pairs for a range of 30 dBV per stage.

Four compensation points are made available to allow slight variations in the gain (slope) of the two individual 15-dBV stages of input A2 and B2. By slightly changing the voltage on any of the compensation pins from its quiescent value, the gain of that particular 15-dBV stage can be adjusted to match the other 15-dBV stage in the pair. The compensation pins may also be used to match the transfer characteristics of input A2 to A1 or B2 to B1.

The log stages in each half of the circuit are summed by directly connecting their collectors together and summing through a common-base output stage. The two sets of output collectors are used to give two log outputs, Y and $\overline{Y}$ (or Z and $\overline{Z}$) which are equal in amplitude but opposite in polarity. This increases the versatility of the device.

By proper choice of external connections, linear amplification, linear attentuation, and many different applications requiring logarithmic signal processing are possible.

input levels

The recommended input voltage range of any one stage is given as 0.01 volt to one volt. Input levels in excess of one volt may result in a distorted output. When several log sections are summed together, the distorted area of one section overlaps with the next section and the resulting distortion is insignificant. However, there is a limit to the amount of overdrive that may be applied. As the input drive reaches ±3.5 volts, saturation occurs, clamping the collector-summing line and severely distorting the output. Therefore, the signal to any input must be limited to approximately ±3 volts to ensure a clean output.

output levels

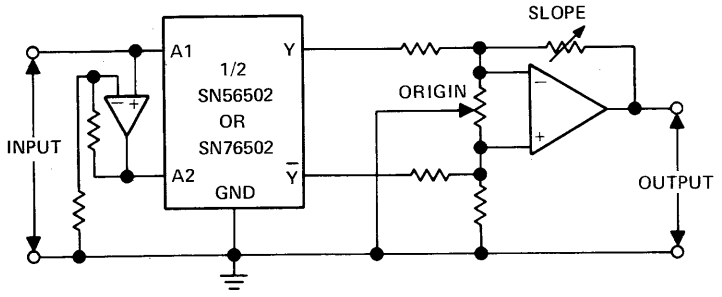
Differential-output-voltage levels are low, generally less than 0.6 volt. As demonstrated in Figure 12, the output swing and the slope of the output response can be adjusted by varying the gain by means of the slope control. The coordinate origin may also be adjusted by positioning the offset of the output buffer.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATION DATA

circuits

Figures 12 through 19 show typical circuits using these logarithmic amplifiers. Operational amplifiers not otherwise designated are SN52741 or SN72741. For operation at higher frequency, use of SN52733/SN72733 is recommended instead of SN52741/SN72741, with the differential outputs connected as in Figure 14. The SN5510/SN7510 or SN5511/SN7511 wideband amplifiers may also be used.



TYPICAL TRANSFER CHARACTERISTICS

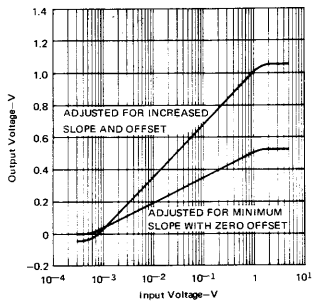
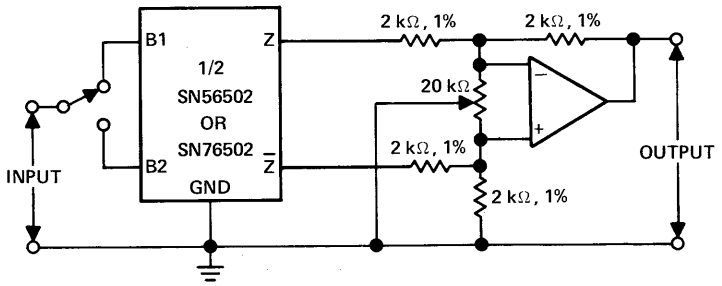


FIGURE 12–OUTPUT SLOPE AND ORIGIN ADJUSTMENT



TRANSFER CHARACTERISTICS OF TWO TYPICAL INPUT STAGES

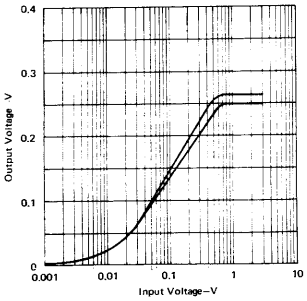
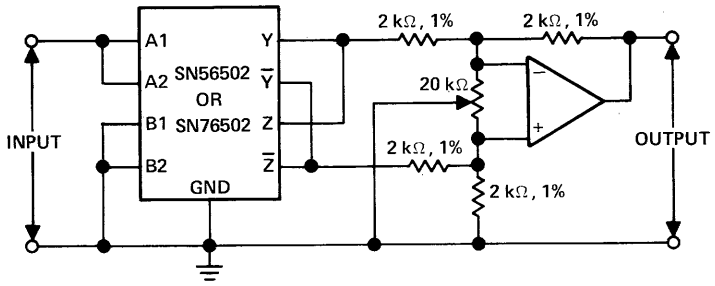


FIGURE 13–UTILIZATION OF SEPARATE STAGES



TRANSFER CHARACTERISTICS WITH BOTH SIDES PARALLELED

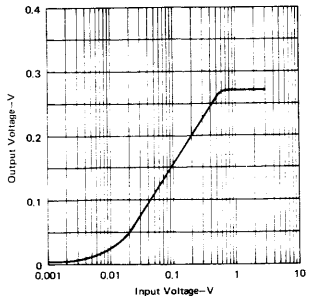
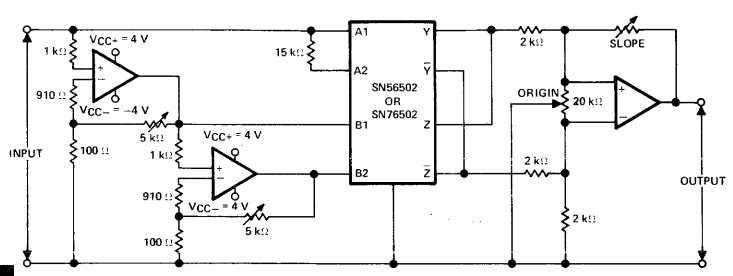
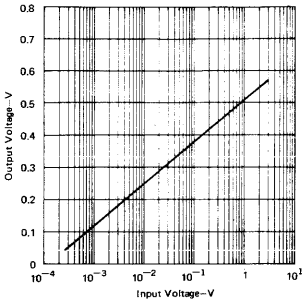


FIGURE 14–UTILIZATION OF PARALLELED INPUTS

TYPICAL APPLICATION DATA

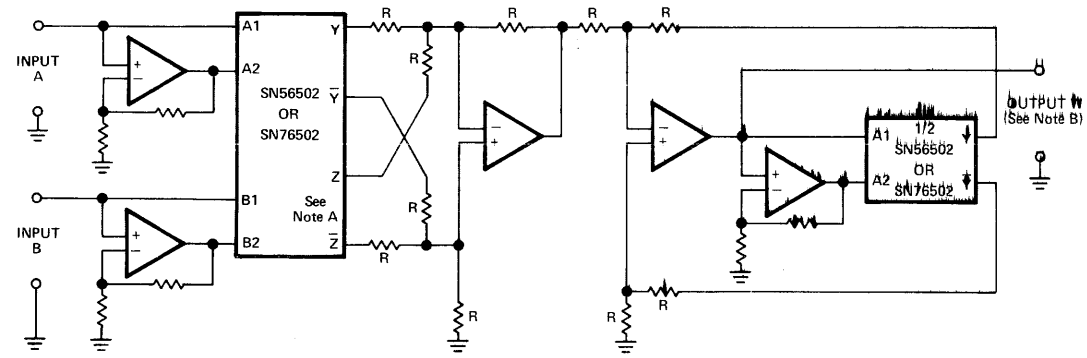


TRANSFER CHARACTERISTICS



NOTES: A. Inputs are limited by reducing the supply voltages for the input amplifiers to ±4 V.
B. The gains of the input amplifiers are adjusted to achieve smooth transitions.

FIGURE 15–LOGARITHMIC AMPLIFIER WITH INPUT VOLTAGE RANGE GREATER THAN 80 dB



NOTES: A. Connections shown are for multiplication. For division, Z and $\bar{Z}$ connections are reversed.
B. Output W may need to be amplified to give actual product or quotient of A and B.
C. R designates resistors of equal value, typically 2 kΩ to 10 kΩ.

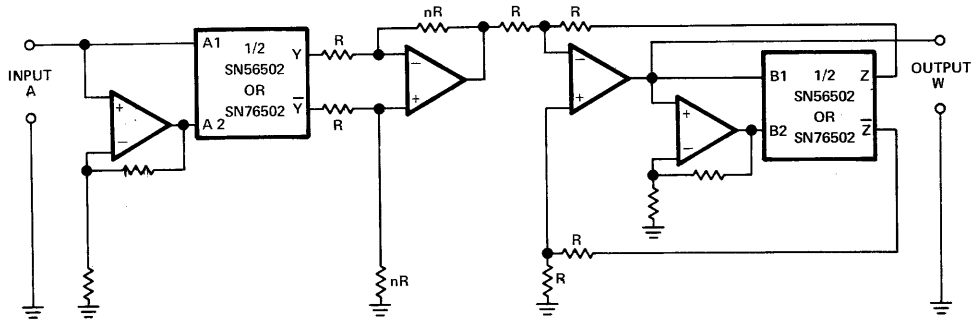
Multiplication: $W = A \cdot B \Rightarrow \log W = \log A + \log B$, or $W = a^{(\log_a A + \log_a B)}$

Division: $W = A/B \Rightarrow \log W = \log A - \log B$, or $W = a^{(\log_a A - \log_a B)}$

FIGURE 16–MULTIPLICATION OR DIVISION

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

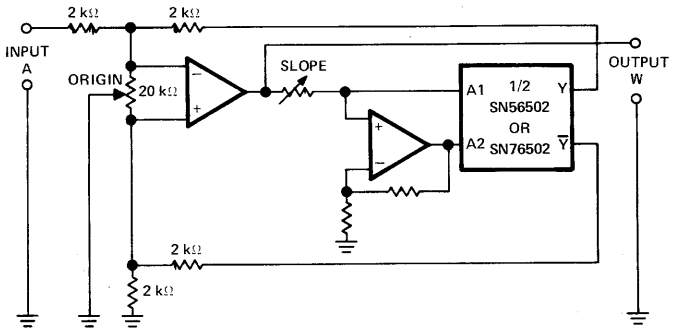
TYPICAL APPLICATION DATA



NOTE: R designates resistors of equal value, typically 2 kΩ to 10 kΩ. The power to which the input variable is raised is fixed by setting nR. Output W may need to be amplified to give the correct value.

Exponential: $W = A^n \Rightarrow \log W = n \log A$, or $W = a^{(n \log_a A)}$

FIGURE 17—RAISING A VARIABLE TO A FIXED POWER



NOTE: Adjust the slope to correspond to the base "a".

Exponential to any base: W = a

FIGURE 18—RAISING A FIXED NUMBER TO A VARIABLE POWER

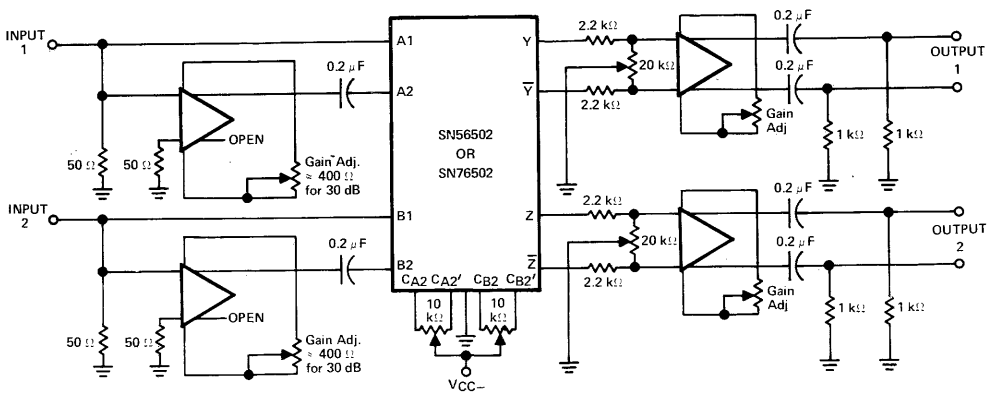


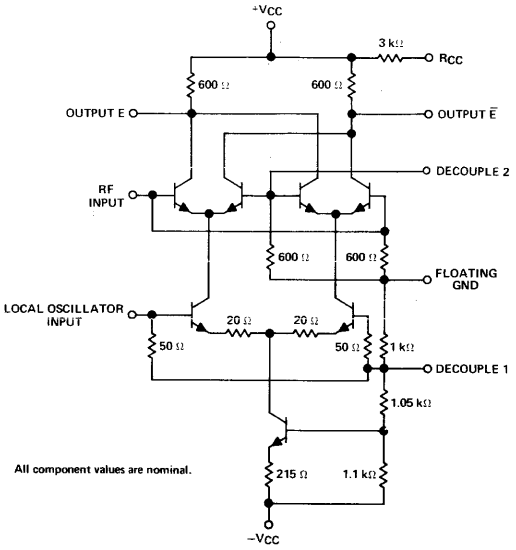
FIGURE 19—DUAL-CHANNEL RF LOGARITHMIC AMPLIFIER WITH 50-dB INPUT RANGE PER CHANNEL AT 10 MHz

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN56514, SN76514
BALANCED MIXERS

- Flat Response to 100 MHz
- Local Oscillator IF Isolation . . . 30 dB Typ
- Local Oscillator RF Isolation . . . 60 dB Typ
- RF-IF Isolation . . . 30 dB Typ
- Conversion Gain . . . 14 dB Typ
- Use with 12-V or ±6-V Power Supplies

schematic

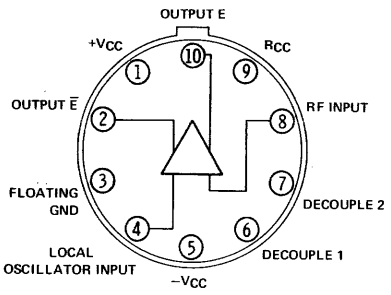


description

The SN56514 and SN76514 are doubly balanced mixers which utilize two cross-coupled, differential transistor pairs driven by a third balanced pair. The circuit features a flat response over a wide band of frequencies. The SN56514 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN76514 is characterized for operation from 0°C to 70°C.

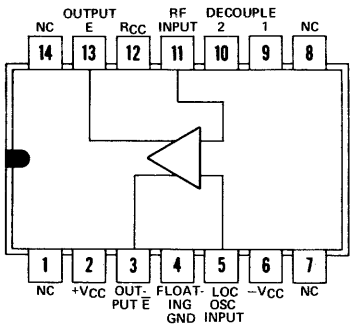
terminal assignments

L PLUG-IN PACKAGE
(TOP VIEW)



PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

J AND N DUAL-IN-LINE PACKAGES
(TOP VIEW)



For operation from a single 12-V supply, connect the positive terminal of the supply to $+V_{CC}$, the negative terminal to $-V_{CC}$, and the floating-ground terminal to R_{CC}. For operation from two 6-V supplies, leave R_{CC} open and connect the positive terminal of one supply to $+V_{CC}$, the negative terminal of the other supply to $-V_{CC}$, and the remaining terminals of the two supplies to the floating-ground terminal. See Figure 19.

NC—No internal connection

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	18 V
Input voltage (see Notes 1 and 2)	7 V
Continuous output current (see Note 3)	10 mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 4)	500 mW
Operating free-air temperature range: SN56514 Circuits	−55°C to 125°C
SN76514 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		12		V
Local oscillator input voltage (see Note 5)		250	300	mV p-p
RF input voltage (see Note 5)		10	30	mV p-p
Operating free-air temperature range: SN56514 Circuits	−55	25	125	°C
SN76514 Circuits	0	25	70	°C

electrical characteristics at 25°C free-air temperature, V_{CC} = 12 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN56514			SN76514			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Quiescent output voltage	1		9.6	10.5	11.3	9.6	10.5	11.3	V
I_{CC}	Supply current	1		5.5	7.4	10.9	5.5	7.4	10.9	mA
G_C	Conversion gain (single-ended output)	2	f_{RF} and f_{LO} = 100 kHz thru 40 MHz	11	14	17	11	14	17	dB
LOIFI	Local oscillator to IF isolation	3	f_{LO} = 100 kHz thru 40 MHz	15	29†			29†		dB
LORFI	Local oscillator to RF isolation	3	f_{LO} = 100 kHz thru 40 MHz	40	52†			52†		dB
RFIFI	RF to IF isolation	4	f_{RF} = 100 kHz thru 40 MHz	15	28†			28†		dB

†The typical values are at 40 MHz.

NOTES: 1. All d-c voltage values are with respect to $-V_{CC}$ terminal.
2. This rating applies to the local-oscillator input, RF input, and Decouple 2.
3. This value applies for both outputs simultaneously.
4. For operation of SN56514 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 18.
5. All signal voltages are with respect to the floating-ground terminal. Alternatively, the RF input may be applied differentially between the RF input terminal and Decouple 2.

PARAMETER MEASUREMENT INFORMATION

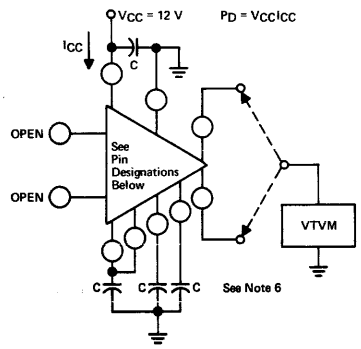


FIGURE 1–V_O, I_{CC}, and P_D

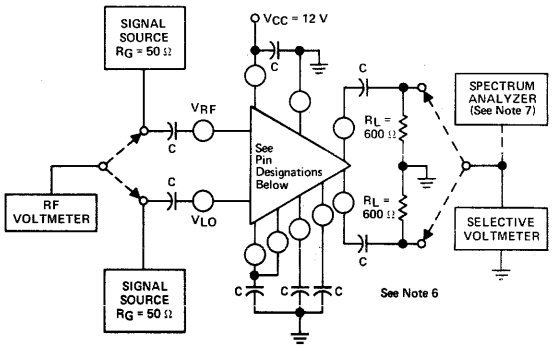


FIGURE 2–G_C

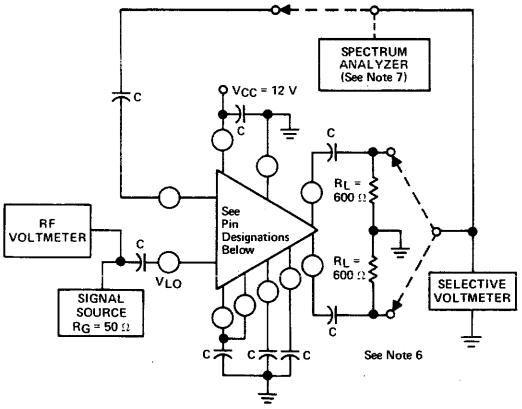


FIGURE 3–LOIFI and LORFI

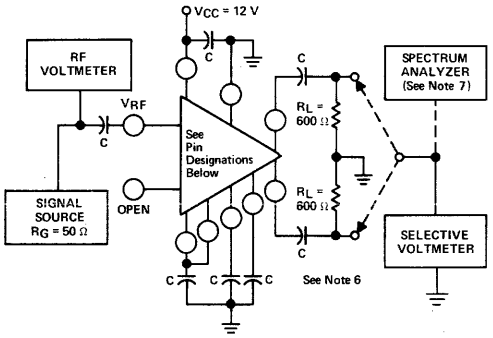
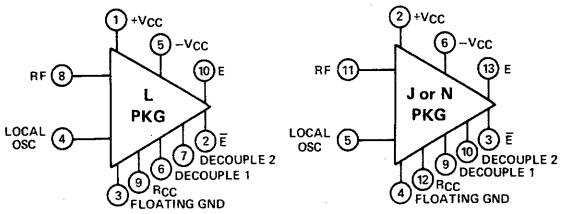


FIGURE 4–RFIFI

Pin Designations: For all test circuits appearing in this data sheet, terminal functions are defined by their relative positions as shown in the drawings in this block.



NOTES: 6. Capacitor C comprises the following capacitors in parallel: 1 μF, 0.1 μF, and 0.0015 μF.
7. The spectrum analyzer is used for frequencies above the normal range of the selective voltmeter.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

QUIESCENT OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

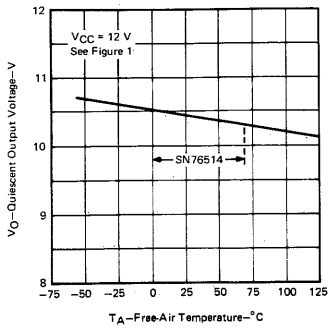


FIGURE 5

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

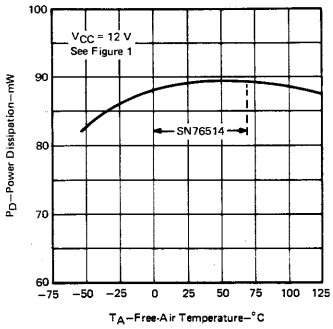


FIGURE 6

CONVERSION GAIN
vs
SUPPLY VOLTAGES

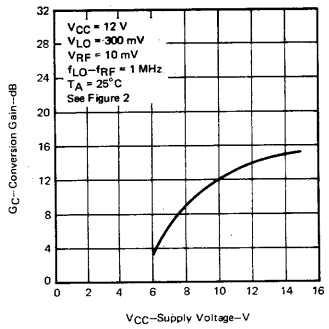


FIGURE 7

CONVERSION GAIN
vs
LOCAL OSCILLATOR VOLTAGE

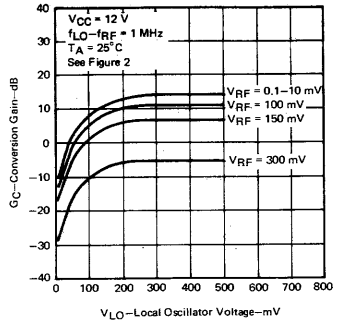


FIGURE 8

CONVERSION GAIN
vs
FREQUENCY

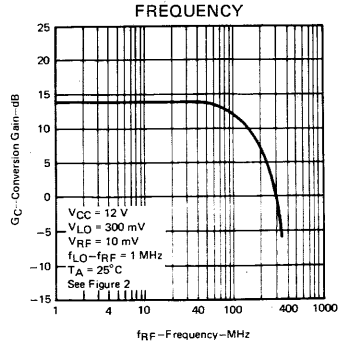


FIGURE 9

CONVERSION GAIN
vs
FREE-AIR TEMPERATURE

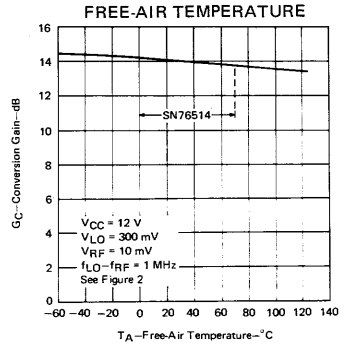


FIGURE 10

TYPICAL CHARACTERISTICS

LOCAL OSCILLATOR TO IF ISOLATION
vs
FREQUENCY

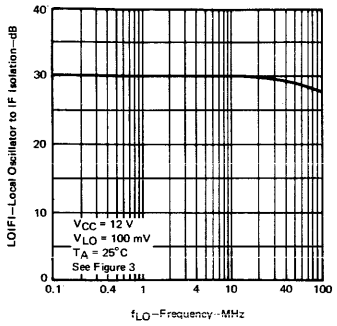


FIGURE 11

LOCAL OSCILLATOR TO IF ISOLATION
vs
FREE-AIR TEMPERATURE

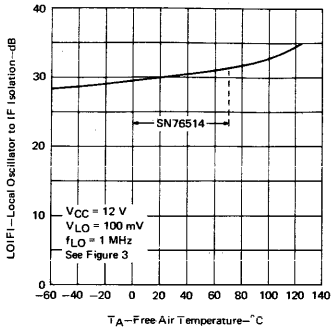


FIGURE 12

LOCAL OSCILLATOR TO RF ISOLATION
vs
FREQUENCY

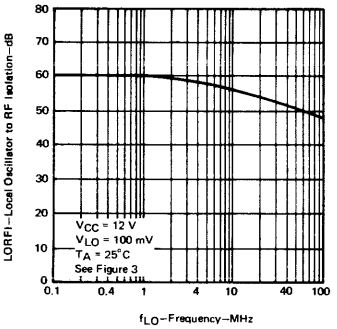


FIGURE 13

LOCAL OSCILLATOR TO RF ISOLATION
vs
FREE-AIR TEMPERATURE

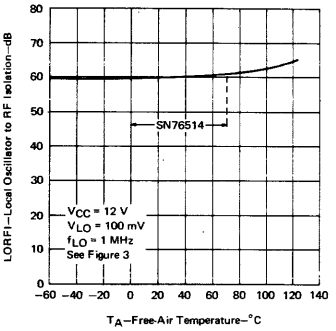


FIGURE 14

RF TO IF ISOLATION
vs
FREQUENCY

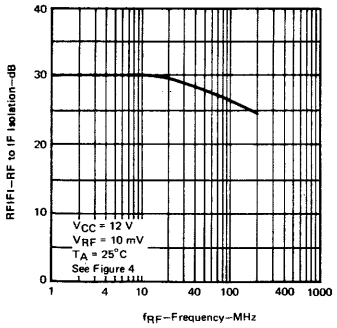


FIGURE 15

RF TO IF ISOLATION
vs
FREE-AIR TEMPERATURE

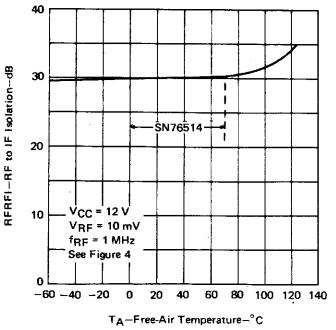


FIGURE 16

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

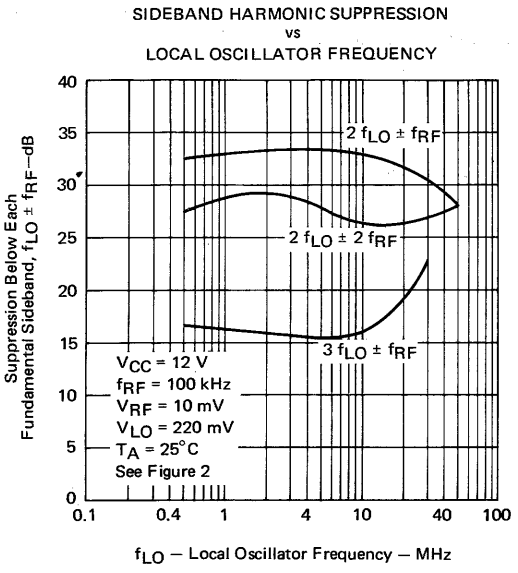


FIGURE 17

THERMAL INFORMATION

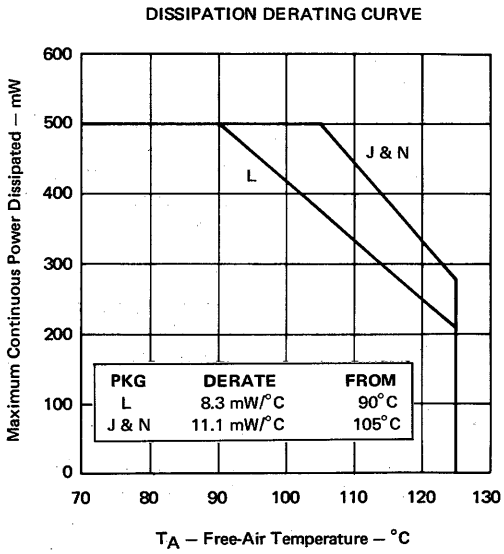


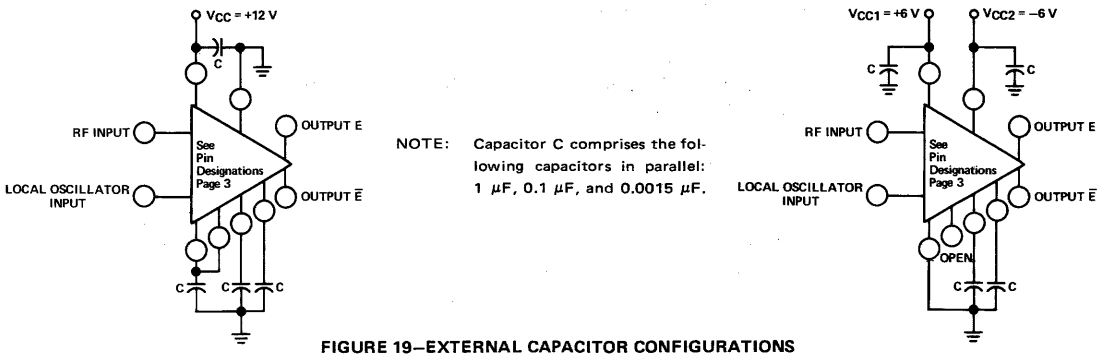
FIGURE 18

TYPICAL APPLICATION DATA

The SN55514 and SN75514 balanced mixers are designed to have considerable circuit flexibility which results in a wide range of applications. Typical applications include use as balanced modulators for sideband-suppressed-carrier generation, product detectors for demodulation, frequency converters, and frequency or phase modulators. In addition, the SN55514 and SN75514 may be used in control systems and analog computers as low-level multipliers or squaring circuits.

The circuits are designed to operate from either a single 12-V supply or two 6-V supplies. Electrical characteristics will be unchanged with the use of either power supply option. External bypass capacitors, as shown in Figure 19, should be used for optimum performance.

The mixer's electrical performance and the inherent IC advantages of size, reliability, and component matching make it very desirable for use in communication and control systems.



NOTE: Capacitor C comprises the following capacitors in parallel: 1 μF, 0.1 μF, and 0.0015 μF.

FIGURE 19—EXTERNAL CAPACITOR CONFIGURATIONS

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CONSUMER CIRCUITS SUMMARY

Following is a listing of Consumer Circuits presently available from Texas Instruments. Should you desire additional information, application engineering advice, or sales assistance, please contact your nearest TI Sales office.

AUDIO AMPLIFIERS

SN76001	1 W Audio at 9 V and 8 Ω
SN76003	3 W Audio at 30 V and 16 Ω
SN76010	Same as SN76001 except for different pin arrangement
SN76013	3 W Audio at 24 V and 8 Ω
SN76005	5 W Audio at 34 V and 16 Ω
SN76050	5 W Audio at 14 V and 4 Ω

DUAL CHANNEL AND STEREO

SN76104	Stereo Multiplex Decoder
SN76105	Stereo Multiplex Decoder
SN76110	Stereo Multiplex Decoder
SN76131	Stereo Preamplifier

CHROMA CIRCUITS

SN76242	Chroma Sub-carrier Regenerator
SN76243	Chroma Amplifier
SN76246	Chroma Demodulator
SN76630	PAL Chroma Demodulator

COMPLEX TV FUNCTIONS

SN76530	Video Detector
SN76532	TV Jungle (suitable for horizontal deflection with tubes)
SN76533	TV Jungle (suitable for horizontal deflection with semiconductors)
SN76540	TV Jungle for N-P-N Tuners and Ge Diode Detection
SN76541	TV Jungle for N-P-N Tuners and Low Level Detection
SN76542	TV Jungle for P-N-P Tuners and Ge Diode Detection
SN76564	Automatic Fine Tuning

REGULATORS FOR VARACTOR TUNERS

SN76550	33 V at 5 mA
SN76552	22 V at 5 mA
SN76553	12 V at 5 mA

IF CIRCUITS FOR RADIO AND TV

SN76600	1st and 2nd Video IF Stages
SN76603	RF/IF Amplifier
SN76619	RF Amplifier/FM Detector
SN76640	Sound IF/Limiter, Slope Detector, Audio Driver, Voltage Regulator
SN76641	IF Limiting Amplifier
SN76642	Sound IF/Detector
SN76643	Sound IF/Detector
SN76650	1st and 2nd Video IF with Keyed AGC
SN76660	Sound IF/Amplifier Limiter, Balanced Coincidence Detector, D-c Volume Control
SN76665	Sound IF/Amplifier Limiter, Detector, Attenuator, Audio Driver, Voltage Regulator
SN76670	SN76660 with Open-Collector Output
SN76680	SN76660 with Audio Driver and Voltage Regulator

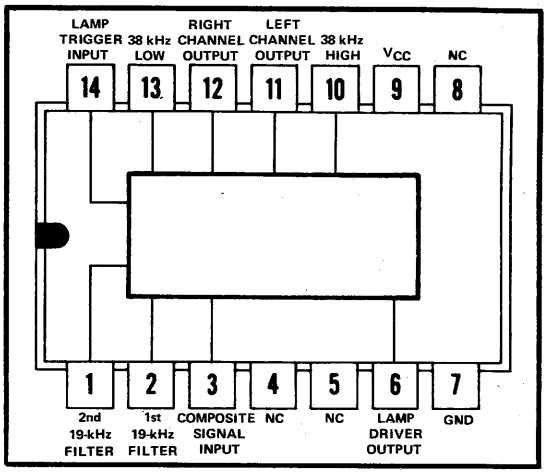
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE SN76110 STEREO DEMODULATOR

FOR USE IN FM MULTIPLEX SYSTEMS

- Designed to be Interchangeable with Motorola MC1307P
- Power Supply Range . . . 8 to 14 V
- Low Harmonic Distortion
- Stereo-Indicator Lamp Driver
- Monaural Squelch Capability

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



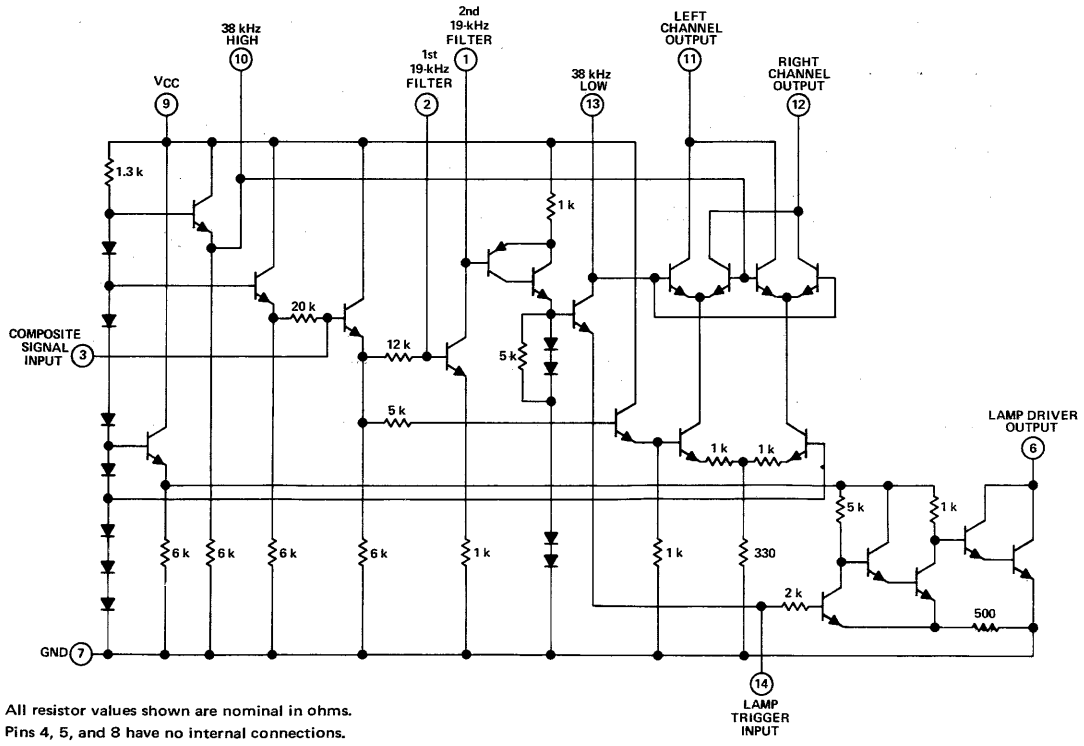
NC—No internal connection

description

The SN76110 is a monolithic integrated circuit designed to process the detected composite multiplex signal. The circuit provides left-channel and right-channel separation and balance, and also has a driver output for a stereo-indicator lamp.

3

schematic



All resistor values shown are nominal in ohms.
Pins 4, 5, and 8 have no internal connections.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE SN76110
STEREO DEMODULATOR

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 22 V
Lamp driver current . . . . . 40 mA
Power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 625 mW
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Derate linearly to 375 mW at 75°C free-air temperature at the rate of 5 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	8	12	14	V
Operating free-air temperature, T_A	0	25	75	°C

3

electrical characteristics (unless otherwise noted V_{CC} = 8 V to 14 V, T_A = 25°C, see figure 1)

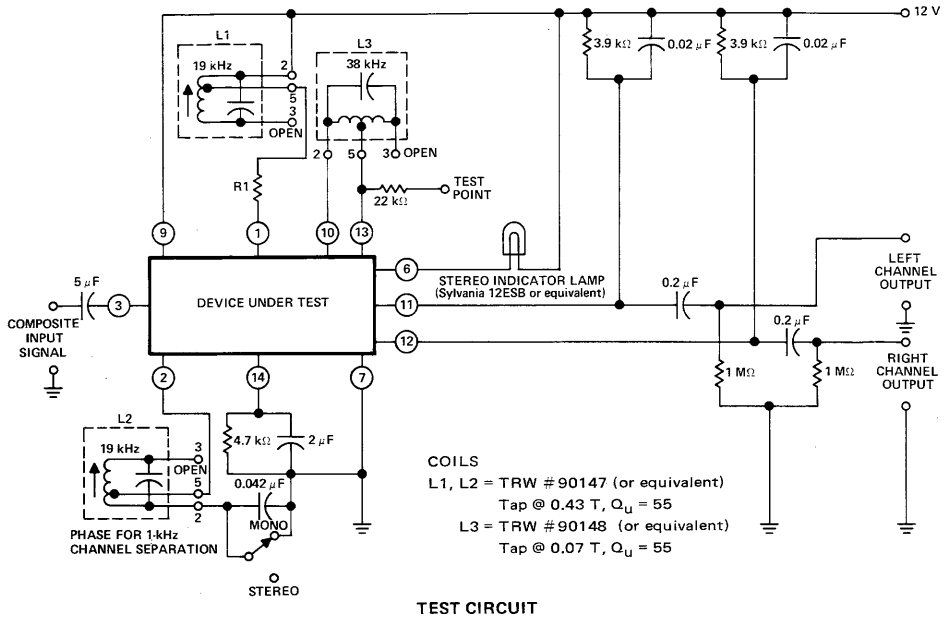
PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Input impedance	f = 1 kHz			20		kΩ
Stereo channel separation	See Note 3	f_{mod} = 100 Hz		40		dB
		f_{mod} = 1 kHz	30	45		
		f_{mod} = 10 kHz		35		
Total harmonic distortion	f_{mod} = 1 kHz, See Notes 3 and 4			0.3%		
Channel balance	Monaural input = 200 mV rms			0.5	1	dB
Ultrasonic frequency rejection	See Note 5	f = 19 kHz		25		dB
		f = 38 kHz		20		
Inherent SCA rejection (without filter)	f_{mod} = 60 kHz to 74 kHz, See Notes 4 and 5 and Figure 2			55‡		dB
Minimum trigger input for on state at lamp-driver output	Trigger frequency = 19 kHz,			10	20	mV rms
Maximum trigger input for off state at lamp-driver output	R1 = 180 Ω		2	6		
Power dissipation	V_{CC} = 12 V	lamp off		140		mW
		lamp on		170		

NOTES: 3. These characteristics are measured with a 564-mV p-p standard multiplex composite signal. This is defined as a signal containing left and/or right audio modulation with a 10-percent, 19-kHz pilot signal in accordance with FCC regulations. For stereo testing, both left-channel-only and right-channel-only modulation are used.
4. The total harmonic distortion and SCA rejection values apply for both stereo and monaural operation.
5. Rejection is referenced to a 1-kHz output signal produced by a 364-mV p-p standard multiplex composite signal as defined in Note 3.

†All typical values are at V_{CC} = 12 V.
‡This is the lowest value for the specified frequency range.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION



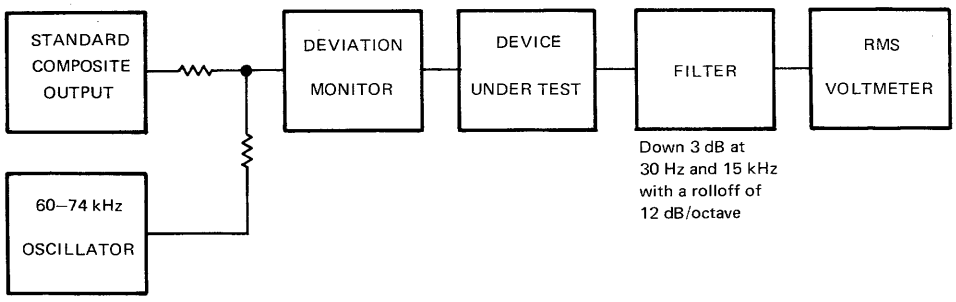
TEST CIRCUIT

typical voltages with respect to pin 7, V_{CC} = 12 V, R1 = 180 Ω, lamp on, measured using a VTVM

Pin Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Volts	11.8	3.2	3.9	NC	NC	0.9	0	NC	12	4.8	8.8	8.8	4.8	1.7

NC—No internal connection

FIGURE 1



test procedure for SCA rejection

1. Modulate the stereo generator with a 1-kHz reference signal.
2. Adjust output for 67.5 kHz deviation.
3. Remove the 1-kHz reference signal.
4. Alternately adjust a 19-kHz pilot signal and a 60-kHz to 74-kHz external signal to deviate 6.7-kHz.
5. Rejection is defined as the difference in dB between the magnitude of the 1-kHz reference signal and the audio components present due to the interaction of the 19-kHz and 38-kHz components with the 60-kHz to 74-kHz signal.

FIGURE 2

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION AND BEAT FREQUENCY COMPONENTS IN AUDIO SIGNAL vs FREQUENCY

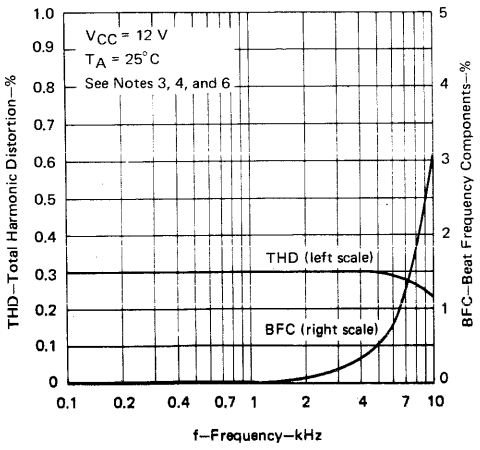


FIGURE 3

TOTAL HARMONIC DISTORTION vs COMPOSITE INPUT LEVEL

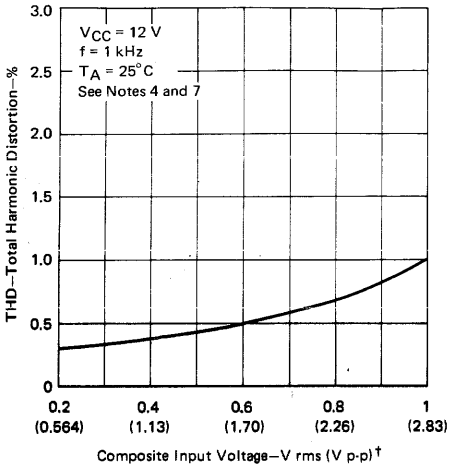


FIGURE 4

CHANNEL SEPARATION vs COMPOSITE INPUT LEVEL

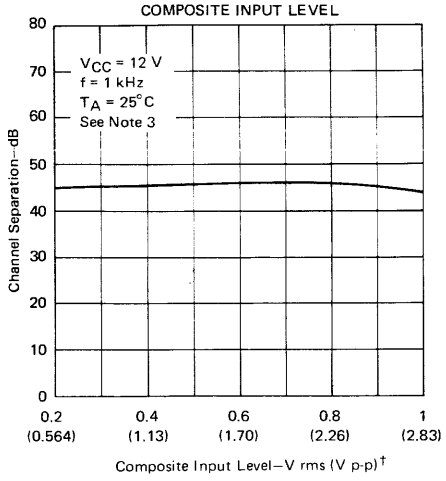


FIGURE 5

CHANNEL SEPARATION vs FREQUENCY

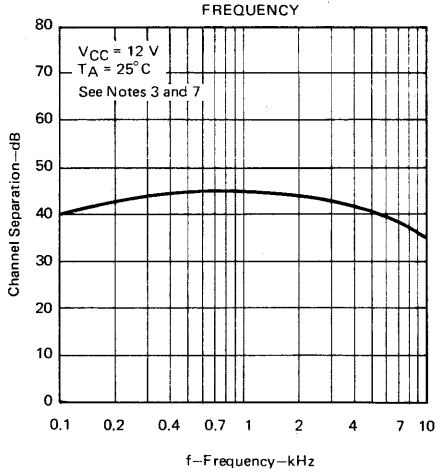


FIGURE 6

NOTES: 3. These characteristics are measured with a 564-mV p-p standard multiplex composite signal. This is defined as a signal containing left and/or right audio modulation with a 10-percent, 19-kHz pilot signal in accordance with FCC regulations. For stereo testing, both left-channel-only and right-channel-only modulation are used.
4. The total harmonic distortion and SCA rejection values apply for both stereo and monaural operation.
6. Beat frequency components (BFC) result from the presence of the 19-kHz pilot signal in stereo broadcasts.
7. Input signal is a 1-kHz composite signal, 846 mV p-p.

†The rms scale is valid for monaural modulation (L=R) only. The peak-to-peak scale is valid for monaural or stereo modulation.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

INHERENT SCA REJECTION
vs
COMPOSITE INPUT LEVEL

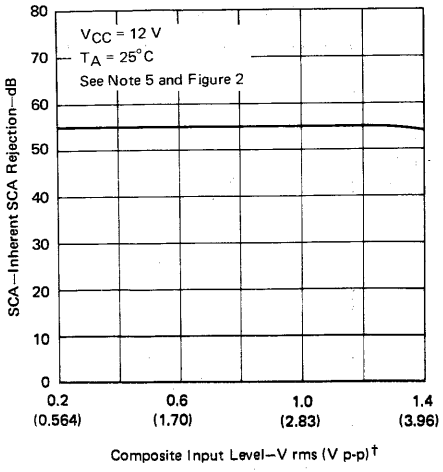


FIGURE 7

TRIGGER LEVELS FOR LAMP DRIVER
vs
19-kHz GAIN ADJUSTMENT RESISTOR

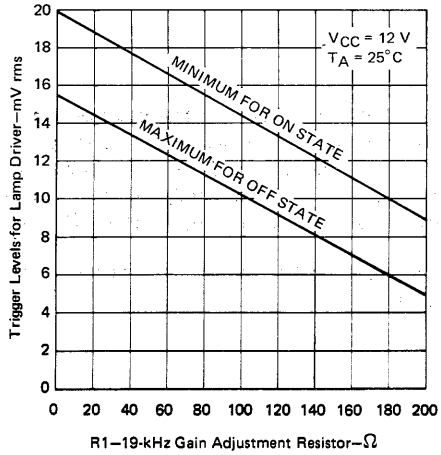


FIGURE 8

ON-STATE TRIGGER LEVEL FOR LAMP DRIVER
vs
SUPPLY VOLTAGE

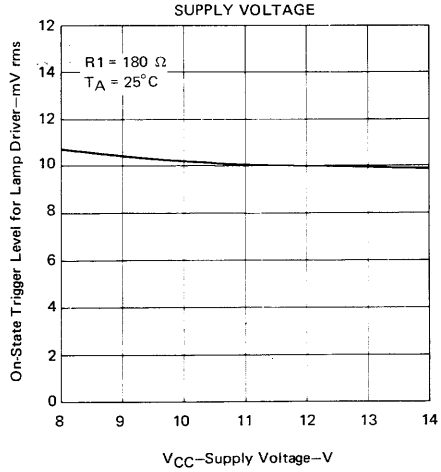


FIGURE 9

NOTE 5: Rejection is referenced to a 1-kHz output signal produced by a 364-mV p-p standard multiplex composite signal as defined in Note 3.

† The rms scale is valid for monaural modulation (L=R) only. The peak-to-peak scale is valid for monaural or stereo modulation.

CIRCUIT TYPE SN76110
STEREO DEMODULATOR

ORDERING INSTRUCTIONS AND MECHANICAL DATA

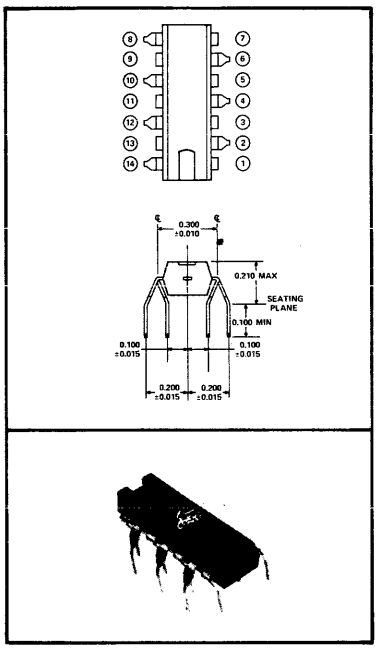
general

The SN76110 is available in the plastic dual-in-line package (outline N). Orders for these devices should include the package outline letter at the end of the type number. The device may also be ordered with the leads formed in the quad-in-line configuration by adding the dash number –07 after the package outline letter, i.e., SN76110N, SN76110N–07.

Refer to Section 1 for physical dimensions for the dual-in-line N-package outline.

3

quad-in-line lead configuration



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

4

ECL Circuits

ECL INDEX
NUMERIC

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

4

ultra-high speed: 2-3 ns

The ECL2500 Series is a compatible catalog family of ultra-high-speed (2-3 ns) ECL functions designed to fulfill the integrated-circuit requirements of next-generation computer systems. Twenty-eight device types perform both multifunction and complex logic, storage, and interface functions (up to 13 gates/package), all of which are offered in the economical industry-standard 16-pin plastic dual-in-line package.

summary of functions

	Gates/Pkg	Number of Types	Remarks
Logic			
Basic Gates and Multifunction Gates	1-6	18	Complementary Outputs High Fan-in High Fan-out Dotted Inputs/Outputs Multi-Output
Arithmetic and Decoder	5-12	3	Full Adder 3-Bit Decoder 5-Bit Group Carry
Interface			
Line Driver	2	1	Drives Two 50-Ω Lines
Line Receiver	2	1	High CMRR
High-Level-to-ECL Converter	2	1	Compatible with TTL, DTL, RTL
ECL-to-High-Level Converter	2	1	
Storage			
Multifunction Latch	4	1	Single-input gated
Complex Latch	9-13	2	2-input gated
Total Compatible Functions		28	

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings

Power Supply Voltage (V_{CC} to V_{EE})	6 V
Input Voltage (V_{in} @ V_{BB} = 0.0 V)	± 2 V
Output Source Current	40 mA d-c
Storage Temperature Range	−40°C to 150°C

recommended operating conditions

V_{CC} (Pin ③ and/or Pin ⑥)	1.32 V
V_{BB} (Pin ⑮)	OV (Gnd)
V_{EE} (Pin ⑩)	-3.2 V
Operating Temperature Range	0° to 75° C
System Impedance	50 Ω

4

electrical characteristics of basic ECL gate

Test Conditions: V_{CC} = 1.32 V, V_{BB} = 0,
V_{EE} = −3.2 V, T_A = 25° C

			Typical
Fan-out			1-10
Speed	Fan-out = 1	t_t (10% – 90% pts)	2.8 ns
		t_p (50% pts)*	2.3 ns
	Fan-out = 10	t_t *	4.3 ns
		t_p *	3.5 ns
Power Dissipation/Gate		Unterminated, P_{DU}	30 mW
		Terminated, P_{DT} **	60 mW
Logic Levels:			
	Logical "1"		400 mV
	Logical "0"		−400 mV
Noise Margin			200 mV

*See switching waveforms in figure 6.
**Complementary outputs driving 50 Ω to Gnd and 270 Ω to -3.2 V.

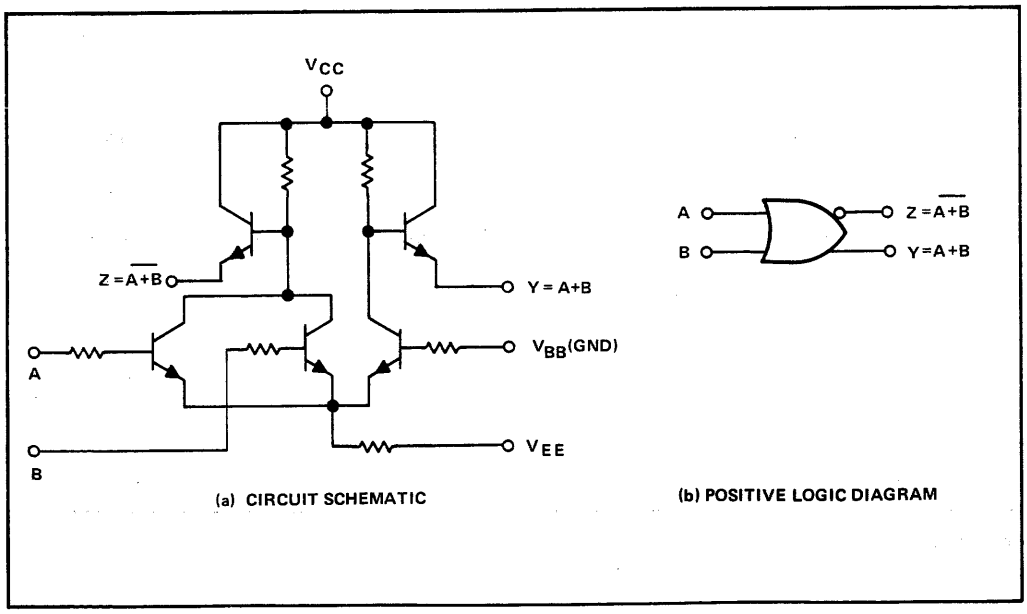
basic ECL gate

The basic ECL gate configuration is shown in figure 1. The high-speed performance results from the nonsaturating operation of the high-f_T transistor current switches. The high impedance of the load (input to differential amplifier) coupled with the low impedance of the driving source (emitter-follower output) allows high d-c fan-out. High-speed operation and high a-c fan-out are possible because all circuits are designed to operate in a 50-Ω system. When high-speed operation is a requirement, it is recommended that terminated 50-Ω transmission lines be utilized to interconnect circuits.

The basic ECL gate design of the ECL2500 Series provides both the output function Y and its complement Z; however, to maximize logic capability, some modules have only one output.

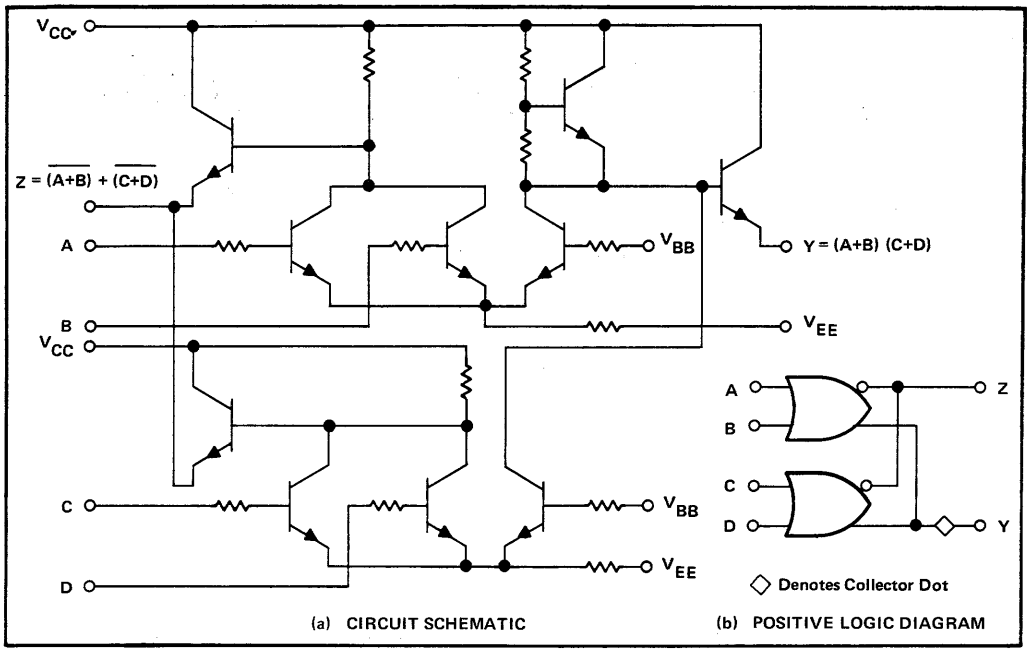
To minimize the number of packages to implement a system, and to reduce external connections, many units in the ECL2500 Series include logical connections between gates within the package. In-phase collector dotting (positive AND logic), out-of-phase emitter dotting (positive OR logic), and multiple inputs common to one package pin have been utilized to provide a very comprehensive logic family. An example of output dotting within the package is shown in figure 2. The positive logic WIRED-AND function is achieved by connecting in-phase collectors and the incorporation of an up-level clamp transistor. The positive logic WIRED-OR function within the package is accomplished by connecting out-of-phase-emitter-follower outputs. This inherent logic flexibility provides the system designer with a logic family with 1.6 times the logic/module density of conventional digital logic families.

figure 1. ECL gate



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

figure 2. ECL output dotting



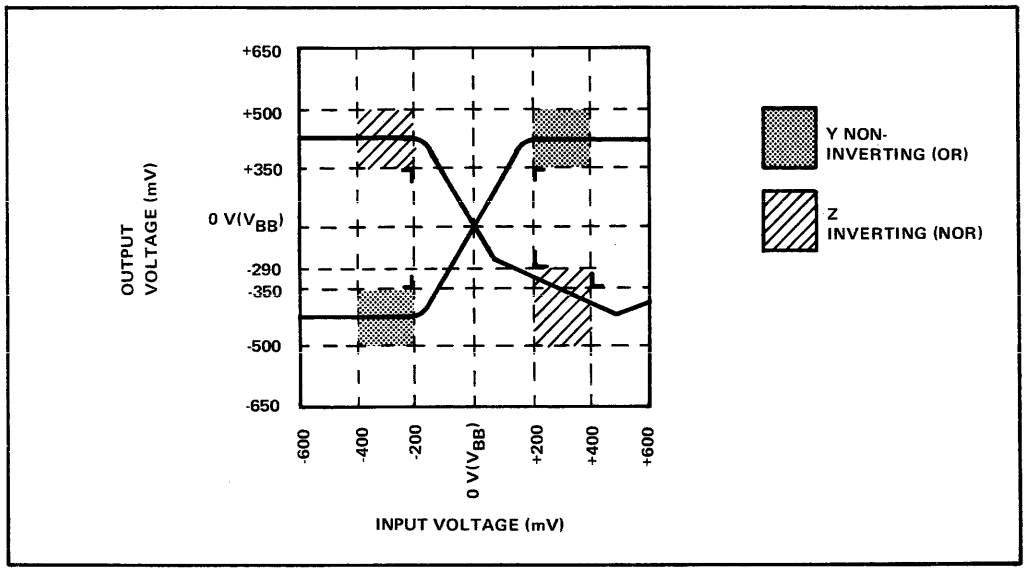
4

logic levels

Typical logic levels for the basic gate are 400 mV for a logical "1" and -400 mV for a logical "0" when operating with V_{CC}= 1.32 V, V_{EE}= −3.2 V, and V_{REF}= 0 V. Minimum levels when operating at 25°C free-air temperature and loaded with 50 Ω to ground and 270 Ω pulldown to −3.2 V are ± 350 mV. These logic levels are ensured with inputs at ±200 mV which provide 150 mV of d-c noise margin. Since the actual threshold is approximately 150 mV and typical output levels are 400 mV, typical d-c noise margin in excess of 200 mV can be expected. Transfer characteristics for the basic gate are shown in figure 3.

For gating functions which have emitter dots or parallel emitter followers, up levels will be increased by 50 mV to 450 mV. Likewise, down levels will increase by a similar amount to -350 mV.

figure 3. transfer characteristics-basic ECL gate



4

loading

To minimize package dissipation and to permit the external WIRED-OR (positive logic) function, the emitter-follower outputs have been left unterminated. The emitter-follower output is capable of driving a load of up to 25 mA d-c, but requires an externally provided negative voltage source and termination. The recommended termination includes a 270-Ω resistive load (pulldown) to V_{EE} (−3.2 V) and 50 Ω to V_{BB} (GND). To utilize the high-speed characteristics (≈ 2-ns switching speeds) of the ECL2500 Series, transmission lines or other controlled-impedance systems should be utilized to accomplish interconnections. The 50 Ω to ground provide proper termination when a 50-Ω transmission line is used.

When operating in a controlled-impedance interconnection system, two general classes of fan-out loading are permitted. The first (cluster loading) involves loads which can be connected within two inches from any source (output). The measurement is made between package pins. (Seating plane is used as a reference point.) These loads, called source stubs, are treated as lumped-capacitance loads which increase switching times but cause no reflection problems.

Since ECL circuit outputs may be directly wired together (emitter "dotted") to provide an OR (positive logic) function, cluster loading constraints apply to each of the sources making up the WIRED-OR. Up to ten such outputs may be "dotted" provided no two are more than two inches apart.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

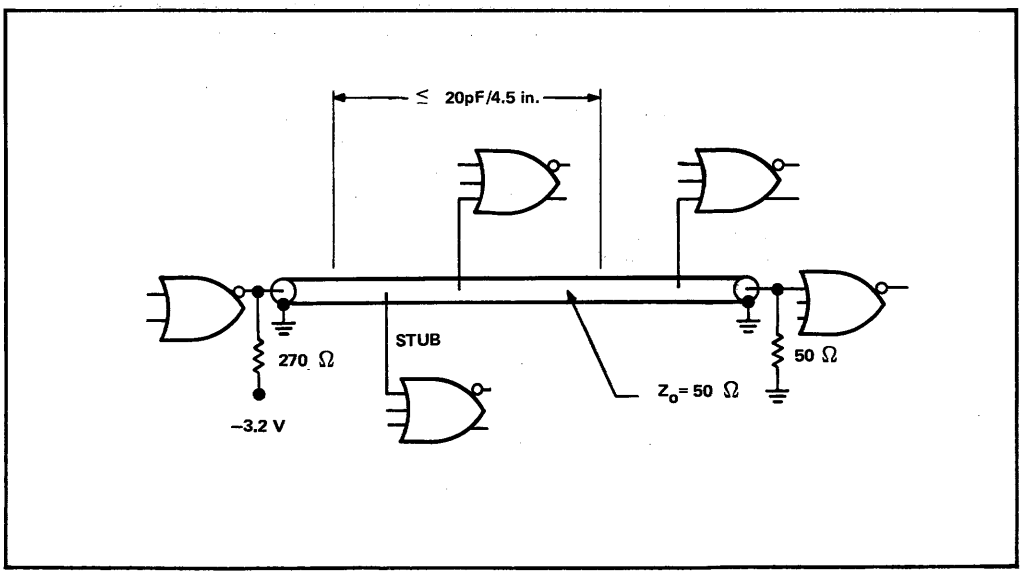
A second class of fan-out loading is commonly referred to as distributive loading. Such loads are greater than two inches from any source as measured between package pins (seating plane is used as reference point). These loads must be treated as lumped loads along a transmission line. The logic levels and switching speeds of the ECL2500 Series permit a maximum lumped load of 20 pF with less than a 20 per cent reflection coefficient for a 50-Ω printed-circuit line (e_r = 4.5). However, these loads must be 4.5 inches or more apart. Smaller lumped loads may be spaced closer together provided no more than 20 pF exists along any 4.5 inches of line measured outside the two-inch source stub.

Lumped loads may consist of circuit (gate) input capacitance and stub capacitance if used. Capacitances due to circuit inputs are ≈ 5.0 pF per input, while that attributed to stubs is dependent on the type of transmission line used. Figure 4 shows a typical distributive-loading arrangement.

Both cluster and distributive loads may be employed separately or in combination. Termination resistors for a load configuration involving only a cluster may be placed where convenient, but any other configuration requires termination at the end of the transmission line.

4

figure 4. typical distributive loading

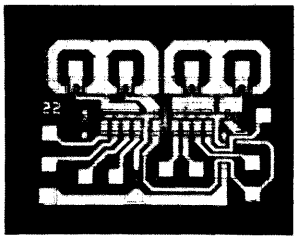


TYPES ECL2500 THRU ECL2505, ECL2511 EMITTER-COUPLED-LOGIC GATES

ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) BASIC GATES FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS

description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.



The ECL2500 family includes:

- **Basic Gate Modules**
- Multifunction Gate Modules
- Bistable Modules
- Arithmetic Modules
- Interface Modules
- Memory Module

family features

- High speed. . .typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ±225 mV typical at 25°C

This data sheet covers the basic gate modules. Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series basic gates

The seven ECL2500 series modules that form the basic gate group are shown in the table below. These modules contain various combinations of the basic ECL gate shown in the schematic of Figure A and the logic diagrams of Figure B.

SUMMARY OF MODULES IN BASIC GATE GROUP

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS PER GATE	
				Y (OR)	Z (NOR)
ECL2500	2	4	OR/NOR	1	1
ECL2501	1	9	OR/NOR	1	1
ECL2502	3	2	OR/NOR	1	1
ECL2503	4	2	NOR		1
ECL2504	4	1	OR/NOR	1	1
ECL2505	3	3	NOR		1
ECL2511	4	2 (1 common to each gate)	OR	1	

unused inputs

To ensure high-speed operation all unused inputs should be tied to -1.0 ± 0.5 V.

power dissipation

Basic gate power drain with outputs unterminated is between 22 mW and 34 mW under the following conditions:

V_{CC} = 1.32 V
V_{EE} = -3.2 V
V_{BB} = 0 V

All inputs at 400 mV

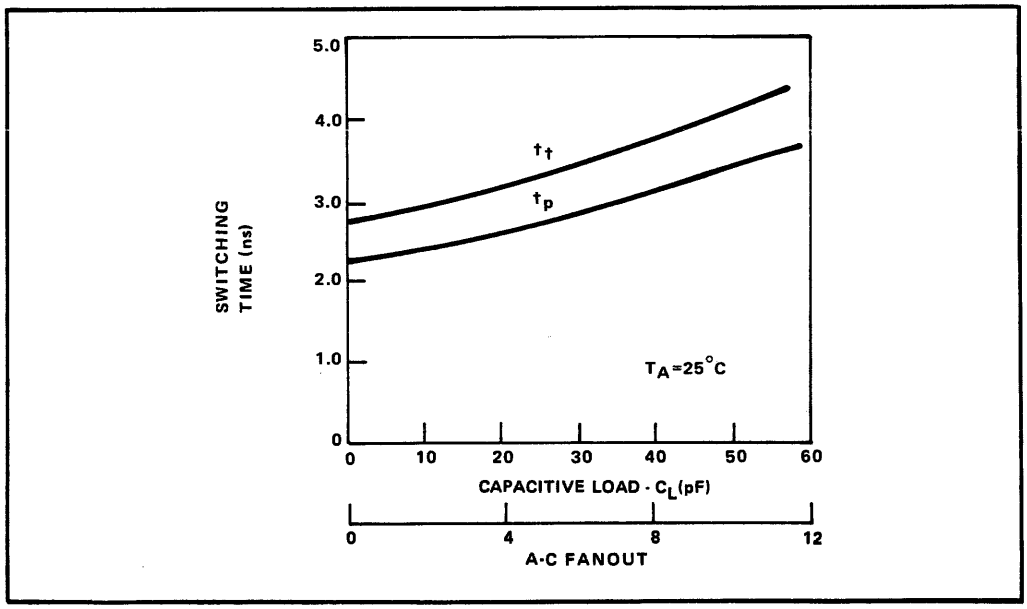
When terminated into 50 Ω to ground and 270 Ω to −3.2 V, each emitter-follower output will dissipate an additional 22 mW in the up-level state and approximately 8 mW in the down-level state. Therefore, a basic gate with terminated complementary outputs will dissipate approximately 60 mW.

4

switching times

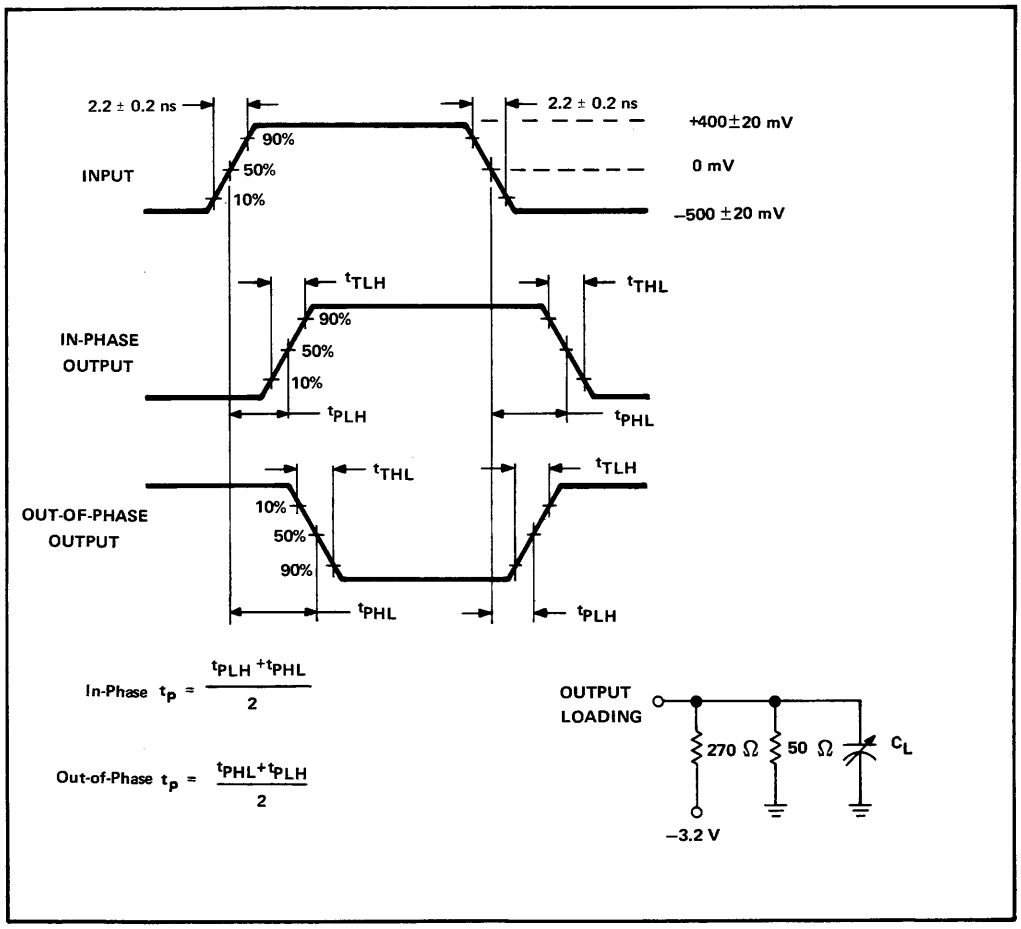
Switching-time performance at 25° C with various capacitive loadings is described in figure 5. This capacitive loading is directly relatable to a-c fan-out assuming 4-5 pF per gate input. Delay-time degradation with increasing fan-out approximates 75 ps per additional load. Switching-time waveform definitions and output terminations used for testing are shown in figure 6.

figure 5. switching time vs loading



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

figure 6. switching time waveforms



4

arithmetic and decoder

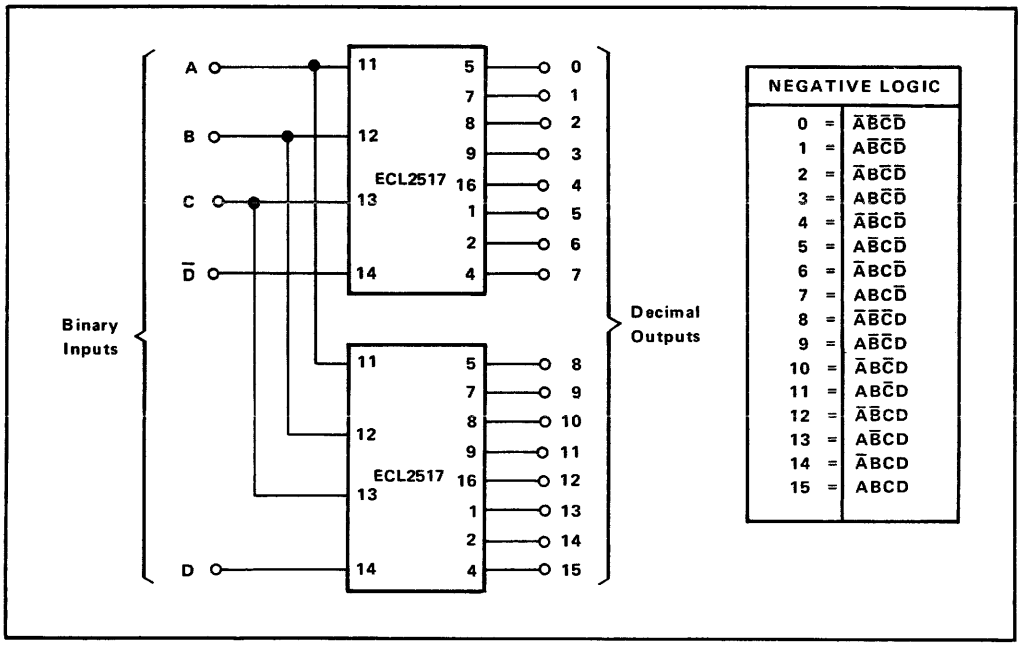
In addition to multifunction logic, more complex gating functions such as a 5-Bit Group Carry, Full Sum/Carry Adder, and 3-Bit Decoder have been included in the ECL2500 Series. Each of these modules will implement logic functions found in most large systems.

The 5-Bit Group Carry (ECL2515) is designed to provide the "look-ahead" carry feature required in high-speed adder applications. By utilizing this device and implementing the add function, significant reduction in addition delay time can be achieved as compared to ripple-through-carry addition.

The Full Sum-Carry Adder (ECL2516) produces the sum and carry outputs along with their complements for 1-bit additions. This addition can be accomplished in less than 3 ns.

The 3-Bit Decoder with Enable (ECL2517) generates a negative logical "1" on one of eight outputs dependent on the 3-bit binary input. The enable or 4th-bit input permits 4-bit binary decoding when two ECL2517 packages are utilized as shown in figure 7. Also shown is the binary decoding for the eight outputs of the ECL2517.

figure 7. 4-bit binary decode application



line driver

Each of the line drivers in the ECL2531 (2 per package) is designed to drive two 50-Ω transmission lines from both its in-phase and out-of-phase outputs. This permits fanning-out in two directions from each output.

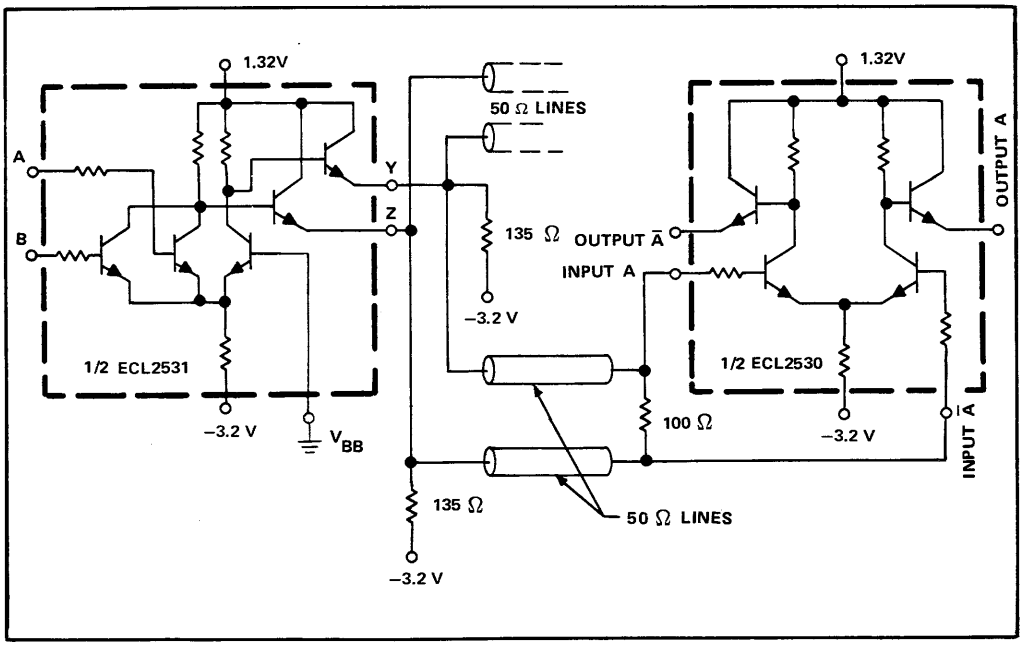
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

line receiver

The Dual Line Receiver (ECL2530) is designed to provide compatibility with the dual-line driver; however, it can be driven by any of the functions in the family. Its unique characteristics stem from optimization of the basic gate differential amplifier allowing input of a differential signal. Common-mode noise rejection of the Line Receiver permits transmission of logic signals over paths which are exposed to rather large noise transients and between areas in a machine which have devices operating at significantly different junction temperatures.

A typical connection arrangement is shown in figure 8.

figure 8. line driver/line receiver application



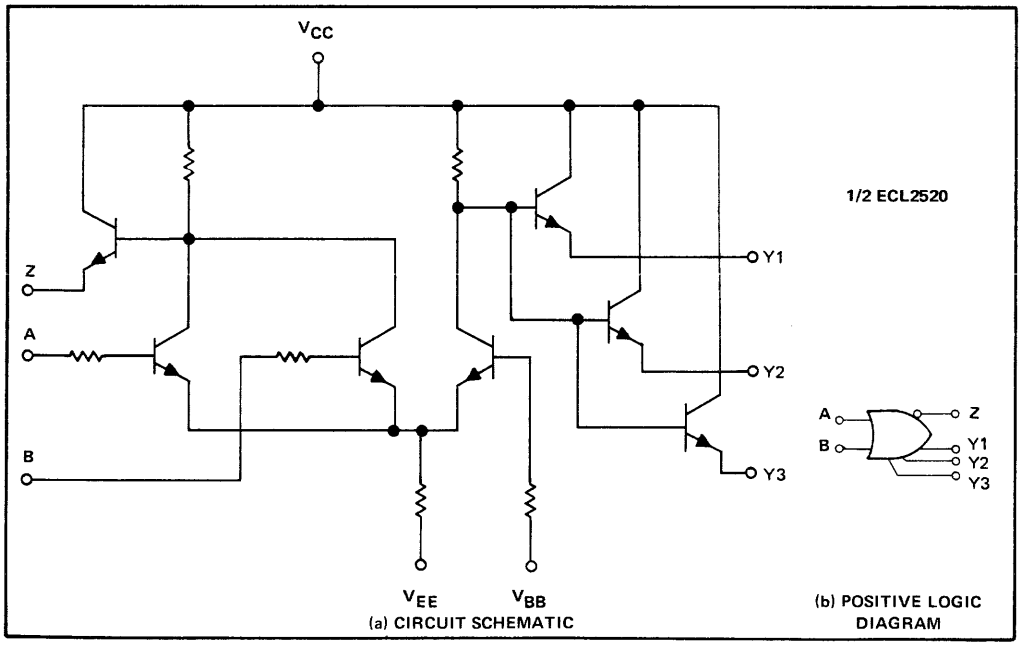
multi-output gates (drivers)

Additional fan-out or drive capability is provided in the ECL2500 Series through the use of gates with multiple emitter-follower outputs on either the in-phase or out-of-phase side of a basic gate. Additional logic flexibility can be obtained via external WIRED-OR connections of emitter-followers from these gates.

There are four dual-gate packages in the family which have gates with as many as four inputs or as many as four emitter-followers. Refer to the ECL2520 through ECL2523 for input/output combinations available.

The multiple emitter-follower circuit diagram and logic diagram is shown in figure 9.

figure 9. multi-output emitter-followers



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

logic-level converters

Two Dual Logic-Level Converters are offered in the ECL2500 Series.

ECL2536	High-Level Logic to ECL
ECL2537	ECL to High-Level Logic (HLL)

The level converters are so designed that the High-Level-Logic inputs or outputs are compatible with standard saturated logic such as TTL, DTL and RTL.

The ECL2536 contains two HLL-to-ECL converters, each having an HLL input and an ECL input. The ECL input is most often used to inhibit the converter. Worst-case HLL-input levels must be $\geq$ 1.2 V and $\leq$ 0.5 V when operating with a V_{CC} of 5.0 V for the input stage.

The ECL2537 contains two ECL-to-HLL converters, each having two ECL inputs. When operating with a V_{CC} = 5.0 V and an external pulldown resistor, the output levels are:

Logical "1"	$\geq$ 3.4 V
Logical "0"	$\leq$ 0.4 V

The external pulldown resistor may be varied to satisfy the current-sinking requirement when driving TTL or DTL. Figure 10(b) shows a typical connection.

storage functions

Storage elements in the ECL2500 Series consist of three Dual "D" type flip-flops, commonly referred to as latches.

The ECL2540 is a dual latch which requires both a negative-going clock and its complement to store data presented at the data (D) input. Each latch has complementary outputs and dissipates the least amount of power ($\approx$ 60 mW) of the latches. Refer to the ECL2540 logic diagram for associated switching-time waveforms.

The ECL2541 and ECL2542 provide single-phase clock operation in addition to built-in gating features. Each latch in the ECL2541 has a single gated input, complementary outputs, plus multi-output emitter followers on one side of the latch. Multiple emitter-followers permit fan-out in two directions. Each latch in the ECL2542 has two gated inputs and a single output.

The ECL2541 and ECL2542 are defined for negative-logic inputs and upon application of a logical "1" (low level) clock the complement of the data presented at the $\overline{D}$ input will appear as output Q. Also, both devices have set and reset inputs which operate independent of the clock. The truth tables and switching waveforms applicable to these devices are shown on the data sheet.

figure 10 (a). TTL to ECL logic-level converter

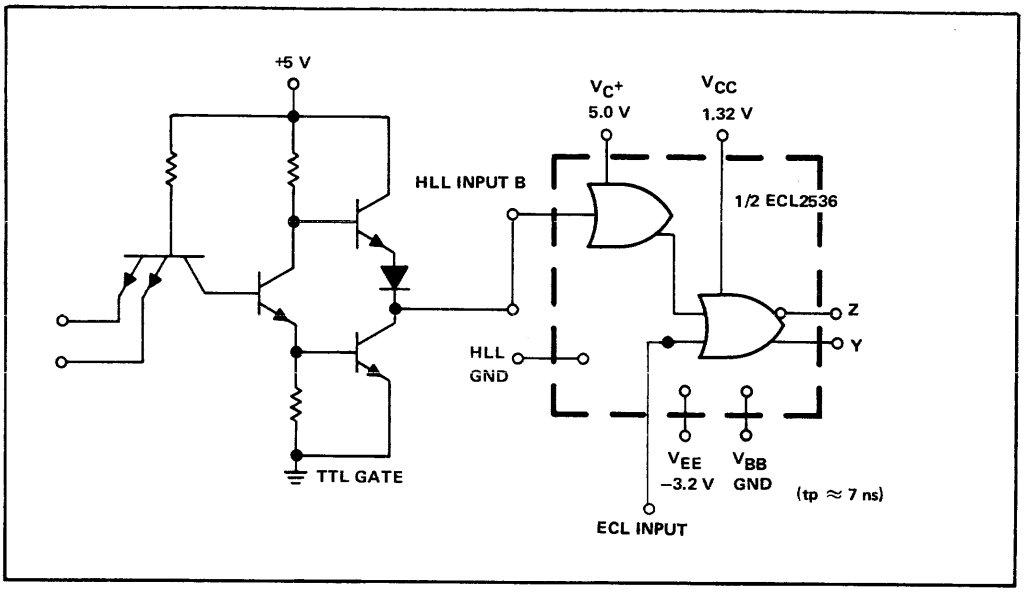
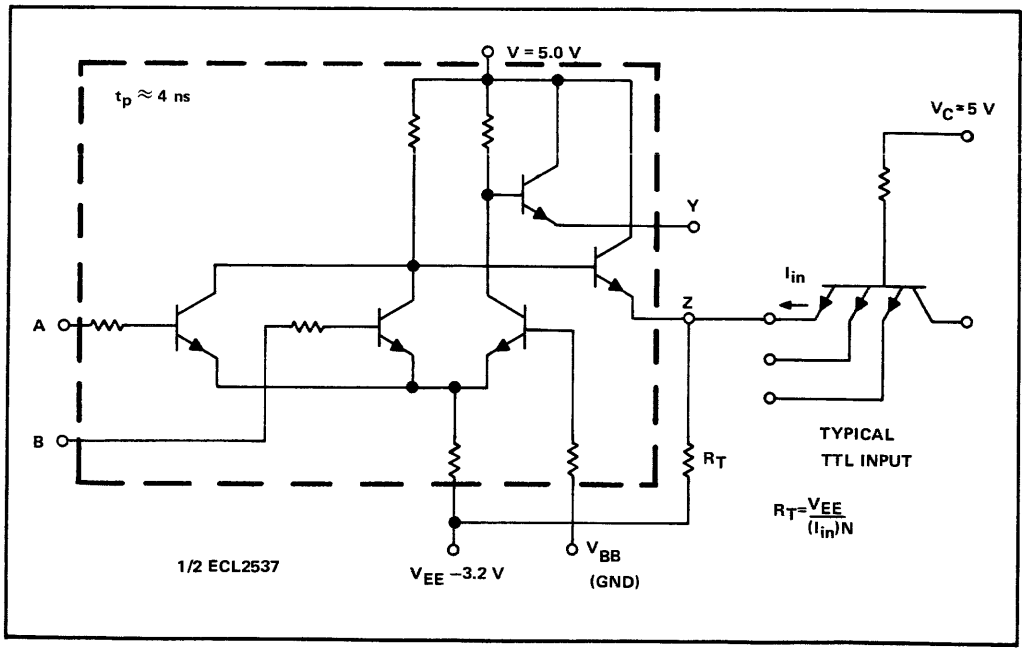


figure 10 (b). ECL to TTL logic-level converter



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES ECL2500 THRU ECL2505, ECL2511
EMITTER-COUPLED-LOGIC GATES

schematic

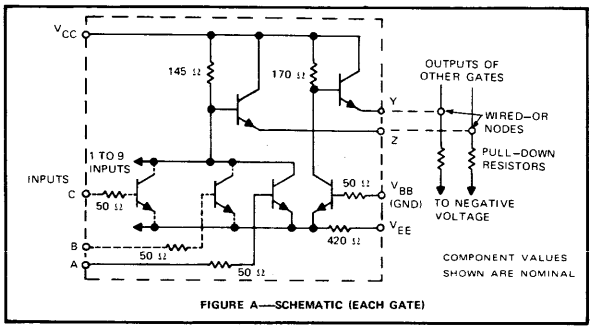


FIGURE A—SCHEMATIC (EACH GATE)

logic

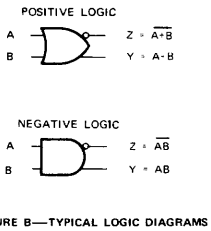


FIGURE B—TYPICAL LOGIC DIAGRAMS

Positive logic OR/NOR functions or negative logic AND/NAND functions are provided at the Y (OR) and Z (NOR) outputs, as shown.

4

Emitter-follower outputs require external pull-down resistors. The wired-OR function can be obtained by connecting emitter-follower outputs of separate gates together. Only one pull-down resistor is required for each wired-OR node.

absolute maximum ratings (see note 1)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Temperature range with supply and bias voltages applied . . . . . −40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Output Y	All inputs high			−40 mA
Output Z	All inputs low			−40 mA

recommended operating conditions

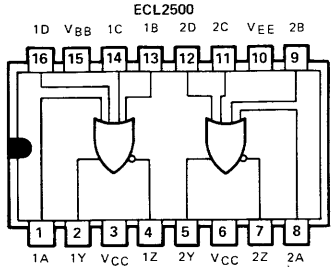
Supply voltage V_{CC} . . . . . 1.32 V ± 2%
Supply voltage V_{EE} . . . . . −3.2 V ± 2%
Reference voltage V_{BB} . . . . . 0 V (GND)
Reverse bias on unused inputs . . . . . −1 V ± 0.5 V
Normalized d-c fan-out . . . . . 0 to 35
Load on each output . . . . . characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range . . . . . 0°C to 75°C

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

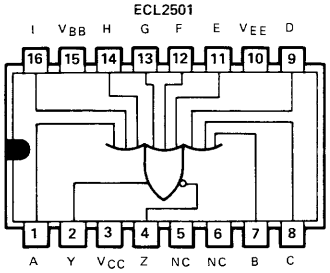
logic

ECL2500



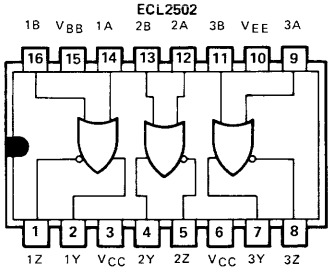
DUAL 4-INPUT OR/NOR GATE

ECL2501



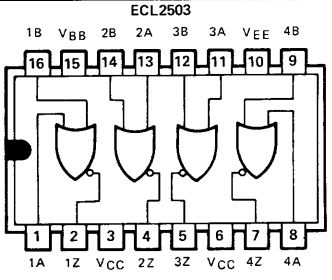
9-INPUT OR/NOR GATE

ECL2502



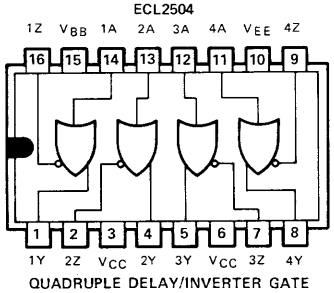
TRIPLE 2-INPUT OR/NOR GATE

ECL2503



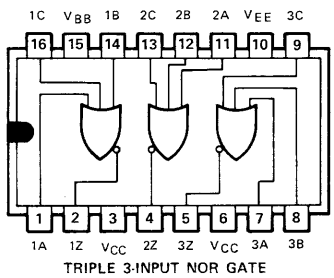
QUADRUPLE 2-INPUT NOR GATE

ECL2504



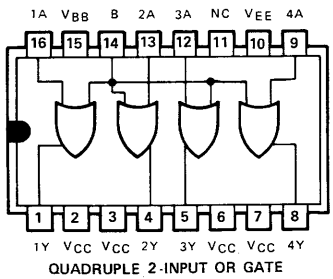
QUADRUPLE DELAY/INVERTER GATE

ECL2505



TRIPLE 3-INPUT NOR GATE

ECL2511



QUADRUPLE 2-INPUT OR GATE

MODULE	POSITIVE LOGIC		NEGATIVE LOGIC	
	Y(OR)	Z(NOR)	Y(AND)	Z(NAND)
ECL2500	A+B+C+D	$\overline{A+B+C+D}$	ABCD	$\overline{ABCD}$
ECL2501	A+B+C+D+E+F+G+H+I	$\overline{A+B+C+D+E+F+G+H+I}$	ABCDEFGHI	$\overline{ABCDEFGHI}$
ECL2502	A+B	$\overline{A+B}$	AB	$\overline{AB}$
ECL2503		$\overline{A+B}$		$\overline{AB}$
ECL2504	A	$\overline{A}$	A	$\overline{A}$
ECL2505		$\overline{A+B+C}$		$\overline{ABC}$
ECL2511	1A+B, 2A+B, 3A+B, 4A+B		1A•B, 2A•B, 3A•B, 4A•B	

NC—No internal connection

truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2500

A	B	C	D	Y	Z
L	L	L	L	L	H
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
H	H	H	H	H	L

ECL2501

A	B	C	D	E	F	G	H	I	Y	Z
L	L	L	L	L	L	L	L	L	L	H
H	X	X	X	X	X	X	X	X	H	L
X	H	X	X	X	X	X	X	X	H	L
X	X	H	X	X	X	X	X	X	H	L
X	X	X	H	X	X	X	X	X	H	L
X	X	X	X	H	X	X	X	X	H	L
X	X	X	X	X	H	X	X	X	H	L
X	X	X	X	X	X	H	X	X	H	L
X	X	X	X	X	X	X	H	X	H	L
X	X	X	X	X	X	X	X	H	H	L
H	H	H	H	H	H	H	H	H	H	L

ECL2502

A	B	Y	Z
L	L	L	H
H	X	H	L
X	H	H	L
H	H	H	L

ECL2503

A	B	Z
L	L	H
H	X	L
X	H	L
H	H	L

ECL2504

A	Y	Z
L	L	H
H	H	L

ECL2505

A	B	C	Z
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L
H	H	H	L

ECL2511

A	B	Y
L	L	L
H	X	H
X	H	H
H	H	H

electrical characteristics at specified free-air temperature

PARAMETER		TEST FIGURE	TEST CONDITIONS*		MODULE ECL2500	ECL2501	ECL2502	ECL2503	ECL2504	ECL2506	ECL2511	SEE NOTE 4 MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage			0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •	150 150 150		720 720 720	mV
V_{IL}	Low-level input voltage			0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •	−1500 −1500 −1500		−150 −150 −150	mV
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.2 V	0°C 25°C 75°C	• • •	• • •	• • •		• • •		• • •	315 350	390 425 495	 500 580	mV
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.2 V	0°C 25°C 75°C	• • •	• • •	• • •		• • •		• • •	−505 −490	−445 −425 −385	 −350 −310	mV
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.2 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	 	315 350	390 425 495	 500 580	mV
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.2 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	 	−420	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.4 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	 	−505 −490	−455 −425 −380	 −315	mV
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.15 V	0°C 25°C 75°C	• • •	• • •	• • •		• • •		• • •	290 325		 	mV
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.15 V	0°C 25°C 75°C	• • •	• • •	• • •		• • •		• • •			 −325 −290	mV
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.15 V	0°C 25°C 75°C				• • •		• • •		290 325		 	mV
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.15 V	0°C 25°C 75°C				• • •		• • •				 −290 −260	mV
I_{IH}	High-level input current (each input)	3	V_I = 0.5 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •			255 235 200	μA
I_{IL}	Low-level input current	4	V_I = −3.2 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •			−0.5† −0.6† −0.9†	μA
I_{CC} or $-I_{EE}$	Supply current	5	V_I = −0.5 V	25°C	• 	 • 	 • 	 • 	 • 	 • 	 •	8 4 13 18 18 13 18		15 8 21 28 28 21 28	mA
C_{in}	Input capacitance (each input)		See Note 5	25°C	•	•	•	•	•	•	•		5		pF
z_{out}	Output impedance		See Note 6	25°C	•	•	•	•	•	•	•		5		Ω

* V_{BB} = GND, V_{CC} = 1.32 V ±1%, V_{EE} = −3.20 V ±1%.

† These are worst-case values for nine inputs in parallel. See Supplementary Parameter Measurement Information for each gate.

NOTES: 4. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

5. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V.

6. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

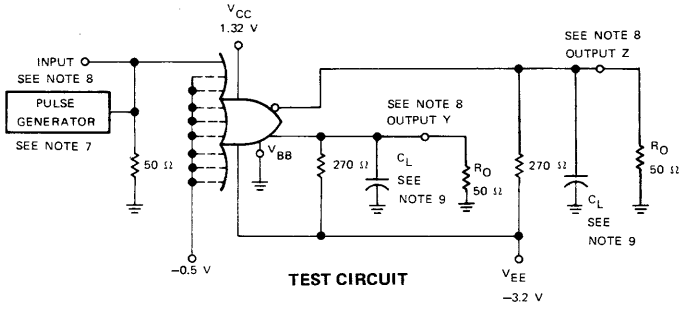
typical operating characteristics at specified free-air temperature (see figure 1)

PARAMETER		C_L	T_A	ECL2500 ECL2502 ECL2504	ECL2501		ECL2503 ECL2505	ECL2511		UNIT
				ANY OUTPUT	Y OUTPUT	Z OUTPUT	ANY OUTPUT	A INPUTS	B INPUT	
				TYP†	TYP†	TYP†	TYP†	TYP†	TYP†	
t_{PHL}	Propagation delay time, high-to-low-level output	4 pF	0°C	2.4	2.4	2.6	2.6	2.4	2.7	ns
			25°C	2.3	2.3	2.4	2.5	2.5	2.8	
			75°C	2.4	2.4	2.6	2.6	2.4	2.7	
	and/or									
t_{PLH}	Propagation delay time, low-to-high-level output	50 pF	0°C	3.5	3.5	3.8	3.8	3.4	3.4	ns
			25°C	3.3	3.3	3.5	3.5	3.6	3.7	
			75°C	3.5	3.5	3.8	3.8	3.4	3.4	
t_{THL}	Transition time, high-to-low-level output	4 pF	0°C	3.3	3.3	5.1	4.3	4.0	4.2	ns
			25°C	3.0	3.0	4.8	4.0	3.8	4.0	
			75°C	3.3	3.3	5.1	4.3	4.0	4.2	
	and/or									
t_{TLH}	Transition time, low-to-high-level output	50 pF	0°C	4.2	4.2	4.7	4.4	4.5	4.7	ns
			25°C	3.9	3.9	4.4	4.1	4.3	4.5	
			75°C	4.2	4.2	4.7	4.4	4.5	4.7	

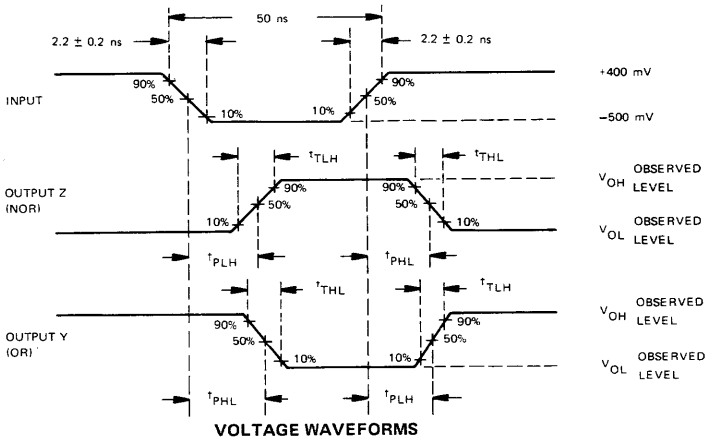
†See Supplementary Parameter Measurement Information for MIN and MAX values at T_A = 25°C.

4

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

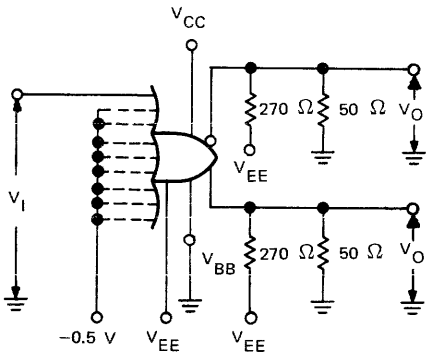


VOLTAGE WAVEFORMS

FIGURE 1—PROPAGATION DELAY AND TRANSITION TIMES

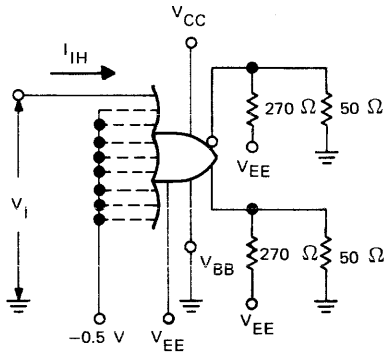
NOTES: 7. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.
8. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistors designated R_O are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.
9. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

PARAMETER MEASUREMENT INFORMATION†



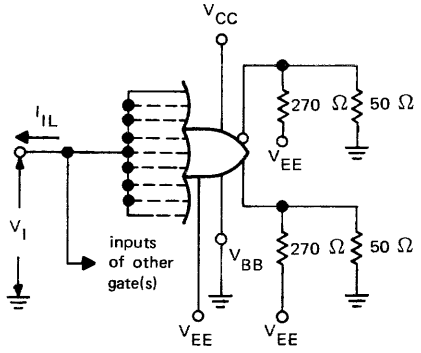
A. V_I is applied to each input separately.
B. Each output is tested separately.

FIGURE 2—V_{OH} AND V_{OL}



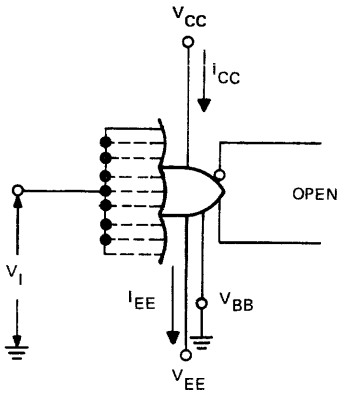
Each input is tested separately.

FIGURE 3—I_{IH}



All inputs of all gates are connected in parallel.

FIGURE 4—I_{IL}



A. All gates are tested simultaneously.
B. I_{CC} is the total current into all V_{CC} terminals.

FIGURE 5—I_{CC} OR I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2500	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	1,13,14,16	2	2	0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
	8,9,11,12	5									
$V_{OL(Y)}$	1,13,14,16	2	2	−0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	−505 −490	−445 −425 −385	−350 −310	mV
	8,9,11,12	5									
$V_{OH(Z)}$	1,13,14,16	4	2	−0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
	8,9,11,12	7									
$V_{OL(Z)}$	1,13,14,16	4	2	0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	−420	−385 −365 −325	−310 −280	mV
	8,9,11,12	7									
$V_{OL(Z)}$	1, 13, 14, 16	4	2	0.4 V	−0.5 V	−0.5 V	0°C 25°C 75°C	−505 −490	−455 −425 −380	−315	mV
	8, 9, 11, 12	7									
$V_{OH(Y)}$	12	5	2	0.15 V	−0.5 V	−0.5 V	0°C 25°C 75°C	290 325			mV
$V_{OL(Y)}$	12	5	2	−0.15 V	−0.5 V	−0.5 V	0°C 25°C 75°C			−325 −290	mV
I_{IH}	1,13,14,16		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
	8,9,11,12										
I_{IL}	1,13,14,16		4	All inputs of both gates in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.5 −0.8	μA
	8,9,11,12										
ECL2501	V_{BB} (pin 15) = GND, V_{CC} (pin 3) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	1,7,8,9,11, 12,13,14,16	2	2	0.2 V	−0.5 V		0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Y)}$	1,7,8,9,11, 12,13,14,16	2	2	−0.2 V	−0.5 V		0°C 25°C 75°C	−505 −490	−455 −425 −385	−350 −310	mV
$V_{OH(Z)}$	1,7,8,9,11, 12,13,14,16	4	2	−0.2 V	−0.5 V		0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	1,7,8,9,11, 12,13,14,16	4	2	0.2 V	−0.5 V		0°C 25°C 75°C	420	385 365 325	310 280	mV
$V_{OL(Z)}$	1,7,8,9,11, 12,13,14,16	4	2	0.4 V	−0.5 V		0°C 25°C 75°C	−505 −490	455 425 380	315	mV
$V_{OH(Y)}$	1	2	2	0.15 V	−0.5 V		0°C 25°C 75°C	290 325			mV
$V_{OL(Y)}$	1	2	2	−0.15 V	−0.5 V		0°C 25°C 75°C			−325 −290	mV
I_{IH}	1,7,8,9,11, 12,13,14,16		3	0.5 V	−0.5 V		0°C 25°C 75°C			255 235 200	μA
I_{IL}	1,7,8,9,11, 12,13,14,16		4	All inputs in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.6 −0.9	μA

NOTES: 10. See page 4 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATES					
ECL2502	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	14,16	2	2	0.2 V	−0.5 V	−0.5 V	0°C	315	390		mV
	12,13	4					25°C	350	425	500	
	9,11	7					75°C		495	580	
$V_{OL(Y)}$	14,16	2	2	−0.2 V	−0.5 V	−0.5 V	0°C	−505	−445		mV
	12,13	4					25°C	−490	−425	−350	
	9,11	7					75°C		−385	−310	
$V_{OH(Z)}$	14,16	1	2	−0.2 V	−0.5 V	−0.5 V	0°C	315	390		mV
	12,13	5					25°C	350	425	500	
	9,11	8					75°C		495	580	
$V_{OL(Z)}$	14,16	1	2	0.2 V	−0.5 V	−0.5 V	0°C		−385		mV
	12,13	5					25°C	−420	−365	−310	
	9,11	8					75°C		−325	−280	
$V_{OL(Z)}$	14,16	1	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−455		mV
	12,13	5					25°C	−490	−425		
	9,11	8					75°C		−380	−315	
$V_{OH(Y)}$	11	7	2	0.15 V	−0.5 V	−0.5 V	0°C	290			mV
							25°C	325			
							75°C				
$V_{OL(Y)}$	11	7	2	−0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−325	
							75°C			−290	
I_{IH}	14,16		3	0.5 V	−0.5 V	−0.5 V	0°C				μA
	12,13						25°C			255	
	9,11						75°C			235	
										200	
I_{IL}	14,16		4	All inputs of all gates in parallel at −3.2 V			0°C				μA
	12,13						25°C			−0.5	
	9,11						75°C			−0.5	
										−0.6	
ECL2503	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Z)}$	1,16	2	2	−0.2 V	−0.5 V	−0.5 V	0°C	315	390		mV
	13,14	4					25°C	350	425	500	
	11,12	5					75°C		495	580	
	8,9	7									
$V_{OL(Z)}$	1,16	2	2	0.2 V	−0.5 V	−0.5 V	0°C		−385		mV
	13,14	4					25°C	−420	−365	−310	
	11,12	5					75°C		−325	−280	
	8,9	7									
$V_{OL(Z)}$	1,16	2	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−455		mV
	13,14	4					25°C	−490	−425		
	11,12	5					75°C		−380	−315	
	8,9	7									
$V_{OH(Z)}$	9	7	2	−0.15 V	−0.5 V	−0.5 V	0°C	290			mV
							25°C	325			
							75°C				
$V_{OL(Z)}$	9	7	2	0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−290	
							75°C			−260	
I_{IH}	1,16		3	0.5 V	−0.5 V	−0.5 V	0°C				μA
	13,14						25°C			255	
	11,12						75°C			235	
	8,9									200	
I_{IL}	1,16		4	All inputs of all gates in parallel at −3.2 V			0°C				μA
	13,14						25°C			−0.5	
	11,12						75°C			−0.5	
	8,9									−0.8	

NOTES: 10. See page 4 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATES					
ECL2504	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	14	1	2	0.2 V		−0.5 V	0°C	315	390		mV
	13	4					25°C	350	425	500	
	12	5					75°C		495	580	
	11	8									
$V_{OL(Y)}$	14	1	2	−0.2 V		−0.5 V	0°C	-505	−445		mV
	13	4					25°C	−490	−425	−350	
	12	5					75°C		−385	−310	
	11	8									
$V_{OH(Z)}$	14	16	2	−0.2 V		−0.5 V	0°C	315	390		mV
	13	2					25°C	350	425	500	
	12	7					75°C		495	580	
	11	9									
$V_{OL(Z)}$	14	16	2	0.2 V		−0.5 V	0°C		−385		mV
	13	2					25°C	-420	-365	-310	
	12	7					75°C		-325	-280	
	11	9									
$V_{OL(Z)}$	14	16	2	0.4 V		−0.5 V	0°C	-505	−455		mV
	13	2					25°C	−490	−425		
	12	7					75°C		−380	−315	
	11	9									
$V_{OH(Y)}$	13	4	2	0.15 V		−0.5 V	0°C	290			mV
							25°C	325			
							75°C				
$V_{OL(Y)}$	13	4	2	−0.15 V		−0.5 V	0°C				mV
							25°C			325	
							75°C			−290	
I_{IH}	14		3	0.5 V		−0.5 V	0°C				μA
	13						25°C			255	
	12						75°C			235	
	11									200	
I_{IL}	14		4	Inputs of all gates in parallel at −3.2 V			0°C				μA
	13						25°C			−0.5	
	12						75°C			−0.5	
	11									−0.5	
ECL2505	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Z)}$	1,14,16	2	2	−0.2 V	−0.5 V	−0.5 V	0°C	315	390		mV
	11,12,13	4					25°C	350	425	500	
	7,8,9	5					75°C		495	580	
$V_{OL(Z)}$	1,14,16	2	2	0.2 V	−0.5 V	−0.5 V	0°C		−385		mV
	11,12,13	4					25°C	-420	-365	-310	
	7,8,9	5					75°C		-325	-280	
$V_{OL(Z)}$	1,14,16	2	2	0.4 V	−0.5 V	−0.5 V	0°C	-505	−455		mV
	11,12,13	4					25°C	−490	−425		
	7,8,9	5					75°C		−380	-315	
$V_{OH(Z)}$	9	5	2	−0.15 V	−0.5 V	−0.5 V	0°C	290			mV
							25°C	325			
							75°C				
$V_{OL(Z)}$	9	5	2	0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−290	
							75°C			−260	
I_{IH}	1,14,16		3	0.5 V	−0.5 V	−0.5 V	0°C				μA
	11,12,13						25°C			255	
	7,8,9						75°C			235	
										200	
I_{IL}	1,14,16		4	All inputs of all gates in parallel at −3.2 V			0°C				μA
	11,12,13						25°C			−0.5	
	7,8,9						75°C			−0.6	
										−0.9	

NOTES: 10. See page 4 for defining term associated with each symbol.

11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATES					
ECL2511	V_{BB} (pin 15) = GND, V_{CC} (pin 2, pin 3, pin 6, and pin 7) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	16,14	1	2	0.2 V	−0.5 V	−0.5 V	0°C	315	390		mV
	13,14	4					25°C	350	425	500	
	12,14	5					75°C		495	580	
	9,14	8									
$V_{OL(Y)}$	16,14	1	2	−0.2 V	−0.5 V	−0.5 V	0°C	−505	−445		mV
	13,14	4					25°C	−490	−425	−350	
	12,14	5					75°C		−385	−310	
	9,14	8									
$V_{OH(Y)}$	16	1	2	0.15 V	−0.5 V	−0.5 V	0°C	290			mV
							25°C	325			
							75°C				
$V_{OL(Y)}$	16	1	2	−0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−325	
							75°C			−290	
I_{IH}	16		3	0.5 V	−0.5 V	−0.5 V	0°C			255	mV
	13						25°C			235	
	12						75°C			200	
	9										
	14		3	0.5 V	−0.5 V		0°C			1020	μA
							25°C			940	
							75°C			800	
I_{IL}	16		4	All inputs of all gates in parallel at −3.2 V			0°C			−0.5	μA
	13						25°C			−0.5	
	12						75°C			−0.8	
	9										
	14										

NOTES: 10. See page 4 for defining term associated with each symbol.

11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

GENERAL APPLICATION INFORMATION

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

Applications of the ECL2500 basic gates at other than data sheet conditions are covered in a separate family application document.

General loading for fan-out may be divided into two classes:

CLASS I — **Short-Line or Cluster Loading.**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II — **Long-Line or Distributive Loading.**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and CLASS I loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

operating characteristics at specified free-air temperature (see figure 1)

TERMINALS TO BE TESTED (SEE NOTES 12, 13, AND 14)				C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns						t_{THL} and/or t_{TLH} TRANSITION TIMES—ns					
					$T_A = 0°C$			$T_A = 25°C$			$T_A = 75°C$			$T_A = 0°C$			$T_A = 25°C$			$T_A = 75°C$		
INPUT	OUTPUT	INPUT	OUTPUT	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2500																						
1, 13, 14, 16	2, 4	8, 9, 11, 12	5, 7	4		2.4			1.5	2.3	3.3		2.4		3.3			1.7	3.0	4.7		3.3
				50		3.5			2.4	3.3	4.4		3.5		4.2			2.5	3.9	6.5		4.2
ECL2501																						
1,7,8, 9,11, 12,13, 14,16	2			4		2.4			1.5	2.3	3.3		2.4		3.3			1.7	3.0	4.7		3.3
				50		3.5			2.4	3.3	4.4		3.5		4.2			2.5	3.9	6.5		4.2
1,7,8, 9,11, 12,13, 14,16	4			4		2.6			1.6	2.4	3.4		2.6		5.1			2.8	4.8	6.5		5.1
				50		3.8			2.4	3.5	4.5		3.8		4.7			2.8	4.4	6.5		4.7
ECL2502																						
2, 14,16	1	4, 12,13	5	4		2.4			1.5	2.3	3.3		2.4		3.3			1.7	3.0	4.7		3.3
				50		3.5			2.4	3.3	4.4		3.5		4.2			2.5	3.9	6.5		4.2
		7, 9,11	8																			
ECL2503																						
1, 16	2	13, 14	4	4		2.6			1.7	2.5	3.5		2.6		4.3			2.8	4.0	5.6		4.3
				50		3.8			2.4	3.5	4.5		3.8		4.4			2.8	4.1	6.5		4.4
11, 12	5	8, 9	7																			
ECL2504																						
14	1, 16	13	4, 2	4		2.4			1.5	2.3	3.3		2.4		3.3			1.7	3.0	4.7		3.3
				50		3.5			2.4	3.3	4.4		3.5		4.2			2.5	3.9	6.5		4.2
12	5, 7	11	8, 9																			
ECL2505																						
1, 14, 16	2	11, 12, 13	4	4		2.6			1.7	2.5	3.5		2.6		4.3			2.8	4.0	5.6		4.3
				50		3.8			2.4	3.5	4.5		3.8		4.4			2.8	4.1	6.5		4.4
7, 8, 9	5																					
ECL2511																						
16	1	13	4	4		2.4			1.7	2.5	3.5		2.4		4.0			2.6	3.8	5.2		4.0
				50		3.4			2.4	3.6	4.5		3.4		4.5			2.6	4.3	6.5		4.5
12	5	9	8																			
14	1	14	4	4		2.7			1.9	2.8	3.7		2.7		4.2			2.6	4.0	5.4		4.2
				50		3.4			2.7	3.7	4.9		3.4		4.7			2.6	4.5	6.5		4.7
14	5	14	8																			

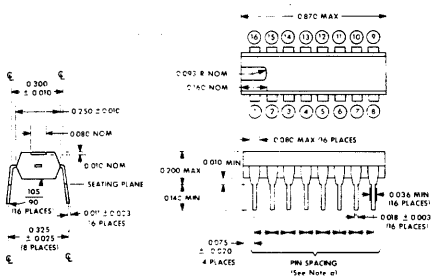
NOTES: 12. Each gate is tested separately.
13. The input pulse is measured as it is applied sequentially to each input of the gate under test and a waveform measurement is made at each of the outputs of that gate. Times are as defined in Figure 1.
14. Bias voltages and loads for the gate under test are shown in Figure 1. Unused gates have inputs biased to −0.5 V, outputs under load, and power applied.

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

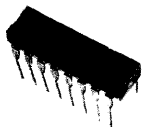
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES a. The true position pin spacing is 0.100 between center lines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted



terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams on page 3.
Outputs are denoted Y or Z. Inputs are denoted A, B, C, etc.
Respective inputs and outputs are identified by a gate number preceding the pin symbol.
Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.
NC indicates no internal connection.

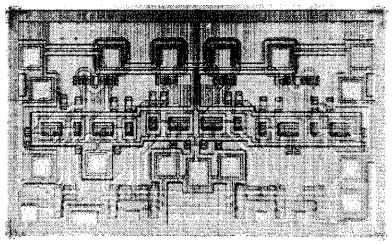
PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2500	1A	1Y	V_{CC}	1Z	2Y	V_{CC}	2Z	2A	2B	V_{EE}	2C	2D	1B	1C	V_{BB}	1D
ECL2501	A	Y	V_{CC}	Z	NC	NC	B	C	D	V_{EE}	E	F	G	H	V_{BB}	I
ECL2502	1Z	1Y	V_{CC}	2Y	2Z	V_{CC}	3Y	3Z	3A	V_{EE}	3B	2A	2B	1A	V_{BB}	1B
ECL2503	1A	1Z	V_{CC}	2Z	3Z	V_{CC}	4Z	4A	4B	V_{EE}	3A	3B	2A	2B	V_{BB}	1B
ECL2504	1Y	2Z	V_{CC}	2Y	3Y	V_{CC}	3Z	4Y	4Z	V_{EE}	4A	3A	2A	1A	V_{BB}	1Z
ECL2505	1A	1Z	V_{CC}	2Z	3Z	V_{CC}	3A	3B	3C	V_{EE}	2A	2B	2C	1B	V_{BB}	1C
ECL2511	1Y	V_{CC}	V_{CC}	2Y	3Y	V_{CC}	V_{CC}	4Y	4A	V_{EE}	NC	3A	2A	B	V_{BB}	1A

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES ECL2506 THRU ECL2510, ECL2512, ECL2513 MULTIFUNCTION EMITTER-COUPLED-LOGIC GATES

ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) MULTIFUNCTION GATES FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS



description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.

The ECL2500 family includes:

- Basic Gate Modules
- **Multifunction Gate Modules**
- Bistable Modules
- Arithmetic Modules
- Interface Modules
- Memory Module

family features

- High speed . . . typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ±225 mV typical at 25°C

This data sheet covers the multifunction-gate modules. Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series multifunction gates

The seven ECL2500 series modules that form the multifunction gate group are shown in the table below. These modules contain various combinations of the multifunction ECL circuit shown in the schematic of Figure A and the logic diagrams of Figure B.

SUMMARY OF MODULES IN MULTIFUNCTION GATE GROUP

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS PER MODULE	
				Y	Z
ECL2506	4	3	NOR-OR		1
ECL2507	5	2	NOR-OR		1
ECL2508	6	2	NOR-OR		1
ECL2509	4	2	OR-AND/NOR-OR	1	1
ECL2510	4	3,3,3,2	OR-AND/NOR-OR	1	1
ECL2512	6	2 (1 common to each 2 gates)	NOR-OR		2
ECL2513	4	2 (1 common to 2 gates)	OR-AND/NOR-OR	2	2

schematic

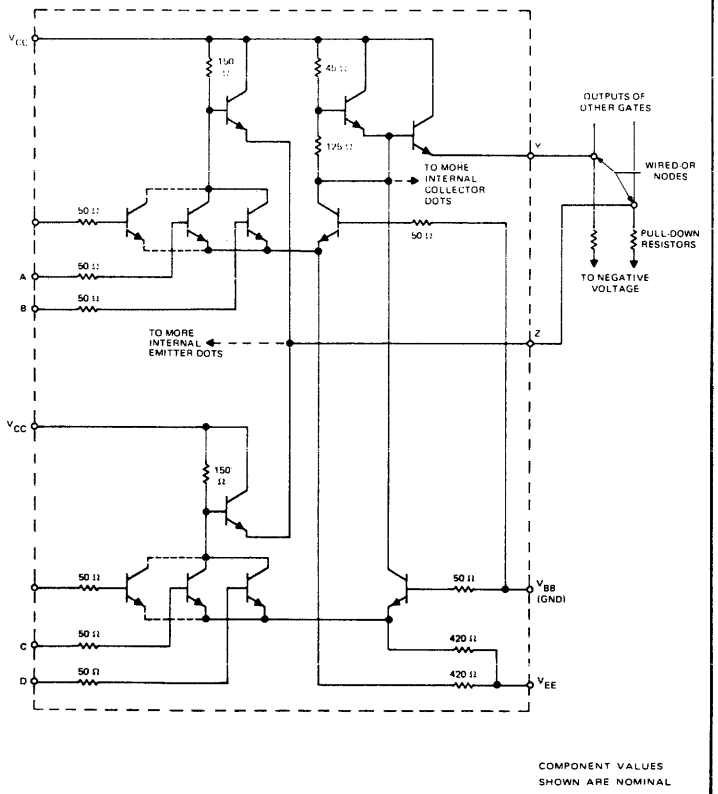


FIGURE A – TYPICAL SCHEMATIC

logic

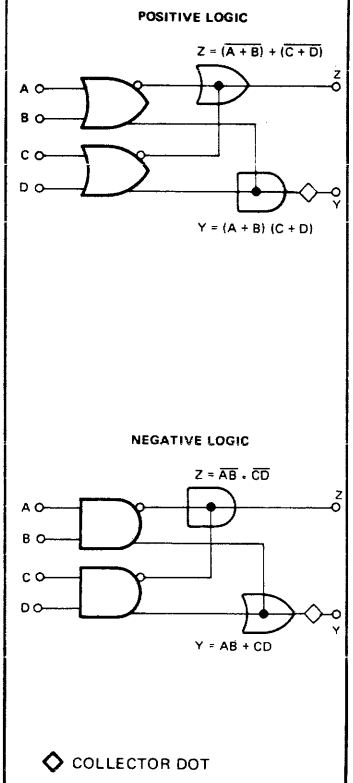


FIGURE B – TYPICAL LOGIC DIAGRAMS

Positive logic OR-AND/NOR-OR functions or negative logic AND-OR/NAND-AND functions are provided at the Y and Z outputs, as shown.

Emitter-follower outputs require an external pull-down resistor. The wired-OR function can be obtained by connecting emitter-follower outputs of separate gates together. Only one pull-down resistor is required for each wired-OR node.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2506

INPUTS												OUTPUT
A	B	C	D	E	F	G	H	I	J	K	L	Z
L	L	L	X	X	X	X	X	X	X	X	X	H
X	X	X	L	L	L	X	X	X	X	X	X	H
X	X	X	X	X	X	L	L	L	X	X	X	H
X	X	X	X	X	X	X	X	X	L	L	L	H
For a LOW output, at least one input of each gate must be HIGH												
H	X	X	H	X	X	H	X	X	H	X	X	L
X	H	X	X	H	X	X	H	X	X	H	X	L
X	X	H	X	X	H	X	X	H	X	X	H	L

ECL2507

INPUTS										OUTPUT
A	B	C	D	E	F	G	H	I	J	Z
L	L	X	X	X	X	X	X	X	X	H
X	X	L	L	X	X	X	X	X	X	H
X	X	X	X	L	L	X	X	X	X	H
X	X	X	X	X	X	L	L	X	X	H
X	X	X	X	X	X	X	X	L	L	H
For a LOW output, at least one input of each gate must be HIGH										
H	X	H	X	H	X	H	X	H	X	L
X	H	X	H	X	H	X	H	X	H	L

ECL2508

INPUTS												OUTPUT
A	B	C	D	E	F	G	H	I	J	K	L	Z
L	L	X	X	X	X	X	X	X	X	X	X	H
X	X	L	L	X	X	X	X	X	X	X	X	H
X	X	X	X	L	L	X	X	X	X	X	X	H
X	X	X	X	X	X	L	L	X	X	X	X	H
X	X	X	X	X	X	X	X	L	L	X	X	H
X	X	X	X	X	X	X	X	X	X	L	L	H
For a LOW output, at least one input of each gate must be HIGH												
H	X	H	X	H	X	H	X	H	X	H	X	L
X	H	X	H	X	H	X	H	X	H	X	H	L

ECL2509

INPUTS								OUTPUTS	
A	B	C	D	E	F	G	H	Y	Z
L	L	X	X	X	X	X	X	L	H
X	X	L	L	X	X	X	X	L	H
X	X	X	X	L	L	X	X	L	H
X	X	X	X	X	X	L	L	L	H
For a HIGH Y and LOW Z, at least one input of each gate must be HIGH									
H	X	H	X	H	X	H	X	H	L
X	H	X	H	X	H	X	H	H	L

ECL2510

INPUTS										OUTPUTS	
A	B	C	D	E	F	G	H	I	J	K	Y	Z
L	L	X	X	X	X	X	X	X	X	X	L	H
X	X	L	L	L	X	X	X	X	X	X	L	H
X	X	X	X	X	L	L	L	X	X	X	L	H
X	X	X	X	X	X	X	X	L	L	L	L	H
For a HIGH Y and LOW Z, at least one input of each gate must be HIGH												
H	X	H	X	X	H	X	X	H	X	X	H	L
X	H	X	H	X	X	H	X	X	H	X	H	L
X	H	X	X	H	X	X	H	X	X	H	H	L

ECL2512

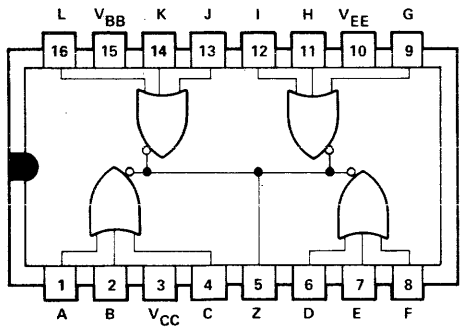
INPUTS												OUTPUTS	
1A	D	1B	E	1C	F	2A	D	2B	E	2C	F	1Z	2Z
L	L	X	X	X	X		L					H	Determined
X	X	L	L	X	X				L			H	by inputs
X	X	X	X	L	L						L	H	2A,2B,2C,
H	X	H	X	H	X							L	D,E, and F.
X	H	X	H	X	H		H		H		H	L	(See below)
	L					L	L	X	X	X	X	Determined	H
			L			X	X	L	L	X	X	by inputs	H
					L	X	X	X	X	L	L	1A,1B,1C,	H
						H	X	H	X	H	X	D,E, and F.	L
	H		H		H	X	H	X	H	X	H	(See above)	L
For a LOW output from either section, at least one input of each gate in that section must be HIGH													

ECL2513

INPUTS								OUTPUTS	
1A	1B	1C	D	2A	2B	2C	D	1Y 1Z	2Y 2Z
L	L	X	X					L H	Determined
X	X	L	L				L	L H	by inputs
H	X	H	X					H L	2A,2B,2C, and D.
X	H	X	H				H	H L	(See below)
				L	L	X	X	Determined	L H
			L	X	X	L	L	by inputs	L H
				H	X	H	X	1A,1B,1C, and D.	H L
			H	X	H	X	H	(See above)	H L
For a HIGH Y and LOW Z from either section, at least one input of each gate in that section must be HIGH									

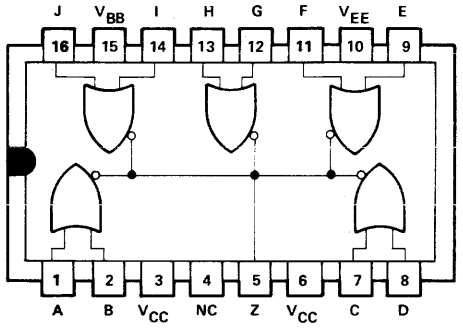
logic

ECL2506



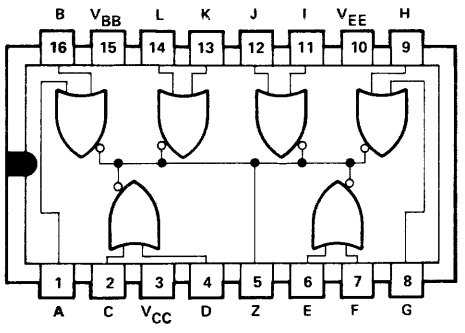
4-WIDE 3-INPUT NOR-OR GATE

ECL2507



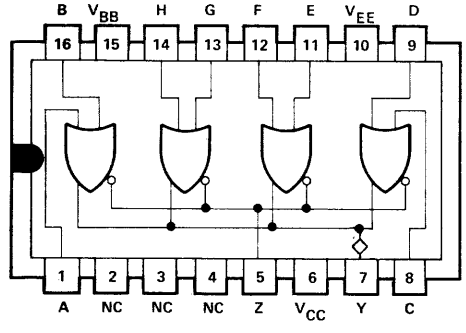
5-WIDE 2-INPUT NOR-OR GATE

ECL2508



6-WIDE 2-INPUT NOR-OR GATE

ECL2509



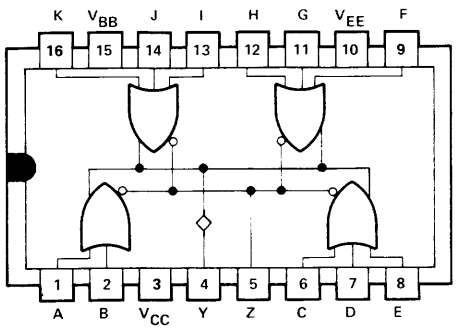
4-WIDE 2-INPUT
OR-AND/NOR-OR GATE

NC—No internal connection

◇ — Collector Dot

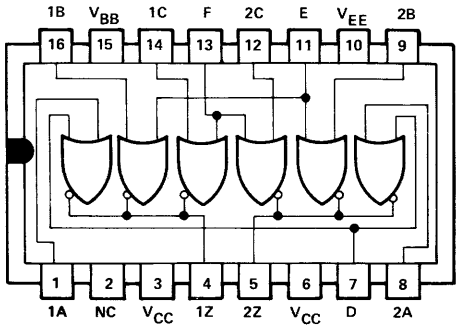
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

ECL2510



4-WIDE 3-3-3-2 INPUT
OR-AND/NOR-OR GATE

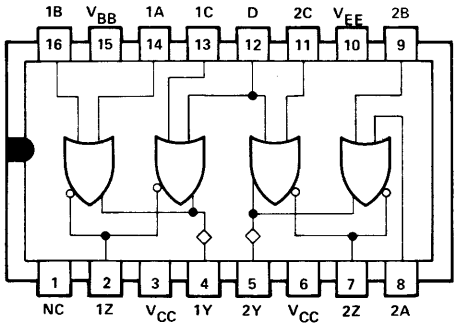
ECL2512



DUAL 3-WIDE 2-INPUT NOR-OR GATE
WITH COMMON INPUTS

4

ECL2513



DUAL 2-WIDE 2-INPUT OR-AND/NOR-OR GATE
WITH COMMON INPUT

MODULE	POSITIVE LOGIC		NEGATIVE LOGIC	
	Y	Z	Y	Z
ECL2506		$\overline{A+B+C} + \overline{D+E+F} + \overline{G+H+I} + \overline{J+K+L}$		$\overline{ABC} \cdot \overline{DEF} \cdot \overline{GHI} \cdot \overline{JKL}$
ECL2507		$\overline{A+B} + \overline{C+D} + \overline{E+F} + \overline{G+H} + \overline{I+J}$		$\overline{AB} \cdot \overline{CD} \cdot \overline{EF} \cdot \overline{GH} \cdot \overline{IJ}$
ECL2508		$\overline{A+B} + \overline{C+D} + \overline{E+F} + \overline{G+H} + \overline{I+J} + \overline{K+L}$		$\overline{AB} \cdot \overline{CD} \cdot \overline{EF} \cdot \overline{GH} \cdot \overline{IJ} \cdot \overline{KL}$
ECL2509	(A+B) (C+D) (E+F) (G+H)	$\overline{A+B} + \overline{C+D} + \overline{E+F} + \overline{G+H}$	AB + CD + EF + GH	$\overline{AB} \cdot \overline{CD} \cdot \overline{EF} \cdot \overline{GH}$
ECL2510	(A+B) (C+D+E) (F+G+H) (I+J+K)	$\overline{A+B} + \overline{C+D+E} + \overline{F+G+H} + \overline{I+J+K}$	AB + CDE + FGH + IJK	$\overline{AB} \cdot \overline{CDE} \cdot \overline{FGH} \cdot \overline{IJK}$
ECL2512		$\overline{A+D} + \overline{B+E} + \overline{C+F}$		$\overline{AD} \cdot \overline{BE} \cdot \overline{CF}$
ECL2513	(A+B) (C+D)	$\overline{A+B} + \overline{C+D}$	AB + CD	$\overline{AB} \cdot \overline{CD}$

NC—No internal connection ◇— Collector Dot

969

GENERAL APPLICATION INFORMATION

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

Applications of the multifunction gates at other than data sheet conditions are covered in a separate ECL2500 series application document.

The multifunction gates divide into two groups with internal wired connections as follows:

MODULE	COLLECTOR DOTS	EMITTER DOTS
ECL2513†	2	2
ECL2509	4	4
ECL2510	4	4

†Each half

MODULE	EMITTER DOTS
ECL2512†	3
ECL2506	4
ECL2507	5
ECL2508	6

†Each half

General loading for fan-out may be divided into two classes:

CLASS I **Short-Line or Cluster Loading.**

Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II **Long-Line or Distributive Loading.**

These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and CLASS I loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings (see note 1)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Temperature range with supply and bias voltages applied . . . . . −40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Output Y	All inputs high			−40 mA
Output Z	All inputs low			−40 mA

4

recommended operating conditions

Supply voltage V_{CC} . . . . . 1.32 V ± 2%
Supply voltage V_{EE} . . . . . −3.2 V ± 2%
Reference voltage V_{BB} . . . . . 0 V (GND)
Reverse bias on unused inputs . . . . . −1 V ± 0.5 V
Normalized d-c fan-out . . . . . 0 to 35
Load on each output . . . . . characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range . . . . . 0°C to 75°C

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

electrical characteristics at specified free-air temperature

PARAMETER		TEST FIGURE	TEST CONDITIONS*		MODULE ECL2506	ECL2507	ECL2508	ECL2509	ECL2510	ECL2512	ECL2513	SEE NOTE 4 MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage			0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •	150 150 150		720 720 720	mV
V_{IL}	Low-level input voltage			0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •	−1500 −1500 −1500		−150 −150 −150	mV
$V_{OH(Y)}$	High-level output voltage at Y output	2	V_I = 0.2 V	0°C 25°C 75°C				• •	• •		• •	315 350	390 425 495	500 580	mV
$V_{OL(Y)}$	Low-level output voltage at Y output	2	V_I = −0.2 V	0°C 25°C 75°C				• •	• •		• •	−505 −490	−450 −410 −290	−350 −230	mV
$V_{OH(Z)}$	High-level output voltage at Z output	2	V_I = −0.2 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	Low-level output voltage at Z output	2	V_I = 0.2 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •	−440	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	Low-level output voltage at Z output	2	V_I = 0.4 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •	−505 −490	−455 −425 −380	−315	mV
$V_{OH(Z)}$	High-level output voltage at Z output	2	V_I = −0.5 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •			630† 700†	mV
$V_{OH(Y)}$	High-level output voltage at Y output	2	V_I = 0.15 V	0°C 25°C 75°C				• •	• •		• •	290 325			mV
$V_{OL(Y)}$	Low-level output voltage at Y output	2	V_I = −0.15 V	0°C 25°C 75°C				• •	• •		• •			−335 −215	mV
$V_{OH(Z)}$	High-level output voltage at Z output	2	V_I = −0.15 V	0°C 25°C 75°C	• • •	• • •	• • •			• •		290 325			mV
$V_{OL(Z)}$	Low-level output voltage at Z output	2	V_I = 0.15 V	0°C 25°C 75°C	• • •	• • •	• • •			• •				−290 −260	mV
I_{IH}	High-level input current (each input)	3	V_I = 0.5 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •			255 235 200	μA
I_{IL}	Low-level input current	4	V_I = −3.2 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •			−0.6‡ −0.8‡ −1.2‡	μA
I_{CC} or $-I_{EE}$	Supply current	5	V_I = −0.5 V	25°C	• • • • • • •	• • • • • • •	• • • • • • •	• • • • • • •	• • • • • • •	• • • • • • •	• • • • • • •	17 23 27 17 17 27 17		28 35 42 28 28 42 28	mA
C_{in}	Input capacitance (each input)		See Note 5	25°C	•	•	•	•	•	•	•		5		pF
z_{out}	Output impedance		See Note 6	25°C	•	•	•	•	•	•	•		5		Ω

*V_{BB} = GND, V_{CC} = 1.32 V ± 1%, V_{EE} = −3.20 V ± 1%.

†These are worst case values for ECL2508 which has six emitters dotted. See Supplementary Parameter Measurement Information for each module.

‡These are worst-case values for twelve inputs in parallel. See Supplementary Parameter Measurement Information for each module.

NOTES: 4. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

5. C_{in} is measured using peak current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V.

6. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

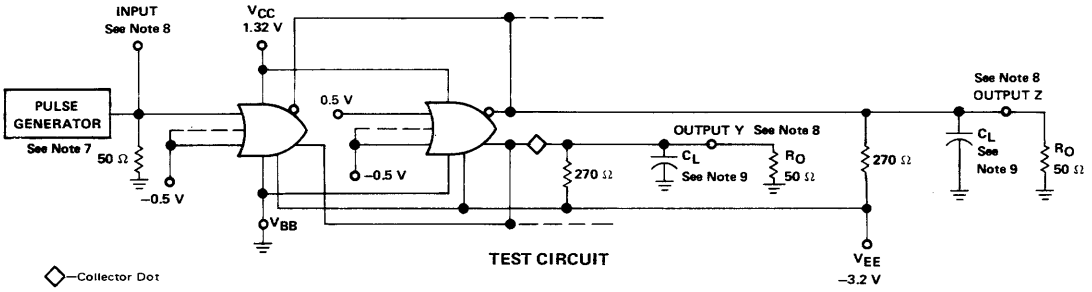
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operating characteristics at specified free-air temperature (see figure 1)

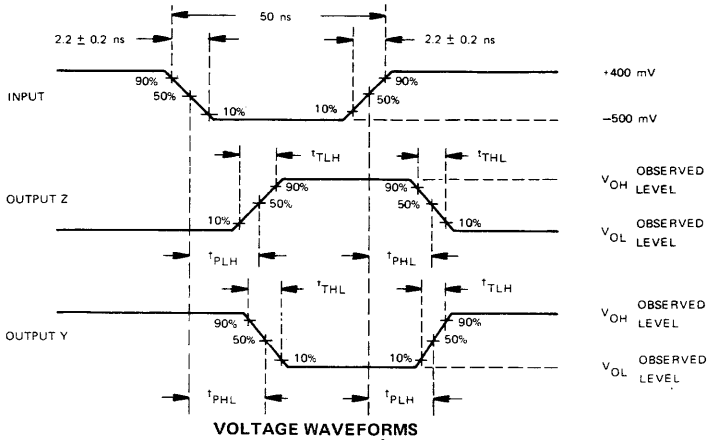
PARAMETER		C_L	T_A	ECL2506 THRU ECL2508, ECL2512			ECL2509, ECL2510, ECL2513			UNIT
				Z OUTPUTS			ANY OUTPUT			
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation delay time, high-to-low-level output and/or Propagation delay time, low-to-high-level output	4 pF	0°C		2.6			2.6		ns
			25°C	1.7	2.6	3.5	1.6	2.6	4.1	
			75°C		2.6			2.6		
t_{PLH}		50 pF	0°C		3.6			3.5		ns
			25°C	2.4	3.6	4.5	2.5	3.5	4.6	
			75°C		3.6			3.6		
t_{THL}	Transition time, high-to-low-level output and/or Transistion time, low-to-high-level output	4 pF	0°C		4.0			3.4		ns
			25°C	2.8	4.0	5.6	2.0	3.4	6.3	
			75°C		4.1			3.5		
t_{TLH}		50 pF	0°C		4.5			4.4		ns
			25°C	2.8	4.5	6.5	2.5	4.3	6.5	
			75°C		4.4			4.1		

4

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

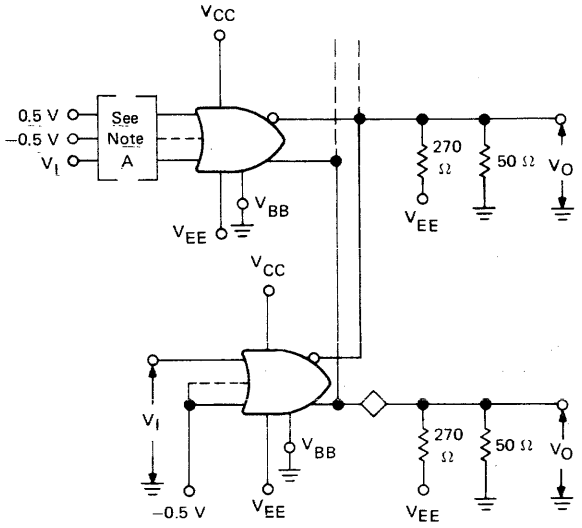


VOLTAGE WAVEFORMS

FIGURE 1–PROPAGATION DELAY AND TRANSITION TIMES

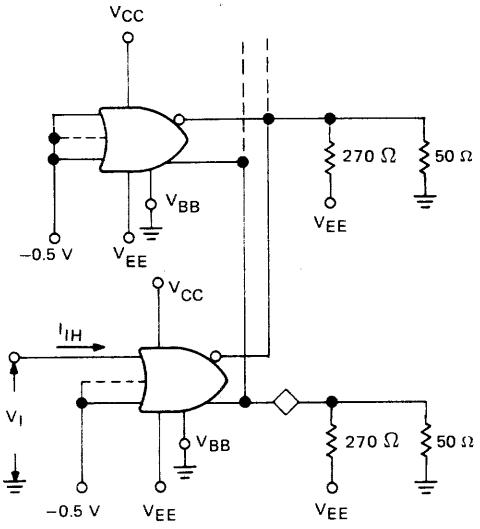
NOTES: 7. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.
8. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistors designated R_O are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.
9. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

PARAMETER MEASUREMENT INFORMATION†



A. The particular input voltages for each module are shown in the Supplementary Parameter Measurement Information Section.
B. V_I is applied to each input separately except where Note 13 applies.
C. Each output is tested separately.

FIGURE 2–V_{OH} and V_{OL}



Each input is tested separately.

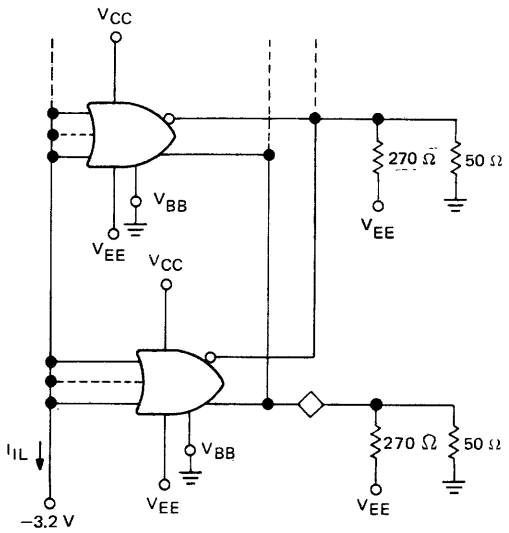
FIGURE 3–I_{IH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

◇ – Collector Dot

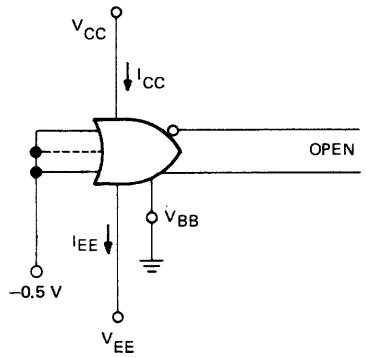
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION†



All inputs of all gates are connected in parallel.

FIGURE 4–I_{IL}



A. All gates are tested simultaneously.
B. I_{CC} is the total current into all V_{CC} terminals.

FIGURE 5–I_{CC} or I_{EE}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

◇ — Collector Dot

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2506	**V_{BB} (pin 15) = GND, V_{CC} (pin 3) = 1.32 V, V_{EE} (pin 10) = −3.2 V**										
$V_{OH(Z)}$	1, 2, 4 6, 7, 8 9, 11, 12 13, 14, 16	5	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	1, 2, 4 6, 7, 8 9, 11, 12 13, 14, 16	5	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	1, 2, 4 6, 7, 8 9, 11, 12 13, 14, 16	5	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	 −315	mV
$V_{OH(Z)}$	1, 2, 4 6, 7, 8 9, 11, 12 13, 14, 16	5	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			615 685	mV
$V_{OH(Z)}$	4	5	2	−0.15 V	−0.5 V	See Note 12	0°C 25°C 75°C	290 325			mV
$V_{OL(Z)}$	4	5	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C			−290 −260	mV
I_{IH}	1, 2, 4 6, 7, 8 9, 11, 12 13, 14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
I_{IL}	1, 2, 4, 6, 7, 8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.6 −0.8 −1.2	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
12. At least one input of each other gate must be at 0.5 V. Other inputs are biased to −0.5 V.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2507	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Z)}$	1, 2 7, 8 9, 11 12, 13 14, 16	5	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	1, 2 7, 8 9, 11 12, 13 14, 16	5	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	1, 2 7, 8 9, 11 12, 13 14, 16	5	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	 −315	mV
$V_{OH(Z)}$	1, 2 7, 8 9, 11 12, 13 14, 16	5	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			625 695	mV
$V_{OH(Z)}$	2	5	2	−0.15 V	−0.5 V	See Note 12	0°C 25°C 75°C	290 325			mV
$V_{OL(Z)}$	2	5	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C			−290 −260	mV
I_{IH}	1, 2 7, 8 9, 11 12, 13 14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
I_{IL}	1, 2, 7, 8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.7 −1.0	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
12. At least one input of each other gate must be at 0.5 V. Other inputs are biased to −0.5 V.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2508	V_{BB} (pin 15) = GND, V_{CC} (pin 3) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Z)}$	1, 16 2, 4 6, 7 8, 9 11, 12 13, 14	5	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	1, 16 2, 4 6, 7 8, 9 11, 12 13, 14	5	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	1, 16 2, 4 6, 7 8, 9 11, 12 13, 14	5	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	 −315	mV
$V_{OH(Z)}$	1, 16 2, 4 6, 7 8, 9 11, 12 13, 14	5	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			630 700	mV
$V_{OH(Z)}$	11	5	2	−0.15 V	−0.5 V	See Note 12	0°C 25°C 75°C	290 325			mV
$V_{OL(Z)}$	11	5	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C			−290 −260	mV
I_{IH}	1, 16 2, 4 6, 7 8, 9 11, 12 13, 14		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
I_{IL}	1, 2, 4, 6, 7, 8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.6 −0.8 −1.2	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
12. At least one input of each other gate must be at 0.5 V. Other inputs are biased to −0.5 V.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2509	V_{BB} (pin 15) = GND, V_{CC} (pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	1, 16 8, 9 11, 12 13, 14	7	2	0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Y)}$	1, 16 8, 9 11, 12 13, 14	7	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	−505 −490	−450 −410 −290	−350 −230	mV
$V_{OH(Z)}$	1, 16 8, 9 11, 12 13, 14	5	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	1, 16 8, 9 11, 12 13, 14	5	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	1, 16 8, 9 11, 12 13, 14	5	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	−315	mV
$V_{OH(Z)}$	1, 16 8, 9 11, 12 13, 14	5	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			615 685	mV
$V_{OH(Y)}$	8	7	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C	290 325			mV
$V_{OL(Y)}$	8	7	2	−0.15 V	−0.5 V	See Note 12	0°C 25°C 75°C			−335 −215	mV
I_{IH}	1, 16 8, 9 11, 12 13, 14		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
I_{IL}	1, 8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.6 −0.8	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
12. At least one input of each other gate must be at 0.5 V. Other inputs are biased to −0.5 V.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

4

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2510	**V_{BB} (pin 15) = GND, V_{CC} (pin 3) = 1.32 V, V_{EE} (pin 10) = −3.2 V**										
$V_{OH(Y)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	4	2	0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	315 350	390 425 495	 500 580	mV
$V_{OL(Y)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	4	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	−505 −490	−450 −410 −290	 −350 −230	mV
$V_{OH(Z)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	5	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	315 350	390 425 495	 500 580	mV
$V_{OL(Z)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	5	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	 −310 −280	mV
$V_{OL(Z)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	5	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	 −315	mV
$V_{OH(Z)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	5	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			 615 685	mV
$V_{OH(Y)}$	2	4	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C	290 325			mV
$V_{OL(Y)}$	2	4	2	−0.15 V	−0.5 V	See Note 12	0°C 25°C 75°C			 −335 −215	mV
I_{IH}	1, 2 6, 7, 8 9, 11, 12 13, 14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
I_{IL}	1, 2, 6, 7, 8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.6 −0.8 −1.1	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
12. At least one input of each other gate must be at 0.5 V. Other inputs are biased to −0.5 V.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	REMAINING INPUTS OF OTHER GATE(S)					
ECL2512	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Z)}$	1, 7 11, 16 13, 14	4	2	−0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
	7, 8 9, 11 12, 13	5									
$V_{OL(Z)}$	1, 7 11, 16 13, 14	4	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
	7, 8 9, 11 12, 13	5									
$V_{OL(Z)}$	1, 7 11, 16 13, 14	4	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	−315	mV
	7, 8 9, 11 12, 13	5									
$V_{OH(Z)}$	1, 7 11, 16 13, 14	4	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			600 670	mV
	7, 8 9, 11 12, 13	5									
$V_{OH(Z)}$	8	5	2	−0.15 V	−0.5 V	0.5 V	0°C 25°C 75°C	290 325			mV
$V_{OL(Z)}$	8	5	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C			−290 −260	mV
I_{IH}	1 16 14 8 9 12		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
	7, 11, 13		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			510 470 400	μA
I_{IL}	1, 7, 8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.6 −0.8 −1.2	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	REMAINING INPUTS OF OTHER GATE(S)					
ECL2513	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	14, 16 12, 13	4	2	0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
	8, 9 11, 12	5									
$V_{OL(Y)}$	14, 16 12, 13	4	2	−0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	−505 −490	−450 −410 −290	−350 −230	mV
	8, 9 11, 12	5									
$V_{OH(Z)}$	14, 16 12, 13	2	2	−0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
	8, 9 11, 12	7									
$V_{OL(Z)}$	14, 16 12, 13	2	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
	8, 9 11, 12	7									
$V_{OL(Z)}$	14, 16 12, 13	2	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	−315	mV
	8, 9 11, 12	7									
$V_{OH(Z)}$	14, 16 12, 13	2	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			580 650	mV
	8, 9 11, 12	7									
$V_{OH(Y)}$	13	4	2	0.15 V	−0.5 V	0.5 V	0°C 25°C 75°C	290 325			mV
$V_{OL(Y)}$	13	4	2	−0.15 V	−0.5 V	0.5 V	0°C 25°C 75°C			−335 −215	mV
I_{IH}	14, 16 13 8, 9 11		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
	12		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			510 470 400	μA
I_{IL}	8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.6 −0.8	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

operating characteristics at specified free-air temperature (see figure 1)

TERMINALS TO BE TESTED (SEE NOTES 16, 17, 18, AND 19)								C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns									t_{THL} and/or t_{TLH} TRANSITION TIMES—ns								
									T_A = 0°C			T_A = 25°C			T_A = 75°C			T_A = 0°C			T_A = 25°C			T_A = 75°C		
INPUT	OUTPUT	INPUT	OUTPUT	INPUT	OUTPUT	INPUT	OUTPUT	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2506																										
1		6		9		13		4		2.6			1.7	2.6	3.5		2.6		4.0			2.8	4.0	5.6		4.1
2	5	7	5	11	5	14	5																			
4		8		12		16		50		3.6			2.4	3.6	4.5		3.6		4.5			2.8	4.5	6.5		4.4
ECL2507																										
1	5	7	5	9	5	12	5	4		2.6			1.7	2.6	3.5		2.6		4.0			2.8	4.0	5.6		4.1
2		8		11		13		50		3.6			2.4	3.6	4.5		3.6		4.5			2.8	4.5	6.5		4.4
14	5							4		2.6			1.7	2.6	3.5		2.6		4.0			2.8	4.0	5.6		4.1
16								50		3.6			2.4	3.6	4.5		3.6		4.5			2.8	4.5	6.5		4.4
ECL2508																										
1	5	2	5	6	5	8	5	4		2.6			1.7	2.6	3.5		2.6		4.0			2.8	4.0	5.6		4.1
16		4		7		9		50		3.6			2.4	3.6	4.5		3.6		4.5			2.8	4.5	6.5		4.4
11	5	13	5					4		2.6			1.7	2.6	3.5		2.6		4.0			2.8	4.0	5.6		4.1
12		14						50		3.6			2.4	3.6	4.5		3.6		4.5			2.8	4.5	6.5		4.4
ECL2509																										
1	7	8	7	11	7	13	7	4		2.6			1.6	2.6	4.1		2.6		3.4			2.0	3.4	6.3		3.5
16	5	9	5	12	5	14	5	50		3.5			2.5	3.5	4.6		3.6		4.4			2.5	4.3	6.5		4.1
ECL2510																										
1	4	6	4	9	4	13	4	4		2.6			1.6	2.6	4.1		2.6		3.4			2.0	3.4	6.3		3.5
		7		11		14																				
2	5	8	5	12	5	16	5	50		3.5			2.5	3.5	4.6		3.6		4.4			2.5	4.3	6.5		4.1
ECL2512																										
1	4	11	4	13	4	7	5	4		2.6			1.7	2.6	3.5		2.6		4.0			2.8	4.0	5.6		4.1
7		16		14		8		50		3.6			2.4	3.6	4.5		3.6		4.5			2.8	4.5	6.5		4.4
9	5	12	5					4		2.6			1.7	2.6	3.5		2.6		4.0			2.8	4.0	5.6		4.1
11		13						50		3.6			2.4	3.6	4.5		3.6		4.5			2.8	4.5	6.5		4.4
ECL2513																										
14	4	12	4	8	5	11	5	4		2.6			1.6	2.6	4.1		2.6		3.4			2.0	3.4	6.3		3.5
16	2	13	2	9	7	12	7	50		3.5			2.5	3.5	4.6		3.6		4.4			2.5	4.3	6.5		4.1

NOTES: 16. Each gate is tested separately. At least one input of each of the other gates (excluding the inactive half of the ECL2512 or ECL2513) must be at 0.5 V with the other inputs at −0.5 V.

17. The input pulse is measured as it is applied sequentially to each input of the gate under test, and a waveform measurement is made at each of the outputs of that gate. Times are as defined in Figure 1.

18. Other inputs of the same gate as input under test are at −0.5 V.

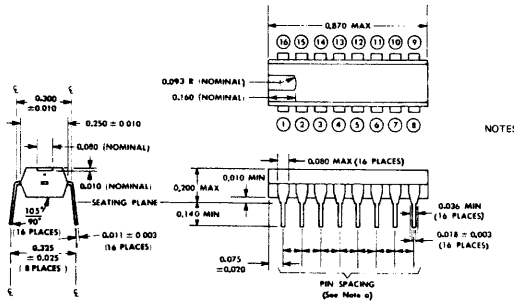
19. Bias voltages and loads for the half of the ECL2512 and ECL2513 under test are shown in Figure 1. The inactive half has remaining inputs biased to −0.5 V, outputs under load, and power applied.

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

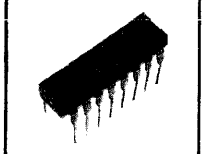
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams on pages 4 and 5.

Outputs are denoted by Y or Z. Inputs are denoted by A, B, C, etc.

Respective inputs and outputs are identified by a gate number preceding the pin symbol.

Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.

V_{BB} is a reference voltage.

NC indicates no internal connection.

PIN ASSIGNMENTS

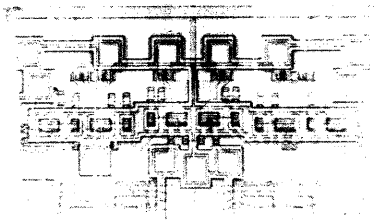
PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2506	A	B	V_{CC}	C	Z	D	E	F	G	V_{EE}	H	I	J	K	V_{BB}	L
ECL2507	A	B	V_{CC}	NC	Z	V_{CC}	C	D	E	V_{EE}	F	G	H	I	V_{BB}	J
ECL2508	A	C	V_{CC}	D	Z	E	F	G	H	V_{EE}	I	J	K	L	V_{BB}	B
ECL2509	A	NC	NC	NC	Z	V_{CC}	Y	C	D	V_{EE}	E	F	G	H	V_{BB}	B
ECL2510	A	B	V_{CC}	Y	Z	C	D	E	F	V_{EE}	G	H	I	J	V_{BB}	K
ECL2512	1A	NC	V_{CC}	1Z	2Z	V_{CC}	D	2A	2B	V_{EE}	E	2C	F	1C	V_{BB}	1B
ECL2513	NC	1Z	V_{CC}	1Y	2Y	V_{CC}	2Z	2A	2B	V_{EE}	2C	D	1C	1A	V_{BB}	1B

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES ECL2515, ECL2516 EMITTER-COUPLED-LOGIC ARITHMETIC MODULES

TYPES ECL2515, ECL2516
BULLETIN NO. DL-S 7011295, JANUARY 1970

ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) ARITHMETIC MODULES FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS



description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.

The ECL2500 family includes:

- Basic Gate Modules
- Multifunction Gate Modules
- Bistable Modules
- **Arithmetic Modules**
- Interface Modules
- Memory Module

family features

- High speed. . .typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ±225 mV typical at 25°C

This data sheet covers the arithmetic modules.
Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series arithmetic modules

The ECL2500 series arithmetic modules are summarized in the table below. These modules contain the multifunction ECL circuits shown in the schematics of Figures A and B. The basic principle of collector dotting and emitter dotting, used in both modules, is the shown in Figure C. Logic diagrams of ECL2515 and ECL2516 are shown on page 4.

SUMMARY OF ARITHMETIC MODULES

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS OF MODULE
ECL2515 GROUP CARRY	5	1, 2, 3, 4, 5	OR-AND/NOR-OR	Y and Z
ECL2516 FULL SUM-CARRY ADDER	7	2, 2, 2, 3, 3, 3, 3	OR-AND/NOR-OR	Σ, $\overline{\Sigma}$, C_O, and $\overline{C}_O$

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

schematic

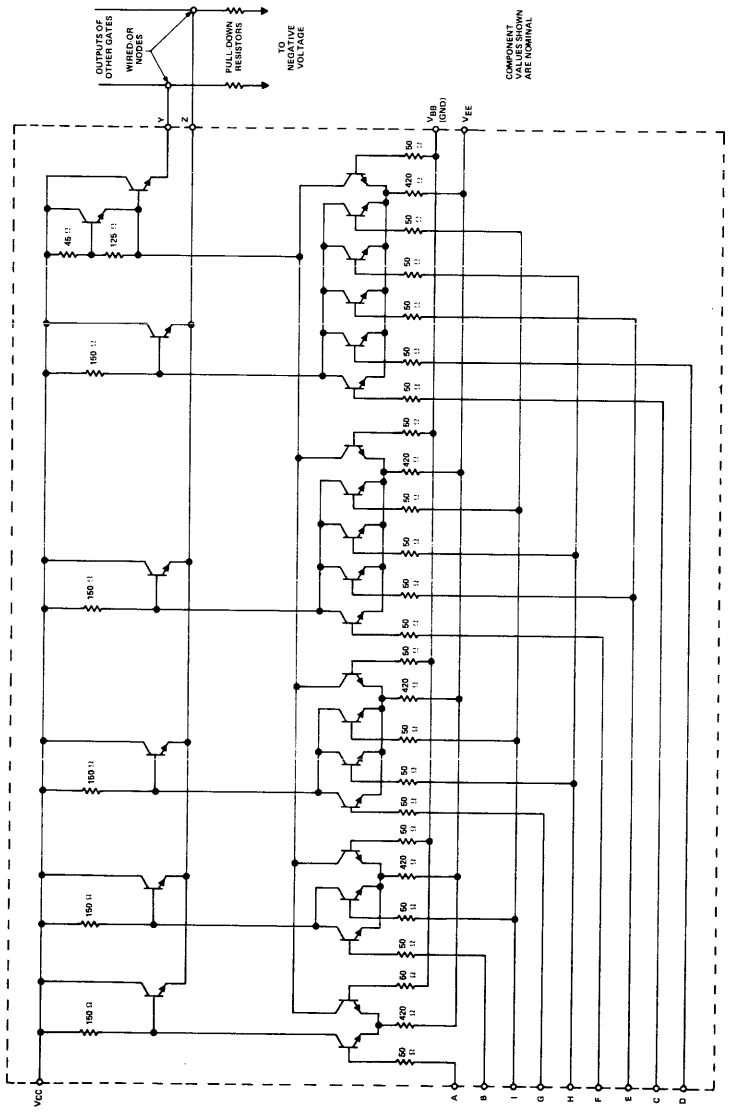
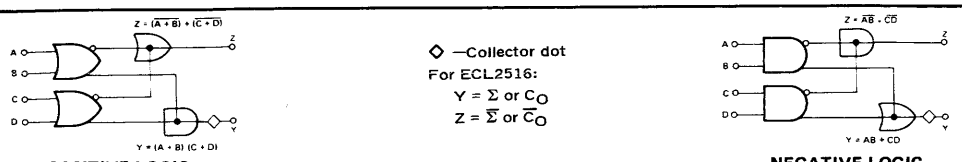


FIGURE A–SCHEMATIC OF ECL2515

4

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

logic



POSITIVE LOGIC

FIGURE C—WIRED-OR/AND LOGIC DIAGRAM

NEGATIVE LOGIC

schematic

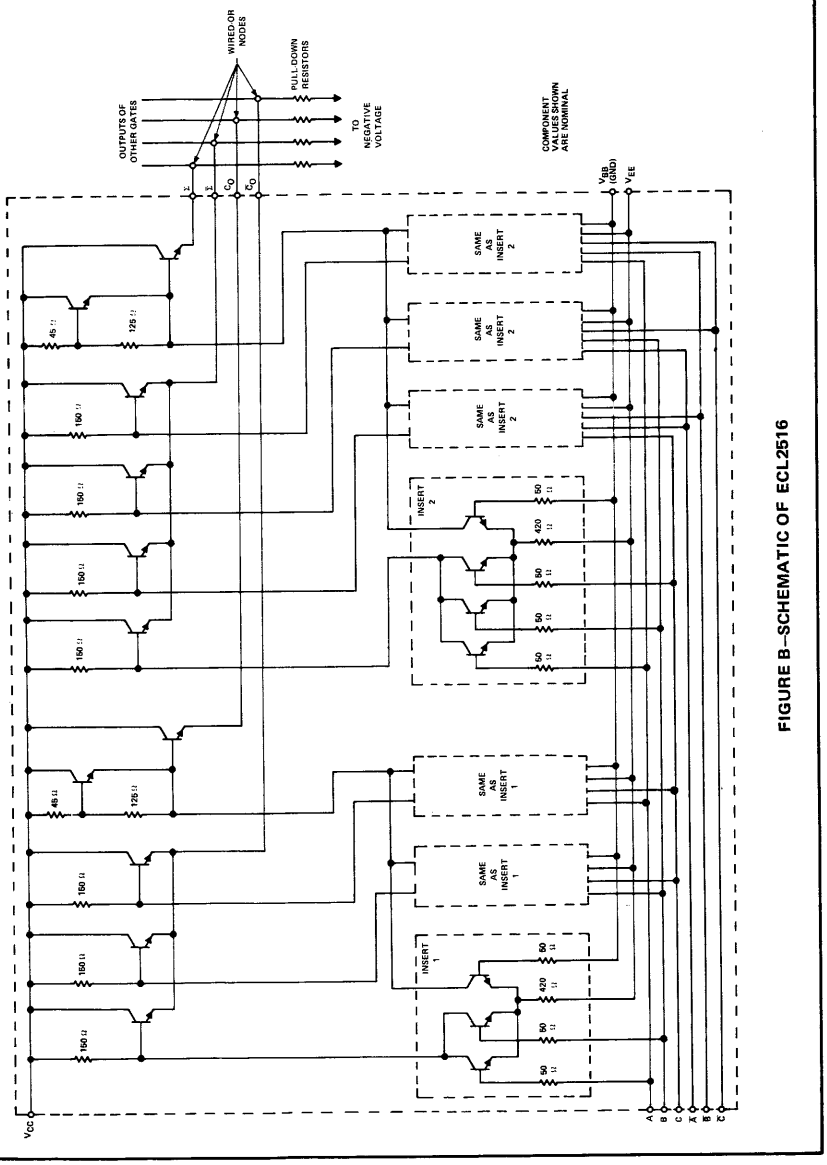


FIGURE B—SCHEMATIC OF ECL2516

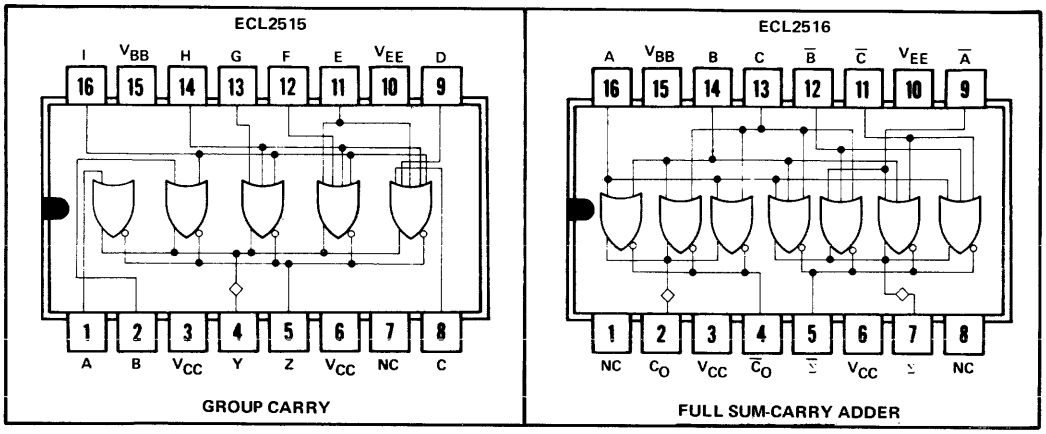
Positive logic OR-AND/NOR-OR functions or negative logic AND-OR/NAND-AND functions are provided at the various outputs of ECL2515 and ECL2516 as shown in the logic table.
Emitter-follower outputs require an external pull-down resistor. The wired-OR function can be obtained by connecting emitter-follower outputs of other modules together. Only one pull-down resistor is required for each wired-OR node. Each output of a module can be wired-OR connected independently of the other outputs of the module.

4

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES ECL2515, ECL2516
EMITTER-COUPLED-LOGIC ARITHMETIC MODULES

logic



4

◇—Collector dot
NC—No internal connection

MODULE	POSITIVE LOGIC		NEGATIVE LOGIC	
	IN-PHASE OUTPUT	OUT-OF-PHASE OUTPUT	IN-PHASE OUTPUT	OUT-OF-PHASE OUTPUT
ECL2515	$Y = A(B+I)(G+H+I) \cdot (E+F+H+I)(C+D+E+H+I)$	$Z = \overline{A+BI}+\overline{G+HI}+\overline{E+F+HI}+\overline{C+D+E+HI}$	$Y = A+BI+GHI+EFHI+CDEHI$	$Z = \overline{A} \cdot \overline{BI} \cdot \overline{GHI} \cdot \overline{EFHI} \cdot \overline{CDEHI}$
ECL2516	$\Sigma = (A+B+C)(\overline{A}+B+C) \cdot (A+\overline{B}+\overline{C})(A+B+\overline{C})$	$\overline{\Sigma} = \overline{A+B+C}+\overline{\overline{A}+B+C}+\overline{A+\overline{B}+\overline{C}}+\overline{A+B+\overline{C}}$	$\Sigma = ABC+\overline{A}BC+A\overline{B}\overline{C}+AB\overline{C}$	$\overline{\Sigma} = \overline{ABC} \cdot \overline{\overline{A}BC} \cdot \overline{A\overline{B}\overline{C}} \cdot \overline{AB\overline{C}}$
	$C_O = (A+B)(B+C)(A+C)$	$\overline{C}_O = \overline{A+B}+\overline{B+C}+\overline{A+C}$	$C_O = AB+BC+AC$	$\overline{C}_O = \overline{AB} \cdot \overline{BC} \cdot \overline{AC}$

truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2515

INPUTS									OUTPUTS	
A	B	C	D	E	F	G	H	I	Y	Z
L	X	X	X	X	X	X	X	X	L	H
X	L	X	X	X	X	X	X	L	L	H
X	X	X	X	X	X	L	L	L	L	H
X	X	X	X	L	L	X	L	L	L	H
X	X	L	L	L	X	X	L	L	L	H
For a LOW Y and HIGH Z, all inputs to at least one gate must be LOW. For a HIGH Y and LOW Z, at least one input of each gate must be HIGH.										
H	X	X	X	X	X	X	X	H	H	L
H	H	X	X	X	X	X	H	X	H	L
H	H	X	X	H	X	H	X	X	H	L
H	H	X	H	X	H	H	X	X	H	L
H	H	H	X	X	H	H	X	X	H	L

ECL2516

INPUTS						OUTPUTS			
A	B	C	Ā	B̄	C̄	Σ	Σ̄	C_O	$\overline{C}_O$
L	L	L	H	H	H	L	H	L	H
L	L	H	H	H	L	H	L	L	H
L	H	L	H	L	H	H	L	L	H
L	H	H	H	L	L	L	H	H	L
H	L	L	L	H	H	H	L	L	H
H	L	H	L	H	L	L	H	H	L
H	H	L	L	L	H	L	H	H	L
H	H	H	L	L	L	H	L	H	L

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings (see note 1)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Temperature range with supply and bias voltages applied . . . . . −40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Output Y†	All inputs high			−40 mA
Output Z†	All inputs low			−40 mA

†For ECL2516: Y = Σ or C_o, Z = $\overline{\Sigma}$ or $\overline{C}_o$

4

recommended operating conditions

Supply voltage V_{CC} . . . . . 1.32 V ± 2%
Supply voltage V_{EE} . . . . . −3.2 V ± 2%
Reference voltage V_{BB} . . . . . 0 V (GND)
Reverse bias on unused inputs . . . . . −1 V ± 0.5 V
Normalized d-c fan-out . . . . . 0 to 35
Load on each output . . . . . characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range . . . . . 0°C to 75°C

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

ECL2515 electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS*						T_A	MIN	TYP	MAX	UNIT
		TEST FIGURE	TERMINALS (SEE NOTE 4)		INPUT CONDITIONS					(SEE NOTE 5)		
			INPUTS	OUTPUTS Y Z	INPUT UNDER TEST, V_I	OTHER INPUT(S) OF SAME GATE	REMAINING INPUTS OF OTHER GATES					
V_{IH}	High-level input voltage							0°C	150		720	mV
								25°C	150		720	
								75°C	150		720	
V_{IL}	Low-level input voltage							0°C	−1500		−150	mV
								25°C	−1500		−150	
								75°C	−1500		−150	
$V_{OH(Y)}$	High-level output voltage at Y output	2	1	4	0.2 V	−0.5 V	0.5 V	0°C	315	390		mV
			2, 16					25°C	350	425	500	
			13, 14, 16					75°C		495	580	
			11, 12, 14, 16									
			8, 9, 11, 14, 16									
$V_{OL(Y)}$	Low-level output voltage at Y output	2	Same as for $V_{OH(Y)}$ above		−0.2 V	−0.5 V	0.5 V	0°C	−505	−450		mV
								25°C	−490	−410	−350	
								75°C		−290	−230	
$V_{OH(Z)}$	High-level output voltage at Z output	2	1	5	−0.2 V	−0.5 V	0.5 V	0°C	315	390		mV
			2, 16					25°C	350	425	500	
			13, 14, 16					75°C		495	580	
			11, 12, 14, 16									
			8, 9, 11, 14, 16									
$V_{OL(Z)}$	Low-level output voltage at Z output	2	Same as for $V_{OH(Z)}$ above		0.2 V	−0.5 V	See Note 6	0°C		−385		mV
								25°C	−440	−365	−310	
								75°C		−325	−280	
$V_{OL(Z)}$	Low-level output voltage at Z output	2	Same as for $V_{OH(Z)}$ above		0.4 V	−0.5 V	See Note 6	0°C	−505	−455		mV
								25°C	−490	−425		
								75°C		−380	−315	
$V_{OH(Z)}$	High-level output voltage at Z output	2	Same as for $V_{OH(Z)}$ above		All inputs of all gates in parallel at −0.5 V			0°C				mV
								25°C			625	
								75°C			695	
$V_{OH(Y)}$	High-level output voltage at Y output	2	1	4	0.15 V	−0.5 V	0.5 V	0°C	290			mV
								25°C	325			
								75°C				
$V_{OL(Y)}$	Low-level output voltage at Y output	2	1	4	−0.15 V	−0.5 V	0.5 V	0°C				mV
								25°C			−335	
								75°C			−215	
I_{IH}	High-level input current (each input)	3	1, 2, 8, 9, 12, 13		0.5 V	0.5 V	−0.5 V	0°C			255	μA
			11, 14, 16 See Note 7					25°C			235	
								75°C			200	
I_{IL}	Low-level input current (all inputs)	4	1, 2, 8, 9, 11, 12, 13, 14, 16		All inputs of all gates in parallel at −3.2 V			0°C			−0.8	μA
								25°C			−1	
								75°C			−1.5	
I_{CC} or I_{EE}	Supply current	5			All inputs of all gates in parallel at −0.5 V			25°C	20		36	mA
C_{in}	Input capacitance (see Note 8)							25°C		5		pF
z_{out}	Output impedance (see Note 9)			4 5				25°C		5		Ω

*V_{BB} (pin 15) = GND, V_{CC} (pins 3 and 6) = 1.32 V ±1%, V_{EE} (pin 10) = −3.20 V ±1%.

NOTES:
4. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.
6. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.
7. Terminals 11, 14, and 16 are internally connected to 2, 3, and 4 gates respectively, and maximum I_{IH} for these terminals at each temperature can be determined by multiplying the value given for I_{IH} by 2, 3, or 4 respectively.
8. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.
9. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

ECL2516 electrical characteristics at specified free-air temperature†

PARAMETER		TEST FIGURE	TERMINALS (SEE NOTE 4) INPUTS	TERMINALS (SEE NOTE 4) OUTPUTS Y	Z	INPUT CONDITIONS: INPUT UNDER TEST, V_I	OTHER INPUT(S) OF SAME GATE	REMAINING INPUTS OF OTHER GATES	T_A	MIN (SEE NOTE 5)	TYP (SEE NOTE 5)	MAX (SEE NOTE 5)	UNIT
V_{IH}	High-level input voltage								0°C 25°C 75°C	150 150 150		720 720 720	mV
V_{IL}	Low-level input voltage								0°C 25°C 75°C	−1500 −1500 −1500		−150 −150 −150	mV
$V_{OH(Y)}$	High-level output voltage at Y output	2	16, 14 14, 13 16, 13	2		0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
			16, 14, 13 9, 12, 13 9, 14, 11 16, 12, 11	7									
$V_{OL(Y)}$	Low-level output voltage at Y output	2	Same as for $V_{OH(Y)}$ above			−0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	−505 −490	−450 −410 −290	−350 −230	mV
$V_{OH(Z)}$	High-level output voltage at Z output	2	16, 14 14, 13 16, 13	4		−0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
			16, 14, 13 9, 12, 13 9, 14, 11 16, 12, 11	5									
$V_{OL(Z)}$	Low-level output voltage at Z output	2	Same as for $V_{OH(Z)}$ above			0.2 V	−0.5 V	See Note 6	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	Low-level output voltage at Z output	2	Same as for $V_{OH(Z)}$ above			0.4 V	−0.5 V	See Note 6	0°C 25°C 75°C	−505 −490	−455 −425 −380	−315	mV
$V_{OH(Z)}$	High-level output voltage at Z output	2	16, 14 14, 13 16, 13	4		All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			600 670	mV
			16, 14, 13 9, 12, 13 9, 14, 11 16, 12, 11	5					0°C 25°C 75°C			615 685	
$V_{OH(Y)}$	High-level output voltage at Y output	2	13	7		0.15 V	−0.5 V	0.5 V	0°C 25°C 75°C	290 325			mV
$V_{OL(Y)}$	Low-level output voltage at Y output	2	13	7		−0.15 V	−0.5 V	0.5 V	0°C 25°C 75°C			−335 −215	mV
I_{IH}	High-level input current (each input)	3	9 11 12			0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			510 470 400	μA
			13 14 16						0°C 25°C 75°C			1020 940 800	μA
I_{IL}	Low-level input current (all inputs)	4	9, 11, 12, 13, 14, 16			All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.9 −1.2 −1.8	μA
I_{CC} or $-I_{EE}$	Supply current	5				All inputs of all gates in parallel at −0.5 V			25°C	30		45	mA
C_{in}	Input capacitance (see Note 8)								25°C		5		pF
z_{out}	Output impedance (see Note 9)								25°C		5		Ω

*V_{BB} (pin 15) = GND, V_{CC} (pins 3 and 6) = 1.32 V ± 1%, V_{EE} (pin 10) = −3.20 V ± 1%.
†$Y = \Sigma$ or C_O; $Z = \overline{\Sigma}$ or $\overline{C}_O$.

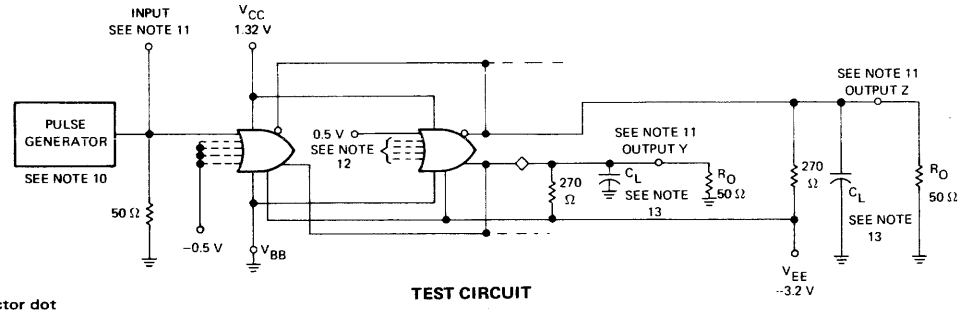
NOTES: 4. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.
6. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.
8. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.
9. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

operating characteristics at specified free-air temperature (see figure 1)

PARAMETER		C_L	T_A	ECL2515 EITHER OUTPUT			ECL2516 ANY OUTPUT			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation delay time, high-to-low level output and/or	4 pF	0°C		2.6			2.6		ns
			25°C	1.5	2.6	4.1	1.5	2.6	4.1	
			75°C		2.6			2.6		
t_{PLH}	Propagation delay time low-to-high-level output	50 pF	0°C		3.5			3.5		ns
			25°C	2.4	3.5	4.8	2.4	3.5	4.8	
			75°C		3.5			3.5		
t_{THL}	Transition time, high-to-low-level output and/or	4 pF	0°C		4.0			4.0		ns
			25°C	1.6	4.0	6.6	1.6	4.0	6.6	
			75°C		4.1			4.1		
t_{TLH}	Transition time, low-to-high-level output	50 pF	0°C		4.7			4.7		ns
			25°C	1.9	4.6	6.9	1.9	4.6	6.9	
			75°C		4.4			4.4		

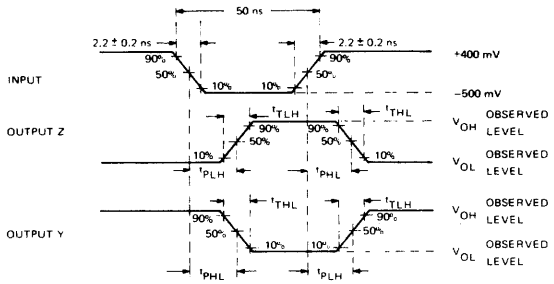
4

PARAMETER MEASUREMENT INFORMATION†



TEST CIRCUIT

◇—Collector dot



VOLTAGE WAVEFORMS

FIGURE 1–PROPAGATION DELAY AND TRANSITION TIMES

†For ECL2516: Y = Σ or C_O; Z = $\overline{\Sigma}$ or $\overline{C}_O$.

NOTES: 10. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.

11. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistors designated R_O are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.

12. This test circuit shows only the principle of measuring propagation delay times and transition times; i.e., no internal connection of the input terminals is shown. See Table I for ECL2515 or Table II for ECL2516 for voltages to be applied to input terminals for each test.

13. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

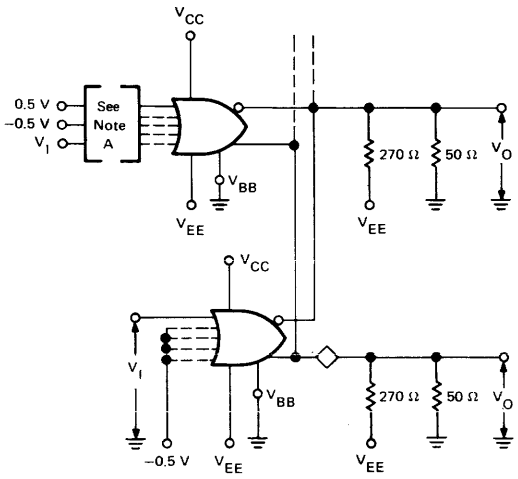
TEST TABLE I—ECL2515

INPUT TERMINAL CONDITIONS			OUTPUT UNDER TEST
PULSE GENERATOR	0.5 V	−0.5 V	
1	16	2, 8, 9, 11, 12, 13, 14	4, 5
2	1, 14	8, 9, 11, 12, 13, 16	4, 5
16		2, 8, 9, 11, 12, 13	
13	1, 2, 11	8, 9, 12, 14, 16	4, 5
14		8, 9, 12, 13, 16	
16		8, 9, 12, 13, 14	
11	1, 2, 9, 13	8, 12, 14, 16	4, 5
12		8, 11, 14, 16	
14		8, 11, 12, 16	
16		8, 11, 12, 14	
8	1, 2, 12, 13	9, 11, 14, 16	4, 5
9		8, 11, 14, 16	
11		8, 9, 14, 16	
14		8, 9, 11, 16	
16		8, 9, 11, 14	

TEST TABLE II—ECL2516

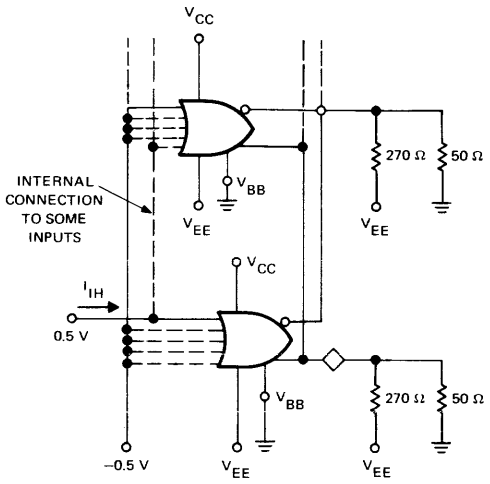
INPUT TERMINAL CONDITIONS			OUTPUT UNDER TEST
PULSE GENERATOR	0.5 V	−0.5 V	
16	11, 13	9, 12, 14	2, 4
14		9, 12, 16	
14	9, 16	11, 12, 13	2, 4
13		11, 12, 14	
16	12, 14	9, 11, 13	2, 4
13		9, 11, 16	
16	9, 11	12, 13, 14	7, 5
14		12, 13, 16	
13		12, 14, 16	
9	14, 16	11, 12, 13	7, 5
12		9, 11, 13	
13		9, 11, 12	
9	12, 13	11, 14, 16	7, 5
14		9, 11, 16	
11		9, 14, 16	
16	9, 14	11, 12, 13	7, 5
12		11, 13, 16	
11		12, 13, 16	

PARAMETER MEASUREMENT INFORMATION†



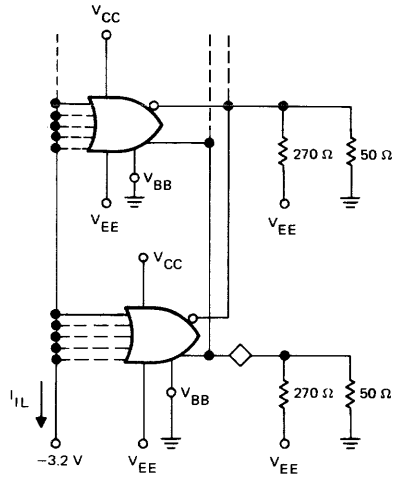
A. The particular input voltages for each module are shown in the electrical characteristics tables.
B. V_I is applied to each input separately except where Note 6 applies.
C. Each output is tested separately.

FIGURE 2–V_{OH} and V_{OL}



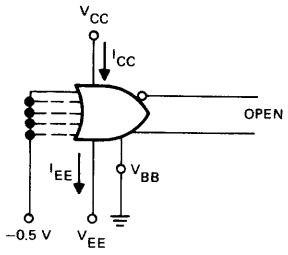
Each input is tested separately.

FIGURE 3–I_{IH}



All inputs of all gates are connected in parallel.

FIGURE 4–I_{IL}



A. All gates are tested simultaneously.
B. I_{CC} is the total current into all V_{CC} terminals.

FIGURE 5–I_{CC} or I_{EE}

◇—Collector dot

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

APPLICATION INFORMATION

ECL2515

The ECL2515 module is designed to provide the logic function for carry look-ahead in high-speed binary adders. In carry look-ahead, bit positions for binary numbers added together produce "generate" terms and "propagate" terms for the carry and sum logic equations.

The ECL2515 produces a "generate" term for 5 bits in one level of logic with a typical propagation delay of 3.0 nanoseconds with a fan-out of 4.

ECL2516

The ECL2516 is a full adder for two binary bits and carry-in that produces a sum and carry-out. The binary bits and their complements, along with carry-in and its complement, are required as inputs.

The sum and its complement and the carry-out and its complement are both produced in one level of logic with a typical propagation delay of 3.0 nanoseconds with a fan-out of 4.

general

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

Applications of the arithmetic modules at other than data sheet conditions are covered in a separate ECL2500 series application document.

General loading for fan-out may be divided into two classes:

CLASS I **Short-Line or Cluster Loading.**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II **Long-Line or Distributive Loading.**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

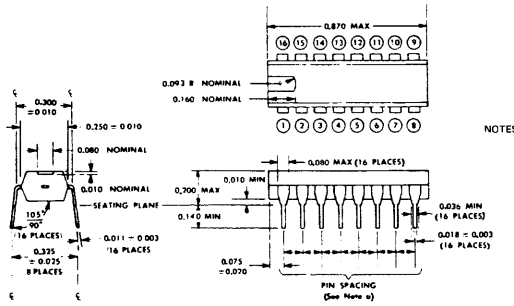
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

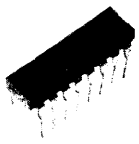
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



terminal designations

Pin assignments are shown in the table below and correspond to logic diagrams on page 4.
Outputs are denoted by Y and Z for ECL2515 and by Σ, $\overline{\Sigma}$, C_O, and $\overline{C}_O$ for ECL2516.
Inputs are denoted by A through I for ECL2515 and by A, B, C, $\overline{A}$, $\overline{B}$, and $\overline{C}$ for ECL2516.
Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.
NC indicates no internal connection.

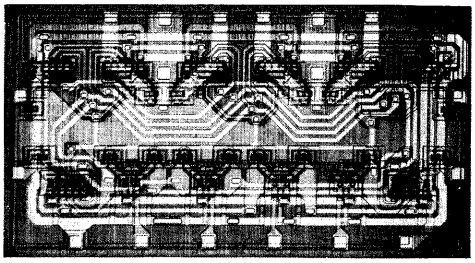
PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2515	A	B	V_{CC}	Y	Z	V_{CC}	NC	C	D	V_{EE}	E	F	G	H	V_{BB}	I
ECL2516	NC	C_O	V_{CC}	$\overline{C}_O$	$\overline{\Sigma}$	V_{CC}	Σ	NC	$\overline{A}$	V_{EE}	$\overline{C}$	$\overline{B}$	C	B	V_{BB}	A

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE ECL2517
EMITTER-COUPLED-LOGIC DECODER

ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) DECODER MODULE FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS



description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.

The ECL2500 family includes:

- Basic Gate Modules
- **Multifunction Gate Modules**
- Bistable Modules
- Arithmetic Modules
- Interface Modules
- Memory Module

family features

- High speed. . .typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ± 225 mV typical at 25°C

This data sheet covers the decoder module. Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series 3-bit-to-8-line decoder with enable

The ECL2500 series decoder module is summarized in the table below. The schematic diagram of this module is shown in Figure A.

SUMMARY OF DECODER MODULE

MODULE	GATES PER MODULE	INPUTS PER MODULE	OUTPUTS PER MODULE
ECL2517	12 (4 input, 8 output)	4 (3 bits plus enable)	8 (1 per output gate)

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE ECL2517
EMITTER-COUPLED-LOGIC DECODER

schematic

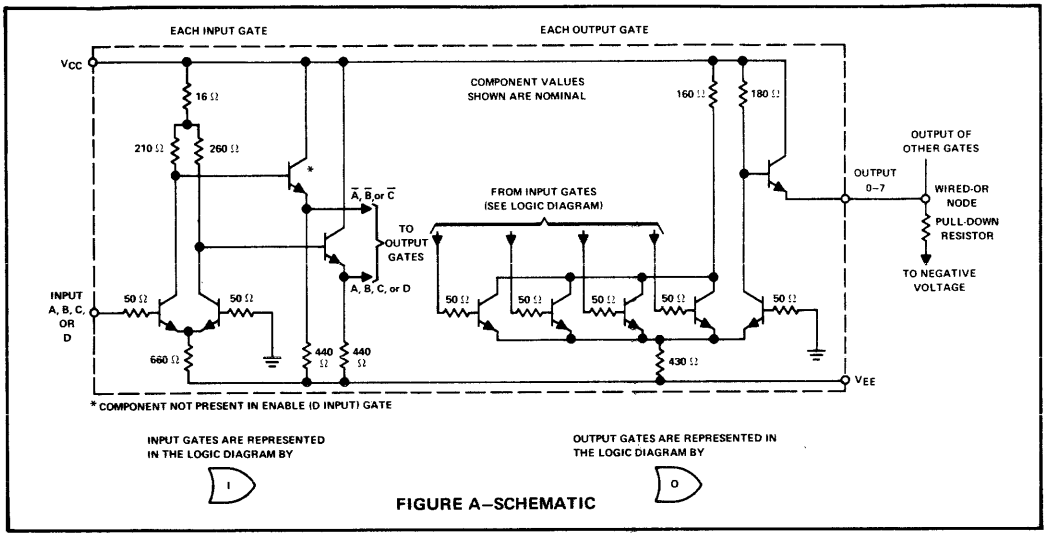


FIGURE A–SCHEMATIC

Emitter-follower outputs require external pull-down resistors. The wired-OR function can be obtained by connecting emitter-follower outputs of other gates to any of the outputs. Only one pull-down resistor is required for each wired-OR node.

absolute maximum ratings (see note 1)

Terminal voltages and currents	See table below
Storage temperature range	−40°C to 150°C
Temperature range with supply and bias voltage applied	−40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Any output	All inputs high			−40 mA

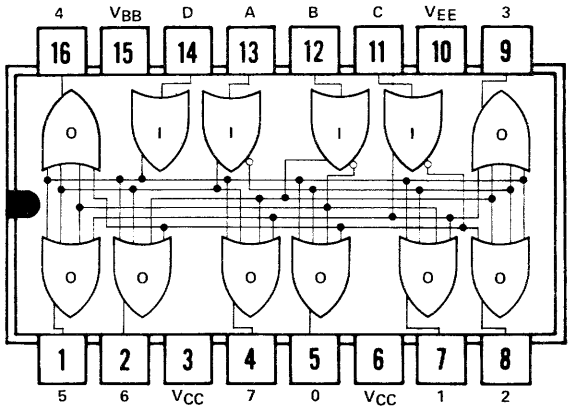
recommended operating conditions

Supply voltage V_{CC}	1.32 V ± 2%
Supply voltage V_{EE}	−3.2 V ± 2%
Reference voltage V_{BB}	0 V (GND)
Reverse bias on unused inputs	−1 V ± 0.5 V
Normalized d-c fan-out	0 to 35
Load on each output	characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range	0°C to 75°C

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

logic



OUTPUT LINE	POSITIVE LOGIC	NEGATIVE LOGIC
0	$\overline{A}+\overline{B}+\overline{C}+D$	$\overline{A}\overline{B}\overline{C}D$
1	$\overline{A}+\overline{B}+C+D$	$\overline{A}\overline{B}CD$
2	$\overline{A}+B+\overline{C}+D$	$\overline{A}B\overline{C}D$
3	$\overline{A}+B+C+D$	$\overline{A}BCD$
4	$A+\overline{B}+\overline{C}+D$	$A\overline{B}\overline{C}D$
5	$A+\overline{B}+C+D$	$A\overline{B}CD$
6	$A+B+\overline{C}+D$	$AB\overline{C}D$
7	$A+B+C+D$	$ABCD$

INPUT GATE

OUTPUT GATE

4

truth table (for this module, H = positive voltage, L = negative voltage, X = irrelevant)

INPUTS				OUTPUT LINES							
A	B	C	D	0	1	2	3	4	5	6	7
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	L
L	L	H	L	H	H	H	H	H	H	L	H
L	H	L	L	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	L	H	H	H
H	L	L	L	H	H	H	L	H	H	H	H
H	L	H	L	H	H	L	H	H	H	H	H
H	H	L	L	H	L	H	H	H	H	H	H
H	H	H	L	L	H	H	H	H	H	H	H

CIRCUIT TYPE ECL2517
EMITTER-COUPLED-LOGIC DECODER

electrical characteristics at specified free-air temperature*

PARAMETER		TEST FIGURE	INPUT CONDITIONS TERMINAL 13 $V_{I(A)}$	12 $V_{I(B)}$	11 $V_{I(C)}$	14 $V_{I(D)}$	OUTPUT TERMINAL	T_A	MIN (SEE NOTE 4)	TYP (SEE NOTE 4)	MAX (SEE NOTE 4)	UNIT
V_{IH}	High-level input voltage							0°C	150		720	mV
								25°C	150		720	
								75°C	150		720	
V_{IL}	Low-level input voltage							0°C	−1500		−150	mV
								25°C	−1500		−150	
								75°C	−1500		−150	
$V_{OH(0)}$	High-level output voltage at line 0	1	0.5 V	0.5 V	0.5 V	0.2 V	5	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(0)}$	Low-level output voltage at line 0	1	0.5 V	0.5 V	0.5 V	−0.2 V	5	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(1)}$	High-level output voltage at line 1	1	0.5 V	−0.2 V	−0.5 V	−0.5 V	7	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(1)}$	Low-level output voltage at line 1	1	0.5 V	0.2 V	−0.5 V	−0.5 V	7	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(2)}$	High-level output voltage at line 2	1	0.5 V	0.2 V	0.5 V	−0.5 V	8	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(2)}$	Low-level output voltage at line 2	1	0.5 V	−0.2 V	0.5 V	−0.5 V	8	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(3)}$	High-level output voltage at line 3	1	−0.2 V	−0.5 V	−0.5 V	−0.5 V	9	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(3)}$	Low-level output voltage at line 3	1	0.2 V	−0.5 V	−0.5 V	−0.5 V	9	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(4)}$	High-level output voltage at line 4	1	0.2 V	0.5 V	0.5 V	−0.5 V	16	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(4)}$	Low-level output voltage at line 4	1	−0.2 V	0.5 V	0.5 V	−0.5 V	16	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(5)}$	High-level output voltage at line 5	1	−0.5 V	0.5 V	0.2 V	−0.5 V	1	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(5)}$	Low-level output voltage at line 5	1	−0.5 V	0.5 V	−0.2 V	−0.5 V	1	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(6)}$	High-level output voltage at line 6	1	−0.5 V	−0.5 V	−0.2 V	−0.5 V	2	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(6)}$	Low-level output voltage at line 6	1	−0.5 V	−0.5 V	0.2 V	−0.5 V	2	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
V_{OH}	High-level output voltage at all lines	1	−0.5 V	−0.5 V	−0.5 V	0.15 V	1, 2, 4, 5, 7, 8, 9, 16	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(7)}$	Low-level output voltage at line 7	1	−0.5 V	−0.5 V	−0.5 V	−0.15 V	4	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
I_{IH}	High-level input current	2	Input under test at 0.5 V, other inputs at −0.5 V					0°C			165	μA
								25°C			150	
								75°C			125	
I_{IL}	Low-level input current (all inputs)	3	All inputs in parallel at −3.2 V					0°C			−0.5	μA
								25°C			−0.5	
								75°C			−0.5	
I_{CC} or $-I_{EE}$	Supply current	4	All inputs in parallel at −0.5 V					25°C	84		133	mA
C_{in}	Input capacitance (see Note 5)							25°C		5		pF
z_{out}	Output impedance (see Note 6)							25°C		5		Ω

*V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V ± 1%, V_{EE} (pin 10) = −3.20 V ± 1%.

NOTES: 4. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

5. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. $C_{in} = Q/V$.

6. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operating characteristics at specified free-air temperature (see figure 5)

TERMINALS TO BE TESTED (SEE NOTE 7)		C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES–ns									t_{THL} and/or t_{TLH} TRANSITION TIMES–ns								
			T_A = 0°C			T_A = 25°C			T_A = 75°C			T_A = 0°C			T_A = 25°C			T_A = 75°C		
INPUT	OUTPUT	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
14	5	4		4.8		3	4.8	6.6		5.0			3.6		2.3	3.7	5.5		3.6	
14	7																			
14	8																			
14	9																			
14	16																			
14	1																			
14	2																			
14	4																			
14	5	50		5.9		3.9	5.8	7.7		5.8			4.5		2.5	4.3	6.5		4.2	
14	7																			
14	8																			
14	9																			
14	16																			
14	1																			
14	2																			
14	4																			

NOTE: 7. The eight combinations of voltages at input terminals A, B, and C shown in the table of Figure 5, are applied sequentially. With each combination of input voltages, the enable input, D, is pulsed from the high level to the low level to give a low-level output at the particular output line shown in the table. The input pulse is measured as it is applied with each combination of input voltages and a waveform measurement is made at the corresponding output.

GENERAL APPLICATION INFORMATION

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected.

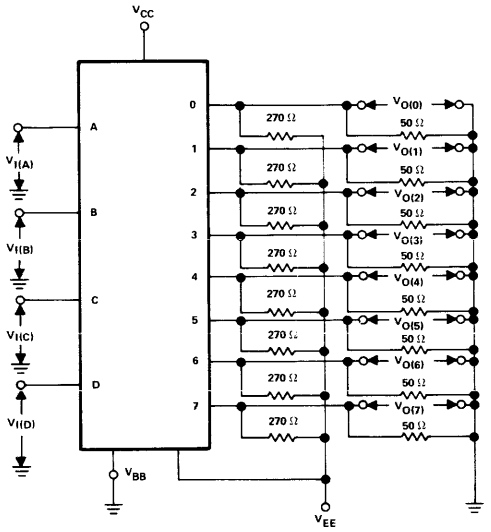
Applications of the ECL2517 decoder module at other than data sheet conditions are covered in a separate ECL2500 series application document.

General loading for fan-out may be divided into two classes:

CLASS I **Short-Line or Cluster Loading.**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

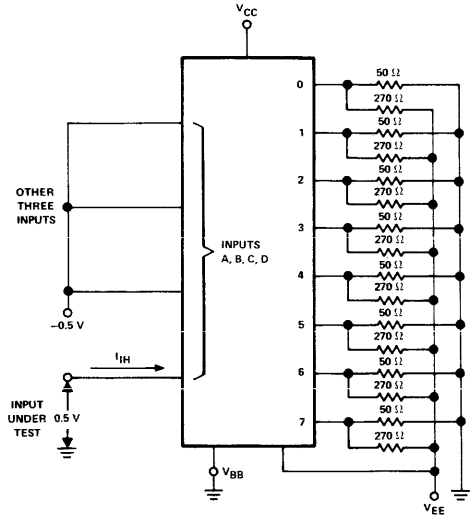
CLASS II **Long-Line or Distributive Loading.**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

PARAMETER MEASUREMENT INFORMATION†



V_I is applied to each input as specified in the electrical characteristics table.

FIGURE 1–V_{OH} AND V_{OL}



Each input is tested separately.

FIGURE 2–I_{IH}

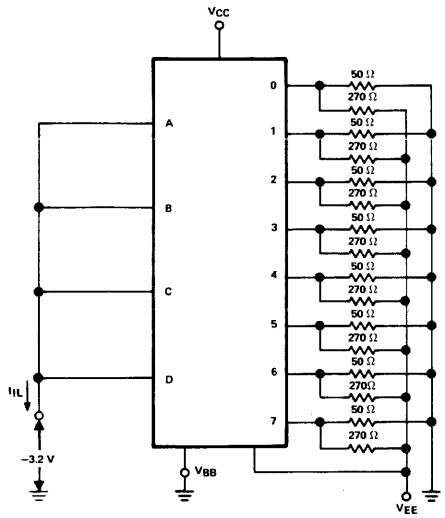
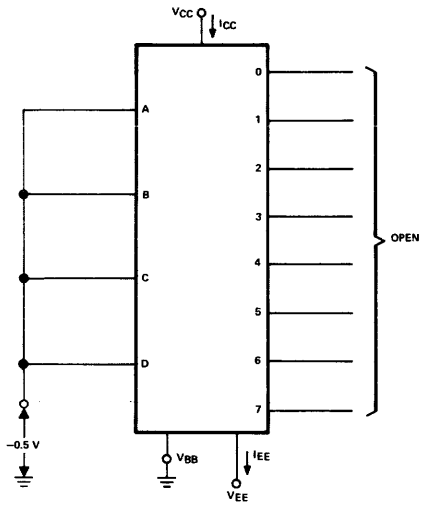


FIGURE 3–I_{IL}



I_{CC} is the total current into both V_{CC} terminals.

FIGURE 4–I_{CC} OR I_{EE}

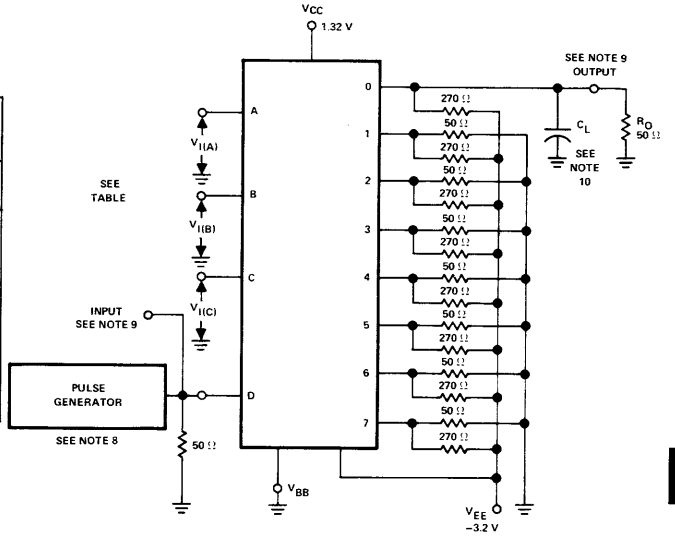
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

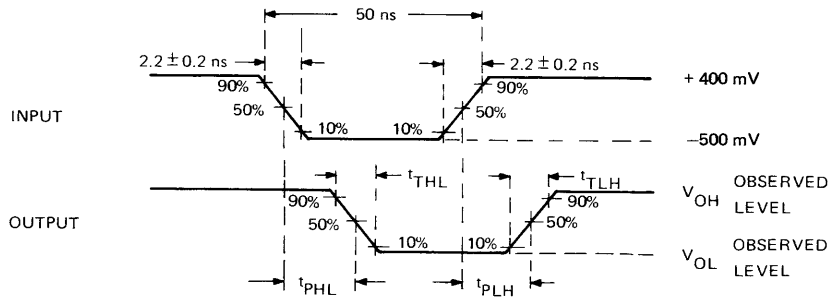
PARAMETER MEASUREMENT INFORMATION

INPUT TERMINAL			OUTPUT UNDER TEST	
13	12	11		
$V_{I(A)}$	$V_{I(B)}$	$V_{I(C)}$	LINE	TERMINAL
0.5 V	0.5 V	0.5 V	0	5
0.5 V	0.5 V	−0.5 V	1	7
0.5 V	−0.5 V	0.5 V	2	8
0.5 V	−0.5 V	−0.5 V	3	9
−0.5 V	0.5 V	0.5 V	4	16
−0.5 V	0.5 V	−0.5 V	5	1
−0.5 V	−0.5 V	0.5 V	6	2
−0.5 V	−0.5 V	−0.5 V	7	4

SEE NOTE 7



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 5—PROPAGATION DELAY AND TRANSITION TIMES

NOTES:
7. The eight combinations of voltages at input terminals A, B, and C shown in the table of Figure 5, are applied sequentially. With each combination of input voltages, the enable input, D, is pulsed from the high level to the low level to give a low-level output at the particular output line shown in the table. The input pulse is measured as it is applied with each combination of input voltages and a waveform measurement is made at the corresponding output.
8. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.
9. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistor designated R_O is the oscilloscope input resistance in the 50-Ω system or a discrete resistor with a high-impedance probe.
10. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

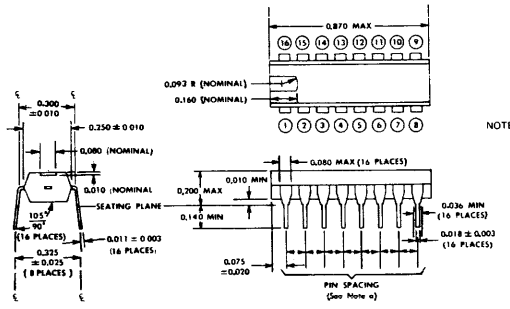
CIRCUIT TYPE ECL2517
EMITTER-COUPLED-LOGIC DECODER

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES a. The true position pin spacing is 0.100 between center lines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.

terminal designations

Pin assignments are shown in the table below and correspond to the logic diagram on page 3.
Outputs are denoted by the numbers 0 through 7. Inputs are denoted by A, B, C, and D.
Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2517	5	6	V_{CC}	7	0	V_{CC}	1	2	3	V_{EE}	C	B	A	D	V_{BB}	4

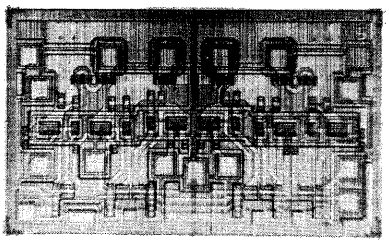
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES ECL2520 THRU ECL2523
DUAL PARALLEL EMITTER-FOLLOWER GATES

ECL2500 SERIES DUAL EMITTER-COUPLED-LOGIC (ECL) PARALLEL EMITTER-FOLLOWER GATES FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS

description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.



The ECL2500 family includes:

- Basic Gate Modules
- **Multifunction Gate Modules**
- Bistable Modules
- Arithmetic Modules
- Interface Modules
- Memory Modules

family features

- High speed . . . typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ± 225 mV typical at 25°C

This data sheet covers the parallel emitter-follower modules.
Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series parallel emitter-follower gates

The four ECL2500 series modules that form the dual parallel emitter-follower gate group are shown in the table below. These modules contain various combinations of the ECL circuit shown in the schematic of Figure A and the logic diagrams of Figure B.

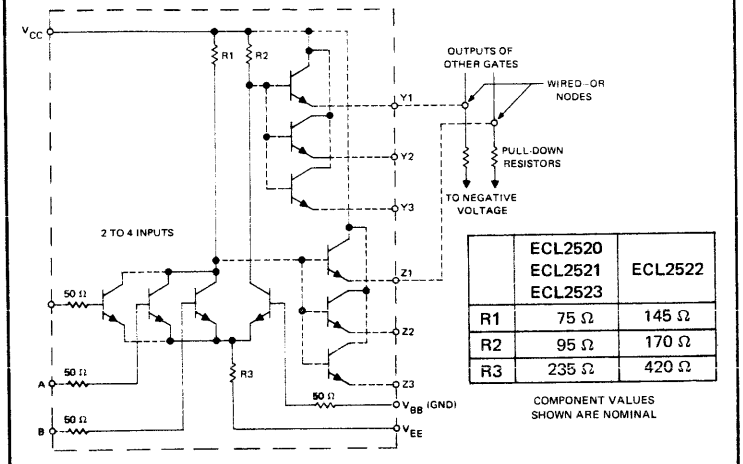
SUMMARY OF MODULES IN PARALLEL EMITTER-FOLLOWER GATE GROUP

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS PER GATE	
				Y(OR)	Z(NOR)
ECL2520	2	2	OR/NOR	3	1
ECL2521	2	3	OR	3	
ECL2522	2	4	NOR		2
ECL2523	2	3	NOR		3

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES ECL2520 THRU ECL2523
DUAL PARALLEL EMITTER-FOLLOWER GATES

schematic



	ECL2520 ECL2521 ECL2523	ECL2522
R1	75 Ω	145 Ω
R2	95 Ω	170 Ω
R3	235 Ω	420 Ω

COMPONENT VALUES SHOWN ARE NOMINAL

FIGURE A—TYPICAL SCHEMATIC (EACH GATE)

logic

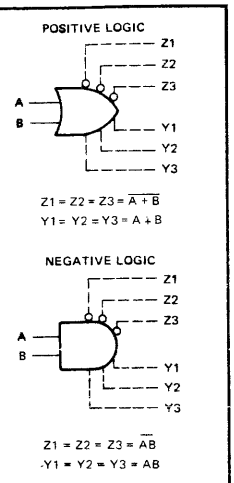


FIGURE B
TYPICAL LOGIC DIAGRAMS

Positive logic OR/NOR functions or negative logic AND/NAND functions are provided at the Y (OR) and Z (NOR) outputs, as shown.

Emitter-follower outputs require an external pull-down resistor. The wired-OR function can be obtained by connecting emitter-follower outputs of separate gates together. Only one pull-down resistor is required for each wire-OR node. Each output of a gate can be wire-OR connected independently of the other outputs of that gate.

absolute maximum ratings (see note 1)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Temperature range with supply and bias voltages applied . . . . . −40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Output Y	All inputs high			−40 mA
Output Z	All inputs low			−40 mA

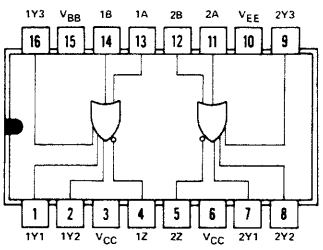
NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

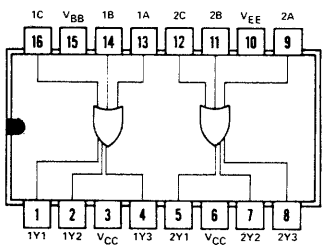
Supply voltage V_{CC}	1.32 V ± 2%
Supply voltage V_{EE}	−3.2 V ± 2%
Reference voltage V_{BB}	0 V (GND)
Reverse bias on unused inputs	−1 V ± 0.5 V
Normalized d-c fan-out	0 to 35
Load on each output	characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range	0°C to 75°C

ECL2520



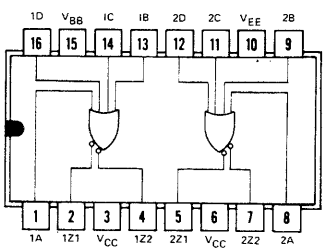
DUAL 2-INPUT OR/NOR GATE
(1 NOR, 3 OR OUTPUTS PER GATE)

ECL2521



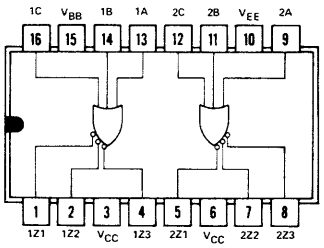
DUAL 3-INPUT OR GATE
(3 OR OUTPUTS PER GATE)

ECL2522



DUAL 4-INPUT NOR GATE
(2 NOR OUTPUTS PER GATE)

ECL2523



DUAL 3-INPUT NOR GATE
(3 NOR OUTPUTS PER GATE)

MODULE	POSITIVE LOGIC OUTPUT		NEGATIVE LOGIC OUTPUT	
	Y(OR)	Z(NOR)	Y (AND)	Z (NAND)
ECL2520	A+B	$\overline{A+B}$	AB	$\overline{AB}$
ECL2521	A+B+C		ABC	
ECL2522		$\overline{A+B+C+D}$		$\overline{ABCD}$
ECL2523		$\overline{A+B+C}$		$\overline{ABC}$

truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2520

INPUTS		OUTPUTS			
A	B	Y1	Y2	Y3	Z
L	L	L	L	L	H
X	H	H	H	H	L
H	X	H	H	H	L
H	H	H	H	H	L

ECL2521

INPUTS			OUTPUTS		
A	B	C	Y1	Y2	Y3
L	L	L	L	L	L
H	X	X	H	H	H
X	H	X	H	H	H
X	X	H	H	H	H
H	H	H	H	H	H

ECL2522

INPUTS				OUTPUTS	
A	B	C	D	Z1	Z2
L	L	L	L	H	H
H	L	L	L	L	L
X	H	X	X	L	L
X	X	H	X	L	L
X	X	X	H	L	L
H	H	H	H	L	L

ECL2523

INPUTS			OUTPUTS		
A	B	C	Z1	Z2	Z3
L	L	L	H	H	H
H	X	X	L	L	L
X	H	X	L	L	L
X	X	H	L	L	L
H	H	H	L	L	L

electrical characteristics at specified free-air temperature

PARAMETER		TEST FIGURE	TEST CONDITIONS*		MODULE ECL2520	MODULE ECL2521	MODULE ECL2522	MODULE ECL2523	MIN	TYP	MAX (SEE NOTE 4)	UNIT
V_{IH}	High-level input voltage			0°C	•	•	•	•	150		720	mV
				25°C					150		720	
				75°C					150		720	
V_{IL}	Low-level input voltage			0°C	•	•	•	•	−1500		−150	mV
				25°C					−1500		−150	
				75°C					−1500		−150	
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.2 V	0°C	•	•			290	365		mV
				25°C					325	400	500	
				75°C						470	580	
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.2 V	0°C	•	•			−505	−445		mV
				25°C					−490	−425	−350	
				75°C						−385	−310	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.2 V	0°C	•				340	415		mV
				25°C					375	450	525	
				75°C						520	605	
				0°C			•		280	355		mV
				25°C					315	390	500	
				75°C						460	580	
				0°C				•	290	365		mV
				25°C					325	400	500	
				75°C						470	580	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.2 V	0°C	•		•	•		−385		mV
				25°C					−420	−365	−310	
				75°C						−325	−280	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.4 V	0°C	•		•	•	−505	−455		mV
				25°C					−490	−425		
				75°C						−380	−315	
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.15 V	0°C	•	•			265			mV
				25°C					300			
				75°C								
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.15 V	0°C	•	•					−325	mV
				25°C							−290	
				75°C								
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.15 V	0°C			•		255			mV
				25°C					290			
				75°C								
				0°C				•	265			mV
				25°C					300			
				75°C								
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.15 V	0°C			•	•			−290	mV
				25°C							−260	
				75°C								
I_{IH}	High-level input current	3	V_I = 0.5 V	0°C	•	•	•	•			510†	μA
				25°C							470†	
				75°C							400†	
I_{IL}	Low-level input current	4	V_I = −3.2 V	0°C	•	•	•	•			−0.5‡	μA
				25°C							−0.6‡	
				75°C							−0.8‡	
I_{CC} or $-I_{EE}$	Supply current	5	V_I = −0.5 V	25°C	•				15		27	mA
						•			15		27	
							•		8		15	
								•	15		27	
C_{in}	Input capacitance		See Note 5	25°C	•	•	•	•		6		pF
z_{out}	Output impedance		See Note 6	25°C	•	•	•	•		5		Ω

*V_{BB} = GND, V_{CC} = 1.32 V ± 1%, V_{EE} = −3.20 V ± 1%.
†These are worst-case values. See Supplementary Parameter Measurement Information for each gate.
‡These are worst-case values for eight inputs in parallel. See Supplementary Parameter Measurement Information for each gate.

NOTES: 4. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.
5. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V.
6. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

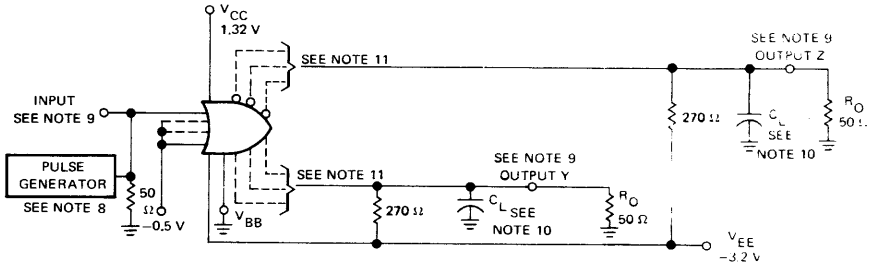
operating characteristics at specified free-air temperature (see figure 1)

PARAMETER		C_L	T_A	ECL2520						ECL2521			ECL2522 ECL2523			UNIT
				Y OUTPUTS			Z OUTPUTS			Y OUTPUTS			Z OUTPUTS			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation delay time, high-to-low-level output and/or	4 pF	0°C		3.2			2.1			3.2			3.3		
			25°C	2.2	3.2	4.3	1.3	2.1	3.1	2.2	3.2	4.3	2.2	3.2	4.3	ns
			75°C		3.2			2.1			3.2			3.3		
t_{PLH}	Propagation delay time, low-to-high-level output	50 pF	0°C		4.3			3.1			4.3			4.5		
			25°C	3.2	4.3	5.6	2.1	3.1	4.2	3.2	4.3	5.6	3.2	4.3	5.6	ns
			75°C		4.3			3.1			4.3			4.5		
t_{THL}	Transition time high-to-low-level output and/or	4 pF	0°C		5.1			2.6			5.1			5.3		
			25°C	2.8	5.2	6.5	1.7	2.6	3.9	2.8	5.2	6.5	2.8	5.2	6.5	ns
			75°C		5.1			2.6			5.1			5.1		
t_{TLH}	Transition time, low-to-high-level output	50 pF	0°C		4.9						4.9			4.9		
			25°C	2.8	4.8	6.5	See Note 7			2.8	4.8	6.5	2.8	4.8	6.5	ns
			75°C		4.7						4.7			4.7		

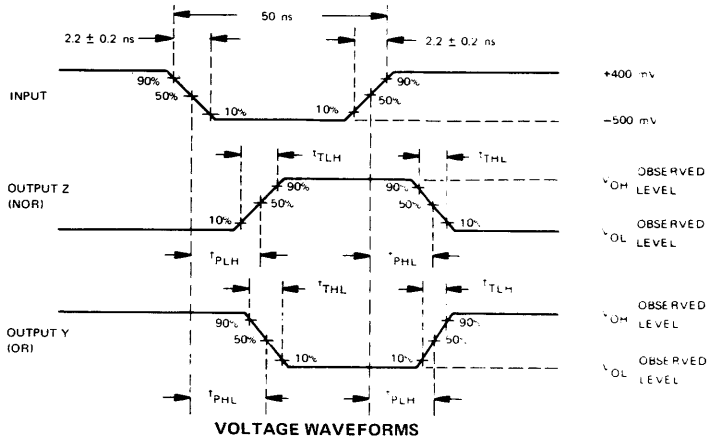
NOTE: 7. The transition times for the Z output at C_L = 50 pF are:
t_{THL} values are the same as for the Y output at 50 pF;
t_{TLH} values are the same as for the Z output at 4 pF.

4

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

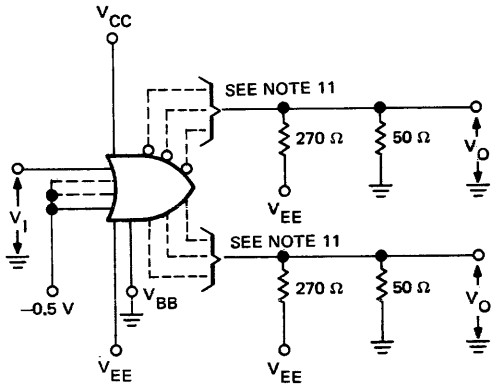


VOLTAGE WAVEFORMS

FIGURE 1—PROPAGATION DELAY AND TRANSITION TIMES

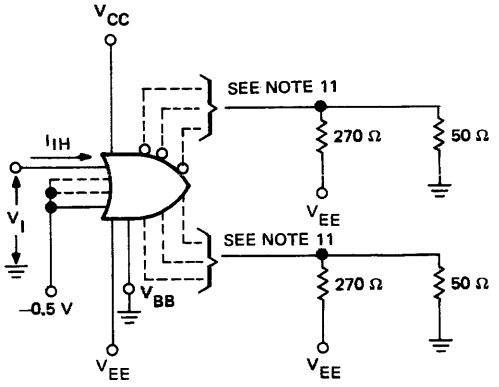
NOTES: 8. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.
9. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistors designated R_O are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.
10. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.
11. Each of the output terminals is loaded as shown.

PARAMETER MEASUREMENT INFORMATION†



A. V_I is applied to each input separately.
B. Each output is tested separately.

FIGURE 2–V_{OH} and V_{OL}



Each input is tested separately.

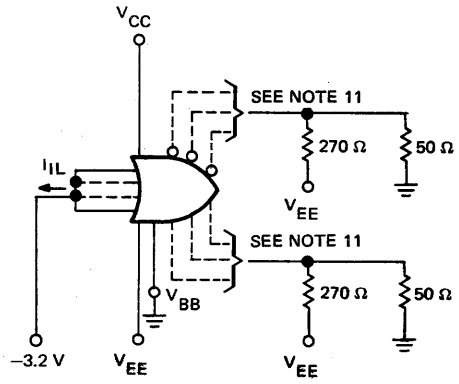
FIGURE 3–I_{IH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

NOTE: 11. Each of the output terminals is loaded as shown.

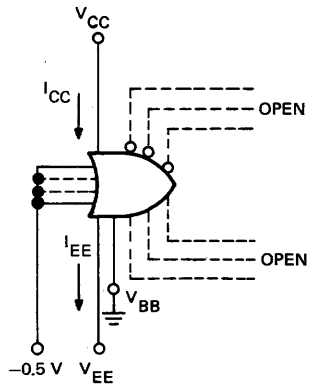
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION†



All inputs of both gates are connected in parallel.

FIGURE 4—I_{IL}



A. Both gates are tested simultaneously.
B. I_{CC} is the total current into both V_{CC} terminals.

FIGURE 5—I_{CC} or I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

NOTE: 11. Each of the output terminals is loaded as shown.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 12)	TERMINALS TO BE TESTED (SEE NOTE 13)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2520 V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V											
$V_{OH(Y)}$	13, 14	1, 2, 16	2	0.2 V	−0.5 V	−0.5 V	0°C	290	365		mV
	11, 12	7, 8, 9					25°C	325	400	500	
							75°C		470	580	
$V_{OL(Y)}$	13, 14	1, 2, 16	2	−0.2 V	−0.5 V	−0.5 V	0°C	−505	−445		mV
	11, 12	7, 8, 9					25°C	−490	−425	−350	
							75°C		−385	−310	
$V_{OH(Z)}$	13, 14	4	2	−0.2 V	−0.5 V	−0.5 V	0°C	340	415		mV
	11, 12	5					25°C	375	450	525	
							75°C		520	605	
$V_{OL(Z)}$	13, 14	4	2	0.2 V	−0.5 V	−0.5 V	0°C		−385		mV
	11, 12	5					25°C	−440	−365	−310	
							75°C		−325	−280	
$V_{OL(Z)}$	13, 14	4	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−455		mV
	11, 12	5					25°C	−490	−425		
							75°C		−380	−315	
$V_{OH(Y)}$	11, 12	7	2	0.15 V	−0.5 V	−0.5 V	0°C	265			mV
							25°C	300			
							75°C				
$V_{OL(Y)}$	11, 12	7	2	−0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−325	
							75°C			−290	
I_{IH}	13, 14		3	0.5 V	−0.5 V	−0.5 V	0°C			510	μA
	11, 12						25°C			470	
							75°C			400	
I_{IL}	11, 12, 13, 14		4	All inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
							25°C			−0.5	
							75°C			−0.5	
ECL2521 V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V											
$V_{OH(Y)}$	9, 11, 12	5, 7, 8	2	0.2 V	−0.5 V	−0.5 V	0°C	290	365		mV
	13, 14, 16	1, 2, 4					25°C	325	400	500	
							75°C		470	580	
$V_{OL(Y)}$	9, 11, 12	5, 7, 8	2	−0.2 V	−0.5 V	−0.5 V	0°C	−505	−445		mV
	13, 14, 16	1, 2, 4					25°C	−490	−425	−350	
							75°C		−385	−310	
$V_{OH(Y)}$	13, 14, 16	1	2	0.15 V	−0.5 V	−0.5 V	0°C	265			mV
							25°C	300			
							75°C				
$V_{OL(Y)}$	13, 14, 16	1	2	−0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−325	
							75°C			−290	
I_{IH}	9, 11, 12		3	0.5 V	−0.5 V	−0.5 V	0°C			510	μA
	13, 14, 16						25°C			470	
							75°C			400	
I_{IL}	9, 11, 12, 13, 14, 16		4	All inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
							25°C			−0.5	
							75°C			−0.6	

NOTES: 12. See page 4 for defining term associated with each symbol.
13. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 12)	TERMINALS TO BE TESTED (SEE NOTE 13)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2522 V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V											
$V_{OH(Z)}$	1, 13, 14, 16	2, 4	2	−0.2 V	−0.5 V	−0.5V	0°C	280	355		mV
	8, 9, 11, 12	5, 7					25°C	315	390	500	
							75°C		460	580	
$V_{OL(Z)}$	1, 13, 14, 16	2, 4	2	0.2 V	−0.5 V	−0.5 V	0°C		−385		mV
	8, 9, 11, 12	5, 7					25°C	−440	−365	−310	
							75°C		−325	−280	
$V_{OL(Z)}$	1, 13, 14, 16	2, 4	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−455		mV
	8, 9, 11, 12	5, 7					25°C	−490	−425		
							75°C		−380	−315	
$V_{OH(Z)}$	1, 13, 14, 16	2	2	−0.15 V	−0.5 V	−0.5 V	0°C	255			mV
							25°C	290			
							75°C				
$V_{OL(Z)}$	1, 13, 14, 16	2	2	0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−290	
							75°C			−260	
I_{IH}	1, 13, 14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C			255	μA
	8, 9, 11, 12						25°C			235	
							75°C			200	
I_{IL}	1, 8, 9, 11, 12, 13, 14, 16		4	All inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
							25°C			−0.6	
							75°C			−0.8	
ECL2523 V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V											
$V_{OH(Z)}$	13, 14, 16	1, 2, 4	2	−0.2 V	−0.5 V	−0.5 V	0°C	290	365		mV
	9, 11, 12	5, 7, 8					25°C	325	400	500	
							75°C		470	580	
$V_{OL(Z)}$	13, 14, 16	1, 2, 4	2	0.2 V	−0.5 V	−0.5 V	0°C		−385		mV
	9, 11, 12	5, 7, 8					25°C	−440	−365	−310	
							75°C		−325	−280	
$V_{OL(Z)}$	9, 11, 12	5	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−455		mV
							25°C	−490	−425		
							75°C		−380	−315	
$V_{OH(Z)}$	9, 11, 12	5	2	−0.15 V	−0.5 V	−0.5 V	0°C	265			mV
							25°C	300			
							75°C				
$V_{OL(Z)}$	9, 11, 12	5	2	0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−290	
							75°C			−260	
I_{IH}	13, 14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C			510	μA
	9, 11, 12						25°C			470	
							75°C			400	
I_{IL}	9, 11, 12, 13, 14, 16		4	All inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
							25°C			−0.5	
							75°C			−0.6	

NOTES: 12. See page 4 for defining term associated with each symbol.
13. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

operating characteristics at specified free-air temperature (see figure 1)

TERMINALS TO BE TESTED (SEE NOTES 14, 15, 16)				C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns									t_{THL} and/or t_{TLH} TRANSITION TIMES—ns								
					$T_A = 0°C$			$T_A = 25°C$			$T_A = 75°C$			$T_A = 0°C$			$T_A = 25°C$			$T_A = 75°C$		
INPUT	OUTPUT	INPUT	OUTPUT	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2520																						
13, 14	1, 2, 16	11, 12	7, 8, 9	4		3.2		2.2	3.2	4.3		3.2			5.1		2.8	5.2	6.5		5.1	
				50		4.3		3.2	4.3	5.6		4.3			4.9		2.8	4.8	6.5		4.7	
13, 14	4	11, 12	5	4		2.1		1.3	2.1	3.1		2.1			2.6		1.7	2.6	3.9		2.6	
				50		3.1		2.1	3.1	4.2		3.1			2.6† 4.9‡		1.7† 2.8‡	2.6† 4.8‡	3.9† 6.5‡		2.6† 4.7‡	
ECL2521																						
13, 14, 16	1, 2, 4	9, 11, 12	5, 7, 8	4		3.2		2.2	3.2	4.3		3.2			5.1		2.8	5.2	6.5		5.1	
				50		4.3		3.2	4.3	5.6		4.3			4.9		2.8	4.8	6.5		4.7	
ECL2522																						
1, 13, 14, 16	2, 4	8, 9, 11, 12	5, 7	4		3.3		2.2	3.2	4.3		3.3			5.3		2.8	5.2	6.5		5.1	
				50		4.5		3.2	4.3	5.6		4.5			4.9		2.8	4.8	6.5		4.7	
ECL2523																						
13, 14, 16	1, 2, 4	9, 11, 12	5, 7, 8	4		3.3		2.2	3.2	4.3		3.3			5.3		2.8	5.2	6.5		5.1	
				50		4.5		3.2	4.3	5.6		4.5			4.9		2.8	4.8	6.5		4.7	

†For t_{TLH} only.
‡For t_{THL} only.

NOTES: 14. Each gate is tested separately.
15. The input pulse is measured as it is applied sequentially to each input of the gate under test, and a waveform measurement is made at each of the outputs of that gate. Times are as defined in Figure 1.
16. Bias voltages and loads for the gate under test are shown in Figure 1. The unused gate has inputs biased to −0.5 V, outputs under load, and power applied.

GENERAL APPLICATION INFORMATION

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

Applications of the parallel emitter-follower gates at other than data sheet conditions are covered in a separate ECL2500 Series application document.

General loading for fan-out may be divided into two classes:

CLASS I Short-Line or Cluster Loading.

Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II Long-Line or Distributive Loading.

These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

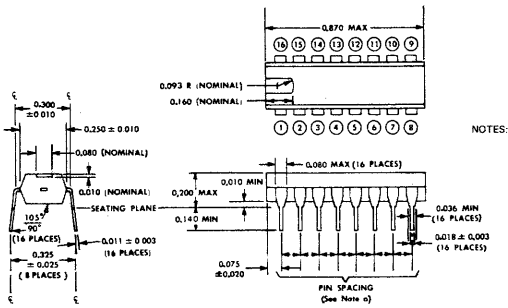
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

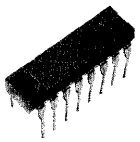
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



4

terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams on page 3.
Outputs are denoted by Y or Z. Inputs are denoted by A, B, C, etc.
Respective inputs and outputs are identified by a gate number preceding the pin symbol.
Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2520	1Y1	1Y2	V_{CC}	1Z	2Z	V_{CC}	2Y1	2Y2	2Y3	V_{EE}	2A	2B	1A	1B	V_{BB}	1Y3
ECL2521	1Y1	1Y2	V_{CC}	1Y3	2Y1	V_{CC}	2Y2	2Y3	2A	V_{EE}	2B	2C	1A	1B	V_{BB}	1C
ECL2522	1A	1Z1	V_{CC}	1Z2	2Z1	V_{CC}	2Z2	2A	2B	V_{EE}	2C	2D	1B	1C	V_{BB}	1D
ECL2523	1Z1	1Z2	V_{CC}	1Z3	2Z1	V_{CC}	2Z2	2Z3	2A	V_{EE}	2B	2C	1A	1B	V_{BB}	1C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TI world-wide sales offices

ALABAMA

Sahara Office Park Bldg., Suite 111
3313 Memorial Parkway, S.W.
Huntsville, Alabama 35801
205-881-4061

ARIZONA

2535 W. Camelback Rd., Suite 1D
Phoenix, Arizona 85017
602-279-5531

CALIFORNIA

1800 North Argyle Ave.
Hollywood, California 90028
213-466-7251

5005 West Century Blvd., Suite 208
Inglewood, California 90301
213-673-3943

230 California Ave., Suite 201
Palo Alto, California 94306
415-326-6770

1505 East 17th St., Suite 201
Santa Ana, California 92701
714-547-6506

4185 Adams Ave.
San Diego, California 92116
714-284-1181

COLORADO

2186 South Holly St., Suite 204
Denver, Colorado 80222
303-757-8548

CONNECTICUT

300 Amity Road
Woodbridge, Connecticut 06525
203-389-4521

FLORIDA

5400 Diplomat Circle
Diplomat Bldg., Suite 252
Orlando, Florida 32810
305-644-3535

3151 Third Ave. North
300 West Bldg., Room 429
St. Petersburg, Florida 33704
813-898-0807

ILLINOIS

Suite 205, Executive Towers
5901 N. Cicero Ave.
Chicago, Illinois 60646
312-286-1000

MASSACHUSETTS

60 Hickory Drive
Waltham, Mass. 02154
617-891-8450

MICHIGAN

Suite 706 West, Northland Towers Bldg.
15565 Northland Dr.
Southfield, Michigan 48075
313-357-1703

MINNESOTA

7615 Metro Blvd.
Suite 202, U.C.L.I. Bldg.
Edina, Minn. 55424
612-941-4384

NEW JERSEY

25 U.S. Highway 22
Springfield, New Jersey 07081
201-376-9400

NEW YORK

P. O. Box 87, 2209 E. Main
Endicott, New York 13760
607-785-9987

4 Nevada Drive
New Hyde Park, N. Y. 11040
516-488-2200

167 Main Street
Fishkill, New York 12524
914-896-6793

6563 Ridings Rd.
Syracuse, New York 13206
315-463-9291

OHIO

23811 Chagrin Blvd., Suite 100
Cleveland, Ohio 44122
216-464-1192

Suite 205, Paul Welch Bldg.
3300 South Dixie Dr.
Dayton, Ohio 45439
513-298-7513

PENNSYLVANIA

Benjamin Fox Pavilion
Suite 424, Foxcroft Square
Jenkintown, Pa. 19046
215-885-3454

TEXAS

MS80 — P.O. Box 5012
Dallas, Texas 75222
214-238-4861

3801 Kirby Bldg., Suite 600
Houston, Texas 77006
713-526-3268, 9

WASHINGTON

5801 Sixth Ave. S.
Seattle, Washington 98108
206-762-4240

WASHINGTON, D.C.

1875 Connecticut Ave., N.W., Suite 913
Washington, D.C. 20009
202-234-9320

CANADA

280 Centre Str. West
Richmond Hill
Ontario, Canada
416-889-7373

EUROPE

Texas Instruments Limited
Manton Lane
Bedford, England

Texas Instruments France S. A.
Boite Postale 5
Villeneuve-Loubet (A.M.), France

Texas Instruments France S. A.
379 Av de la Liberation
92 Clamart, France

Texas Instruments France S.A.
Lyon Branch
30-31 Quai Rambaud
69 — Lyon, France

Texas Instruments France S.A.
Metz Branch
5, Rue Lancon
57 — Metz, France

Texas Instruments France S.A.
Toulouse Branch
20, Avenue Honore-Serre
31 — Toulouse, France

Texas Instruments Holland N.V.
P.O. Box 7603
Entrepotgebouw Kamer 225-227
Schiphol-Centrum
Netherland

Texas Instruments Italia S.p.A.
Via Colautti 1
Milan, Italy

Texas Instruments Italia S.p.A.
Via Padre Semeria, 63
Rome, Italy

Texas Instruments Sweden A.B.
Timmermansgatan 34, Box 17116
Stockholm 17, Sweden

Texas Instruments Deutschland GmbH
Am Mittelfelde 169
3000 Hannover, W. Germany

Texas Instruments Deutschland GmbH
Im Kaisemer 5
7000 Stuttgart-N
West Germany

Texas Instruments Deutschland GmbH
Arabellastrasse 4-Sternhaus
8000 Munich 81
West Germany

Texas Instruments Deutschland GmbH
Kepserstrasse 33
8050 Freising-Lerchenzeld
West Germany

Texas Instruments Deutschland GmbH
Westendstrasse 52
6000 Frankfurt, West Germany

MEXICO

Texas Instruments de Mexico S.A.
Poniente 116 #489
Col. Ind. Vallejo
Mexico 15, D.F.

ARGENTINA

Texas Instruments Argentina S.A.I.C.F.
Ruta Panamericana KM. 13,5
Don Torcuato (Pdo. de Tigre)
Prov. de Buenos Aires

BRAZIL

Texas Instrumentos Electronicos
do Brazil Ltda.
Rua Cesario Alvim 770
Caixa Postal 30.103
Sao Paulo 6, Brazil

AUSTRALIA

Texas Instruments Australia Ltd.
Box 63, Oldham Road
Elizabeth, South Australia

Texas Instruments Australia Ltd.
Room 5, Rural Bank Bldg.
Burwood, N.S.W., Australia

ASIA

Texas Instruments Asia Limited
617 Sanno Grand Building
14-2, Nagatacho 2 Chome
Chiyoda-Ku, Tokyo, Japan

Texas Instruments Japan Limited
18-8, Minami 3 Chome
Hatogaya City, Saitama Pref.
334 Japan

Texas Instruments Asia Limited
Room 1502 Star House
Harbour Centre
Kowloon
Hong Kong

Texas Instruments Singapore (PTE)
Limited
Factory 4-B
27 Kallang Place
Singapore 12
Republic of Singapore

I-2180 30M 109

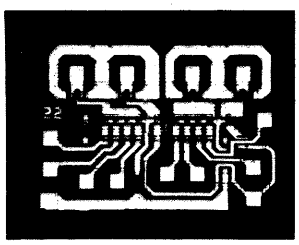
Printed in U.S.A.

TYPES ECL2530, ECL2531
DUAL LINE RECEIVER AND DUAL LINE DRIVER

TYPES ECL2530, ECL2531
BULLETIN NO. DL-S 6911250, NOVEMBER 1969

ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL)
DUAL LINE RECEIVER AND DUAL LINE DRIVER
FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS

description



The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.

The ECL2500 family includes:

- Basic Gate Modules
- Multifunction Gate Modules
- Bistable Modules
- Arithmetic Modules
- **Interface Modules**
- Memory Module

family features

- High speed . . . typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ± 225 mV typical at 25°C

This data sheet covers the line receiver and the line driver modules.
Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series line receiver and line driver

The ECL2500 series dual line receiver and dual line driver modules are shown in the tables below. These modules contain various combinations of the ECL circuit shown in the schematic of Figure A and the logic diagrams of Figure B.

SUMMARY OF LINE RECEIVER AND LINE DRIVER MODULES

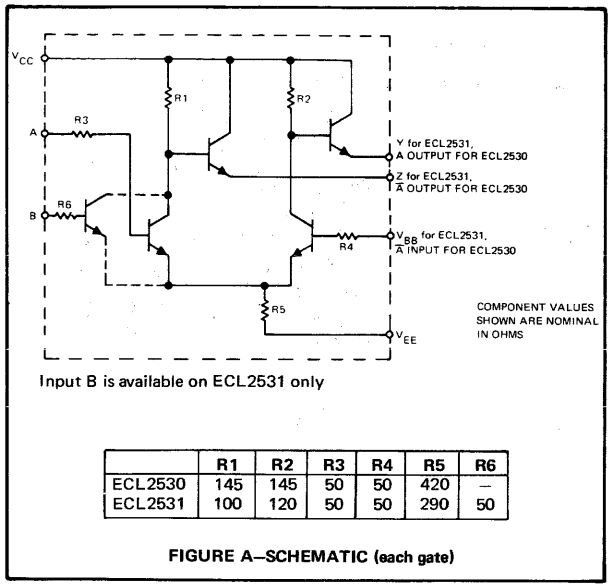
MODULE	DIFFERENTIAL AMPLIFIERS PER MODULE	DIFFERENTIAL INPUTS PER AMPLIFIER	POSITIVE LOGIC	DIFFERENTIAL OUTPUTS PER AMPLIFIER	
				A	$\overline{A}$
ECL2530 Line Receiver	2	2	NOR/OR	1	1

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS PER GATE	
				Y (OR)	Z (NOR)
ECL2531 Line Driver	2	2	NOR/OR	1	1

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES ECL2530, ECL2531
DUAL LINE RECEIVER AND DUAL LINE DRIVER

schematic



Input B is available on ECL2531 only

	R1	R2	R3	R4	R5	R6
ECL2530	145	145	50	50	420	—
ECL2531	100	120	50	50	290	50

FIGURE A–SCHEMATIC (each gate)

logic

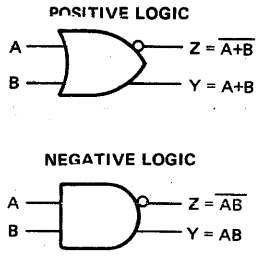


FIGURE B–ECL2531 LOGIC DIAGRAMS

Positive logic OR/NOR functions or negative logic AND/NAND functions are provided at the Y (OR) and Z (NOR) outputs, as shown. When the $\overline{A}$ input of the ECL2530 is connected to V_{BB}, the A and $\overline{A}$ outputs function as OR (Y) and NOR (Z) outputs respectively; and vice versa when the A input is connected to V_{BB}.

Emitter-follower outputs require an external pull-down resistor. The wired-OR function can be obtained by connecting emitter-follower outputs of separate gates together. Only one pull-down resistor is required for each wired-OR node.

absolute maximum ratings (see note 1)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Temperature range with supply and bias voltage applied . . . . . −40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C to 75°C (SEE NOTES 2 AND 3)

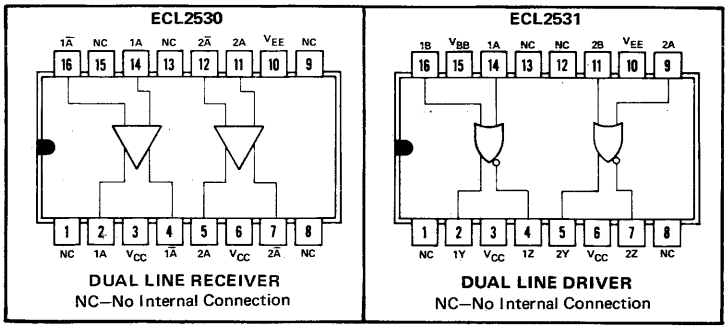
TERMINAL	REMARKS	VOLTAGE		CURRENT	
		CONTINUOUS	20-μs SURGE	ECL2530	ECL2531
V_{CC}		2 V	4.5 V		
V_{EE}		−4 V	−7 V		
Each Input	Other input of ECL2530 at V_{BB}, all other inputs of ECL2531 open	−3.5 V	−4 V		
		2 V	2 V		
Output Y	All inputs (input A of ECL2530) high			−40 mA	−50 mA
Output Z	All inputs (input A of ECL2530) low			−40 mA	−50 mA

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

1169

logic



ECL2530†

POSITIVE LOGIC		NEGATIVE LOGIC	
A (OR)	Ā (NOR)	A (AND)	Ā (NAND)
A	Ā	A	Ā

†With Ā input at V_{BB}

ECL2531

POSITIVE LOGIC		NEGATIVE LOGIC	
Y (OR)	Z (NOR)	Y (AND)	Z (NAND)
A + B	$\overline{A+B}$	AB	$\overline{AB}$

truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2530			
INPUTS		OUTPUTS	
A	Ā	A	Ā
L	V_{BB}	L	H
H	V_{BB}	H	L
V_{BB}	L	H	L
V_{BB}	H	L	H

ECL2531			
INPUTS		OUTPUTS	
A	B	Y	Z
L	L	L	H
H	X	H	L
X	H	H	L
H	H	H	L

4

recommended operating conditions

Supply voltage V_{CC}	1.32 V ± 2%
Supply voltage V_{EE}	−3.2 V ± 2%
Reference voltage V_{BB}	0 V (GND)
Reverse bias on unused inputs	−1 V ± 0.5 V
Normalized d-c fan-out	0 to 35
Load on each output	ECL2530 characterized at 270 Ω to V_{EE}, 50 Ω to GND ECL2531 characterized at 135 Ω to V_{EE}, 25 Ω to GND
Operating free-air temperature range	0°C to 75°C

GENERAL APPLICATION INFORMATION

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

Applications of the line receiver and the line driver modules at other than data sheet conditions are covered in a separate ECL2500 series application document.

General loading for fan-out may be divided into two classes:

CLASS I **Short-Line or Cluster Loading.**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II **Long-Line or Distributive Loading.**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 4)		TEST FIGURE	TEST CONDITIONS*		ECL2530 MIN	ECL2530 TYP (SEE NOTE 5)	ECL2530 MAX	ECL2531 MIN	ECL2531 TYP (SEE NOTE 5)	ECL2531 MAX	UNIT
V_{IH}	High-level input voltage			0°C	150		720	150		720	mV
				25°C	150		720	150		720	
				75°C	150		720	150		720	
V_{IL}	Low-level input voltage			0°C	−1500		−150	−1500		−150	mV
				25°C	−1500		−150	−1500		−150	
				75°C	−1500		−150	−1500		−150	
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.2 V	0°C				290	365		mV
				25°C				325	400	475	
				75°C					470	560	
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.2 V	0°C				−505	−450		mV
				25°C				−495	−430	−355	
				75°C					−390	−310	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.2 V	0°C	315	390		290	365		mV
				25°C	350	425	500	325	400	475	
				75°C		495	580		470	560	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.2 V	0°C		−385			−400		mV
				25°C	−440	−365	−310	−450	−380	−310	
				75°C		−325	−280		−340	−280	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.4 V	0°C	−505	−455		−505	−460		mV
				25°C	−490	−425		−495	−430		
				75°C		−380	−315		−385	−315	
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.15 V	0°C				270			mV
				25°C				305			
				75°C							
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.15 V	0°C							mV
				25°C						−330	
				75°C						−290	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.15 V	0°C	290						mV
				25°C	325						
				75°C							
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.15 V	0°C							mV
				25°C			−290				
				75°C			−260				
I_{IH}	High-level input current	3	V_I = 0.5 V	0°C			255			385	μA
				25°C			235			350	
				75°C			200			300	
I_{IL}	Low-level input current	4	V_I = −3.2 V	0°C			−0.5			−0.5	μA
				25°C			−0.5			−0.5	
				75°C			−0.5			−0.5	
I_{CC} or I_{EE}	Supply current	5	V_I = −0.5 V	25°C	8		15	12		22	mA
C_{in}	Input capacitance		See Note 6	25°C		5			5		pF
z_{out}	Output impedance		See Note 7	25°C		5			5		Ω

*V_{BB} = GND, V_{CC} = 1.32 V ± 1%, V_{EE} = −3.20 V ± 1%

NOTES: 4. When the $\bar{A}$ input of the ECL2530 is connected to V_{BB}, the A and $\bar{A}$ outputs function as OR (Y) and NOR (Z) outputs respectively; and vice versa when the A input is connected to V_{BB}.

5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e. g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

6. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V.

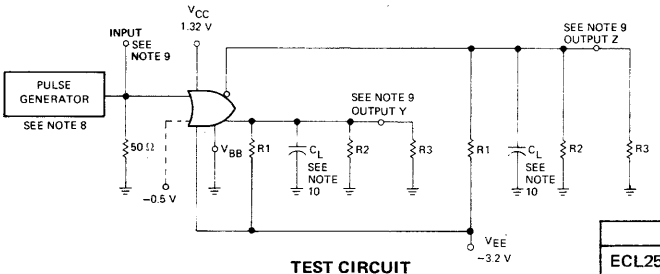
7. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operating characteristics at specified free-air temperature (see figure 1)

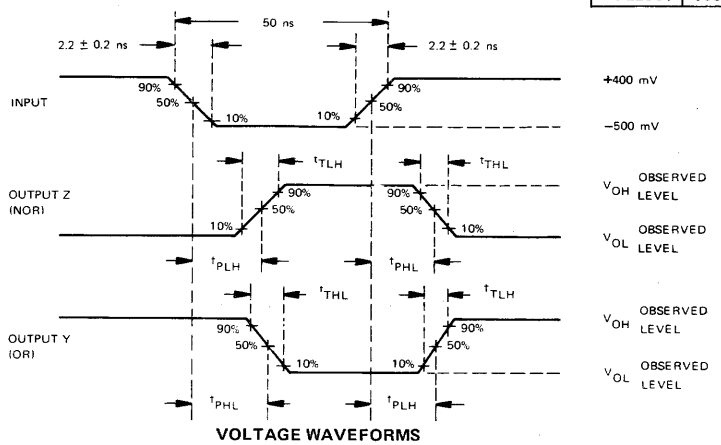
PARAMETER		C_L	T_A	ECL2530 ANY OUTPUT			ECL2531 ANY OUTPUT			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation delay time, high-to-low-level output and/or	4 pF	0°C		2.1			2.7		ns
			25°C	1.3	2.1	3	1.8	2.7	3.7	
			75°C		2.2			2.8		
t_{PLH}	Propagation delay time, low-to-high-level output	50 pF	0°C		3.1			3.5		ns
			25°C	2.3	3.1	4.2	2.6	3.5	4.6	
			75°C		3.1			3.5		
t_{THL}	Transition time, high-to-low-level output and/or	4 pF	0°C		2.7			3.8		ns
			25°C	1.6	2.9	4.2	2.5	3.8	5	
			75°C		2.8			3.9		
t_{TLH}	Transition time, low-to-high-level output	50 pF	0°C		3.6			3.7		ns
			25°C	2.2	3.6	6	2.5	3.7	5	
			75°C		3.6			3.7		

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

	R1	R2	R3
ECL2530	270 Ω	Not Used	50 Ω
ECL2531	135 Ω	50 Ω	50 Ω

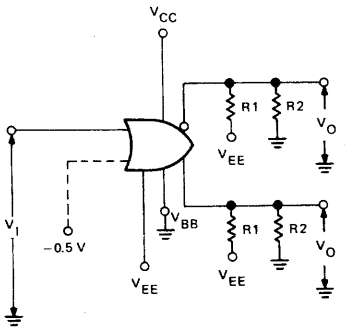


VOLTAGE WAVEFORMS

FIGURE 1–PROPAGATION DELAY AND TRANSITION TIMES

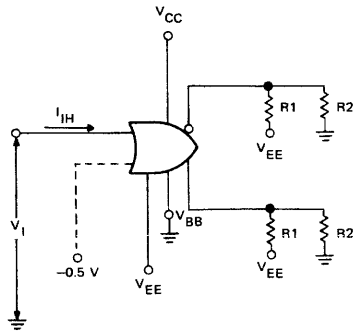
NOTES: 8. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.
9. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF or a 50-Ω impedance system can be used. Resistors R3 are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.
10. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

PARAMETER MEASUREMENT INFORMATION†



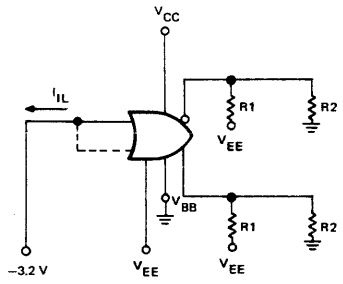
A. V_I is applied to each input separately.
B. Each output is tested separately.
C. For ECL2530, R1 = 270 Ω and R2 = 50 Ω.
For ECL2531, R1 = 135 Ω and R2 = 25 Ω.

FIGURE 2–V_{OH} AND V_{OL}



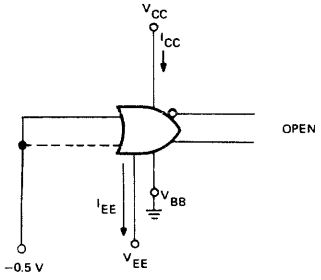
A. Each input is tested separately.
B. For ECL2530, R1 = 270 Ω and R2 = 50 Ω.
For ECL2531, R1 = 135 Ω and R2 = 25 Ω.

FIGURE 3–I_{IH}



A. All inputs of both gates are connected in parallel.
B. For ECL2530, R1 = 270 Ω and R2 = 50 Ω.
For ECL2531, R1 = 135 Ω and R2 = 25 Ω.

FIGURE 4–I_{IL}



A. Both gates are tested simultaneously.
B. I_{CC} is the total current into both V_{CC} terminals.

FIGURE 5–I_{CC} or I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams of page 3.
Outputs are denoted by A and $\overline{A}$ for ECL2530, Y and Z for ECL2531. Inputs are denoted by A, $\overline{A}$, or B.
Respective inputs and outputs are identified by a gate number preceding the pin symbol.
Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.
NC indicates no internal connection.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2530	NC	1A (OUT)	V_{CC}	$1\overline{A}$ (OUT)	2A (OUT)	V_{CC}	$2\overline{A}$ (OUT)	NC	NC	V_{EE}	2A (IN)	$2\overline{A}$ (IN)	NC	1A (IN)	NC	$1\overline{A}$ (IN)
ECL2531	NC	1Y	V_{CC}	1Z	2Y	V_{CC}	2Z	NC	2A	V_{EE}	2B	NC	NC	1A	V_{BB}	1B

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTES 4 AND 11)	TERMINALS TO BE TESTED (SEE NOTE 12)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)		(SEE NOTE 5)			
ECL2530 V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V											
$V_{OH(Z)}$	14 16 11 12	4 2 7 5	2	−0.2 V	GND	OPEN	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	14 16 11 12	4 2 7 5	2	0.2 V	GND	OPEN	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	14 16 11 12	4 2 7 5	2	0.4 V	GND	OPEN	0°C 25°C 75°C	−505 −490	−455 −425 −380	−315	mV
$V_{OH(Z)}$	11	7	2	−0.15 V	GND	OPEN	0°C 25°C 75°C	290 325			mV
$V_{OL(Z)}$	11	7	2	0.15 V	GND	OPEN	0°C 25°C 75°C			−290 −260	mV
I_{IH}	14 16 11 12		3	0.5 V	GND	OPEN	0°C 25°C 75°C			255 235 200	μA
I_{IL}	11, 12, 14, 16		4	All inputs of both gates in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.5 −0.5	μA
ECL2531 V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V											
$V_{OH(Y)}$	14, 16 9, 11	2 5	2	0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	290 325	365 400 470	475 560	mV
$V_{OL(Y)}$	14, 16 9, 11	2 5	2	−0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	−505 −495	−450 −430 −390	−355 −310	mV
$V_{OH(Z)}$	14, 16 9, 11	4 7	2	−0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	290 325	365 400 470	475 560	mV
$V_{OL(Z)}$	14, 16 9, 11	4 7	2	0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	−450	−400 −380 −340	−310 −280	mV
$V_{OL(Z)}$	14, 16 9, 11	4 7	2	0.4 V	−0.5 V	−0.5 V	0°C 25°C 75°C	−505 −495	−460 −430 −385	−315	mV
$V_{OH(Y)}$	9	5	2	0.15 V	−0.5 V	−0.5 V	0°C 25°C 75°C	270 305			mV
$V_{OL(Y)}$	9	5	2	−0.15 V	−0.5 V	−0.5 V	0°C 25°C 75°C			−330 −290	mV
I_{IH}	14, 16 9, 11		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			385 350 300	μA
I_{IL}	9, 11, 14, 16		4	All inputs of both gates in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.5 −0.5	μA

NOTES: 4. When the $\overline{A}$ input of the ECL2530 is connected to V_{BB}, the A and $\overline{A}$ outputs function as OR (Y) and NOR (Z) outputs respectively; and vice versa when the A input is connected to V_{BB}.

5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

11. See page 4 for defining term associated with each symbol.

12. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

operating characteristics at specified free-air temperature (see figure 1)

TERMINALS TO BE TESTED (SEE NOTES 13, 14, 15)				C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns									t_{THL} and/or t_{TLH} TRANSITION TIMES—ns								
					T_A = 0°C			T_A = 25°C			T_A = 75°C			T_A = 0°C			T_A = 25°C			T_A = 75°C		
INPUT	OUTPUT	INPUT	OUTPUT	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2530 (See Note 16)																						
14	2	16	4	4		2.1		1.3	2.1	3		2.2			2.7		1.6	2.9	4.2		2.8	
	4		2	50		3.1		2.3	3.1	4.2		3.1			3.6		2.2	3.6	6		3.6	
11	5	12	7	4		2.1		1.3	2.1	3		2.2			2.7		1.6	2.9	4.2		2.8	
	7		5	50		3.1		2.3	3.1	4.2		3.1			3.6		2.2	3.6	6		3.6	
ECL2531																						
14, 16	2, 4	9, 11	5, 7	4		2.7		1.8	2.7	3.7		2.8			3.8		2.5	3.8	5		3.9	
				50		3.5		2.6	3.5	4.6		3.5			3.7		2.5	3.7	5		3.7	

4

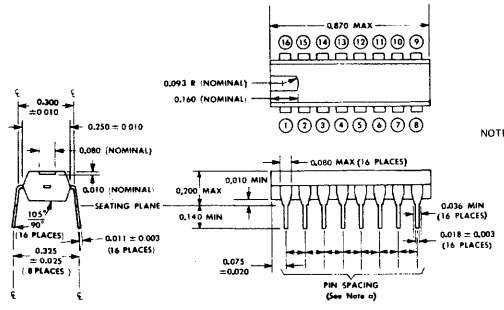
NOTES: 13. Each gate is tested separately.
14. The input pulse is measured as it is applied sequantially to each input of the gate under test and a waveform measurement is made at each of the outputs of that gate. Times are as defined in Figure 1.
15. Bias voltages and loads for the gate under test are shown in Figure 1. The unused gate has inputs biased to −0.5 V, outputs under load, and power applied.
16. When an input pulse is applied to pin 11, pin 12 is at GND, and vice versa. The same relationship holds true between pins 14 and 16.

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

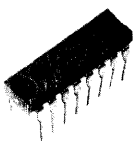
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

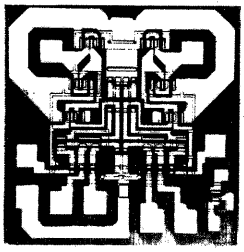
b. All dimensions are in inches unless otherwise noted.



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES ECL2536, ECL2537
BULLETIN NO. DL-S 6911286, DECEMBER 1969

ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) LEVEL CONVERTERS FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS



description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.

The ECL2500 family includes:

- Basic Gate Modules
- Multifunction Gate Modules
- Bistable Modules
- Arithmetic Modules
- Interface Modules
- Memory Module

family features

- High speed . . . typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ± 225 mV typical at 25°C

This data sheet covers the ECL-to-HLL and HLL-to-ECL converter modules.
Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series ECL-to-HLL and HLL-to-ECL converters

The ECL2536 contains two high-level-logic-to-emitter-coupled-logic converters each having an HLL input (B*) and an ECL input (A). Each converter has complementary ECL outputs. The ECL input (A) is provided to be used as an INHIBIT/ENABLE control. When input A is low, the converter is enabled and the output state is determined by input B*. When input A is high, output Y is high and output Z is low regardless of the state of input B*.

The ECL2537 contains two emitter-coupled-logic-to-high-level-logic converters. Each converter has two ECL inputs and complementary HLL outputs.

The ECL2536 and ECL2537 are summarized in the table below, shown schematically in Figure A, and shown logically in Figure B.

SUMMARY OF HLL-TO-ECL AND ECL-TO-HLL CONVERTERS

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS PER GATE	
				Y (OR)	Z (NOR)
ECL2536 DUAL HLL-TO-ECL CONVERTER	2	1 HLL input 1 ECL inhibit input	OR/NOR	1	1
ECL2537 DUAL ECL-TO-HLL CONVERTER	2	2	OR/NOR	1	1

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES ECL2536, ECL2537
HLL-TO-ECL AND ECL-TO-HLL CONVERTERS

schematic

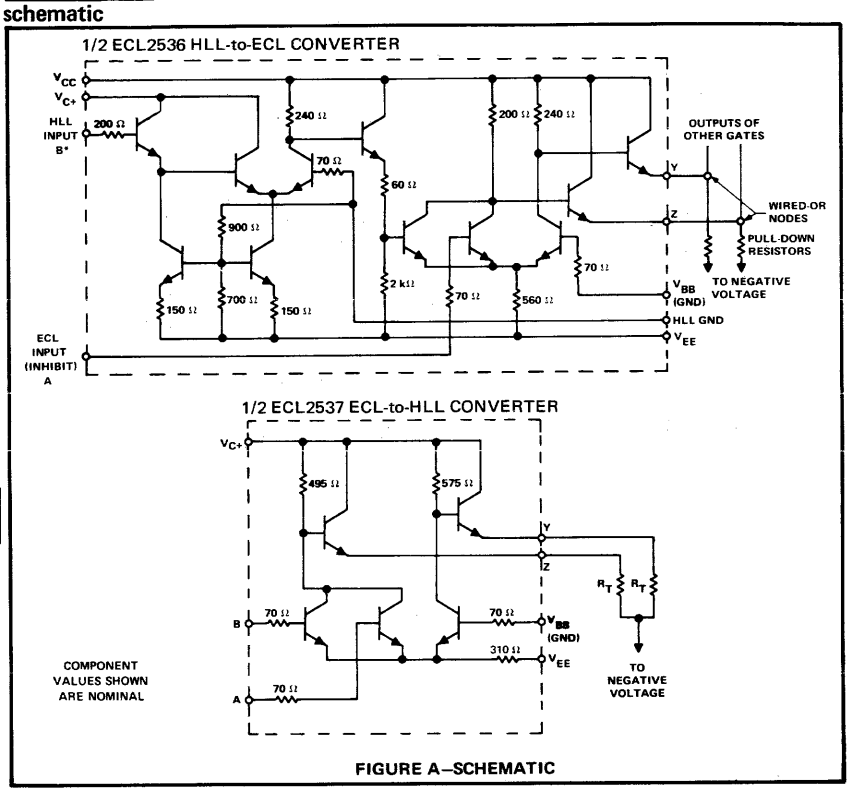


FIGURE A—SCHEMATIC

logic

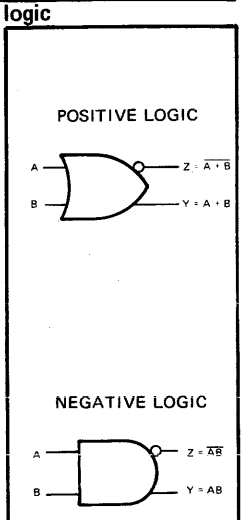
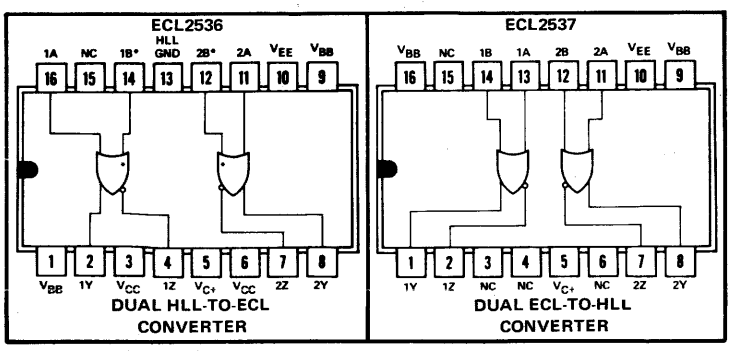


FIGURE B
LOGIC DIAGRAMS

Positive logic OR/NOR functions or negative logic AND/NAND functions are provided at the Y (OR) and Z (NOR) outputs, as shown.

Emitter-follower outputs require an external pull-down resistor. For ECL2536 only, the wired-OR function can be obtained by connecting emitter-follower outputs of separate gates together. Only one pull-down resistor is required for each wired-OR node. ECL2537 outputs require pull-down resistors (R_T in schematic above) to sink the low-level input current of the driven HLL inputs. ECL2537 cannot have wired-OR connections.

logic



NC—No internal connection

MODULE	POSITIVE LOGIC		NEGATIVE LOGIC	
	Y (OR)	Z (NOR)	Y (AND)	Z (NAND)
ECL2536	A+B*	$\overline{A+B^*}$	AB*	$\overline{AB^*}$
ECL2537	A+B	$\overline{A+B}$	AB	$\overline{AB}$

B* is the HLL input of the ECL2536.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

truth tables

(For HLL inputs, H = high-level positive voltage, L = low-level positive voltage. For ECL inputs, H = positive voltage, L = negative voltage)

ECL2536

INPUTS		OUTPUTS	
A	B*	Y (OR)	Z (NOR)
L	L	L	H
L	H	H	L
H	L	H	L
H	H	H	L

B* is the HLL input of the ECL2536.

ECL2537

INPUTS		OUTPUTS	
A	B	Y (OR)	Z (NOR)
L	L	L	H
L	H	H	L
H	L	H	L
H	H	H	L

absolute maximum ratings (see note 1)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Temperature range with supply and bias voltages applied . . . . . −40°C to 100°C

4

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C to 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{C+}		6 V	7 V	
V_{CC} (ECL2536)		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each ECL input (ECL2536 and ECL2537)	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Each HLL input (ECL2536 only)		−1.25 V	−1.5 V	
		4.5 V	5 V	
Output Y (ECL2536)	A input low, B* input high			−40 mA
Output Y (ECL2537)	All inputs high			−40 mA
Output Z	All inputs low			−40 mA

recommended operating conditions

Supply voltage V_{C+} . . . . . 4.8 V ± 1%
Supply voltage V_{CC} (ECL2536 only) . . . . . 1.32 V ± 2%
Supply voltage V_{EE} . . . . . −3.2 V ± 2%
Reference voltage V_{BB} . . . . . 0 V (GND)
Reverse bias on unused ECL inputs . . . . . −1 V ± 0.5 V
Low-level bias on unused HLL inputs . . . . . 0 V (GND)
Normalized d-c fan-out: ECL2536 . . . . . 0 to 35
ECL2537 . . . . . 0 to 8 loads, each requiring 1.6 mA
Load on each output: ECL2536 . . . . . characterized at 270 Ω to V_{EE}, 50 Ω to GND
ECL2537 . . . . . characterized at 300 Ω to V_{EE}
Operating free-air temperature range . . . . . 0°C to 75°C

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

ECL2536 electrical characteristics using HLL inputs

PARAMETER		TEST CONDITIONS*						MIN	TYP	MAX	UNIT
		TEST FIGURE	TERMINALS (SEE NOTE 4)		INPUT CONDITIONS		T_A	(SEE NOTE 5)			
			INPUTS	OUTPUTS Y	OUTPUTS Z	INPUT UNDER TEST, V_I	HLL INPUT OF OTHER GATE					
V_{IH}	High-level input voltage		14					0°C	1.05		4.5	V
			12					25°C	1.05		4.5	
								75°C	1.05		4.5	
V_{IL}	Low-level input voltage		14					0°C	−1		0.65	V
			12					25°C	−1		0.65	
								75°C	−1		0.65	
$V_{OH(Y)}$	High-level output voltage at OR output	2	14	2		1.2 V	0 V	0°C	315	410		mV
			12	8				25°C	350	450	525	
								75°C		520	600	
$V_{OL(Y)}$	Low-level output voltage at OR output	2	14	2		0.5 V	0 V	0°C	−505	−470		mV
			12	8				25°C	−505	−450	−350	
								75°C		−410	−310	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	14		4	0.5 V	0 V	0°C	315	410		mV
			12		7			25°C	350	450	525	
								75°C		520	600	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	14		4	1.2 V	0 V	0°C	−505	−470		mV
			12		7			25°C	−505	−450	−350	
								75°C		−410	−315	
$V_{OH(Y)}$	High-level output voltage at OR output	2	14	2		1.05 V	0 V	0°C	315	410		mV
			12	8				25°C	350	450	525	
								75°C		520	600	
$V_{OL(Y)}$	Low-level output voltage at OR output	2	14	2		0.65 V	0 V	0°C	−505	−470		mV
			12	8				25°C	−505	−450	−350	
								75°C		−410	−310	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	14		4	0.65 V	0 V	0°C	315	410		mV
			12		7			25°C	350	450	525	
								75°C		520	600	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	14		4	1.05 V	0 V	0°C	−505	−470		mV
			12		7			25°C	−505	−450	−350	
								75°C		−410	−315	
I_{IH}	High-level input current	3	14			2.8 V	0 V	0°C			220	μA
			12					25°C			200	
								75°C			170	
I_{IL}	Low-level input current	3	12, 14			0 V	0 V	0°C			220	μA
								25°C			200	
								75°C			170	
I_{C+}	Supply current from V_{C+}	4				Both HLL inputs at 2.4 V		25°C	10		17.5	mA
I_{CC}	Supply current from V_{CC}	4				Both HLL inputs at 2.4 V		25°C	9		16	mA
I_{EE}	Supply current from V_{EE}	4				Both HLL inputs at 2.4 V		25°C	−22		−38	mA
C_{in}	Input capacitance (see Note 6)		14									pF
			12					25°C		2		
z_{out}	Output impedance (see Note 7)			2	4			25°C		5		Ω
				8	7							

*ECL inputs (pins 11 and 16) biased to −0.5 V, V_{BB} (pins 1 and 9) = GND, V_{CC} (pins 3 and 6) = 1.32 V ± 1%, V_{EE} (pin 10) = −3.2 V ±1%, V_{C+} (pin 5) = 4.8 V ± 1%.

NOTES: 4. Each gate is tested separately unless otherwise noted. See referenced test figure for output terminations.
5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.
6. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. $C_{in} = Q/V$.
7. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

ECL2536 electrical characteristics using ECL inputs

PARAMETER		TEST CONDITIONS*						MIN	TYP	MAX	UNIT
		TEST FIGURE	TERMINALS (SEE NOTE 4)		INPUT CONDITIONS		T_A	(SEE NOTE 5)			
			INPUTS	OUTPUTS Y Z	INPUT UNDER TEST, V_I	ECL INPUT OF OTHER GATE					
V_{IH}	High-level input voltage		16				0°C	150		720	mV
			11				25°C	150		720	
							75°C	150		720	
V_{IL}	Low-level input voltage		16				0°C	−1500		−150	mV
			11				25°C	−1500		−150	
							75°C	−1500		−150	
$V_{OH(Y)}$	High-level output voltage at OR output	2	16	2	0.2 V	−0.5 V	0°C	315	410		mV
			11	8			25°C	350	450	525	
							75°C		520	600	
$V_{OL(Y)}$	Low-level output voltage at OR output	2	16	2	−0.2 V	−0.5 V	0°C	−505	−470		mV
			11	8			25°C	−505	−450	−350	
							75°C		−410	−310	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	16	4	−0.2 V	−0.5 V	0°C	315	410		mV
			11	7			25°C	350	450	525	
							75°C		520	600	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	16	4	0.2 V	−0.5 V	0°C		−410		mV
			11	7			25°C		−390	−310	
							75°C		−350	−280	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	16	4	0.4 V	−0.5 V	0°C	−505	−470		mV
			11	7			25°C	−505	−450		
							75°C		−410	−315	
$V_{OH(Y)}$	High-level output voltage at OR output	2	11	8	0.15 V	−0.5 V	0°C	290			mV
							25°C	325			
							75°C				
$V_{OL(Y)}$	Low-level output voltage at OR output	2	11	8	−0.15 V	−0.5 V	0°C				mV
							25°C			−325	
							75°C			−290	
I_{IH}	High-level input current	3	16		0.5 V	−0.5 V	0°C			255	μA
			11				25°C			235	
							75°C			200	
I_{IL}	Low-level input current (both ECL inputs)	5	11, 16		Both ECL inputs at −3.2 V		0°C			−0.5	μA
							25°C			−0.5	
							75°C			−0.5	
I_{C+}	Supply current from V_{C+}	4			Both ECL inputs at −0.5 V		25°C	5		8.5	mA
I_{CC}	Supply current from V_{CC}	4			Both ECL inputs at −0.5 V		25°C	13		22	mA
I_{EE}	Supply current from V_{EE}	4			Both ECL inputs at −0.5 V		25°C	−20		−35	mA
C_{in}	Input capacitance (see Note 6)		16				25°C		5		pF
			11								
z_{out}	Output impedance (see Note 7)			2 4			25°C		5		Ω
				8 7							

*HLL inputs (pins 12 and 14) grounded, V_{BB} (pins 1 and 9) = GND, V_{CC} (pins 3 and 6) = 1.32 V ± 1%, V_{EE} (pin 10) = −3.2 V ± 1%, V_{C+} (pin 5) = 4.8 V ± 1%.

NOTES: 4. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination.
5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.
6. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. $C_{in} = Q/V$.
7. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

ECL2537 electrical characteristics

PARAMETER (SEE NOTE 8)	TEST CONDITIONS*								MIN	TYP	MAX	UNIT
	TEST FIGURE	TERMINALS (SEE NOTE 4)		INPUT CONDITIONS			T_A	(SEE NOTE 5)			
		INPUTS	OUTPUTS Y Z	INPUT UNDER TEST, V_I	OTHER INPUT OF SAME GATE	INPUTS OF OTHER GATE					
V_{IH}		13, 14					0°C	150		720	mV
		11, 12					25°C	150		720	
							75°C	150		720	
V_{IL}		13, 14					0°C	−1500		−150	mV
		11, 12					25°C	−1500		−150	
							75°C	−1500		−150	
$V_{OH(Y)}$	6	13, 14	1	0.2 V	−0.5 V	−0.5 V	0°C	3	3.4		V
		11, 12	8				25°C	3.2	3.6		
							75°C		3.8		
$V_{OL(Y)}$	6	13, 14	1	−0.2 V	−0.5 V	−0.5 V	0°C	−0.8	−0.35		V
		11, 12	8				25°C	−0.7	−0.25	0.2	
							75°C		−0.15	0.3	
$V_{OH(Z)}$	6	13, 14	2	−0.2 V	−0.5 V	−0.5 V	0°C	3	3.4		V
		11, 12	7				25°C	3.2	3.6		
							75°C		3.8		
$V_{OL(Z)}$	6	13, 14	2	0.2 V	−0.5 V	−0.5 V	0°C	−0.7	−0.2		V
		11, 12	7				25°C	−0.6	−0.1	0.2	
							75°C		0.0	0.3	
$V_{OL(Z)}$	6	13, 14	2	0.4 V	−0.5 V	−0.5 V	0°C	−1	−0.35		V
		11, 12	7				25°C	−0.9	−0.25	0.2	
							75°C		−0.15	0.3	
$V_{OH(Y)}$	6	13, 14	1	0.15 V	−0.5 V	−0.5 V	0°C	2.9			V
		11, 12	8				25°C	3.1			
							75°C				
$V_{OL(Y)}$	6	13, 14	1	−0.15 V	−0.5 V	−0.5 V	0°C				V
		11, 12	8				25°C			0.3	
							75°C			0.4	
I_{IH}	7	13, 14		0.5 V	−0.5 V	−0.5 V	0°C			510	μA
		11, 12					25°C			470	
							75°C			400	
I_{IL} (all inputs)	8	11, 12, 13, 14		Both inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
							25°C			−0.5	
							75°C			−0.5	
I_{C+}	9			All inputs at −0.5 V			25°C	8		17	mA
I_{EE}	9			All inputs at −0.5 V			25°C	−8		−17	mA
C_{in} (see Note 6)		13, 14					25°C		5		pF
		11, 12									
z_{out} (see Note 7)			1 2				25°C		10		Ω
			8 7								

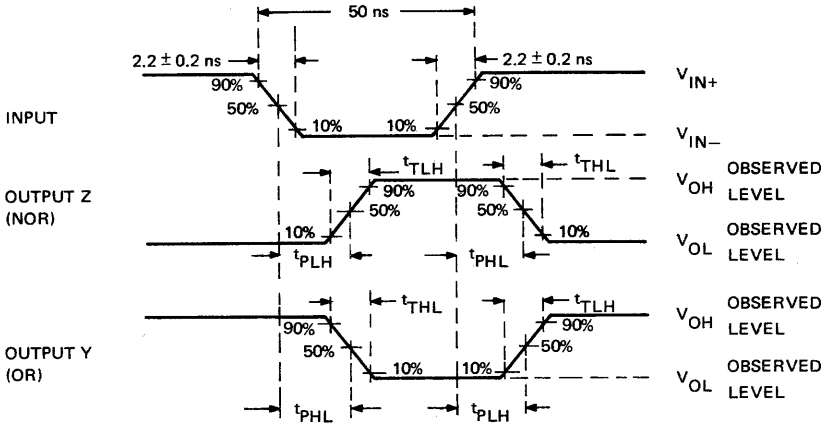
*V_{BB} (pins 9 and 16) = GND, V_{C+} (pin 5) = 4.8 V ± 1%, V_{EE} (pin 10) = −3.2 V ± 1%.

NOTES: 4. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination.
5. The algebraic convention where the most positive limit is designated at maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.
6. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V.
7. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.
8. See pages 4 or 5 for defining term associated with each symbol.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operating characteristics at specified free-air temperature (see figure 1)

TERMINALS TO BE TESTED (SEE NOTES 9, 10, and 11)				C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns									t_{THL} and/or t_{TLH} TRANSITION TIMES—ns								
					$T_A = 0°C$			$T_A = 25°C$			$T_A = 75°C$			$T_A = 0°C$			$T_A = 25°C$			$T_A = 75°C$		
INPUT	OUTPUT	INPUT	OUTPUT	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2536 using HLL inputs (see figure 10)																						
14	2, 4	12	8, 7	4		4.0			2.8	3.9	5.5		4.0		3.9			2.5	4.0	6.5		4.2
				50		5.0			3.7	5.0	6.5		5.2		4.3			2.5	4.4	7		4.3
ECL2536 using ECL inputs (see figure 11)																						
16	2, 4	11	8, 7	4		2.5			1.3	2.4	3.7		2.5		4.1			2.5	4.0	6.5		4.1
				50		3.4			2.2	3.5	4.8		3.4		4.4			2.5	4.4	7		4.3
ECL2537 (see figure 12)																						
13 14	1, 2	11 12	8, 7	15		3.4			2.2	3.5	5		3.6		3.7			2.2	3.7	6.5		3.8



VOLTAGE WAVEFORMS

MODULE	V_{IN+} (V)	V_{IN-} (V)
ECL2536 (HLL)	1.40 ± 0.05	0 ± 0.05
ECL2536 (ECL)	0.40 ± 0.02	−0.50 ± 0.02
ECL2537	0.40 ± 0.05	−0.50 ± 0.05

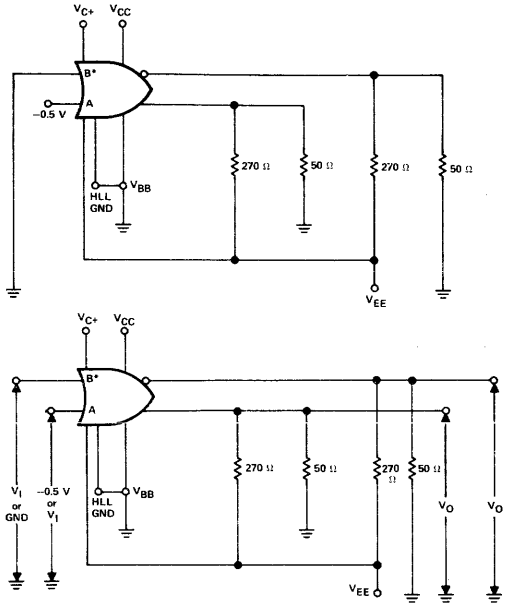
FIGURE 1—PROPAGATION DELAY AND TRANSITION TIMES

NOTES: 9. Each gate is tested separately.

10. The input pulse is measured as it is applied sequentially to each input of the gate under test and a waveform measurement is made at each of the outputs of that gate.

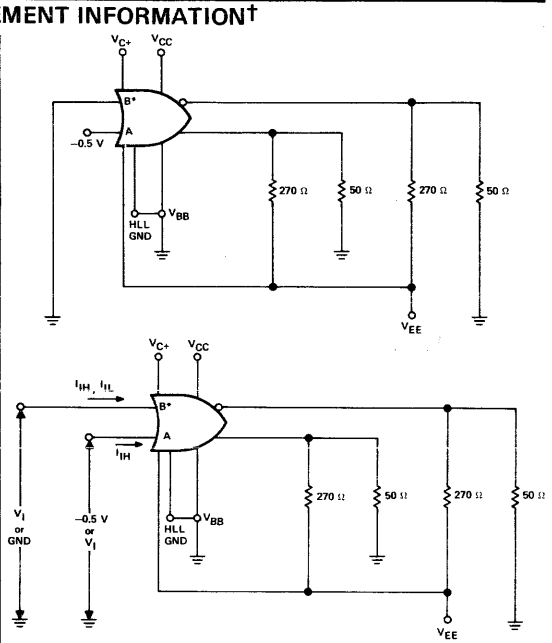
11. Bias voltages and loads for the gate under test are shown in Figures 10 through 12. Unused gates have inputs biased as shown in Figure 2 for the ECL2536 or Figure 6 for the ECL2537, outputs under load, and power applied.

PARAMETER MEASUREMENT INFORMATION†



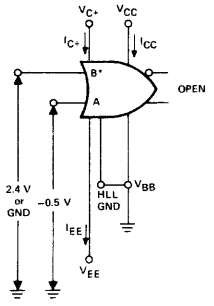
A. V_I is first applied to each HLL input separately (other HLL input grounded) with both ECL inputs at −0.5 V; then V_I is applied to each ECL input separately (other ECL input at −0.5 V) with both HLL inputs at ground.
B. Each output is tested separately.

FIGURE 2–V_{OH} AND V_{OL}



V_I is first applied to each HLL input separately (other HLL input grounded) with both ECL inputs at −0.5 V; then V_I is applied to each ECL input separately (other ECL input at −0.5 V) with both HLL inputs at ground.

FIGURE 3–I_{IH} AND I_{IL}



A. The supply currents are measured with both the HLL inputs first at 2.4 V, then at GND.
B. Both gates are tested simultaneously. I_{CC} is the total current into the two V_{CC} terminals.

FIGURE 4–I_{C+}, I_{CC}, AND I_{EE}

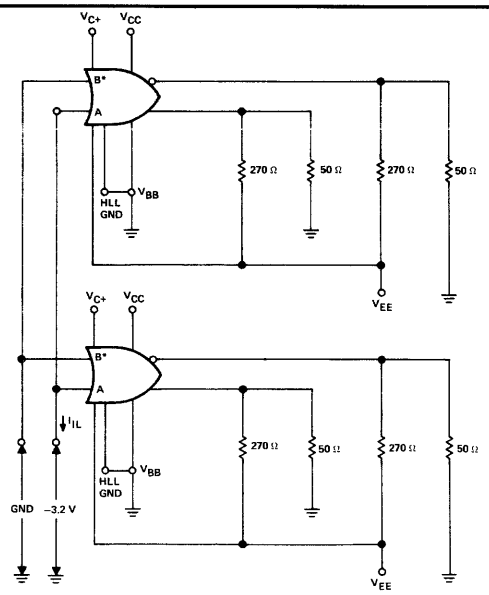
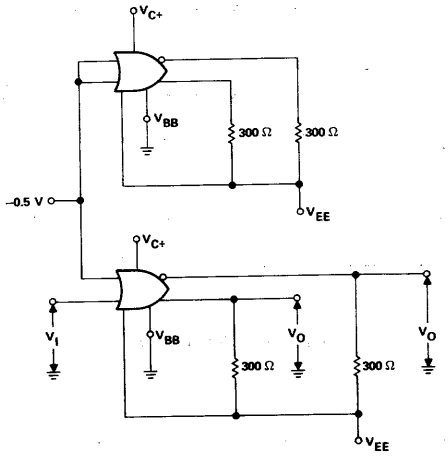


FIGURE 5–I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

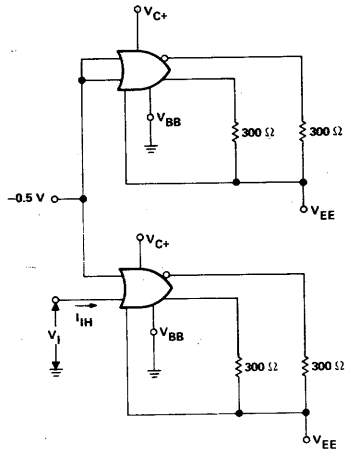
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION†



A. V_I is applied to each input separately.
B. Each output is tested separately.

FIGURE 6—V_{OH} AND V_{OL}



Each input is tested separately.

FIGURE 7—I_{IH}

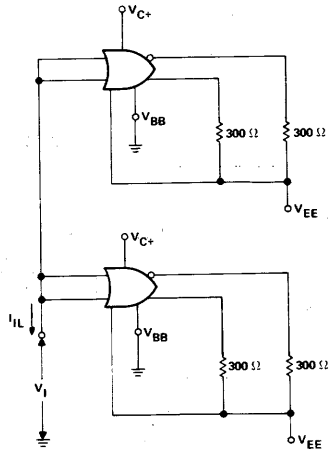
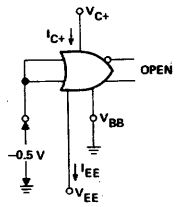


FIGURE 8—I_{IL}



Both gates are tested simultaneously.

FIGURE 9—I_{C+} OR I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

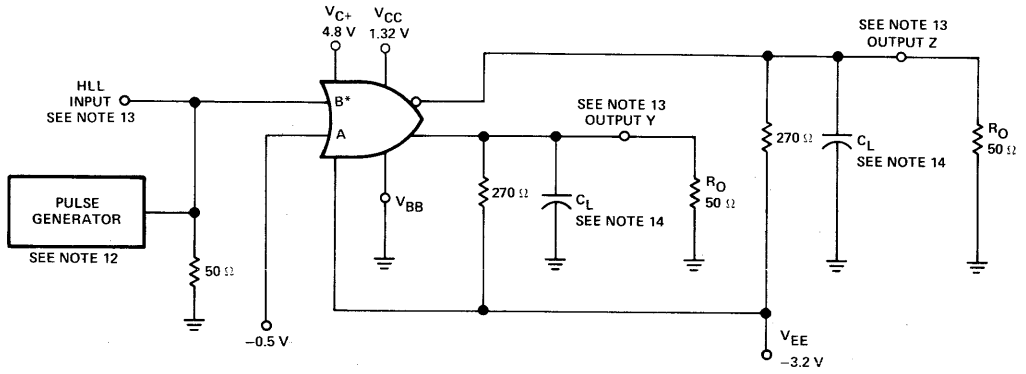


FIGURE 10–ECL2536 PROPAGATION DELAY AND TRANSITION TIMES (HLL INPUT)

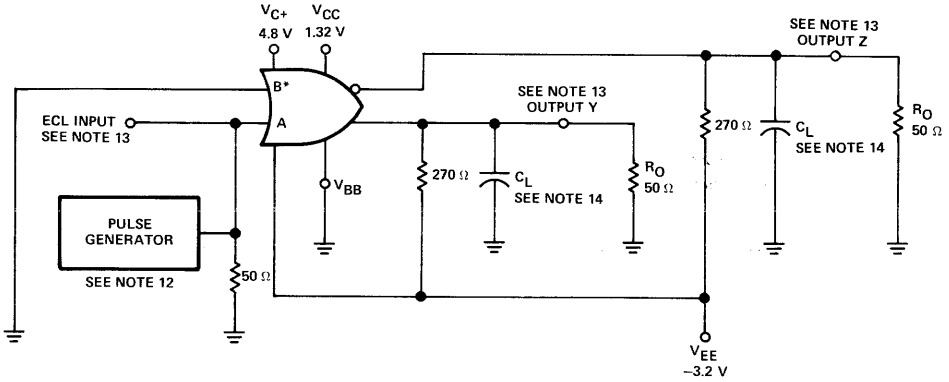


FIGURE 11–ECL2536 PROPAGATION DELAY AND TRANSITION TIMES (ECL INPUT)

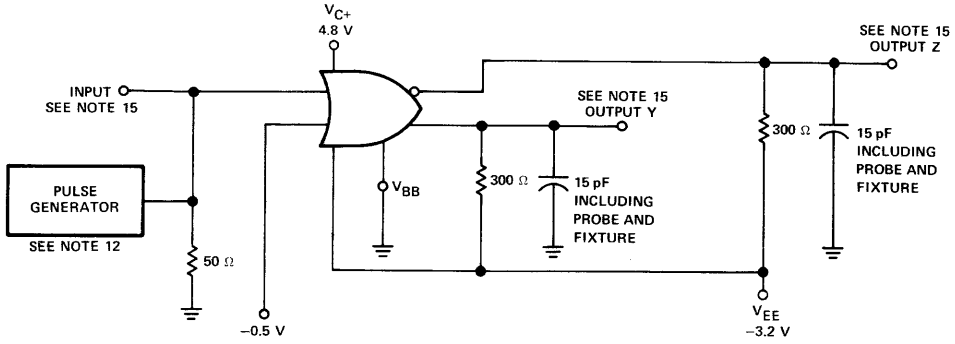


FIGURE 12–ECL2537 PROPAGATION DELAY AND TRANSITION TIMES

NOTES: 12. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz. See waveform details in Figure 1.
13. The waveforms for ECL2536 are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistors designated R_O are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.
14. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.
15. The waveforms for ECL2537 are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. A high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF is used.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

GENERAL APPLICATION INFORMATION

ECL2536

input conditions

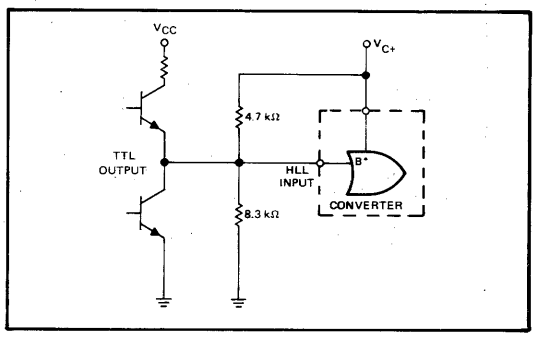
The ECL2536 converts high-level-logic inputs to ECL2500-logic-level outputs.

A control INHIBIT/ENABLE ECL input is provided to lock out data presented at the HLL input. A high-level (H) input voltage inhibits the converter outputs in a stable state such that signals on the HLL input are not transmitted through the converter. A low-level (L) input voltage enables the converter and the output levels are determined by the logic level of the HLL input.

The output feeding the HLL input should have an H level $\geq$ 1.2 V and an L level $\leq$ 0.5 V in order to maintain at least a 150-mV noise margin.

driving by TTL

The HLL input requires up to 220 μA of current to be supplied with both H-level and L-level voltage inputs. TTL outputs are designed to sink current in the low state, not to supply current. To assure reliable performance with all types of TTL circuits, it is recommended that a resistor divider be placed at the HLL input external to the package. The divider has 4.7 kΩ from the HLL input to V_{C+} and 8.3 kΩ to ground, as shown.



ECL output loading

General loading for fan-out from the ECL outputs may be divided into two classes:

CLASS I **Short-Line or Cluster Loading**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II **Long-Line or Distributive Loading**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

ECL2537

The ECL2537 converts ECL2500-logic-level inputs to high-level-logic outputs.

An external pull-down resistor to a negative voltage must be provided on the HLL output terminals. The size of the resistor is determined by the current it must sink in order to maintain the correct low-level voltage with the DTL or TTL fan-out being driven.

Characterization is with a pull-down resistor of 300 Ω to -3.2 V which represents a fan-out of five Texas Instruments Series 54/74 TTL logic gates.

No wired-OR connection is allowed on the HLL outputs because an emitter-follower junction breakdown may occur if one converter output is high and this forces another output to be high which would otherwise be low.

The V_{C+} power supply must be held at 4.8 V $\pm$ 1%. Otherwise, the output voltage specifications for maximum V_{OL} or minimum V_{OH} may be exceeded.

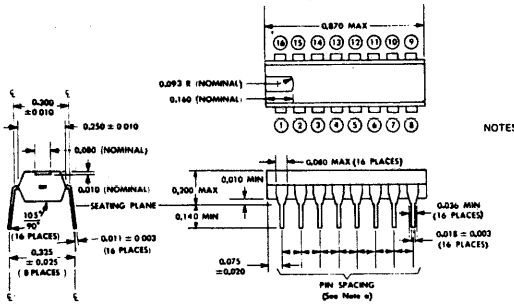
TYPES ECL2536, ECL2537
HLL-TO-ECL AND ECL-TO-HLL CONVERTERS

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

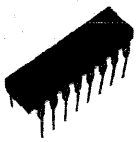
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



4

terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams on page 2.
Outputs are denoted Y or Z. Inputs are denoted A, B, or B*.
Respective inputs and outputs are identified by a gate number preceding the pin symbol.
Power is supplied via the V_{C+}, V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.
NC indicates no internal connection.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2536	V_{BB}	1Y	V_{CC}	1Z	V_{C+}	V_{CC}	2Z	2Y	V_{BB}	V_{EE}	2A	2B*	HLL GND	1B*	NC	1A
ECL2537	1Y	1Z	NC	NC	V_{C+}	NC	2Z	2Y	V_{BB}	V_{EE}	2A	2B	1A	1B	NC	V_{BB}

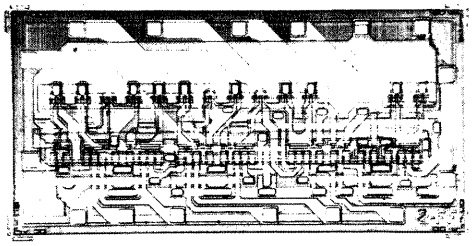
*HLL input

Multiple V_{CC} terminals have been supplied to reduce cross-talk noise. Multiple V_{BB} terminals are also provided. All V_{BB} and V_{CC} terminals should be connected even if all gates in the module are not used.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES ECL2540 THRU ECL2542
EMITTER-COUPLED-LOGIC BISTABLE MODULES

ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) BISTABLE MODULES FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS



description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 70°C.

The ECL2500 family includes:

- Basic Gate Modules
- Multifunction Gate Modules
- **Bistable Modules**
- Arithmetic Modules
- Interface Modules
- Memory Module

family features

- High speed . . . typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ±225 mV typical at 25°C

This data sheet covers the bistable modules.
Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series bistable modules

The ECL2500 series bistable modules are summarized in the table below. These modules contain the ECL circuits shown in the schematics of Figures A, B, and C on pages 6 and 7. Logic diagrams of ECL2540 through ECL2542 are shown on page 4.

SUMMARY OF BISTABLE MODULES

MODULE	GATES PER MODULE	LATCHES PER MODULE	OUTPUTS PER BISTABLE CIRCUIT	
			Q (LATCH)	$\overline{Q}$ (LATCH COMPLEMENT)
ECL2540	4	2	1	1
ECL2541	9	2	1	2
ECL2542	13	2		1

APPLICATION INFORMATION

general

The bistable modules specified in this data sheet contain dual latches. Each half of the ECL2540 is a latch with a separate data input. Two clock inputs, C and C′, feed both latches. Q and $\overline{Q}$ outputs are provided from each latch. Each half of the ECL2541 is a latch with additional circuitry which provides a data input and a gate input to control the input data. Common clock, set, and reset inputs are included. One Q and two $\overline{Q}$ outputs are provided for each latch. Each half of the ECL2542 is a latch with additional circuitry which provides two data inputs each with a gate input to control the input data. Common clock, set, and reset inputs serve both latches. Only $\overline{Q}$ outputs are provided.

Each latch has the possibility to operate in the following modes:

Register – The mode in which the data input controls the state of the latch. Q is high when data is high.

Storage – The mode in which the latch stores data received during the register mode. Input data is locked out from changing the latch state.

Set – The mode whereby Q is set high (or $\overline{Q}$ low) which is normally done when the clock is high.

Reset – The mode whereby Q is set low (or $\overline{Q}$ high) which is normally done when the clock is high (low for ECL2540).

4

The ECL2541 and ECL2542 have the register mode subdivided:

Register Mode/Clock Control – The mode whereby the gate input is low, allowing the data to set the latch when the clock goes low.

Register Mode/Gate Control – The mode whereby the clock input is low, allowing the data to set the latch when the gate is low.

Each Q and $\overline{Q}$ output must be terminated in a pull-down resistor.

The Q terminal of the ECL2541 must have a termination resistor (in addition to the pull-down resistor) on the output at all times (whether the output is used for fan-out or not), because internal feedback occurs from this point.

For full-temperature-range operation of all devices, data must be present before the clock pulse and the minimum width of the clock pulse is 4.5 ns. For the ECL2541 and ECL2542, the data pulse must extend beyond the clock pulse to allow for the delay associated with the clock-buffering gate.

For the ECL2540, latching occurs on either the leading or trailing edge of the C or C′ pulse. For the ECL2541 and ECL2542, latching occurs on the leading edge of the clock pulse.

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

General loading for fan-out may be divided into two classes:

CLASS I **Short-Line or Cluster Loading.**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II **Long-Line or Distributive Loading.**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

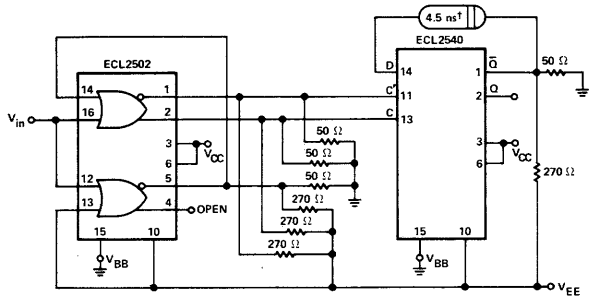
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

APPLICATION INFORMATION

ECL2540

The ECL2540 requires two clock inputs. Faulty operation occurs if the C′ input lags behind C by more than 0.5 ns. The interval between the transition of the two clocks is referred to as skew. C′ can be skewed ahead of C by as much as 1.5 ns.

The ECL2540 can be used as a toggle as shown in Figure 1. However, the delay from $\overline{Q}$ to D must be greater than the clock pulse width. Thus, when pulse widths are very long, this becomes impractical unless a technique such as that shown in Figure 1 is used. This technique uses two gates of an ECL2502 as a pulse-shaping network to allow operation of a toggle from 100 megacycles per second down to cycles per second.



†Delay between $\overline{Q}$ and D must be greater than 4.5 ns based on the propagation delay characteristics of the ECL2502 and its feedback loop.

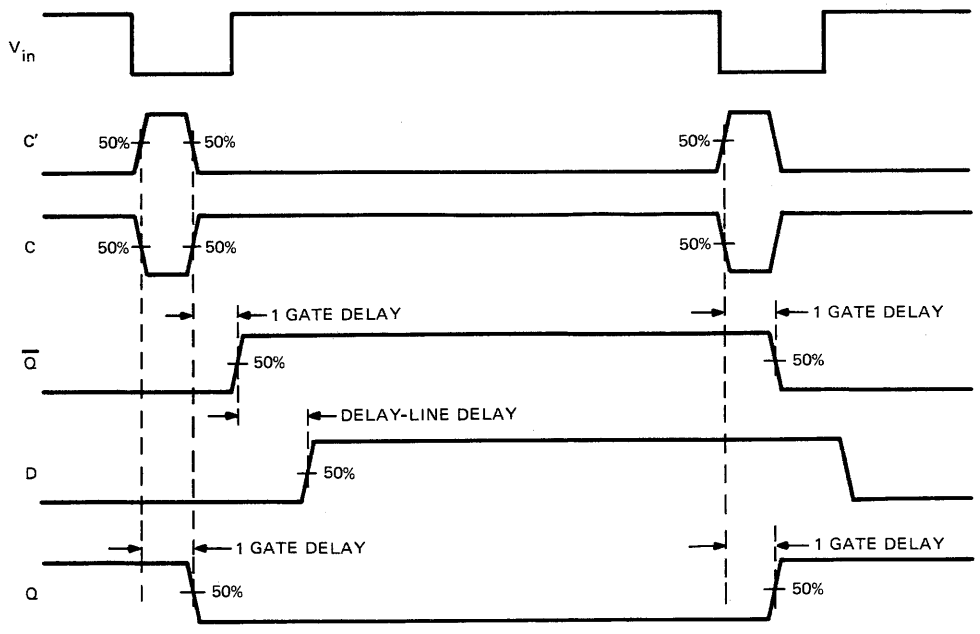
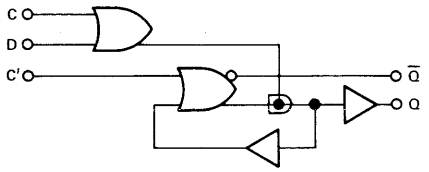


FIGURE 1–ECL2540 USED AS A TOGGLE (WITHOUT SKEW)

TYPES ECL2540 THRU ECL2542
EMITTER-COUPLED-LOGIC BISTABLE MODULES

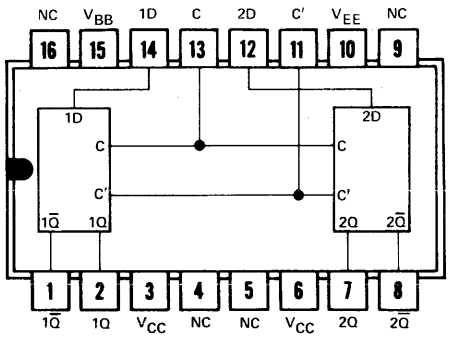
logic†

ECL2540



$Q_{n+1} = (C+D)(Q_n+C')$

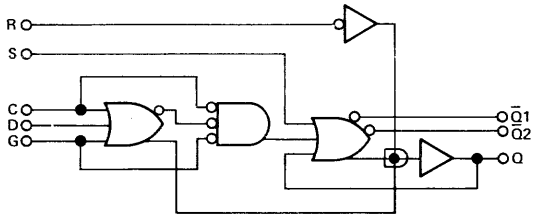
$\bar{Q}_{n+1} = (\bar{C}\bar{D}+\bar{Q}_n)\bar{C}'$



NC—No internal connection

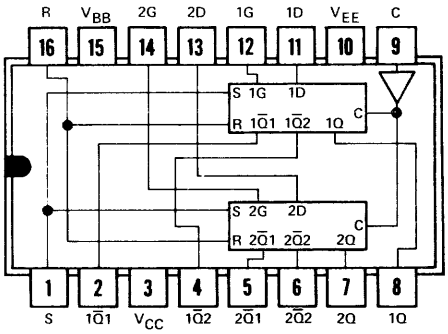
4

ECL2541

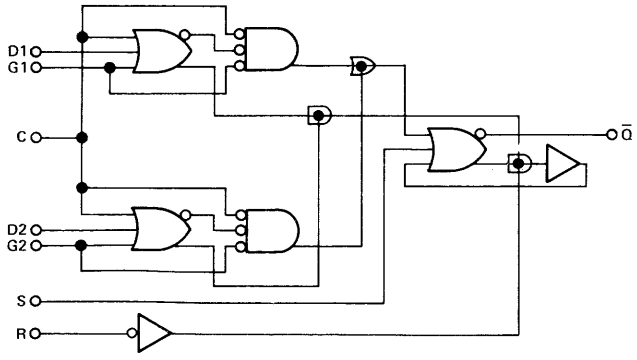


$Q_{n+1} = \bar{R}[(C+D+G)(Q_n+S)+\bar{C}D\bar{G}]$

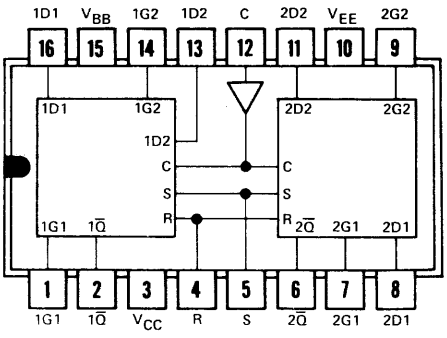
$\bar{Q}_{n+1} = \bar{S}(C+\bar{D}+G)(\bar{Q}_n+R+\bar{C}\bar{D}\bar{G})$



ECL2542



$\bar{Q}_{n+1} = \bar{S}[C+(\bar{D}1+G1)(\bar{D}2+G2)]\,[\bar{Q}_n+R+\bar{C}(\bar{D}1\bar{G}1+\bar{D}2\bar{G}2)]$



†One half of each bistable module is shown in the logic diagrams.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2540

MODE	INPUTS			OUTPUTS	
	CLOCK		DATA	LATCH	LATCH COMPLEMENT
	C	C′	D	Q_{n+1}	$\overline{Q}_{n+1}$
Register	L	H	H	H	L
	L	H	L	L	(L)†
Clock-controlled storage	H	L	X	Q_n	$\overline{Q}_n$
Set	H	H	X	H	L
Reset	L	L	L	L	H
Forbidden (see Note 1)	L	L	H	Q_n	$\overline{Q}_n$

ECL2541

MODE	INPUTS					OUTPUTS	
	SET	RESET	CLOCK	GATE	DATA	LATCH	LATCH COMPLEMENT
	S	R	C	G	D	Q_{n+1}	$\overline{Q}_{n+1}$
Register	L	L	L	L	H	H	L
	L	L	L	L	L	L	H
Clock-controlled storage	L	L	H	X	X	Q_n	$\overline{Q}_n$
Gate-controlled storage	L	L	X	H	X	Q_n	$\overline{Q}_n$
Set	H	L	H	X	X	H	L
	H	L	X	H	X	H	L
Reset	L	H	H	X	X	L	H
	L	H	X	H	X	L	H
Forbidden	H	L	L	L	H	H	L
	H	L	L	L	L	L	L
	L	H	L	L	H	L	L
	L	H	L	L	L	L	H
	H	H	X	X	X	L	L

ECL2542

MODE	INPUTS							OUTPUT
	SET	RESET	CLOCK	GATE		DATA		LATCH COMPLEMENT
	S	R	C	G1	G2	D1	D2	$\overline{Q}_{n+1}$
Register	L	L	L	H	L	X	D2	$\overline{D2}$
	L	L	L	L	H	D1	X	$\overline{D1}$
	L	L	L	L	L	D1	D2	$\overline{D1 + D2}$
Clock-controlled storage	L	L	H	X	X	X	X	$\overline{Q}_n$
Gate-controlled storage	L	L	X	H	H	X	X	$\overline{Q}_n$
Set	H	L	H	X	X	X	X	L
	H	L	X	H	H	X	X	L
Reset	L	H	H	X	X	X	X	H
	L	H	X	H	H	X	X	H
Forbidden	H	L	L	L	X	X	X	See Note 2
	H	L	L	X	L	X	X	
	L	H	L	L	X	X	X	
	L	H	L	X	L	X	X	
	H	H	X	X	X	X	X	

†$\overline{Q}$ is made low by C′ being high. When C′ returns to its normal state (low) following the clock pulse, $\overline{Q}$ goes high (the complement of data)

NOTES: 1. This condition is data-controlled storage, whereas only clock-controlled storage is desired in the ECL2540. Hence, this condition is placed in the forbidden category.
2. The forbidden input combinations for ECL2542 may produce pseudo-stable output states which do not persist when a storage mode is subsequently selected or may produce outputs not in harmony with the normally used input patterns.

schematics

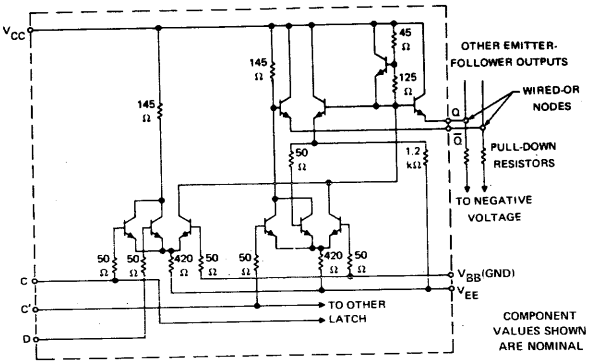


FIGURE A–SCHEMATIC OF HALF OF ECL2540

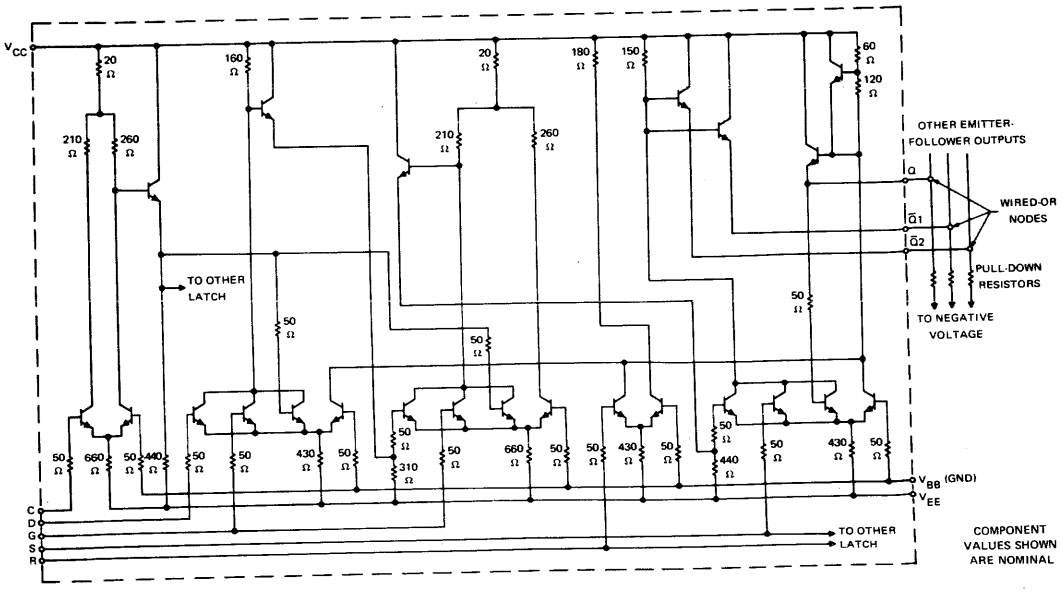


FIGURE B–SCHEMATIC OF HALF OF ECL2541

Emitter-follower outputs require an external pull-down resistor. The wired-OR function can be obtained by connecting the emitter-follower outputs of a bistable module to the emitter-follower outputs of other gates or other bistable modules. Only one pull-down resistor is required for each wire-OR node.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

schematic

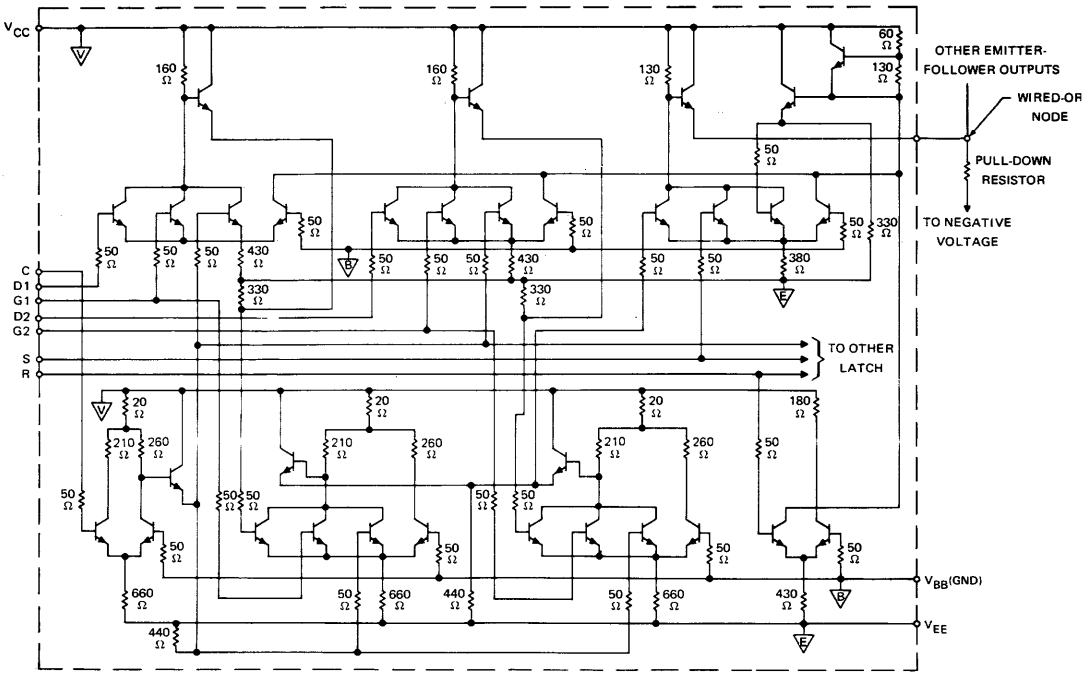


FIGURE C–SCHEMATIC OF HALF OF ECL2542

COMPONENT VALUES SHOWN ARE NOMINAL

▽ –V_{CC} bus
▽ –V_{BB} bus
▽ –V_{EE} bus (substrate)

4

absolute maximum ratings (see note 3)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Free-air temperature range with supply and bias voltages applied . . . . . −40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 4 AND 5)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Output Q	At high level			−40 mA
Output $\overline{Q}$	At high level			−40 mA

4

recommended operating conditions

Supply voltage V_{CC} . . . . . 1.32 V ± 2%
Supply voltage V_{EE} . . . . . −3.2 V ± 2%
Reference voltage V_{BB} . . . . . 0 V (GND)
Reverse bias on unused inputs . . . . . −1 V ± 0.5 V
Normalized d-c fan-out . . . . . 0 to 35
Load on each output . . . . . characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range . . . . . 0°C to 75°C

NOTES: 3. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
4. Maximum terminal conditions must be considered as mutually exclusive.
5. All voltages are referenced to V_{BB}, which is at GND.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

ECL2540 electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS*							T_A	MIN	TYP	MAX (SEE NOTE 6)	UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE I)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS 0.5 V	OTHER INPUT TERMINALS −0.5 V	OUTPUT TERMINAL Q	OUTPUT TERMINAL $\bar{Q}$				
V_{IH}	High-level input voltage									0°C 25°C 75°C	150 150 150		720 720 720	mV
V_{IL}	Low-level input voltage									0°C 25°C 75°C	−1500 −1500 −1500		−150 −150 −150	mV
$V_{OH(Q)}$	High-level output voltage at Q output, register mode	4	X	0.2 V	14	11	13	2		0°C 25°C	280 315			mV
					12	11	13	7		75°C				
$V_{OL(Q)}$	Low-level output voltage at Q output, register mode	4	X	−0.2 V	14	11	13	2		0°C 25°C				mV
					12	11	13	7		75°C			−330 −210	
$V_{OH(Q)}$	High-level output voltage at Q output, storage mode	4	S	0.2 V	13		11, 14	2		0°C 25°C	280 315	365 400		mV
					13		11, 12	7		75°C		470	500 580	
$V_{OL(Q)}$	Low-level output voltage at Q output, storage mode	4	R	−0.2 V	11	13, 14		2		0°C 25°C	−505 −480	−440 −400		mV
					11	13, 12		7		75°C		−280	−330 −210	
$V_{OH(\bar{Q})}$	High-level output voltage at $\bar{Q}$ output, storage mode	4	R	−0.2 V	11	13, 14			1	0°C 25°C	280 315	365 400		mV
					11	13, 12			8	75°C		470	500 580	
$V_{OL(\bar{Q})}$	Low-level output voltage at $\bar{Q}$ output, storage mode	4	S	0.2 V	13		11, 14		1	0°C 25°C	−505 −490	−440 −425		mV
					13		11, 12		8	75°C		−390	−350 −315	
$V_{OH(Q)}$	High-level output voltage at Q output, set mode	4	R	0.2 V	11, 13		14	2		0°C 25°C	280 315			mV
					11, 13		12	7		75°C				
$V_{OL(Q)}$	Low-level output voltage at Q output, reset mode	4	S	−0.2 V	11, 13		14	2		0°C 25°C				mV
					11, 13		12	7		75°C			−330 −210	
I_{IH}	High-level input current	5	X	0.5 V	14		11, 12, 13			0°C 25°C			255 235	μA
					12		11, 13, 14			75°C			200	
			X	0.5 V	11		12, 13, 14			0°C 25°C			510 470	μA
					13		11, 12, 14			75°C			400	
I_{IL}	Low-level input current	6	X	All inputs in parallel at −3.2 V						0°C 25°C 75°C			−0.5 −0.5 −0.6	μA
I_{CC} or $-I_{EE}$	Supply current	7	X	All inputs in parallel at −0.5 V						25°C	20		34	mA
C_{in}	Input capacitance (see Note 7)		X		Each					25°C		5		pF
Z_{out}	Output impedance (see Note 8)		X					2, 7	1, 8	25°C		5		Ω

NOTES: 6. The algebraic convention where the most-positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more-negative voltages.

7. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.

8. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TABLE I—INITIAL CONDITIONS

Several of the parameters require the application of conditions which cause the outputs to assume definite states prior to applying test conditions specified above.

SYMBOL	DESCRIPTION	INPUT TERMINALS* 0.5 V	INPUT TERMINALS* −0.5 V
X	Irrelevant		
S	Set 1Q and 2Q high, 1$\bar{Q}$ and 2$\bar{Q}$ low	11, 13	14, 12
R	Reset 1Q and 2Q low, 1$\bar{Q}$ and 2$\bar{Q}$ high		11, 12, 13, 14

*V_{BB} (pin 15) = GND, V_{CC} (pins 3 and 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V. Input and output terminals are open except as specified in these tables and in the d-c test figures.

ECL2541 electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS*									MIN	TYP	MAX	UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE II)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS 0.5 V	OTHER INPUT TERMINALS −0.5 V	OUTPUT TERMINAL Q	OUTPUT TERMINAL $\bar{Q}$	T_A	(SEE NOTE 6)			
V_{IH}	High-level input voltage									0°C	150		720	mV
										25°C	150		720	
										75°C	150		720	
V_{IL}	Low-level input voltage									0°C	−1500		−150	mV
										25°C	−1500		−150	
										75°C	−1500		−150	
$V_{OH(Q)}$	High-level output voltage at Q output, register mode	4	X	0.2 V	11		1, 9, 12, 16	8						mV
					13		1, 9, 14, 16	7		0°C	280			
				−0.2 V	12	11	1, 9, 16	8		25°C	315			
					14	13	1, 9, 16	7		75°C				
				−0.2 V	9	11	1, 12, 16	8						
					9	13	1, 14, 16	7						
$V_{OL(Q)}$	Low-level output voltage at Q output, register mode	4	X	−0.2 V	11		1, 9, 12, 16	8						mV
					13		1, 9, 14, 16	7		0°C				
				−0.2 V	12		1, 9, 11, 16	8		25°C			−330	
					14		1, 9, 13, 16	7		75°C			−210	
				−0.2 V	9		1, 11, 12, 16	8						
					9		1, 13, 14, 16	7						
$V_{OH(Q)}$	High-level output voltage at Q output, storage mode	4	S	0.2 V	12		1, 9, 11, 16	8		0°C	280	365		mV
					14		1, 9, 13, 16	7		25°C	315	400	500	
				0.2 V	9		1, 11, 12, 16	8		75°C		470	580	
					9		1, 13, 14, 16	7						
$V_{OL(Q)}$	Low-level output voltage at Q output, storage mode	4	R	0.2 V	12	11	1, 9, 16	8		0°C	−505	−440		mV
					14	13	1, 9, 16	7		25°C	−480	−400	−330	
				0.2 V	9	11	1, 12, 16	8		75°C		−280	−210	
					9	13	1, 14, 16	7						
$V_{OH(\bar{Q})}$	High-level output voltage at $\bar{Q}$ output, storage mode	4	R	0.2 V	12	11	1, 9, 16		2, 4	0°C	280	365		mV
					14	13	1, 9, 16		5, 6	25°C	315	400	500	
				0.2 V	9	11	1, 12, 16		2, 4	75°C		470	580	
					9	13	1, 14, 16		5, 6					
$V_{OL(\bar{Q})}$	Low-level output voltage at $\bar{Q}$ output, storage mode	4	S	0.2 V	12		1, 9, 11, 16		2, 4	0°C	−505	−440		mV
					14		1, 9, 13, 16		5, 6	25°C	−490	−425	−350	
				0.2 V	9		1, 11, 12, 16		2, 4	75°C		−390	−315	
					9		1, 13, 14, 16		5, 6					
$V_{OH(Q)}$	High-level output voltage at Q output, set mode	4	R	0.2 V	1	9	16	8		0°C	280			mV
					1	9	16	7		25°C	315			
										75°C				
$V_{OL(Q)}$	Low-level output voltage at Q output, reset mode	4	S	0.2 V	16	9	1	8		0°C			−330	mV
					16	9	1	7		25°C			−210	
										75°C				

(Continued on page 11)

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

ECL2541 electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS*									MIN	TYP	MAX	UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE II)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS 0.5 V	OTHER INPUT TERMINALS −0.5 V	OUTPUT TERMINAL Q	OUTPUT TERMINAL $\overline{Q}$	T_A	(SEE NOTE 6)			
I_{IH}	High-level input current	5	X	0.5 V	9		1, 11, 12 13,14,16			0°C			255	μA
					11		1, 9, 12, 13, 14, 16			25°C			235	
					13		1, 9, 11, 12, 14, 16			75°C			200	
					1		9, 11, 12 13, 14, 16			0°C			510	μA
					12		1, 9, 11 13, 14, 16			25°C			470	
					14		1, 9, 11 12, 13, 16			75°C			400	
					16		1, 9, 11 12, 13, 14							
I_{IL}	Low-level input current	6	X	All inputs in parallel at −3.2 V						0°C			−0.6	μA
										25°C			−0.8	
										75°C			−1.1	
I_{CC} or $-I_{EE}$	Supply current	7	X	All inputs in parallel at −0.5 V						25°C	60		124	mA
C_{in}	Input capacitance (see Note 7)		X		Each					25°C		5		pF
Z_{out}	Output impedance (see Note 8)		X					7, 8	2, 4, 5, 6	25°C		5		Ω

NOTES: 6. The algebraic convention where the most-positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more-negative voltages.

7. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Z. C_{in} = Q/V. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.

8. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TABLE II—INITIAL CONDITIONS

Several of the parameters require the application of conditions which cause the outputs to assume definite states prior to applying test conditions specified above.

SYMBOL	DESCRIPTION	INPUT TERMINALS* 0.5 V	INPUT TERMINALS* −0.5 V
X	Irrelevant		
S	Set 1Q and 2Q high, 1$\overline{Q}$1, 1$\overline{Q}$2, 2$\overline{Q}$1, and 2$\overline{Q}$2 low	1, 9	16
R	Reset 1Q and 2Q low, 1$\overline{Q}$1, 1$\overline{Q}$2, 2$\overline{Q}$1, and 2$\overline{Q}$2 high	9, 16	1

*V_{BB} (pin 15) = GND, V_{CC} (pin 3) = 1.32 V, V_{EE} (pin 10) = −3.2 V. Input and output terminals are open except as specified in these tables and in the d-c test figures.

ECL2542 electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS*														UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE III)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS		OUTPUT TERMINAL	T_A	MIN	TYP	MAX (SEE NOTE 6)				
						0.5 V	−0.5 V	$\overline{Q}$								
V_{IH}	High-level input voltage								0°C	150		720				mV
									25°C	150		720				
									75°C	150		720				
V_{IL}	Low-level input voltage								0°C	−1500		−150				mV
									25°C	−1500		−150				
									75°C	−1500		−150				
V_{OH}	High-level output voltage, register mode	4	X	−0.2 V	13	1, 16	4, 5, 12, 14	2	0°C		280					mV
					11	7, 8	4, 5, 9, 12	6	25°C		315					
					14	1, 16	4, 5, 12, 13	2	75°C							
					9	7, 8	4, 5, 11, 12	6								
					12	1, 16	4, 5, 13, 14	2								
					12	7, 8	4, 5, 9, 11	6								
					16	13, 14	1, 4, 5, 12	2								
					8	9, 11	4, 5, 7, 12	6								
					1	13, 14	4, 5, 12, 16	2								
					7	9, 11	4, 5, 8, 12	6								
					12	13, 14	1, 4, 5, 16	2								
					12	9, 11	4, 5, 7, 8	6								
V_{OL}	Low-level output voltage, register mode	4	X	0.2 V	13	1	4, 5, 12, 14, 16	2	0°C			−350				mV
					11	7	4, 5, 8, 9, 12	6	25°C			−315				
				−0.2 V	14	1, 13	4, 5, 12, 16	2	75°C							
					9	7, 11	4, 5, 8, 12	6								
				−0.2 V	12	1, 13	4, 5, 14, 16	2								
					12	7, 11	4, 5, 8, 9	6								
				0.2 V	16	14	1, 4, 5, 12, 13	2								
					8	9	4, 5, 7, 11, 12	6								
				−0.2 V	1	14, 16	4, 5, 12, 13	2								
					7	8, 9	4, 5, 11, 12	6								
				−0.2 V	12	14, 16	1, 4, 5, 13	2								
					12	8, 9	4, 5, 7, 11	6								
					14	1, 13	4, 5, 12, 16	2								
V_{OH}	High-level output voltage, storage mode	4	R	0.2 V	9	7, 11	4, 5, 8, 12	6	0°C	280	365					mV
					1	14, 16	4, 5, 12, 13	2	25°C	315	400	500				
					7	8, 9	4, 5, 11, 12	6	75°C		470	580				
					12		1, 4, 5, 13, 14, 16	2								
					12		4, 5, 7, 8, 9, 11	6								
V_{OL}	Low-level output voltage, storage mode	4	S	0.2 V	14	1	4, 5, 12, 13, 16	2	0°C	−505	−440					mV
					9	7	4, 5, 8, 11, 12	6	25°C	−490	−425	−350				
					1	14	4, 5, 12, 13, 16	2	75°C		−390	−315				
					7	9	4, 5, 8, 11, 12	6								
					12		1, 4, 5, 13, 14, 16	2								
					12		4, 5, 7, 8, 9, 11	6								
V_{OL}	Low-level output voltage, set mode	4	R	0.2 V	5	12	4	2	0°C			−350				mV
					5	12	4	6	25°C			−315				
									75°C							
V_{OH}	High-level output voltage, reset mode	4	S	0.2 V	4	12	5	2	0°C	280						mV
					4	12	5	6	25°C	315						
									75°C							

(Continued on page 13)

ECL2542 electrical characteristics at specified free-air temperature (continued)

PARAMETER	TEST CONDITIONS*							MIN	TYP (SEE NOTE 6)	MAX	UNIT
	TEST FIGURE	INITIAL CONDITIONS (SEE TABLE III)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS 0.5 V	OTHER INPUT TERMINALS −0.5 V	OUTPUT TERMINAL $\overline{Q}$	T_A			
I_{IH} High level input current	5	X	0.5 V	8		1, 4, 5, 7, 9, 11, 12, 13, 14, 16		0°C		255	μA
				11		1, 4, 5, 7, 8, 9, 12, 13, 14, 16		25°C		235	
				12		1, 4, 5, 7, 8, 9, 11, 13, 14, 16		75°C		200	
				13		1, 4, 5, 7, 8, 9, 11, 12, 14, 16					
				16		1, 4, 5, 7, 8, 9, 11, 12, 13, 14					
				1		4, 5, 7, 8, 9, 11, 12, 13, 14, 16		0°C		510	μA
				4		1, 5, 7, 8, 9, 11, 12, 13, 14, 16		25°C		470	
				5		1, 4, 7, 8, 9, 11, 12, 13, 14, 16		75°C		400	
				7		1, 4, 5, 8, 9, 11, 12, 13, 14, 16					
				9		1, 4, 5, 7, 8, 11, 12, 13, 14, 16					
				14		1, 4, 5, 7, 8, 9, 11, 12, 13, 16					
I_{IL} Low-level input current	6	X	0.5 V	All inputs in parallel at −3.2 V				0°C		−0.9	μA
								25°C		−1.2	
								75°C		−1.7	
I_{CC} or $-I_{EE}$ Supply current	7	X	0.5 V	All inputs in parallel at −0.5 V				25°C	81	165	mA
C_{in} Input capacitance (see Note 7)		X		Each				25°C		5	pF
Z_{out} Output impedance (see Note 8)		X					2, 6	25°C		5	Ω

*V_{BB} (pin 15) = GND, V_{CC} (pin 3) = −1.3 V, V_{EE} (pin 10) = −3.2 V. Input and output terminals are open except as specified in these tables and in the d-c test figures.

NOTES: 6. The algebraic convention where the most-positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more-negative voltages.

7. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.

8. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TABLE III–INITIAL CONDITIONS

Several of the parameters require the application of conditions which cause the outputs to assume definite states prior to applying test conditions specified above.

SYMBOL	DESCRIPTION	INPUT TERMINALS* 0.5 V	INPUT TERMINALS* −0.5 V
X	Irrelevant		
S	Set $1\overline{Q}$ and $2\overline{Q}$ low	5, 12	4
R	Reset $1\overline{Q}$ and $2\overline{Q}$ high	4, 12	5

4

operating characteristics at specified free-air temperature

MODE	C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns									t_{THL} and/or t_{TLH} TRANSITION TIMES—ns								
		T_A = 0°C			T_A = 25°C			T_A = 75°C			T_A = 0°C			T_A = 25°C			T_A = 75°C		
	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2540 (see Figure 2 and Table IV)																			
Register	4		2.5		1.6	2.4	3.5		2.5			3.8		2	3.7	5.2		3.9	
	50		3.6		2.4	3.6	4.5		3.6			4.7		2.5	4.6	6.7		4.4	
ECL2541 (see Figure 3 and Table V)																			
Register (Clock Controlled)	4		6.3		4.2	6.2	7.7		6.5			4.6		2	4.7	6.9		4.7	
	50		7.7		5.5	7.8	10.8		8.0			5.9		2.7	5.8	8.6		5.5	
Register (Gate Controlled)	4		4.3		2.3	4.2	5.8		4.3			4.6		2.3	4.6	6.5		4.6	
	50		5.6		3.4	5.7	8.5		5.7			5.6		2.7	5.4	7.8		5.1	
Set	4		2.7		1.9	2.7	3.5		2.8			4.5		2.9	4.5	6		4.6	
	50		3.8		2.7	3.8	4.7		3.8			4.7		2.7	4.6	7		4.5	
Reset	4		3.8		2.3	3.8	5.8		4.1			4.4		2.3	4.3	6.5		4.6	
	50		6.0		3.4	5.9	8.5		6.0			7.1		4.6	7.0	8.6		6.4	
ECL2542 (see Figure 3 and Table VI)																			
Register (Clock Controlled)	4		7.0		5.5	7.0	8.1		7.1			4.6		3	4.5	5.7		4.5	
	50		8.2		6.7	8.1	9.4		8.3			4.8		3	4.8	6.9		4.7	
Register (Gate Controlled)	4		4.5		3.3	4.4	5.7		4.4			4.2		3	4.1	5.7		4.1	
	50		5.7		4.5	5.6	6.8		5.5			4.7		3	4.7	6.9		4.6	
Set	4		2.9		1.7	2.7	3.1		2.6			4.6		3	4.5	5.7		4.6	
	50		4.0		3.2	4.0	4.7		3.9			5.4		4	5.6	6.9		5.5	
Reset	4		4.4		3.3	4.3	5.8		4.6			4.2		3	4.2	5.7		4.4	
	50		5.4		4.5	5.4	6.8		5.4			3.9		3	4.0	5		4.0	

4

PARAMETER MEASUREMENT INFORMATION

TABLE IV—ECL2540

INPUT TERMINALS		OUTPUT UNDER TEST		PARAMETER MEASURED
DATA GENERATOR	−0.5 V			
14	12	2	Q	t_{PLH}, t_{TLH}, t_{PHL}, and t_{THL}
14	12	1	$\overline{Q}$	
12	14	7	Q	
12	14	8	$\overline{Q}$	

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

TABLE V–ECL2541

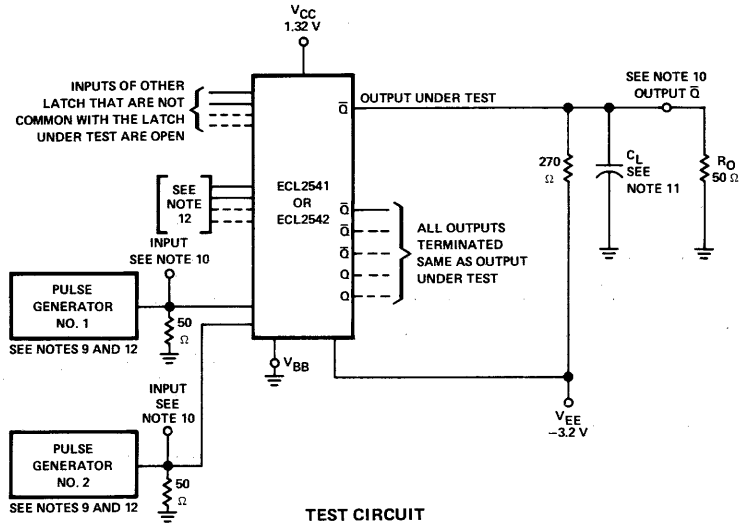
MODE	INPUT TERMINAL CONDITIONS				OUTPUT UNDER TEST	WAVEFORM	PARAMETER MEASURED
	PULSE GENERATOR NO. 1	PULSE GENERATOR NO. 2	0.5 V	−0.5 V			
REGISTER (Clock Controlled)	16	9	11	1, 12	8	LH	t_{PLH}, t_{TLH}
	1			11, 12, 16	8	HL	t_{PHL}, t_{THL}
	1			11, 12, 16	2, 4	LH	t_{PLH}, t_{TLH}
	16		11	1, 12	2, 4	HL	t_{PHL}, t_{THL}
	16	9	13	1, 14	7	LH	t_{PLH}, t_{TLH}
	1			13, 14, 16	7	HL	t_{PHL}, t_{THL}
	1			13, 14, 16	5, 6	LH	t_{PLH}, t_{TLH}
	16		13	1, 14	5, 6	HL	t_{PHL}, t_{THL}
REGISTER (Gate Controlled)	16	12	11	1, 9	8	LH	t_{PLH}, t_{TLH}
	1			9, 11, 16	8	HL	t_{PHL}, t_{THL}
	1			9, 11, 16	2, 4	LH	t_{PLH}, t_{TLH}
	16		11	1, 9	2, 4	HL	t_{PHL}, t_{THL}
	16	14	13	1, 9	7	LH	t_{PLH}, t_{TLH}
	1			9, 13, 16	7	HL	t_{PHL}, t_{THL}
	1			9, 13, 16	5, 6	LH	t_{PLH}, t_{TLH}
	16		13	1, 9	5, 6	HL	t_{PHL}, t_{THL}
SET TIME	16	1	9	All other input terminals open	8	LH	t_{PLH}, t_{TLH}
					2, 4	HL	t_{PHL}, t_{THL}
					7	LH	t_{PLH}, t_{TLH}
					5, 6	HL	t_{PHL}, t_{THL}
RESET TIME	1	16	9		2, 4	LH	t_{PLH}, t_{TLH}
					8	HL	t_{PHL}, t_{THL}
					5, 6	LH	t_{PLH}, t_{TLH}
					7	HL	t_{PHL}, t_{THL}

TABLE VI–ECL2542

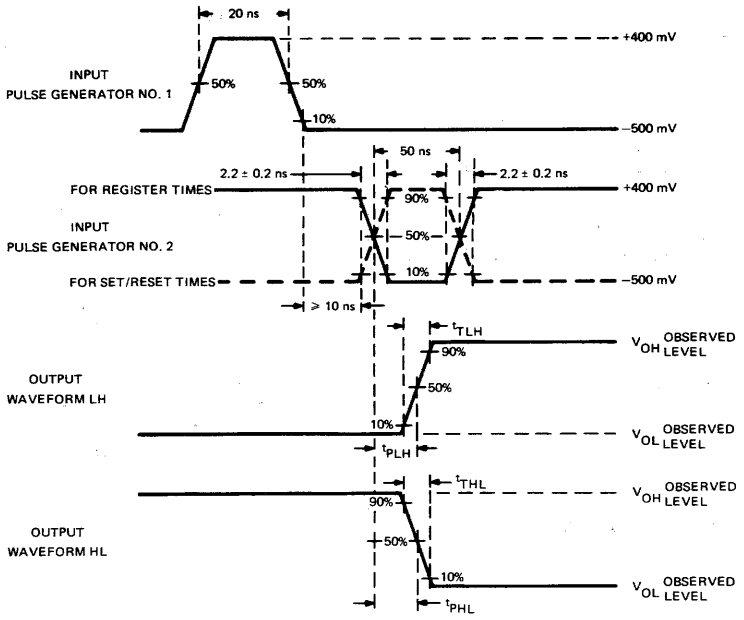
MODE	INPUT TERMINAL CONDITIONS				OUTPUT UNDER TEST	WAVEFORM	PARAMETER MEASURED
	PULSE GENERATOR NO. 1	PULSE GENERATOR NO. 2	0.5 V	−0.5 V			
REGISTER (Clock Controlled)	5	12	1, 16	4, 13, 14	2	LH	t_{PLH}, t_{TLH}
			13, 14	1, 4, 16		LH	t_{PLH}, t_{TLH}
	4		1, 13, 16	5, 14		HL	t_{PHL}, t_{THL}
			13, 14, 16	1, 5		HL	t_{PHL}, t_{THL}
	5	12	7, 8	4, 9, 11	6	LH	t_{PLH}, t_{TLH}
			9, 11	4, 7, 8		LH	t_{PLH}, t_{TLH}
	4		7, 8, 11	5, 9		HL	t_{PHL}, t_{THL}
			8, 9, 11	5, 7		HL	t_{PHL}, t_{THL}
REGISTER (Gate Controlled)	5	14	1, 16	4, 12, 13	2	LH	t_{PLH}, t_{TLH}
		1	13, 14	4, 12, 16		LH	t_{PLH}, t_{TLH}
	4	14	1, 13, 16	5, 12		HL	t_{PHL}, t_{THL}
		1	13, 14, 16	5, 12		HL	t_{PHL}, t_{THL}
	5	9	7, 8	4, 11, 12	6	LH	t_{PLH}, t_{TLH}
		7	9, 11	4, 8, 12		LH	t_{PLH}, t_{TLH}
	4	9	7, 8, 11	5, 12		HL	t_{PHL}, t_{THL}
		7	8, 9, 11	5, 12		HL	t_{PHL}, t_{THL}
SET TIME	4	5	12	All other input terminals open	2, 6	HL	t_{PHL}, t_{THL}
RESET TIME	5	4	12		2, 6	LH	t_{PLH}, t_{TLH}

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION
ECL2541 AND ECL2542



TEST CIRCUIT

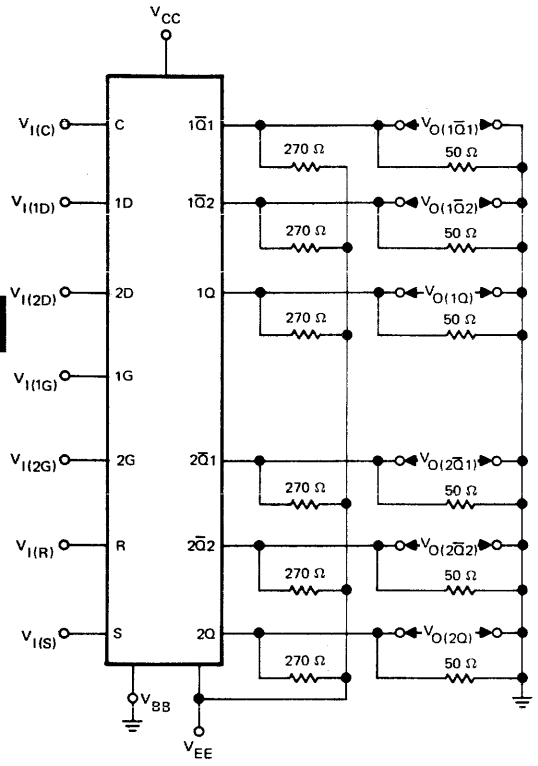


VOLTAGE WAVEFORMS

FIGURE 3—ECL2541 AND ECL2542 PROPAGATION DELAY AND TRANSITION TIMES

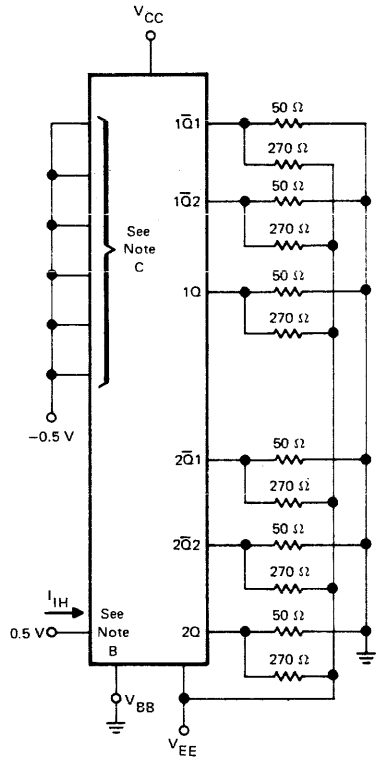
NOTES:
9. Each generator has a 50-Ω output impedance.
10. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistor designated R_O is the oscilloscope input resistance in the 50-Ω system or a discrete resistor with a high-impedance probe.
11. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.
12. See Table V (ECL2541) or Table VI (ECL2542) for voltages to be applied to input terminals for each test.

PARAMETER MEASUREMENT INFORMATION†
ECL2541
(See Note 13)



V_I is applied to each input as specified in the electrical characteristics table.

FIGURE 4–V_{OH} AND V_{OL}



A. Each input is tested separately.
B. Any one of the following seven inputs: C, 1D, 1G, 2D, 2G, R, and S.
C. Other six inputs listed in note B that are not under test.

FIGURE 5–I_{IH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.
NOTE 13: ECL2540 and ECL2542 are tested in a manner similar to that shown for ECL2541.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION†
ECL2541
(See Note 13)

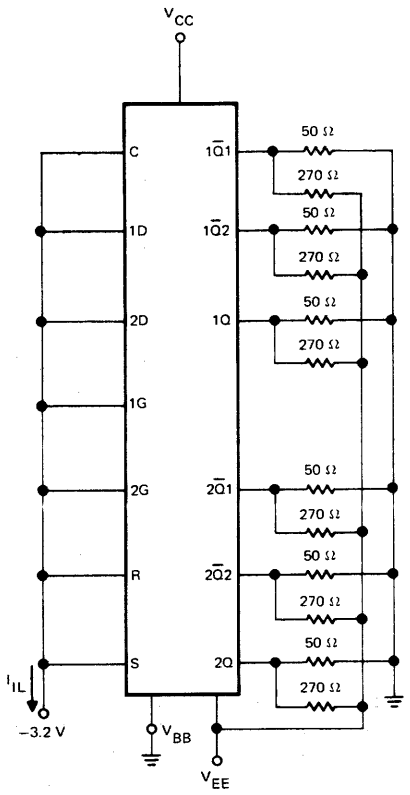


FIGURE 6–I_{IL}

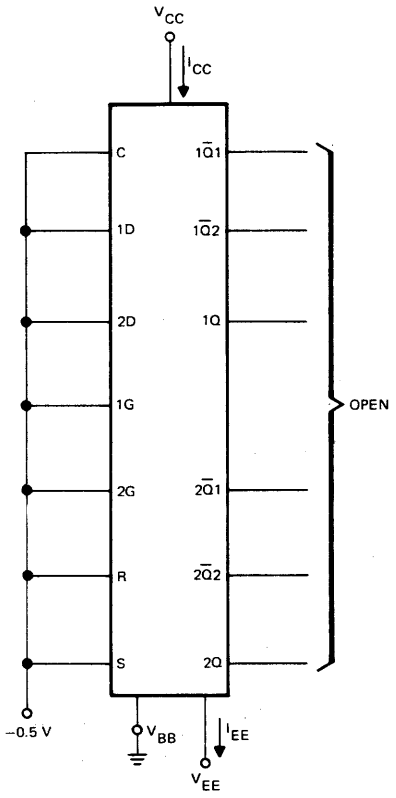


FIGURE 7–I_{CC} OR I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.
NOTE 13: ECL2540 and ECL2542 are tested in a manner similar to that shown for ECL2541.

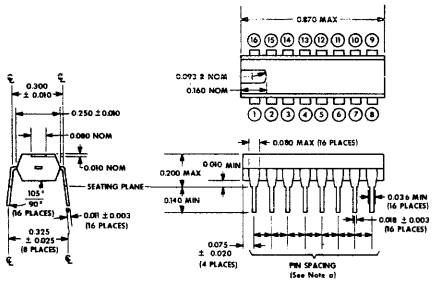
TYPES ECL2540 THRU ECL2542
EMITTER-COUPLED-LOGIC BISTABLE MODULES

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

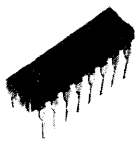
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between center-lines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams on pages 2 and 3. Outputs are denoted by 1Q, 1$\overline{Q}$, 2Q, 2$\overline{Q}$, 1$\overline{Q}$1, 1$\overline{Q}$2, 2$\overline{Q}$1, and 2$\overline{Q}$2. Inputs are denoted by C, C', 1D, 2D, 1D1, 1D2, 2D1, 2D2, 1G, 2G, 1G1, 1G2, 2G1, 2G2, S and R. The number preceding the letter denotes whether the input (or output) is part of the first or second latch. The number (if any) following the letter distinguishes inputs (or outputs) of the same latch from each other.

Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.

V_{BB} is a reference voltage.

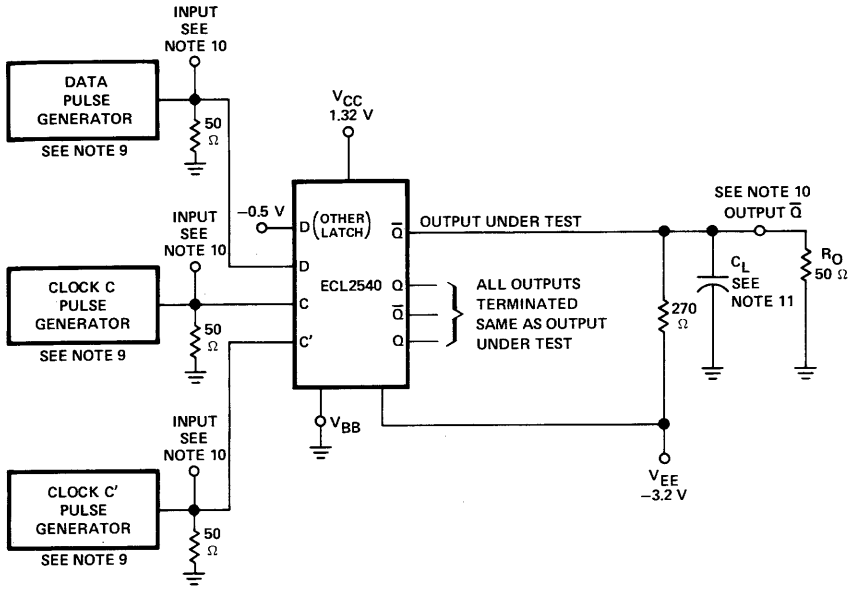
NC indicates no internal connection.

PIN ASSIGNMENTS

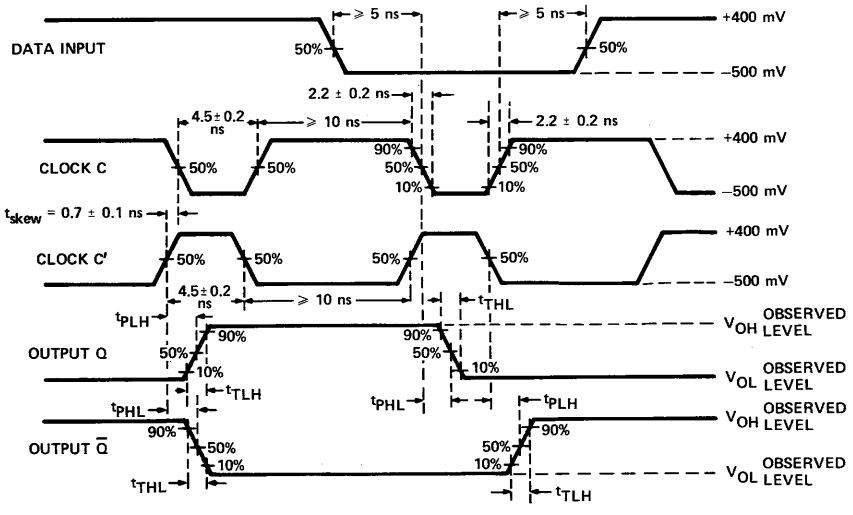
PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2540	1$\overline{Q}$	1Q	V_{CC}	NC	NC	V_{CC}	2Q	2$\overline{Q}$	NC	V_{EE}	C'	2D	C	1D	V_{BB}	NC
ECL2541	S	1$\overline{Q}$1	V_{CC}	1$\overline{Q}$2	2$\overline{Q}$1	2$\overline{Q}$2	2Q	1Q	C	V_{EE}	1D	1G	2D	2G	V_{BB}	R
ECL2542	1G1	1$\overline{Q}$	V_{CC}	R	S	2$\overline{Q}$	2G1	2D1	2G2	V_{EE}	2D2	C	1D2	1G2	V_{BB}	1D1

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION
ECL2540



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2–ECL2540 PROPAGATION DELAY AND TRANSITION TIMES (WITH SKEW)

NOTES:
9. Each generator has a 50-Ω output impedance.
10. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistor designated R_O is the oscilloscope input resistance in the 50-Ω system or a discrete resistor with a high-impedance probe.
11. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

Series 54S/74S Circuits

Schottky TTL
Previewing Three Series 54S/74S MSI Functions*

SN54S/74S181 Arithmetic/Logic Units

- Fastest and most versatile IC adder
- 20 ns typical add time for 16 bit words
- Performs all arithmetic/logic functions of a CPU
- Cascadable to N-bits
- Pin-for-pin functional equivalent of SN54/74181 ALU

SN54S/74S194 Universal Bidirectional Shift-Registers

- Industry's first fully universal 100-MHz TTL shift registers
  - Parallel broadside load
  - Shift right
  - Shift left
  - Inhibit clock (do nothing)
- Cascadable to N-bits
- Designed specifically for performing all shift functions required of high-speed accumulators employing SN74S181 ALU's

SN54S/74S157 Quad 2-Input Multiplexers

- Typical propagation delays of 2.25 ns per level at 13 mW per gate
- May be used with SN74S181 and SN74S194 to implement high-speed CPU accumulator
- Selects bused data from one of two sources
- Generates four functions of two variables (one variable is common)

* Available Mid-1971

For the Full Line of Series 54S/74S Schottky SSI, See Page 5-

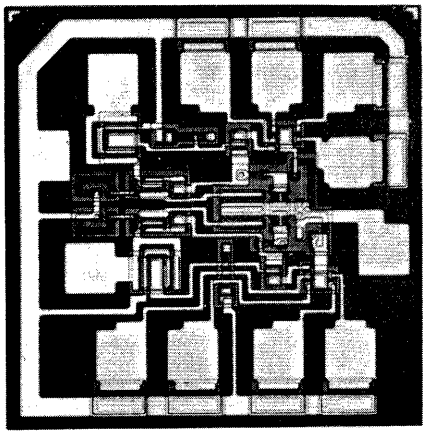
SCHOTTKY TTL

SERIES 54S/74S
SCHOTTKY-CLAMPED† TRANSISTOR-TRANSISTOR LOGIC

FOR HIGH-SPEED, HIGH-PERFORMANCE DIGITAL SYSTEMS

description

Series 54S/74S Schottky TTL circuits are implemented with full Schottky-barrier-diode clamping to achieve ultra-high speeds previously obtainable only with emitter-coupled logic, yet they retain the desirable features of, and are completely compatible with, most of the popular saturated logic circuits. Schottky TTL circuits currently offer the best speed-power product of any high-speed logic family.



Schottky-barrier-diode clamping prevents transistors from achieving classic saturation and thereby effectively eliminates excess charge storage and subsequent recovery times. These recovery times contribute significantly to overall propagation delays experienced with saturated digital-logic circuits.

Series 54S/74S circuits are completely compatible with the Series 54/74, Series 54H/74H, and Series 54L/74L TTL logic families. Ease of use and compatibility with other TTL families result in flexibility of choice within the four speed-power ranges offered (Series 54/74, 54H/74H, 54L/74L, 54S/74S) to achieve highly efficient system grading to specific performance requirements.

5

Definitive specifications are provided for operating characteristics over the full military temperature range of −55°C to 125°C for Series 54S circuits and over the temperature range of 0°C to 70°C for Series 74S circuits.

features

VERY-HIGH-SPEED, LOW-POWER OPERATION

- **3-ns typical gate propagation delay time**
- **19-mW-per-gate power dissipation at 50% duty cycle — speed-power product = 57 pJ**
- **125-MHz typical J-K flip-flop maximum input clock frequency (d-c coupled)**

EASE OF SYSTEM DESIGN

- **fully compatible with Series 54/74, 54H/74H, and 54L/74L TTL (including MSI/LSI), and most DTL**
- **Schottky-diode-clamped inputs simplify system design**
- **terminated, controlled-impedance lines not normally required**
- **low output impedance: provides low a-c noise susceptability**
  drives highly capacitive loads

IMPROVED CIRCUIT PERFORMANCE

- **switching times virtually insensitive to power supply and/or temperature variations**
- **power dissipation remains relatively low at operating frequencies up to 100 MHz**
- **high fan-out: 20 54S/74S loads at the high logic level**
  10 54S/74S loads at the low logic level
- **high d-c noise margin—typically 1 volt**

CONTENTS

271

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

SERIES 54S/74S
SCHOTTKY-CLAMPED TRANSISTOR-TRANSISTOR LOGIC

SERIES 54S/74S
FEATURING 3-ns SPEED AND 20-mW-PER-GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

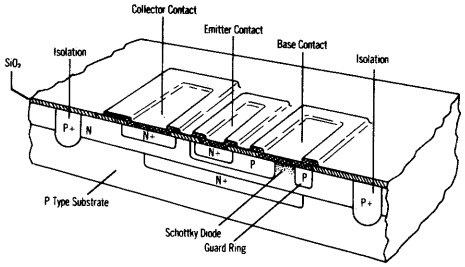
FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	PAGE
NAND/NOR GATES						
Quadruple 2-Input Positive-NAND Gates	SN54S00	SN74S00	J	N	W	5-4
Quadruple 2-Input Positive-NAND Gates (with Open-Collector Output)	SN54S03	SN74S03	J	N	W	5-8
Hex Inverters	SN54S04	SN74S04	J	N	W	5-4
Hex Inverters (with Open-Collector Output)	SN54S05	SN74S05	J	N	W	5-8
Triple 3-Input Positive-NAND Gates	SN54S10	SN74S10	J	N	W	5-4
Triple 3-Input Positive-AND Gates	SN54S11	SN74S11	J	N	W	5-10
Triple 3-Input Position-AND Gates (with Open-Collector Output)	SN54S15	SN74S15	J	N	W	5-10
Dual 4-Input Positive-NAND Gates	SN54S20	SN74S20	J	N	W	5-4
Dual 4-Input Positive-NAND Gates (with Open-Collector Output)	SN54S22	SN74S22	J	N	W	5-8
Dual 4-Input Positive-NAND Buffers	SN54S40	SN74S40	J	N	W	5-12
Dual 4-Input Positive-NAND Line Drivers	SN54S140	SN74S140	J	N	W	5-12
AND-OR-INVERT GATES						
4-2-3-2-Input AND-OR-INVERT Gates	SN54S64	SN74S64	J	N	W	5-13
4-2-3-2-Input AND-OR-INVERT Gates (with Open-Collector Output)	SN54S65	SN74S65	J	N	W	5-13
FLIP-FLOPS						
Dual D-Type Edge-Triggered Flip-Flops	SN54S74	SN74S74	J	N	W	5-15
Dual J-K Negative Edge-Triggered Flip-Flops (80 MHz) with Preset and Clear	SN54S112	SN74S112	J	N	W	5-17
Dual J-K Negative Edge-Triggered Flip-Flops (80 MHz) with Preset	SN54S113	SN74S113	J	N	W	5-21
Dual J-K Negative Edge-Triggered Flip-Flops (80 MHz) Common Clock and Common Clear	SN54S114	SN74S114	J	N	W	5-21

*For outline drawings of all packages, see Section 1.

5

The Schottky TTL Technology

The Schottky-clamped transistor is produced utilizing conventional diffusions. The base contact opening is extended beyond the base diffusion and over the collector region. Metallization is deposited over both the base and collector regions and simultaneously serves as the transistor base contact and the SBD anode contact. The collector n-type material and the metallization then form the metal-silicon SBD structure (refer to cross-section at right).



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

The Schottky TTL Technology (Continued)

The SBD is connected in parallel to the base-collector junction of the normal TTL n-p-n transistor. As the SBD has a lower forward voltage than the base-collector junction, it clamps the transistor as base drive increases, diverting most excess base current from the base-collector junction, and prevents the transistor from reaching classic saturation. Excess stored charge, which exists in usual transistor structures and which must be removed before switching occurs, does not exist in the SBD-clamped transistor.

In addition to incorporation of the SBD into popular 54/74 TTL, the Series 54S/74S Schottky TTL family employs shallower diffusion and smaller geometries which lower internal capacitances and further reduces overall propagation delays. Elimination of gold-doping simplifies processing and stabilizes switching speeds over the operating temperature range.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Output voltage (see Notes 1 and 3) . . . . . 7 V
Operating free-air temperature range: Series 54S Circuits . . . . . −55°C to 125°C
Series 74S Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This is the maximum voltage which should be applied to any open-collector output when it is in the off state.

5

recommended operating conditions

	SERIES 54S CIRCUITS			SERIES 74S CIRCUITS			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

unused inputs of positive-AND/NAND gates

For optimum switching times and minimum noise susceptibility, unused inputs of AND or NAND gates should be maintained at a voltage greater than 2.7 V, but not to exceed the absolute maximum rating of 5.5 V. This eliminates the distributed capacitance associated with the floating input emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between 2.7 V and 3.5 V.
b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each additional input presents a full load to the driving output at a high-level voltage but adds no loading at a low-level voltage.
c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor.

input-current requirements

Input-current requirements reflect worst-case V_{CC} and temperature conditions. Each input of the multiple-emitter input transistors requires a maximum of 2 mA out of the input at a low logic level which is defined as 1 normalized load. Each input requires current into the input at a high logic level. This current is 50 μA maximum for each emitter. Currents into the input terminals are specified as positive values.

fan-out capability

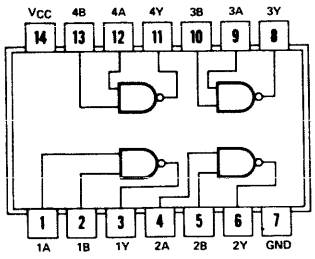
Fan-out (N) reflects the ability of an output to supply current to a number of normalized loads at a high logic level and to sink current at the low logic level. At the high logic level, each standard output is capable of supplying current to drive 20 Series 54H, 74H, 54S, or 74S loads (N_H = 20). Currents out of the output are specified as negative values. At the low logic level, each standard output is capable of sinking current from 10 Series 54H, 74H, 54S, or 74S loads (N_L = 10).

CIRCUIT TYPES SN54S00, SN54S04, SN54S10, SN54S20, SN74S00, SN74S04, SN74S10, SN74S20
POSITIVE-NAND GATES/HEX INVERTERS

Typical Propagation Time . . . 3 ns at C_L = 15 pF
Typical Power Dissipation . . . 19 mW per Gate at 50% Duty Cycle

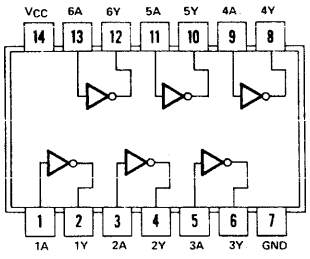
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)

SN54S00, SN74S00
QUADRUPLE 2-INPUT NAND GATES



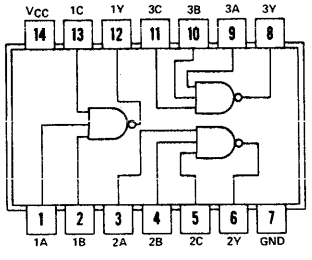
positive logic: $Y = \overline{AB}$

SN54S04, SN74S04
HEX INVERTERS



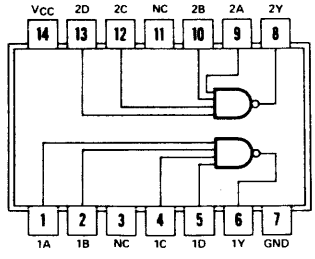
positive logic: $Y = \overline{A}$

SN54S10, SN74S10
TRIPLE 3-INPUT NAND GATES



positive logic: $Y = \overline{ABC}$

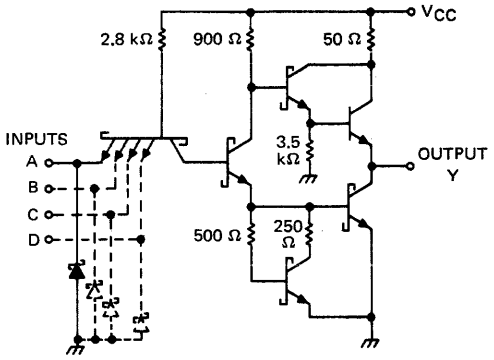
SN54S20, SN74S20
DUAL 4-INPUT NAND GATES



positive logic: $Y = \overline{ABCD}$

NC - No internal connection

schematic (each gate)



Component values shown are nominal.

recommended operating conditions

		SN54S00, SN54S04, SN54S10, SN54S20			SN74S00, SN74S04, SN74S10, SN74S20			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature, T_A		−55		125	0		70	°C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	V_{IL} = 0.8 V,	Series 54S	2.5	3.4		V
		I_{OH} = −1 mA		Series 74S	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20 mA	V_{IH} = 2 V,				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7 V				50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−40		−100	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0 V			2.5	4	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5 V			5	9	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

5

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS¶		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	R_L = 280 Ω	2	3	4.5	ns
		C_L = 50 pF,	R_L = 280 Ω		4.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	R_L = 280 Ω	2	3	5	ns
		C_L = 50 pF,	R_L = 280 Ω		5		

¶Switching characteristic measurements are made utilizing the same test circuits as illustrated for Darlington outputs in Figure 74 of the Series 54H/74H section. The inverting-output waveform is applicable for these three circuits. In lieu of Notes 1 through 4, the following notes are applicable:

NOTES: A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 2.5 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.

B. Inputs not under test are at 2.7 V.

C. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

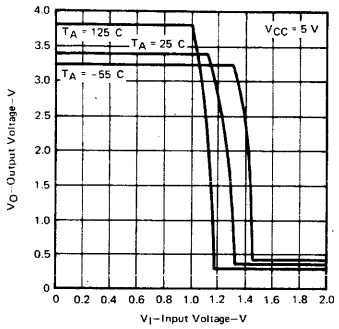


FIGURE 1

INPUT-CLAMPING-DIODE
FORWARD VOLTAGE
vs
FREE-AIR TEMPERATURE

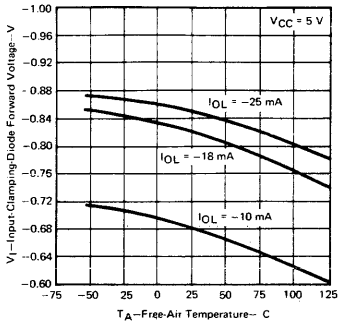


FIGURE 2

INPUT CURRENT
vs
INPUT VOLTAGE

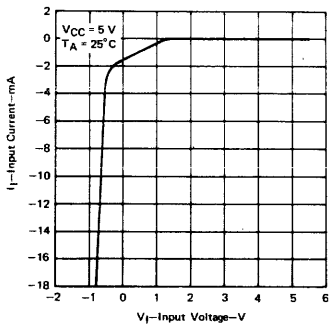


FIGURE 3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

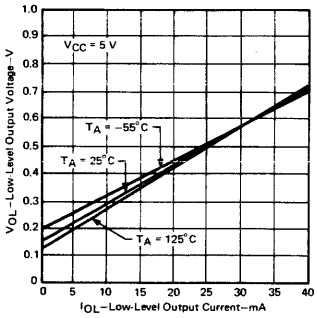


FIGURE 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

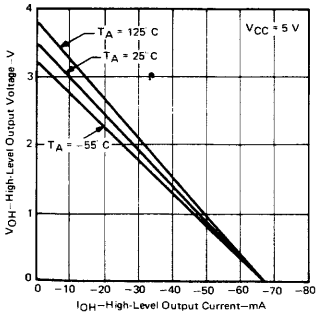


FIGURE 5

HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

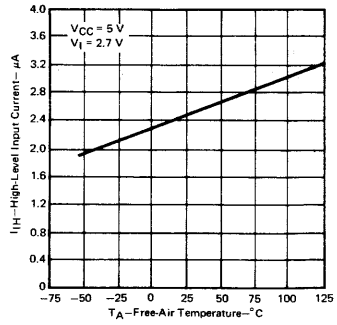


FIGURE 6

†Data for temperatures below 0°C and above 70°C is applicable to Series 54S circuits only.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

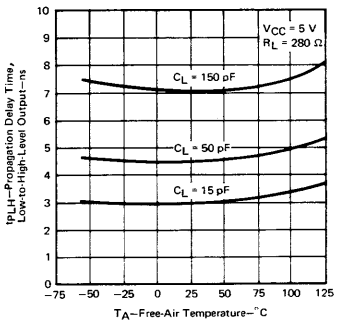


FIGURE 7

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

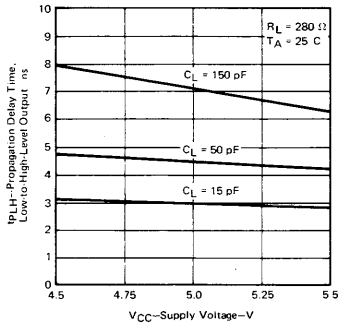


FIGURE 8

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

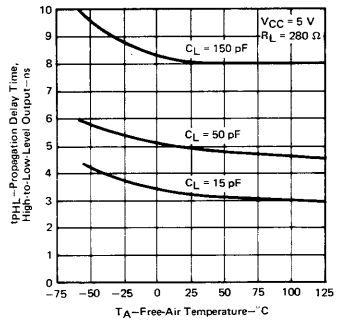


FIGURE 9

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

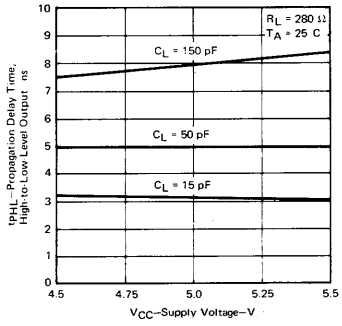


FIGURE 10

AVERAGE PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

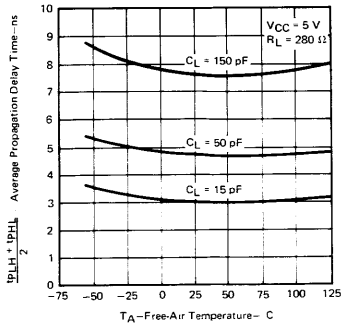


FIGURE 11

POWER DISSIPATION PER GATE
vs
FREQUENCY

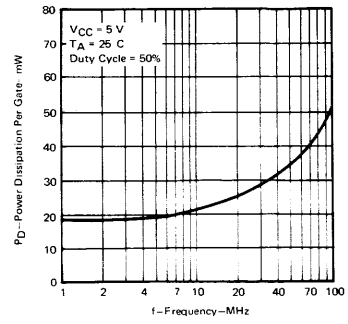


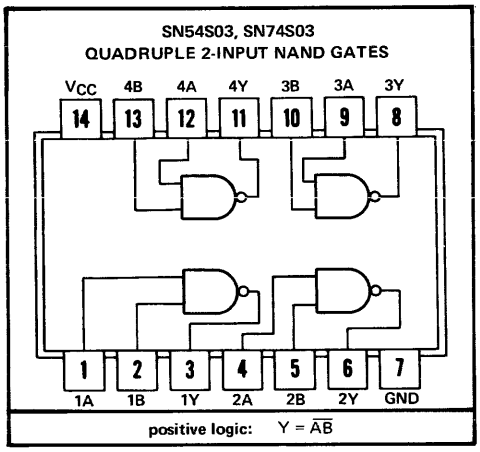
FIGURE 12

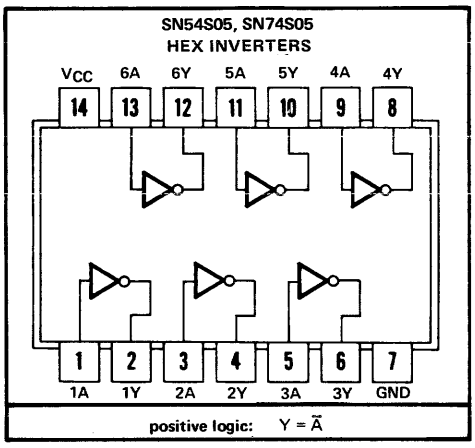
†Data for temperatures below 0°C and above 70°C is applicable to Series 54S circuits only.

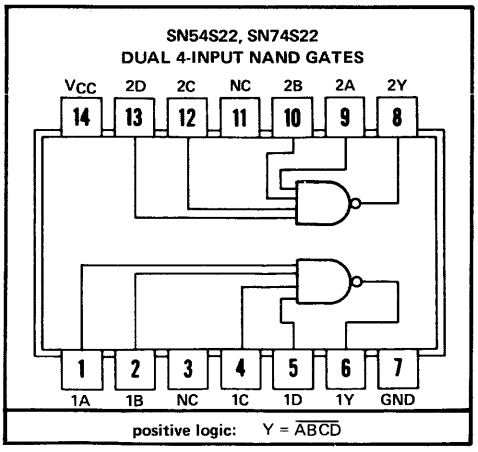
CIRCUIT TYPES SN54S03, SN54S05, SN54S22, SN74S03, SN74S05, SN74S22
POSITIVE-NAND GATES/HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

Typical Propagation Time . . . 5 ns at C_L = 15 pF
Typical Power Dissipation . . . 17 mW per Gate at 50% Duty Cycle

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)

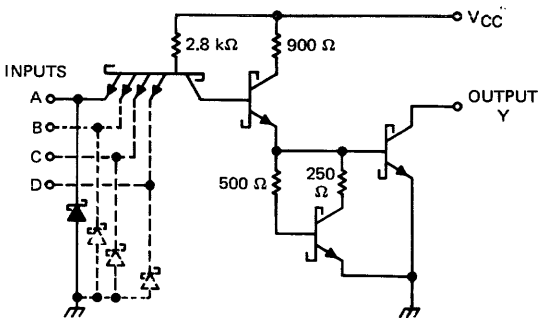






NC—No internal connection

schematic (each gate)



Component values shown are nominal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

	SN54S03, SN54S05, SN54S22			SN74S03, SN74S05, SN74S22			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from any output, N			10			10	
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 5.5 V	V_{IL} = 0.8 V,			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20 mA	V_{IH} = 2 V,			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7 V			50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5 V			−2	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0 V		1.5	3.3	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5 V		5	9	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS¶		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	R_L = 280 Ω	2	5	7.5	ns
		C_L = 50 pF,	R_L = 280 Ω		7.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	R_L = 280 Ω	2	4.5	7	ns
		C_L = 50 pF,	R_L = 280 Ω		7		

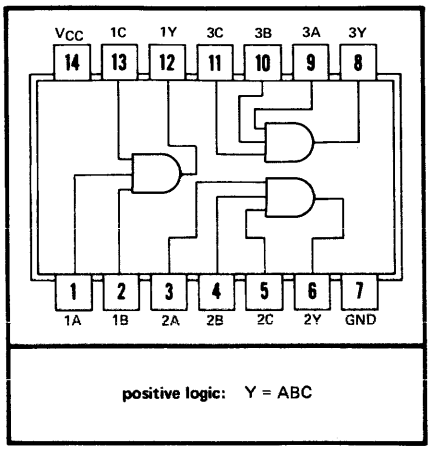
¶ Switching characteristic measurements are made utilizing the same test circuit as illustrated for open-collector outputs in Figure 74 of the Series 54H/74H section. The inverting-output waveform is applicable for these circuits. In lieu of Notes 1 through 4, the following notes are applicable:

NOTES: A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 2.5 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.
B. Inputs not under test are at 2.7 V.
C. C_L includes probe and jig capacitance.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54S11, SN54S15, SN74S11, SN74S15
TRIPLE 3-INPUT POSITIVE-AND GATES

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: Y = ABC

SN54S11, SN74S11 ACTIVE PULL-UP

- Typical Propagation Time . . . 5 ns at C_L = 15 pF
- Typical Power Dissipation . . . 32 mW per Gate at 50% Duty Cycle

SN54S15, SN74S15 OPEN-COLLECTOR

- Typical Propagation Time . . . 6 ns at C_L = 15 pF
- Typical Power Dissipation . . . 29 mW per Gate at 50% Duty Cycle

5

recommended maximum fan-out from each output

	SN54S11 SN74S11	SN54S15 SN74S15
Loads at a high logic level	20	
Loads at a low logic level	10	10

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		SN54S11 SN74S11 MIN	TYP‡	MAX	SN54S15 SN74S15 MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −1 mA	SN54S11	2.5	3.4					V
			SN74S11	2.7	3.4					
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 5.5 V							250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.7 V				50			50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.5 V				−2			−2	mA
I_{OS}	Short-circuit output current §	V_{CC} = MAX		−40		−100				mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX, All inputs at 5 V			4.5	8		3.5	6.5	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX, All inputs at 0 V			8	14		8	14	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable series on the second page of this section.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS¶	SN54S11 SN74S11			SN54S15 SN74S15			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 280 Ω	2.5	4.5	7	2.5	5.5	8.5	ns
		C_L = 50 pF, R_L = 280 Ω		6			8.5		ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 280 Ω	2.5	5	7.5	2.5	6	9	ns
		C_L = 50 pF, R_L = 280 Ω		7.5			8		ns

¶Switching characteristic measurements are made utilizing the same test circuits as illustrated in Figure 74 of the Series 54H/74H section. The noninverting-output waveform is applicable for these circuits. In lieu of Notes 1 through 4, the following notes are applicable:

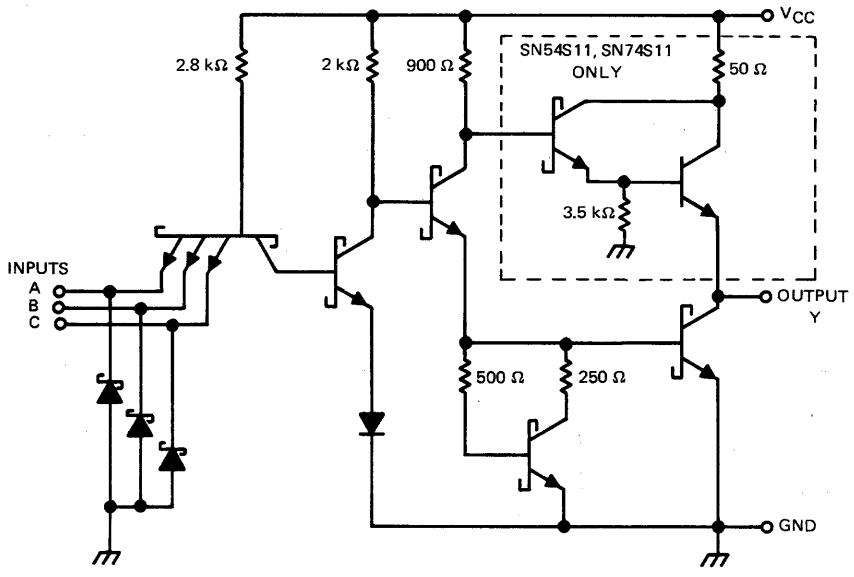
NOTES: A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 2.5 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.

B. Inputs not under test are at 2.7 V.

C. C_L includes probe and jig capacitance.

5

schematic (each gate)

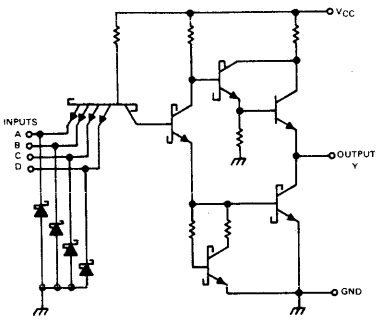


Component values shown are nominal.

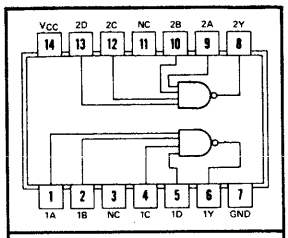
CIRCUIT TYPES SN54S40, SN54S140, SN74S40, SN74S140
DUAL 4-INPUT POSITIVE-NAND BUFFERS/LINE DRIVERS

Typical Propagation Time . . . 4 ns at C_L = 50 pF

schematic (each gate)



J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCD}$

NC - No internal connection

recommended maximum fan-out from each output

Loads at a high logic level 60
Load at a low logic level 30

electrical characteristics over operating free-air temperature range (unless otherwise noted)

5

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −3 mA	Series 54S	2.5	3.4		V
			Series 74S	2.7	3.4		
		V_{CC} = MIN, V_I = 0.5 V, R_O = 50 Ω to GND	SN54S140 SN74S140	2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 60 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.7 V				100	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.5 V				−4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−50		−225	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX, All inputs at 0 V			5	9	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX, All inputs at 5 V			12.5	22	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable series on the second page of this section.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed 100 milliseconds.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 30

PARAMETER		TEST CONDITIONS¶	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 93 Ω	2	4	6.5	ns
		C_L = 150 pF, R_L = 93 Ω		6		ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 50 pF, R_L = 93 Ω	2	4	6.5	ns
		C_L = 150 pF, R_L = 93 Ω		6		ns

¶Switching characteristic measurements are made utilizing the same test circuits as illustrated for Darlington outputs in Figure 74 of the Series 54H/74H section. The inverting waveform is applicable for these circuits. In lieu of Notes 1 through 4, the following notes are applicable:

NOTES: A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 2.5 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.
B. Inputs not under test are at 2.7 V.
C. C_L includes probe and jig capacitance.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54S64, SN54S65, SN74S64, SN74S65
4-2-3-2-INPUT AND-OR-INVERT GATES

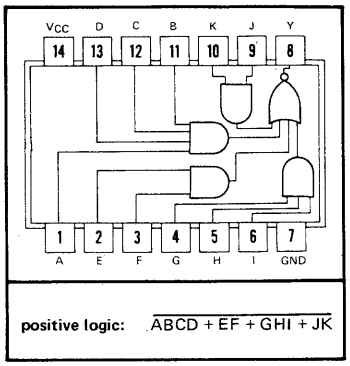
SN54S64, SN74S64 ACTIVE PULL-UP

- Typical Propagation Time . . . 3.5 ns at C_L = 15 pF
- Typical Power Dissipation . . . 39 mW at 50% Duty Cycle

SN54S65, SN74S65 OPEN-COLLECTOR

- Typical Propagation Time . . . 5 ns at C_L = 15 pF
- Typical Power Dissipation . . . 36 mW at 50% Duty Cycle

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: $\overline{ABCD + EF + GHI + JK}$

recommended maximum fan-out from each output

	SN54S64 SN74S64	SN54S65 SN74S65
Loads at a high logic level	20	
Loads at a low logic level	10	10

5

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54S64 SN74S64 MIN	SN54S64 SN74S64 TYP‡	SN54S64 SN74S64 MAX	SN54S65 SN74S65 MIN	SN54S65 SN74S65 TYP‡	SN54S65 SN74S65 MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 0.8 V, I_{OH} = −1 mA	SN54S64	2.5	3.4					V
			SN74S64	2.7	3.4					
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 0.8 V, V_{OH} = 5.5 V							250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 2 V, I_{OL} = 20 mA				0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.7 V				50			50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.5 V				−2			−2	mA
I_{OS}	Short-circuit output current §	V_{CC} = MAX		−40		−100				mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX, See Note 1			7	12.5	6	11		mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, See Note 2			8.5	16	8.5	16		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable Series on the second page of this section.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTES: 1. I_{CCH} is measured with all inputs grounded, and the outputs open.
2. I_{CCL} is measured with all inputs of one gate at 5 V, the remaining inputs grounded, and the outputs open.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54S64, SN54S65, SN74S64, SN74S65
4-2-3-2-INPUT AND-OR-INVERT GATES

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS¶	SN54S64 SN74S64			SN54S65 SN74S65			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 280 Ω	2	3.5	5.5	2	5	7.5	ns
		C_L = 50 pF, R_L = 280 Ω		5			8		ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 280 Ω	2	3.5	5.5	2	5.5	8.5	ns
		C_L = 50 pF, R_L = 280 Ω		5.5			6.5		ns

¶ Switching characteristic measurements are made utilizing the same test circuits as illustrated in Figure 74 of the Series 54H/74H section. The inverting output waveform is applicable for these circuits. In lieu of Notes 1 through 4, the following notes are applicable:

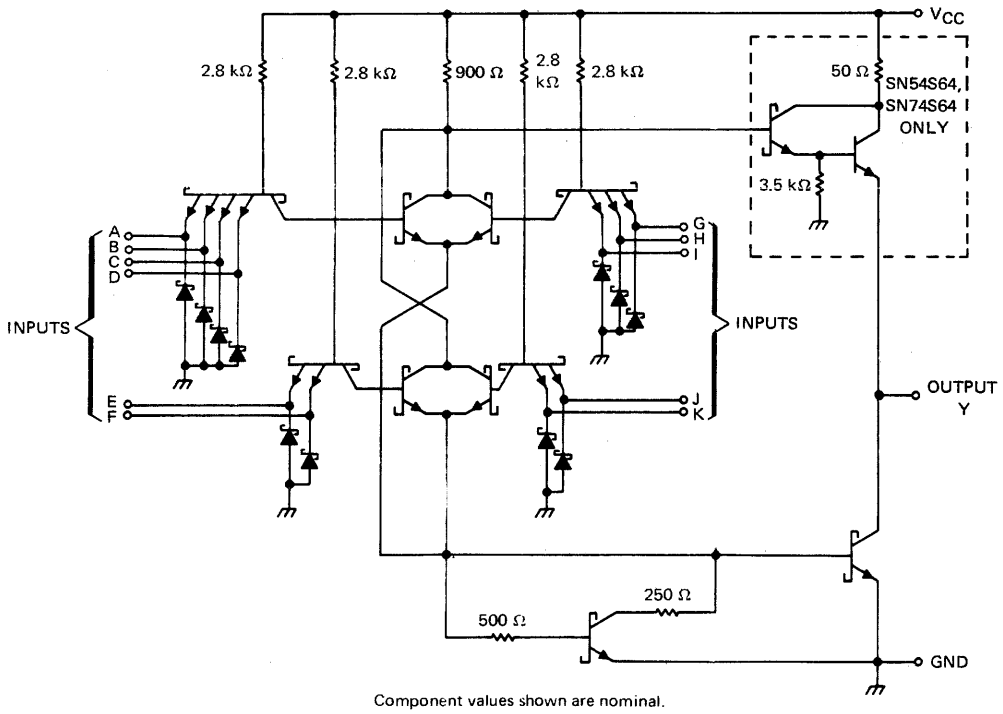
NOTES: A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 \approx t_0$ = 2.5 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx$ 50 Ω.

B. Input pulse is applied to one input of one AND section, 2.7 V is applied to all unused inputs of that AND section, and all inputs of unused AND sections are grounded.

C. C_L includes probe and jig capacitance.

5

schematic



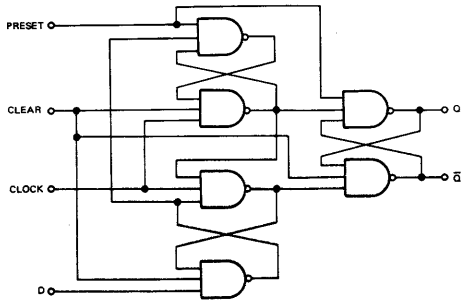
Component values shown are nominal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54S74, SN74S74
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

Typical Maximum Input Clock Frequency . . . 90 MHz
Typical Power Dissipation . . . 75 mW per Flip-Flop

functional block diagram (each flip-flop)



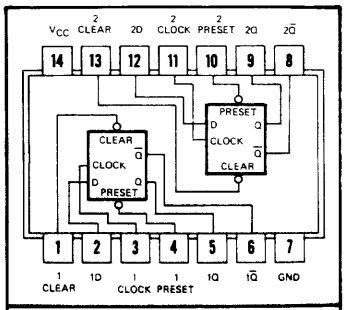
TRUTH TABLE
(Each Flip-Flop)

t_n	t_{n+1}	
INPUT	OUTPUT	
D	Q	Q̄
L	L	H
H	H	L

H = high level, L = low level

NOTES: A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

description

These monolithic dual edge-triggered flip-flops utilize Schottky TTL circuitry to produce very-high-speed D-type flip-flops. Each flip-flop has individual clear and preset inputs, and also complementary Q and Q̄ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL circuits. A full fan-out to 10 normalized Series 54S/74S loads is available from each of the outputs at a low logic level. At a high logic level, a fan-out of 20 is available to facilitate tying unused inputs to used inputs. Maximum clock frequency is 75 megahertz, with a typical power dissipation of 75 milliwatts per flip-flop.

The SN54S74 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74S74 is characterized for operation from 0°C to 70°C.

recommended operating conditions

		SN54S74			SN74S74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Clock frequency, f_{clock}			70			70		MHz
Width of clock pulse, $t_{w(clock)}$			7			7		ns
Width of preset pulse, $t_{w(preset)}$			7			7		ns
Width of clear pulse, $t_{w(clear)}$			7			7		ns
Input setup time, t_{setup}	High-level data		10			10		ns
	Low-level data		12			12		ns
Input hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA					−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8, I_{OH} = −1 mA		SN54S74	2.5	3.4		V
				SN74S74	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8, I_{OL} = 20 mA					0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V	D input				50	μA
			Clock or Preset				100	
			Clear				150	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V	D input				−2	mA
			Clock or Preset				−4	
			Clear				−6	
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 1				30		mA

5

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. See Figures 1 through 5 of the Series 54H/74H section for test circuits.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTE 1: I_{CC} is measured with outputs open, clock grounded, and J, K, preset, and clear at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS¶	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 280 Ω		90		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset			5		ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset			8		ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock			7		ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock			7		ns

¶Switching characteristic measurements are made utilizing the same test circuits as illustrated in Figures 6, 7, and 8 of the Series 54H/74H section, except that the input pulse rise and fall times (shown as ⩽ 7 ns) are ⩽ 2.5 ns. Information in the notes of these figures is applicable except as follows:

In Figures 7 and 8: $t_{w(clock)}$ = 10 ns.

In Figure 7: t_{setup} = 8 ns and t_w = 30 ns.

In Figure 8: t_{setup} = 8 ns and t_w = 30 ns.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54S112, SN74S112
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

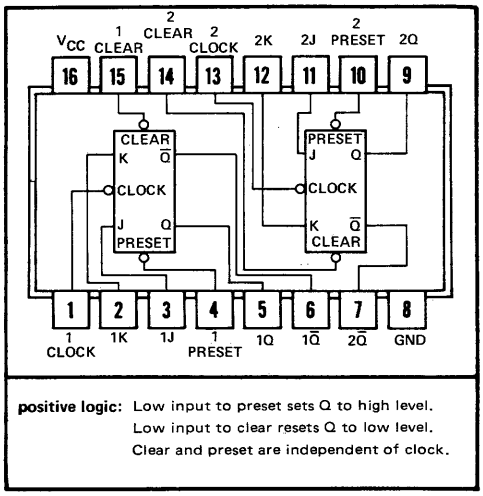
- Typical Maximum Input Clock Frequency . . . 125 MHz
- Fully D-C Coupled
- Typical Power Dissipation . . . 75 mW per Flip-Flop

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES: A. t_n = Bit time before clock pulse.
B. t_{n+1} = Bit time after clock pulse.

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to high level.
Low input to clear resets Q to low level.
Clear and preset are independent of clock.

5

description

These monolithic dual J-K flip-flops feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the truth table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

recommended operating conditions

		SN54S112			SN74S112			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		80	0		80	MHz
Width of clock pulse, $t_{w(clock)}$		6			6			ns
Width of preset pulse, $t_{w(preset)}$		8			8			ns
Width of clear pulse, $t_{w(clear)}$		8			8			ns
Input setup time, t_{setup} (see Note 1)		3			3			ns
Input hold time, t_{hold} (see Note 2)		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTES: 1. Setup time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −1 mA	SN54S112	2.5	3.4		V
				SN74S112	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V		J or K input			50	μA
				Clock, preset, or clear			100	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V		J or K input			−1.6	mA
				Clock			−4	
				Preset or clear			−7	
I_{OS}	Short-circuit output current§	V_{CC} = MAX,			−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3			30	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTE 3: I_{CC} is measured with outputs open, clock grounded, and J, K, preset, and clear at 4.5 V.

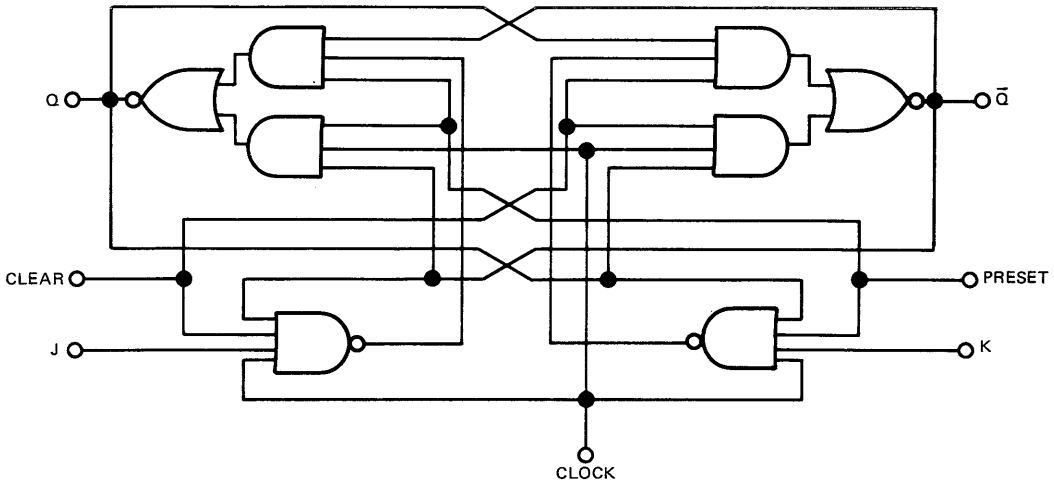
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS¶		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF,	R_L = 280 Ω	80	125		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset			2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset			2	5	7	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock			2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock			2	5	7	ns

¶Switching characteristic measurements are made utilizing the same test circuits as illustrated for Darlington outputs in Figures 77 and 78 of the Series 54H/74H section. Information in the notes of these figures pertaining to the SN74H108 is applicable for the SN74S112, except $t_1 = t_0$ = 2.5 ns for all input pulse characteristics and the steady-state J and K input voltages are 2.7 V instead of 2.4 V.

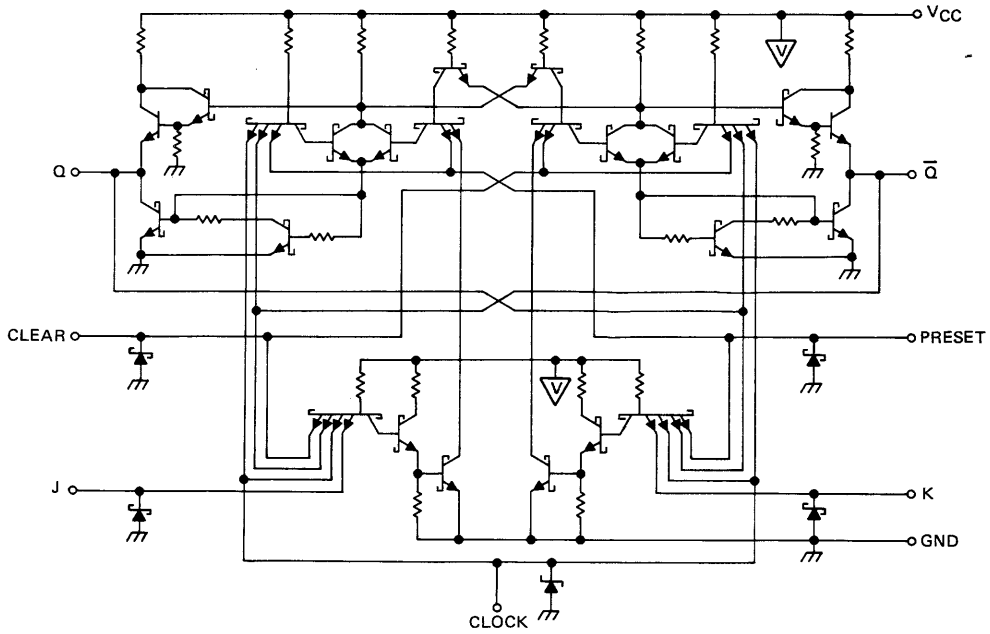
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram (each flip-flop)



5

schematic (each flip-flop)



▽ . . . V_{CC} bus

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

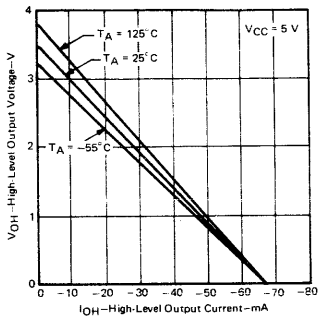


FIGURE 1

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

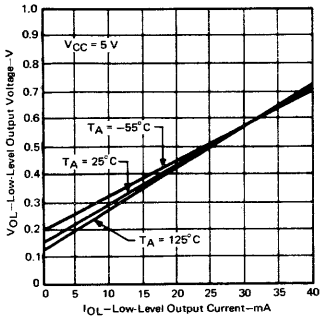


FIGURE 2

INPUT CURRENT
vs
INPUT VOLTAGE

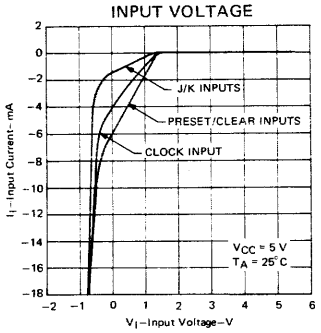


FIGURE 3

HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

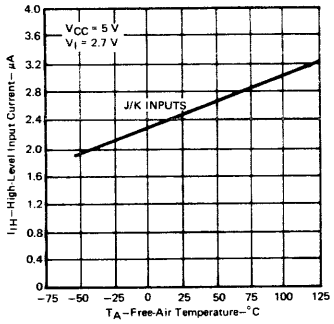


FIGURE 4

AVERAGE PROPAGATION DELAY TIME,
CLOCK TO OUTPUT
vs
FREE-AIR TEMPERATURE

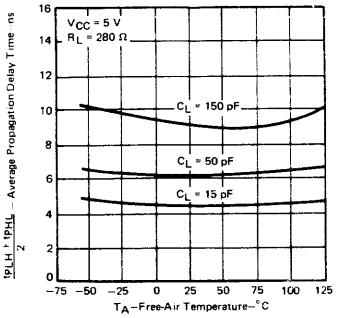


FIGURE 5

AVERAGE PROPAGATION DELAY TIME,
CLOCK TO OUTPUT
vs
LOAD CAPACITANCE

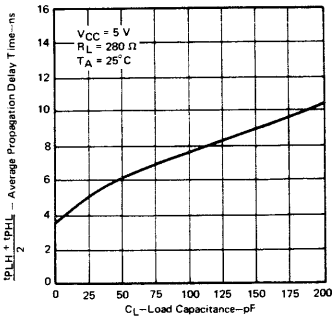


FIGURE 6

†Data for temperatures below 0°C and above 70°C is applicable to Series 54S circuits only.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54S113, SN54S114, SN74S113, SN74S114
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

Typical Maximum Input Clock Frequency . . . 125 MHz
Typical Power Dissipation . . . 75 mW per Flip-Flop

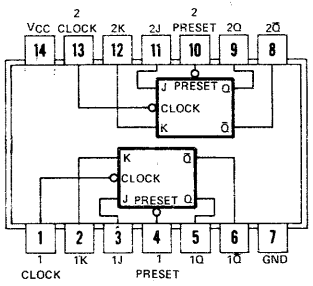
TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES: A. t_n = Bit time before clock pulse.
B. t_{n+1} = Bit time after clock pulse.

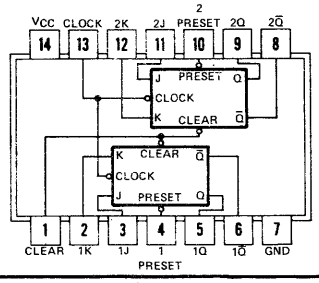
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)

SN54S113, SN74S113
DUAL PRESETTABLE FLIP-FLOPS



positive logic:
Low input to preset sets Q to high level
Preset is independent of clock

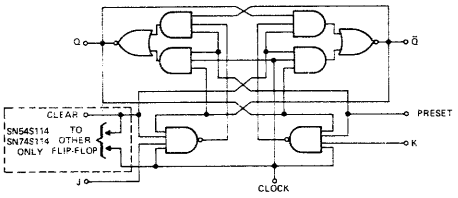
SN54S114, SN74S114
DUAL FLIP-FLOPS WITH
COMMON CLOCK AND CLEAR



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

5

functional block diagram (each flip-flop)



description

The SN54S113 and SN74S113 offer individual J, K, preset, and clock inputs. The SN54S114 and SN74S114 offer common clock and common clear inputs and individual J, K, and preset inputs.

These monolithic dual flip-flops are designed so that when the clock goes high, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

recommended operating conditions

		SN54S113 SN54S114			SN74S113 SN74S114			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		80	0		80	MHz
Width of clock pulse, $t_{w(clock)}$		6			6			ns
Width of preset pulse, $t_{w(preset)}$		8			8			ns
Width of clear pulse, $t_{w(clear)}$	SN54S114, SN74S114	8			8			ns
Input setup time, t_{setup}		3			3			ns
Input hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

CIRCUIT TYPES SN54S113, SN54S114, SN74S113, SN74S114
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN545113 SN74S113			SN54S114 SN74S114			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	Series 54S	2.5	3.4		2.5	3.4		V
			Series 74S	2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V	J or K input			50			50	μA
			Clock			100			200	
			Preset			100			100	
			Clear						200	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V	J or K input			−1.6			−1.6	mA
			Clock			−4			−8	
			Preset			−7			−7	
			Clear						−14	
I_{OS}	Short circuit output current§	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3		30	50		30	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. See Figures 64 through 69 of the Series 54H/74H section for test circuits.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTE 3: I_{CC} is measured with outputs open, clock grounded, and J, K, preset, and clear at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS¶	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 280 Ω	80	125		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset		2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset		2	5	7	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock		2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock		2	5	7	ns

¶ Switching characteristic measurements are made utilizing the same test circuits as illustrated for Darlington outputs in Figures 77 and 78 of the Series 54H/74H section. Information in the notes of these figures pertaining to the SN74H108 is applicable except $t_1 = t_0 = 2.5$ ns for all input pulse characteristics and the steady-state J and K input voltages are 2.7 V instead of 2.4 V.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Series 54/74
Circuits

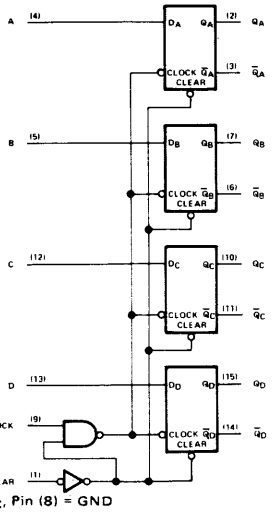
New TTL/MSI Now Available

SN54/74175 Quad and SN54/74174 HEX D-Type Flip-Flops With Direct Clear

- Replace latch circuits with clocked operation
- Reduce F-F Package count by 50 to 66
- Fully buffered inputs/outputs
- Economical for use as:
  - Buffer registers
  - Shift registers
  - Shift-register generators
  - Pattern generators
  - Scratch-pad memories

LOGIC

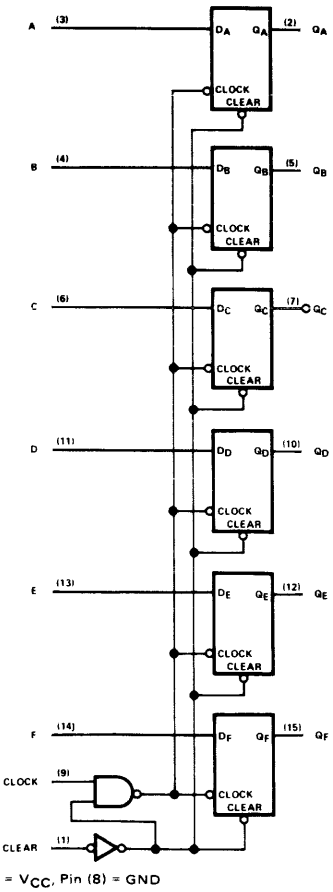
SN54175, SN74175



Pin (16) = V_{CC}, Pin (8) = GND

LOGIC

SN54174, SN74174



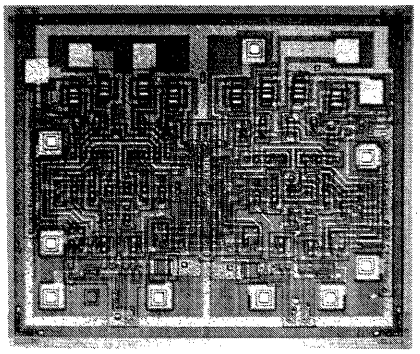
Pin (16) = V_{CC}, Pin (8) = GND

Available in 16-pin
J, N, and W packages

HIGH-SPEED SATURATED TRANSISTOR-TRANSISTOR LOGIC CIRCUITS FOR GENERAL-PURPOSE DIGITAL SYSTEM APPLICATIONS

description

TYPICAL DUAL FLIP-FLOP CIRCUIT BAR



Series 54/74 integrated circuits are designed and characterized for high-speed, general-purpose digital applications where high d-c noise margin and relatively low power dissipation are important system considerations. This logic series includes the basic gates, flip-flop elements, and complex logic and storage elements needed to perform all functions of general-purpose digital systems. Series 54 and 74 are completely compatible with Series 54H/74H, 54L/74L, and 54S/74S TTL logic families. Compatibility of these four TTL families permits improved systems design as the logician is permitted the flexibility of selecting component switching speed or circuit power dissipation with respect to system requirements. Series 54H/74H or 54S/74S high-speed TTL circuits can be selectively used to perform those functions requiring minimal propagation delay times. Series 54L/74L low-power TTL circuits can be used to reduce total power requirements. All four TTL families are designed to operate at the same supply voltages and compatible logic levels. In addition, high d-c noise margins characteristic of TTL circuits are maintained.

6

Definitive specifications are provided for operating characteristics over the full military temperature range of −55°C to 125°C for Series 54 circuits, and over the temperature range of 0°C to 70°C for Series 74 circuits.

features

LOW SYSTEM COST

- **choice of packages — ceramic flat package**
  — economical dual-in-line plastic package
  — ceramic dual-in-line package
- **broad selection of SSI and MSI functions — reduces package count**

OPTIMUM CIRCUIT PERFORMANCE

- **high speed — typical gate propagation delay time of 10 ns**
- **high d-c noise margin — typically one volt**
- **low output impedance provides low a-c noise susceptibility**
- **diode-clamped inputs simplify system design**
- **low power dissipation — 10 mW per gate at 50% duty cycle**
- **full fan-out —10 Series 54/74L loads**
  — 40 Series 54L/74L loads
  — 8 Series 54S/74S or 54H/74H loads
- **compatible for use with other current-sinking logic families — DTL, other TTL**
- **all inputs are diode clamped to minimize transmission-line effects**

SERIES 54/74
FEATURING 10 ns SPEED AND 10 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGES		PACKAGES*			
	–55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	SEC.-PAGE
NAND/NOR/AND/OR GATES AND BUFFERS						
Quadruple 2-Input Positive NAND Gates	SN5400	SN7400	J	N	W	6-5
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN5401	SN7401	J	N	W	6-6
Quadruple 2-Input Positive NOR Gates	SN5402	SN7402	J	N	W	6-9
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN5403	SN7403	J	N		6-10
Hex Inverters	SN5404	SN7404	J	N	W	6-11
Hex Inverters (with Open-Collector Output)	SN5405	SN7405	J	N	W	6-12
Hex Inverter Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5406	SN7406	J	N	W	6-13
Hex Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5407	SN7407	J	N	W	6-15
Quadruple 2-Input Positive AND Gates	SN5408	SN7408	J	N	W	6-17
Quadruple 2-Input Positive AND Gates	SN5409	SN7409	J	N	W	6-17
Triple 3-Input Positive NAND Gates	SN5410	SN7410	J	N	W	6-20
Triple 3-Input Positive NAND Gates (with Open-Collector Output)	SN5412	SN7412	J	N	W	6-21
Dual NAND Schmitt Triggers	SN5413	SN7413	J	N	W	6-22
Hex Inverter Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5416	SN7416	J	N	W	6-13
Hex Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5417	SN7417	J	N	W	6-15
Dual 4-Input Positive NAND Gates	SN5420	SN7420	J	N	W	6-26
Expandable Dual 4-Input Positive NOR Gates (with Strobe)	SN5423	SN7423	J	N	W	6-27
Dual 4-Input Positive NOR Gates	SN5425	SN7425	J	N	W	6-27
Quadruple 2-Input High-Voltage Interface NAND Gates	SN5426	SN7426	J	N		6-30
Triple 3-Input Positive NOR Gates	SN5427	SN7427	J	N	W	6-32
8-Input Positive NAND Gates	SN5430	SN7430	J	N	W	6-34
Quadruple 2-Input Positive OR Gates	SN5432	SN7432	J	N	W	6-35
Quadruple 2-Input Positive NAND Buffers	SN5437	SN7437	J	N	W	6-37
Quadruple 2-Input Positive NAND Buffers (with Open-Collector Output)	SN5438	SN7438	J	N	W	6-37
Dual 4-Input Positive NAND Buffers	SN5440	SN7440	J	N	W	6-39

SEE PAGES 9-1, 9-2, AND 9-3 FOR LISTING OF TTL MSI CIRCUITS

*For outline drawings of all packages, see Section 1.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES 54/74
FEATURING 10 ns SPEED AND 10 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGES		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
AND-OR-INVERT GATES						
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN5450	SN7450	J	N	W	6-40
Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN5451	SN7451	J	N	W	6-40
Expandable 4-Wide 2-Input AND-OR-INVERT Gates	SN5453	SN7453	J	N	W	6-42
4-Wide 2-Input AND-OR-INVERT Gates	SN5454	SN7454	J	N	W	6-42
EXPANDERS						
Dual 4-Input Expander	SN5460		J	N	W	6-44
Dual 4-Input Expander		SN7460	J	N	W	6-45
FLIP-FLOPS						
Positive Edge-Triggered J-K Flip-Flops (AND Inputs)	SN5470	SN7470	J	N	W	6-46
J-K Master-Slave Flip-Flops (AND Inputs)	SN5472	SN7472	J	N	W	6-49
Dual J-K Master-Slave Flip-Flops	SN5473	SN7473	J	N	W	6-52
Dual D-Type Edge-Triggered Flip-Flops	SN5474	SN7474	J	N	W	6-55
Dual-J-K Master-Slave Flip-Flops with Preset and Clear	SN5476	SN7476	J	N	W	6-58
Gated J-K Master-Slave Flip-Flops	SN54104	SN74104	J	N	W	6-61
Gated J-K Master-Slave Flip-Flops	SN54105	SN74105	J	N	W	6-61
Dual J-K Master-Slave Flip-Flops (V_{CC}-14, Gnd-7)	SN54107	SN74107	J	N		6-52
Gated J-K Master-Slave Flip-Flops with Data Lockout	SN54110	SN74110	J	N	W	6-66
Dual J-K Master-Slave Flip-Flops with Data Lockout	SN54111	SN74111	J	N	W	6-69
Monostable Multivibrators	SN54121	SN74121	J	N	W	6-72
Retriggerable Monostable Multivibrators with Clear	SN54122	SN74122	J	N	W	6-79
Dual Retriggerable Monostable Multivibrators with Clear	SN54123	SN74123	J	N	W	6-79

6

SEE PAGES 9-1, 9-2, AND 9-3 FOR LISTING OF TTL MSI CIRCUITS

*For outline drawings of all packages, see Section 1.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage, V_{in} (See Note 1)	5.5 V
Interemitter Voltage (See Note 2)	5.5 V
Resistor Node Voltage, SN54121, SN74121 (See Note 1)	−5.5 V to 7 V
Operating Free-Air Temperature Range: Series 54 Circuits	−55°C to 125°C
Series 74 Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

logic definition

Series 54/74 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

HIGH VOLTAGE = LOGICAL 1

LOW VOLTAGE = LOGICAL 0

input clamping diodes

Although not shown on all schematic diagrams, all of these SSI circuits incorporate input diodes. Each clamping diode is capable of limiting negative excursions at the input to a maximum of 1.5 volts below ground, even if −12 mA of current is drawn.

unused inputs of NAND/AND gates

6

For optimum switching times and minimum noise susceptibility, unused inputs should be maintained at a positive voltage greater than 2.4 V but not exceed the absolute maximum rating of 5.5 V. This eliminates the distributed capacitance associated with the floating input-transistor emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between 2.4 V and 3.5 V.
b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each input presents a full load in the logical 1 state to the driving output.
c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor.

input-current requirements

Input-current requirements reflect worst-case conditions over the specified recommended operating free-air temperature and V_{CC} ranges. Each input, of the multiple emitter input transistors which have a 4-kΩ base resistor, requires that no more than −1.6 mA flow out of the input at a logical 0 voltage level; therefore, one load (N = 1) is −1.6 mA maximum. Each input requires current into the input at a logical 1 voltage level. This current is 40 μA maximum for each emitter of input transistors with the 4-kΩ base resistor. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

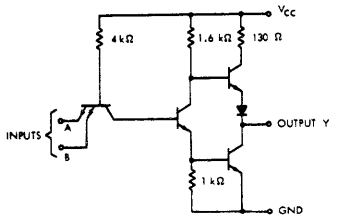
fan-out capability

Fan-out reflects the ability of an output to sink current from a number of loads (N) at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each standard output is capable of sinking current or supplying current to 10 loads (N = 10). The buffer gate is capable of sinking current or supplying current to 30 loads (N = 30). Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuits indicate the actual direction of current flow.

Series 54/74 circuits are well suited for driving Series 54H/74H and 54S/74S high-speed TTL and Series 54L/74L low-power TTL circuits. As examples, a Series 54/74 output, rated for a fan-out of ten (N=10), will drive eight 54H/74H loads or forty 54/74L loads.

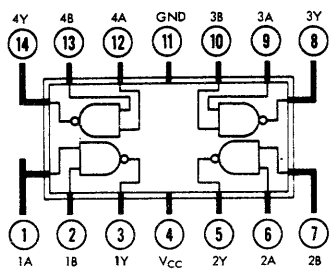
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

schematic (each gate)

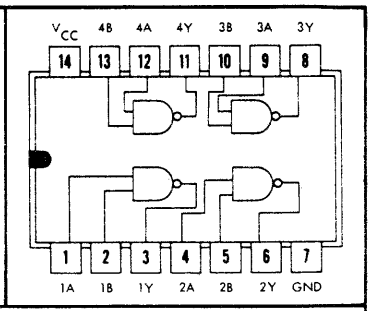


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5400 Circuits	4.5	5	5.5	V
SN7400 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5400 Circuits	−55	25	125	°C
SN7400 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 level at output	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN5400	−20		−55	mA
				SN7400	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			4	8	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		7	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		11	22	ns

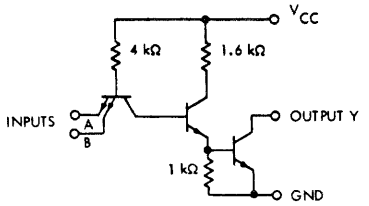
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

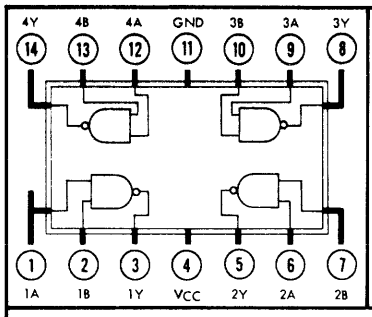
CIRCUIT TYPES SN5401, SN7401
QUADRUPLE 2-INPUT POSITIVE NAND GATES
(WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)

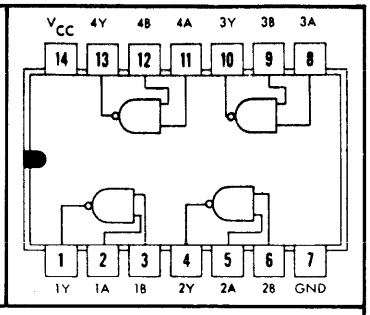


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5401 Circuits	4.5	5	5.5	V
SN7401 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5401 Circuits	−55	25	125	°C
SN7401 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7					0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, $V_{out(1)}$ = 5.5 V	V_{in} = 0.8 V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, I_{sink} = 16 mA	V_{in} = 2 V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX,	V_{in} = 5 V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX,	V_{in} = 0		4	8	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF,	R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF,	R_L = 4 kΩ		35	45	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), can be paralleled with other similar TTL gates to perform the wire-AND function, and simultaneously, will drive from one to nine Series 54 TTL loads. When no other open-collector gates are paralleled, this gate can be used to drive ten TTL loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available during a logical 1 level at output. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the logical 0 level even if one of the paralleled outputs is sinking all the current.

In both conditions (logical 0 and logical 1) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where: V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

logical 1 (off level) circuit calculations (see figure F)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the $V_{out(1)}$ level required at the load:

$$V_{RL} = V_{CC} - V_{out(1)\ required}$$

The total current through the load resistor (I_{RL} is the sum of the load currents ($I_{in(1)}$) and off-level reverse currents ($I_{out(1)}$ through each of the wire-AND connected outputs:

$$I_{RL} = \eta \cdot I_{out(1)} + N \cdot I_{in(1)} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{out(1)\ required}}{\eta \cdot I_{out(1)} + N \cdot I_{in(1)}}$$

where: η = number of gates wire-AND connected, and N = number of TTL loads.

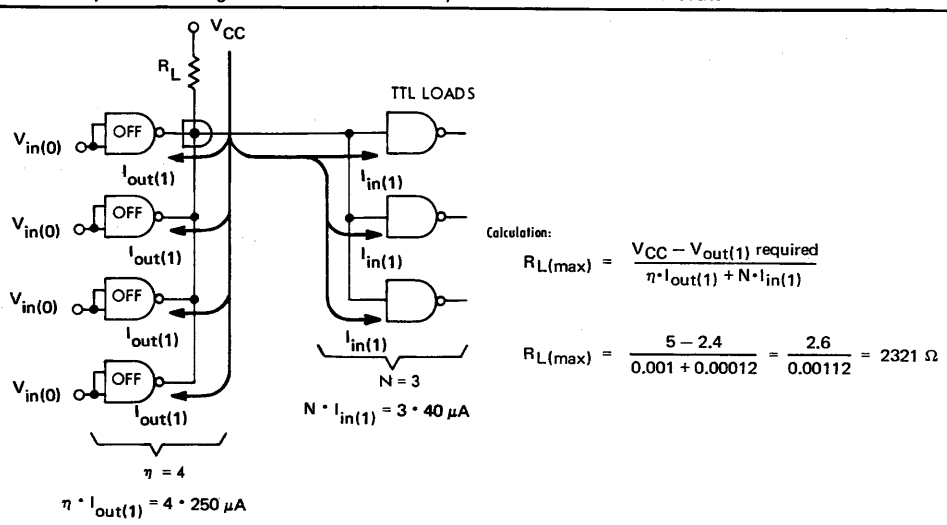


FIGURE F – LOGICAL 1 CIRCUIT CONDITIONS

APPLICATION DATA

logical 0 (on level) circuit calculations (see figure G)

The current through the resistor must be limited to the maximum sink-current capability of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during logical 0 periods, the current must be limited to 16 mA, the maximum current which will ensure a logical 0 maximum of 0.4 volts.

Also, fan-out must be considered. Part of the 16 mA will be supplied from the inputs which are being driven. This reduces the amount of current allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L is:

$$R_{L(min)} = \frac{V_{CC} - V_{out(0)\ required}}{I_{sink\ capability} - I_{sink\ from\ TTL\ loads}}$$

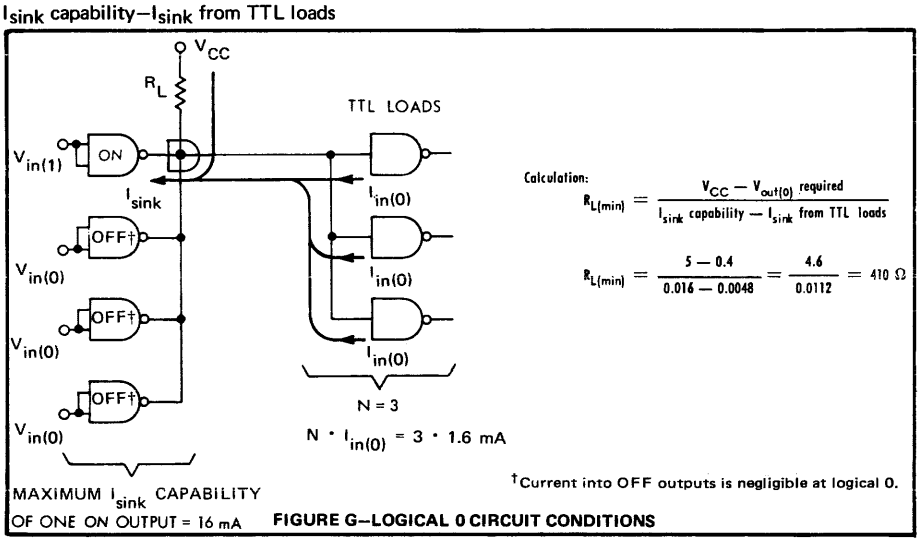


FIGURE G–LOGICAL 0 CIRCUIT CONDITIONS

driving TTL loads and combining outputs

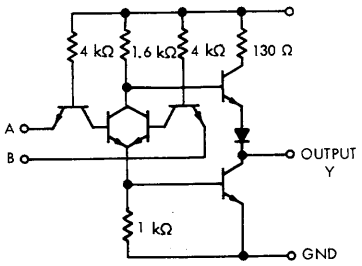
Table I provides minimum and maximum resistor values, calculated from equations shown above, for driving one to ten TTL loads and wire-AND connecting two to seven parallel outputs. Each value shown for one wire-AND output is determined by the fan-out plus the cutoff current of a single output transistor. Extension beyond seven wire-AND connections is permitted with fan-outs of seven or fewer if a valid minimum and maximum R_L is possible. When fanning-out to ten TTL loads, the calculation for the minimum value of R_L indicates that an infinite resistance should be used ($V_{RL} \div 0 = \infty$); however, the use of a 4 kΩ resistor in this case will satisfy the logical 1 condition and limit the logical 0 level to less than 0.43 V.

FAN-OUT TO TTL LOADS	WIRE-AND OUTPUTS							
	1	2	3	4	5	6	7	1 to 7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000§
	MAXIMUM							MIN

TABLE 1–LOAD RESISTOR VALUE IN OHMS

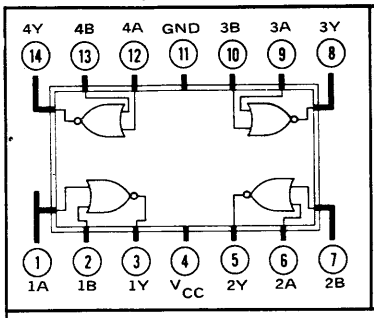
‡ All values shown in the table are based on:
Logical 1 conditions: V_{CC} = 5 V, $V_{out(1)}$ required = 2.4 V
Logical 0 conditions: V_{CC} = 5 V, $V_{out(0)}$ required = 0.4 V
§ – The theoretical value is ∞. See explanation in text.
X – Not recommended or not possible.

schematic (each gate)

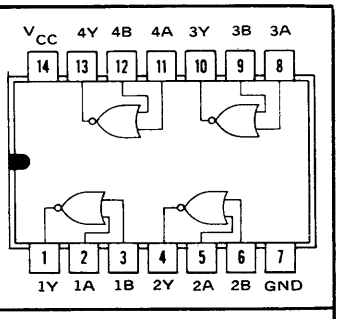


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N-DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{A + B}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5402 Circuits	4.5	5	5.5	V
	SN7402 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5402 Circuits	−55	25	125	°C
	SN7402 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	8			2			V
$V_{in(0)}$	Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	9					0.8	V
$V_{out(1)}$	Logical 1 output voltage	9	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	10	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	11	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	12	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	13	V_{CC} = MAX	SN5402	−20		−55	mA
				SN7402	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	14	V_{CC} = MAX, V_{in} = 5 V			14	27	mA
$I_{CC(1)}$	Logical 1 level supply current	14	V_{CC} = MAX, V_{in} = 0			8	16	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		12	22	ns

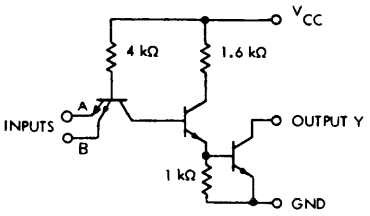
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

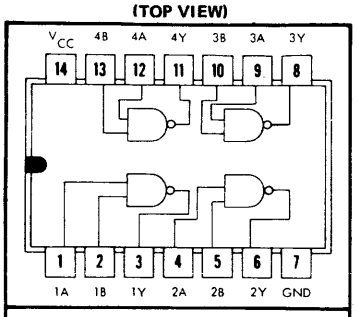
CIRCUIT TYPES SN5403, SN7403
QUADRUPLE 2-INPUT POSITIVE NAND GATES
(WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)



NOTE: Component values shown are nominal.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5403 Circuits	4.5	5	5.5	V
SN7403 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N (and see pages 2-7 and 2-8)			10	
Operating Free-Air Temperature Range, T_A: SN5403 Circuits	−55	25	125	°C
SN7403 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7				0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		4	8	mA

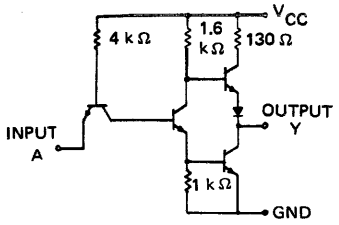
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 4 kΩ		35	45	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

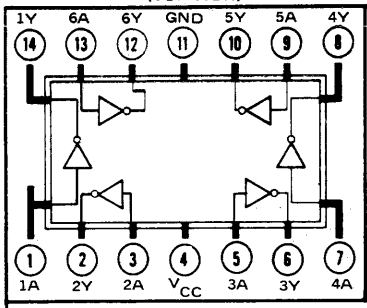
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

schematic (each inverter)

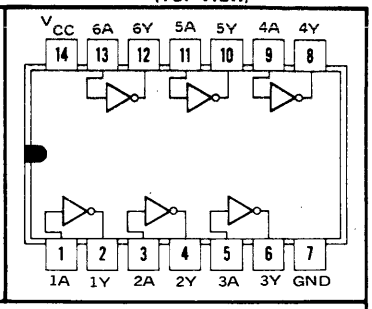


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \bar{A}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5404 Circuits	4.5	5	5.5	V
SN7404 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5404 Circuits	−55	25	125	°C
SN7404 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	15			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	16					0.8	V
$V_{out(1)}$	Logical 1 output voltage	16	V_{CC} = MIN, I_{load} = −400 μA	V_{in} = 0.8 V,	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	15	V_{CC} = MIN, I_{sink} = 16 mA	V_{in} = 2 V,		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current	18	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current	18	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current§	19	V_{CC} = MAX	SN5404	−20		−55	mA
				SN7404	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	20	V_{CC} = MAX,	V_{in} = 5 V		18	33	mA
$I_{CC(1)}$	Logical 1 level supply current	20	V_{CC} = MAX,	V_{in} = 0		6	12	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF,	R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF,	R_L = 400 Ω		12	22	ns

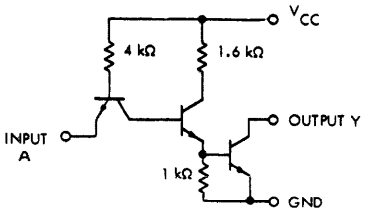
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

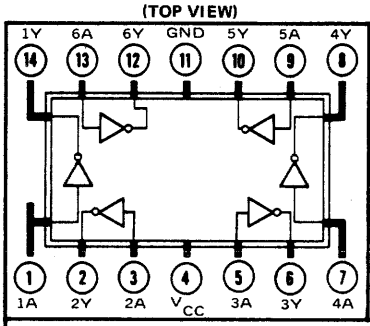
CIRCUIT TYPES SN5405, SN7405
HEX INVERTERS (WITH OPEN-COLLECTOR OUTPUT)

schematic (each inverter)

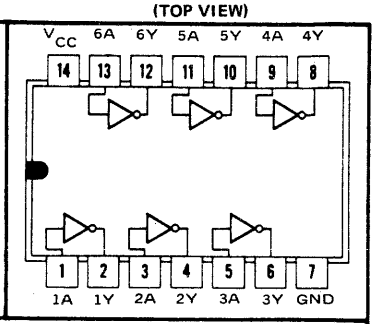


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic $Y = \overline{A}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5405 Circuits	4.5	5	5.5	V
SN7405 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N (and see pages 2-7 and 2-8)			10	
Operating Free-Air Temperature Range, T_A: SN5405 Circuits	−55	25	125	°C
SN7405 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 (on) level at output	15		2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 (off) level at output	17				0.8	V
$I_{out(1)}$	Output reverse current	17	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	15	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current	18	V_{CC} = MAX, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current	18	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	20	V_{CC} = MAX, V_{in} = 5 V, T_A = 25°C		18	33	mA
$I_{CC(1)}$	Logical 1 level supply current	20	V_{CC} = MAX, V_{in} = 0, T_A = 25°C		6	12	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 4 kΩ		40	55	ns

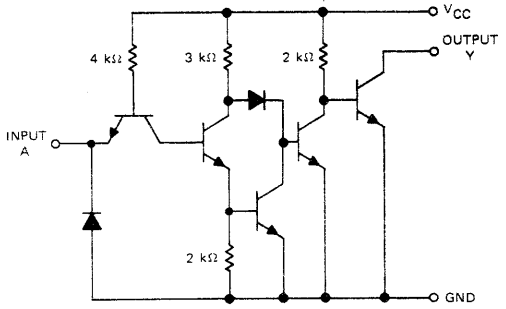
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ These typical values are at V_{CC} = 5 V, T_A = 25°C.

CIRCUIT TYPES SN5406, SN5416, SN7406, SN7416
HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

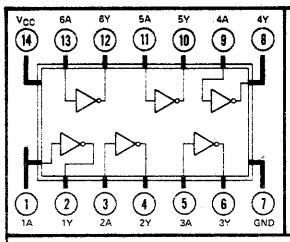
FOR INTERFACING WITH HIGH-LEVEL CIRCUITS OR FOR DRIVING HIGH-CURRENT LOADS

schematic (each inverter)

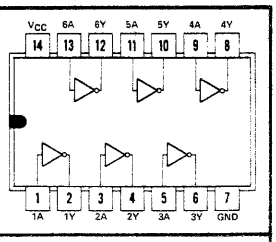


NOTE: Component values shown are nominal.

W
FLAT PACKAGE
(TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{A}$

- **Converts TTL voltage levels to MOS levels**
- **High sink-current capability**
- **Input clamping diodes simplify system design**
- **Typical propagation delay time: 15 ns**
- **Open-collector driver for indicator lamps and relays**
- **Inputs fully compatible with most TTL and DTL circuits**
- **Typical power dissipation: 105 mW**

6

description

These monolithic TTL hex inverter buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS), or for driving high-current loads (such as lamps or relays), and are also characterized for use as inverter buffers for driving TTL inputs. For increased fan-out, several inverters in a single package may be paralleled. The SN5406 and SN7406 have minimum breakdown voltages of 30 volts and the SN5416 and SN7416 have minimum breakdown voltages of 15 volts. The maximum sink current is 30 milliamperes for the SN5406 and SN5416, and 40 milliamperes for the SN7406 and SN7416.

These circuits are completely compatible with most TTL or DTL families. Inputs are diode-clamped to minimize transmission-line effects which simplifies design. Typical power dissipation is 150 milliwatts and average propagation delay time is 15 nanoseconds. The SN5406 and SN5416 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN7406 and SN7416 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Output voltage (see Notes 1 and 2):	SN5406, SN7406 Circuits	30 V
	SN5416, SN7416 Circuits	15 V
Operating free-air temperature range:	SN5406, SN5416 Circuits	−55°C to 125°C
	SN7406, SN7416 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

		SN5406, SN5416			SN7406, SN7416			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}	SN5406, SN7406			30			30	V
	SN5416, SN7416			15			15	
Low-level output current, I_{OL}				30			40	mA
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	74		2			V
V_{IL}	Low-level input voltage	75				0.8	V
I_{OH}	High-level output current	75	V_{CC} = MIN, V_I = 0.8 V, V_{OH} = MAX			250	μA
V_{OL}	Low-level output voltage	74	V_{CC} = MIN, V_I = 2 V, I_{OL} = MAX			0.7	V
			V_{CC} = MIN, V_I = 2 V, I_{OL} = 16 mA			0.4	
I_{IH}	High-level input current (each input)	76	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	77	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	78	V_{CC} = MAX, V_I = 0		30	42	mA
I_{CCL}	Supply current, low-level output	78	V_{CC} = MAX, V_I = 5 V		27	38	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

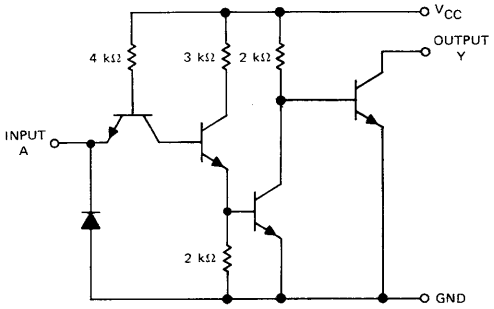
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	79	C_L = 15 pF, R_L = 110 Ω		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output	79	C_L = 15 pF, R_L = 110 Ω		15	23	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

CIRCUIT TYPES SN5407, SN5417, SN7407, SN7417
HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

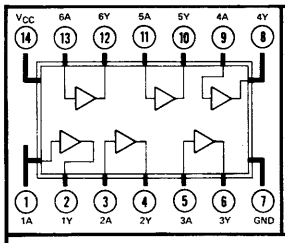
FOR INTERFACING WITH HIGH-LEVEL CIRCUITS
OR FOR DRIVING HIGH-CURRENT LOADS

schematic (each buffer/driver)

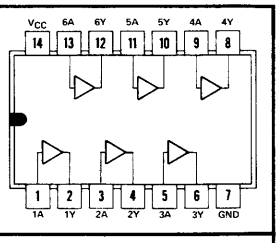


NOTE: Component values shown are nominal.

W
FLAT PACKAGE
(TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: Y = A

- **Converts TTL voltage levels to MOS levels**
- **High sink-current capability**
- **Input clamping diodes simplify system design**
- **Typical propagation delay time: 14 ns**
- **Open-collector driver for indicator lamps and relays**
- **Inputs fully compatible with most TTL and DTL circuits**
- **Typical power dissipation: 145 mW**

6

description

These monolithic TTL hex buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS), or for driving high-current loads (such as lamps or relays), and are also characterized for use as buffers for driving TTL inputs. For increased fan-out, several buffers in a single package may be paralleled. The SN5407 and SN7407 have minimum breakdown voltages of 30 volts and the SN5417 and SN7417 have minimum breakdown voltages of 15 volts. The maximum sink current is 30 milliamperes for the SN5407 and SN5417, and 40 milliamperes for the SN7407 and SN7417.

These circuits are completely compatible with most TTL and DTL families. Inputs are diode-clamped to minimize transmission-line effects which simplifies design. Typical power dissipation is 145 milliwatts and average propagation delay time is 14 nanoseconds. The SN5407 and SN5417 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN7407 and SN7417 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Output voltage (see Notes 1 and 2):	SN5407, SN7407 Circuits	30 V
	SN5417, SN7417 Circuits	15 V
Operating free-air temperature range:	SN5407, SN5417 Circuits	−55°C to 125°C
	SN7407, SN7417 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

		SN5407, SN5417			SN7407, SN7417			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}	SN5407, SN7407			30			30	V
	SN5417, SN7417			15			15	
Low-level output current, I_{OL}				30			40	mA
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	80		2			V
V_{IL}	Low-level input voltage	81				0.8	V
I_{OH}	High-level output current	80	V_{CC} = MIN, V_I = 2 V, V_{OH} = MAX			250	μA
V_{OL}	Low-level output voltage	81	V_{CC} = MIN, V_I = 0.8 V, I_{OL} = MAX			0.7	V
			V_{CC} = MIN, V_I = 0.8 V, I_{OL} = 16 mA			0.4	
I_{IH}	High-level input current (each input)	82	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	83	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	84	V_{CC} = MAX, V_I = 5 V		29	41	mA
I_{CCL}	Supply current, low-level output	84	V_{CC} = MAX, V_I = 0		21	30	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

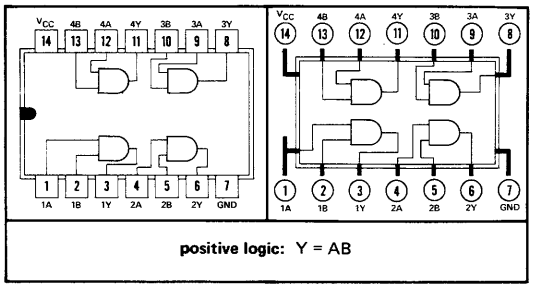
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	85	C_L = 15 pF, R_L = 110 Ω		6	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output	85	C_L = 15 pF, R_L = 110 Ω		20	30	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

Choice of Totem-Pole Outputs (SN5408/SN7408) or Open-Collector Outputs (SN5409/SN7409)

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)

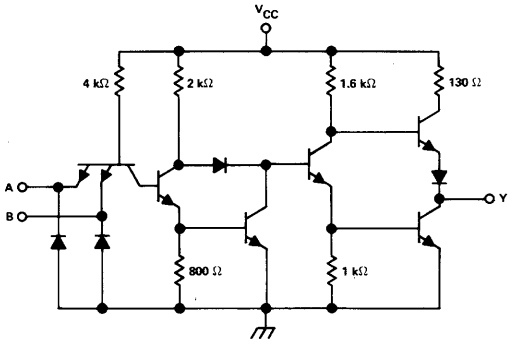
W
FLAT PACKAGE
(TOP VIEW)



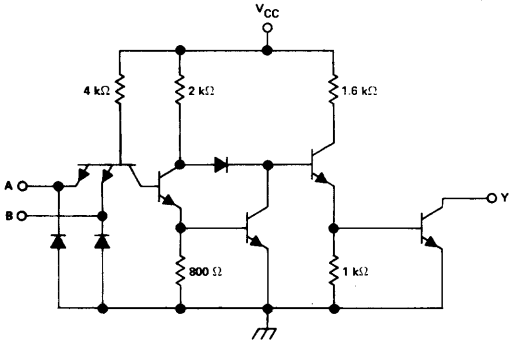
positive logic: Y = AB

schematics (each gate)

SN5408, SN7408



SN5409, SN7409



Component values shown are nominal.

description

These Series 54/74 TTL gates provide the system designer with direct implementation of the positive AND or negative OR functions.

The SN5408/SN7408, with totem-pole outputs, drives 10 normalized Series 54/74 loads at the low output level and 20 loads at the high output level. The SN5409/SN7409, with open-collector output, provides additional logic flexibility, as the outputs may be wire-AND connected to extend the AND function. The SN5409/SN7409 will sink sufficient current to drive 10 normalized Series 54/74 loads at the low output level.

The SN5408 and SN5409 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN7408 and SN7409 are characterized for operation from 0°C to 70°C.

CIRCUIT TYPES SN5408, SN5409, SN7408, SN7409
QUADRUPLE 2-INPUT POSITIVE AND GATES

SN5408, SN7408

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range, T_A: SN5408 Circuits . . . . . −55°C to 125°C
SN7408 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

	SN5408			SN7408			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN5408, SN7408 MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	86			2			V
V_{IL}	Low-level input voltage	88					0.8	V
V_{OH}	High-level output voltage	86	V_{CC} = MIN, I_{OH} = −800 μA	V_{IH} = 2 V,	2.4			V
V_{OL}	Low-level output voltage	88	V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,			0.4	V
I_{IH}	High-level input current (each input)	89	V_{CC} = MAX,	V_I = 2.4 V			40	μA
			V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	90	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	91	V_{CC} = MAX	SN5408	−20		−55	mA
				SN7408	−18		−55	
I_{CCH}	Supply current, high-level output	92	V_{CC} = MAX,	V_I = 5 V		11	21	mA
I_{CCL}	Supply current, low-level output	92	V_{CC} = MAX,	V_I = 0		20	33	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN5408, SN7408 MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	93	C_L = 15 pF, R_L = 400 Ω		17.5	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output				12	19	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

SN5409, SN7409

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Output voltage (see Notes 1 and 3) . . . . . 5.5 V
Operating free-air temperature range: SN5409 Circuits . . . . . −55°C to 125°C
SN7409 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

	SN5409			SN7409			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	SN5409, SN7409			UNIT
				MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	87		2			V
V_{IL}	Low-level input voltage	88				0.8	V
I_{OH}	High-level output current	87	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 5.5 V			250	μA
V_{OL}	Low-level output voltage	88	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4	V
I_{IH}	High-level input current (each input)	89	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	90	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	92	V_{CC} = MAX, V_I = 5 V		11	21	mA
I_{CCL}	Supply current, low-level output	92	V_{CC} = MAX, V_I = 0		20	33	mA

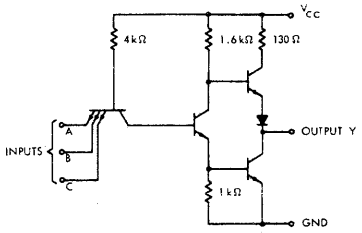
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN5409, SN7409			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	93	C_L = 15 pF, R_L = 400 Ω		21	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output				16	24	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

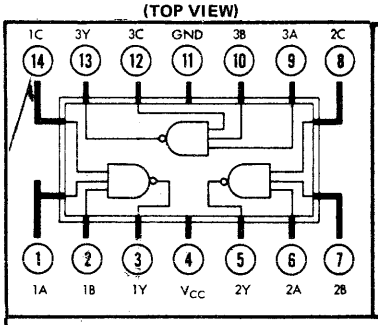
CIRCUIT TYPES SN5410, SN7410
TRIPLE 3-INPUT POSITIVE NAND GATES

schematic (each gate)

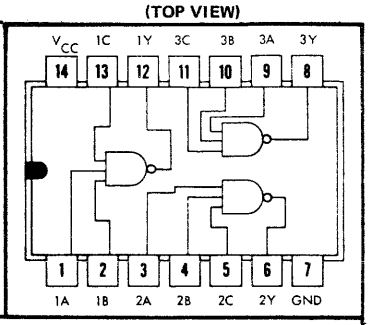


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{ABC}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5410 Circuits	4.5	5	5.5	V
	SN7410 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5410 Circuits	−55	25	125	°C
	SN7410 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, I_{load} = −400 μA	V_{in} = 0.8 V,	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, I_{sink} = 16 mA	V_{in} = 2 V,		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short circuit output current§	5	V_{CC} = 5.5 V	SN5410	−20		−55	mA
				SN7410	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX,	V_{in} = 5 V		9	16.5	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX,	V_{in} = 0		3	6	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF,	R_L = 400 Ω		7	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF,	R_L = 400 Ω		11	22	ns

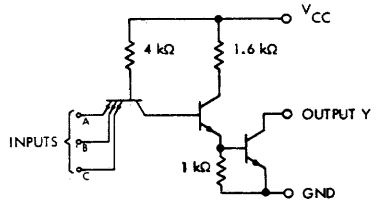
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

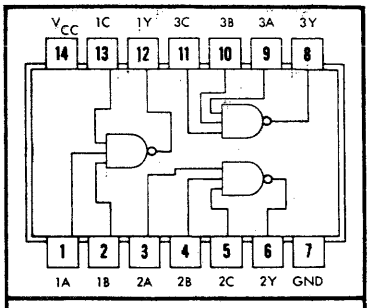
CIRCUIT TYPES SN5412, SN7412
TRIPLE 3-INPUT POSITIVE NAND GATES
(WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)



NOTE: Component values shown are nominal.

J OR N DUAL-IN-LINE OR
W FLAT PACKAGES (TOP VIEW)



positive logic: $Y = \overline{ABC}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5412 Circuits	4.5	5	5.5	V
	SN7412 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5412 Circuits	−55	25	125	°C
	SN7412 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7				0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, $V_{in(0)}$ = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V		9	16.5	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		3	6	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

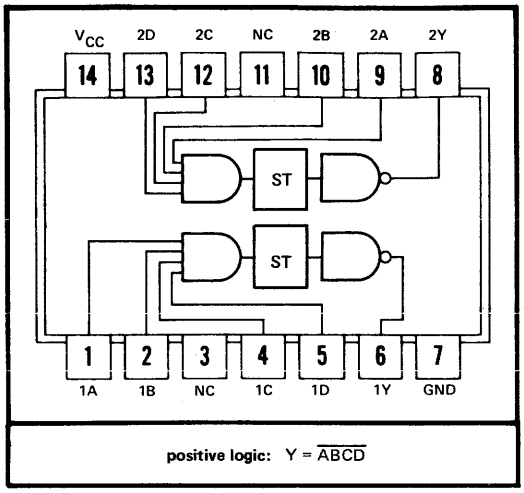
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 4 kΩ		35	45	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating condionts for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

CIRCUIT TYPES SN5413,SN7413
DUAL NAND SCHMITT TRIGGERS

- Operation from Very Slow Edges
- Temperature-Compensated Threshold Levels
- Temperature-Compensated Hysteresis, Typically 0.8 V
- High Noise Immunity

J OR N DUAL-IN-LINE OR
W FLAT PACKAGES (TOP VIEW)†



NC—No internal connection.
†Pin assignments for these circuits are the same for all packages.

description

6

The SN5413 and SN7413 dual Schmitt triggers consist of two identical Schmitt-trigger circuits in monolithic integrated circuit form. Logically, each circuit functions as a four-input NAND gate, but because of the Schmitt action, the gate has different input threshold levels for positive- and negative-going signals. The hysteresis, or backlash, which is the difference between the two threshold levels, is typically 800 mV.

An important design feature is the built-in temperature compensation which ensures very high stability of the threshold levels and the hysteresis over a very wide temperature range. Typically, the hysteresis changes by 3% over the temperature range of −55°C to 125°C and the upper threshold changes by 1% over the same range. The SN5413/SN7413 can be triggered from the slowest of input ramps and still give clean, jitter-free output signals. It can also be triggered from straight d-c levels.

These circuits are fully compatible with most other TTL, DTL, or MSI circuits. The SN5413 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN7413 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Interemitter voltage (see Note 2)		5.5 V
Operating free-air temperature range:	SN5413 Circuits	−55°C to 125°C
	SN7413 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

		SN5413			SN7413			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	0	125	0	25	70	°C
Maximum input rise and fall times		No restriction			No restriction			

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{T+}	Positive-going threshold voltage	94	V_{CC} = 5 V	1.5	1.7	2	V
V_{T-}	Negative-going threshold voltage	95	V_{CC} = 5 V	0.6	0.9	1.1	V
$V_{T+}-V_{T-}$	Hysteresis	94 & 95	V_{CC} = 5 V	0.4	0.8		V
V_I	Input clamp voltage	97	V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	95	V_{CC} = MIN, V_I = 0.6 V, I_{OH} = −800 μA	2.4	3.3		V
V_{OL}	Low-level output voltage	94	V_{CC} = MIN, V_I = 2 V, I_{OL} = 16 mA		0.22	0.4	V
I_{T+}	Input current at positive-going threshold	94	V_{CC} = 5 V, $V_I = V_{T+}$		−0.65		mA
I_{T-}	Input current at negative-going threshold	95	V_{CC} = 5 V, $V_I = V_{T-}$		−0.85		mA
I_I	Input current at maximum input voltage	96	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	96	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	97	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6	mA
I_{OS}	Short-circuit output current§	98	V_{CC} = MAX	−18		−55	mA
I_{CCH}	Supply current, high-level output	99	V_{CC} = MAX, V_I = 0		14	23	mA
I_{CCL}	Supply current, low-level output	99	V_{CC} = MAX, V_I = 4.5 V		20	32	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

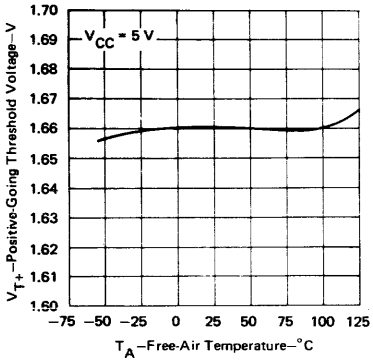
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	100	C_L = 15 pF, R_L = 400 Ω		18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output	100	C_L = 15 pF, R_L = 400 Ω		15	22	ns

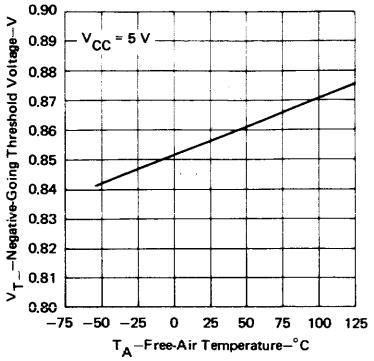
6

TYPICAL CHARACTERISTICS

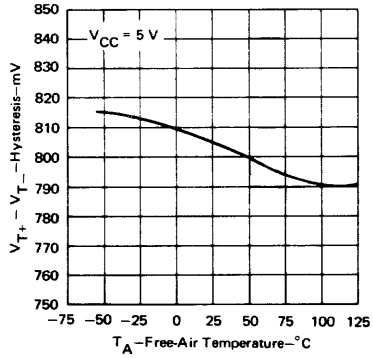
POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



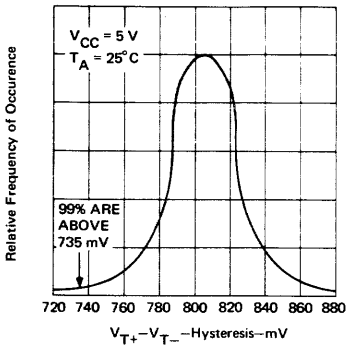
NEGATIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



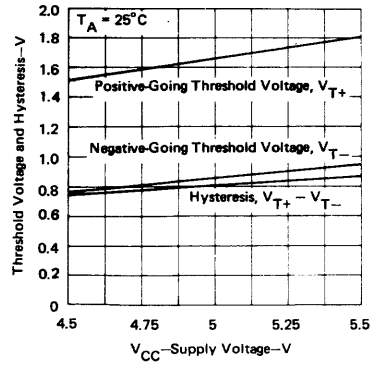
HYSTERESIS
vs
FREE-AIR TEMPERATURE



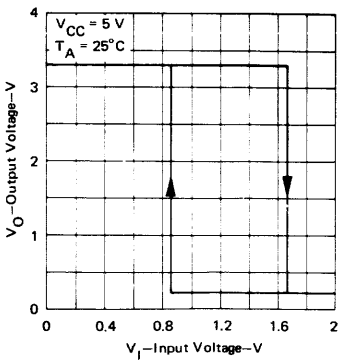
DISTRIBUTION OF UNITS
FOR HYSTERESIS



THRESHOLD VOLTAGES AND HYSTERESIS
vs
SUPPLY VOLTAGE

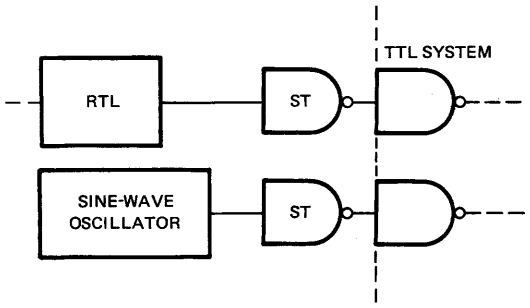


OUTPUT VOLTAGE
vs
INPUT VOLTAGE

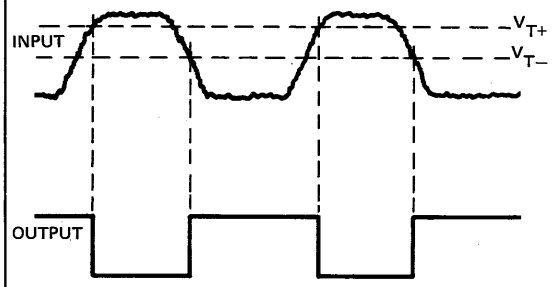


6

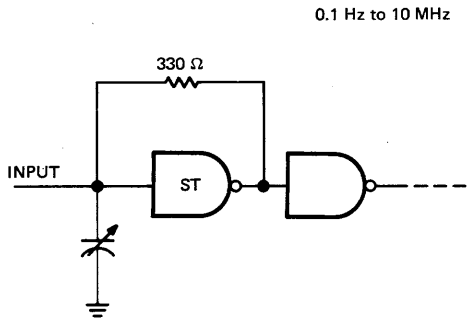
TYPICAL APPLICATION DATA



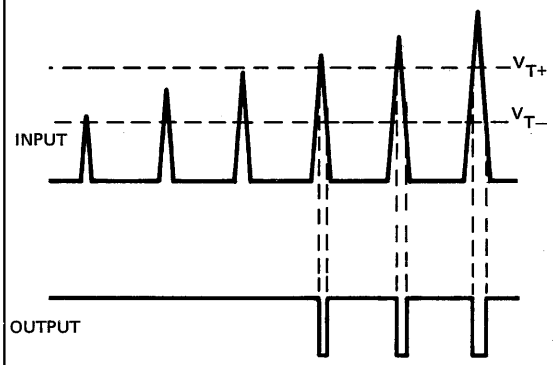
TTL SYSTEM INTERFACE
FOR SLOW INPUT WAVEFORMS



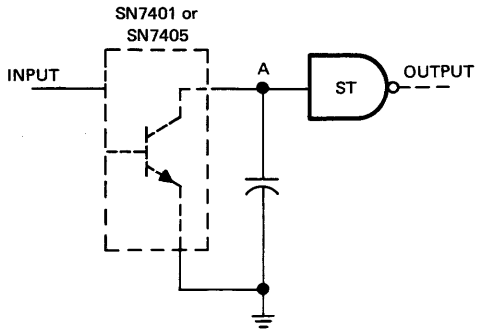
PULSE SHAPER

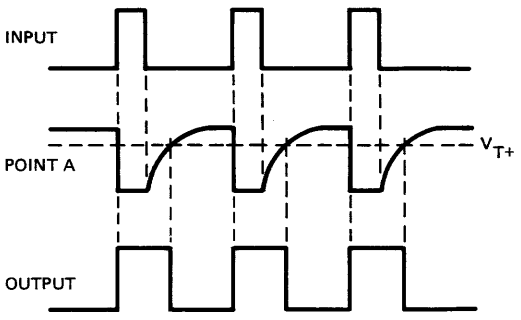


MULTIVIBRATOR



THRESHOLD DETECTOR



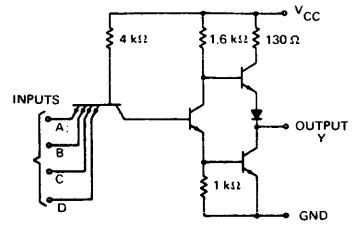


PULSE STRETCHER

6

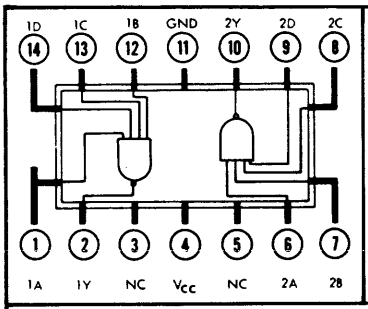
CIRCUIT TYPES SN5420, SN7420
DUAL 4-INPUT POSITIVE NAND GATES

schematic (each gate)

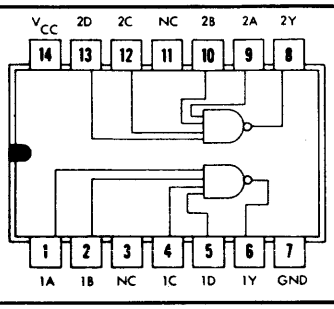


Component values shown are nominal.
NC—No Internal Connection

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{ABCD}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5420 Circuits	4.5	5	5.5	V
	SN7420 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5420 Circuits	−55	25	125	°C
	SN7420 Circuits	0	25	70	°C

6

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN5420	−20		−55	mA
				SN7420	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			6	11	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			2	4	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

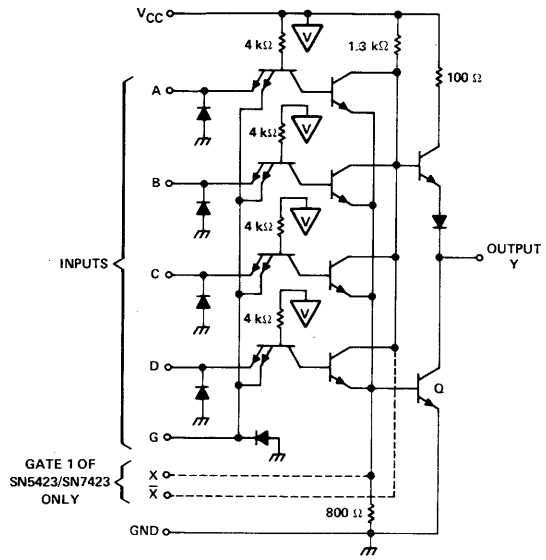
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		12	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

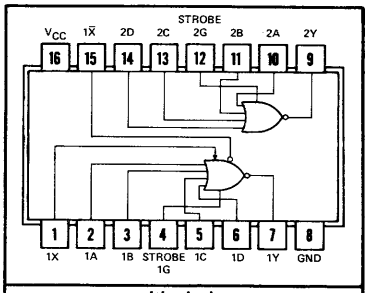
schematic (each gate)



NOTES: A. Component values shown are nominal.
B. Both expander inputs are used simultaneously for expanding.
C. If expander is not used leave X and $\overline{X}$ open.
D. A total of four expander gates can be connected to the expander inputs.

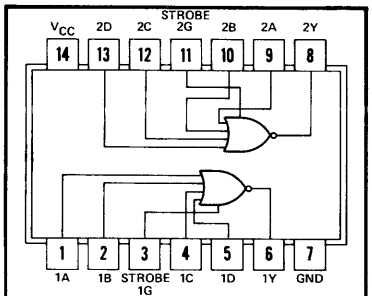
▽ $-V_{CC}$ bus

SN5423, SN7423
J OR N DUAL-IN-LINE OR
W FLAT PACKAGES (TOP VIEW)†



positive logic:
$1Y = \overline{1G(1A+1B+1C+1D)+X}$
$2Y = \overline{2G(2A+2B+2C+2D)}$
X = output of SN5460/SN7460

SN5425, SN7425
J OR N DUAL-IN-LINE OR
W FLAT PACKAGES (TOP VIEW)†



positive logic:
$Y = \overline{G(A+B+C+D)}$

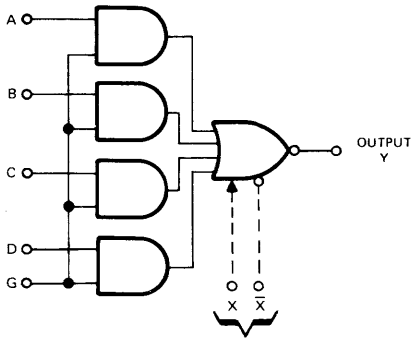
†Pin assignments for these circuits are the same for all packages.

logic and functional block diagram (each gate)

TRUTH TABLE

INPUTS					OUTPUT
A	B	C	D	G	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	X	H
X	X	X	X	L	H

Expander inputs are open.
H = high level, L = low level, X = irrelevant



6

CIRCUIT TYPES SN5423, SN5425, SN7423, SN7425
DUAL 4-INPUT NOR GATES WITH STROBE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5423, SN5425 Circuits . . . . . −55°C to 125°C
SN7423, SN7425 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

		SN5423, SN5425			SN7423, SN7425			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −800 μA	V_{IL} = 0.8 V,	2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = 16 mA	V_{IH} = 2 V,		0.22	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	data inputs	V_{CC} = MAX,	V_I = 2.4 V			40	μA
		strobe inputs					160	
I_{IL}	Low-level input current	data inputs	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
		strobe inputs					−6.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−55	mA
I_{CCH}	Supply current, high-level output		V_{CC} = MAX,	All inputs at 0 V		8	16	mA
I_{CCL}	Supply current, low-level output		V_{CC} = MAX,	All inputs at 5 V		10	19	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and $\overline{X}$ are open.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

electrical characteristics (SN5423 circuits) using expander inputs, V_{CC} = 4.5 V, T_A = −55°C

PARAMETER		TEST FIGURE¶	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{OL} = 16 mA			2.9	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{OL} = 16 mA, I_1 = 0.41 mA, R_1 = 0			1	V
V_{OH}	High-level output voltage	30	I_{OH} = −400 μA, I_1 = 0.15 mA, I_2 = −0.15 mA	2.4	3.3		V
V_{OL}	Low-level output voltage	29	I_{OL} = 16 mA, I_1 = 0.3 mA, R_1 = 138 Ω		0.22	0.4	V

electrical characteristics (SN7423 circuits) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		TEST FIGURE¶	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{OL} = 16 mA			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{OL} = 16 mA, I_1 = 0.62 mA, R_1 = 0			1	V
V_{OH}	High-level output voltage	30	I_{OH} = −400 μA, I_1 = 270 μA, I_2 = −270 μA	2.4	3.3		V
V_{OL}	Low-level output voltage	29	I_{OL} = 16 mA, I_1 = 0.43 mA, R_1 = 130 Ω		0.22	0.4	V

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Referenced test figures appear on page 2-49 of TTL Integrated Circuits Catalog (CC201).

6

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, (see note 3)

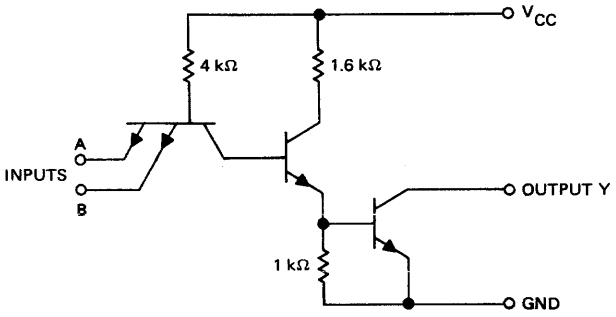
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 400 Ω		13	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 400 Ω		8	15	ns

NOTE 3: Switching characteristics of the SN5423 and SN7424 are tested with the expander pins open.

CIRCUIT TYPES SN5426, SN7426
QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE NAND GATES

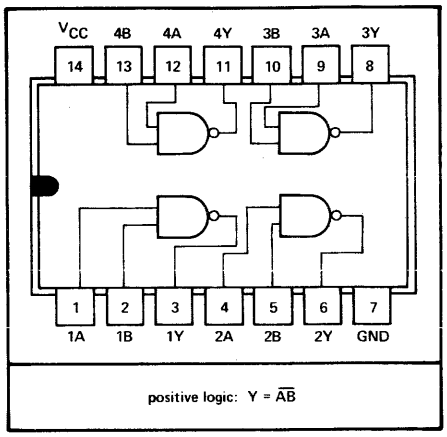
FOR DRIVING LOW-THRESHOLD-VOLTAGE MOS INPUTS

schematic (each gate)



Component values shown are nominal.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

These open-collector NAND gates feature high output voltage ratings for interfacing with low-threshold-voltage MOS logic circuits or other 12-volt systems. Although the output is rated to withstand 15 volts, the V_{CC} terminal is connected to the standard 5-volt source. The output transistor will sink 16 milliamperes while maintaining a low-level output voltage of 0.4 volt maximum thus providing a high-fan-out driver with the nominal power dissipation of standard Series 54/74 gates.

The SN5426 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN7426 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Output voltage (see Notes 1 and 2) . . . . . 15 V
Operating free-air temperature range: SN5426 Circuits . . . . . −55°C to 125°C
SN7426 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

	SN5426			SN7426			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage	4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}			15			15	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	101		2			V
V_{IL}	Low-level input voltage	102				0.8	V
V_{OH}	High-level output voltage	102	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = 1 mA	15			V
I_{OH}	High-level output current	102	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 12 V			50	μA
V_{OL}	Low-level output voltage	101	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA			0.4	V
I_{IH}	High-level input current (each input)	103	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	104	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	105	V_{CC} = MAX, V_I = 0		4	8	mA
I_{CCL}	Supply current, low-level output	105	V_{CC} = MAX, V_I = 5 V		12	22	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

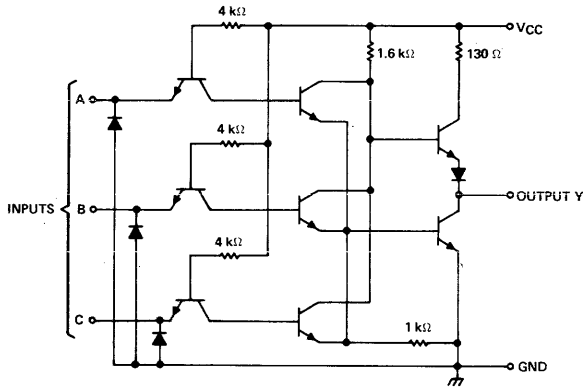
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	106	C_L = 15 pF, R_L = 1 kΩ		16	24	ns
t_{PHL}	Propagation delay time, high-to-low-level output	106	C_L = 15 pF, R_L = 1 kΩ		11	17	ns

6

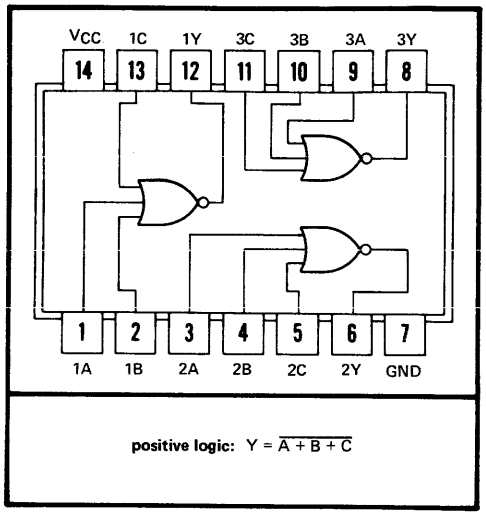
CIRCUIT TYPES SN5427, SN7427
TRIPLE 3-INPUT POSITIVE-NOR GATES

schematic (each gate)



Component values shown are nominal.

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN5427 Circuits . . . . . −55°C to 125°C
SN7427 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5427			SN7427			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA			0.22	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN5427	−20		−55	mA
			SN7427	−18		−55	
I_{CCH}	Supply current, high-level output	V_{CC} = MAX, See Note 2			10	16	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, See Note 3			16	26	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTES: 2. I_{CCH} is measured with all inputs grounded, and outputs open.
3. I_{CCL} is measured with one input of each gate at 4.5 V, the remaining inputs grounded, and outputs open.

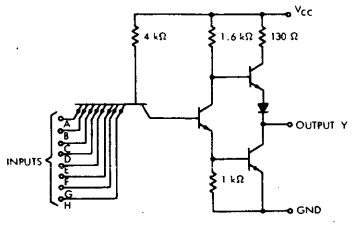
6

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 400 Ω		10	15	ns
t_{PLH}	Propagation delay time, low-to-high-level output			7	11	ns

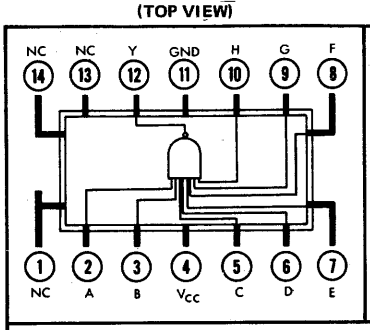
CIRCUIT TYPES SN5430, SN7430
8-INPUT POSITIVE NAND GATES

schematic

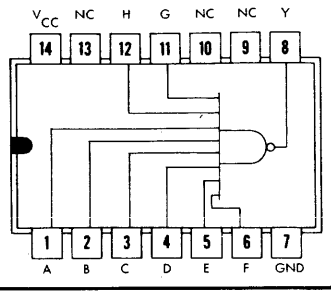


Component values shown are nominal.
NC—No Internal Connection

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{ABCDEFGH}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5430 Circuits	4.5	5	5.5	V
SN7430 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5430 Circuits	−55	25	125	°C
SN7430 Circuits	0	25	70	°C

6

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

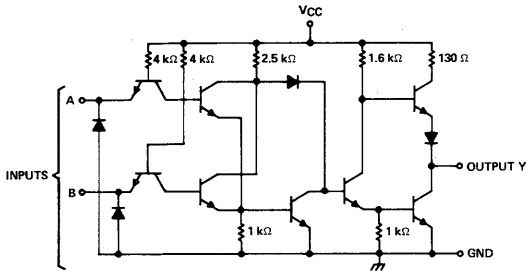
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN5430	−20		−55	mA
				SN7430	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			3	6	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			1	2	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

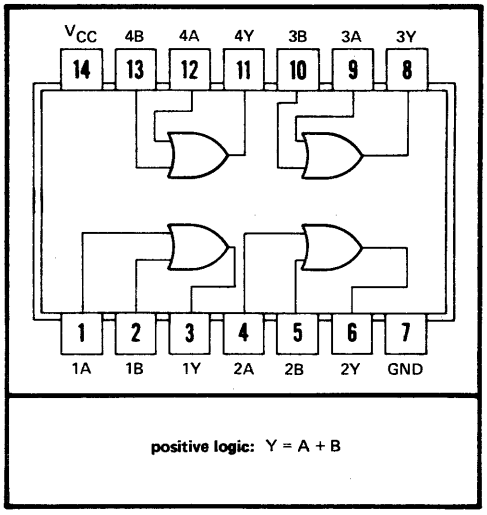
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		13	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

schematic (each gate)



J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN5432 Circuits . . . . . −55°C to 125°C
SN7432 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE: 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5432			SN7432			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MAX, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −800 μA		2.4	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.22	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX. V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN5432	−20		−55	mA
			SN7432	−18		−55	
I_{CCH}	Supply current, high-level output	V_{CC} = MAX,	See Note 2		15	22	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX,	See Note 3		23	38	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTES: 2. I_{CCH} is measured with one input of each gate at 4.5 V, the remaining inputs grounded, and outputs open.
3. I_{CCL} is measured with both inputs of all gates grounded, and outputs open.

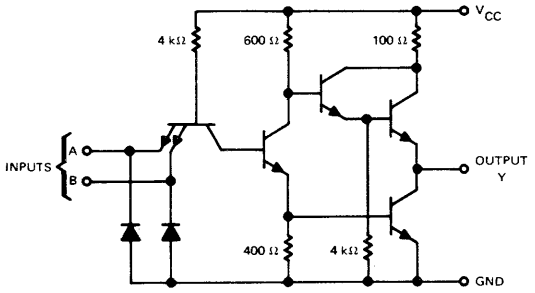
6

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

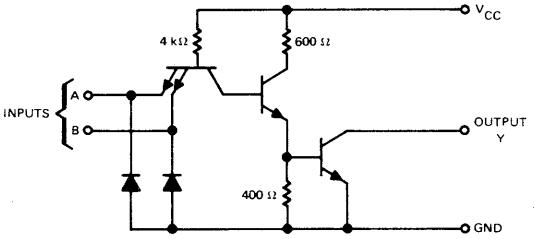
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 400 Ω		14	22	ns
t_{PLH}	Propagation delay time, low-to-high-level output			10	15	ns

schematics (each buffer)

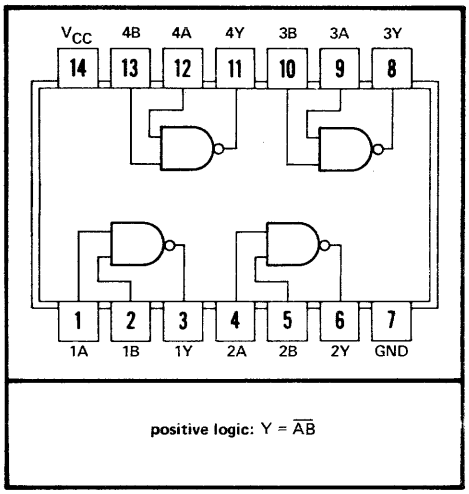
SN5437, SN7437 (TOTEM-POLE OUTPUT)



SN5438, SN7438 (OPEN-COLLECTOR OUTPUT)



J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Output voltage (see Notes 1 and 3): SN5438, SN7438 Circuits . . . . . 5.5 V
Operating free-air temperature range: SN5437, SN5438 Circuits . . . . . −55°C to 125°C
SN7437, SN7438 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

	SN5437, SN5438			SN7437, SN7438			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			30			30	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5437, SN7437			UNIT
			MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −1.2 mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 48 mA		0.22	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_I = 0	−20		−70	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX, All inputs at 0 V		9	15.5	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, All inputs at 5 V		34	54	mA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5438, SN7438			UNIT
			MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 5.5 V			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 48 mA		0.22	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX, All inputs at 0 V		5	8.5	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, All inputs at 5 V		34	54	mA

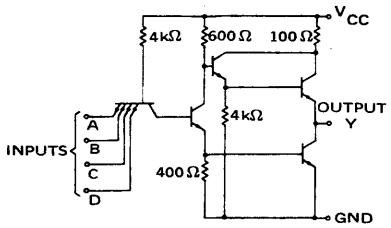
6

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 30

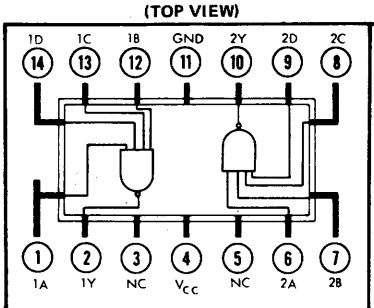
PARAMETER		TEST CONDITIONS	SN5437, SN7437			SN5438, SN7438			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, R_L = 133 Ω		13	22		14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output			8	15		11	18	ns

schematic (each gate)

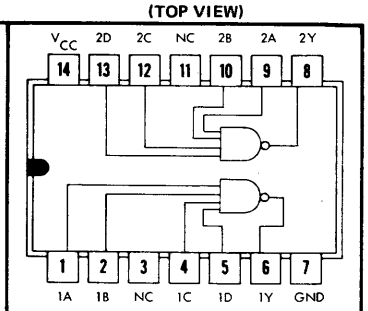


Component values shown are nominal.
NC—No Internal Connection

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{ABCD}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5440 Circuits	4.5	5	5.5	V
SN7440 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Output, N			30	
Operating Free-Air Temperature Range, T_A: SN5440 Circuits	−55	25	125	°C
SN7440 Circuits	0	25	70	°C

electrical characteristics (over recommended free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −1.2 mA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 48 mA			0.28	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current §	5	V_{CC} = MAX	SN5440	−20		−70	mA
				SN7440	−18		−70	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			17	27	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			4	8	mA

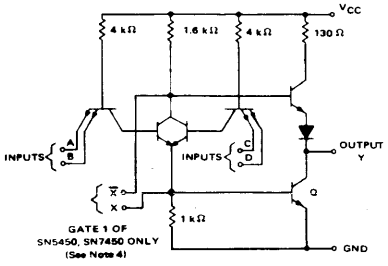
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 30

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 133 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 133 Ω		13	22	ns

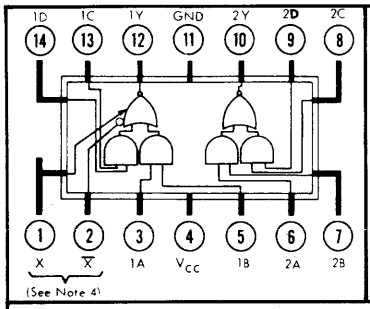
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

CIRCUIT TYPES SN5450, SN5451, SN7450, SN7451
EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

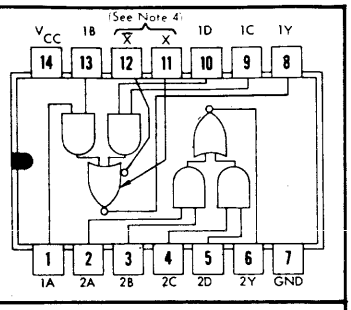
schematic (each gate)



W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{(AB) + (CD) + (X)}$
X = Output of SN5460/SN7460

NOTES:
1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Make no external connection to X and $\overline{X}$ pins of the SN5451 and SN7451.
5. A total of four expander gates can be connected to the expander inputs.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5450, SN5451 Circuits	4.5	5	5.5	V
	SN7450, SN7451 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5450, SN5451 Circuits	−55	25	125	°C
	SN7450, SN7451 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	21			2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	22					0.8	V
$V_{out(1)}$	Logical 1 output voltage	22	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	21	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	23	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	24	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	25	V_{CC} = MAX	SN5450, SN5451	−20		−55	mA
				SN7450, SN7451	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	26	V_{CC} = MAX, V_{in} = 5 V			7.4	14	mA
$I_{CC(1)}$	Logical 1 level supply current	27	V_{CC} = MAX, V_{in} = 0			4	8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and $\overline{X}$ are open.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

electrical characteristics (SN5450 circuits) using expander inputs, V_{CC} = 4.5 V, T_A = –55°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{sink} = 16 mA			2.9	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{sink} = 16 mA, I_1 = 0.41 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	30	I_{load} = –400 μA, I_1 = 0.15 mA, I_2 = –0.15 mA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	29	I_{sink} = 16 mA, I_1 = 0.3 mA, R_1 = 138 Ω		0.22	0.4	V

electrical characteristics (SN7450 circuits) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{sink} = 16 mA			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{sink} = 16 mA, I_1 = 0.62 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	30	I_{load} = –400 μA, I_1 = 270 μA, I_2 = –270 μA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	29	I_{sink} = 16 mA, I_1 = 0.43 mA, R_1 = 130 Ω		0.22	0.4	V

6

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

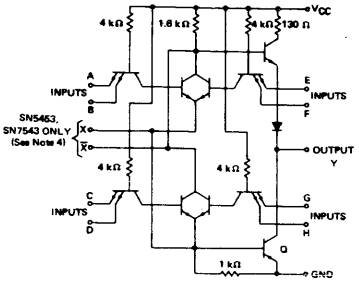
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		13	22	ns

†Expander pins X and $\overline{X}$ are open.

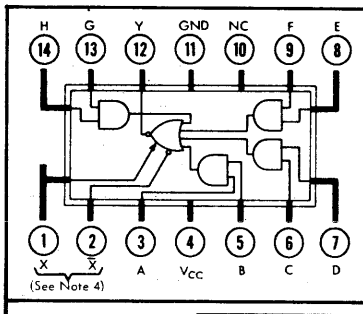
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

CIRCUIT TYPES SN5453, SN5454, SN7453, SN7454
EXPANDABLE 4-WIDE 2-INPUT AND-OR-INVERT GATES

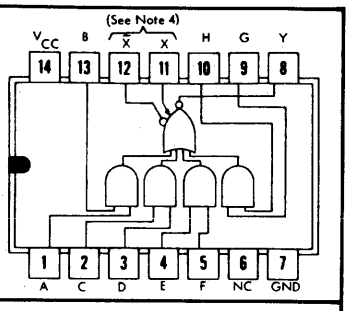
schematic



W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{(AB) + (CD) + (EF) + (GH) + (X)}$
X = Output of SN5460/SN7460

NOTES:
1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Make no external connection to X and $\overline{X}$ pins of the SN5454 and SN7454.
5. A total of four expander gates can be connected to the expander inputs.
6. NC—No Internal Connection

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5453, SN5454 Circuits	4.5	5	5.5	V
SN7453, SN7454 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5453, SN5454 Circuits	−55	25	125	°C
SN7453, SN7454 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of one AND section to ensure logical 0 level at output	21			2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 level at output	22					0.8	V
$V_{out(1)}$	Logical 1 output voltage	22	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	21	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	23	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	24	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	25	V_{CC} = 5.5 V	SN5453, SN5454	−20		−55	mA
				SN7453, SN7454	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	26	V_{CC} = MAX, V_{in} = 5 V			5.1	9.5	mA
$I_{CC(1)}$	Logical 1 level supply current	27	V_{CC} = MAX, V_{in} = 0			4	8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and $\overline{X}$ are open.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

electrical characteristics (SN5453 circuits) using expander inputs, V_{CC} = 4.5 V, T_A = –55°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{sink} = 16 mA			2.9	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{sink} = 16 mA I_1 = 0.41 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	30	I_{load} = –400 μA, I_1 = 0.15 mA, I_2 = –0.15 mA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	29	I_{sink} = 16 mA, I_1 = 0.3 mA, R_1 = 138 Ω		0.22	0.4	V

electrical characteristics (SN7453 circuits) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{sink} = 16 mA			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{sink} = 16 mA, I_1 = 0.62 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	30	I_{load} = –400 μA, I_1 = 270 μA, I_2 = –270 μA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	29	I_{sink} = 16 mA, I_1 = 0.43 mA, R_1 = 130 Ω		0.22	0.4	V

6

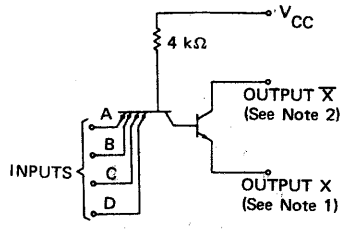
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		13	22	ns

† Expander inputs X and $\overline{X}$ are open.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

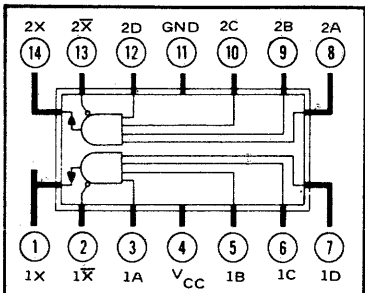
CIRCUIT TYPE SN5460
DUAL 4-INPUT EXPANDER

schematic (each expander)

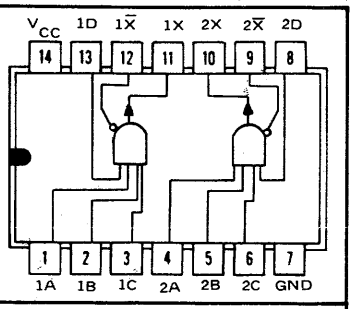


NOTES: 1. Connect to X input of SN5450 or SN5453 circuit.
2. Connect to $\overline{X}$ input of SN5450 or SN5453 circuit.
3. Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: X=ABCD
when connected to X and $\overline{X}$ pins of SN5450 or SN5453 circuit.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Maximum number of expanders that may be fanned-in to one SN5450 or one SN5453 circuit 4

electrical characteristics (unless otherwise noted T_A = −55°C to 125°C)

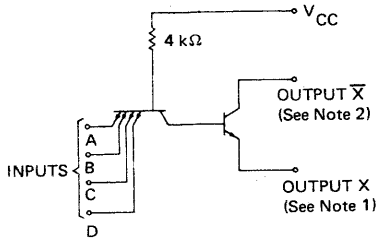
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	31		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	32				0.8	V
V_{on}	On-state output voltage	31	V_{CC} = 4.5 V, V_{in} = 2 V, V_I = 1 V, R = 1.1 kΩ, T_A = −55°C			0.4	V
I_{off}	Off-state output current	32	V_{CC} = 4.5 V, V_{in} = 0.8 V, V_I = 4.5 V, R = 1.2 kΩ, T_A = −55°C			150	μA
I_{on}	On-state output current	33	V_{CC} = 4.5 V, V_{in} = 2 V, V_I = 1 V, T_A = −55°C	−0.3			mA
$I_{in(0)}$	Logical 0 level input current (each input)	32	V_{CC} = 5.5 V, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	34	V_{CC} = 5.5 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	35	V_{CC} = 5.5 V, V_{in} = 5 V, V_I = 0.85 V		1.2	2.5	mA
$I_{CC(off)}$	Off-state supply current	35	V_{CC} = 5.5 V, V_{in} = 0, V_I = 0.85 V		2	4	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

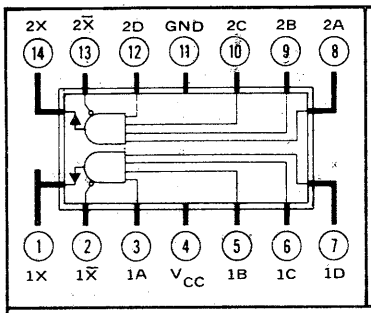
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (through SN5450 or SN5453 circuit)	66	C_L = 15 pF, R_L = 400 Ω		10	20	ns
t_{pd1}	Propagation delay time to logical 1 level (through SN5450 or SN5453 circuit)	66	C_L = 15 pF, R_L = 400 Ω		15	30	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

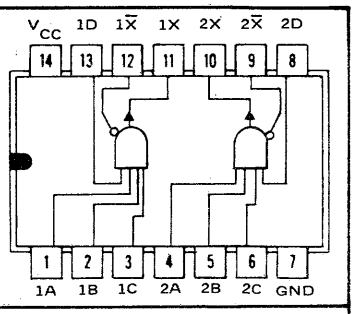
schematic (each expander)



W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: X=ABCD
when connected to X and X̄ pins of SN7450 or SN7453 circuit.

NOTES: 1. Connect to X input of SN7450 or SN7453 circuit.
2. Connect to X̄ input of SN7450 or SN7453 circuit.
3. Component values shown are nominal.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Maximum number of expanders that may be fanned-in to one SN7450 or one SN7453 Circuit 4

electrical characteristics (unless otherwise noted T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals is in the on state	31		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal is in the off state	32				0.8	V
V_{on}	On-state output voltage	31	V_{CC} = 4.75 V, V_{in} = 2 V, V_1 = 1 V, R = 1.1 kΩ, T_A = 0°C			0.4	V
I_{off}	Off-state output current	32	V_{CC} = 4.75 V, V_{in} = 0.8 V, V_1 = 4.5 V, R = 1.2 kΩ T_A = 0°C			270	μA
I_{on}	On-state output current	33	V_{CC} = 4.75 V, V_{in} = 2 V, V_1 = 1 V	−0.43			mA
$I_{in(0)}$	Logical 0 level input current (each input)	32	V_{CC} = 5.25 V, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	34	V_{CC} = 5.25 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	35	V_{CC} = 5.25 V, V_{in} = 5 V, V_1 = 0.85 V		1.2	2.5	mA
$I_{CC(off)}$	Off-state supply current	35	V_{CC} = 5.25 V, V_{in} = 0, V_1 = 0.85 V		2	4	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (through SN7450 or SN7453)	66	C_L = 15 pF, R_L = 400 Ω		10	20	ns
t_{pd1}	Propagation delay time to logical 1 level (through SN7450 or SN7453)	66	C_L = 15 pF, R_L = 400 Ω		15	30	ns

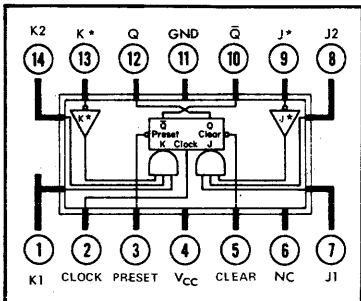
CIRCUIT TYPES SN5470, SN7470
EDGE-TRIGGERED J-K FLIP-FLOPS

logic

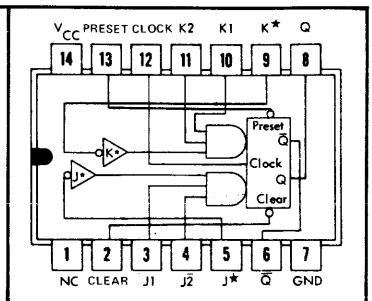
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. $J = J1 \cdot J2 \cdot \overline{J^*}$.
2. $K = K1 \cdot K2 \cdot \overline{K^*}$.
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. If inputs J* or K* are not used they must be grounded.
6. NC - No Internal Connection

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset or clear function can occur only when clock input is low.

description

These monolithic, edge-triggered J-K flip-flops feature gated inputs, direct clear and preset inputs, and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse, and after the clock input threshold voltage has been passed, the gated inputs are locked out.

These flip-flops are ideally suited for medium- to high-speed applications and can result in a significant saving in system power dissipation and package count where input gating is required.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5470 Circuits	4.5	5	5.5	V
SN7470 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN5470 Circuits	−55	25	125	°C
SN7470 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Clock Pulse Transition Time to Logical 1 Level, $t_{1(clock)}$ (See Figure 68)	5		150	ns
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 68)	20			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 67)	25			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 67)	25			ns

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	36 and 37			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	36 and 37					0.8	V
$V_{out(1)}$	Logical 1 output voltage	36	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	37	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J*, K1, K2, K*, or clock	38	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset or clear	38	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J*, K1, K2, K*, or clock	39	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	39	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	40	V_{CC} = MAX, V_{in} = 0	SN5470	−20		−57	mA
				SN7470	−18		−57	
I_{CC}	Supply current	39	V_{CC} = MAX, V_{in} = 5 V			13	26	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

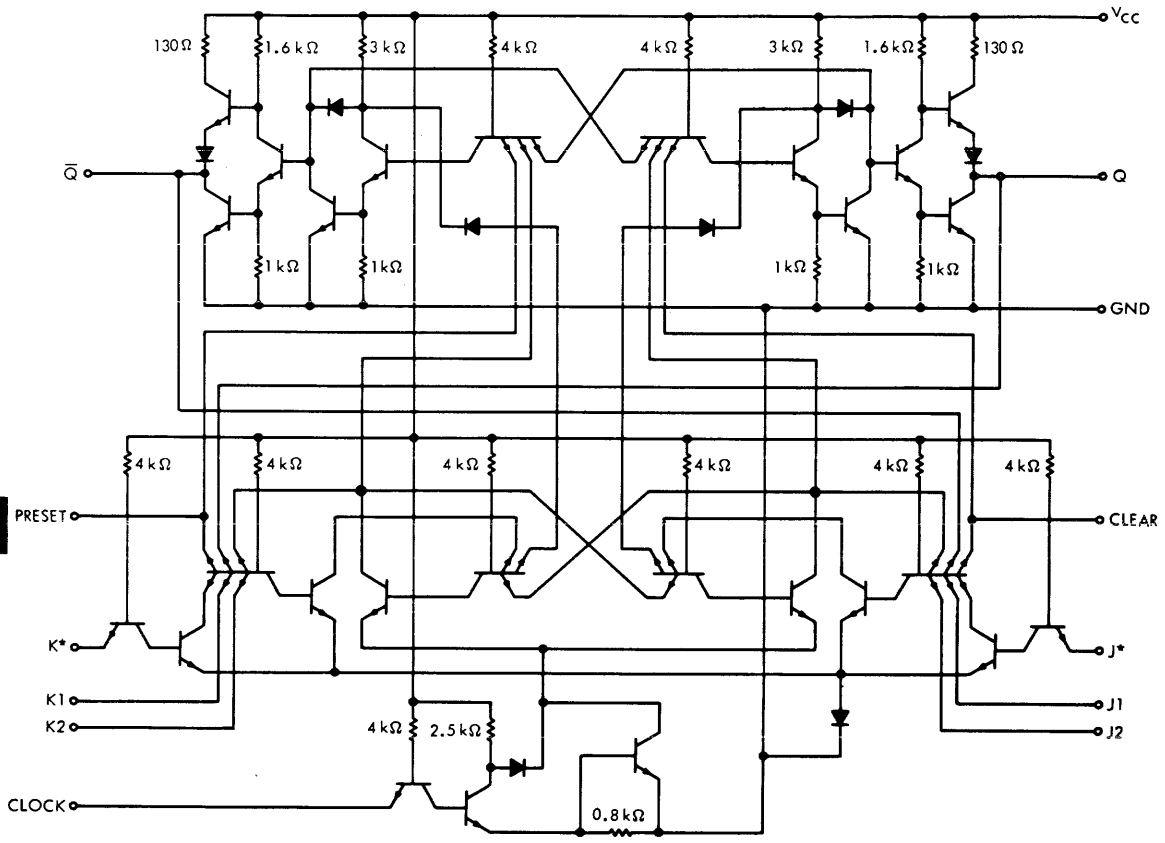
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	68	C_L = 15 pF, R_L = 400 Ω	20	35		MHz
t_{setup}	Minimum input setup time	68	C_L = 15 pF, R_L = 400 Ω		10	20	ns
t_{hold}	Minimum input hold time	68	C_L = 15 pF, R_L = 400 Ω		0	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	67	C_L = 15 pF, R_L = 400 Ω			50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	67	C_L = 15 pF, R_L = 400 Ω			50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	68	C_L = 15 pF, R_L = 400 Ω	10	27	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	68	C_L = 15 pF, R_L = 400 Ω	10	18	50	ns

schematic



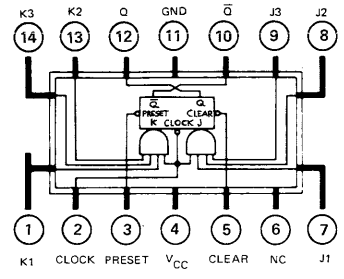
NOTE: Component values shown are nominal.

logic

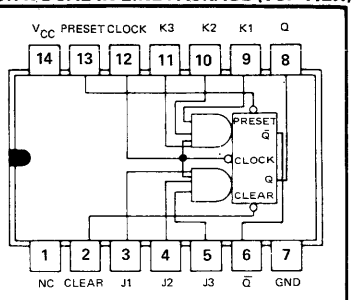
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. NC = No Internal Connection.

W FLAT PACKAGE (TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

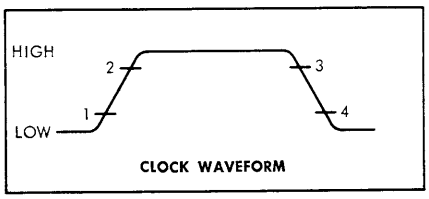


positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These J-K flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5472 Circuits	4.5	5	5.5	V
SN7472 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN5472 Circuits	−55	25	125	°C
SN7472 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See figure 69)	20			ns
Width of Preset Pulse, $t_{p(preset)}$ (See figure 70)	25			ns
Width of Clear Pulse, $t_{p(clear)}$ (See figure 70)	25			ns
Input Setup Time, t_{setup} (See figure 69)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

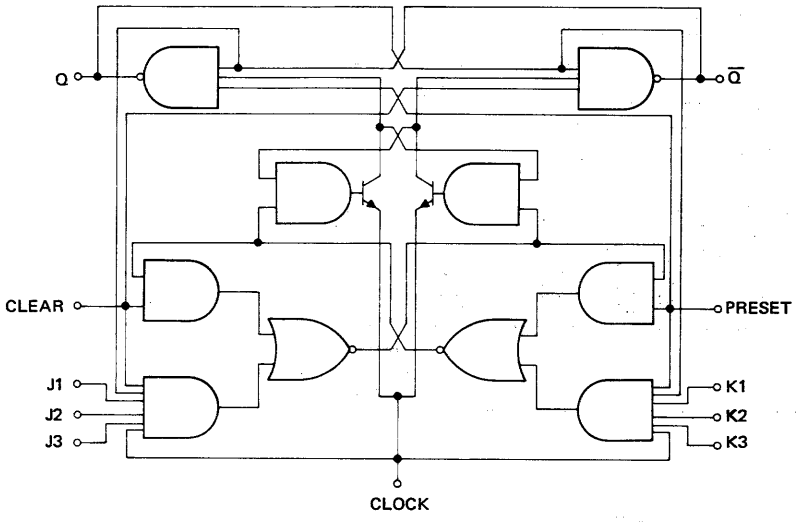
PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	41 and 42				2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	41 and 42						0.8	V
$V_{out(1)}$	Logical 1 output voltage	41	V_{CC} = MIN,	I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	42	V_{CC} = MIN,	I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, or K3	43	V_{CC} = MAX,	V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	43	V_{CC} = MAX,	V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	44	V_{CC} = MAX,	V_{in} = 2.4 V				40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset, clear, or clock	44	V_{CC} = MAX,	V_{in} = 2.4 V				80	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	45	V_{CC} = MAX,	V_{in} = 0	SN5472	−20		−57	mA
					SN7472	−18		−57	
I_{CC}	Supply current	44	V_{CC} = MAX,	V_{in} = 5 V			10	20	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

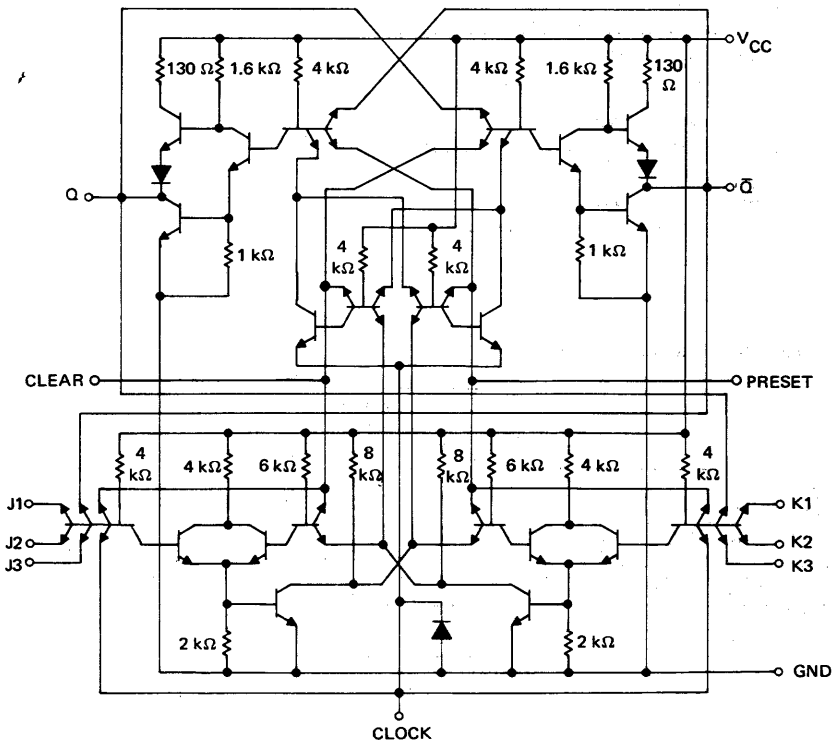
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	69	C_L = 15 pF,	R_L = 400 Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	70	C_L = 15 pF,	R_L = 400 Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	70	C_L = 15 pF,	R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	69	C_L = 15 pF,	R_L = 400 Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	69	C_L = 15 pF,	R_L = 400 Ω	10	25	40	ns

functional block diagram



schematic

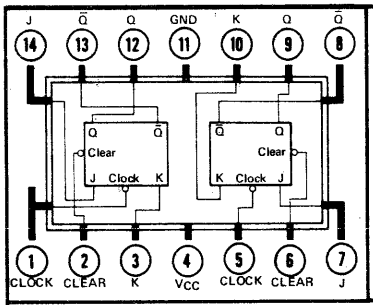


Component values shown are nominal.

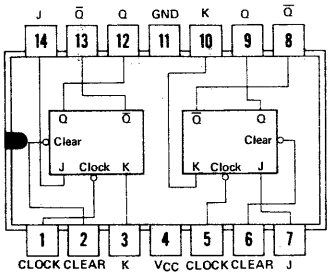
6

CIRCUIT TYPES SN5473, SN54107, SN7473, SN74107
DUAL J-K MASTER-SLAVE FLIPS-FLOPS

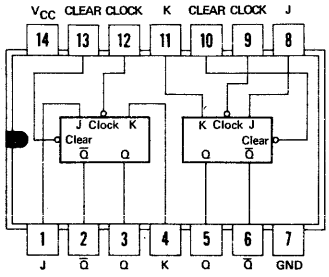
SN5473, SN7473
W FLAT PACKAGE
(TOP VIEW)



SN5473, SN7473
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



SN54107, SN74107
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic:
Low input to clear sets Q to logical 0.
Clear is independent of clock.

description

These J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: (See waveform on page 2-26)

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

logic

TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

recommended operating conditions

	SN5473 SN54107			SN7473 SN74107			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Width of clock pulse, $t_{p(clock)}$ (See Figure 69)	20			20			ns
Width of clear pulse, $t_{p(clear)}$ (See Figure 70)	25			25			ns
Input setup time, t_{setup} (See Figure 69)	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input hold time, t_{hold}	0			0			
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	46 and 47				2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	46 and 47						0.8	V
$V_{out(1)}$	Logical 1 output voltage	46	V_{CC} = MIN,	I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	47	V_{CC} = MIN,	I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	48	V_{CC} = MAX,	V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	48	V_{CC} = MAX,	V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	49	V_{CC} = MAX,	V_{in} = 2.4 V				40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at clear or clock	49	V_{CC} = MAX,	V_{in} = 2.4 V				80	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	50	V_{CC} = MAX,	V_{in} = 0	SN5473, SN54107	−20		−57	mA
					SN7473, SN74107	−18		−57	
I_{CC}	Supply current	49	V_{CC} = MAX				20	40	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

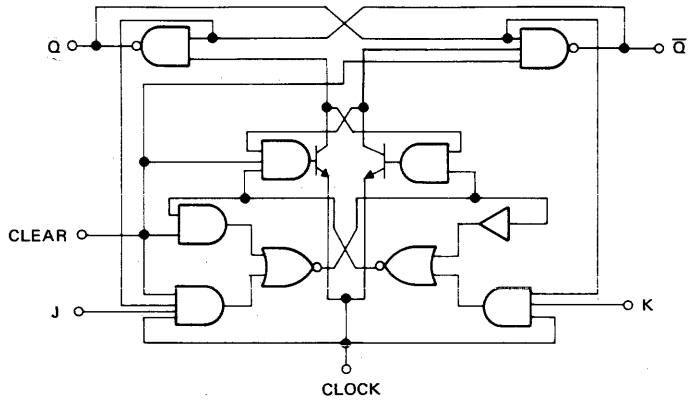
6

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

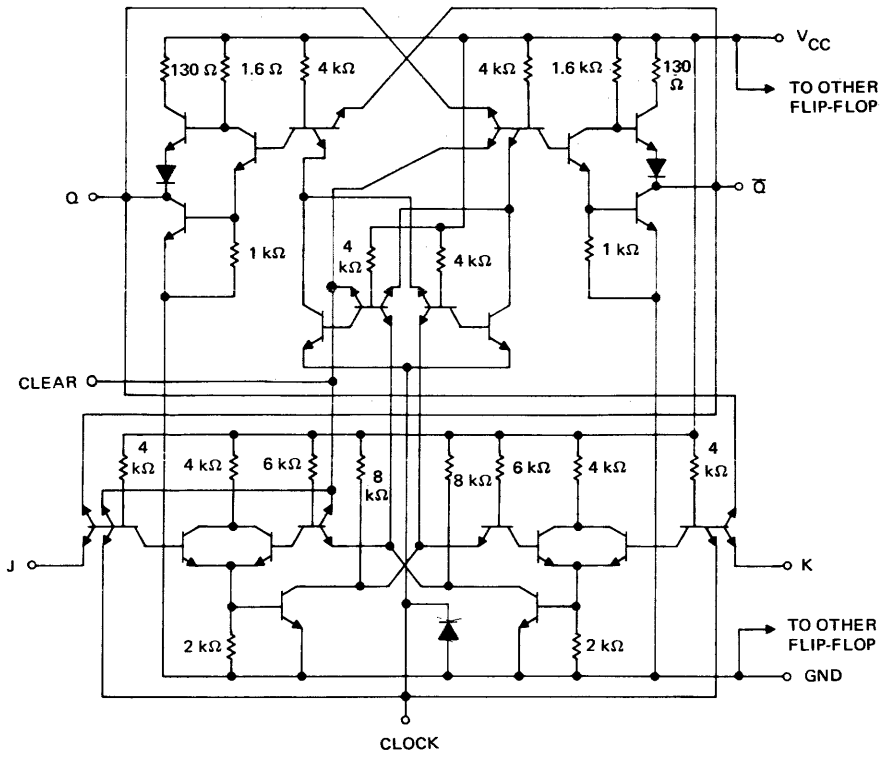
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	69	C_L = 15 pF,	R_L = 400 Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	70	C_L = 15 pF,	R_L = 400 Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	70	C_L = 15 pF,	R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	69	C_L = 15 pF,	R_L = 400 Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	69	C_L = 15 pF,	R_L = 400 Ω	10	25	40	ns

CIRCUIT TYPES SN5473,SN54107,SN7473,SN74107
DUAL J-K MASTER-SLAVE FLIP-FLOPS

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

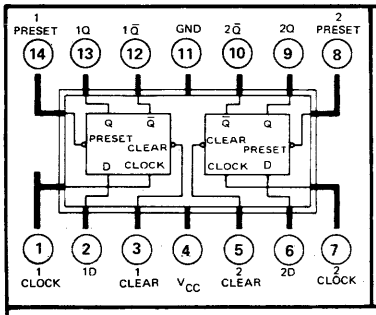
logic

TRUTH TABLE (Each Flip-Flop)

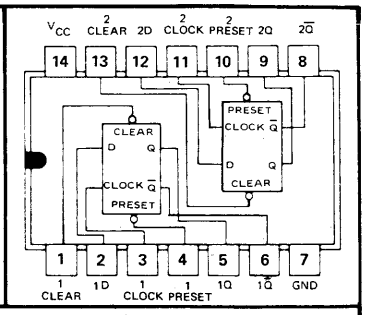
t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\bar{Q}$
0	0	1
1	1	0

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These monolithic, dual, D-type, edge-triggered flip-flops feature direct clear and preset inputs and complementary Q and $\bar{Q}$ outputs. Input information is transferrred to the outputs on the positive edge of the clock pulse.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out.

These dual flip-flops have the same clocking characteristics as the SN5470/SN7470 gated (edge-triggered) flip-flop circuits, and both are ideally suited for medium- to-high-speed applications. They can result in a significant saving in system power dissipation and package count in applications where input gating is not required.

recommended operating conditions

	SN5474			SN7474			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Width of clock pulse, $t_{p(clock)}$ (See Figure 71)	30			30			ns
Width of preset pulse, $t_{p(preset)}$ (See Figure 67)	30			30			ns
Width of clear pulse, $t_{p(clear)}$ (See Figure 67)	30			30			ns
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	52 and 53				2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	52 and 53						0.8	V
$V_{out(1)}$	Logical 1 output voltage	52	V_{CC} = MIN,	I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	53	V_{CC} = MIN,	I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at preset or D	54	V_{CC} = MAX,	V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	54	V_{CC} = MAX,	V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at D	55	V_{CC} = MAX,	V_{in} = 2.4 V				40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clock	55	V_{CC} = MAX,	V_{in} = 2.4 V				80	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at clear	55	V_{CC} = MAX,	V_{in} = 2.4 V				120	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	56	V_{CC} = MAX,	V_{in} = 0	SN5474	−20		−57	mA
					SN7474	−18		−57	
I_{CC}	Supply current	55	V_{CC} = MAX				17	30	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

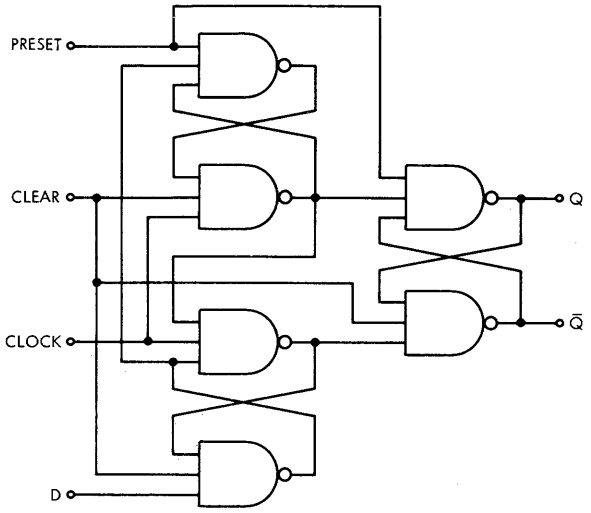
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

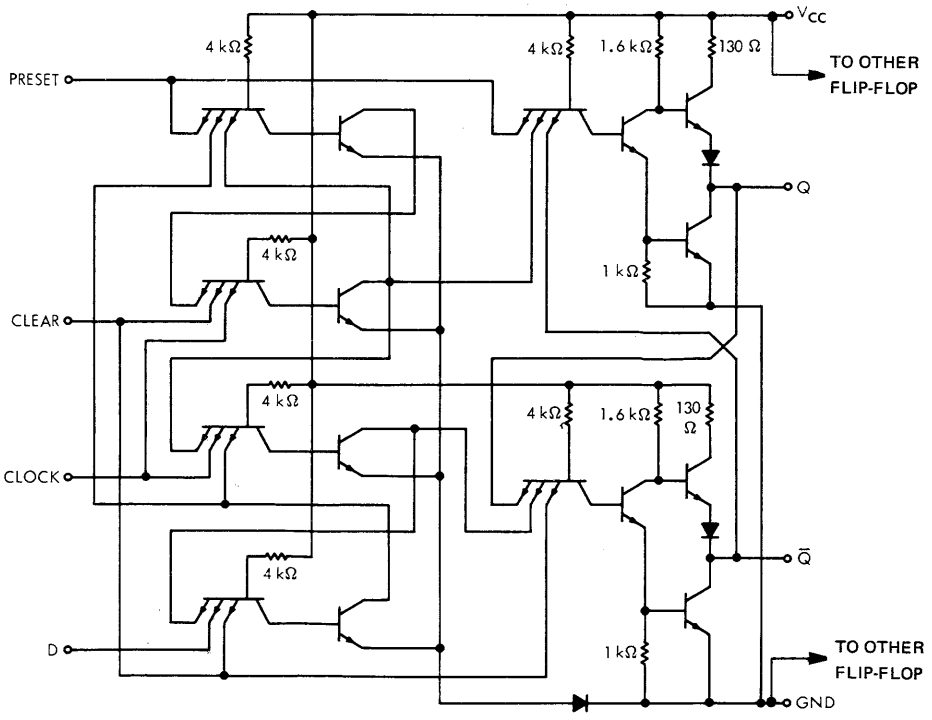
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	71	C_L = 15 pF,	R_L = 400 Ω	15	25		MHz
t_{setup}	Minimum input setup time	71	C_L = 15 pF,	R_L = 400 Ω		15	20	ns
t_{hold}	Minimum input hold time	71	C_L = 15 pF,	R_L = 400 Ω		2	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	67	C_L = 15 pF,	R_L = 400 Ω			25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	67	C_L = 15 pF,	R_L = 400 Ω			40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	71	C_L = 15 pF,	R_L = 400 Ω	10	14	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	71	C_L = 15 pF,	R_L = 400 Ω	10	20	40	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

6

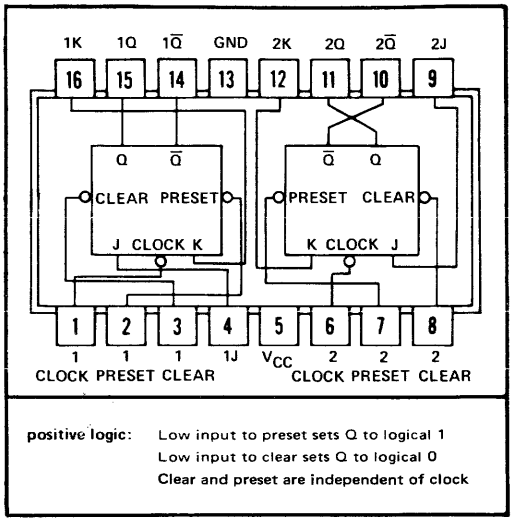
CIRCUIT TYPES SN5476, SN7476
DUAL J-K MASTER-SLAVE FLIP-FLOPS
WITH PRESET AND CLEAR

logic

TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

J OR N DUAL-IN-LINE OR
W FLAT PACKAGES (TOP VIEW)†



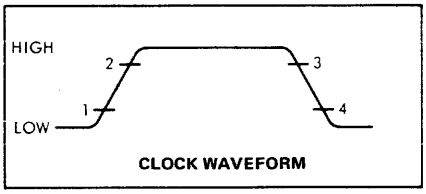
positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Clear and preset are independent of clock

†Pin assignments for these circuits are the same for all packages.

description

The SN7476 J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5476 Circuits	4.5	5	5.5	V
SN7476 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN5476 Circuits	−55	25	125	°C
SN7476 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See figure 69)	20			ns
Width of Preset Pulse, $t_{p(preset)}$ (See figure 70)	25			ns
Width of Clear Pulse, $t_{p(clear)}$ (See figure 70)	25			ns
Input Setup Time, t_{setup} (See figure 69)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

electrical characteristics, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	46 and 47			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	46 and 47					0.8	V
$V_{out(1)}$	Logical 1 output voltage	46	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	47	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	48	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear, preset, or clock	48	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	49	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at clear, preset, or clock	49	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	51	V_{CC} = MAX, V_{in} = 0	SN5476	−20		−57	mA
				SN7476	−18		−57	
I_{CC}	Supply current (each flip-flop)	49	V_{CC} = MAX			20	40	mA

6

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	69	C_L = 15 pF, R_L = 400 Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 0 level from clear or preset to output	70	C_L = 15 pF, R_L = 400 Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 1 level from clear or preset to output	70	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	69	C_L = 15 pF, R_L = 400 Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	69	C_L = 15 pF, R_L = 400 Ω	10	25	40	ns

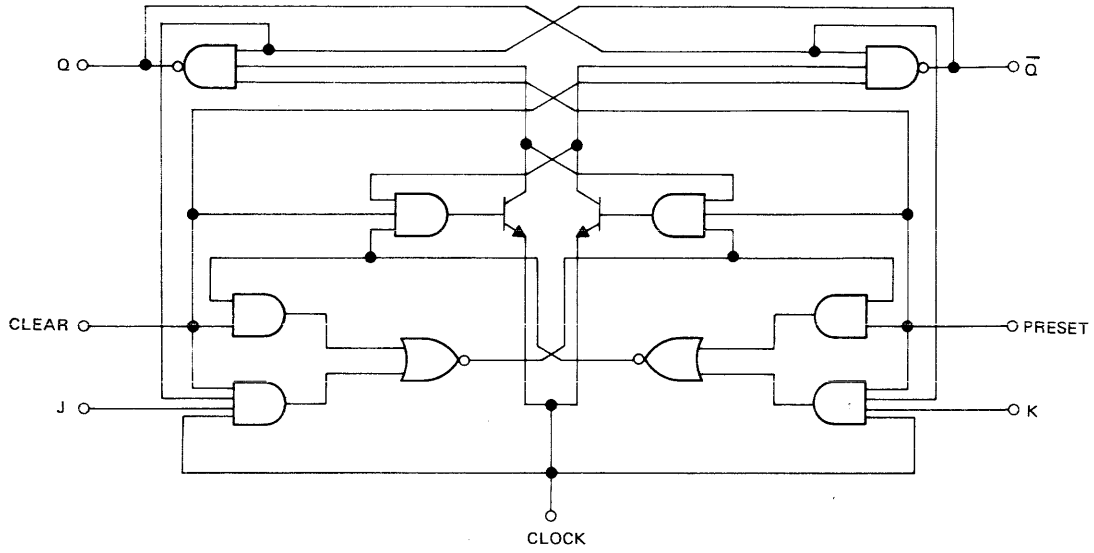
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

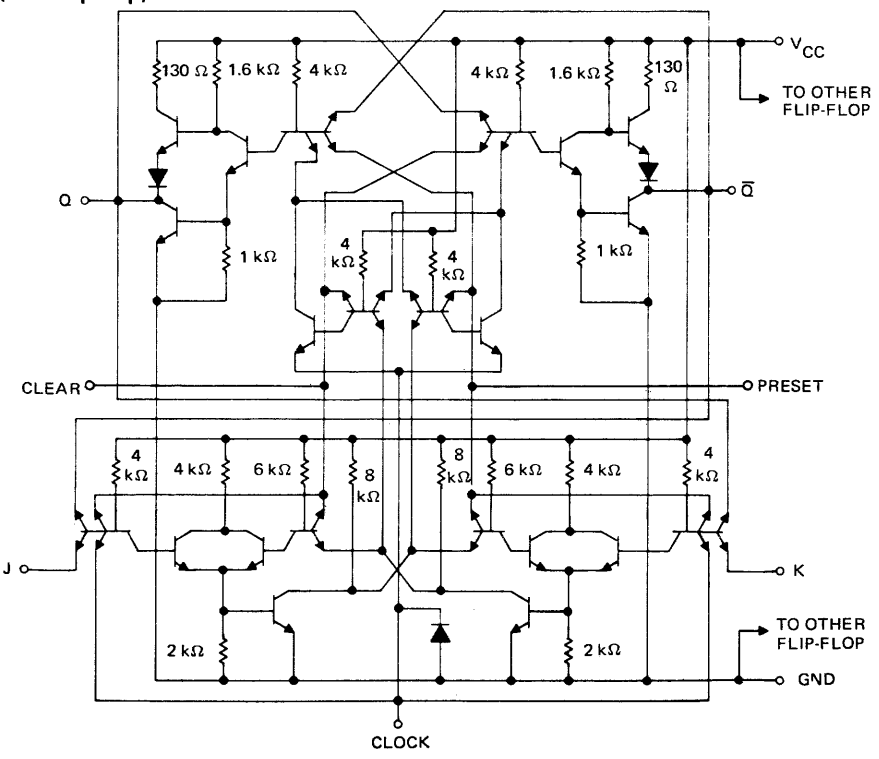
§Not more than one output should be shorted at a time.

CIRCUIT TYPES SN5476, SN7476
DUAL J-K MASTER-SLAVE FLIP-FLOPS
WITH PRESET AND CLEAR

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

CIRCUIT TYPES SN54104, SN54105, SN74104, SN74105
GATED J-K MASTER-SLAVE FLIP-FLOPS

featuring

● Buffered Clock Input ● Direct Preset and Clear ● Common JK Gate Input

logic

TRUTH TABLE

INPUTS AT t_n			OUTPUTS AT t_{n+1}	
JK	J†	K†	Q	$\overline{Q}$
L‡	X	X	Q_n	$\overline{Q}_n$
H	L‡	L‡	Q_n	$\overline{Q}_n$
H	L	H	L	H
H	H	L	H	L
H	H	H	$\overline{Q}_n$	Q_n

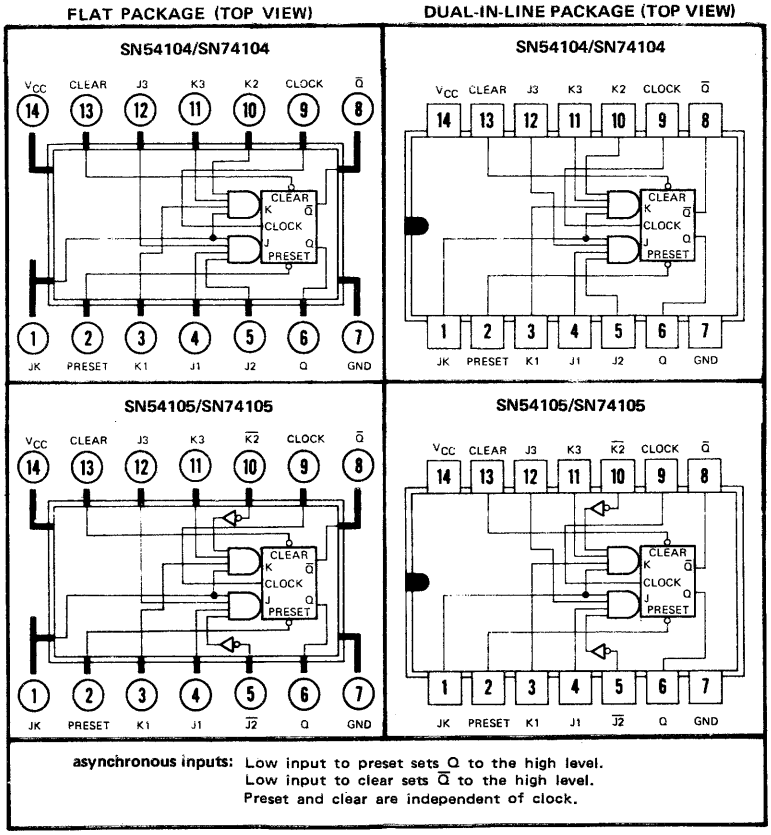
† SN54104/SN74104: J = J1 • J2 • J3,
K = K1 • K2 • K3
SN54105/SN74105: J = J1 • $\overline{J2}$ • J3,
K = K1 • $\overline{K2}$ • K3

‡ These low levels must be maintained while the clock is low

NOTES:
A. t_n = bit time before clock pulse.
B. t_{n+1} = bit time after clock pulse.
C. H = high, L = low, X = irrelevant.

W
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



asynchronous inputs: Low input to preset sets Q to the high level.
Low input to clear sets $\overline{Q}$ to the high level.
Preset and clear are independent of clock.

description

These J-K master-slave flip-flops feature a buffered clock input, direct preset and clear, gated J and K inputs, and a common JK input. The clock buffer offers typical TTL high noise immunity, low clock-line loading, and, in most cases, eliminates the need for stringent control of system-clock rise and fall times. When activated, the direct preset and clear inputs control the state of both the master and slave flip-flops independent of the clock and synchronous-input states. Gated inputs may be used to perform a wide variety of control functions without the need for external gates, and the common JK input simplifies hardware design for applications utilizing a single gate-control source.

Due to the internal clock buffer, the JK input gates accept data when the clock line is low, and transfer of data from the master to the slave occurs during the clock-line transition from the low state to the high state. When the clock line is high, the data inputs are inhibited.

The SN54104/SN74104 includes internal capacitive loading on the J and K input gates and, as the input setup and hold times are lengthened, this circuit displays improved performance in systems where appreciable clock skew is anticipated.

The SN54105/SN74105 offers an inverting data input to each of the J and K input gates for additional control flexibility. As the input setup and hold times are not lengthened, this circuit permits operation at higher toggle rates than the SN54104/SN74104.

These TTL circuits feature one-volt typical d-c noise margins and are compatible for use with most TTL and DTL families. Full fan-out to 10 normalized Series 54/74 loads is available from the outputs. The SN54104 and SN54105 circuits are characterized for operation over the full military temperature range of −55°C to 125°C, and the SN74104 and SN74105 circuits are characterized for operation from 0°C to 70°C.

6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (See Note 1) . . . . . 8 V

Input voltage (See Note 1) . . . . . −1.5 V to 5.5 V

Voltage applied to any output (See Note 2) . . . . . −0.5 V to V_{CC}

Operating free-air temperature range: SN54104, SN54105 Circuits . . . . . −55°C to 125°C
SN74104, SN74105 Circuits . . . . . 0°C to 70°C

Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage V_{CC} (See Note 1)	SN54104, SN54105		4.5	5	5.5	V
	SN74104, SN74105		4.75	5	5.25	
Operating free-air temperature range	SN54104, SN54105		−55	25	125	°C
	SN74104, SN74105		0	25	70	
Width of low-level clock pulse, $t_{w(clock)}$ (See Figure 112)			15†			ns
Width of preset and clear pulse, $t_{w(preset)}$ and $t_{w(clear)}$			20†			ns
Input release time for low-level data, $t_{release(L)}$ (See Note 3 and Figure 113)	SN54104, SN74104				10†	ns
	SN54105, SN74105				1†	
Input setup time for high-level data, $t_{setup(H)}$ (See Note 4 and Figure 113)	SN54104, SN74104		35†			ns
	SN54105, SN74105		10†			

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This rating applied at the Q output with preset held low and at the $\overline{Q}$ output with clear held low.
3. Release time for low-level data is an interval between the release of low-level data and the positive-going edge of the clock pulse; this interval being sufficiently short to ensure recognition of the low-level data.
4. Setup time for high-level data is an interval between the arrival of the high-level data and the positive-going edge of the clock pulse; this interval being sufficiently long to ensure recognition of the high-level data.

†These conditions are recommended for use at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	107 and 108		T_A = MIN	2			V
				T_A = 25°C	1.7			
				T_A = MAX	1.4			
V_{IL}	Low-level input voltage	107 and 108		T_A = MIN			0.8	V
				T_A = 25°C			0.9	
				T_A = MAX			0.8	
V_{OH}	High-level output voltage	107	V_{CC} = MIN, I_{OH} = −1 mA		2.4	2.7		V
V_{OL}	Low-level output voltage	108	V_{CC} = MAX, I_{OL} = 17.7 mA			0.2	0.4	V
			V_{CC} = MIN, I_{OL} = 16 mA			0.2	0.4	
I_{IH}	High-level input current into any input except JK, preset, or clear	109	V_{CC} = MAX, V_I = 4.5 V	T_A = 25°C		2	40	μA
				T_A = MAX			40	
I_{IH}	High-level input current into JK	109	V_{CC} = MAX, V_I = 4.5 V	T_A = 25°C		4	80	μA
				T_A = MAX			80	
I_{IH}	High-level input current into preset or clear	109	V_{CC} = MAX, V_I = 4.5 V	T_A = 25°C		8	120	μA
				T_A = MAX			120	
I_{IL}	Low-level input current into any input except JK, preset, or clear	110	V_{CC} = MAX, V_I = 0.4 V			−1.1	−1.6	mA
			V_{CC} = MIN, V_I = 0.4 V			−0.9	−1.45	
I_{IL}	Low-level input current into JK	110	V_{CC} = MAX, V_I = 0.4 V			−2.2	−3.2	mA
			V_{CC} = MIN, V_I = 0.4 V			−1.8	−2.9	
I_{IL}	Low-level input current into preset or clear	110	V_{CC} = MAX, V_I = 0.4 V			−3	−4.75	mA
			V_{CC} = MIN, V_I = 0.4 V			−2.5	−3.9	
I_{CC}	Supply current	111	V_{CC} = 5 V	SN54104, SN74104		15	24	mA
				SN54105, SN74105		17	28	

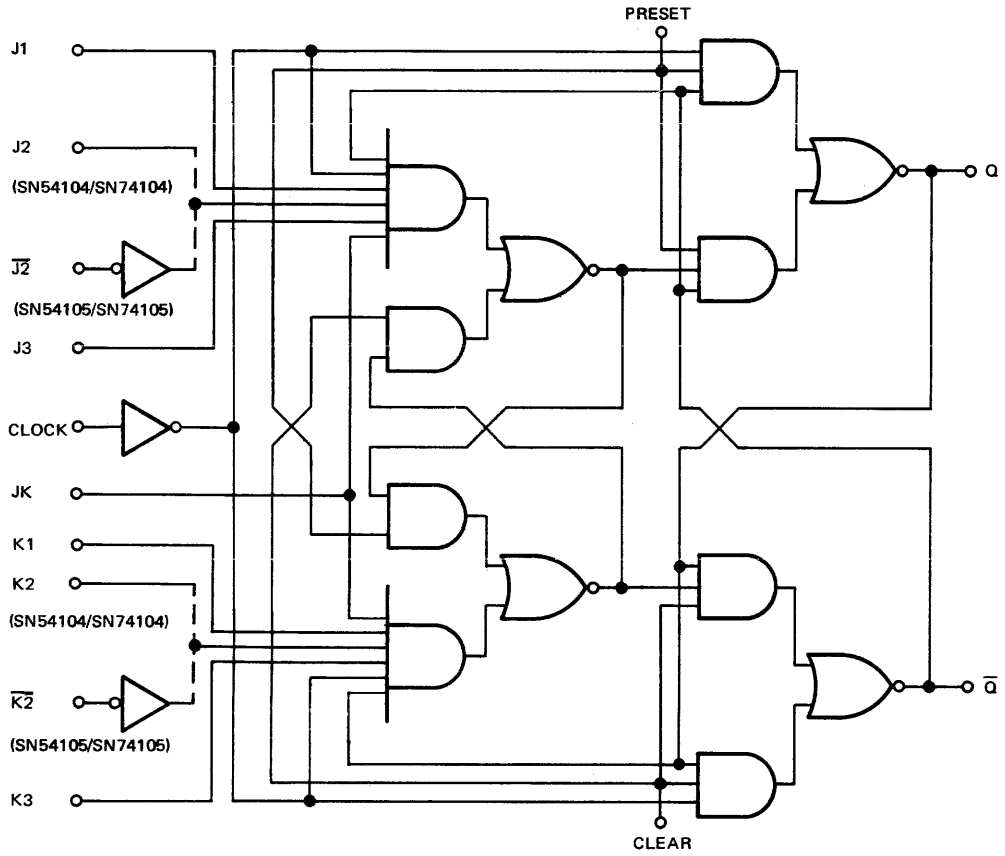
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from clock	112	C_L = 15 pF, R_L = 400 Ω		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock	112	C_L = 15 pF, R_L = 400 Ω		16	25	ns

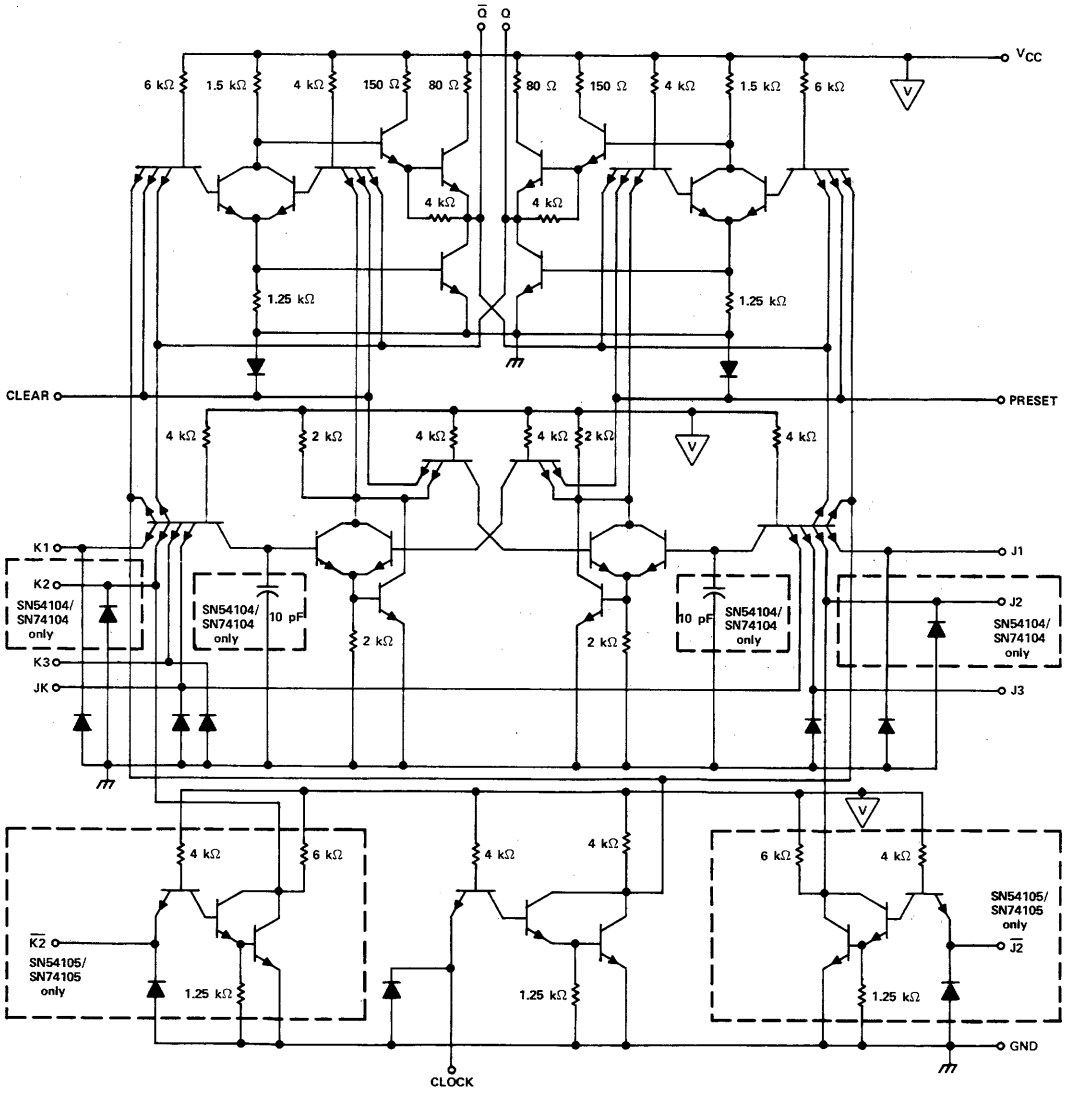
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

functional block diagram



schematic



Component values shown are nominal.

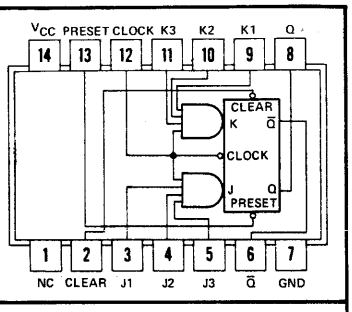
▽ ... V_{CC} bus

6

CIRCUIT TYPES SN54110, SN74110
GATED J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

- Data Lockout Solves Clock-Skew Problems
- Improved Immunity to Noise
- Input-Clamping Diodes Simplify System Design
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with Most TTL, DTL, and MSI Circuits
- Typical Maximum Input Clock Frequency . . . 25 MHz

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

†Pin assignments for these circuits are the same for all packages.
NC—No internal connection.

description

The SN54110 and SN74110 are d-c coupled, variable-skew, J-K flip-flops which utilize TTL circuitry to obtain 25-MHz performance typically. They are termed "variable-skew" because they allow the maximum clock skew in a system to be a direct function of the clock pulse width. The J and K inputs are enabled only during a short period (20 nanoseconds maximum setup time plus 5 nanoseconds maximum hold time) on the rising edge of the clock pulse as shown in the timing diagram, Figure 1. After this, inputs may be changed while the clock is at the high level without affecting the state of the master. On the threshold level of the falling edge of the clock pulse, the data stored in the master during the rising edge will be transferred to the output. The effective allowable clock skew then is minimum propagation delay time minus hold time, plus clock pulse width. This means that the system designer can set the maximum allowable clock skew needed by varying the clock pulse width. Thus system design is made easier and the requirements for sophisticated clock distribution systems are minimized or, in some cases, entirely eliminated. These flip-flops have an additional feature—the synchronous input has reduced sensitivity to data change while the clock is high because the data need be present for only a short period of time and the system's susceptability to noise is thereby effectively reduced.

The SN54110/SN74110 has the same functional advantage as the SN5472/SN7472 in that three-input AND logic is provided for both the J and K data functions. Preset and clear inputs, which are completely independent of the state of the clock, are also provided. The SN54110 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74110 is characterized for operation from 0°C to 70°C.

TRUTH TABLE

INPUTS AT t_n		OUTPUT AT t_{n+1}
J‡	K‡	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

H = high level, L = low level
NOTES: A. t_n = bit time before clock pulse.
B. t_{n+1} = bit time after clock pulse.
‡ J = J1 • J2 • J3
K = K1 • K2 • K3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54110 Circuits	−55°C to 125°C
SN74110 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to the J input with respect to clear and clock, and to the K input with respect to preset and clock.

recommended operating conditions

		SN54110			SN74110			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Clock frequency, f_{clock}		0		20†	0		20†	MHz
Width of clock pulse, $t_{w(clock)}$		25†			25†			ns
Width of preset pulse, $t_{w(preset)}$		25†			25†			ns
Width of clear pulse, $t_{w(clear)}$		25†			25†			ns
Input setup time, high-level or low-level data, t_{setup} (see Note 3 and Figure 114)		20†			20†			ns
Input hold time, high-level or low-level data, t_{hold} (see Note 4)		5†			5†			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

NOTES: 3. Setup time is the interval immediately preceding the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to insure its recognition.

†These conditions are recommended for use at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS‡	MIN	TYP§	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −800 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	J, K, or clock input	V_{CC} = MAX, V_I = 2.4 V			40	μA
		preset or clear input				160	
I_{IL}	Low-level input current	J, K, or clock input	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
		preset or clear input				−3.2	
I_{OS}	Short-circuit output current¶		V_{CC} = MAX	−20		−57	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 5		20	34	mA

NOTE 5: With J and K inputs grounded, the clock input at 4.5 V, and the outputs open, I_{CC} is tested first with clear at 4.5 V and preset grounded, then with clear grounded and preset at 4.5 V.

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

§All typical values are at V_{CC} = 5 V, T_A = 25°C.

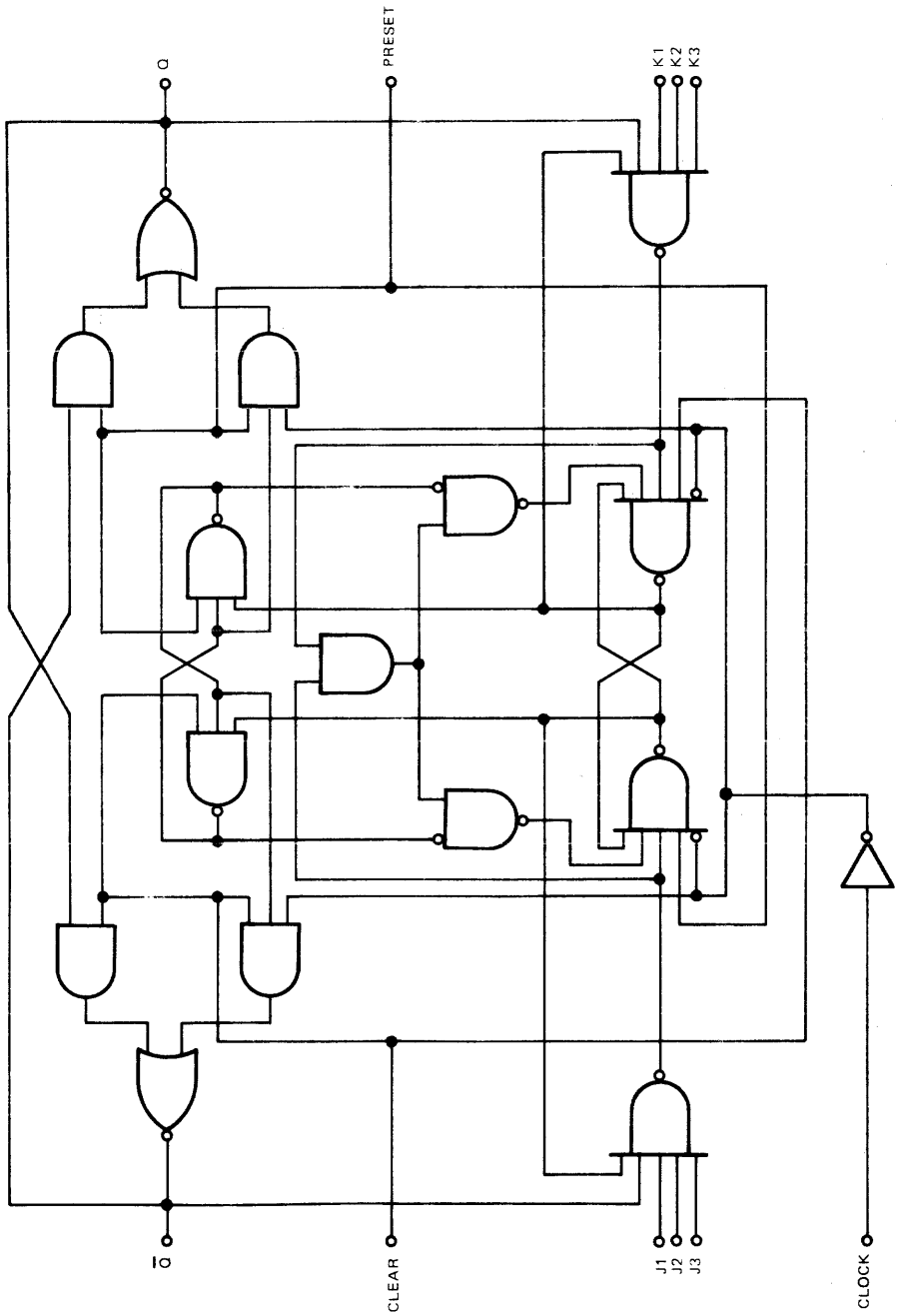
¶Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 114	20	25		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear or preset			12	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear or preset			18	25	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		10	20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		6	13	20	ns

6

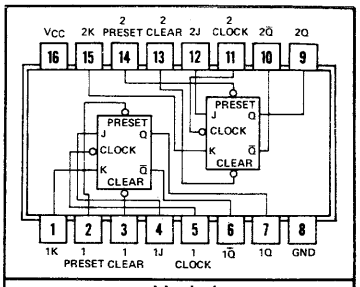
functional block diagram



CIRCUIT TYPES SN54111, SN74111
DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

- Data Lockout Solves Clock-Skew Problems
- Improved Immunity to Noise
- Input-Clamping Diodes Simplify System Design
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with Most TTL, DTL, and MSI Circuits
- Typical Maximum Input Clock Frequency . . . 25 MHz

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

†Pin assignments for these circuits are the same for all packages.

description

The SN54111 and SN74111 are d-c coupled, variable-skew, J-K flip-flops which utilize TTL circuitry to obtain 25-MHz performance typically. They are termed "variable-skew" because they allow the maximum clock skew in a system to be a direct function of the clock pulse width. The J and K inputs are enabled to accept data only during a short period (30 nanoseconds maximum hold time) starting with, and immediately following, the rising edge of the clock pulse as shown in the timing diagram, Figure 1. After this, inputs may be changed while the clock is at the high level without affecting the state of the master. At the threshold level of the falling edge of the clock pulse, the data stored in the master will be transferred to the output. The effective allowable clock skew then is minimum propagation delay time minus hold time, plus clock pulse width. This means that the system designer can set the maximum allowable clock skew needed by varying the clock pulse width. Thus system design is made easier and the requirements for sophisticated clock distribution systems are minimized or, in some cases, entirely eliminated. These flip-flops have an additional feature—the synchronous input has reduced sensitivity to data change while the clock is high because the data need be present for only a short period of time and the system's susceptibility to noise is thereby effectively reduced.

The SN54111 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74111 is characterized for operation from 0°C to 70°C.

TRUTH TABLE

INPUTS AT t_n		OUTPUT AT t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

H = high level, L = low level

NOTES: A. t_n = bit time before clock pulse.
B. t_{n+1} = bit time after clock pulse.

6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54111 Circuits . . . . . −55°C to 125°C
SN74111 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to the J input with respect to clear and clock, and to the K input with respect to preset and clock.

recommended operating conditions

		SN54111			SN74111			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of preset pulse, $t_{w(preset)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		25			25			ns
Input setup time, high-level or low-level data, t_{setup} (see Figure 115)		0			0			ns
Input hold time, high-level or low-level data, t_{hold} (see Figure 115)		30			30			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −800 μA	V_{IH} = 2 V,	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	J or K input	V_{CC} = MAX,	V_I = 2.4 V			40	μA
		Clear or Preset input					80	
		Clock input					120	
I_{IL}	Low-level input current	J or K input	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
		Clear or Preset input					−3.2	
		Clock input					−4.8	
I_{OS}	Short-circuit output current §		V_{CC} = MAX	SN54111	−20		−57	mA
				SN74111	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX,	See Note 3		28	41	mA

NOTE 3: With J and K inputs grounded, the clock input at 4.5 V, and the outputs open, I_{CC} is tested first with clear at 4.5 V and preset grounded, then with clear grounded and preset at 4.5 V.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

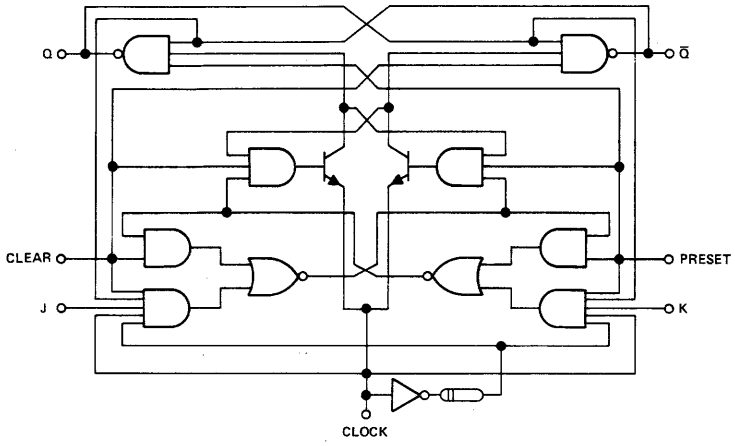
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 115	20	25		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear or preset			12	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear or preset			21	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		6	12	17	ns
t_{PHL}	Propaagtion delay time, high-to-low-level output from clock		10	20	30	ns

functional block diagram (each flip-flop)



CIRCUIT TYPES SN54121, SN74121
MONOSTABLE MULTIVIBRATORS

logic

TRUTH TABLE (See Notes 1 thru 3)

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	One Shot
X	0	0	X	0	1	One Shot
1	1	1	X	0	1	One Shot
1	1	1	0	X	1	One Shot
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

$1 = V_{in(1)} \geq 2\ V$

$0 = V_{in(0)} \leq 0.8\ V$

NOTES: 1. t_n = time before input transition.

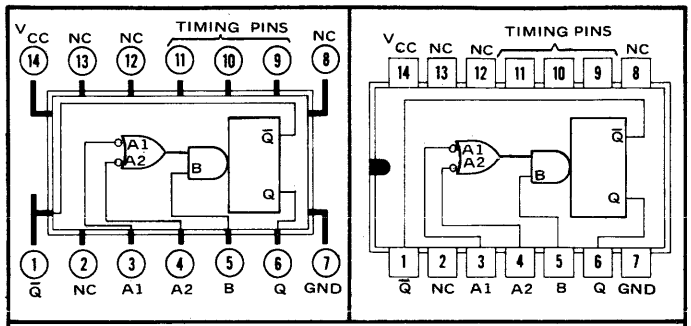
2. t_{n+1} = time after input transition.

3. X indicates that either a logical 0 or 1 may be present.

4. NC = No Internal Connection.

W FLAT PACKAGE
(TOP VIEW)
(See Notes 6 thru 9)

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)
(See Notes 6 thru 9)



positive logic: see truth table and notes 5 and 6

5. A1 and A2 are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.
6. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table)
7. External timing capacitor may be connected between pin (10) (positive) and pin (11). With no external capacitance, an output pulse width of typically 30 ns is obtained.
8. To use the internal timing resistor (2 kΩ nominal), connect pin (9) to pin (14).
9. To obtain variable pulse width connect external variable resistance between pin (9) and pin (14). No external current limiting is needed.
10. For accurate repeatable pulse widths connect an external resistor between pin (11) and pin (14) with pin (9) open-circuit.

description

This monolithic TTL monostable multivibrator features d-c triggering from positive or gated negative-going inputs with inhibit facility. Both positive and negative-going output pulses are provided with full fan-out to 10 normalized loads.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL compatible and featuring temperature-independent backlash, See Figure L) for the B input allows jitter-free triggering from inputs with transition times as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 40 nanoseconds to 40 seconds by choosing appropriate timing components. With no external timing components (i.e., pin (9) connected to pin (14), pins (10), (11) open) an output pulse of typically 30 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

description (continued)

Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 40 kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{p(out)} = C_T R_T \log_e 2$.

Circuit performance is achieved with a nominal power dissipation of 90 milliwatts at 5 volts (50% duty cycle) and a quiescent dissipation of typically 65 milliwatts.

Duty cycles as high as 90% are achieved when using R_T = 40 kΩ. Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54121 Circuits	4.5	5	5.5	V
SN74121 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Input Pulse Rise/Fall Time: Schmitt Input (B)			1	V/s
Logic Inputs (A1, A2)			1	V/μs
Input Pulse Width	50			ns
External Timing Resistance Between Pins (11) and (14) (Pin (9) open)	1.4			kΩ
External Timing Resistance: SN54121			30	kΩ
SN74121			40	kΩ
Timing Capacitance	0		1000	μF
Output Pulse Width			40	s
Duty Cycle: R_T = 2 kΩ			67%	
R_T = 30 kΩ (SN54121) or R_T = 40 kΩ (SN74121)			90%	

6

electrical characteristics over operating free-air temperature range

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNITS
V_{T+}	Positive-going threshold voltage at A input	57	V_{CC} = MIN			1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	57	V_{CC} = MIN		0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	57	V_{CC} = MIN			1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	57	V_{CC} = MIN		0.8	1.35		V
$V_{out(0)}$	Logical 0 output voltage	57	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$V_{out(1)}$	Logical 1 output voltage	57	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.3		V
$I_{in(0)}$	Logical 0 level input current at A1 or A2	58	V_{CC} = MAX, V_{in} = 0.4 V			−1	−1.6	mA
$I_{in(0)}$	Logical 0 level input current at B	59	V_{CC} = MAX, V_{in} = 0.4 V			−2	−3.2	mA
$I_{in(1)}$	Logical 1 level input current at A1 or A2	60	V_{CC} = MAX, V_{in} = 2.4 V			2	40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			0.05	1	mA
$I_{in(1)}$	Logical 1 level input current at B	61	V_{CC} = MAX, V_{in} = 2.4 V			4	80	μA
			V_{CC} = MAX, V_{in} = 5.5 V			0.05	1	mA
I_{OS}	Short circuit output current at Q or $\overline{Q}$§	62 and 63	V_{CC} = MAX	SN54121	−20	−25	−55	mA
				SN74121	−18	−25	−55	
I_{CC}	Power supply current in quiescent (unfired) state	64	V_{CC} = MAX			13	25	mA
I_{CC}	Power supply current in fired state	64	V_{CC} = MAX			23	40	mA

6

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd1}	Propagation delay time to logical 1 level from B input to Q output	72	C_L = 15 pF,	C_T = 80 pF	15	35	55	ns
t_{pd1}	Propagation delay time to logical 1 level from A1/A2 inputs to Q output				25	45	70	ns
t_{pd0}	Propagation delay time to logical 0 level from B input to $\overline{Q}$ output	72	C_L = 15 pF,	C_T = 80 pF	20	40	65	ns
t_{pd0}	Propagation delay time to logical 0 level from A1/A2 inputs to $\overline{Q}$ output				30	50	80	ns
$t_{p(out)}$	Pulse width obtained using internal timing resistor	73	C_L = 15 pF, R_T = Open,	C_T = 80 pF, Pin ⑨ to V_{CC}	70	110	150	ns
$t_{p(out)}$	Pulse width obtained with zero timing capacitance	73	C_L = 15 pF, R_T = Open,	C_T = 0, Pin ⑨ to V_{CC}	20	30	50	ns
$t_{p(out)}$	Pulse width obtained using external timing resistor	73	C_L = 15 pF, R_T = 10 kΩ,	C_T = 100 pF, Pin ⑨ Open	600	700	800	ns
			C_L = 15 pF, R_T = 10 kΩ,	C_T = 1 μF, Pin ⑨ Open	6	7	8	ms
t_{hold}	Minimum duration of trigger pulse	73	C_L = 15 pF, R_T = Open,	C_T = 80 pF, Pin ⑨ to V_{CC}		30	50	ns

TYPICAL CHARACTERISTICS§

DISTRIBUTION OF UNITS
for
OUTPUT PULSE WIDTH

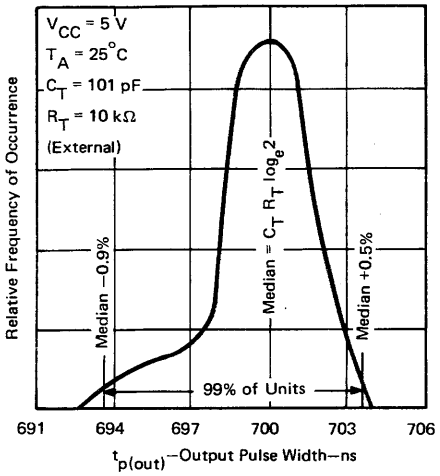


FIGURE H

VARIATION IN INTERNAL TIMING RESISTOR VALUE
vs
FREE-AIR TEMPERATURE

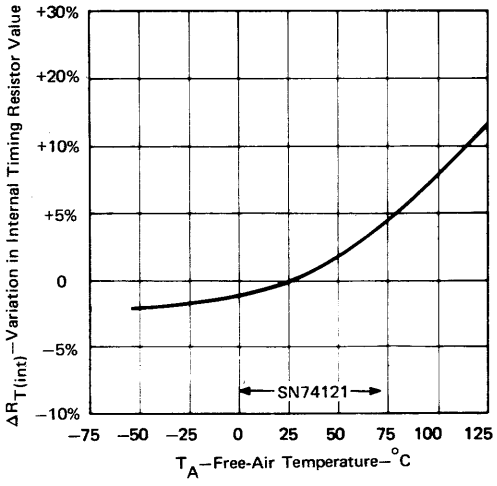


FIGURE I

6

VARIATION IN OUTPUT PULSE WIDTH
vs
SUPPLY VOLTAGE

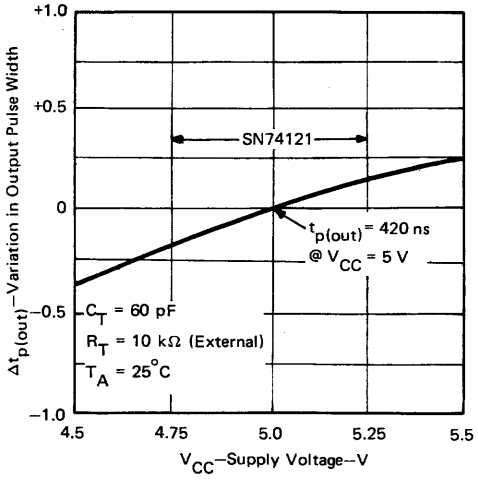


FIGURE J

VARIATION IN OUTPUT PULSE WIDTH
vs
FREE-AIR TEMPERATURE

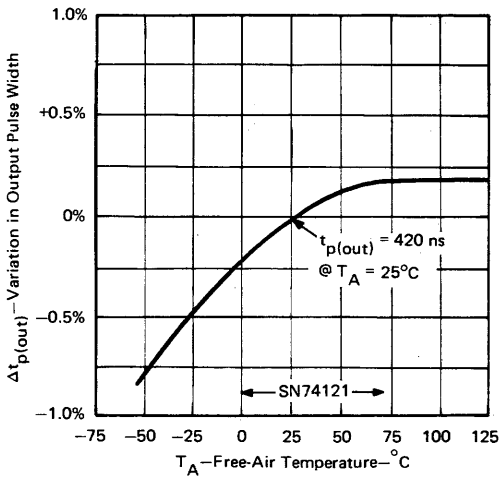


FIGURE K

§ Unless otherwise noted data is applicable for SN54121 and SN74121.

TYPICAL CHARACTERISTICS§

SCHMITT TRIGGER THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

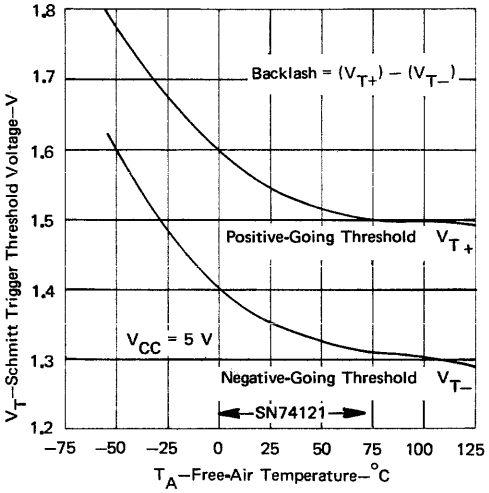


FIGURE L

PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL
(B INPUT TO Q OUTPUT)
vs
FREE-AIR TEMPERATURE

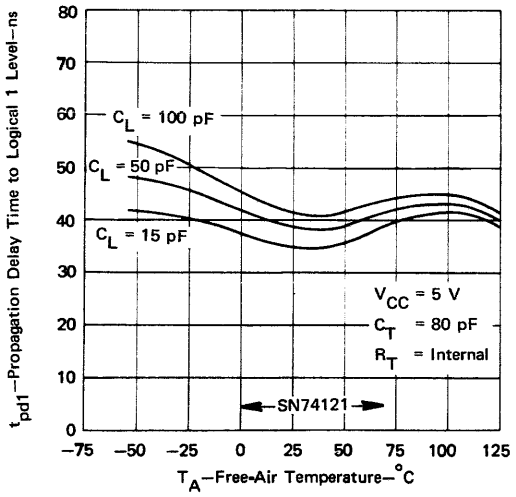


FIGURE M

PROPAGATION DELAY TIME TO LOGICAL 0 LEVEL
(B INPUT TO $\overline{Q}$ OUTPUT)
vs
FREE-AIR TEMPERATURE

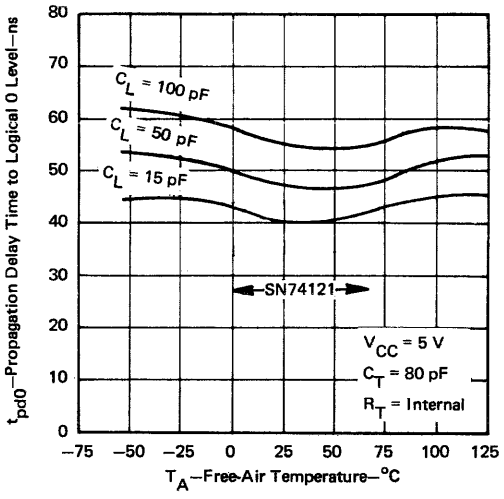


FIGURE N

§Unless otherwise noted data is applicable for SN54121 and SN74121.

TYPICAL CHARACTERISTICS §

OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE

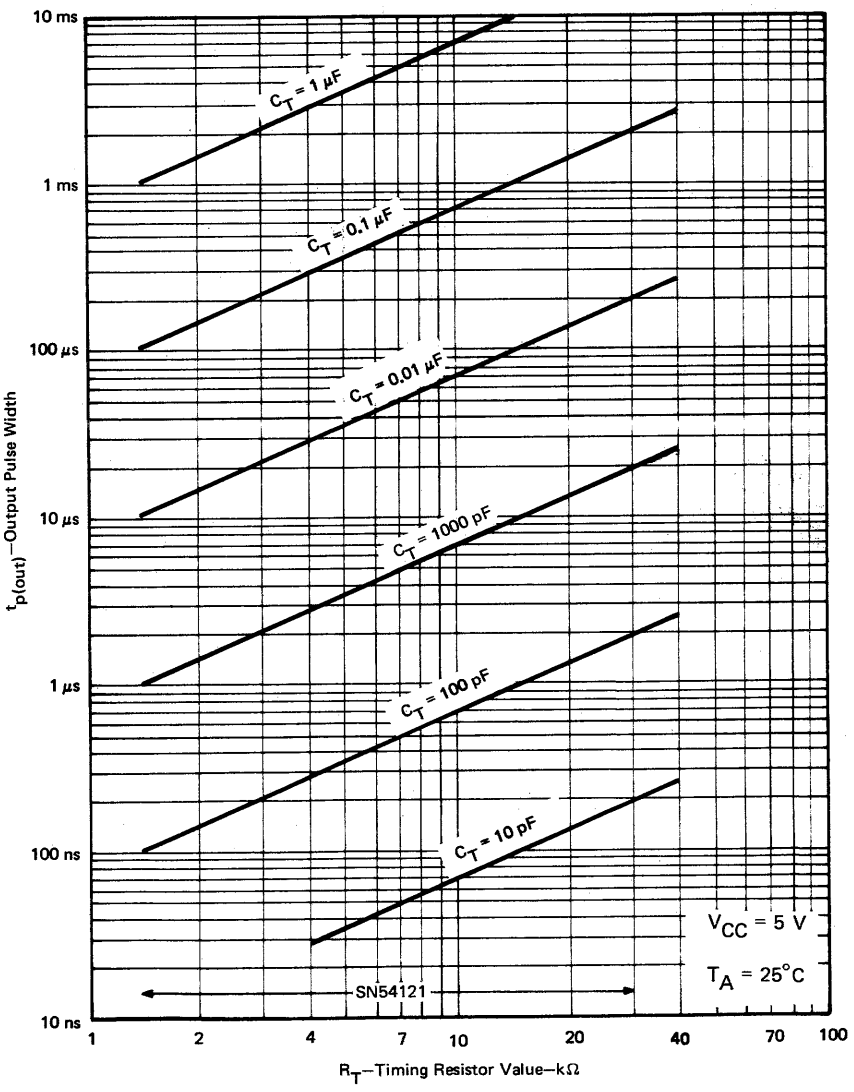


FIGURE O

§ Unless otherwise noted data is applicable for SN54121 and SN74121.

6

TYPICAL CHARACTERISTICS §

OUTPUT PULSE WIDTH
vs
EXTERNAL CAPACITANCE

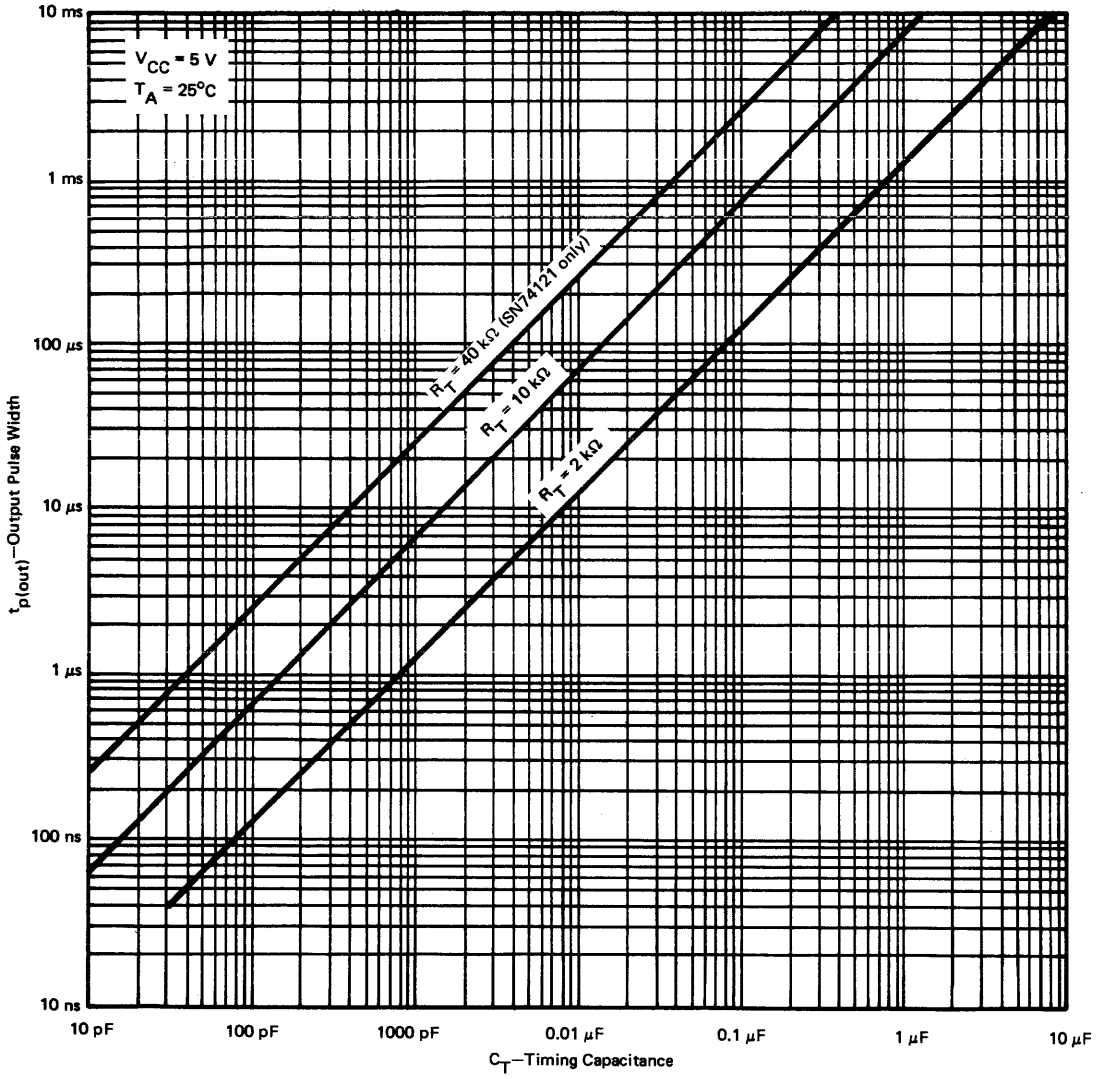


FIGURE P

§ Unless otherwise noted data is applicable for SN54121 and SN74121.

CIRCUIT TYPES SN54122, SN54123, SN74122, SN74123
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

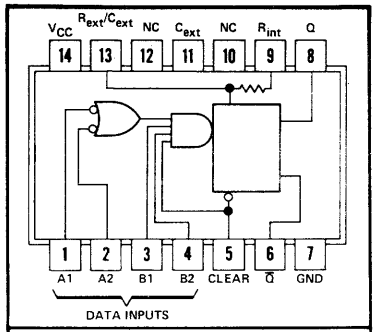
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Diode-Clamped Inputs
- D-C Triggered from High- or Low-Level Gated Logic Inputs
- Compatible for Use with TTL or DTL
- Typical Average Propagation Delay to Output Q . . . 21 ns

logic

SN54122, SN74122
TRUTH TABLE
(See Note A)

INPUTS				OUTPUTS	
A1	A2	B1	B2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎎
L	X	H	↑	⎍	⎎
X	L	H	H	L	H
X	L	↑	H	⎍	⎎
X	L	H	↑	⎍	⎎
H	↓	H	H	⎍	⎎
↓	↓	H	H	⎍	⎎
↓	H	H	H	⎍	⎎

SN54122, SN74122
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†
(SEE NOTES B THRU D)

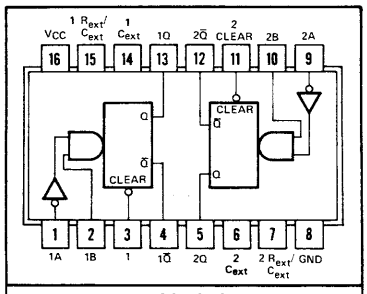


positive logic:
Low input to clear resets Q to low level and inhibits data inputs

SN54123, SN74123
TRUTH TABLE
(See Note A)

INPUTS		OUTPUTS	
A	B	Q	$\overline{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎎
↓	H	⎍	⎎

SN54123, SN74123
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†
(SEE NOTE D)



positive logic:
Low input to clear resets Q to low level and inhibits data inputs

†Pin assignments for these circuits are the same for all packages.

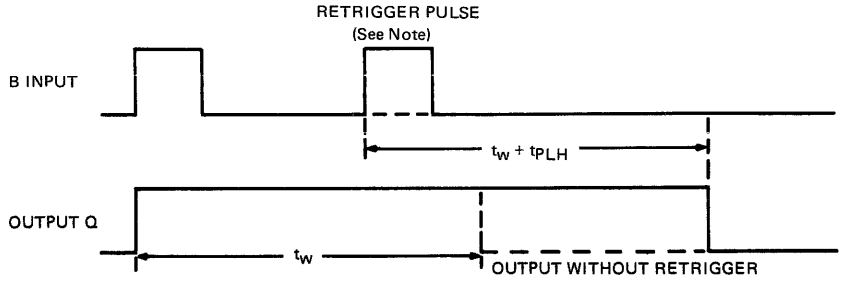
NOTES: A. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎎ = one low-level pulse, X = irrelevant (any input, including transitions).
B. NC = No internal connection.
C. To use the internal timing resistor of SN54122/SN74122 (10 kΩ nominal), connect R_{int} to V_{CC}.
D. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).

CIRCUIT TYPES SN54122, SN54123, SN74122, SN74123
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

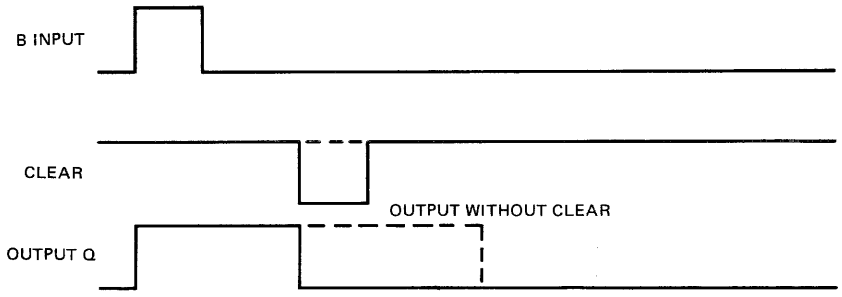
description

These monolithic TTL retriggerable monostable multivibrators feature d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. A full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs at the low logic level, and in the high-level state, a fan-out of 20 is available. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C.

Figure A below illustrates triggering the one-shot with the high-level-active (B) inputs.



OUTPUT PULSE CONTROL USING RETRIGGER PULSE



OUTPUT PULSE CONTROL USING CLEAR INPUT

FIGURE A—TYPICAL INPUT/OUTPUT PULSES

NOTE: Retrigger pulse must not start before 0.22 C_{ext} (in picofarads) nanoseconds after previous trigger pulse.

description (continued)

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. SN54122/SN74122 has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired. Applications requiring more precise pulse widths and not requiring the clear feature can best be satisfied with SN54121/SN74121.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse width (t_w) is defined as:

$$t_w = 0.32\ R_T C_{ext} \left(1 + \frac{0.7}{R_T}\right)$$

where

R_T is in kΩ (either internal or external timing resistor)
C_{ext} is in pF
t_w is in ns

For pulse widths when $C_{ext} \leqslant 1000$ pF, see Figure 3.

These circuits are fully compatible with most TTL or DTL families. Inputs are diode-clamped to minimize reflections due to transmission-line effects, which simplifies design. Typical power dissipation per one shot is 115 milliwatts; typical average propagation delay time to the Q output is 21 nanoseconds. The SN54122 and SN54123 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74122 and SN74123 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage, SN54122, SN74122 Circuits only (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54122, SN54123 Circuits . . . . . −55°C to 125°C
SN74122, SN74123 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

6

recommended operating conditions

		SN54122, SN54123			SN74122, SN74123			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input data setup time, t_{setup} (see Note 3 and Figure 116)		40†			40†			ns
Input data hold time, t_{hold} (see Note 4 and Figure 116)		40†			40†			ns
Width of clear pulse, $t_{w(clear)}$		40†			40†			ns
External timing resistance		5		25	5		50	kΩ
External capacitance		No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal				50			50	pF
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

†These conditions are recommended for use at $V_{CC} = 5$ V, $T_A = 25°C$.

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For the SN54122/SN74122 circuit, this rating applies to each A input with respect to the other and to each B input with respect to the other.
3. Setup time for a dynamic input is the interval immediately preceding the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure recognition of the transition.
4. Hold time for a dynamic input is the interval immediately following the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure continued recognition of the transition.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, See Note 5	I_{OH} = −800 μA,	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, See Note 5	I_{OL} = 16 mA,		0.22	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	data inputs	V_{CC} = MAX,	V_I = 2.4 V			40	μA
		clear input					80	
I_{IL}	Low-level input current	data inputs	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
		clear input					−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX,	See Note 5	−10		−40	mA
I_{CC}	Supply current (quiescent or triggered)		V_{CC} = MAX, See Notes 6 and 7	SN54122, SN74122		23	28	mA
				SN54123, SN74123		46	66	

†For conditions shown as MIN or MAX, use the value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

NOTES: 5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
6. Quiescent I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of SN54122/SN74122 is open.
7. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of SN54122/SN74122 is open.

6

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either A input	C_{ext} = 0, C_L = 15 pF, See Figure 116	R_{ext} = 5 kΩ, R_L = 400 Ω,		22	33	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either B input				19	28	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either A input				30	40	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either B input				27	36	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output, from clear input				18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}$ output, from clear input				30	40	ns
$t_{w(min)}$	Minimum width of Q output pulse				45	65	ns
t_w	Width of Q output pulse	C_{ext} = 1000 pF, C_L = 15 pF,	R_{ext} = 10 kΩ, R_L = 400 Ω	3.08	3.42	3.76	μs

TYPICAL CHARACTERISTICS

OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE

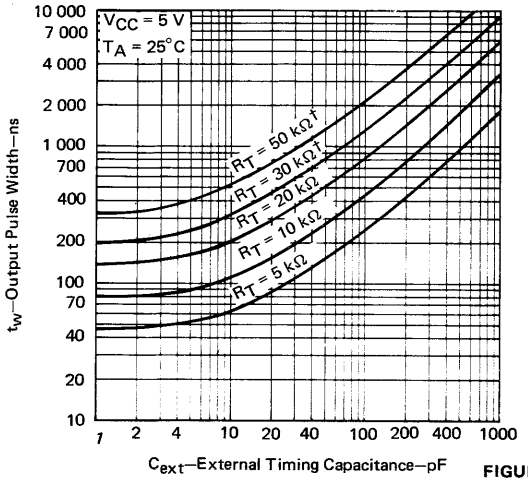
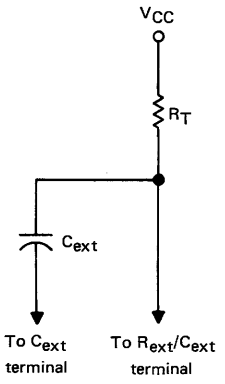


FIGURE B

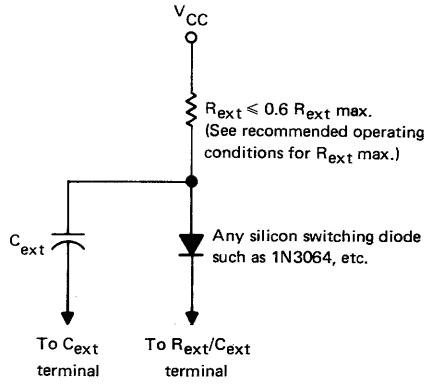
†These values of resistance exceed the maximums recommended for use over the full temperature range of the SN54122 and SN54123.

TYPICAL APPLICATION DATA



TIMING COMPONENT CONNECTIONS WHEN $C_{ext} \leq 1000$ pF

FIGURE C



TIMING COMPONENT CONNECTIONS WHEN $C_{ext} > 1000$ pF AND CLEAR IS USED

FIGURE D

To prevent reverse voltage across C_{ext}, it is recommended that the method shown in Figure D be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse width is:

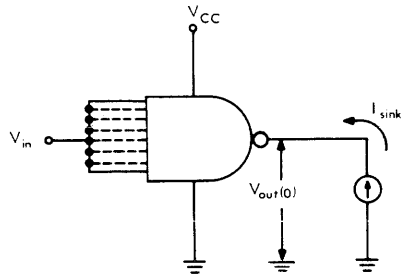
$$t_w = 0.28\ R_{ext}C_{ext}\left(1 + \frac{0.7}{R_{ext}}\right)$$

where

R_{ext} is in kΩ
C_{ext} is in pF
t_w is in ns

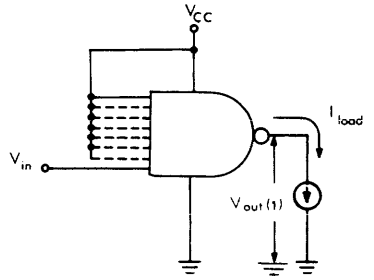
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



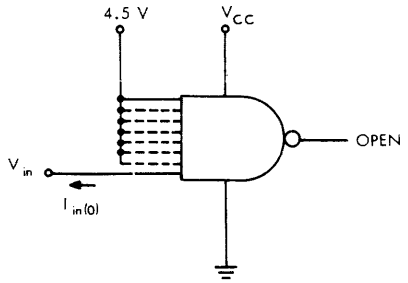
1. All inputs are tested simultaneously.

FIGURE 1



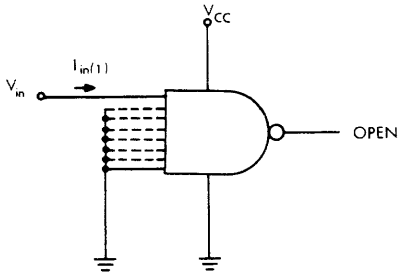
1. Each input is tested separately.

FIGURE 2



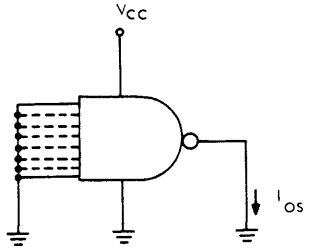
1. Each input is tested separately.

FIGURE 3



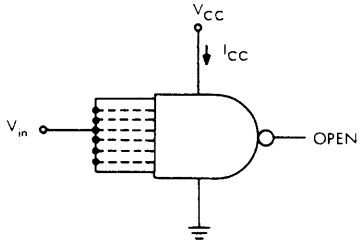
1. Each input is tested separately.

FIGURE 4



1. Each gate is tested separately.

FIGURE 5



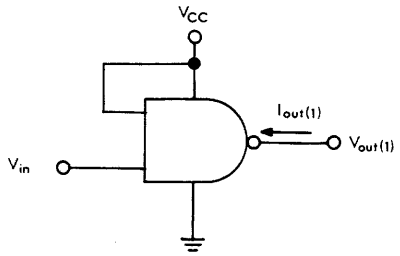
1. Logical 0 and logical 1 conditions are tested.
2. All gates are tested simultaneously.

FIGURE 6

§ Arrows indicate actual direction of current flow.

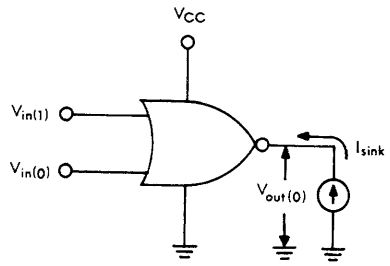
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



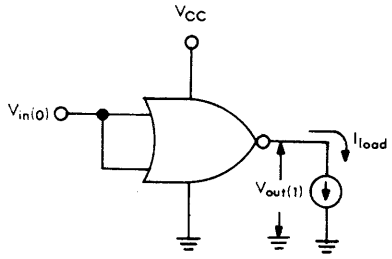
1. Each input is tested separately.

FIGURE 7



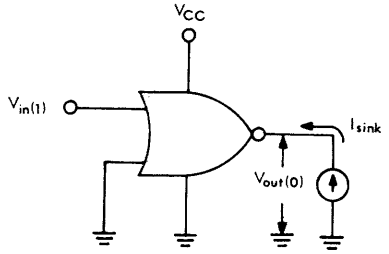
1. Each input is tested separately.

FIGURE 8



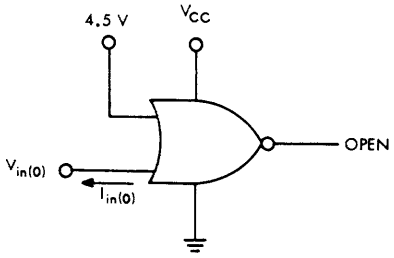
1. Both inputs are tested simultaneously.

FIGURE 9



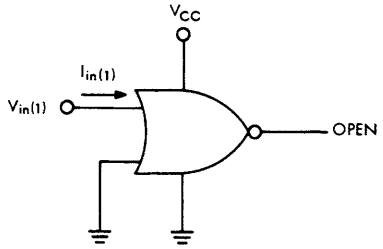
1. Each input is tested separately.

FIGURE 10



1. Each input is tested separately.

FIGURE 11



1. Each input is tested separately.

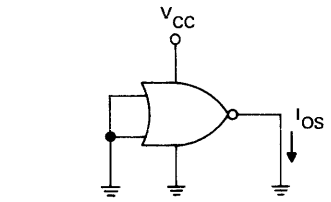
FIGURE 12

§Arrows indicate actual direction of current flow.

6

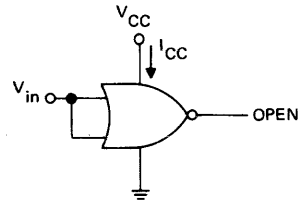
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each gate is tested separately.

FIGURE 13



1. Logical 0 and logical 1 conditions are tested.
2. All gates are tested simultaneously.

FIGURE 14

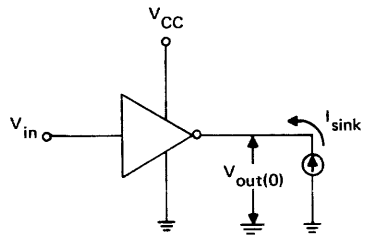


FIGURE 15

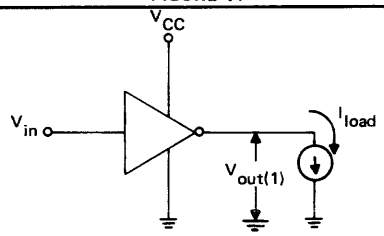


FIGURE 16

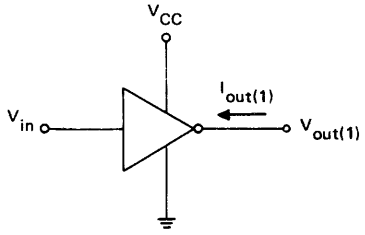


FIGURE 17

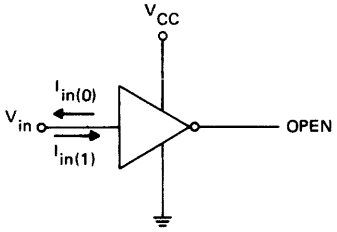
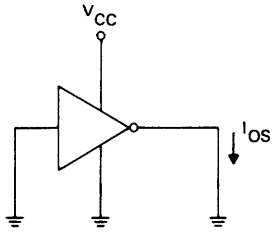
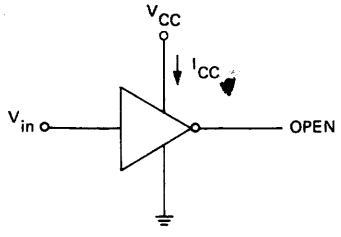


FIGURE 18



1. Each inverter is tested separately.

FIGURE 19



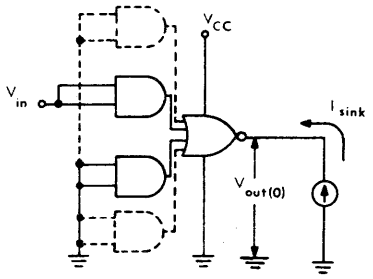
1. All inverters are tested simultaneously.

FIGURE 20

§Arrows indicate actual direction of current flow

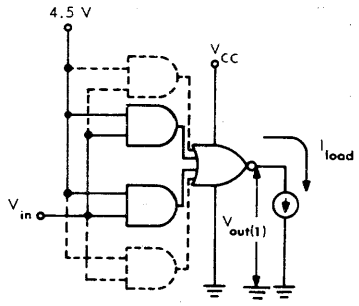
PARAMETER MEASUREMENT INFORMATION

d-c test circuits § (continued)



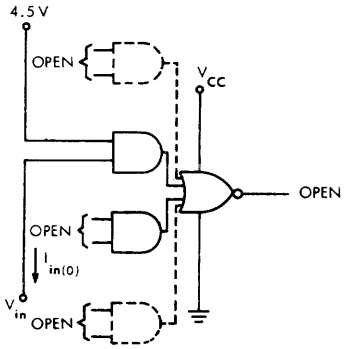
1. Each AND section is tested separately.

FIGURE 21



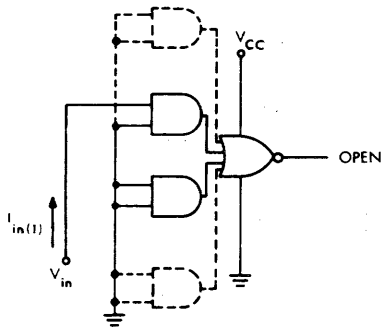
1. Each pair of inputs is tested separately.

FIGURE 22



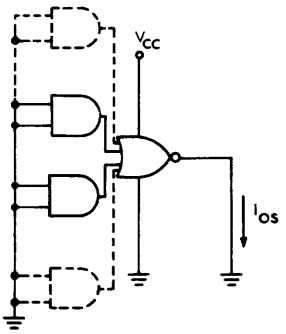
1. Each input is tested separately.

FIGURE 23



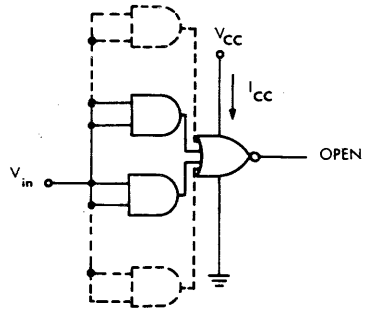
1. Each input is tested separately.

FIGURE 24



1. Each gate is tested separately.

FIGURE 25



1. All gates are tested simultaneously.

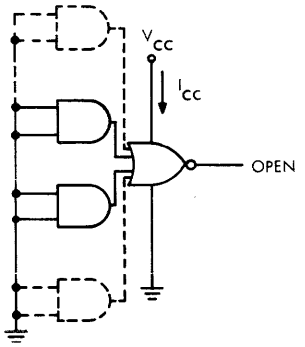
FIGURE 26

§ Arrows indicate actual direction of current flow.

6

PARAMETER MEASUREMENT INFORMATION

d-c test circuits § (continued)



1. All gates are tested simultaneously.

FIGURE 27

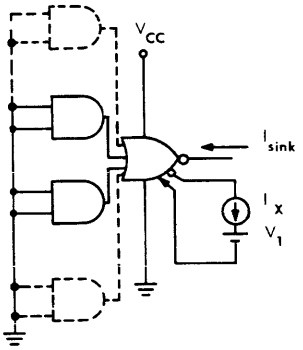


FIGURE 28

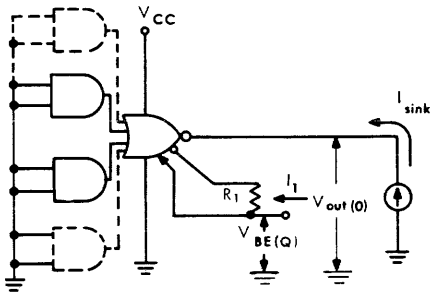


FIGURE 29

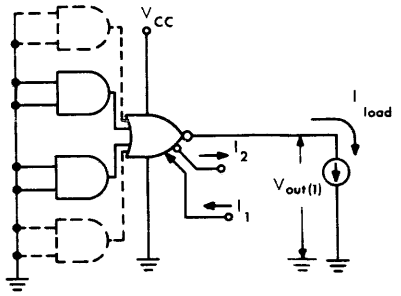
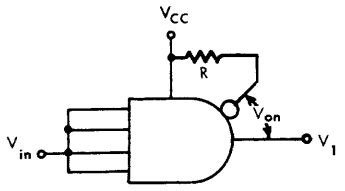
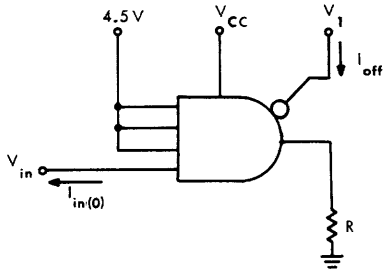


FIGURE 30



1. All inputs are tested simultaneously.

FIGURE 31



1. Each input is tested separately.

FIGURE 32

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

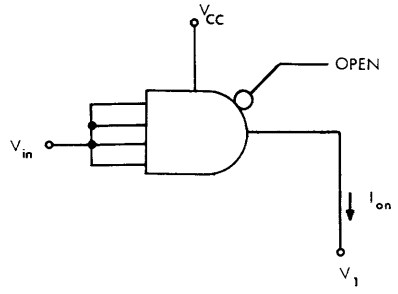
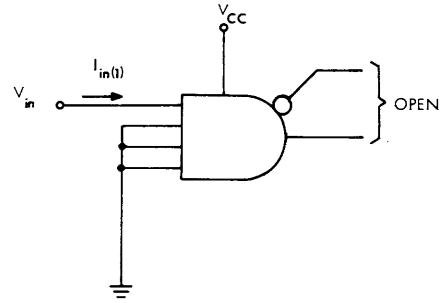
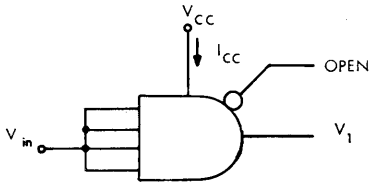


FIGURE 33



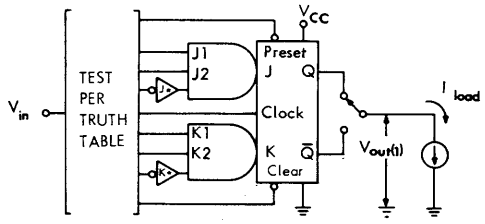
1. Each input is tested separately.

FIGURE 34



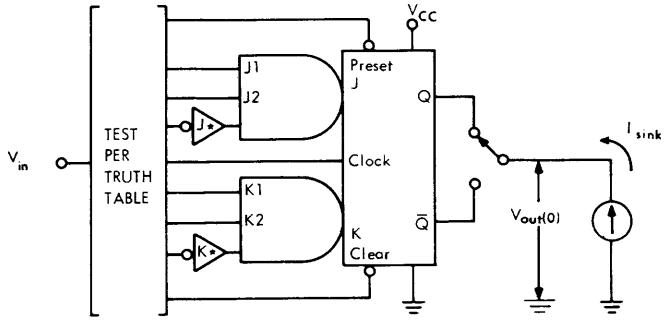
1. "On" and "off" conditions are tested separately.
2. All gates are tested simultaneously.

FIGURE 35



1. Each output is tested separately.
2. Preset and clear are tested with $V_{in(clock)} = 0$.

FIGURE 36



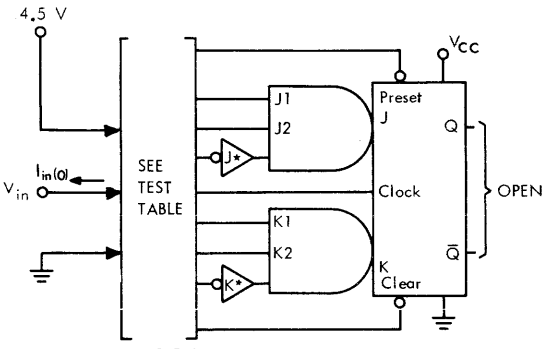
1. Each output is tested separately.

FIGURE 37

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

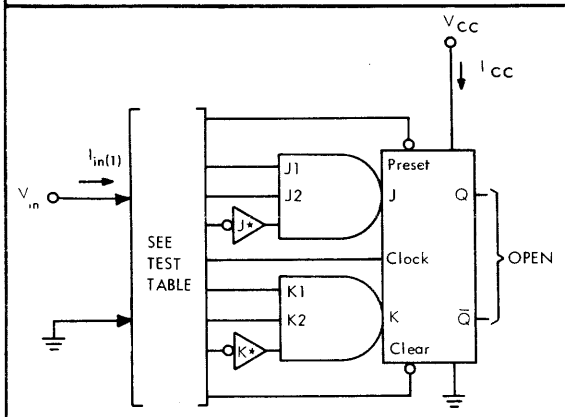
d-c test circuits § (continued)



1. Each output is tested separately.

TEST TABLE			
Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	Ground	Apply Momentary GND, then 4.5 V
J2	J1	J★	Clear
J1	J2	J★	Clear
J★	None	None	None
K2	K1	K★	Preset
K1	K2	K★	Preset
K★	None	None	None
Clock	None	None	None
Preset	K1 and K2	K★	None
Clear	J1 and J2	J★	None

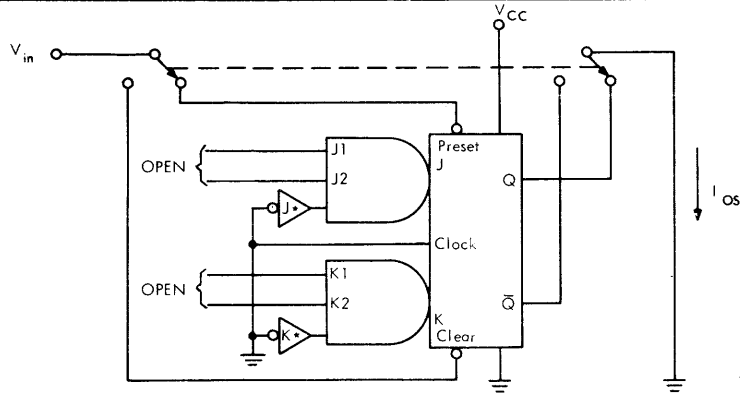
FIGURE 38



TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply 4.5 V
J2	J1 and Clear	J★
J1	J2 and Clear	J★
J★	None	None
K2	K1 and Preset	K★
K1	K2 and Preset	K★
K★	None	None
Clock	None	None
Preset	K1 and K2	K★
Clear	J1 and J2	J★

1. Each input is tested separately.
2. I_{CC} is measured with clear at GND, then with preset at GND.

FIGURE 39



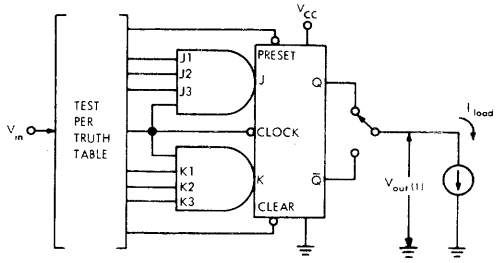
1. Each output is tested separately.

FIGURE 40

§ Arrows indicate actual direction of current flow.

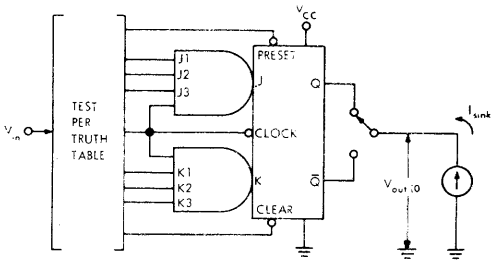
PARAMETER MEASUREMENT INFORMATION

d-c test circuits § (continued)



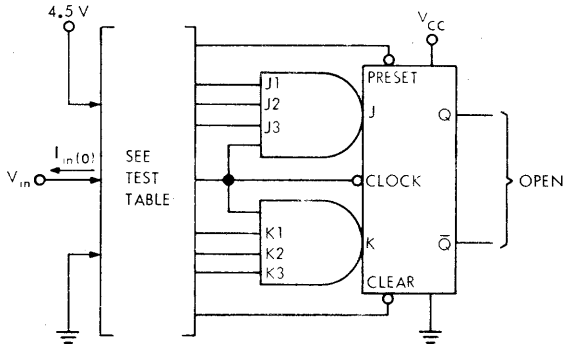
1. Each output is tested separately.

FIGURE 41



1. Each output is tested separately.

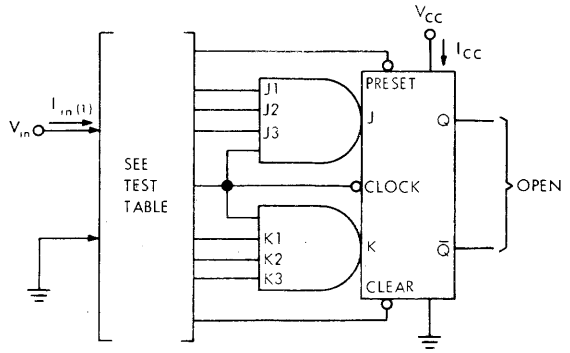
FIGURE 42



1. Each input is tested separately.

TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND, then 4.5 V	Apply 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

FIGURE 43



1. Each input is tested separately.
2. I_{CC} is measured with clear at GND, then with preset at GND.

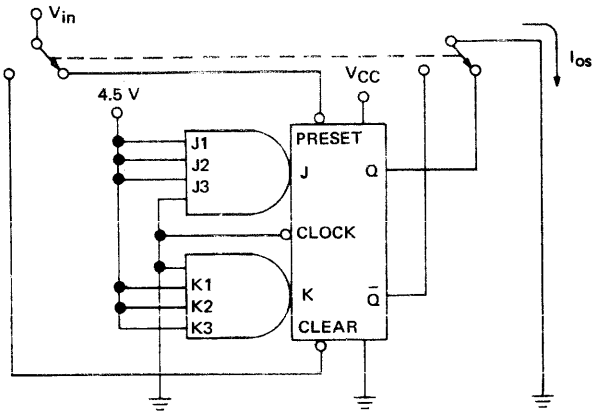
TEST TABLE	
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2, and K3
Clear	Clock, J1, J2, and J3
J1	Clock, Clear, J2, and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

FIGURE 44

§Arrows indicate actual direction of current flow.

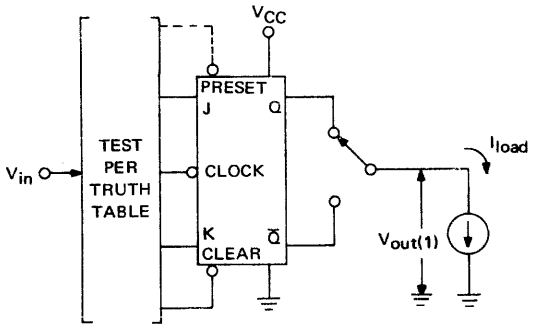
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



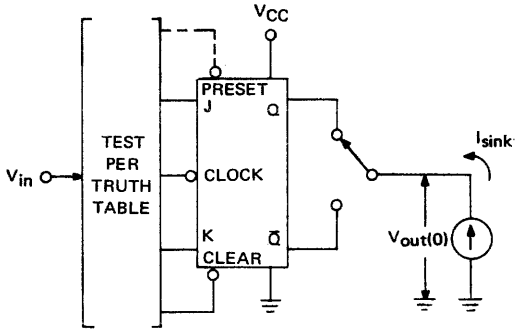
1. Each output is tested separately.

FIGURE 45



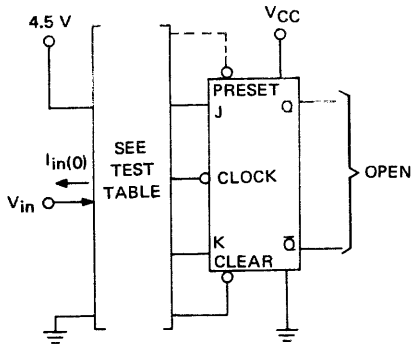
1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 46



1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 47



TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
Preset	None (See Note 5)	Clock and K
J	Q (See Note 3)	Clock and Clear
K	$\bar{Q}$ (See Note 3)	Clock and Clear

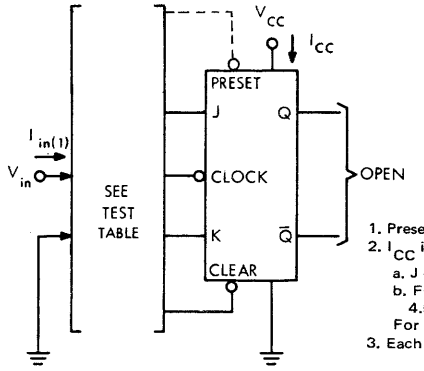
1. Each flip-flop is tested separately.
2. Apply momentary ground, then 4.5 V.
3 After application of momentary ground, Q and $\bar{Q}$ are left floating.
4. Ground all inputs of the unused flip-flop.
5. Preset is applicable for SN5476/SN7476 circuits only.

FIGURE 48

§ Arrows indicate actual direction of current flow

PARAMETER MEASUREMENT INFORMATION

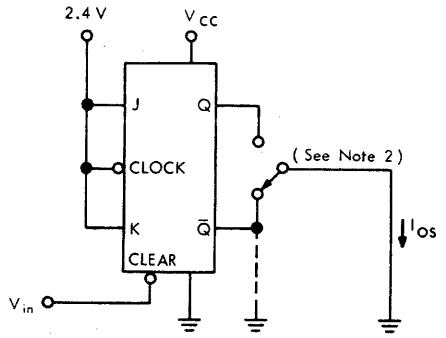
d-c test circuits§ (continued)



TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
Preset (See Note 1)	Clock and K	None
J (See Note 1)	Clock and Clear	Preset
K (See Note 1)	Clock and Preset	Clear

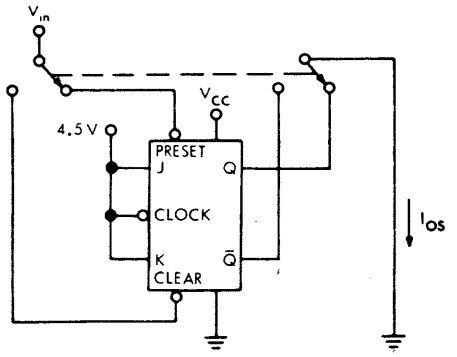
1. Preset is applicable for SN5476/SN7476 circuits only.
2. I_{CC} is measured (simultaneously for both flip-flops) for the following conditions:
   a. J = K = Clock = Clear = GND. For SN5476/SN7476: Preset = 4.5 V.
   b. For SN5473/SN7473: J = Clear = 4.5 V, K = GND, and apply momentary 4.5 V, then GND to Clock.
   For SN5476/SN7476: J = K = Clock = Preset = GND, and Clear = 4.5 V.
3. Each flip-flop is tested separately for $I_{in(1)}$.

FIGURE 49



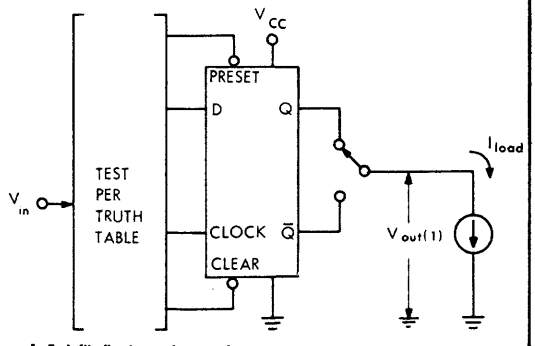
1. Each flip-flop is tested separately.
2. Test circuit shows setup for testing $\bar{Q}$. When testing Q, apply 2.4 V to Clear, ground $\bar{Q}$, and limit duration of test to 100 ms.

FIGURE 50



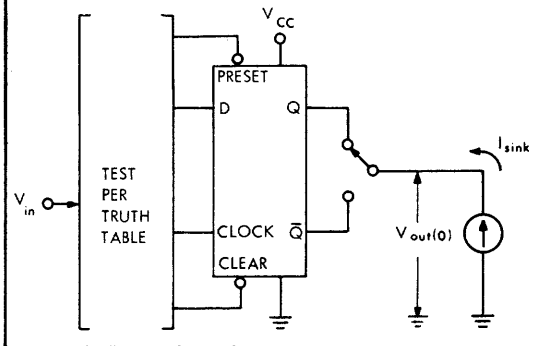
1. Each flip-flop is tested separately.

FIGURE 51



1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 52



1. Each flip-flop is tested separately.
2. Each output is tested separately.

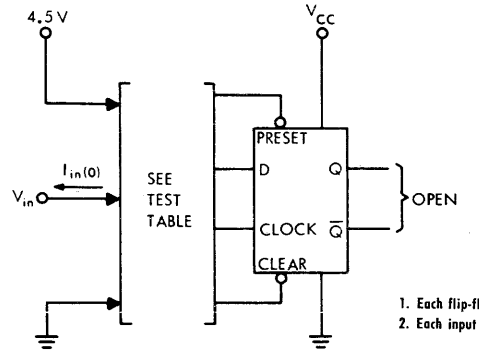
FIGURE 53

§Arrows indicate actual direction of current flow.

6

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

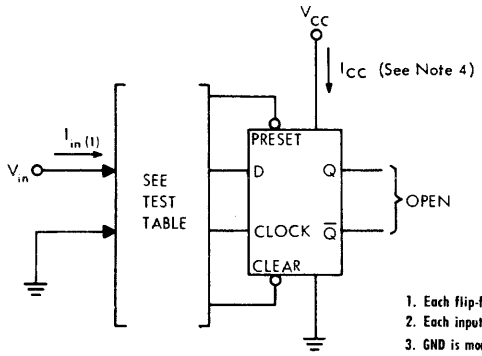


TEST TABLE

APPLY V_{in} (TEST $I_{in(0)}$)	APPLY 4.5 V	APPLY GND
Clock	Clear	Preset and D
Preset	Clear	Clock and D
Clear	Clock, D, and Preset	None
D	Clear and Clock	Preset

1. Each flip-flop is tested separately.
2. Each input is tested separately.

FIGURE 54

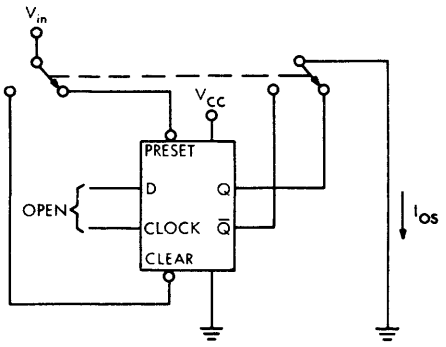


TEST TABLE

APPLY V_{in} (TEST $I_{in(1)}$)	APPLY 4.5 V	APPLY GND
Clock	Clear and D	Preset
Clock	Preset and D	Clear
Preset	Clear and D	Clock (See Note B)
Clear	Preset	Clock, D, and Q
Clear	Preset	D and Clock (See Note B)
D	Preset and Clock	Clear

1. Each flip-flop is tested separately.
2. Each input is tested separately.
3. GND is momentarily applied to clock, then 4.5 V.
4. I_{CC} is measured with D, clock, and preset at GND, then with D, clock, and clear at GND.

FIGURE 55



1. Each output is tested separately.

FIGURE 56

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

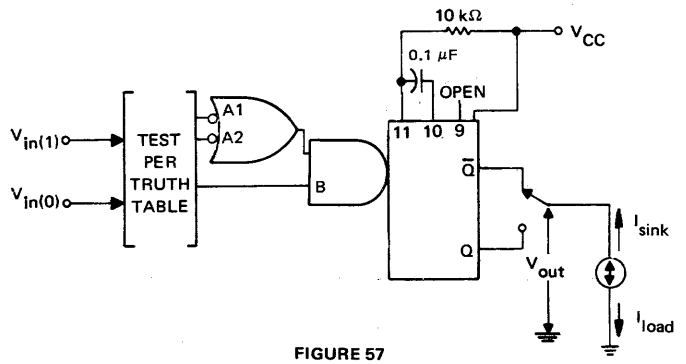
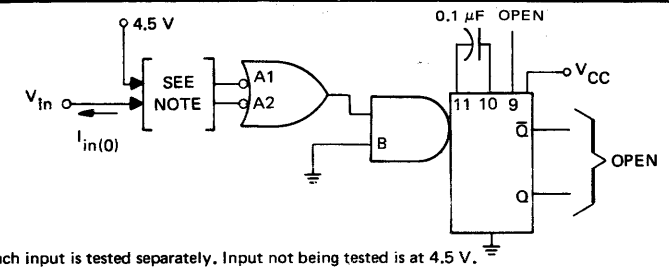


FIGURE 57



1. Each input is tested separately. Input not being tested is at 4.5 V.

FIGURE 58

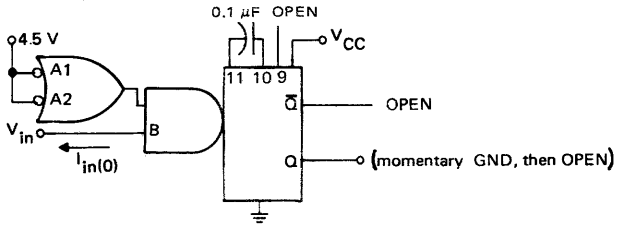
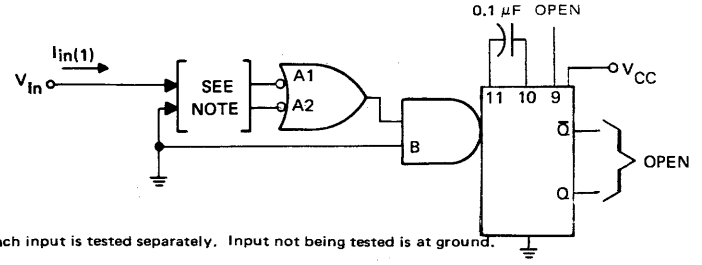


FIGURE 59



1. Each input is tested separately. Input not being tested is at ground.

FIGURE 60

§ Arrows indicate actual direction of current flow.

6

d-c test circuits § (continued) PARAMETER MEASUREMENT INFORMATION

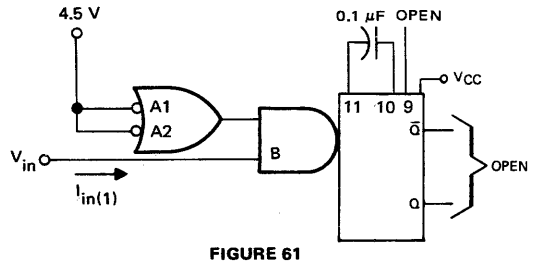
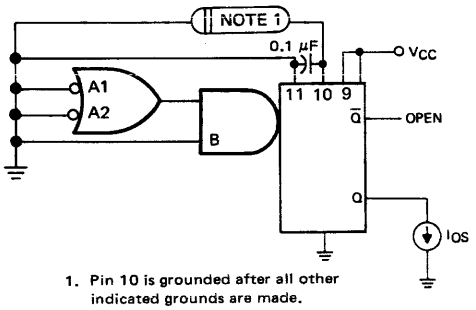


FIGURE 61



1. Pin 10 is grounded after all other indicated grounds are made.

FIGURE 62

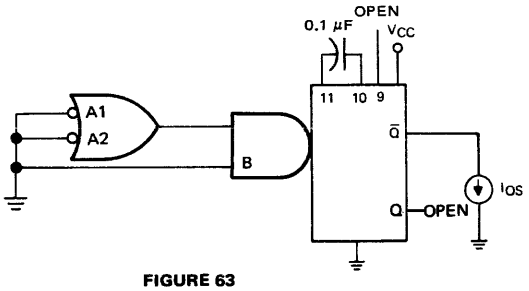
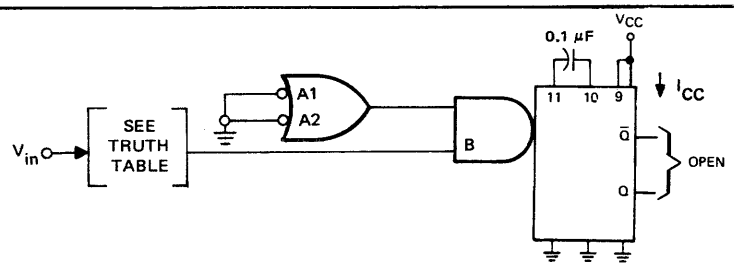


FIGURE 63



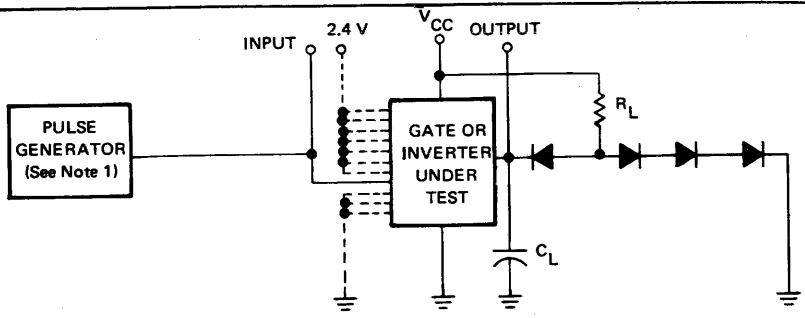
1. Quiescent and fired conditions are tested.

FIGURE 64

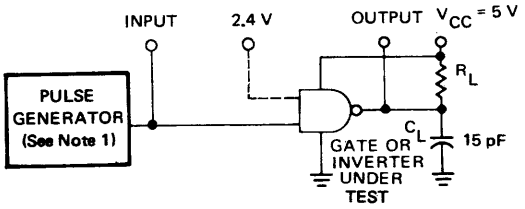
§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

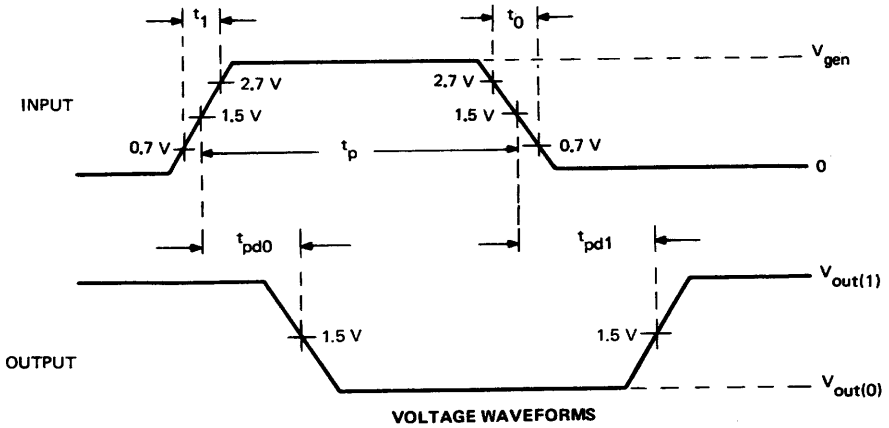
switching characteristics



TEST CIRCUIT FOR SN5400, SN5402, SN5404, SN5410, SN5420, SN5430, SN5440, SN5450, SN5451, SN5453, SN5454, SN7400, SN7402, SN7404, SN7410, SN7420, SN7430, SN7440, SN7450, SN7451, SN7453, AND SN7454



TEST CIRCUIT FOR SN5401, SN5403, SN5405, SN7401, SN7403, SN7405



VOLTAGE WAVEFORMS

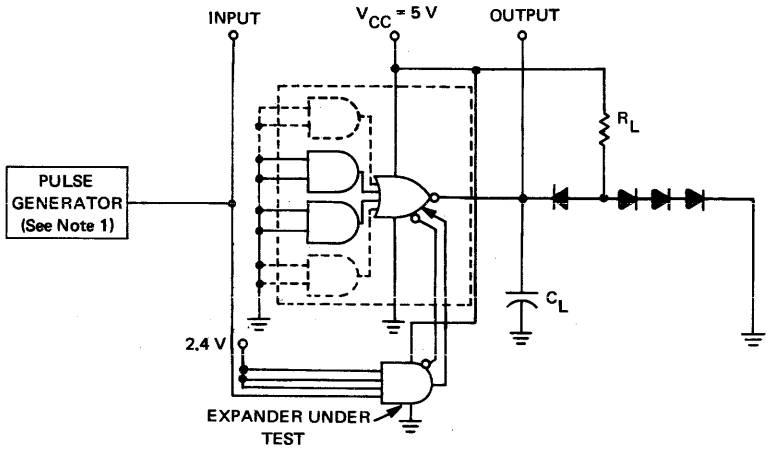
NOTES: 1. The generator has the following charactertistic: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. $t_{pd} = \dfrac{t_{pd0} + t_{pd1}}{2}$
4. C_L includes probe and jig capacitance.
5. When testing the SN5400/SN7400 through SN5440/SN7440 (except SN5402/SN7402) connect all unused inputs to 2.4 V. When testing the SN5402/SN7402 or SN5450/SN7450 through SN5454/SN7454, apply the input pulse to one input of one AND section and 2.4 V to all unused inputs of that AND section. All inputs of unused AND sections are grounded.

FIGURE 65-GATE PROPAGATION DELAY TIMES

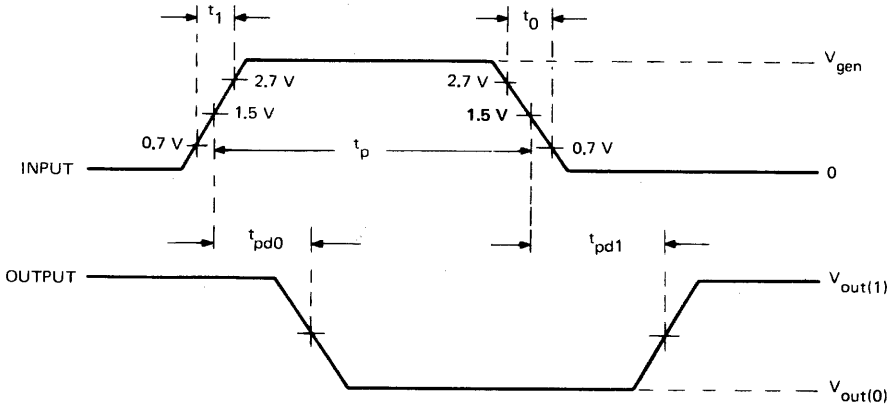
6

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



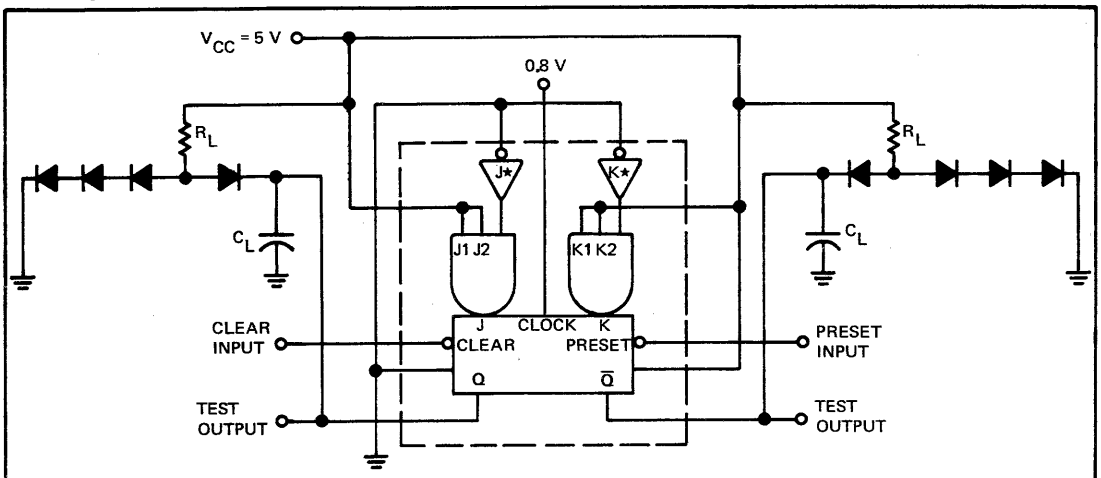
VOLTAGE WAVEFORMS

NOTES:
1. The generator has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. $t_{pd} = \dfrac{t_{pd0} + t_{pd1}}{2}$
4. C_L includes probe and jig capacitance.

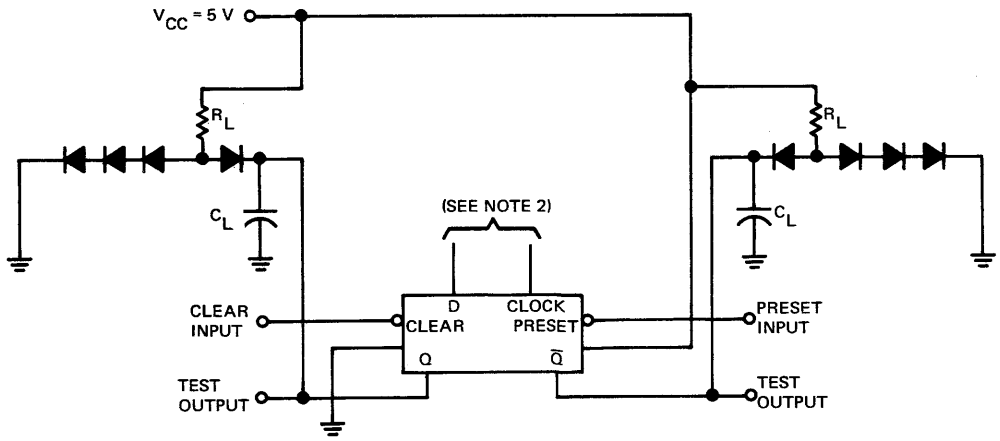
FIGURE 66—EXPANDER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



SN5470/SN7470 TEST CIRCUIT



SN5474/SN7474 TEST CIRCUIT

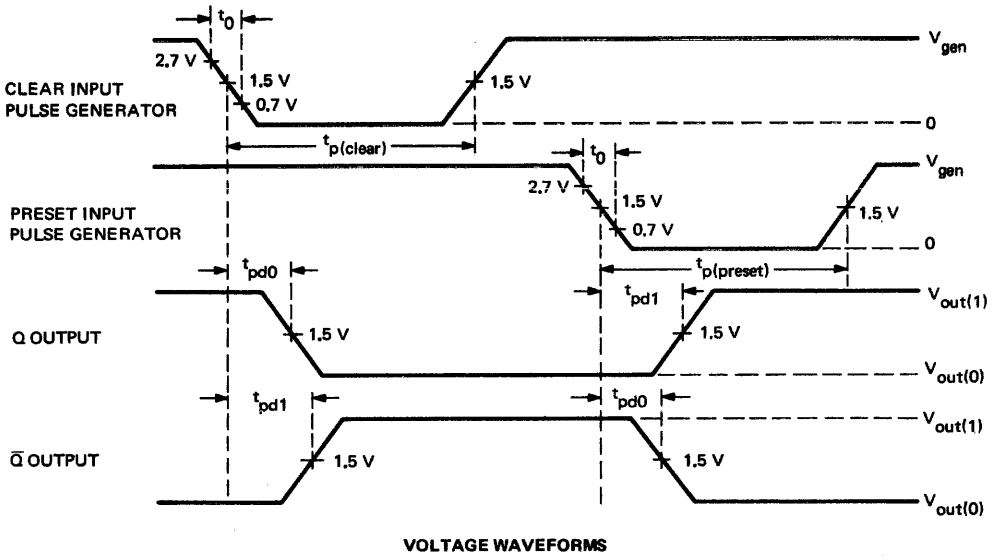
NOTES:
1. Preset or clear function of the SN5470/SN7470 can occur only when clock input is low. Gated inputs are inhibited.
2. Clear and preset inputs of the SN5474/SN7474 dominate regardless of the state of clock or D inputs.
3. All diodes are 1N3064.
4. C_L includes probe and jig capacitance.

FIGURE 67–SN5470/SN7470 AND SN5474/SN7474 PRESET/CLEAR PROPAGATION DELAY TIMES (SHEET 1 OF 2)

6

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



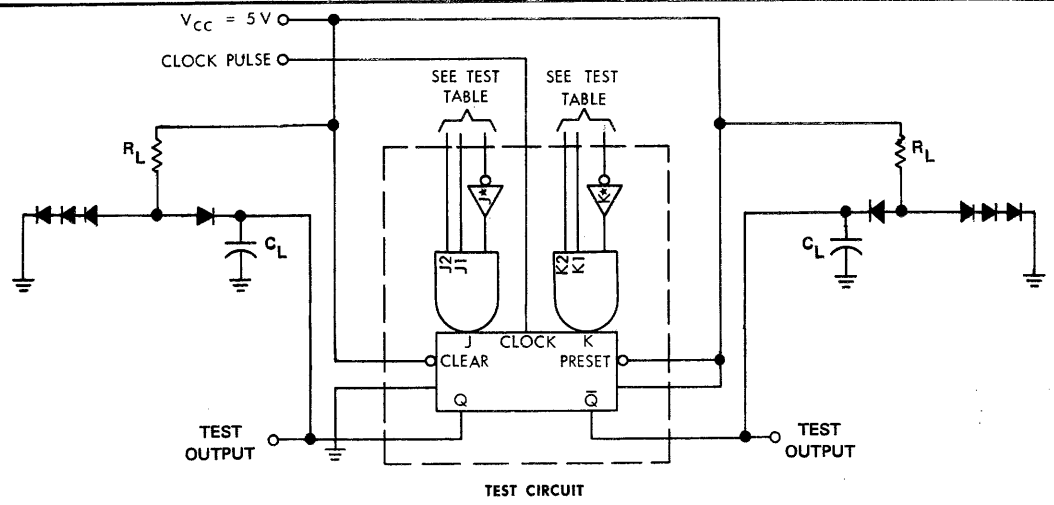
VOLTAGE WAVEFORMS

NOTE 6: Clear or preset input pulse characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_p = 25 ns for the SN5470/SN7470, and t_p = 30 ns for SN5474/SN7474.

FIGURE 67—SN5470/SN7470 AND SN5474/SN7474 PRESET/CLEAR PROPAGATION DELAY TIMES (SHEET 2 OF 2)

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT

TEST TABLE					
TEST NO.	TEST	INPUT A	INPUT B	APPLY 2.4 V	GND
1	t_{setup} at J★	J★	None	J1, J2, K1, K2	K★
2	t_{hold} at J1, J2	None	J1, J2	K1, K2	J★ and K★
3	t_{setup} at K★	K★	None	J1, J2, K1, K2	J★
4	t_{hold} at K1, K2	None	K1, K2	J1, J2	J★ and K★

NOTES: 1. Clock pulse (see note 3), input A, and input B are used to measure t_{setup} and t_{hold}.

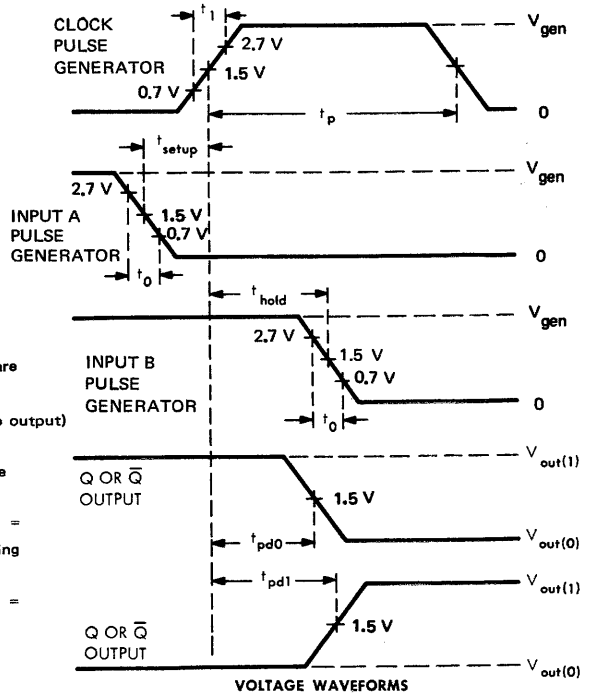
2. Clock frequency, t_{pd1}, and t_{pd0} (from clock to output) are measured in the toggle mode. Hold J = K = Logical 1 per truth table and apply clock pulse (see note 3).

3. Clock pulse characteristics: V_{gen} = 3.5 V, t_1 = 10 ns, t_p = 20 ns, and PRR = 1 MHz. When testing f_{max}, vary PRR.

4. Input pulse characteristics: V_{gen} = 3.5 V, t_0 = 5 ns.

5. All diodes are 1N3064.

6. C_L includes probe and jig capacitance.



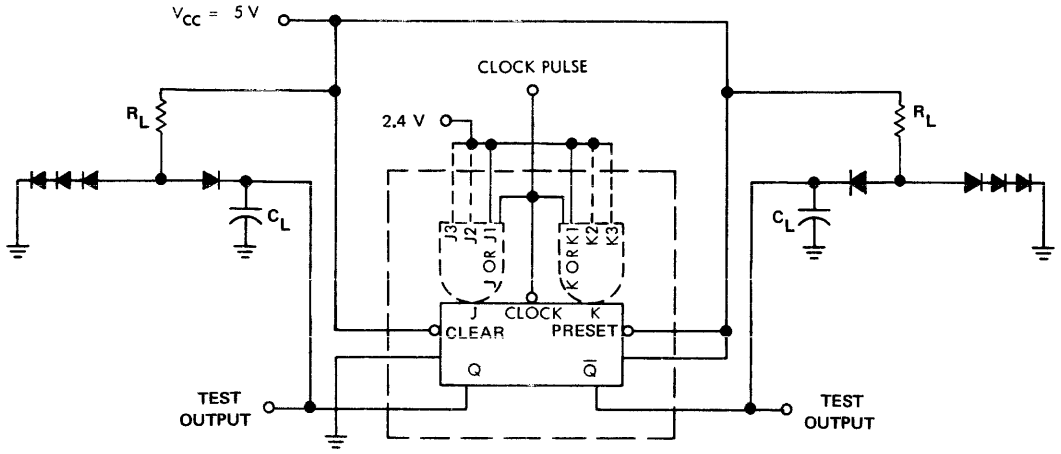
VOLTAGE WAVEFORMS

FIGURE 68–SN5470/SN7470 FLIP-FLOP SWITCHING TIMES

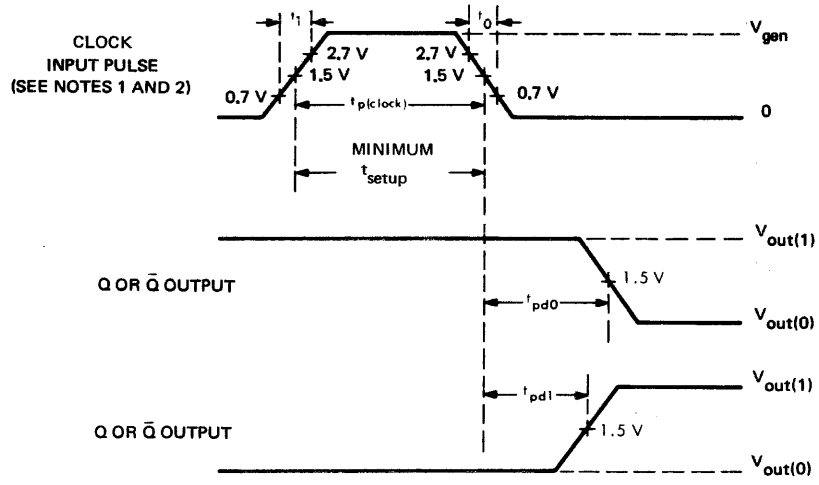
6

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



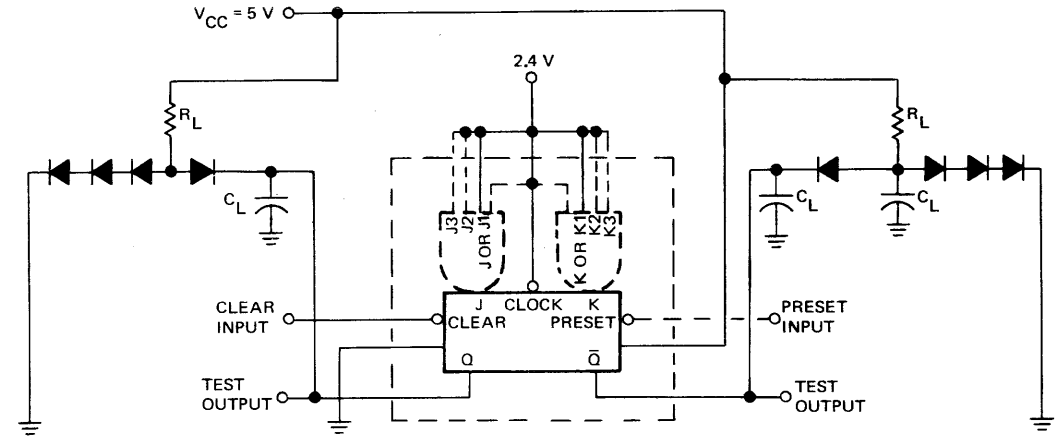
VOLTAGE WAVEFORMS

NOTES:
1. Clock, J, and K input pulse characteristics: V_{gen} = 3.5 V, t_0 = 10 ns, t_1 = 10 ns, t_p = 20 ns, and PRR = 1 MHz. When testing f_{max}, vary PRR.
2. For the SN5472/SN7472, J = J1 • J2 • J3; and K = K1 • K2 • K3.
3. Gated inputs (shown with dotted lines) are for the SN5472/SN7472 only. The SN5473/SN7473, SN54107/SN74107 and SN5476/SN7476. Dual Flip-Flops have direct J and K inputs, and preset is not available on the SN5473/SN7473 and SN54107/SN74107.
4. All diodes are 1N3064.
5. C_L includes probe and jig capacitance.

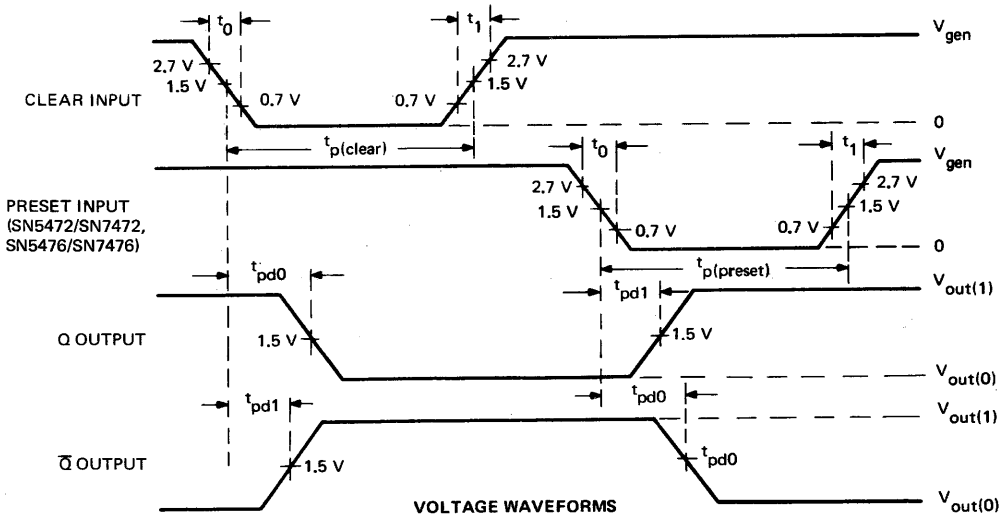
FIGURE 69—SN5472/SN7472, SN5473/SN7473, SN5476/SN7476, SN54107/SN74107 FLIP-FLOP SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

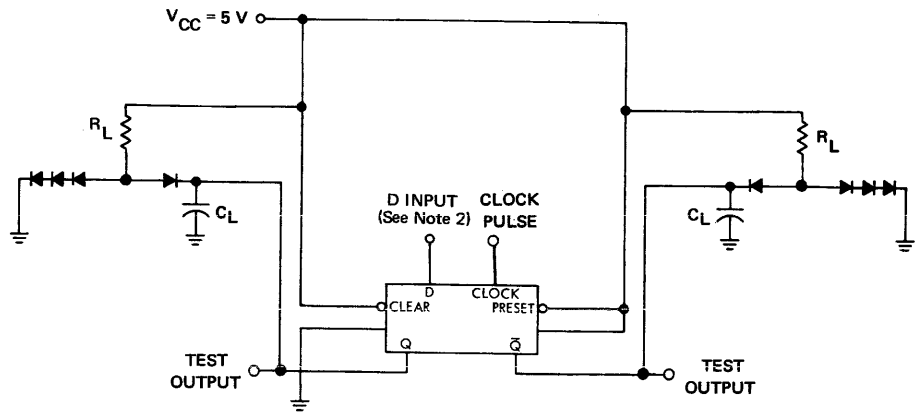
1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. Clear or preset input pulse characteristics: V_{CC} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, $t_{p(clear)} = t_{p(preset)}$ = 25 ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
3. Gates inputs (shown with dotted lines) are for the SN5472/SN7472 only. The SN5473/SN7473, SN5476/SN7476, and SN54107/SN74107 Dual Flip-Flops have direct J and K inputs, and preset is not available on the SN5473/SN7473 or SN54107/SN74107.
4. All diodes are 1N3064.
5. C_L includes probe and jig capacitance.

FIGURE 70–SN5472/SN7472, SN5473/SN7473, SN5476/SN7476, SN54107/SN74107 PRESET/CLEAR PROPAGATION DELAY TIMES

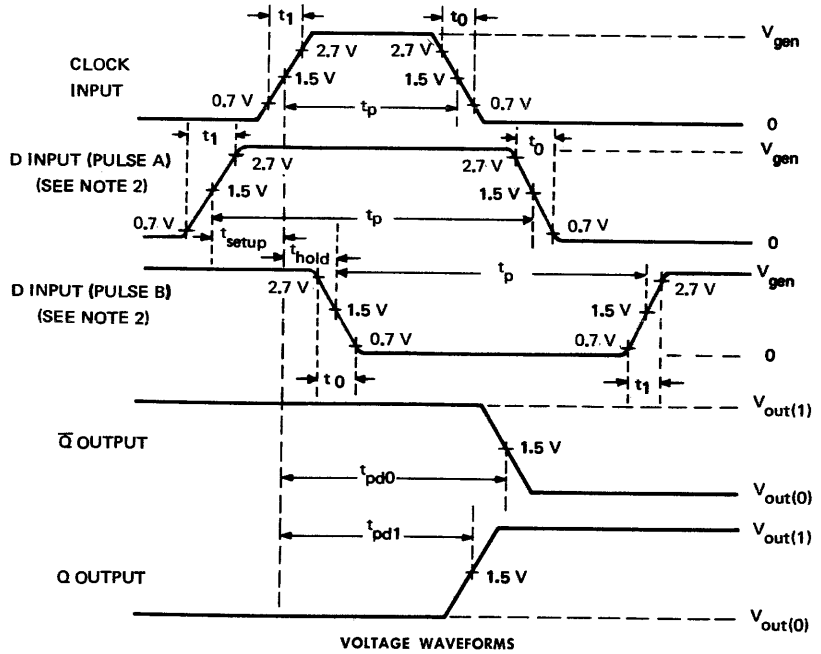
6

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



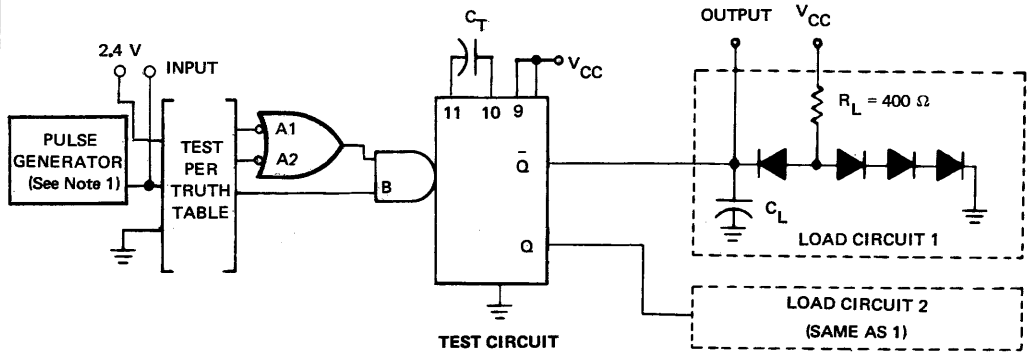
VOLTAGE WAVEFORMS

NOTES:
1. Clock input pulse has the following characteristics: V_{gen} = 3.5 V, t_0 = 10 ns, t_1 = 10 ns, t_p = 30 ns, and PRR = 1 MHz. When testing f_{max}, vary PRR.
2. D input (pulse A) has the following characteristics: V_{gen} = 3.5 V, t_0 = 10 ns, t_1 = 10 ns, t_{setup} = 20 ns, t_p = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: V_{gen} = 3.5 V, t_0 = 10 ns, t_1 = 10 ns, t_{hold} = 5 ns, t_p = 60 ns, and PRR is 50% of the clock PRR.
3. All diodes are 1N3064.
4. C_L includes probe and jig capacitance.

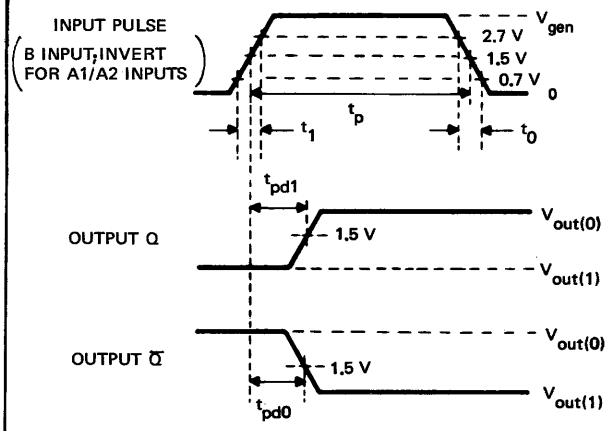
FIGURE 71—SN5474/SN7474 FLIP-FLOP SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



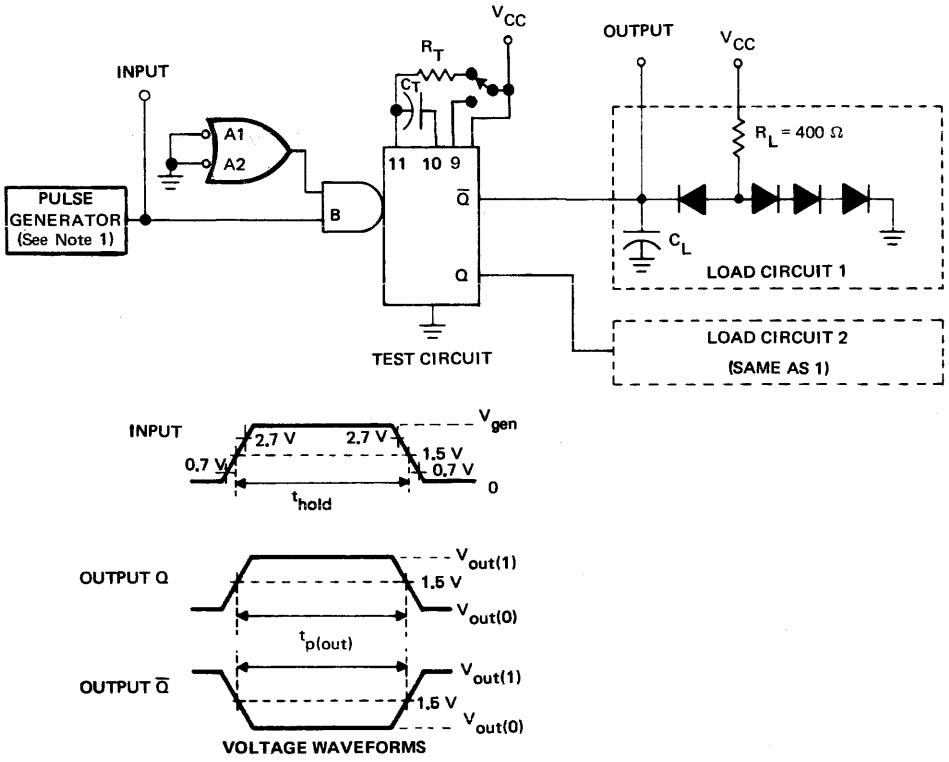
VOLTAGE WAVEFORMS

1. The pulse generator has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, $t_p \geq 50$ ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. C_L includes probe and jig capacitance.

FIGURE 72–SN54121/SN74121 SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



1. The pulse generator has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_p = 50 ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. C_L includes probe and jig capacitance.

FIGURE 73–$t_{p(out)}$ (internal/minimum), t_{hold}

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§

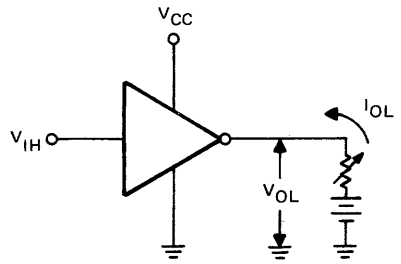


FIGURE 74–V_{IH}, V_{OL}

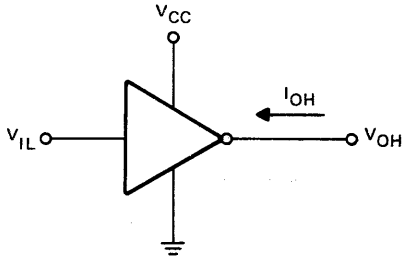


FIGURE 75–V_{IL}, I_{OH}

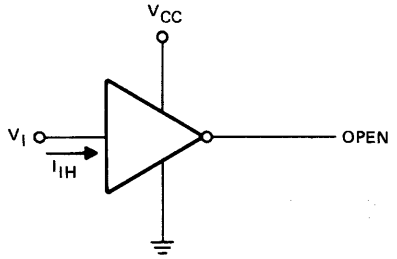


FIGURE 76–I_{IH}

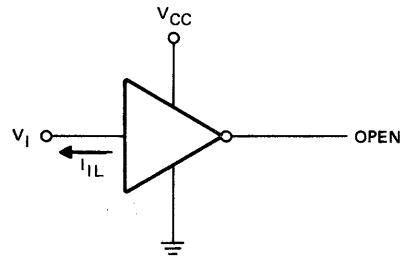
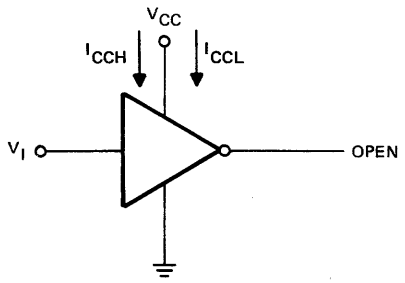


FIGURE 77–I_{IL}



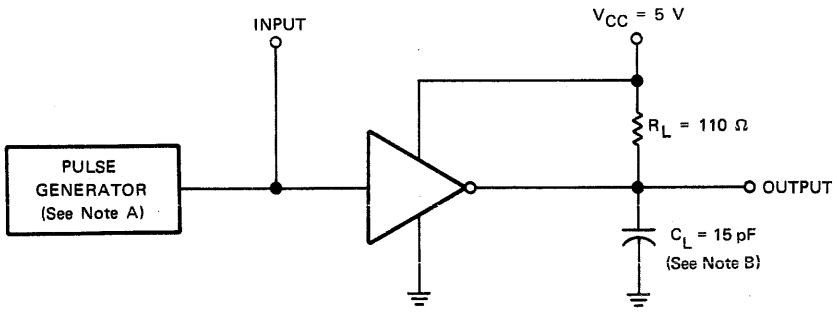
All inverters are tested simultaneously.

FIGURE 78–I_{CCH}, I_{CCL}

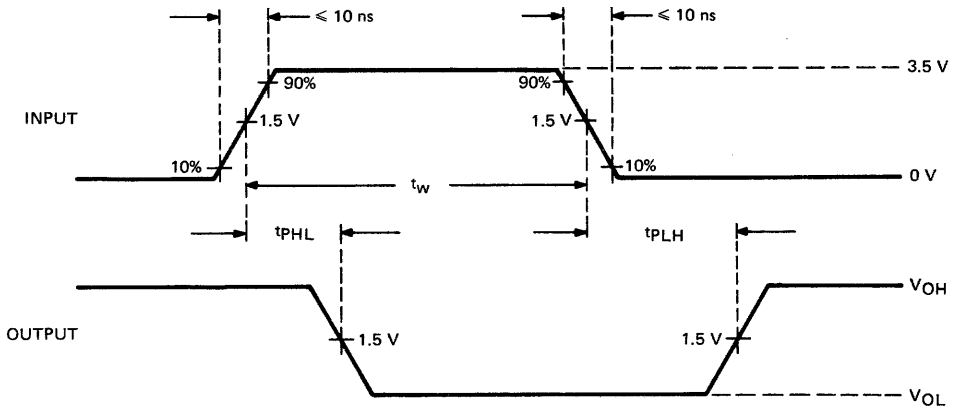
§Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 79–PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§

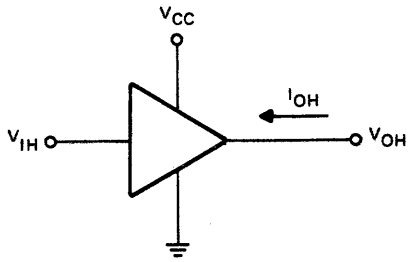


FIGURE 80–V_{IH}, I_{OH}

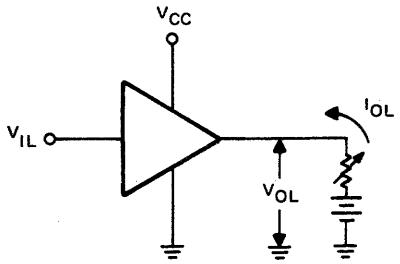


FIGURE 81–V_{IL}, V_{OL}

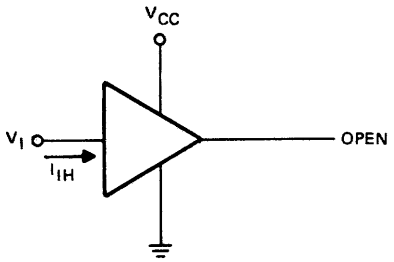


FIGURE 82–I_{IH}

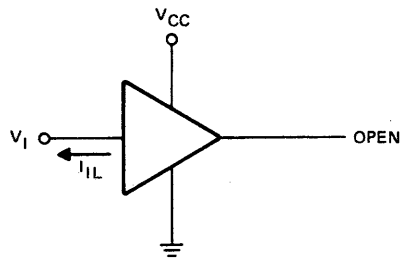
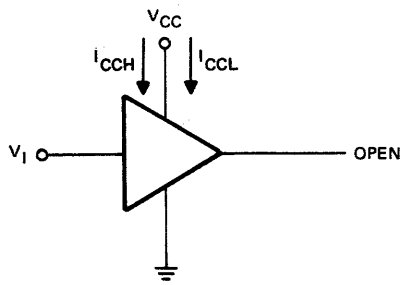


FIGURE 83–I_{IL}



All buffers/drivers are tested simultaneously.

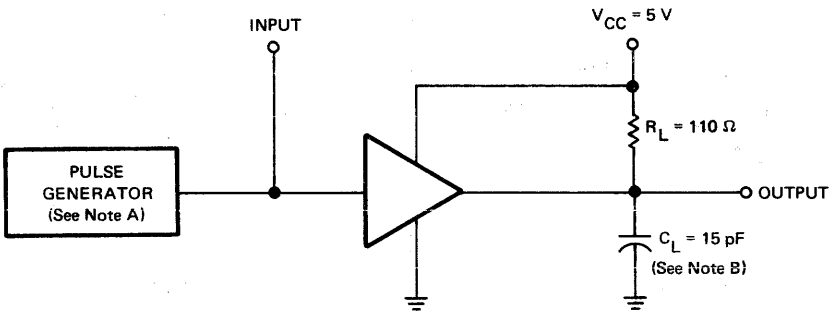
FIGURE 84–I_{CCH}, I_{CCL}

§Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

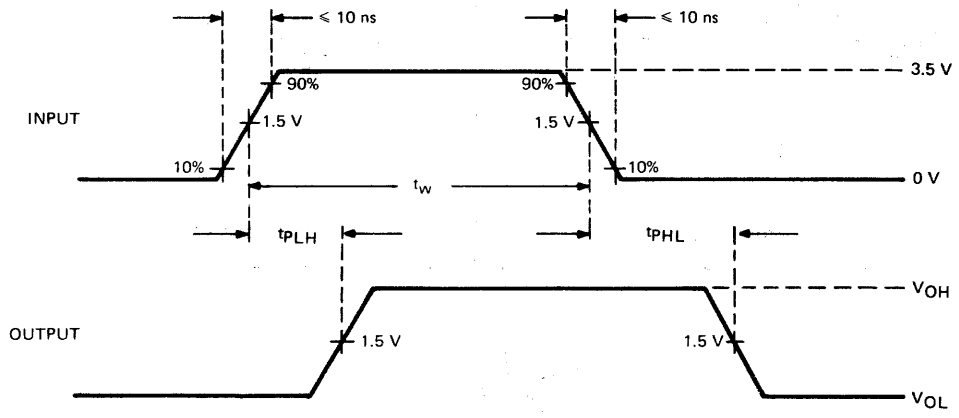
6

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



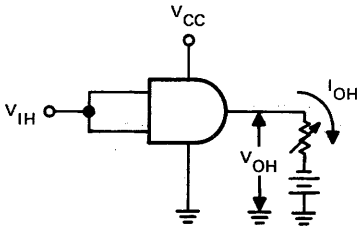
VOLTAGE WAVEFORMS

NOTES: A. The generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 85–PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶



Both inputs are tested simultaneously.

FIGURE 86–V_{IH}, V_{OH}

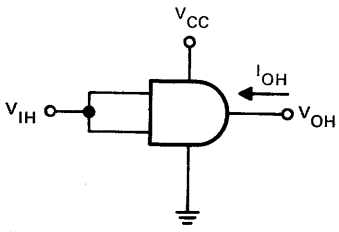
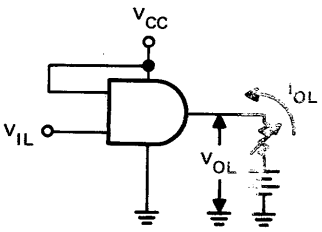
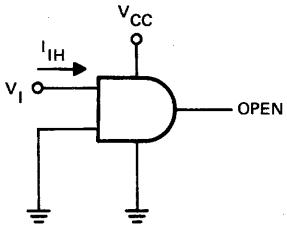


FIGURE 87–V_{IH}, I_{OH}



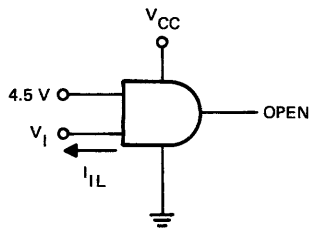
Each input is tested separately.

FIGURE 88–V_{IL}, V_{OL}



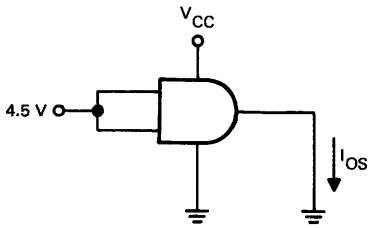
Each input is tested separately.

FIGURE 89–I_{IH}



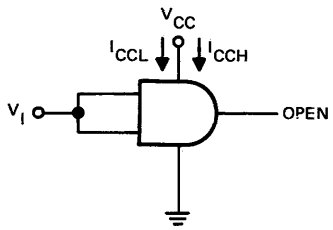
Each input is tested separately.

FIGURE 90–I_{IL}



Each gate is tested separately.

FIGURE 91–I_{OS}



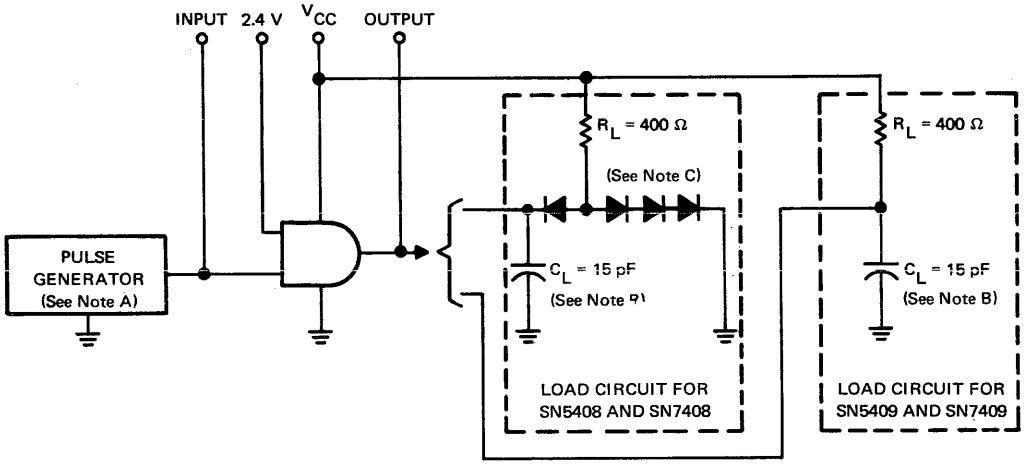
A. High-level and low-level conditions are tested.
B. All gates are tested simultaneously.

FIGURE 92–I_{CCH}, I_{CCL}

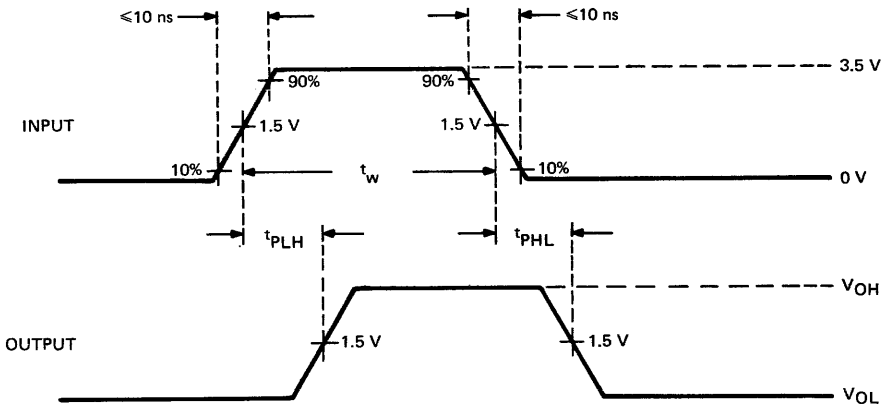
¶Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 93—PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§

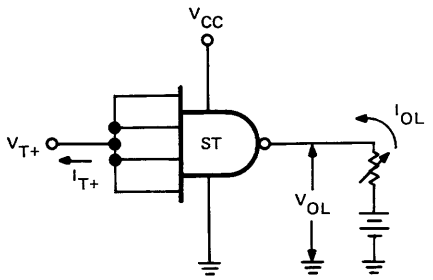


FIGURE 94–V_{T+}, I_{T+}, V_{OL}

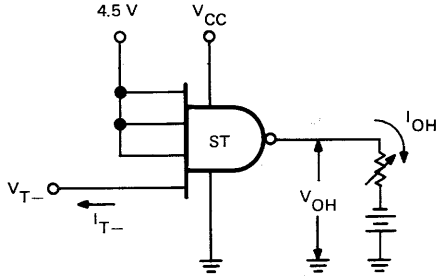
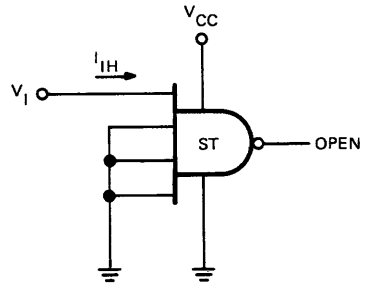
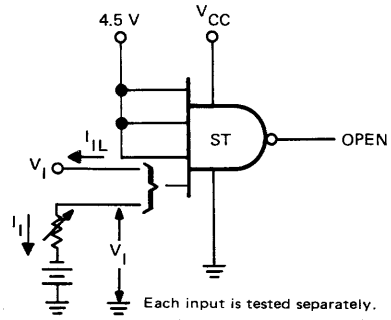


FIGURE 95–V_{T-}, I_{T-}, V_{OH}



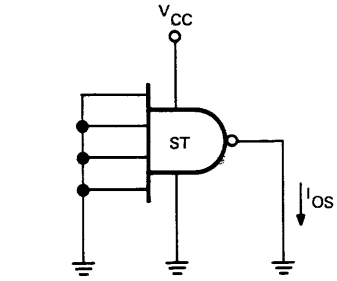
Each input is tested separately.

FIGURE 96–I_{IH}



Each input is tested separately.

FIGURE 97–V_I, I_{IL}



Each gate is tested separately.

FIGURE 98–I_{OS}

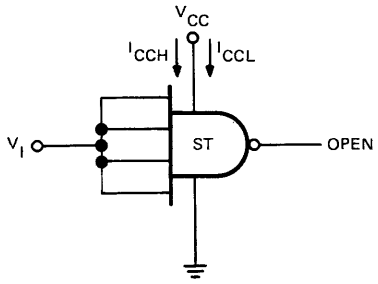


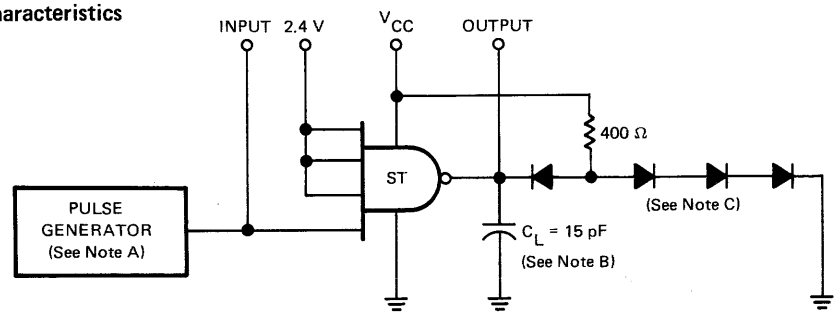
FIGURE 99–I_{CCH}, I_{CCL}

§Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

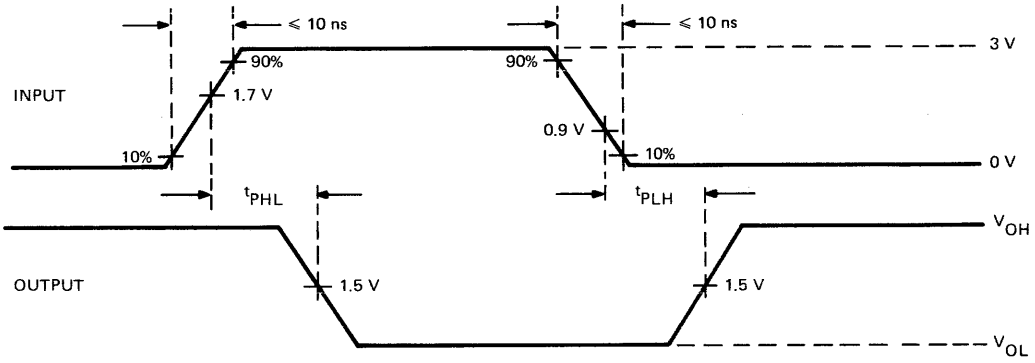
6

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



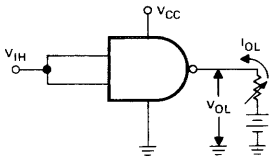
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 100–PROPAGATION DELAY TIMES

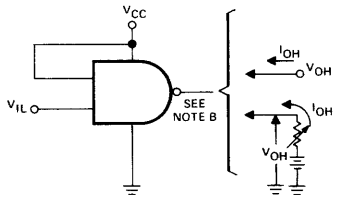
PARAMETER MEASUREMENT INFORMATION

d-c test circuits §



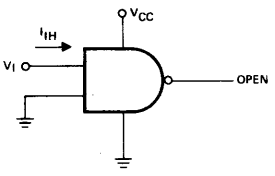
Both inputs are tested simultaneously.

FIGURE 101–V_{IH}, V_{OL}



A. Each input is tested separately.
B. I_{OH} is tested at V_{OH} = 12 V and V_{OH} is tested at I_{OH} = 1 mA.

FIGURE 102–V_{IL}, V_{OH}, I_{OH}



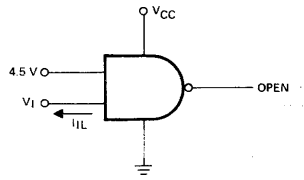
Each input is tested separately.

FIGURE 103–I_{IH}

§ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

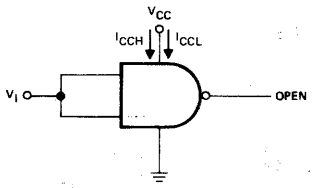
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



Each input is tested separately.

FIGURE 104–I_{IL}

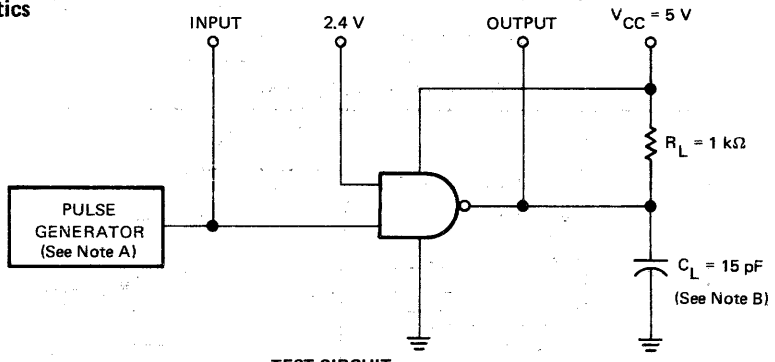


High-level and low-level output conditions are tested.

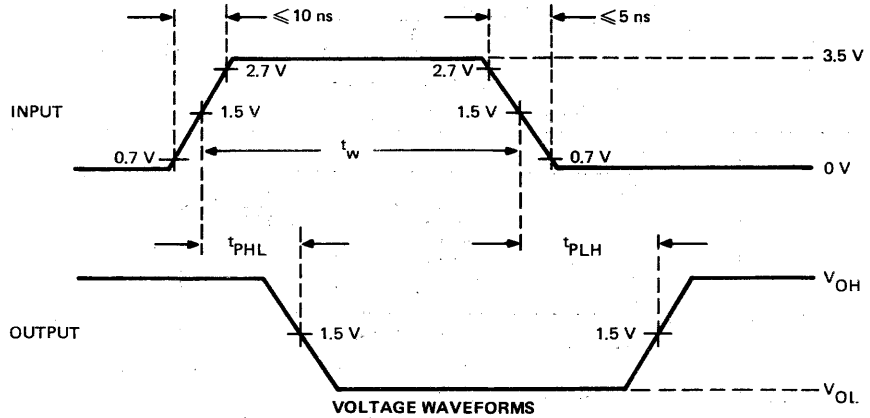
FIGURE 105–I_{CCH}, I_{CCL}

§Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

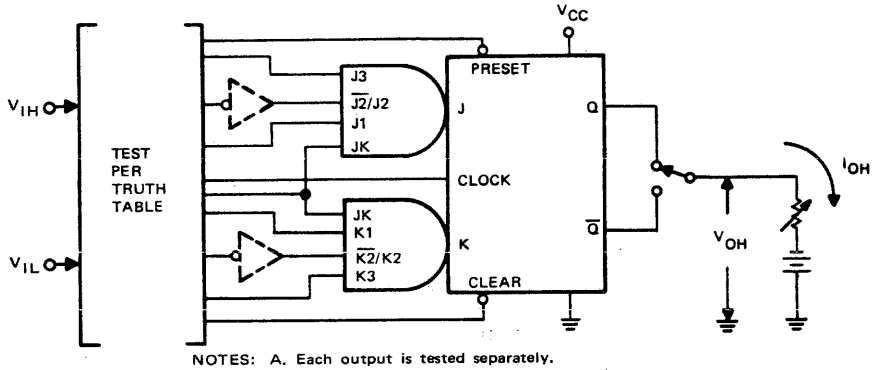
NOTES: A. The generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 106–PROPAGATION DELAY TIMES

6

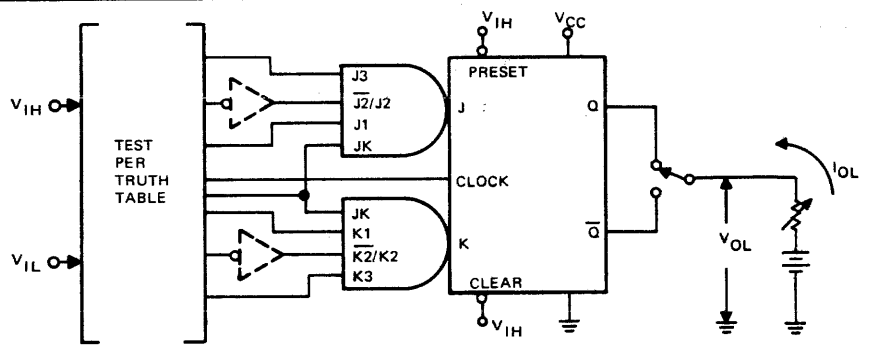
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



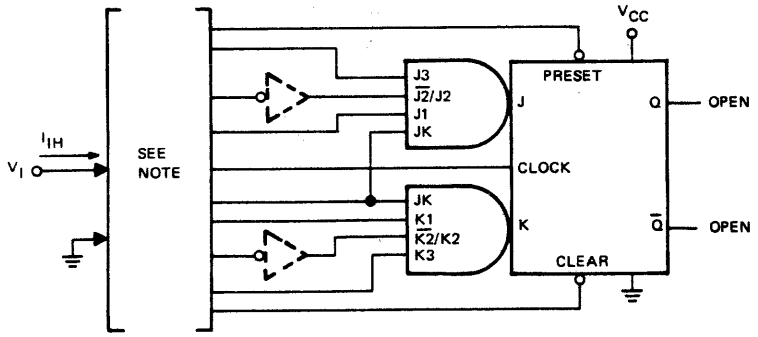
NOTES: A. Each output is tested separately.
B. V_{OH} is also tested using clear and preset inputs.

FIGURE 107 – V_{IH}, V_{IL}, V_{OH}



NOTE: Each output is tested separately.

FIGURE 108 – V_{IH}, V_{IL}, V_{OL}



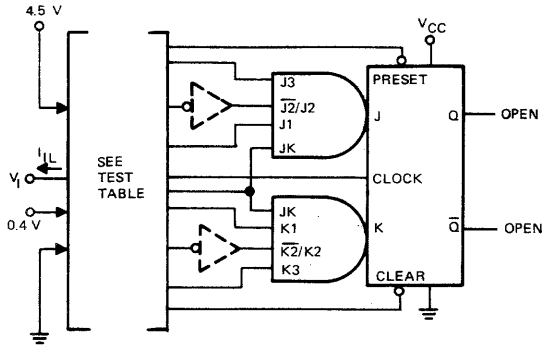
NOTE: V_I is applied and I_{IH} is measured separately for each input. All other inputs are grounded.

FIGURE 109 – I_{IH}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



NOTES: A. Each input is tested separately.
B. V_I is applied and I_{IL} is measured separately for each input.
C. All unspecified inputs are at 4.5 V.

TEST TABLE

APPLY V_I TEST I_{IL}	CONDITIONS ON OTHER INPUTS	
	APPLY 0.4 V	APPLY GND
CLOCK	NONE	NONE
PRESET	CLEAR	CLOCK
CLEAR	PRESET	CLOCK
J1	$\overline{J2}$ (OR 4.5 V TO J2)	CLOCK, CLEAR
$\overline{J2}$ (OR J2)	NONE	CLOCK, CLEAR
J3	$\overline{J2}$ (OR 4.5 V TO J2)	CLOCK, CLEAR
JK	$\overline{J2}$, $\overline{K2}$ (OR 4.5 V TO J2, K2)	CLOCK, CLEAR
JK	$\overline{J2}$, $\overline{K2}$ (OR 4.5 V TO J2, K2)	CLOCK, PRESET
K1	$\overline{K2}$ (OR 4.5 V TO K2)	CLOCK, PRESET
$\overline{K2}$ (OR K2)	NONE	CLOCK, PRESET
K3	$\overline{K2}$ (OR 4.5 V TO K2)	CLOCK, PRESET

6

FIGURE 110– I_{IL}

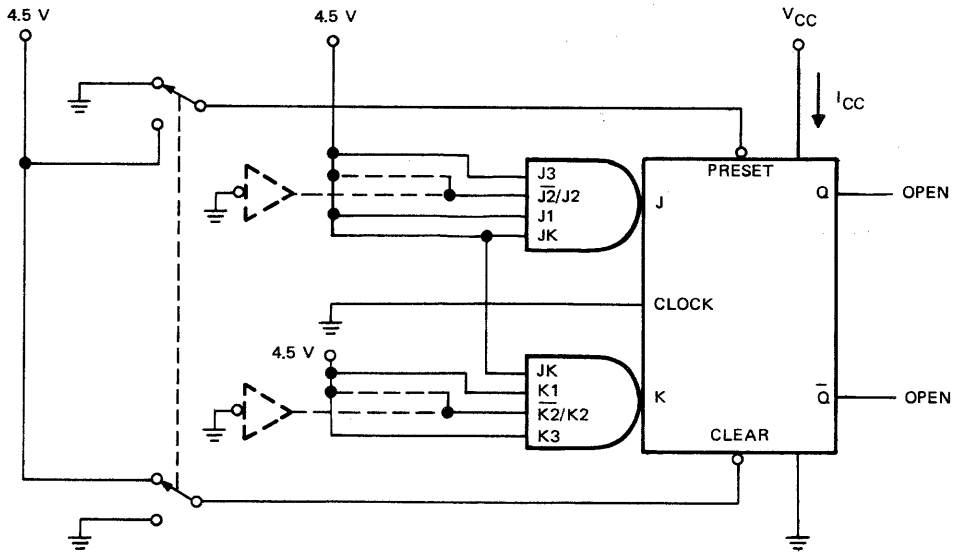
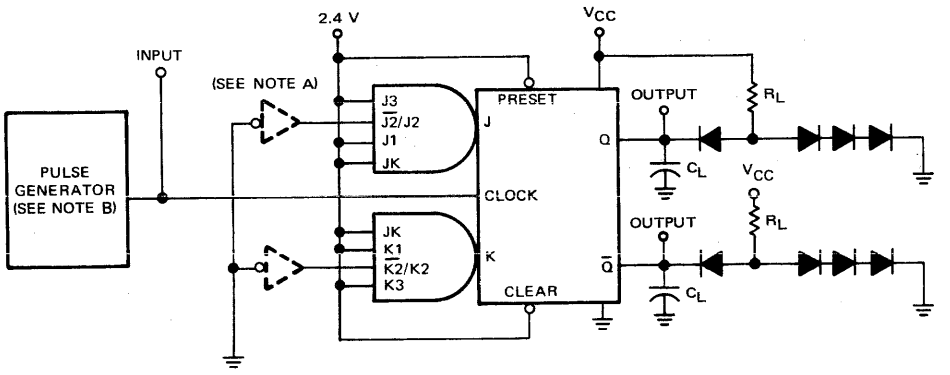


FIGURE 111– I_{CC}

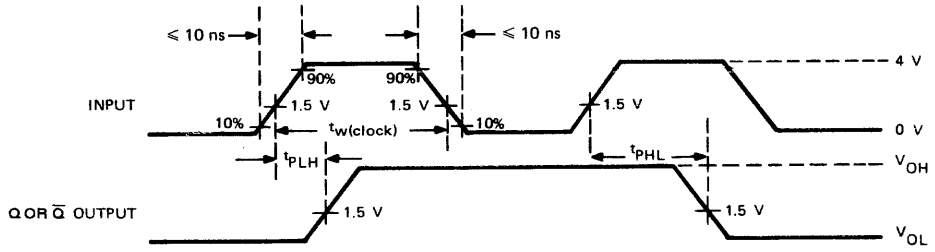
† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



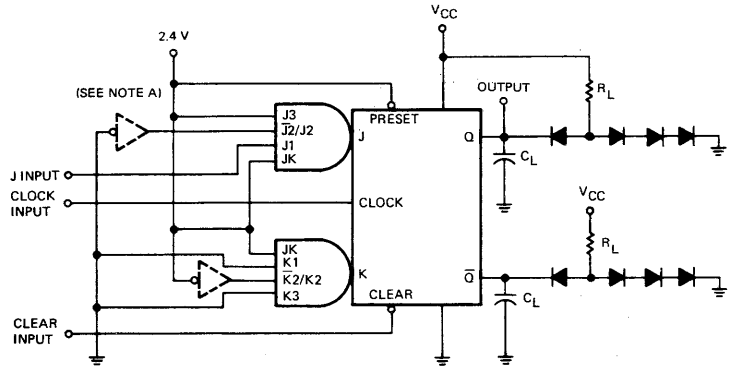
VOLTAGE WAVEFORMS

NOTES: A. Test circuit shown is for the SN54105/SN74105. When testing SN54104/SN74104, the J2 and K2 inputs are connected in parallel with the other J and K inputs.
B. The pulse generator has the following characteristics: $t_{w(clock)}$ = 250 ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N3064.

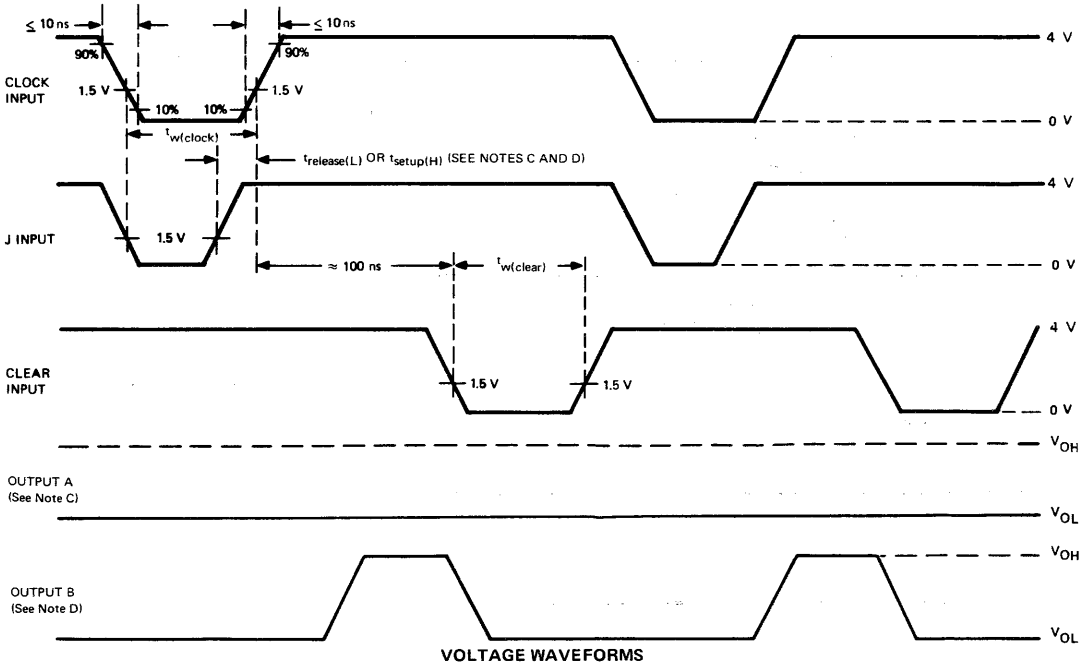
FIGURE 112– PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Test circuit shown is for the SN54105/SN74105. When testing SN54104/SN74104, the J2 input is connected in parallel with the other J inputs and K2 is grounded.

B. The input pulses have the following characteristics: PRR = 1 MHz, $t_{w(clock)}$ = 100 ns, and $t_{w(clear)}$ = 100 ns. For duration of the J-input pulse, see Notes C and D.

C. Output A is valid for: SN54104/SN74104, $t_{release(L)} \leqslant 10$ ns; SN54105/SN74105, $t_{release(L)} \leqslant 1$ ns.

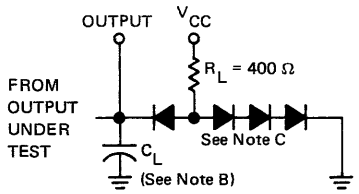
D. Output B is valid for: SN54104/SN74104, $t_{setup(H)} \geqslant 35$ ns; SN54105/SN74105, $t_{setup(H)} \geqslant 10$ ns.

E. C_L includes probe and jig capacitance.

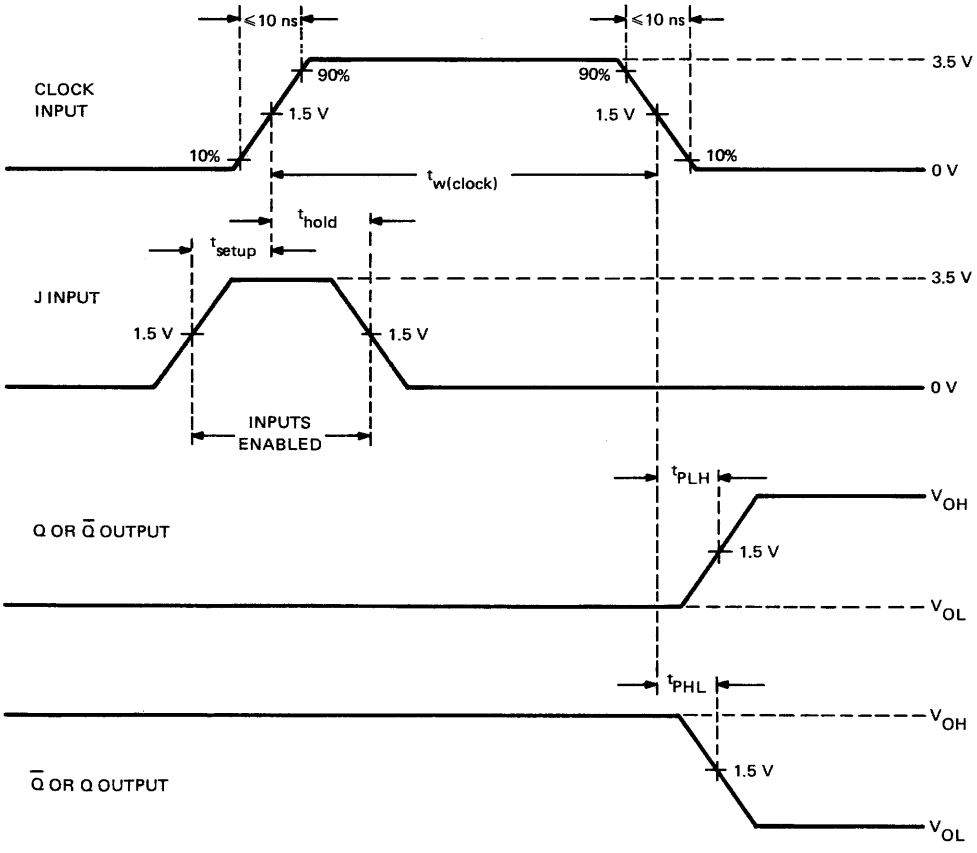
F. All diodes are 1N3064.

FIGURE 113 – INPUT SETUP/RELEASE TIMES

PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

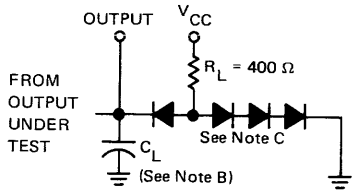


VOLTAGE WAVEFORMS

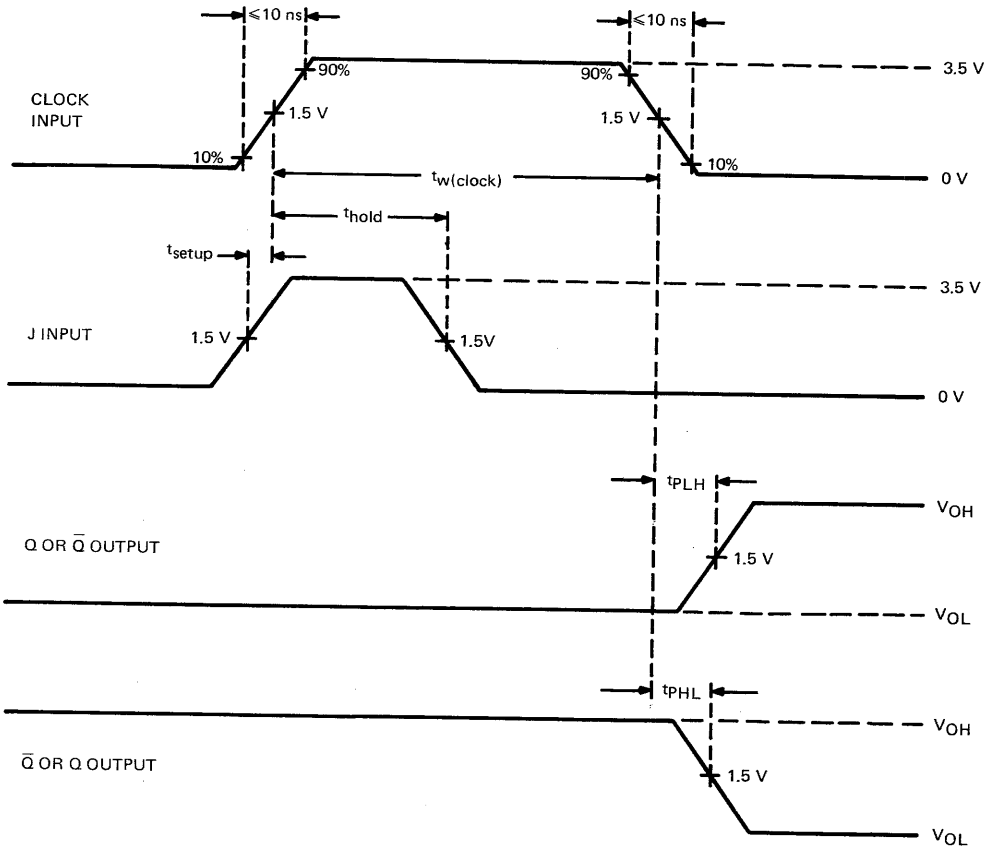
NOTES: A. Both input pulses are supplied by generators with the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$. Clock duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 114

PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST



VOLTAGE WAVEFORMS

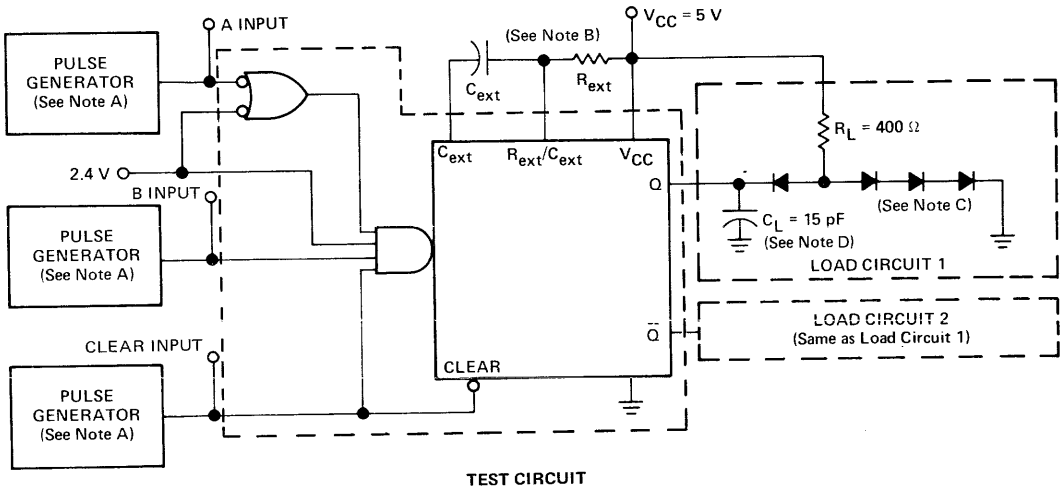
NOTES: A. Both input pulses are supplied by generators with the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$, clock duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 115

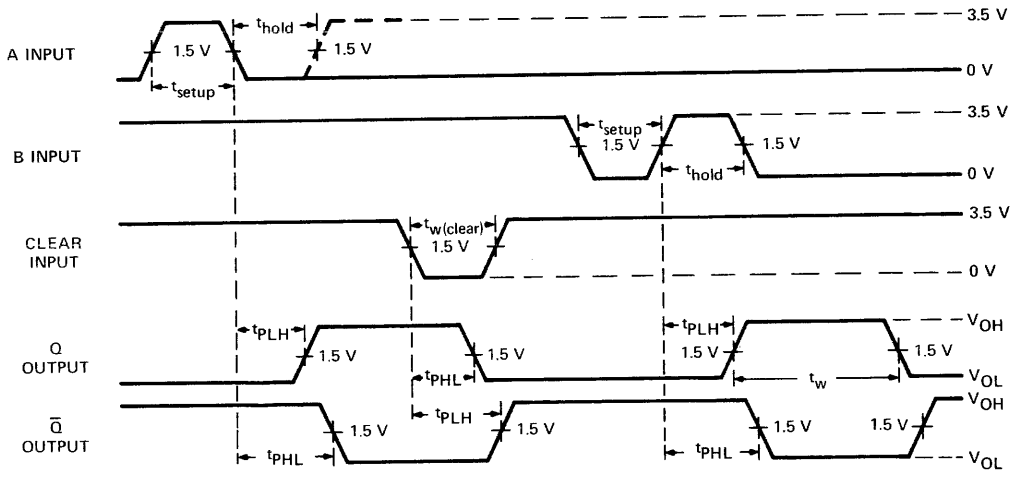
6

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



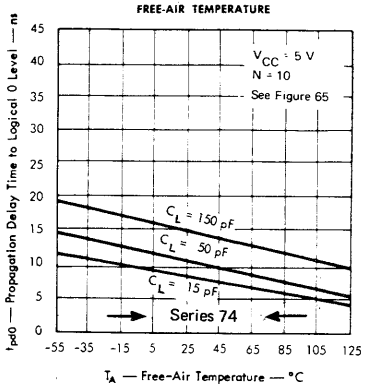
VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $t_r \leq 10$ ns (10% to 90% level), $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\ \Omega$.
B. See Test Conditions, switching characteristics table, page 3, for values of R_{ext} and C_{ext}.
C. All diodes are 1N3064.
D. C_L includes probe and jig capacitance.

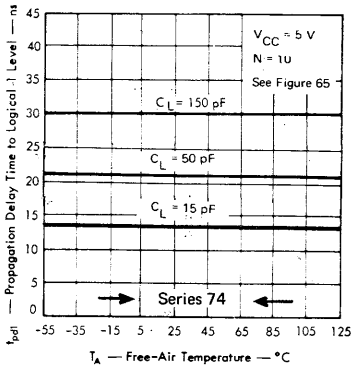
FIGURE 116–SWITCHING TIMES

TYPICAL CHARACTERISTICS §

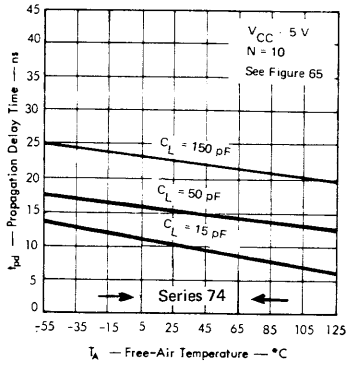
PROPAGATION DELAY TIME TO LOGICAL 0 LEVEL
vs
FREE-AIR TEMPERATURE



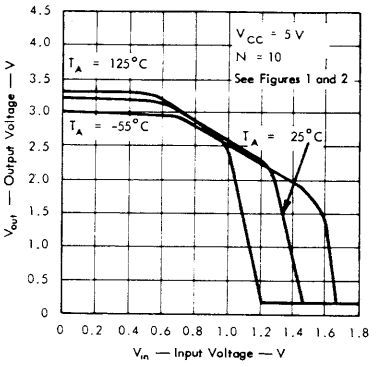
PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL
vs
FREE-AIR TEMPERATURE



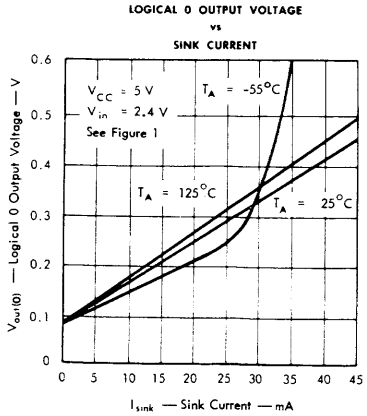
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE



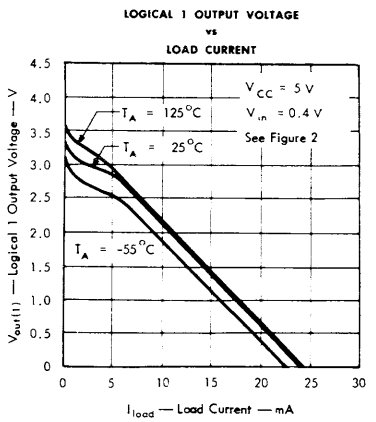
OUTPUT VOLTAGE
vs
INPUT VOLTAGE



LOGICAL 0 OUTPUT VOLTAGE
vs
SINK CURRENT



LOGICAL 1 OUTPUT VOLTAGE
vs
LOAD CURRENT

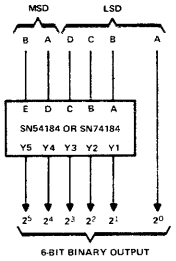


§ Unless otherwise noted, data as shown is applicable for: SN5400, SN5402, SN5404, SN5410, SN5420, SN5430, SN5450, SN5451, SN5453, SN5454, SN7400, SN7402, SN7404, SN7410, SN7420, SN7430, SN7450, SN7451, SN7453, SN7454.

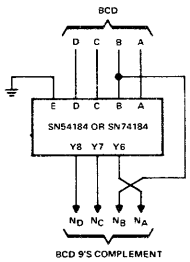
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SN54184 and SN74184 BCD-to-binary converters (continued)

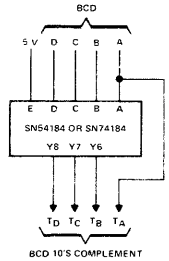
6-BIT CONVERTER



BCD 9'S COMPLEMENT CONVERTER



BCD 10'S COMPLEMENT CONVERTER



TRUTH TABLE
BCD-TO-BINARY CONVERTER

BCD WORDS	INPUTS (See Note A)						OUTPUTS (See Note B)				
	E	D	C	B	A	G	Y5	Y4	Y3	Y2	Y1
0-1	L	L	L	L	L	L	L	L	L	L	L
2-3	L	L	L	L	H	L	L	L	L	L	H
4-5	L	L	L	H	L	L	L	L	L	H	L
6-7	L	L	L	H	H	L	L	L	L	H	H
8-9	L	L	H	L	L	L	L	L	H	L	L
10-11	L	H	L	L	L	L	L	L	H	L	H
12-13	L	H	L	L	H	L	L	L	H	H	L
14-15	L	H	L	H	L	L	L	L	H	H	H
16-17	L	H	L	H	H	L	L	H	L	L	L
18-19	L	H	H	L	L	L	L	H	L	L	H
20-21	H	L	L	L	L	L	L	H	L	H	L
22-23	H	L	L	L	H	L	L	H	L	H	H
24-25	H	L	L	H	L	L	L	H	H	L	L
26-27	H	L	L	H	H	L	L	H	H	L	H
28-29	H	L	H	L	L	L	L	H	H	H	L
30-31	H	H	L	L	L	L	L	H	H	H	H
32-33	H	H	L	L	H	L	H	L	L	L	L
34-35	H	H	L	H	L	L	H	L	L	L	H
36-37	H	H	L	H	H	L	H	L	L	H	L
38-39	H	H	H	L	L	L	H	L	L	H	H
ANY	X	X	X	X	X	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

NOTES: A. Input conditions other than those shown produce highs at outputs Y1 through Y5.

B. Outputs Y6, Y7, and Y8 are not used for BCD-to-binary conversion.

In addition to BCD-to-binary conversion, the SN54184 and SN74184 are programmed to generate BCD 9's complement or BCD 10's complement. Again, in each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs Y6, Y7, and Y8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the truth table (above, right) when the devices are connected as shown above the truth table.

TRUTH TABLE
BCD 9'S OR BCD 10'S COMPLEMENT CONVERTER

BCD WORD	INPUTS (See Note C)						OUTPUTS (See Note D)		
	E†	D	C	B	A	G	Y8	Y7	Y6
0	L	L	L	L	L	L	H	L	H
1	L	L	L	L	H	L	H	L	L
2	L	L	L	H	L	L	L	H	H
3	L	L	L	H	H	L	L	H	L
4	L	L	H	L	L	L	L	H	H
5	L	L	H	L	H	L	L	H	L
6	L	L	H	H	L	L	L	L	H
7	L	L	H	H	H	L	L	L	L
8	L	H	L	L	L	L	L	L	H
9	L	H	L	L	H	L	L	L	L
0	H	L	L	L	L	L	L	L	L
1	H	L	L	L	H	L	H	L	L
2	H	L	L	H	L	L	H	L	L
3	H	L	L	H	H	L	L	H	H
4	H	L	H	L	L	L	L	H	H
5	H	L	H	L	H	L	L	H	L
6	H	L	H	H	L	L	L	H	L
7	H	L	H	H	H	L	L	L	H
8	H	H	L	L	L	L	L	L	H
9	H	H	L	L	H	L	L	L	L
ANY	X	X	X	X	X	H	H	H	H

H = high level, L = low level, X = irrelevant

NOTES: C. Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.

D. Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

†When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

9

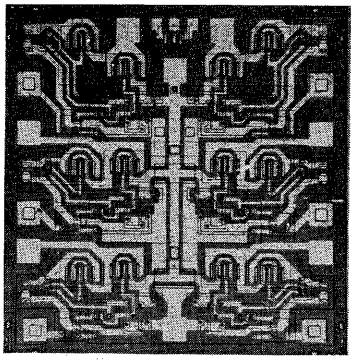
Series 54H/74H Circuits

SERIES 54H, 74H
HIGH-SPEED TRANSISTOR-TRANSISTOR LOGIC

FOR GENERAL-PURPOSE DIGITAL SYSTEM APPLICATIONS

description

TYPICAL HEX INVERTER CIRCUIT BAR



Series 54H and 74H TTL integrated circuits are designed to be used in systems where very-high-speed saturated logic and high d-c noise margins are required. Definitive specifications are provided for operating characteristics over the full military temperature range (−55°C to 125°C) and the industrial temperature range (0°C to 70°C). This logic series includes the gates and flip-flop elements needed to perform all functions within general-purpose digital systems.

Series 54H and 74H are completely compatible with Series 54 and 74 TTL logic families and circuits are designed to operate at the same supply voltages, logic levels, and high d-c noise margins which are characteristic of Series 54/74 TTL circuits. Series 54H/74H circuits feature a darlington-connected, double-ended, high-speed output for improved switching speeds. Typical flip-flop clock frequencies are 30 and 50 megahertz.

Since the Series 54H/74H circuits are compatible with other products in the TTL family, these higher-speed devices may be selectively used in system locations requiring minimal propagation delay times. In other locations where speed is not critical, Series 54/74 circuits may be used, thus minimizing total system power dissipation.

7

Further flexibility is provided by the addition of noninverting AND and AND-OR functions to the Series 54H/74H line. This eliminates, in so far as possible, the need for extra packages and resultant wiring to perform mere signal-inverting functions. In addition to improving speed, the low impedance of the double-ended output rejects capacitively coupled a-c pulses, ensures waveshape integrity, and provides the necessary additional drive capability.

features

LOW SYSTEM COST

- **multifunction gates and dual flip-flops offer low cost per function**
- **special circuit types (AND and AND-OR functions) reduce system package count**

OPTIMUM CIRCUIT PERFORMANCE

- **high speed — typical gate propagation delay times: 6 ns at C_L = 25 pF**
- **high d-c noise margin — typically one volt**
- **low output impedance provides low a-c noise susceptibility**
- **waveform integrity over full range of loading and temperature conditions**
- **power dissipation — typically 23 mW per NAND gate at 50% duty cycle**
- **fan-out — 10 Series 54H/74H or 54S/74S loads or 12 Series 54/74 loads**
- **compatible with standard Series 54/74 logic circuits**
- **all inputs are diode clamped to minimize transmission-line effects**
- **entirely compatible with Schottky TTL Series 54S/74S.**

SERIES 54H, 74H
HIGH-SPEED TRANSISTOR-TRANSISTOR LOGIC

SERIES 54H/74H
FEATURING 6 ns SPEED AND 22 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
NAND/NOR GATES						
Quadruple 2-Input Positive NAND Gates	SN54H00	SN74H00	J	N	W	7-5
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN54H01	SN74H01	J	N	W	7-6
Hex Inverters	SN54H04	SN74H04	J	N	W	7-9
Hex Inverters (with Open-Collector Output)	SN54H05	SN74H05	J	N	W	7-10
Triple 3-Input Positive NAND Gates	SN54H10	SN74H10	J	N	W	7-11
Triple 3-Input Positive AND Gates	SN54H11	SN74H11	J	N	W	7-12
Dual 4-Input Positive NAND Gates	SN54H20	SN74H20	J	N	W	7-13
Dual 4-Input Positive AND Gates	SN54H21	SN74H21	J	N	W	7-14
Dual 4-Input Positive NAND Gates (with Open-Collector Output)	SN54H22	SN74H22	J	N	W	7-15
8-Input Positive NAND Gates	SN54H30	SN74H30	J	N	W	7-16
Dual 4-Input Positive NAND Buffers	SN54H40	SN74H40	J	N	W	7-17
AND-OR/AND-OR-INVERT GATES						
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN54H50	SN74H50	J	N	W	7-18
Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN54H51	SN74H51	J	N	W	7-18
Expandable 2-2-2-3-Input AND-OR Gates	SN54H52	SN74H52	J	N	W	7-20
Expandable 2-2-2-3-Input AND-OR-INVERT Gates	SN54H53	SN74H53	J	N	W	7-22
4-Wide 2-Input AND-OR-INVERT Gates	SN54H54	SN74H54	J	N	W	7-22
Expandable 2-Wide 4-Input AND-OR-INVERT Gates	SN54H55	SN74H55	J	N	W	7-24
EXPANDERS						
Dual 4-Input Expander	SN54H60		J	N	W	7-26
Dual 4-Input Expander		SN74H60	J	N	W	7-27
Triple 3-Input Expanders	SN54H61	SN74H61	J	N	W	7-28
3-2-2-3-Input AND-OR Expander	SN54H62		J	N	W	7-29
3-2-2-3-Input Expander		SN74H62	J	N	W	7-30

7

SEE PAGES 9-1, 9-2, AND 9-3 FOR LISTING OF TTL MSI CIRCUITS

*For outline drawings of all packages, see Section 1.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES 54H/74H
FEATURING 6 ns SPEED AND 22 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
FLIP-FLOPS						
J-K Master-Slave Flip-Flops (AND-OR Inputs)	SN54H71	SN74H71	J	N	W	7-31
J-K Master-Slave Flip-Flops (AND Inputs)	SN54H72	SN74H72	J	N	W	7-34
Dual J-K Master-Slave Flip-Flops	SN54H73	SN74H73	J	N	W	7-37
Dual D-Type Edge-Triggered Flip-Flops	SN54H74	SN74H74	J	N	W	7-40
Dual J-K Master-Slave Flip-Flops with Preset and Clear	SN54H76	SN74H76	J	N	W	7-44
Dual J-K Master-Slave Flip-Flops (Common Clock)	SN54H78	SN74H78	J	N	W	7-47
J-K Negative Edge-Triggered Flip-Flops with AND-OR Inputs (50 MHz)	SN54H101	SN74H101	J	N	W	7-50
J-K Negative Edge-Triggered Flip-Flops with AND Inputs (50 MHz)	SN54H102	SN74H102	J	N	W	7-53
Dual J-K Negative Edge-Triggered Flip-Flops (50 MHz)	SN54H103	SN74H103	J	N	W	7-56
Dual J-K Negative Edge-Triggered Flip-Flops (50 MHz) with Preset and Clear	SN54H106	SN74H106	J	N	W	7-59
Dual J-K Negative Edge-Triggered Flip-Flops (50 MHz) (Common Clock)	SN54H108	SN74H108	J	N	W	7-62

7

SEE PAGES 9-1, 9-2, AND 9-3 FOR LISTING OF TTL MSI CIRCUITS

*For outline drawings of all packages, see Section 1.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage, V_{in} (See Notes 1 and 2)	5.5 V
Operating Free-Air Temperature Range: Series 54H	−55°C to 125°C
Series 74H	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

logic definition

Series 54H and 74H logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

HIGH VOLTAGE = LOGICAL 1

LOW VOLTAGE = LOGICAL 0

unused inputs of NAND/AND gates

For optimum switching times and minimum noise susceptibility unused inputs should be maintained at a positive voltage greater than 2.4 V but not exceed the absolute maximum rating of 5.5 V. This eliminates the distributed capacitance associated with the floating input-transistor emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferrably, this voltage should be between 2.4 V and 3.5 V.
b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each input presents a full load in the logical 1 state to the driving output.
c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor.

7

input-current requirements

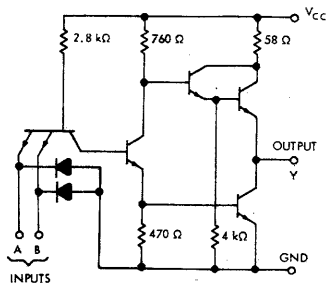
Input-current requirements reflect worst-case V_{CC} and temperature conditions. Each input, of the multiple-emitter input transistors which has a 2.8-kΩ base resistor, requires no more than a 2-mA flow out of the input at a logical 0 voltage level; therefore, one load (N = 1) is −2 mA maximum. Each input requires current into the output at a logical 1 voltage level. This current is 50 μA maximum for each emitter of input transistors with the 2.8-kΩ base resistor. Currents into the input terminals are specified as positive values.

fan-out capability

Fan-out (N) reflects the ability of an output to sink current from a number of Series 54H or 74H loads at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each standard output is capable of sinking current or supplying current to 10 Series 54H or 74H loads (N = 10) or 12 Series 54 or 74 loads. Load currents (out of the output termina!) are specified as negative values.

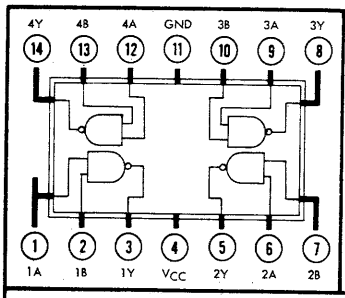
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

schematic (each gate)

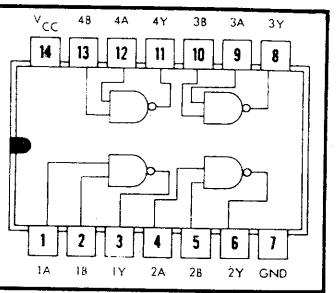


NOTE: Component values shown are nominal

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H00 Circuits	4.5	5	5.5	V
SN74H00 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H00 Circuits	−55	25	125	°C
SN74H00 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

7

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	5	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		26	40	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		10	16.8	mA

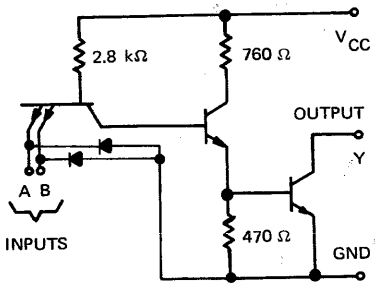
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.2	10	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		5.9	10	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

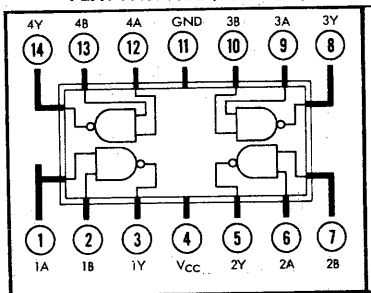
CIRCUIT TYPES SN54H01, SN74H01
QUADRUPLE 2-INPUT POSITIVE NAND GATES
(WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)

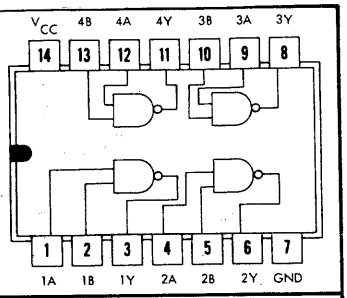


NOTE: Component values shown are nominal.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H01 Circuits	4.5	5	5.5	V
SN74H01 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Each Output, N (and see pages 3-7 and 3-8)			10	
Operating Free-Air Temperature Range: SN54H01 Circuits	−55	25	125	°C
SN74H01 Circuits	0	25	70	°C

electrical characteristics (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7				0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		26	40	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		6.8	10	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		7.5	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		10	15	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-AND function and simultaneously, will drive from one to nine 54H or 74H loads. When no other open-collector gates are paralleled, this gate may be used to drive ten 54H or 74H loads. For any of these conditions an appropriate load-resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to loads) and I_{off} current (through paralleled outputs) will be available during a logical 1 level at the output. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the loads will not cause the output voltage to rise above the logical 0 level even if one of the paralleled outputs is sinking all the current.

In both conditions (logical 0 and logical 1) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where: V_{RL} is voltage drop in volts, and I_{RL} is the current in amperes.

logical 1 (off level) circuit calculations (see figure A)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the $V_{out(1)}$ level required at the load:

$$V_{RL} = V_{CC} - V_{out(1)\ required}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents ($I_{in(1)}$) and off-level reverse currents ($I_{out(1)}$) through each of the wire-AND connected outputs:

$$I_{RL} = \eta \cdot I_{out(1)} + N \cdot I_{in(1)} \text{ to loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{out(1)\ required}}{\eta \cdot I_{out(1)} + N \cdot I_{in(1)}}$$

where: η = number of gates wire-AND connected, and N = number of 54H/74H loads

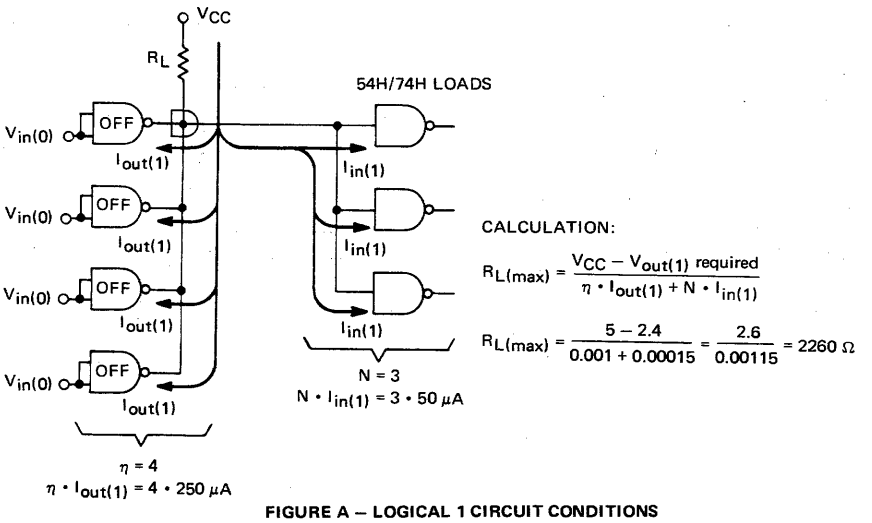


FIGURE A – LOGICAL 1 CIRCUIT CONDITIONS

7

SERIES 54H, 74H
OPEN-COLLECTOR-OUTPUT APPLICATION DATA

APPLICATION DATA

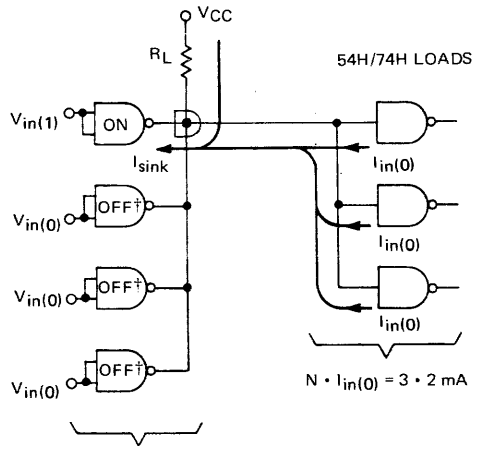
logical 0 (on level) circuit calculations (see figure B)

The current through the resistor must be limited to the maximum sink-current capability of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during logical 0 periods, the current must be limited to 20 mA, the maximum current which will ensure a logical 0 maximum of 0.4 volts.

Also, fan-out must be considered. Part of the 20 mA will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(min)} = \frac{V_{CC} - V_{out(0)}\ \text{required}}{I_{sink}\ \text{capability} - I_{sink}\ \text{from loads}}$$



CALCULATION:

$$R_{L(min)} = \frac{V_{CC} - V_{out(0)}\ \text{required}}{I_{sink}\ \text{capability} - I_{sink}\ \text{from TTL loads}}$$

$$R_{L(min)} = \frac{5 - 0.4}{0.02 - 0.006} = \frac{4.6}{0.014} = 323\ \Omega$$

†Current into OFF outputs is negligible at logical 0.

FIGURE B – LOGICAL 0 CIRCUIT CONDITIONS

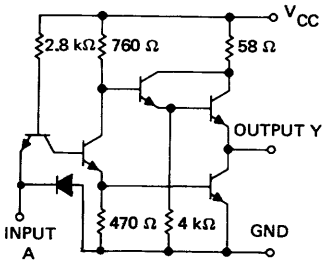
Table I provides minimum and maximum resistor values, calculated from equations shown above,for driving one to ten 54H/74H loads and wire-AND connecting two to seven parallel output. Each value shown for one wire-AND output is determined by the fan-out plus the cutoff current of a single output transistor. Extension beyond seven wire-AND connections is permitted with fan-outs of seven or less if a valid minimum and maximum R_L is possible. Fastest rise times are obtained when $R_{L(min)}$ is used. When fanning-out to ten 54H/74H loads, the calculation for the minimum value of R_L indicates that and infinite resistance should be used ($V_{R_L} \div 0 = \infty$); however, the use of a 3466 Ω resistor in this case will satisfy the logical 1 condition and limit the logical 0 voltage level to less than 0.42 V.

FAN-OUT TO 54H/74H LOADS	WIRE-AND OUTPUTS							
	1	2	3	4	5	6	7	1 to 7
1	8666	4727	3250	2476	2000	1677	1444	255
2	7428	4333	3058	2363	1925	1625	1405	288
3	6500	4000	2888	2260	1857	1575	1368	323
4	5777	3714	2736	2166	1793	1529	1333	384
5	5200	3466	2600	2080	1733	1485	1300	460
6	4727	3250	2476	2000	1677	1444	1268	578
7	4333	3058	2363	1925	1625	1405	1238	767
8	4000	2888	2260	1857	1575	1368	1209	1150
9	3714	2736	X	X	X	X	X	2300
10	3466	X	X	X	X	X	X	3466‡
	MAXIMUM							MIN
	LOAD RESISTOR VALUE IN OHMS							

TABLE I – LOAD RESISTOR VALUES

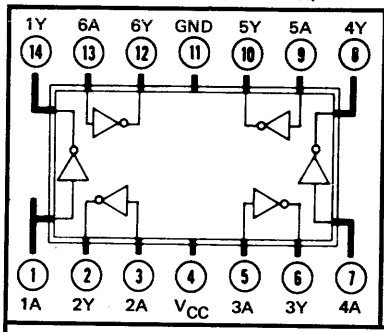
X – Not recommended or not possible.
‡ – The theoretical value is ∞. See explanation in text.
All values shown in the table are based on:
Logical 1 conditions: V_{CC} = 5 V, $V_{out(1)}$ required = 2.4 V
Logical 0 conditions: V_{CC} = 5 V, $V_{out(0)}$ required = 0.4 V

schematic (each inverter)

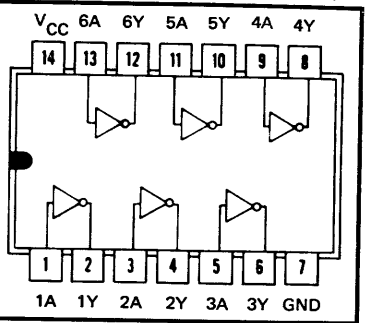


Component values shown are normal

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H04 Circuits	4.5	5	5.5	V
SN74H04 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H04 Circuits	−55	25	125	°C
SN74H04 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	8		2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 level at output	9				0.8	V
$V_{out(1)}$	Logical 1 output voltage	9	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	8	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current	11	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current	11	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	12	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	13	V_{CC} = MAX, V_{in} = 4.5 V		40	58	mA
$I_{CC(1)}$	Logical 1 level supply current	13	V_{CC} = MAX, V_{in} = 0		16	26	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.5	10	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		6	10	ns

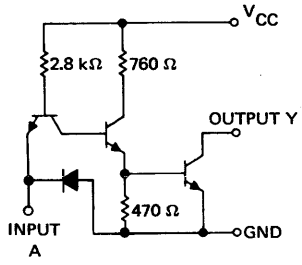
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

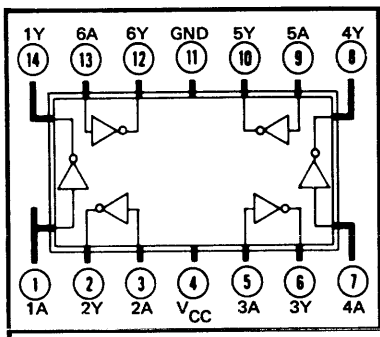
CIRCUIT TYPES SN54H05, SN74H05
HEX INVERTERS (WITH OPEN-COLLECTOR OUTPUT)

schematic (each inverter)

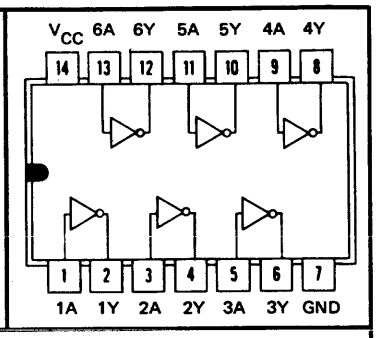


Component values shown are normal

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H05 Circuits	4.5	5	5.5	V
SN74H05 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N (and see pages 3-7 and 3-8)			10	
Operating Free-Air Temperature Range, T_A: SN54H05 Circuits	−55	25	125	°C
SN74H05 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 (on) level at output	8		2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 (off) level at output	10				0.8	V
$I_{out(1)}$	Output reverse current	10	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	8	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current	11	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current	11	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	13	V_{CC} = MAX, V_{in} = 4.5 V		40	58	mA
$I_{CC(1)}$	Logical 1 level supply current	13	V_{CC} = MAX, V_{in} = 0		16	26	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

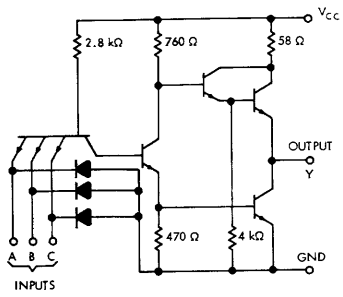
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		7.5	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		10	15	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

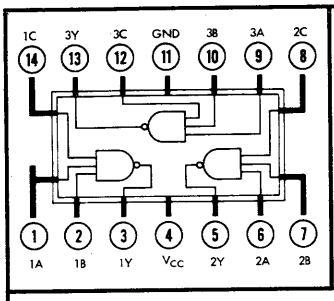
CIRCUIT TYPES SN54H10, SN74H10
TRIPLE 3-INPUT POSITIVE NAND GATES

schematic (each gate)

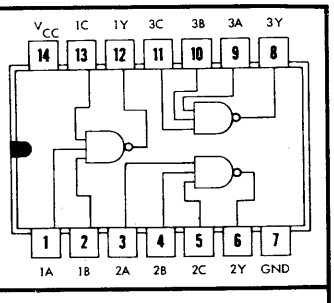


NOTE: Component values shown are nominal

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABC}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H10 Circuits	4.5	5	5.5	V
SN74H10 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H10 Circuits	−55	25	125	°C
SN74H10 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

7

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	5	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		19.5	30	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		7.5	12.6	mA

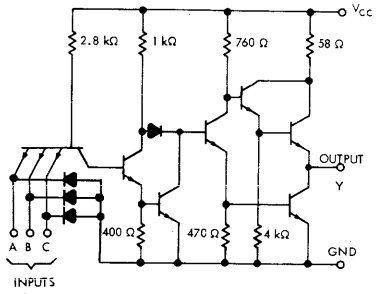
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.3	10	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		5.9	10	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

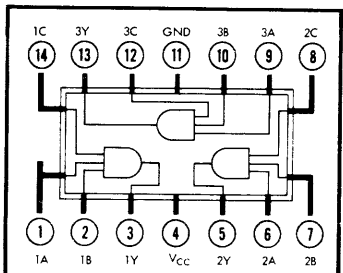
CIRCUIT TYPES SN54H11, SN74H11
TRIPLE 3-INPUT POSITIVE AND GATES

schematic (each gate)

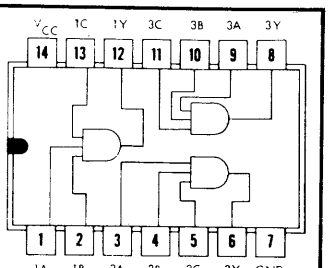


NOTE: Component values shown are nominal

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = ABC$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H11 Circuits	4.5	5	5.5	V
SN74H11 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H11 Circuits	−55	25	125	°C
SN74H11 Circuits	0	25	70	°C

7

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	14		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 0 level at output	15				0.8	V
$V_{out(1)}$	Logical 1 output voltage	14	V_{CC} = MIN, $V_{in(1)}$ = 2 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	15	V_{CC} = MIN, $V_{in(0)}$ = 0.8 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	16	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	17	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	18	V_{CC} = MAX, V_{in} = 4.5 V	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	19	V_{CC} = MAX, V_{in} = 0		30	48	mA
$I_{CC(1)}$	Logical 1 level supply current	19	V_{CC} = MAX, V_{in} = 4.5 V		18	30	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

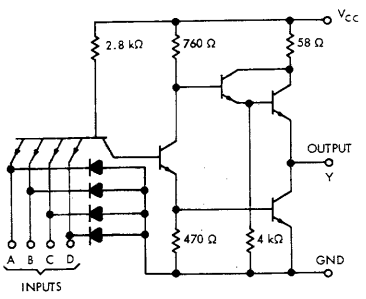
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		8.8	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		7.6	12	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

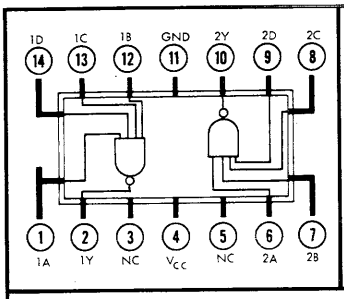
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

schematic (each gate)

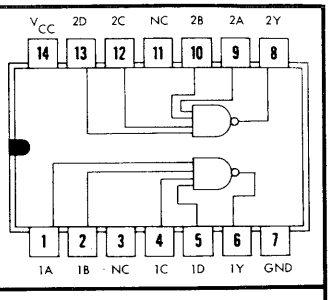


NOTES: 1. Component values shown are nominal
2. NC — No internal connection

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCD}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H20 Circuits	4.5	5	5.5	V
SN74H20 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H20 Circuits	−55	25	125	°C
SN74H20 Circuits	0	25	70	°C

7

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 output voltage	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	5	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		13	20	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		5	8.4	mA

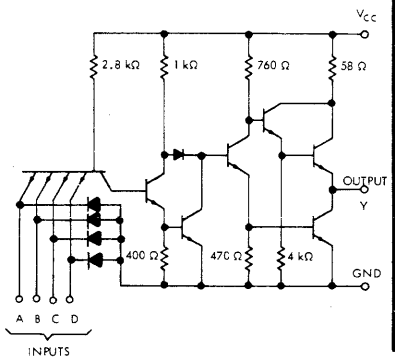
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		7	10	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		6	10	ns

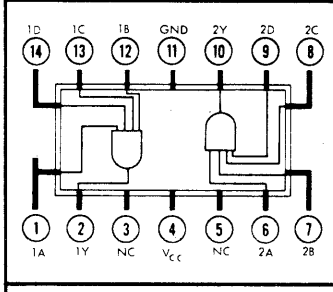
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

CIRCUIT TYPES SN54H21, SN74H21
DUAL 4-INPUT POSITIVE AND GATES

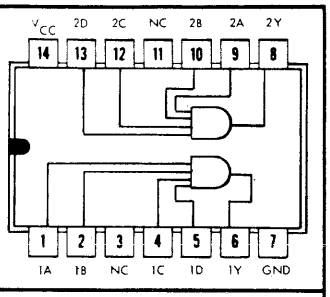
schematic (each gate)



W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = ABCD

NOTES: 1. Component values shown are nominal
2. NC — No internal connection

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H21 Circuits	4.5	5	5.5	V
SN74H21 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H21 Circuits	−55	25	125	°C
SN74H21 Circuits	0	25	70	°C

7

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	14		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 0 level at output	15				0.8	V
$V_{out(1)}$	Logical 1 output voltage	14	V_{CC} = MIN, $V_{in(1)}$ = 2 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	15	V_{CC} = MIN, $V_{in(0)}$ = 0.8 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	16	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	17	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	18	V_{CC} = MAX, V_{in} = 4.5 V	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	19	V_{CC} = MAX, V_{in} = 0		20	32	mA
$I_{CC(1)}$	Logical 1 level supply current	19	V_{CC} = MAX, V_{in} = 4.5 V		12	20	mA

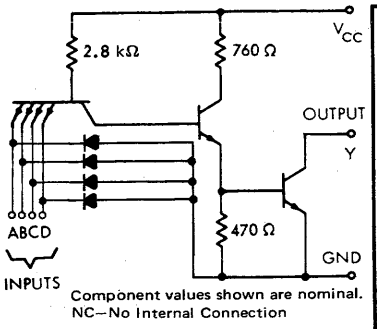
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		8.8	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		7.6	12	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

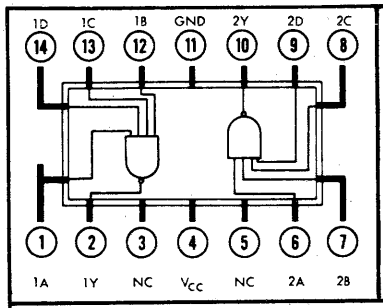
CIRCUIT TYPES SN54H22, SN74H22
DUAL 4-INPUT POSITIVE NAND GATES (WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)

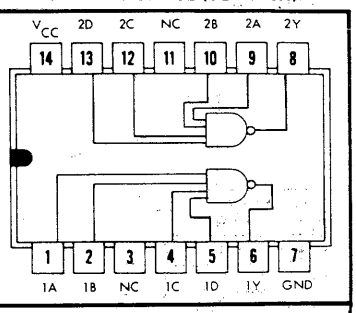


Component values shown are nominal.
NC—No Internal Connection

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCD}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H22 Circuits	4.5	5	5.5	V
SN74H22 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Each Output, N (and see pages 3-7 and 3-8)			10	
Operating Free-Air Temperature Range: SN54H22 Circuits	−55	25	125	°C
SN74H22 Circuits	0	25	70	°C

electrical characteristics (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on) level at output	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off) level at output	7				0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		13	20	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		3.4	5	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

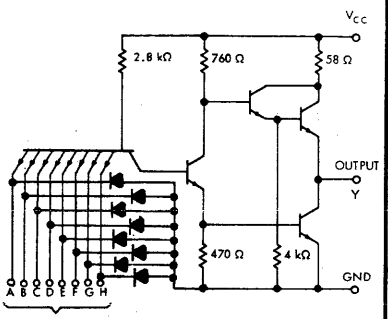
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		7.5	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		10	15	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

For Applications Data, see pages 3-7 and 3-8.

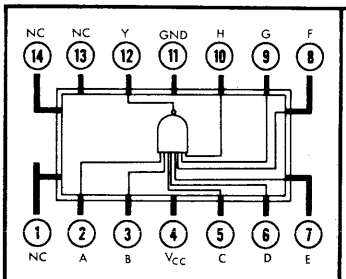
CIRCUIT TYPES SN54H30, SN74H30
8-INPUT POSITIVE NAND GATES

schematic

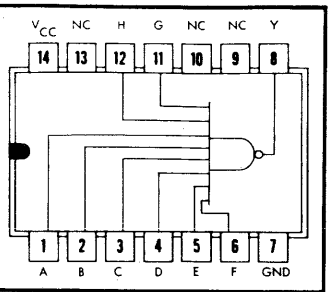


NOTES: 1. Component values shown are nominal
2. NC — No internal connection

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCDEFGH}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H30 Circuits	4.5	5	5.5	V
SN74H30 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H30 Circuits	−55	25	125	°C
SN74H30 Circuits	0	25	70	°C

7

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	5	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		6.5	10	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		2.5	4.2	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

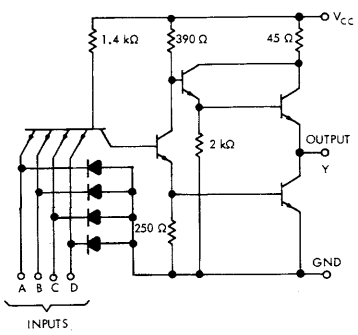
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		8.9	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		6.8	10	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Duration of short-circuit test should not exceed 1 second.

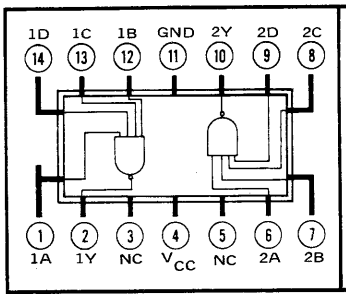
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

schematic (each gate)

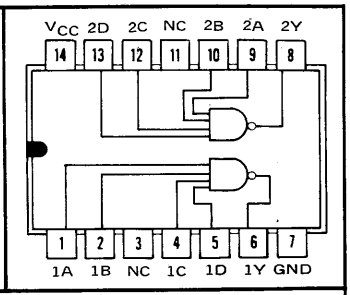


NOTES: 1. Component values shown are nominal
2. NC — No internal connection

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCD}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H40 Circuits	4.5	5	5.5	V
SN74H40 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			30	
Operating Free-Air Temperature Range, T_A: SN54H40 Circuits	−55	25	125	°C
SN74H40 Circuits	0	25	70	°C

7

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −1.5 mA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 60 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−4	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	5	V_{CC} = MAX	−40		−125	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		25	40	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		10.4	16	mA

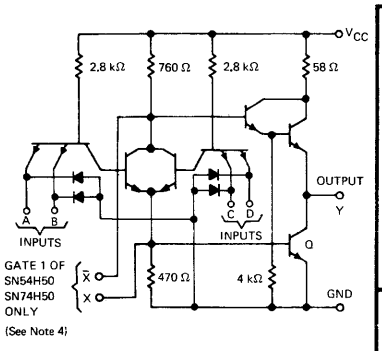
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 30

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 93 Ω		6.5	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 93 Ω		8.5	12	ns

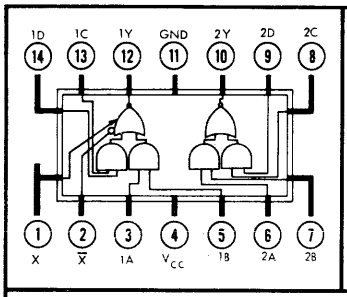
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

CIRCUIT TYPES SN54H50, SN54H51, SN74H50, SN74H51
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

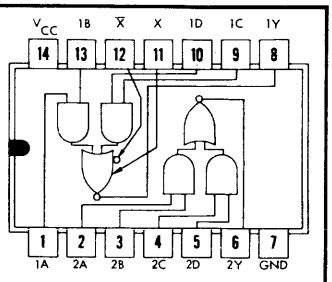
schematic (each gate)



W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{(AB) + (CD) + (X)}$
(X = Output of SN54H60/SN74H60 or SN54H62/SN74H62)

NOTES: 1. Component values are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\bar{X}$ pins open.
4. Expander inputs X and $\bar{X}$ are functional on the SN54H50 and SN75H50 circuits only. Make no external connection to X and $\bar{X}$ pins of the SN54H51 and SN74H51.
5. A total of four SN54H60/SN74H60 expander gates or one SN54H62/SN74H62 expander gate may be connected to the expander inputs.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H50, SN54H51 Circuits	4.5	5	5.5	V
SN74H50, SN74H51 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H50, SN54H51 Circuits	−55	25	125	°C
SN74H50, SN74H51 Circuits	0	25	70	°C

7

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	20		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	21				0.8	V
$V_{out(1)}$	Logical 1 output voltage	21	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	20	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	22	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	23	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	24	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	25	V_{CC} = MAX, V_{in} = 4.5 V		15.2	24	mA
$I_{CC(1)}$	Logical 1 level supply current	26	V_{CC} = MAX, V_{in} = 0		8.2	12.8	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.

‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics (SN54H50 circuits only) using expander inputs, V_{CC} = 4.5 V, T_A = −55°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\overline{x}}$	Expander-node input current	27	$V_{\overline{x}}$ = 1.4 V			−5.85	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 700 μA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = −500 μA, I_1 = 320 μA, I_2 = −320 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 470 μA, R_1 = 68 Ω			0.4	V

electrical characteristics (SN74H50 circuits only) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\overline{x}}$	Expander-node input current	27	$V_{\overline{x}}$ = 1.4 V			−6.3	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 1.1 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = −500 μA, I_1 = 570 μA, I_2 = −570 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 600 μA, R_1 = 63 Ω			0.4	V

7

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, expander pins are open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.2	11	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		6.8	11	ns

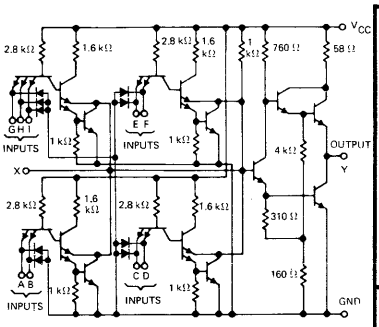
switching characteristics, (SN54H50/SN74H50 circuits only), V_{CC} = 5 V, T_A = 25°C, N = 10, $C_{\overline{x}}$ = 15 pF¶

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	75	C_L = 25 pF, R_L = 280 Ω		7.4		ns
t_{pd1}	Propagation delay time to logical 1 level	75	C_L = 25 pF, R_L = 280 Ω		11		ns

¶See curves on page 7-90 for effect of other values of $C_{\overline{x}}$.

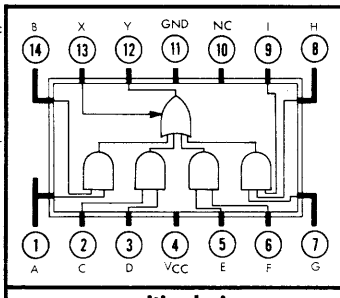
CIRCUIT TYPES SN54H52, SN74H52
EXPANDABLE 2-2-2-3-INPUT AND-OR GATES

schematic



NOTES: 1. Component values shown are nominal.
2. A total of six expander gates may be connected to the expander input X.
3. NC — No internal connection.

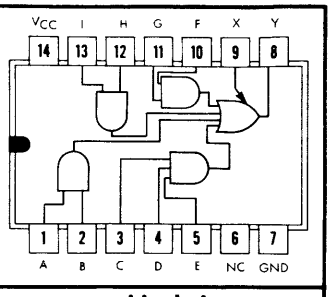
W
FLAT PACKAGE (TOP VIEW)



positive logic:

Y = (AB) + (CD) + (EF) + (GHI) + (X)
(X = Output of SN54H61/SN74H61)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic:

Y = (AB) + (CDE) + (FG) + (HI) + (X)
(X = Output of SN54H61/SN74H61)

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H52 Circuits	4.5	5	5.5	V
SN74H52 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H52 Circuits	−55	25	125	°C
SN74H52 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure logical 1 at output	30		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 0 at output	31				0.8	V
$V_{out(1)}$	Logical 1 output voltage	30	V_{CC} = MIN, V_{in} = 2 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	31	V_{CC} = MIN, V_{in} = 0.8 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	32	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	33	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	34	V_{CC} = MAX, V_{in} = 4.5 V	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	35	V_{CC} = MAX, V_{in} = 0		15.2	24	mA
$I_{CC(1)}$	Logical 1 level supply current	35	V_{CC} = MAX, V_{in} = 4.5 V		20	31	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pin is open.
‡Duration of short-circuit test should not exceed 1 second.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics (SN54H52 circuits only) using expander input, V_{CC} = 4.5 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{inX}	Expander-node input current	36	V_X = 1 V, I_{load} = −500 μA, T_A = −55°C	−2.7		−4.5	mA
$V_{out(1)}$	Logical 1 output voltage	36	V_X = 1 V, I_{load} = −500 μA, T_A = −55°C	2.4			V
$V_{out(0)}$	Logical 0 output voltage	37	I_{inX} = −300 μA, I_{sink} = 20 mA, T_A = 125°C			0.4	V

electrical characteristics (SN74H52 circuits only) using expander input, V_{CC} = 4.75 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{inX}	Expander-node input current	36	V_X = 1 V, I_{load} = −500 μA, T_A = 0°C	−2.9		−5.35	mA
$V_{out(1)}$	Logical 1 output voltage	36	V_X = 1 V, I_{load} = −500 μA, T_A = 0°C	2.4			V
$V_{out(0)}$	Logical 0 output voltage	37	I_{inX} = −300 μA, I_{sink} = 20 mA, T_A = 70°C			0.4	V

7

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, expander pin is open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		9.2	15	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		10.6	15	ns

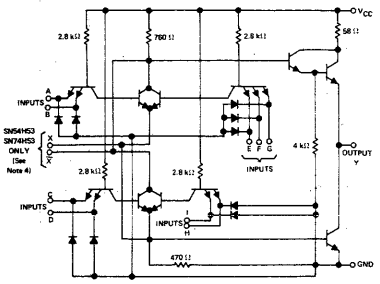
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, C_X = 15 pF¶

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	76	C_L = 25 pF, R_L = 280 Ω		9.8		ns
t_{pd1}	Propagation delay time to logical 1 level	76	C_L = 25 pF, R_L = 280 Ω		14.8		ns

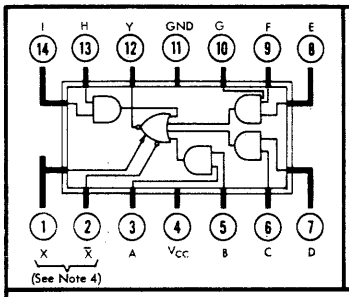
¶See curves on page 7-90 for effect of other values of C_X.

CIRCUIT TYPES SN54H53, SN54H54, SN74H53, SN74H54
EXPANDABLE 2-2-2-3-INPUT AND-OR-INVERT GATES

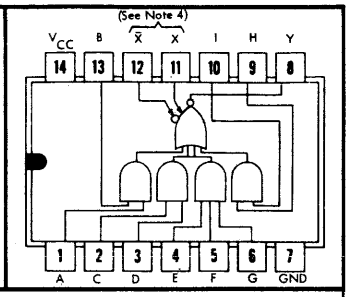
schematic



W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{(AB) + (CD) + (EFG) + (HI) + (X)}$
(X = Output of SN54H60/SN74H60 or SN54H62/SN74H62)

NOTES: 1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Expander inputs X and $\overline{X}$ are functional on the SN54H53 and SN74H53 circuits only. Make no external connection to X and $\overline{X}$ pins of the SN54H54 and SN74H54.
5. A total of four SN54H60/SN74H60 expander gates or one SN54H62/SN74H62 expander gate may be connected to the expander inputs.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H53, SN54H54 Circuits	4.5	5	5.5	V
SN74H53, SN74H54 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H53, SN54H54 Circuits	−55	25	125	°C
SN74H53, SN74H54 Circuits	0	25	70	°C

7

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure logical 0 at output	20		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	21				0.8	V
$V_{out(1)}$	Logical 1 output voltage	21	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	20	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	22	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	23	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	24	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	25	V_{CC} = MAX V_{in} = 4.5 V		9.4	14	mA
$I_{CC(1)}$	Logical 1 level supply current	26	V_{CC} = MAX, V_{in} = 0		7.1	11	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.
‡Duration of short-circuit test should not exceed 1 second.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics (SN54H53 circuits only) using expander inputs, V_{CC} = 4.5 V, T_A = −55° C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\,\overline{x}}$	Expander-node input current	27	$V_{\overline{x}}$ = 1.4 V			−5.85	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 700 μA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = −500 μA, I_1 = 320 μA, I_2 = −320 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 470 μA, R_1 = 68 Ω			0.4	V

electrical characteristics (SN74H53 circuits only) using expander inputs, V_{CC} = 4.75 V, T_A = 0° C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\,\overline{x}}$	Expander-node input current	27	$V_{\overline{x}}$ = 1.4 V			−6.3	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 1.1 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = −500 μA, I_1 = 570 μA, I_2 = −570 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 600 μA, R_1 = 63 Ω			0.4	V

7

switching characteristics, V_{CC} = 5 V, T_A = 25° C, N = 10 , expander pins are open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.2	11	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		7	11	ns

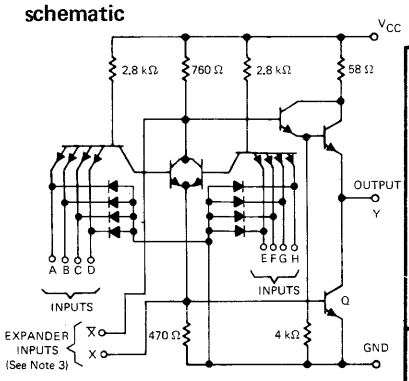
switching characteristics, (SN54H53/SN74H53 circuits only) V_{CC} = 5 V, T_A = 25°C, N = 10, $C_{\overline{x}}$ = 15 pF¶

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	75	C_L = 25 pF, R_L = 280 Ω		7.4		ns
t_{pd1}	Propagation delay time to logical 1 level	75	C_L = 25 pF, R_L = 280 Ω		11.4		ns

¶See curves on page 7-90 for effect of other values of $C_{\overline{x}}$.

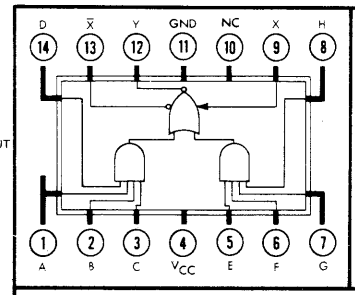
CIRCUIT TYPES SN54H55, SN74H55
EXPANDABLE 4-INPUT AND-OR-INVERT GATES

schematic

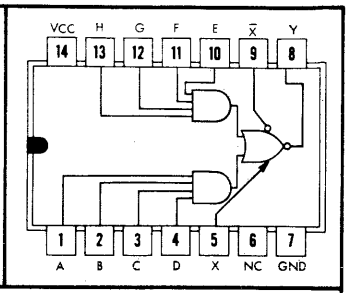


NOTES:
1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used, leave X and X̄ pins open.
4. A total of four SN54H60/SN74H60 expander gates or one SN54H62/SN74H62 expander gate may be connected to the expander inputs.
5. NC — No internal connection.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{(ABCD) + (EFGH) + (X)}$

X = Output of SN54H60/SN74H60 or SN54H62/SN74H62 circuit.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H55 Circuits	4.5	5	5.5	V
SN74H55 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H55 Circuits	−55	25	125	°C
SN74H55 Circuits	0	25	70	°C

7 electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of either AND section to ensure logical 0 at output	20		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	21				0.8	V
$V_{out(1)}$	Logical 1 output voltage	21	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	20	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	22	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	23	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	24	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	25	V_{CC} = MAX, V_{in} = 4.5 V		7.5	12	mA
$I_{CC(1)}$	Logical 1 level supply current	26	V_{CC} = MAX, V_{in} = 0		4.5	6.4	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.

‡Duration of short-circuit test should not exceed 1 second.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics (SN54H55 circuits only) using expander inputs, V_{CC} = 4.5 V, T_A = −55°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\bar{x}}$	Expander-node input current	27	$V_{\bar{x}}$ = 1.4 V			−5.85	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 700 μA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = −500 μA, I_1 = 320 μA, I_2 = −320 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 470 μA, R_1 = 68 Ω			0.4	V

electrical characteristics (SN74H55 circuits only) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\bar{x}}$	Expander-node input current	27	$V_{\bar{x}}$ = 1.4 V			−6.3	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 1.1 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = −500 μA, I_1 = 570 μA, I_2 = −570 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 600 μA, R_1 = 63 Ω			0.4	V

7

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, expander pins are open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.5	11	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		7	11	ns

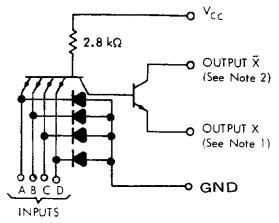
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, $C_{\bar{x}}$ = 15 pF¶

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	75	C_L = 25 pF, R_L = 280 Ω		7.7		ns
t_{pd1}	Propagation delay time to logical 1 level	75	C_L = 25 pF, R_L = 280 Ω		11.4		ns

¶ See curves on page 7-90 for effect of other values of $C_{\bar{x}}$.

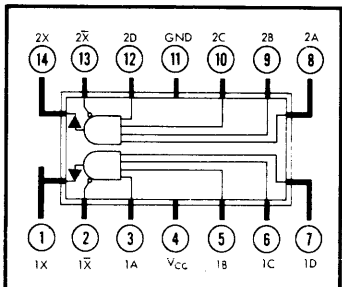
CIRCUIT TYPE SN54H60
DUAL 4-INPUT EXPANDER (FOR USE WITH SN54H50, SN54H53, SN54H55 CIRCUITS)

schematic (each expander)

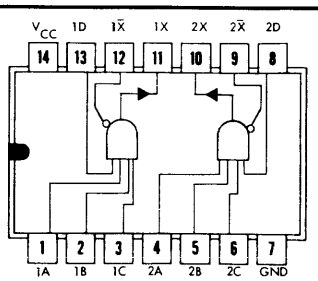


NOTES: 1. Connect to X input of SN54H50, SN54H53, or SN54H55 circuit.
2. Connect to $\bar{X}$ input of SN54H50, SN54H53, or SN54H55 circuit.
3. Component values shown are nominal.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: X = ABCD
when connected to X and $\bar{X}$ pins of SN54H50, SN54H53, or SN54H55 circuit.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Maximum number of expanders that may be fanned-in to one SN54H50, SN54H53, or SN54H55 circuit 4

electrical characteristics (unless otherwise noted T_A = –55°C to 125°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	38		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	39				0.8	V
V_{on}	On-state output voltage	38	V_{CC} = 4.5 V, V_{in} = 2 V, V_1 = 1 V, I_{on} = 5.85 mA, T_A = –55°C			0.4	V
			V_{CC} = 5.5 V, V_{in} = 2 V, V_1 = 0.6 V, I_{on} = 7.85 mA, T_A = 125°C			0.4	V
I_{off}	Off-state output current	39	V_{CC} = 4.5 V, V_{in} = 0.8 V, V_1 = 4.5 V, R = 575 Ω, T_A = –55°C			320	μA
I_{on}	On-state output current	40	V_{CC} = 4.5 V, V_{in} = 2 V, V_1 = 1 V, T_A = –55°C	–470			μA
$I_{in(0)}$	Logical 0 level input current (each input)	39	V_{CC} = 5.5 V, V_{in} = 0.4 V			–2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	41	V_{CC} = 5.5 V, V_{in} = 2.4 V			50	μA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	42	V_{CC} = 5.5 V, V_{in} = 4.5 V, V_1 = 0.85 V		1.9	3.5	mA
$I_{CC(off)}$	Off-state supply current	42	V_{CC} = 5.5 V, V_{in} = 0, V_1 = 0.85 V		3	4.5	mA

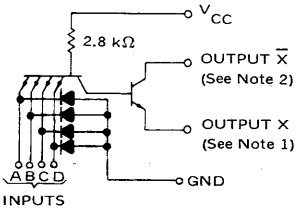
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

output capacitance, V_{CC} and GND terminals open, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{\bar{x}}$	Effective capacitance of output transistor Q_1	79	f = 1 MHz		1.3		pF

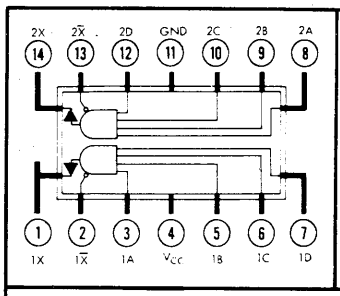
CIRCUIT TYPE SN74H60
DUAL 4-INPUT EXPANDER

schematic (each expander)

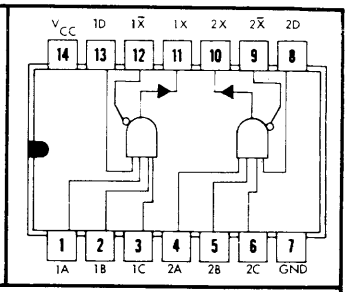


NOTES: 1. Connect to X input of SN74H50, SN74H53, or SN74H55 circuit.
2. Connect to $\overline{X}$ input of SN74H50, SN74H53, or SN74H55 circuit.
3. Component values shown are nominal.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: X = ABCD
when connected to X and $\overline{X}$ pins of SN74H50, SN74H53, or SN74H55 circuits.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Maximum number of expanders that may be fanned-in to one SN74H50, SN74H53, or SN74H55 circuit 4

electrical characteristics (unless otherwise noted T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	38		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	39				0.8	V
V_{on}	On-state output voltage	38	V_{CC} = 4.75 V, V_{in} = 2 V, V_I = 1 V, I_{on} = 6.3 mA, T_A = 0°C			0.4	V
			V_{CC} = 5.25 V, V_{in} = 2 V, V_I = 0.6 V, I_{on} = 7.4 mA, T_A = 70°C			0.4	V
I_{off}	Off-state output current	39	V_{CC} = 4.75 V, V_{in} = 0.8 V, V_I = 4.5 V, R = 575 Ω, T_A = 0°C			570	μA
I_{on}	On-state output current	40	V_{CC} = 4.75 V, V_{in} = 2 V, V_I = 1 V, T_A = 0°C	−600			μA
$I_{in(0)}$	Logical 0 level input current (each input)	39	V_{CC} = 5.25 V, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	41	V_{CC} = 5.25 V, V_{in} = 2.4 V			50	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	42	V_{CC} = 5.25 V, V_{in} = 4.5 V, V_I = 0.85 V		1.9	3.5	mA
$I_{CC(off)}$	Off-state supply current	42	V_{CC} = 5.25 V, V_{in} = 0, V_I = 0.85 V		3	4.5	mA

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

output capacitance, V_{CC} and GND terminals open, T_A = 25°C

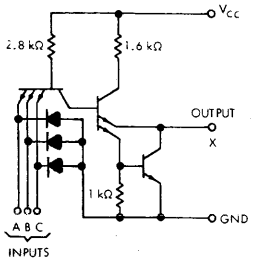
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{\overline{x}}$	Effective capacitance of output transistor Q_1	79	f = 1 MHz		1.3		pF

7

CIRCUIT TYPES SN54H61, SN74H61
TRIPLE 3-INPUT EXPANDERS

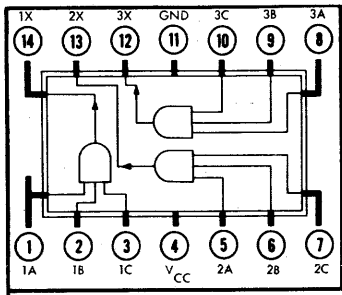
(FOR USE WITH SN54H52, SN74H52 CIRCUITS)

schematic (each expander)

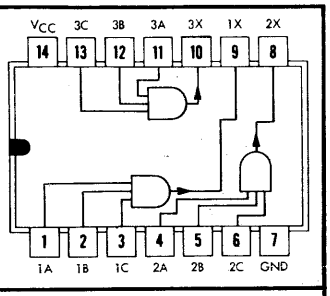


NOTES: 1. Component values shown are nominal.
2. A total of six expander gates may be connected to the SN54H52/SN74H52 expander input.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: X = ABC
when connected to the X input of the SN54H52 or SN74H52 circuit.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H61 Circuits	4.5	5	5.5	V
SN74H61 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H61 Circuits	−55	25	125	°C
SN74H61 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	43				0.8	V
I_{off}	Off-state reverse current	43	V_{CC} = MIN, $V_{in(0)}$ = 0.8 V, V_{off} = 2.2 V, T_A = MAX			50	μA
$I_{in(0)}$	Logical 0 level input current (each input)	44	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	45	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	46	V_{CC} = MAX, V_{in} = 4.5 V		11	16	mA
$I_{CC(off)}$	Off-state supply current	46	V_{CC} = MAX, V_{in} = 0		5	7	mA

electrical characteristics SN54H61 circuits only

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	47	V_{CC} = 4.5 V	2			V
V_{on}	On-state output voltage	47	V_{CC} = 4.5 V, $V_{in(1)}$ = 2 V, I_{on} = 4.5 mA, T_A = −55°C			1	V

electrical characteristics SN74H61 circuits only

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	47	V_{CC} = 4.75 V	2			V
V_{on}	On-state output voltage	47	V_{CC} = 4.75 V, $V_{in(1)}$ = 2 V, I_{on} = 5.35 mA, T_A = 0°C			1	V

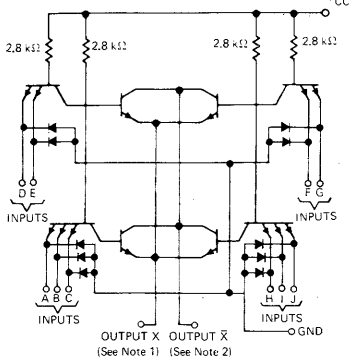
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

output capacitance, V_{CC} and GND terminals open, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_x	Effective capacitance of output transistor Q_1	80	f = 1 MHz		1.3		pF

CIRCUIT TYPE SN54H62
3-2-2-3-INPUT AND-OR EXPANDER

schematic

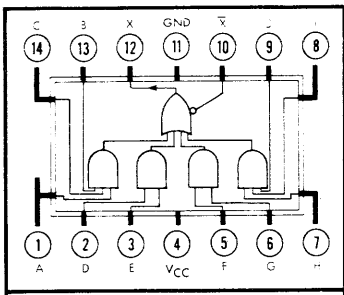


NOTES: 1. Connect to X input of SN54H50, SN54H53, or SN54H55 circuit.

2. Connect to $\overline{X}$ input of SN54H50, SN54H53, or SN54H55 circuit.

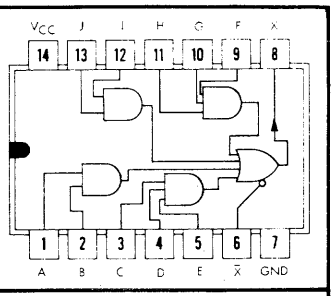
3. Component values shown are nominal.

W
FLAT PACKAGE (TOP VIEW)



positive logic:
X = (ABC) + (DE) + (FG) + (HIJ)
when connected to X and $\overline{X}$ pins of
SN54H50, SN54H53, or SN54H55 circuit.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic:
X = (AB) + (CDE) + (FGH) + (IJ)
when connected to X and $\overline{X}$ pins of
SN54H50, SN54H53, or SN54H55 circuit.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Maximum number of expanders that may be fanned-in to one SN54H50, SN54H53, or SN54H55 circuit 1

electrical characteristics (unless otherwise noted T_A = –55°C to 125°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure output is in the on state	48		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure output is in the off state	49				0.8	V
V_{on}	On-state output voltage	48	V_{CC} = 4.5 V, V_{in} = 2 V, V_1 = 1 V, I_{on} = 5.85 mA, T_A = –55°C			0.4	V
			V_{CC} = 5.5 V, V_{in} = 2 V, V_1 = 0.6 V, I_{on} = 7.85 mA, T_A = 125°C			0.4	V
I_{off}	Off-state output current	49	V_{CC} = 4.5 V, V_{in} = 0.8 V, V_1 = 4.5 V, R = 575 Ω, T_A = –55°C			320	μA
I_{on}	On-state output current	50	V_{CC} = 4.5 V, V_{in} = 2 V, V_1 = 1 V, T_A = –55°C	–470			μA
$I_{in(0)}$	Logical 0 level input current (each input)	51	V_{CC} = 5.5 V, V_{in} = 0.4 V			–2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	52	V_{CC} = 5.5 V, V_{in} = 2.4 V			50	μA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	53	V_{CC} = 5.5 V, V_{in} = 4.5 V, V_1 = 0.85 V		3.8	7	mA
$I_{CC(off)}$	Off-state supply current	53	V_{CC} = 5.5 V, V_{in} = 0, V_1 = 0.85 V		6	9	mA

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

output capacitance, V_{CC} and GND terminals open, T_A = 25°C

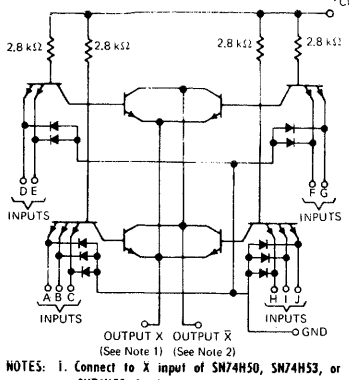
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{\overline{x}}$	Effective capacitance of output transistor Q_1	79	f = 1 MHz		1.3		pF

7

CIRCUIT TYPE SN74H62
3-2-2-3-INPUT AND-OR EXPANDER

(FOR USE WITH SN74H50, SN74H53, SN74H55 CIRCUITS)

schematic

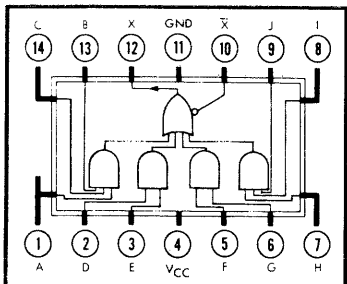


NOTES: 1. Connect to X input of SN74H50, SN74H53, or SN74H55 circuit.

2. Connect to X̄ input of SN74H50, SN74H53, or SN74H55 circuit.

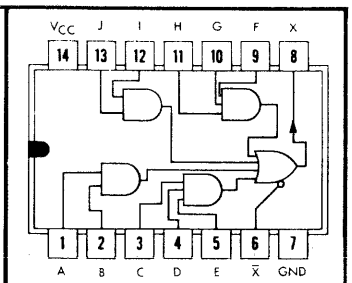
3. Component values shown are nominal.

W
FLAT PACKAGE (TOP VIEW)



positive logic:
X = (ABC) + (DE) + (FG) + (HIJ)
when connected to X and X̄ pins of SN74H50, SN74H53, or SN74H55 circuit.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic:
X = (AB) + (CDE) + (FGH) + (IJ)
when connected to X and X̄ pins of SN74H50, SN74H53, or SN74H55 circuit.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V

Maximum number of expanders that may be fanned-in to one SN74H50, SN74H53, or SN74H55 circuit 1

electrical characteristics (unless otherwise noted T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure output is in the on state	48		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure output is in the off state	49				0.8	V
V_{on}	On-state output voltage	48	V_{CC} = 4.75 V, V_{in} = 2 V, V_I = 1 V, I_{on} = 6.3 mA, T_A = 0°C			0.4	V
			V_{CC} = 5.25 V, V_{in} = 2 V, V_I = 0.6 V, I_{on} = 7.4 mA, T_A = 70°C			0.4	V
I_{off}	Off-state output current	49	V_{CC} = 4.75 V, V_{in} = 0.8 V, V_I = 4.5 V, R = 575 Ω, T_A = 0°C			570	μA
I_{on}	On-state output current	50	V_{CC} = 4.75 V, V_{in} = 2 V, V_I = 1 V, T_A = 0°C	−600			μA
$I_{in(0)}$	Logical 0 level input current (each input)	51	V_{CC} = 5.25 V, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	52	V_{CC} = 5.25 V, V_{in} = 2.4 V			50	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	53	V_{CC} = 5.25 V, V_{in} = 4.5 V, V_I = 0.85 V		3.8	7	mA
$I_{CC(off)}$	Off-state supply current	53	V_{CC} = 5.25 V, V_{in} = 0, V_I = 0.85 V		6	9	mA

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

output capacitance, V_{CC} and GND terminals open, T_A = 25°C

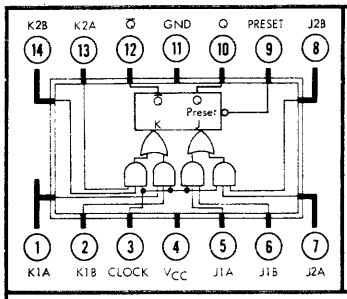
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{\bar{X}}$	Effective capacitance of output transistor Q_1	79	f = 1 MHz		1.3		pF

logic

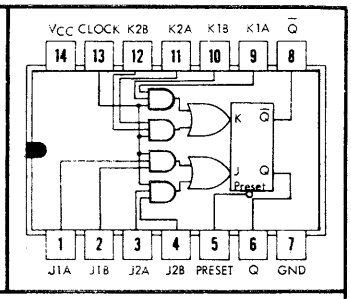
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. J = (J1A • J1B) + (J2A • J2B)
2. K = (K1A • K1B) + (K2A • K2B)
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



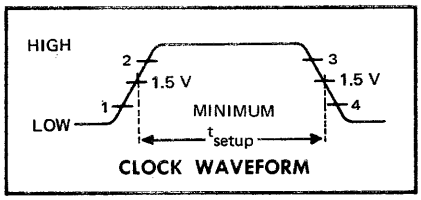
positive logic: Low input to preset sets Q to logical 1
Preset is independent of clock.

description

These J-K flip-flops are based on the master-slave principle. The AND-OR gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND-OR gate inputs to master
3. Disable AND-OR gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

7

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H71 Circuits	4.5	5	5.5	V
SN74H71 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H71 Circuits	−55	25	125	°C
SN74H71 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See Above)	≥ $t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	54 and 55		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	54 and 55				0.8	V
$V_{out(1)}$	Logical 1 output voltage	54	V_{CC} = MIN, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	55	V_{CC} = MIN, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, or K2B	56	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(0)}$	Logical 0 level input current at preset	56	V_{CC} = MAX, V_{in} = 0.4 V			−6	mA
$I_{in(0)}$	Logical 0 level input current at clock	56	V_{CC} = MAX, V_{in} = 0.4 V			−4	mA
$I_{in(1)}$	Logical 1 level input current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, or K2B	57	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset	57	V_{CC} = MAX, V_{in} = 2.4 V			150	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	57	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	58	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	57	V_{CC} = MAX		19	30	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

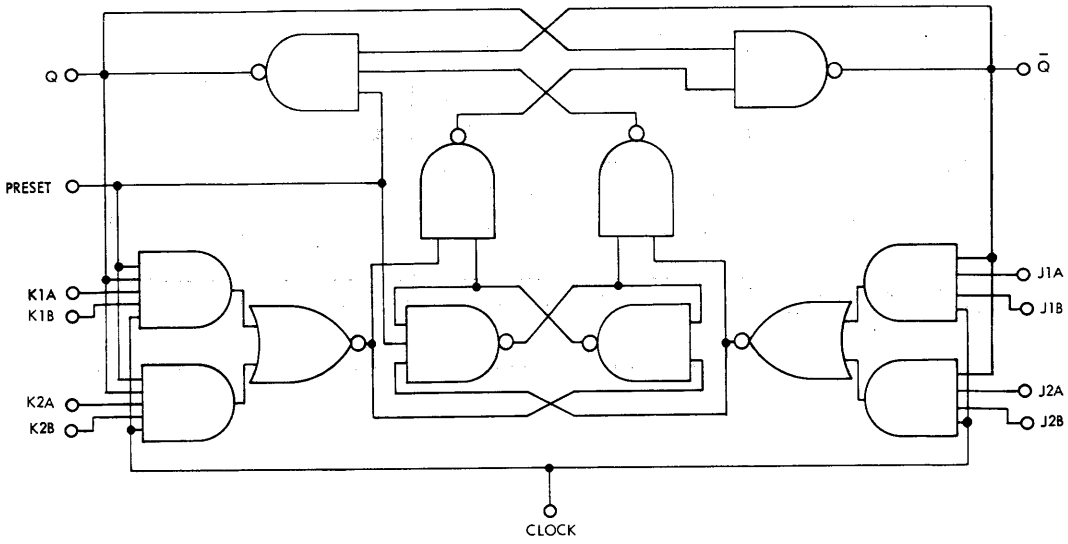
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

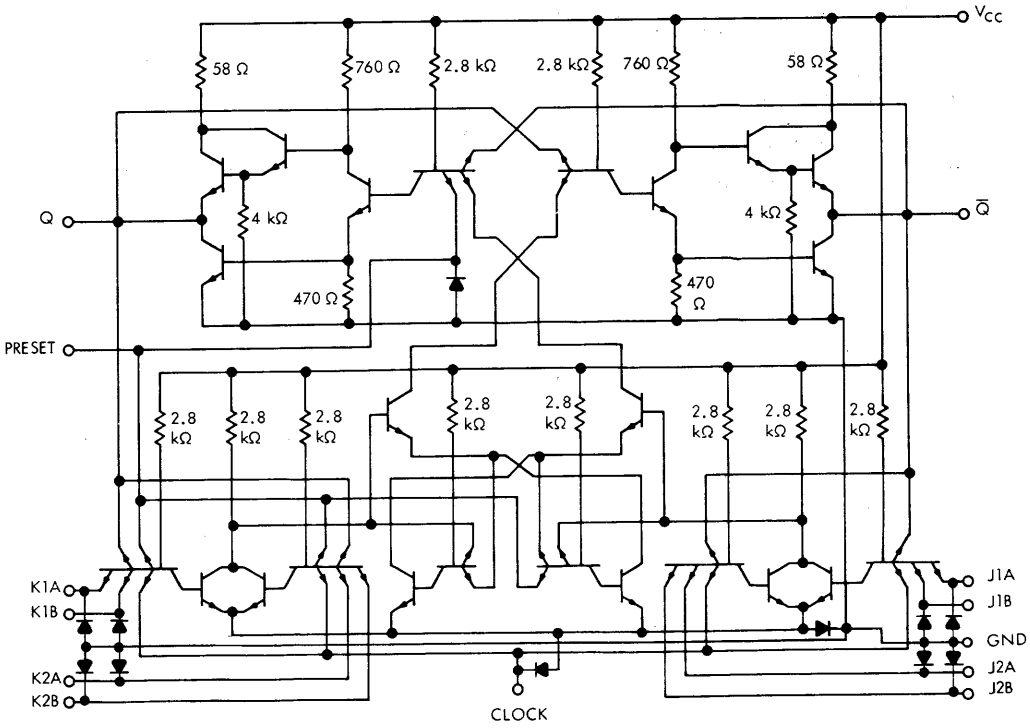
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	77	C_L = 25 pF, R_L = 280 Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset to output	78	C_L = 25 pF, R_L = 280 Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output	78	C_L = 25 pF, R_L = 280 Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	6	14	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	10	22	27	ns

functional block diagram



schematic



Component values shown are nominal.

7

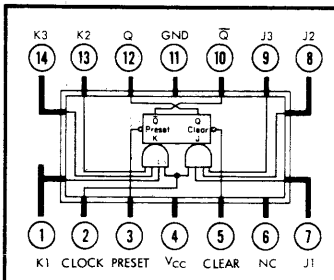
CIRCUIT TYPES SN54H72, SN74H72
J-K MASTER-SLAVE FLIP-FLOPS

logic

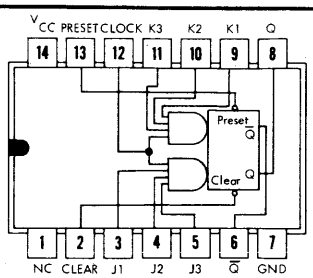
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. $J = J1 \cdot J2 \cdot J3$
2. $K = K1 \cdot K2 \cdot K3$
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



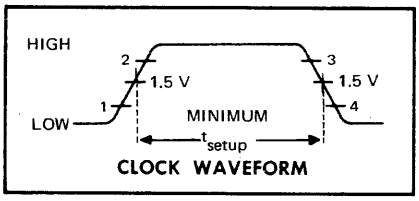
positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These J-K flip-flops are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H72 Circuits	4.5	5	5.5	V
SN74H72 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H72 Circuits	−55	25	125	°C
SN74H72 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See Above)	≥ $t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	59 and 60			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	59 and 60					0.8	V
$V_{out(1)}$	Logical 1 output voltage	59	V_{CC} = MIN,	I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	60	V_{CC} = MIN,	I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, K3, or clock	61	V_{CC} = MAX,	V_{in} = 0.4 V			−2	mA
$I_{in(0)}$	Logical 0 level input current at preset or clear	61	V_{CC} = MAX,	V_{in} = 0.4 V			−4	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	62	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	62	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	62	V_{CC} = MAX,	V_{in} = 2.4 V			100	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	63	V_{CC} = MAX,	V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	62	V_{CC} = MAX			16	25	mA

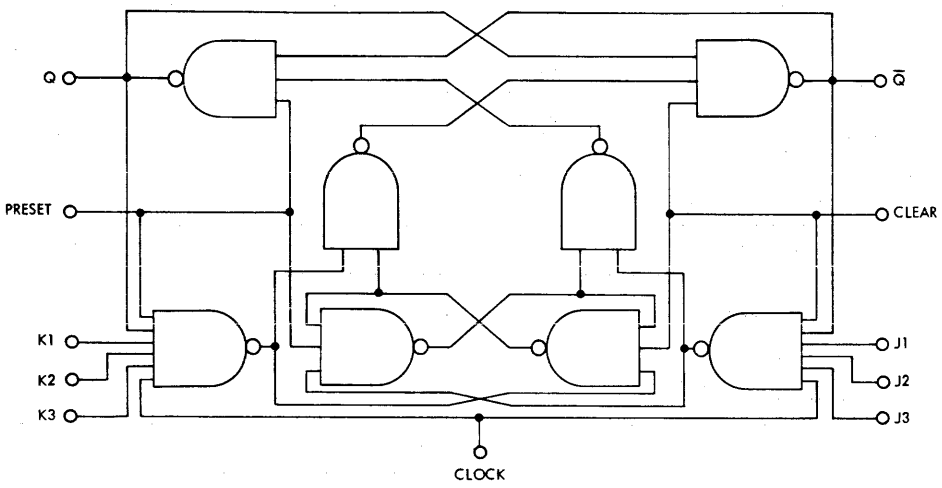
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

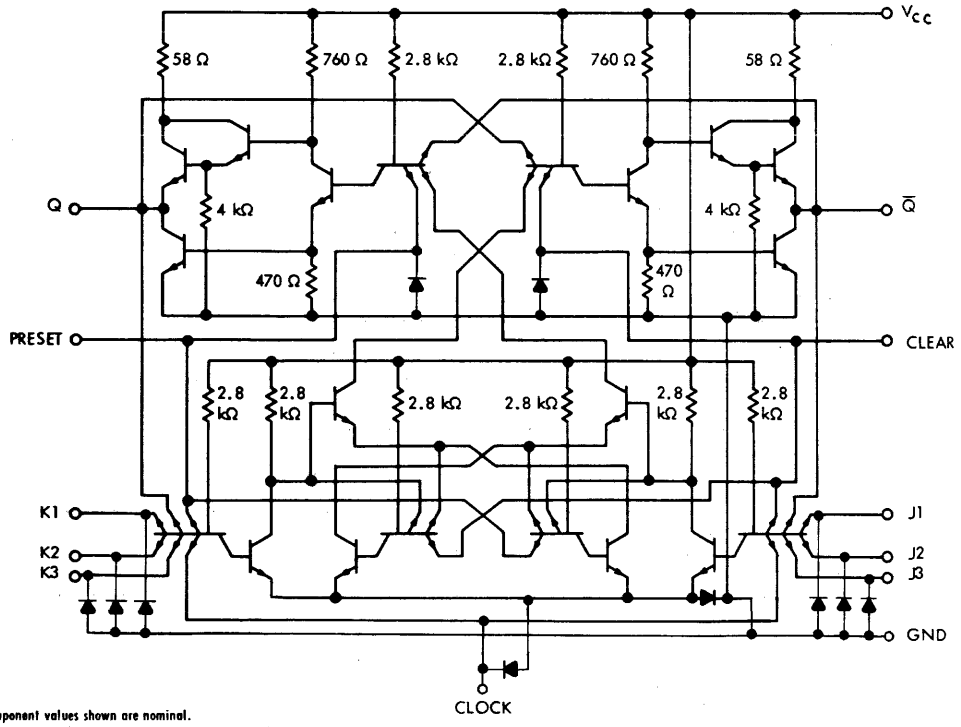
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	77	C_L = 25 pF,	R_L = 280 Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	78	C_L = 25 pF,	R_L = 280 Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	78	C_L = 25 pF,	R_L = 280 Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF,	R_L = 280 Ω	6	14	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF,	R_L = 280 Ω	10	22	27	ns

CIRCUIT TYPES SN54H72, SN74H72
J-K MASTER-SLAVE FLIP-FLOPS

functional block diagram



schematic



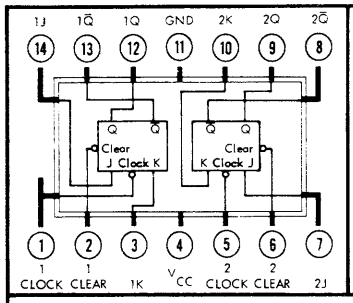
Component values shown are nominal.

logic

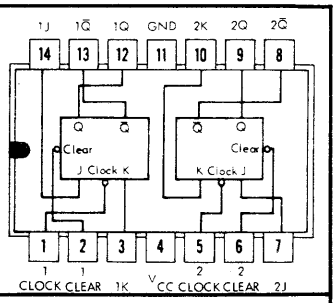
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to clear sets Q to logical 0
Clear is independent of clock

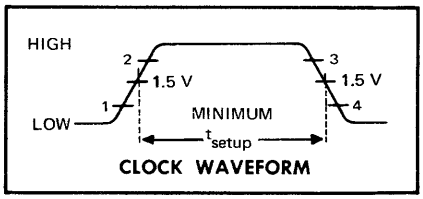
description

These J-K flip-flops are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections.

The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

7

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H73 Circuits	4.5	5	5.5	V
SN74H73 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H73 Circuits	−55	25	125	°C
SN74H73 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	12			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See Above)	≥ $t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65					0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN,	I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN,	I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or clock	66	V_{CC} = MAX,	V_{in} = 0.4 V			−2	mA
$I_{in(0)}$	Logical 0 level input current at clear	66	V_{CC} = MAX,	V_{in} = 0.4 V			−4	mA
$I_{in(1)}$	Logical 1 level input current at J or K	67	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	67	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	67	V_{CC} = MAX,	V_{in} = 2.4 V			100	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	68	V_{CC} = MAX,	V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX			32	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

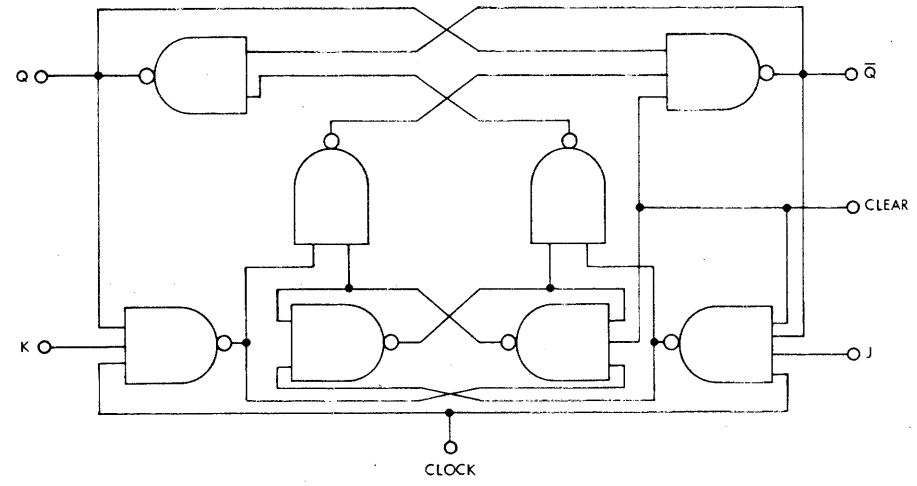
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

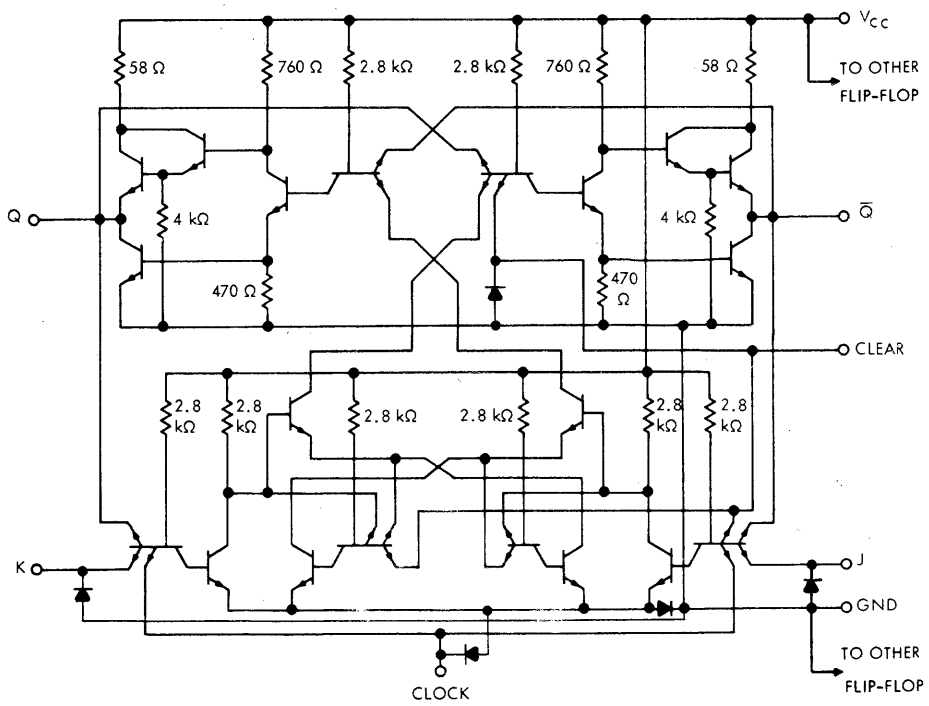
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	77	C_L = 25 pF,	R_L = 280 Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	78	C_L = 25 pF,	R_L = 280 Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	78	C_L = 25 pF,	R_L = 280 Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF,	R_L = 280 Ω	6	14	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF,	R_L = 280 Ω	10	22	27	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



Component values shown are nominal.

7

CIRCUIT TYPES SN54H74, SN74H74
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- Maximum Clock Frequency: 35 Megahertz
- Positive-Edge Triggering
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Input Clamping Diodes Simplify System Design
- Fully Compatible with most TTL and DTL Circuits
- Typical Power Dissipation: 75 Milliwatts per Flip-Flop

logic

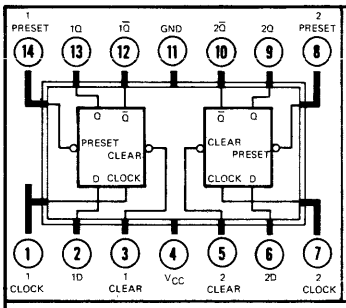
TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
L	L	H
H	H	L

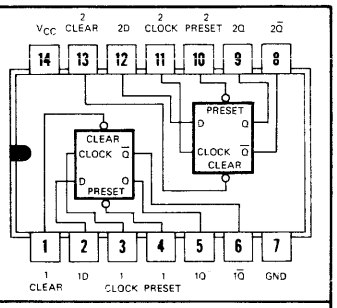
H = high level, L = low level

NOTES: A. t_n = bit time before clock pulse.
B. t_{n+1} = bit time after clock pulse.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



asynchronous inputs: Low input to preset sets Q to high level
Low input to clear sets Q to low level
Preset and clear are independent of clock

description

These monolithic, high-speed, dual, edge-triggered flip-flops utilize TTL circuitry to perform D-type flip-flop logic. Each flip-flop has individual clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify systems design. A full fan-out to 10 normalized Series 54H/74H loads is available from each of the outputs in the low-level condition. In the high-level state, a fan-out of 20 is available to facilitate tying unused inputs to used inputs. Maximum clock frequency is 35 megahertz, with a typical power dissipation of 75 milliwatts per flip-flop.

The SN54H74 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74H74 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54H74 Circuits . . . . . −55°C to 125°C
SN74H74 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

		SN54H74			SN74H74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Clock frequency, f_{clock}		0		35	0		35	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 87 or 88)		15			15			ns
Width of preset pulse, $t_{w(preset)}$ (see Figure 86)		25			25			ns
Width of clear pulse, $t_{w(clear)}$ (see Figure 86)		25			25			ns
Input setup time, t_{setup} (see Note 3)	High-level data (see Figure 87)	10			10			ns
	Low-level data (see Figure 88)	15			15			ns
Input hold time, t_{hold} (see Note 4 and Figures 87 and 88)		0			0			ns
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

NOTES: 3. Setup time is the interval immediately preceding the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	81 and 82			2			V
V_{IL}	Low-level input voltage	81 and 82					0.8	V
V_{OH}	High-level output voltage	81	V_{CC} = MIN, I_{OH} = −1 mA		2.4	3.5		V
V_{OL}	Low-level output voltage	82	V_{CC} = MIN, I_{OL} = 20 mA			0.22	0.4	V
I_{IH}	High-level input current into D	83	V_{CC} = MAX, V_I = 2.4 V				50	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current into preset or clock	83	V_{CC} = MAX, V_I = 2.4 V				100	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current into clear	83	V_{CC} = MAX, V_I = 2.4 V				150	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current into preset or D	84	V_{CC} = MAX, V_I = 0.4 V				−2	mA
I_{IL}	Low-level input current into clear or clock	84	V_{CC} = MAX, V_I = 0.4 V				−4	mA
I_{OS}	Short-circuit output current§	85	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current	83	V_{CC} = MAX	SN54H74		30	42	mA
				SN74H74		30	50	

7

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

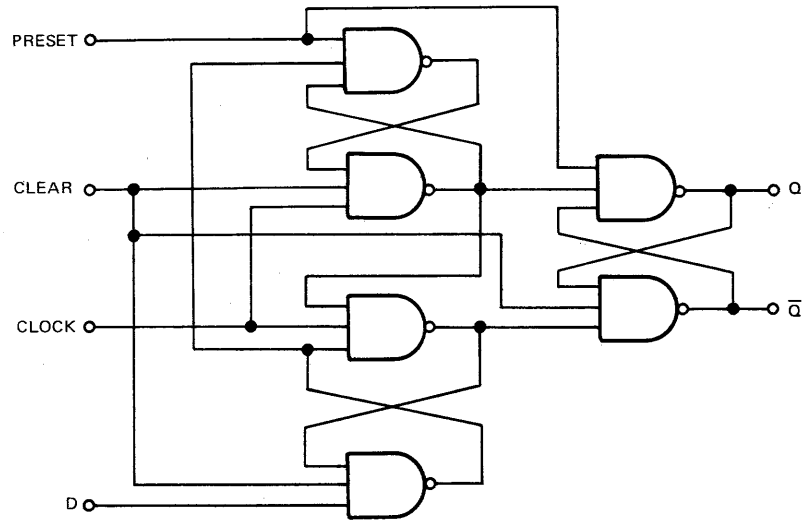
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

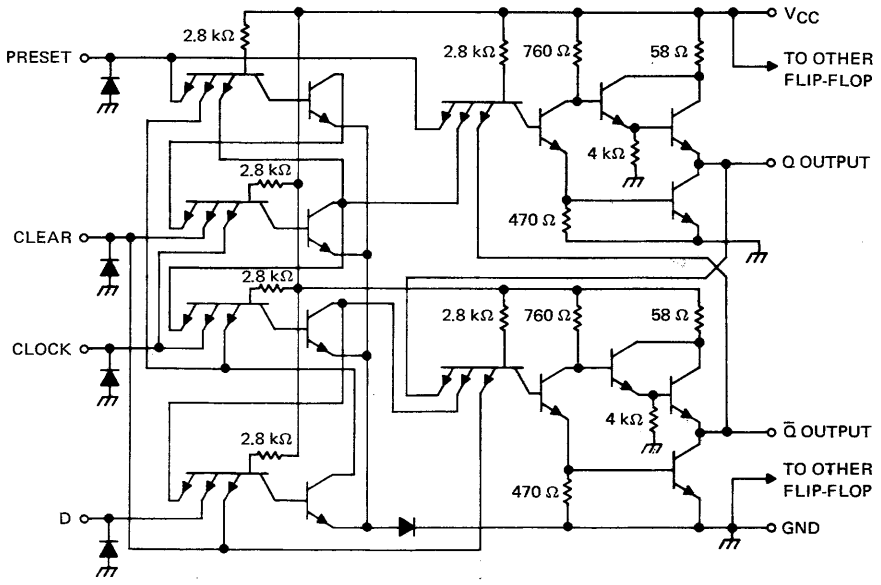
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	87 and 88	C_L = 25 pF, R_L = 280 Ω	35	43		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset inputs	86				20	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset inputs	86				30	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock input	87 and 88		4	8.5	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock input	87 and 88		7	13	20	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

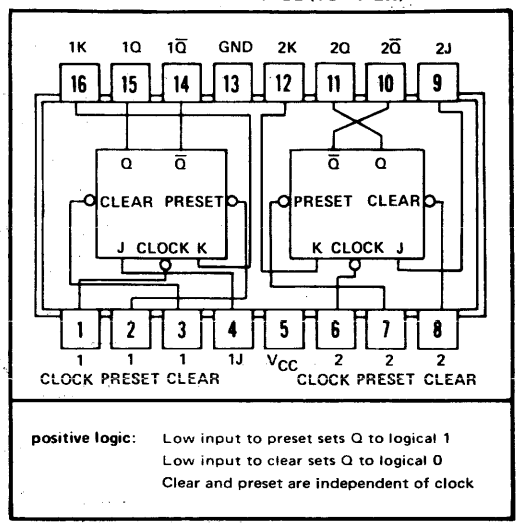
CIRCUIT TYPES SN54H76, SN74H76
DUAL J-K MASTER-SLAVE FLIP-FLOPS

logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse
2. t_{n+1} = Bit time after clock pulse

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Clear and preset are independent of clock

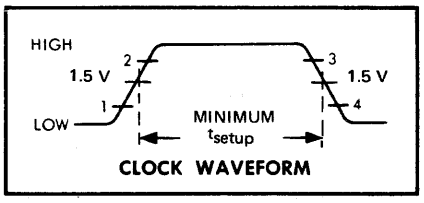
†Pin assignments for these circuits are the same for all packages.

description

These dual J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	SN54H76			SN74H76			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Width of clock pulse, $t_{p(clock)}$ (See Figure 77)	12			12			ns
Width of preset pulse, $t_{p(preset)}$ (See Figure 78)	16			16			ns
Width of clear pulse, $t_{p(clear)}$ (See Figure 78)	$\geqslant t_{p(clock)}$			$\geqslant t_{p(clock)}$			
Input setup time, t_{setup} (See Above)							
Input hold time, t_{hold}	0			0			
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65				0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or clock	66	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(0)}$	Logical 0 level input current at clear or preset	66	V_{CC} = MAX, V_{in} = 0.4 V			−4	mA
$I_{in(1)}$	Logical 1 level input current at J, K, or clock	67	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear or preset	67	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	68	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX, V_{in} = 4.5 V		32	50	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time.

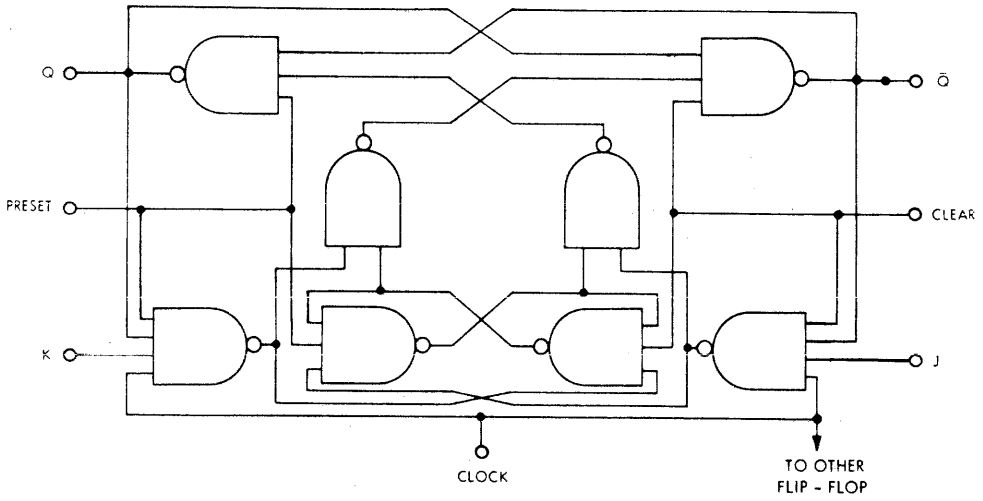
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

7

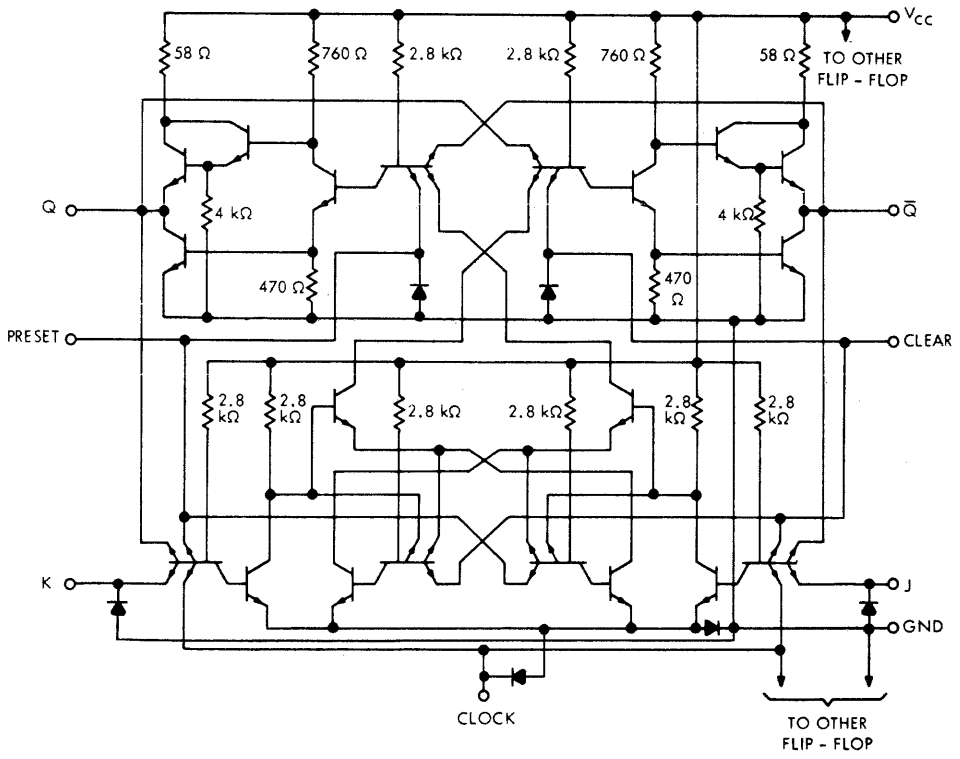
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	77	C_L = 25 pF, R_L = 280 Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	78	C_L = 25 pF, R_L = 280 Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	78	C_L = 25 pF, R_L = 280 Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	6	14	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	10	22	27	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



Component values shown are nominal.

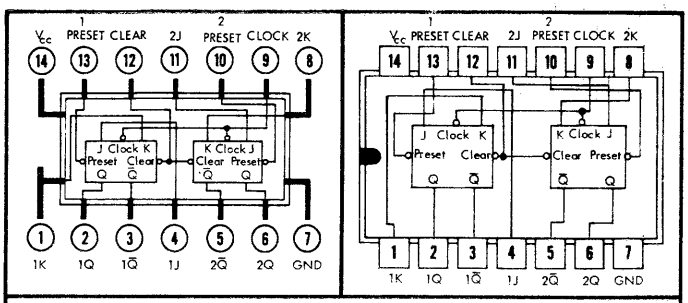
logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

W
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

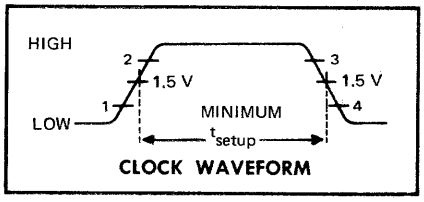


positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections.
The sequence of operation is as follows:
1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H78 Circuits	4.5	5	5.5	V
SN74H78 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H78 Circuits	−55	25	125	°C
SN74H78 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See Above)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65					0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN,	I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN,	I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	66	V_{CC} = MAX,	V_{in} = 0.4 V			−2	mA
$I_{in(0)}$	Logical 0 level input current at preset or clock	66	V_{CC} = MAX,	V_{in} = 0.4 V			−4	mA
$I_{in(0)}$	Logical 0 level input current at clear	66	V_{CC} = MAX,	V_{in} = 0.4 V			−8	mA
$I_{in(1)}$	Logical 1 level input current at J or K	67	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clock	67	V_{CC} = MAX,	V_{in} = 2.4 V			100	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	67	V_{CC} = MAX,	V_{in} = 2.4 V			200	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	69	V_{CC} = MAX,	V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX			32	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

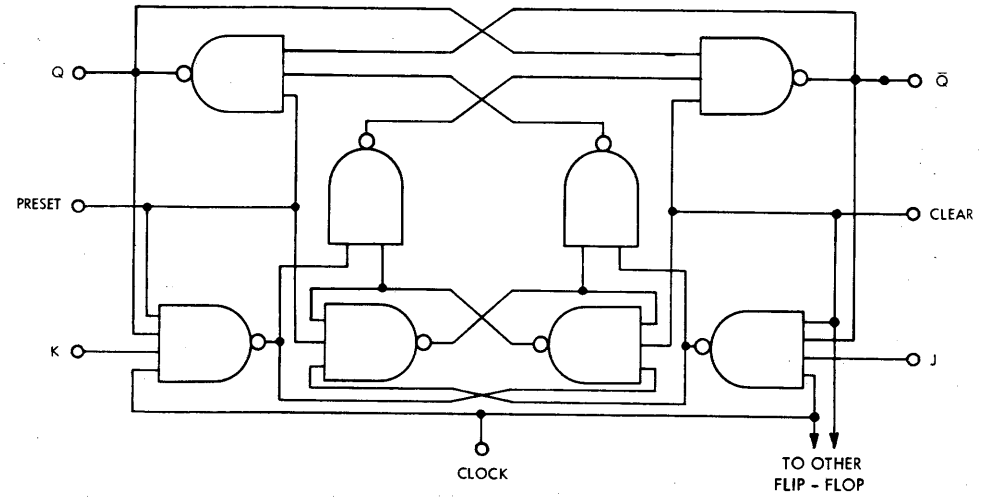
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§All typical values are at V_{CC} = 5 V, T_A = 25°C.

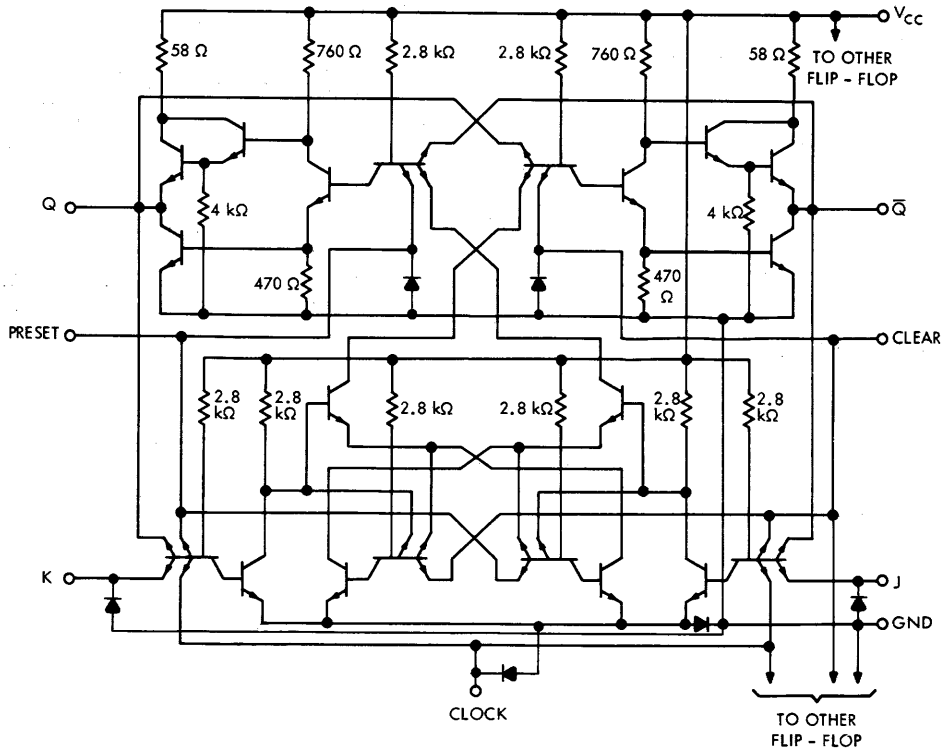
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	77	C_L = 25 pF,	R_L = 280 Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	78	C_L = 25 pF,	R_L = 280 Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	78	C_L = 25 pF,	R_L = 280 Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF,	R_L = 280 Ω	6	14	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF,	R_L = 280 Ω	10	22	27	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



Component values shown are nominal.

7

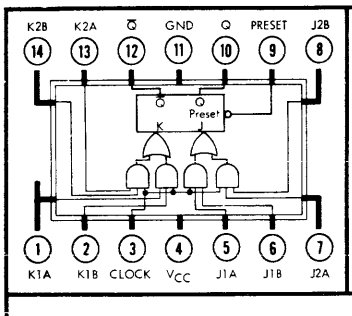
CIRCUIT TYPES SN54H101, SN74H101
J-K EDGE-TRIGGERED FLIP-FLOPS

logic

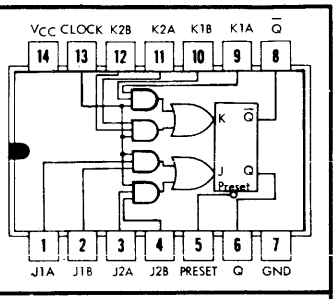
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. J = (J1A • J1B) + (J2A • J2B)
2. K = (K1A • K1B) + (K2A • K2B)
3. t_n = Bit time before clock pulse
4. t_{n+1} = Bit time after clock pulse

W
FLAT PACKAGE (TOP VIEW)



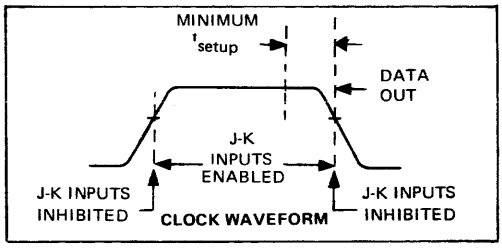
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Preset is independent of clock.

description

These monolithic J-K flip-flops are negative-edge-triggered. The AND-OR gate inputs are inhibited while the clock input is low; when the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.



recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H101 Circuits	4.5	5	5.5	V
SN74H101 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H101 Circuits	−55	25	125	°C
SN74H101 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See Above): Logical 1	10			ns
Logical 0	13			ns
Input Hold Time, t_{hold}	0			ns
Clock Pulse Transition Time, t_0 (See Figure 77)			150	ns

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	54 and 55		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	54 and 55				0.8	V
$V_{out(1)}$	Logical 1 output voltage	54	V_{CC} = MIN, I_{load} = −500 μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	55	V_{CC} = MIN, I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, or preset	56	V_{CC} = MAX, V_{in} = 0.4 V		−1	−2	mA
$I_{in(0)}$	Logical 0 level input current at clock	56	V_{CC} = MAX, V_{in} = 0.4 V		−3	−4.8	mA
$I_{in(1)}$	Logical 1 level input current at J or K	57	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset	57	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	57	V_{CC} = MAX, V_{in} = 2.4 V	0		−1	mA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	58	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	57	V_{CC} = MAX		20	38	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

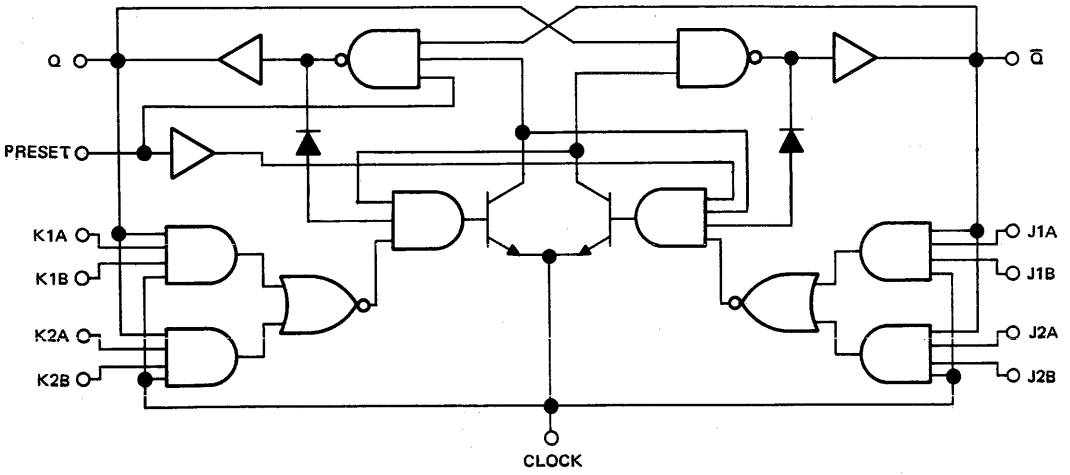
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

7

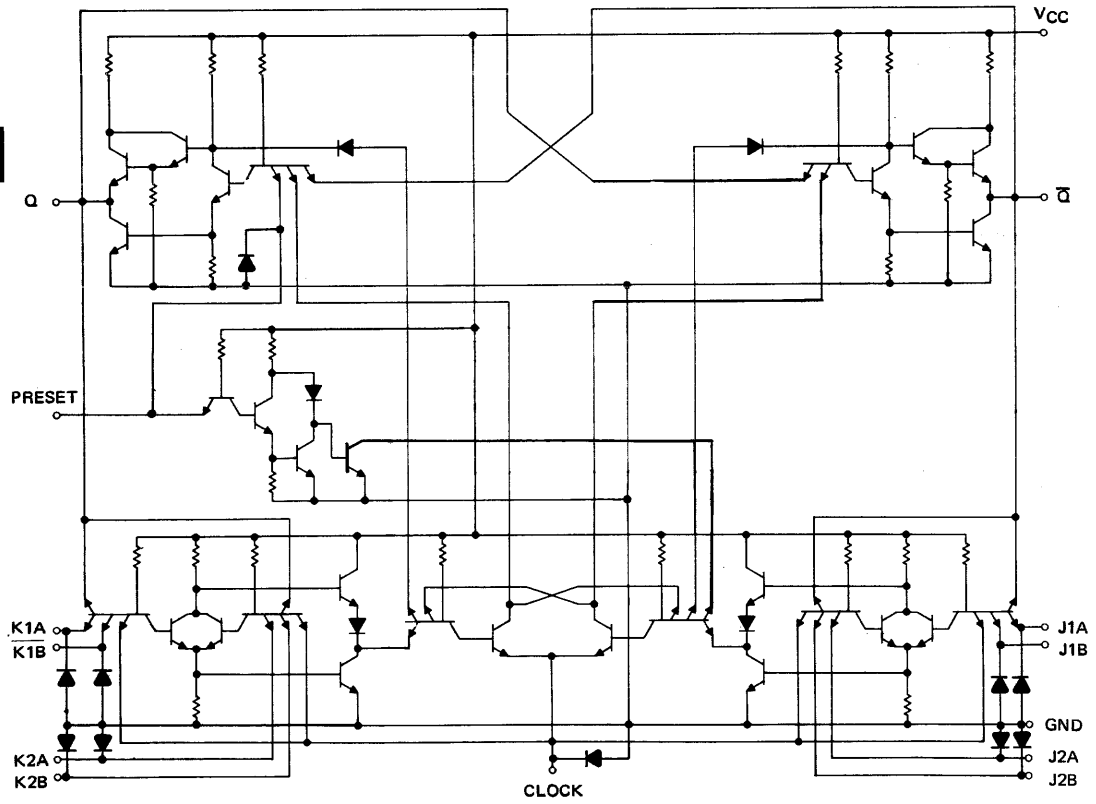
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	77	C_L = 25 pF, R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset to output	78	C_L = 25 pF, R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output (clock low)	78	C_L = 25 pF, R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output (clock high)	78	C_L = 25 pF, R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	8	16	20	ns

functional block diagram



schematic

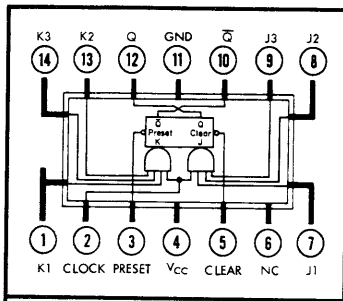


logic

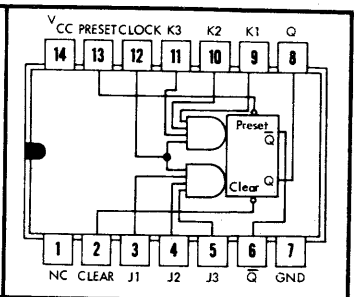
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = Bit time before clock pulse
4. t_{n+1} = Bit time after clock pulse
5. NC—No Internal Connection

W
FLAT PACKAGE (TOP VIEW)



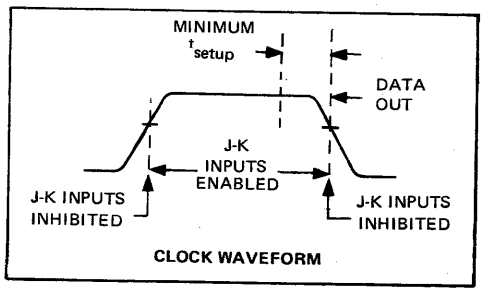
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These monolithic J-K flip-flops are negative edge-triggered. They feature gated J-K inputs and an asynchronous clear input. The AND gate inputs are inhibited while the clock input is low; when the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H102 Circuits	4.5	5	5.5	V
SN74H102 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H102 Circuits	−55	25	125	°C
SN74H102 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	15			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)	15			ns
Input Setup Time, t_{setup} (See Above): Logical 1	10			ns
Logical 0	13			ns
Input Hold Time, t_{hold}	0			ns
Clock Pulse Transition Time, t_0 (See Figure 77)			150	ns

7

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	59 and 60		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	59 and 60				0.8	V
$V_{out(1)}$	Logical 1 output voltage	59	V_{CC} = MIN, I_{load} = −500 μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	60	V_{CC} = MIN, I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, K3, preset, or clear	61	V_{CC} = MAX, V_{in} = 0.4 V		−1	−2	mA
$I_{in(0)}$	Logical 0 level input current clock	61	V_{CC} = MAX, V_{in} = 0.4 V		−3	−4.8	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	62	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	62	V_{CC} = MAX, V_{in} = 2.4 V	0		−1	mA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	62	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	63	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	62	V_{CC} = MAX		20	38	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

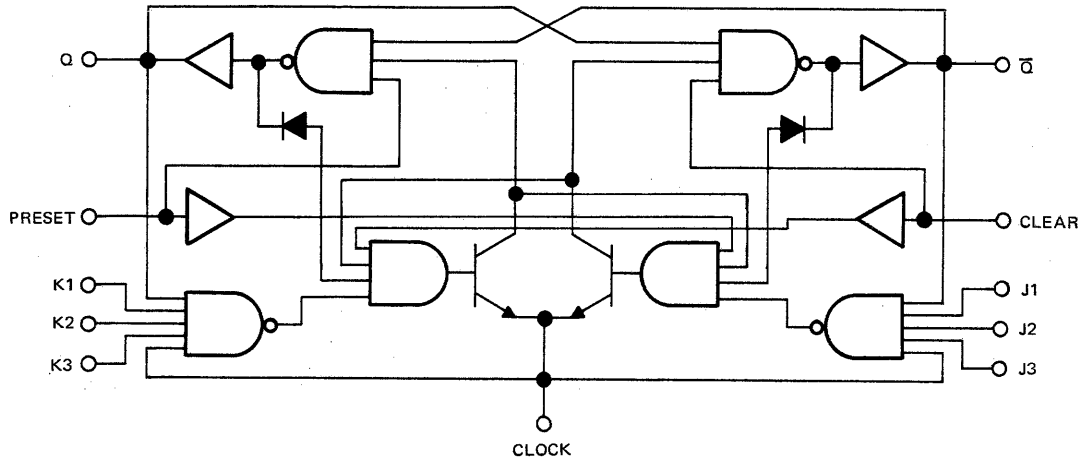
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

7

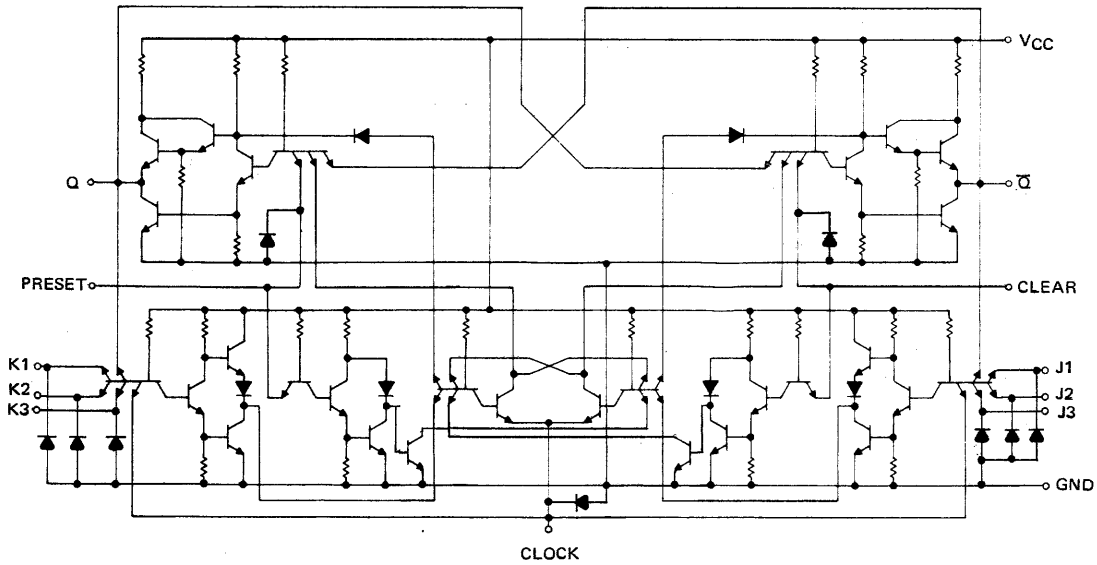
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	77	C_L = 25 pF, R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset to output	78	C_L = 25 pF, R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output (clock low)	78	C_L = 25 pF, R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output (clock high)	78	C_L = 25 pF, R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	8	16	20	ns

functional block diagram



schematic



CIRCUIT TYPES SN54H103, SN74H103
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

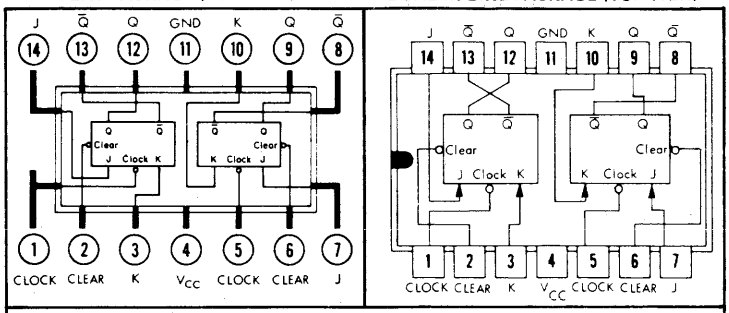
logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse
2. t_{n+1} = Bit time after clock pulse

W
FLAT PACKAGE (TOP VIEW)

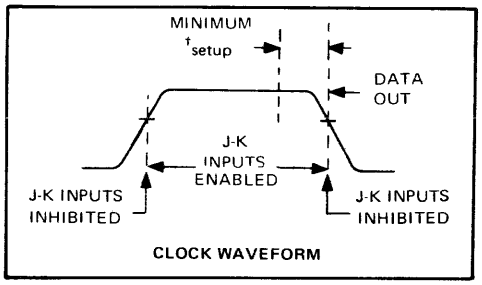
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to clear sets Q to logical 0
Clear is independent of clock

description

These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, clock, and asynchronous clear inputs to each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H103 Circuits	4.5	5	5.5	V
SN74H103 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H103 Circuits	−55	25	125	°C
SN74H103 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	10			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See Figure 79): Logical 1	10			ns
Logical 0	13			ns
Input Hold Time, t_{hold}	0			ns
Clock Pulse Transition Time, t_0 (See Figure 77)			150	ns

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65				0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN, I_{load} = −500 μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN, I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or clear	66	V_{CC} = MAX, V_{in} = 0.4 V		−1	−2	mA
$I_{in(0)}$	Logical 0 level input current at clock	66	V_{CC} = MAX, V_{in} = 0.4 V		−3	−4.8	mA
$I_{in(1)}$	Logical 1 level input current at J or K	67	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	67	V_{CC} = MAX, V_{in} = 2.4 V	0		−1	mA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	67	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	68	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX		40	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

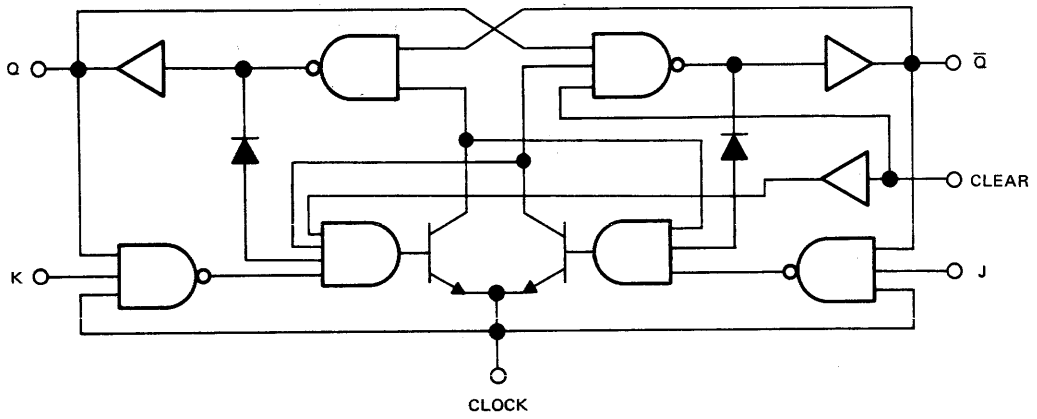
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

7

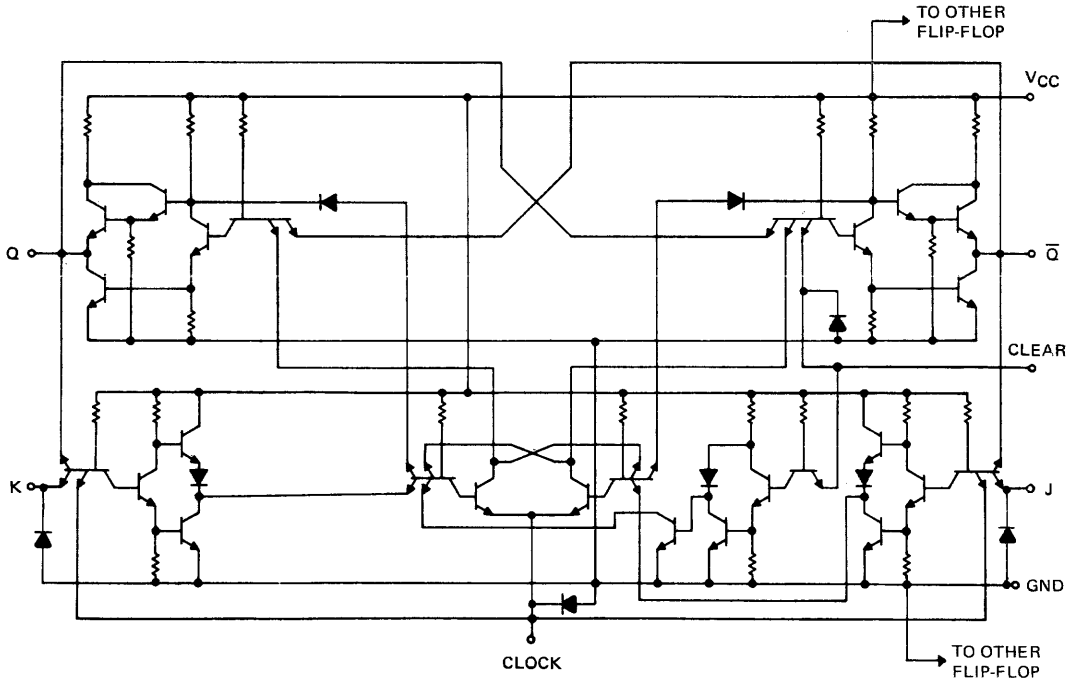
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	77	C_L = 25 pF, R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	78	C_L = 25 pF, R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output (Clock low)	78	C_L = 25 pF, R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output (clock high)	78	C_L = 25 pF, R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	8	16	20	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)

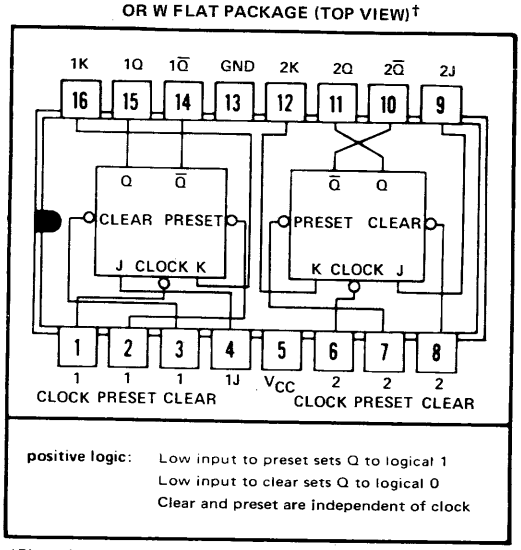


logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse
2. t_{n+1} = Bit time after clock pulse

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†

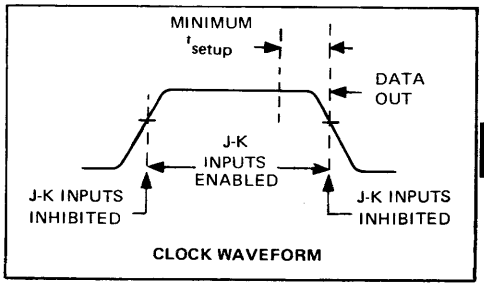


positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Clear and preset are independent of clock

†Pin assignments for these circuits are the same for all packages.

description

These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H106 Circuits	4.5	5	5.5	V
SN74H106 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H106 Circuits	−55	25	125	°C
SN74H106 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See Above): Logical 1	10			ns
Logical 0	13			ns
Input Hold Time, t_{hold}	0			ns
Clock Pulse Transition Time, t_0 (See Figure 77)			150	ns

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65				0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN, I_{load} = −500 μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN, I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, preset, or clear	66	V_{CC} = MAX, V_{in} = 0.4 V		−1	−2	mA
$I_{in(0)}$	Logical 0 level input current at clock	66	V_{CC} = MAX, V_{in} = 0.4 V		−3	−4.8	mA
$I_{in(1)}$	Logical 1 level input current at J or K	67	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	67	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	67	V_{CC} = MAX, V_{in} = 2.4 V	0		−1	mA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	69	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX		40	76	mA

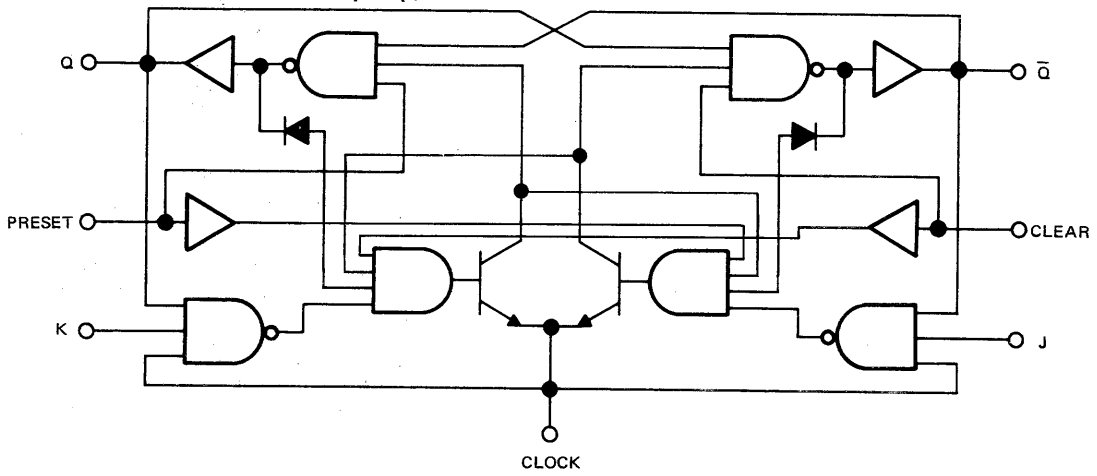
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

7

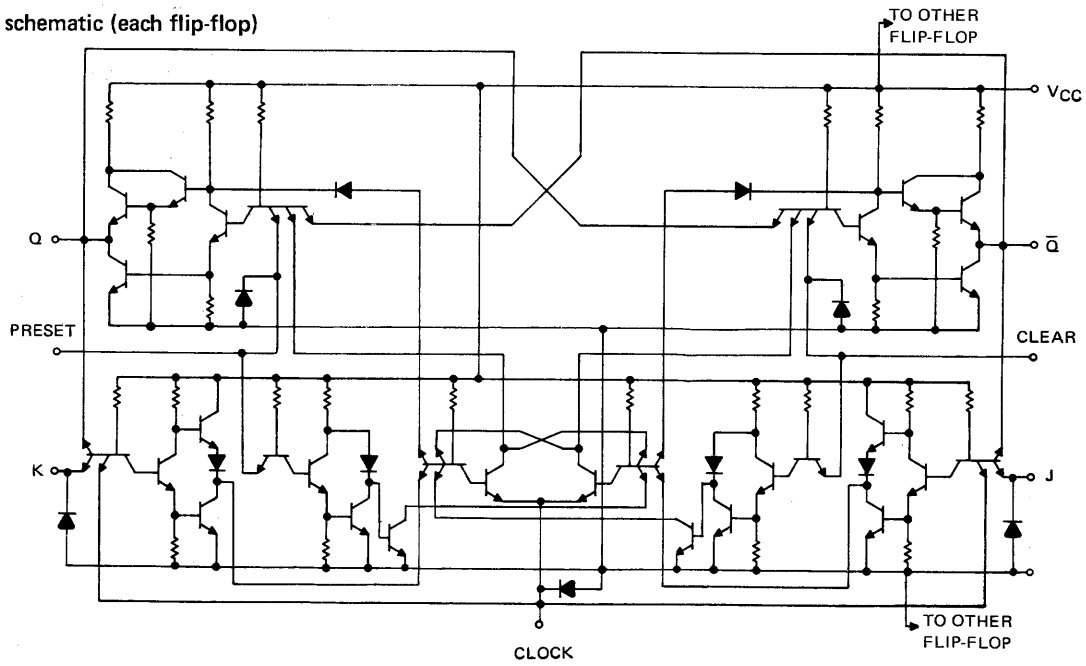
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	77	C_L = 25 pF, R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset or clear to output	78	C_L = 25 pF, R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output (clock low)	78	C_L = 25 pF, R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output (clock high)	78	C_L = 25 pF, R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	8	16	20	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



7

CIRCUIT TYPES SN54H108, SN74H108
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

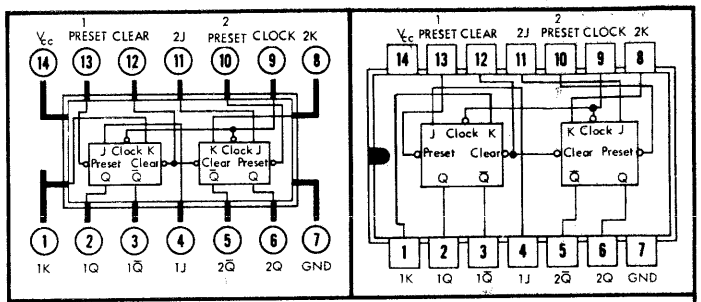
logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse
2. t_{n+1} = Bit time after clock pulse

W
FLAT PACKAGE (TOP VIEW)

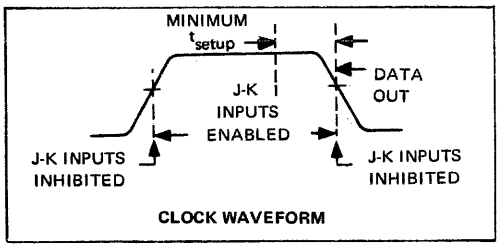
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, and asynchronous preset inputs to each flip-flop as well as common clock and asynchronous clear inputs. When the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H108 Circuits	4.5	5	5.5	V
SN74H108 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H108 Circuits	−55	25	125	°C
SN74H108 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	15			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See above): Logical 1	10			ns
Logical 0	13			ns
Input Hold Time, t_{hold}	0			ns
Clock Pulse Transition Time, t_0 (See Figure 77)			150	ns

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65				0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN, I_{load} = −500 μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN, I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or preset	66	V_{CC} = MAX, V_{in} = 0.4 V		−1	−2	mA
$I_{in(0)}$	Logical 0 level input current at clock	66	V_{CC} = MAX, V_{in} = 0.4 V		−6	−9.6	mA
$I_{in(0)}$	Logical 0 level input current at clear	66	V_{CC} = MAX, V_{in} = 0.4 V		−2	−4	mA
$I_{in(1)}$	Logical 1 level input current at J or K	67	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	67	V_{CC} = MAX, V_{in} = 2.4 V	0		−1	mA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset	67	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	67	V_{CC} = MAX, V_{in} = 2.4 V			200	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	69	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX		40	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

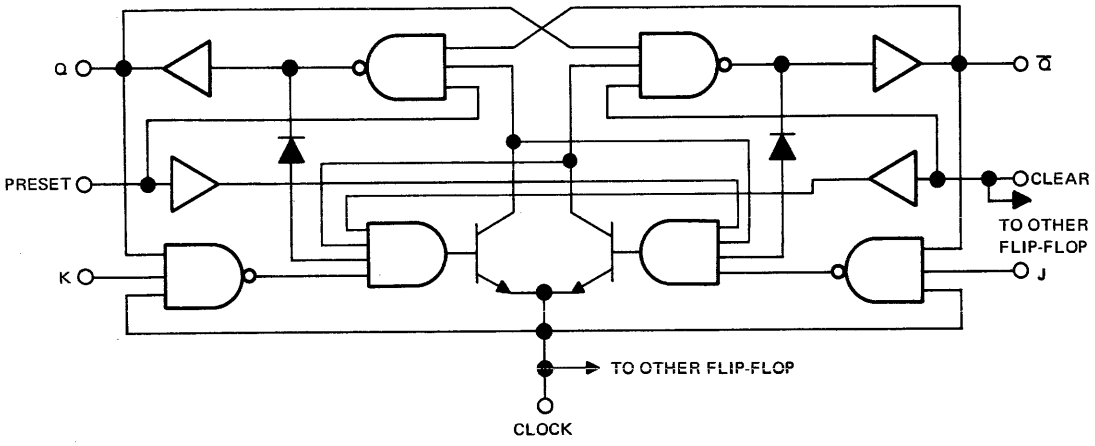
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

7

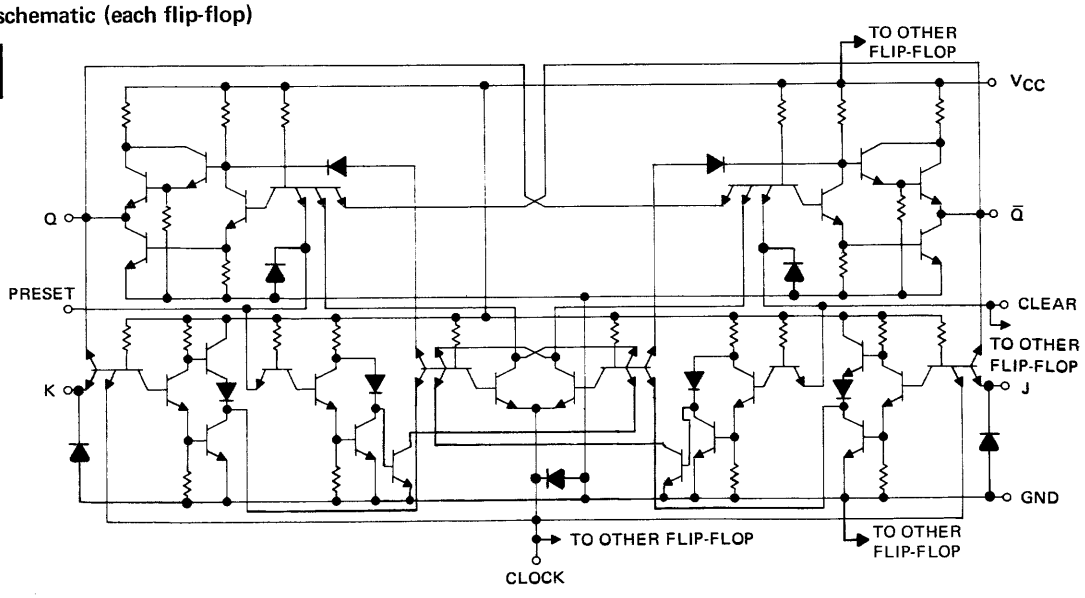
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	77	C_L = 25 pF, R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset or clear to output	78	C_L = 25 pF, R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output output (clock low)	78	C_L = 25 pF, R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output output (clock high)	78	C_L = 25 pF, R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	8	16	20	ns

functional block diagram (each flip-flop)

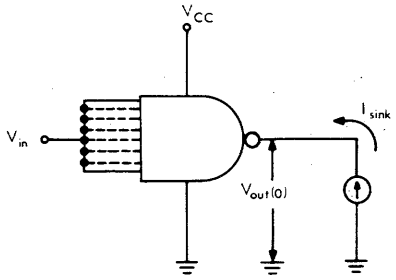


schematic (each flip-flop)



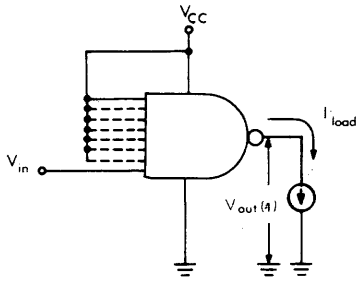
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



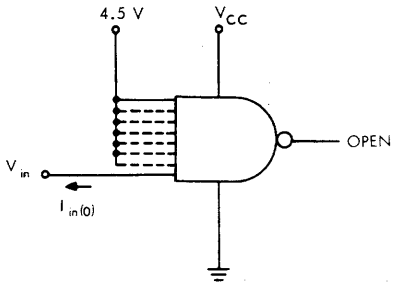
1. All inputs are tested simultaneously.

FIGURE 1



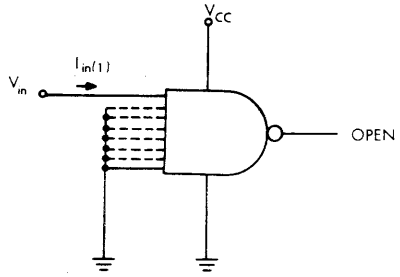
1. Each input is tested separately.

FIGURE 2



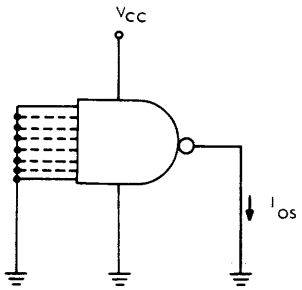
1. Each input is tested separately.

FIGURE 3



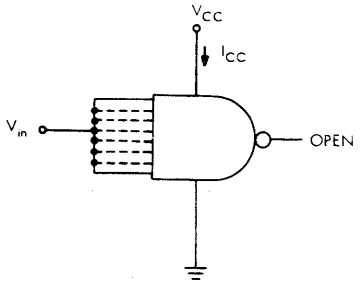
1. Each input is tested separately.

FIGURE 4



1. Each gate is tested separately.

FIGURE 5



1. Logical 0 and logical 1 conditions are tested.
2. All gates are tested simultaneously.

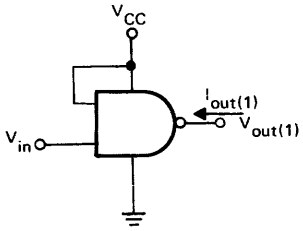
FIGURE 6

§Arrows indicate actual direction of current flow.

7

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each input is tested separately.

FIGURE 7

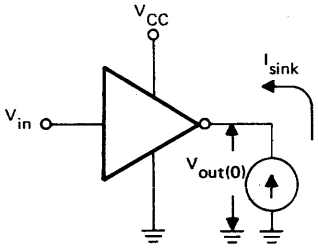


FIGURE 8

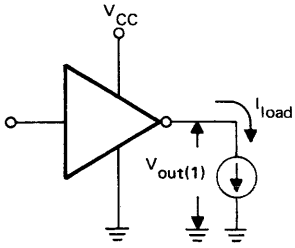


FIGURE 9

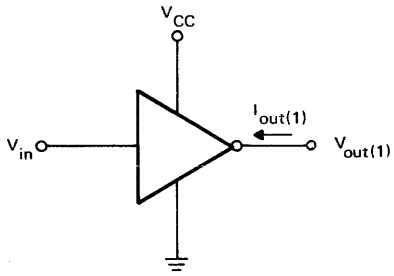


FIGURE 10

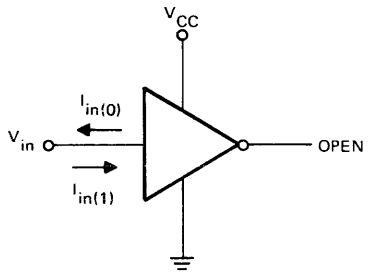
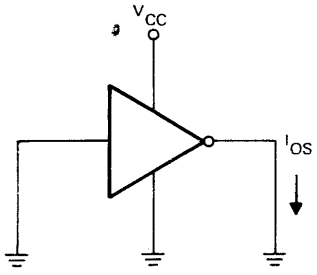
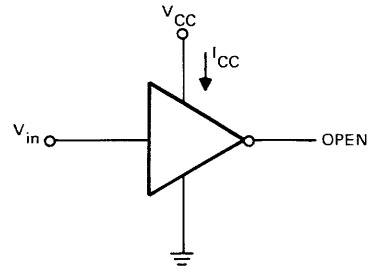


FIGURE 11



1. Each inverter is tested separately.

FIGURE 12



1. All inverters are tested simultaneously.

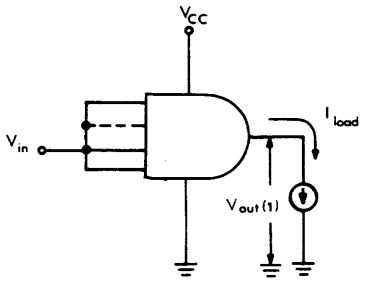
FIGURE 13

§Arrows indicate actual direction of current flow.

7

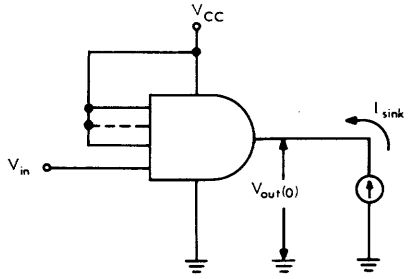
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



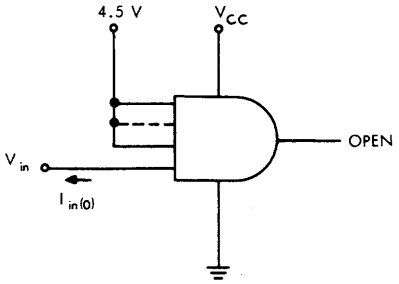
1. All inputs are tested simultaneously.

FIGURE 14



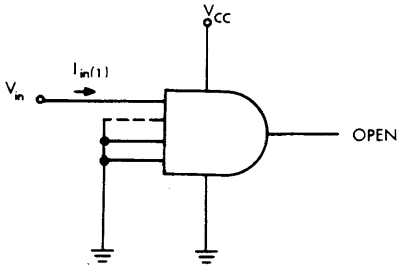
1. Each input is tested separately.

FIGURE 15



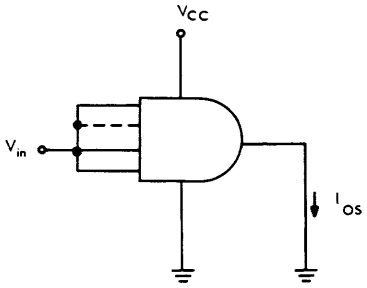
1. Each input is tested separately.

FIGURE 16



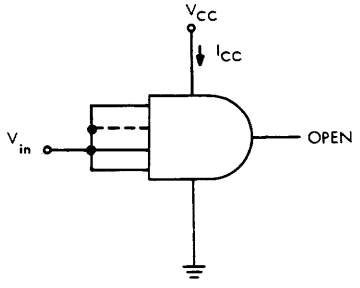
1. Each input is tested separately.

FIGURE 17



1. Each gate is tested separately.

FIGURE 18



1. Logical 0 and logical 1 conditions are tested.
2. All gates are tested simultaneously.

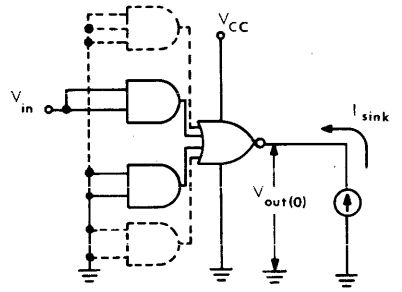
FIGURE 19

§Arrows indicate actual direction of current flow.

7

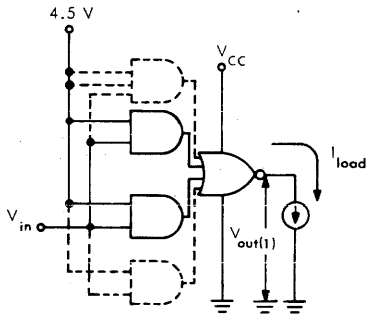
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



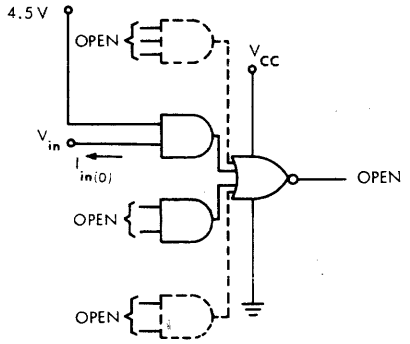
1. Each AND section is tested separately.

FIGURE 20



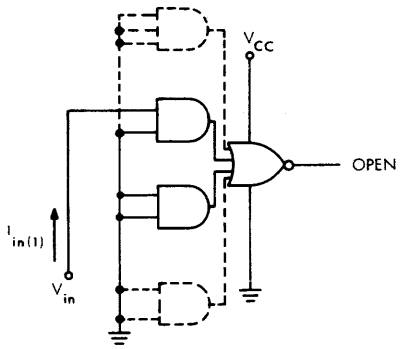
1. Each set of inputs is tested separately.

FIGURE 21



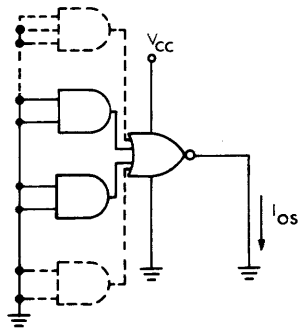
1. Each input is tested separately.

FIGURE 22



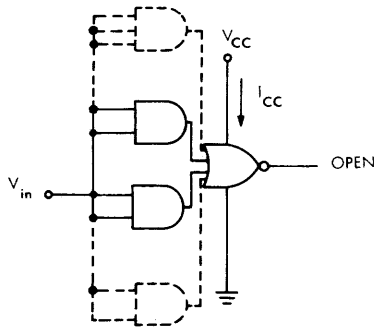
1. Each input is tested separately.

FIGURE 23



1. Each gate is tested separately.

FIGURE 24.



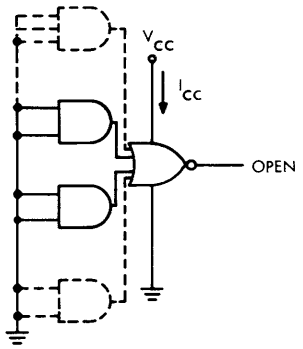
1. All gates are tested simultaneously

FIGURE 25

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. All gates are tested simultaneously.

FIGURE 26

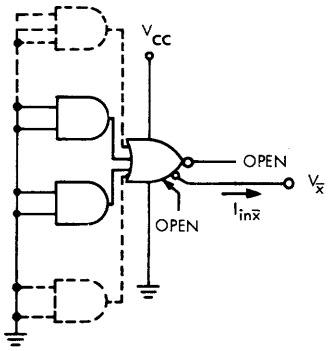


FIGURE 27

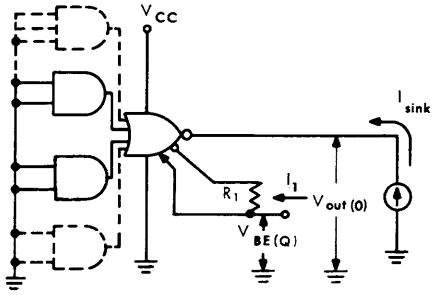


FIGURE 28

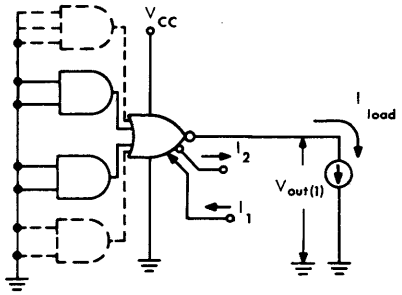
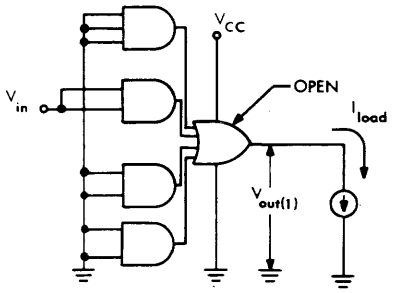
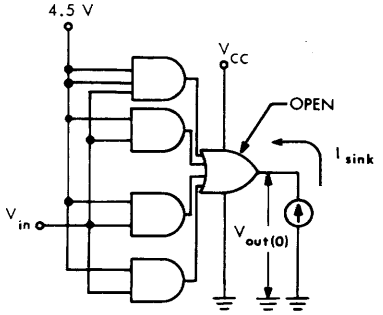


FIGURE 29



1. Each AND section is tested separately.

FIGURE 30



1. Each set of inputs is tested separately.

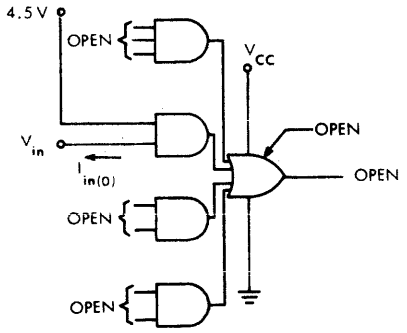
FIGURE 31

§Arrows indicate actual direction of current flow.

7

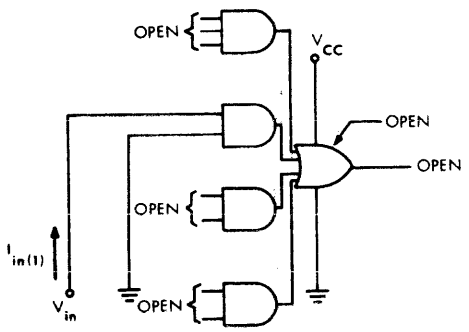
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each input of each AND section is tested separately.

FIGURE 32



1. Each input of each AND section is tested separately.

FIGURE 33

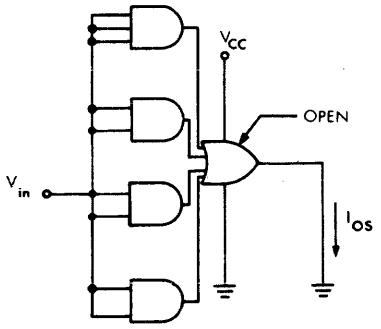
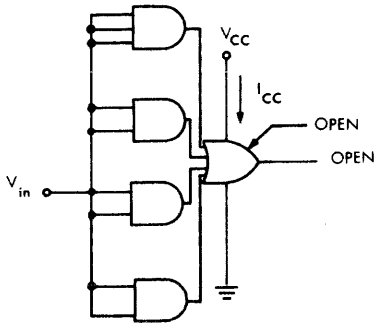


FIGURE 34



1. Logical 0 and logical 1 conditions are tested.

FIGURE 35

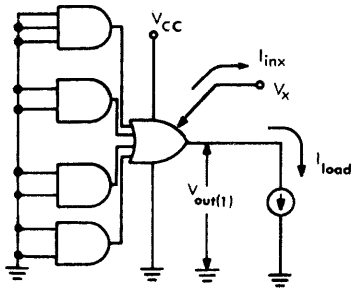


FIGURE 36

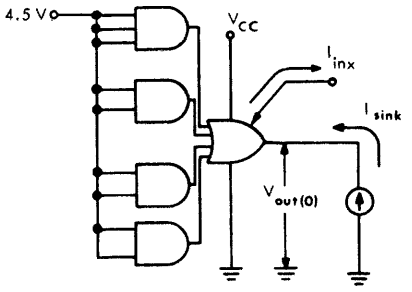
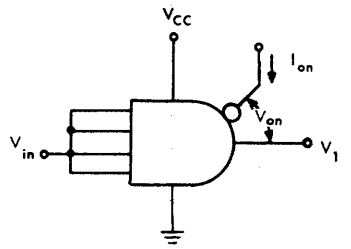


FIGURE 37

§Arrows indicate actual direction of current flow.

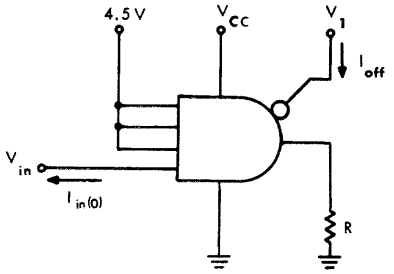
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. All inputs are tested simultaneously.

FIGURE 38



1. Each input is tested separately.

FIGURE 39

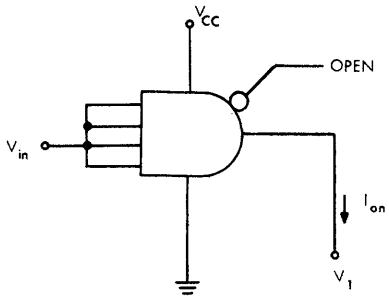
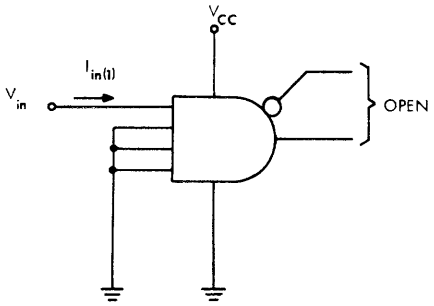
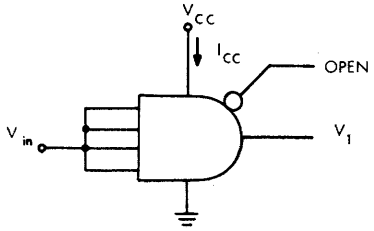


FIGURE 40



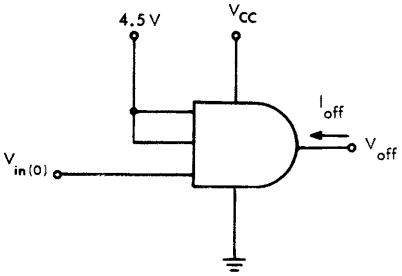
1. Each input is tested separately.

FIGURE 41



1. On and off conditions are tested separately.
2. All gates are tested simultaneously.

FIGURE 42



1. Each input is tested separately.

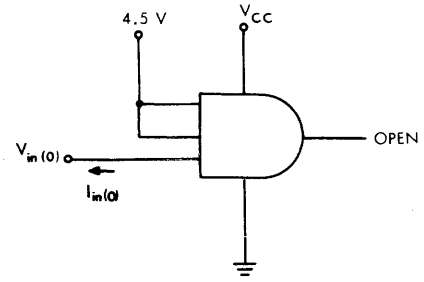
FIGURE 43

§Arrows indicate actual direction of current flow.

7

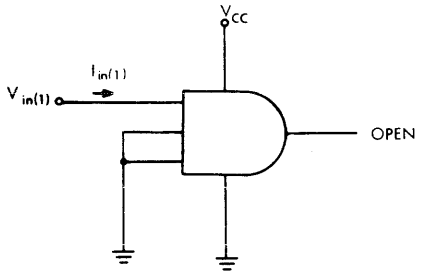
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



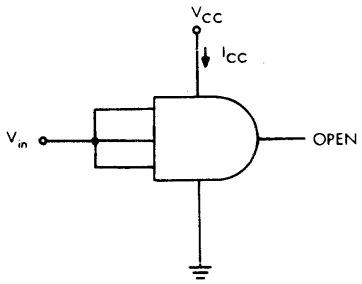
1. Each input is tested separately.

FIGURE 44



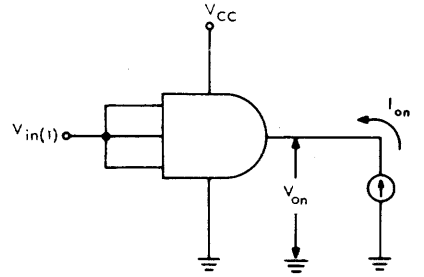
1. Each input is tested separately.

FIGURE 45



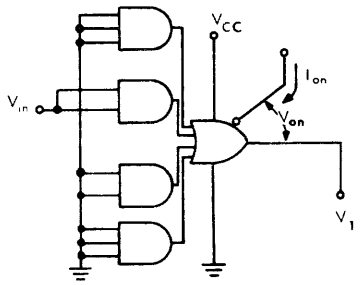
1. On and off conditions are tested separately.
2. All gates are tested simultaneously.

FIGURE 46



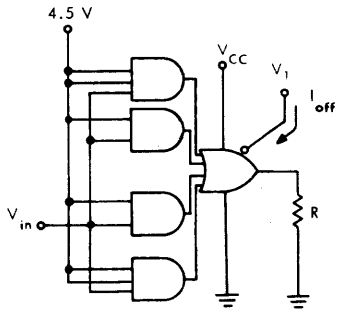
1. All inputs are tested simultaneously.

FIGURE 47



1. Each AND section is tested separately.

FIGURE 48



1. Each set of inputs is tested separately.

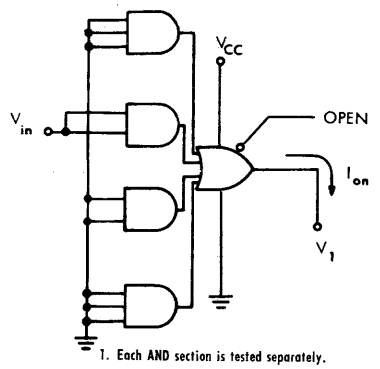
FIGURE 49

§Arrows indicate actual direction of current flow.

7

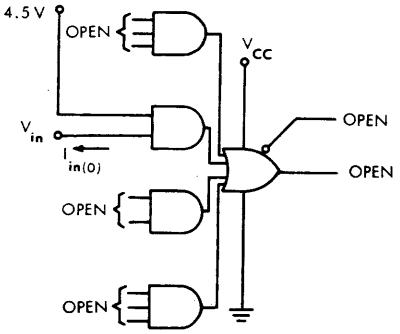
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



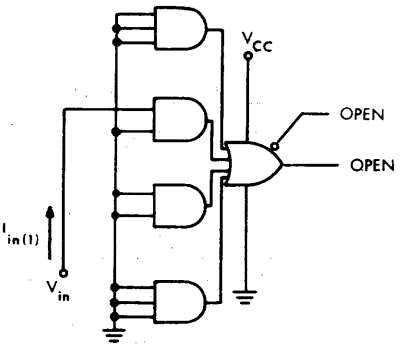
1. Each AND section is tested separately.

FIGURE 50



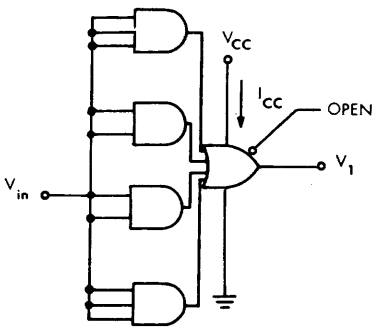
1. Each input is tested separately.

FIGURE 51



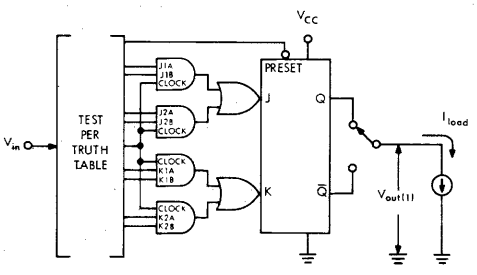
1. Each input is tested separately.

FIGURE 52



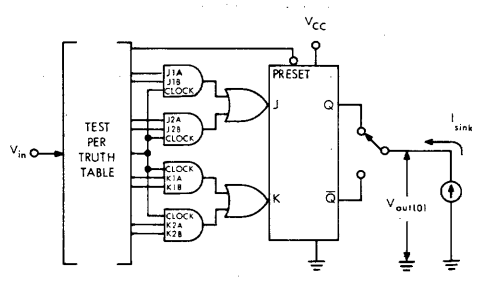
1. On and off conditions are tested separately.

FIGURE 53



1. Each output is tested separately.

FIGURE 54



1. Each output is tested separately.

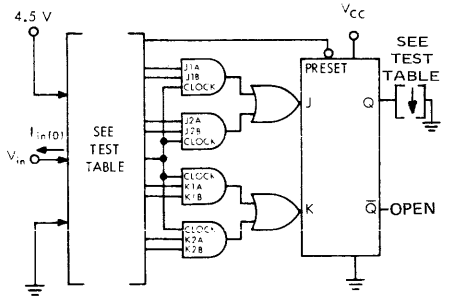
FIGURE 55

§Arrows indicate actual direction of current flow.

7

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each input is tested separately.

TEST TABLES†

SN54H71, SN74H71

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	Apply Momentary GND then 4.5 V	GND
Clock	J1A, J1B, J2A, J2B, K1A, K1B, K2A, and K2B	Preset	None
Clock¶	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, and Preset	None	Q
Preset	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, and Clock	None	None
J1A¶	J1B and Clock	None	Q
J1B¶	J1A and Clock	None	Q
J2A¶	J2B and Clock	None	Q
J2B¶	J2A and Clock	None	Q
K1A	K1B and Clock	Preset	None
K1B	K1A and Clock	Preset	None
K2A	K2B and Clock	Preset	None
K2B	K2A and Clock	Preset	None

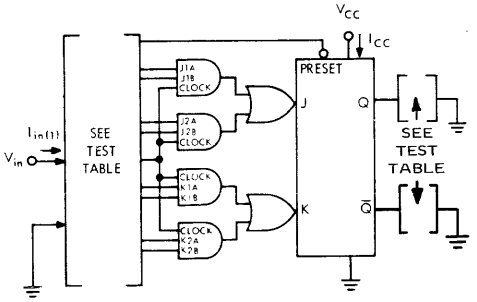
†Inputs and outputs not specified are open.
¶Duration of this test should not exceed 1 second.

SN54H101, SN74H101

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	Ground
Clock	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B	Preset
Preset	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, Clock	None
J1A¶	J1B, J2A, J2B, K1A, K1B, K2A, K2B, Clock, Preset	Q
J1B¶	J1A, J2A, J2B, K1A, K1B, K2A, K2B, Clock, Preset	Q
J2A¶	J1A, J1B, J2B, K1A, K1B, K2A, K2B, Clock, Preset	Q
J2B¶	J1A, J1B, J2A, K1A, K1B, K2A, K2B, Clock, Preset	Q
K1A	J1A, J1B, J2A, J2B, K1B, K2A, K2B, Clock	Preset
K1B	J1A, J1B, J2A, J2B, K1A, K2A, K2B, Clock	Preset
K2A	J1A, J1B, J2A, J2B, K1A, K1B, K2B, Clock	Preset
K2B	J1A, J1B, J2A, J2B, K1A, K1B, K2A, Clock	Preset

†Inputs and outputs not specified are open.
¶Duration of this test should not exceed 1 second.

FIGURE 56



1. Each input is tested separately.
2. I_{CC} is measured for each of the following conditions:
   a. J1A = J1B = J2A = J2B = K1A = K1B = K2A = K2B = Preset = 4.5 V, and Clock = momentary 4.5 V, then Gnd.

TEST TABLES†

SN54H71, SN74H71

Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, and Preset
Clock¶	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, Preset, and Q
Preset	K1A, K1B, K2A K2B, Clock, and Q
J1A	J1B, Clock, and Preset
J1B	J1A, Clock, and Preset
J2A	J2B, Clock, and Preset
J2B	J2A, Clock, and Preset
K1A¶	K1B, Clock, Preset, and Q
K1B¶	K1A, Clock, Preset, and Q
K2A¶	K2B, Clock, Preset, and Q
K2B¶	K2A, Clock, Preset, and Q

†Inputs and outputs not specified are open.
¶Duration of this test should not exceed one second.

SN54H101, SN74H101

Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply 4.5 V
Clock	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, Preset	None
Preset¶	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, $\overline{Q}$	Clock
J1A,	J1B, J2A, J2B, Preset, Clock	K1A, K1B, K2A, K2B
J1B	J1A, J2A, J2B, Preset, Clock	K1A, K1B, K2A, K2B
J2A	J1A, J1B, J2B, Preset, Clock	K1A, K1B, K2A, K2B
J2B	J1A, J1B, J2A, Preset, Clock	K1A, K1B, K2A, K2B
K1A	K1B, K2A, K2B, Clock	Preset J1A, J1B, J2A, J2B
K1B	K1A, K2A, K2B, Clock	Preset J1A, J1B, J2A, J2B
K2A	K1A, K1B, K2B, Clock	Preset J1A, J1B, J2A, J2B
K2B	K1A, K1B, K2A, Clock	Preset J1A, J1B, J2A, J2B

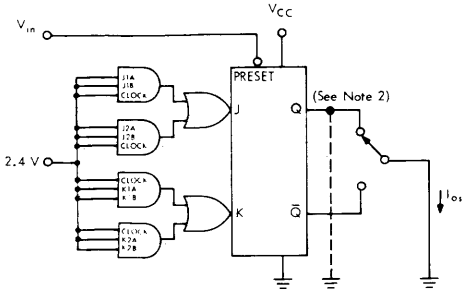
†Inputs and outputs not specified are open.
¶Duration of this test should not exceed 1 second.

FIGURE 57

§Arrows indicate actual direction of current flow.

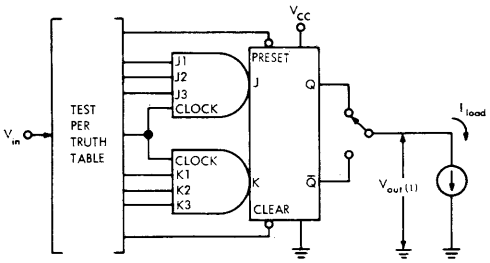
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



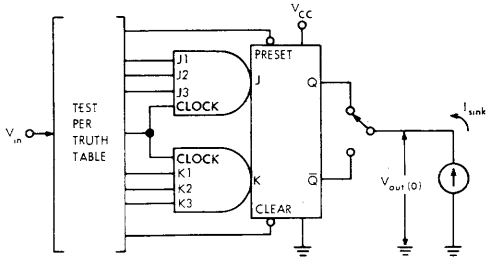
1. Each output is tested separately.
2. Test circuit shows setup for testing Q. When testing $\bar{Q}$, apply 2.4 V to Preset, ground Q, and limit duration of test to 100 ms.

FIGURE 58



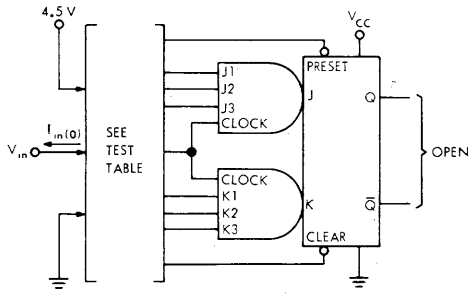
1. Each output is tested separately.

FIGURE 59



1. Each output is tested separately.

FIGURE 60



1. Each input is tested separately.

TEST TABLES

SN54H72, SN74H72

Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND, then 4.5 V	Apply 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

SN54H102, SN74H102

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	Ground
Clock	J1, J2, J3, K1, K2, K3, Clear	Preset
Clock	J1, J2, J3, K1, K2, K3, Preset	Clear
Preset	J1, J2, J3, K1, K2, K3, Clock, Clear	None
Clear	J1, J2, J3, K1, K2, K3, Clock, Preset	None
J1	J2, J3, K1, K2, K3, Clock, Preset	Clear
J2	J1, J3, K1, K2, K3, Clock, Preset	Clear
J3	J1, J2, K1, K2, K3, Clock, Preset	Clear
K1	J1, J2, J3, K2, K3, Clock, Clear	Preset
K2	J1, J2, J3, K1, K3, Clock, Clear	Preset
K3	J1, J2, J3, K1, K2, Clock, Clear	Preset

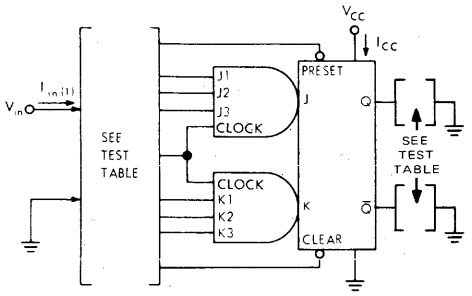
FIGURE 61

§ Arrows indicate actual direction of current flow.

7

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each input is tested separately.
2. I_{CC} is measured for each of the following conditions:
   a. J1 = J2 = J3 = K1 = K2 = K3 = Clock = Preset = Gnd.
   b. J1 = J2 = J3 = K1 = K2 = K3 = Clock = Clear = Gnd.

TEST TABLES

SN54H72, SN74H72

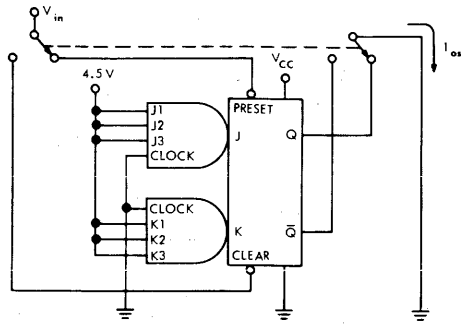
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2,and K3
Clear	Clock,J1, J2, and J3
J1	Clock, Clear, J2,and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

SN54H102, SN74H102

Apply V_{in} (Test $I_{in(1)}$)	Ground	4.5 V
Clock	J1, J2, J3, K1, K2, K3, Preset	Clear
Clock	J1, J2, J3, K1, K2, K3, Clear	Preset
Preset ¶	J1, J2, J3, K1, K2, K3, $\bar{Q}$	Clock, Clear
Clear ¶	J1, J2, J3, K1, K2, K3, Q	Clock, Preset
J1	J2, J3, Clock, Preset	K1, K2, K3, Clear
J2	J1, J3, Clock, Preset	K1, K2, K3, Clear
J3	J1, J2, Clock, Preset	K1, K2, K3, Clear
K1	K2, K3, Clock, Clear	J1, J2, J3, Preset
K2	K1, K3, Clock, Clear	J1, J2, J3, Preset
K3	K1, K2, Clock, Clear	J1, J2, J3, Preset

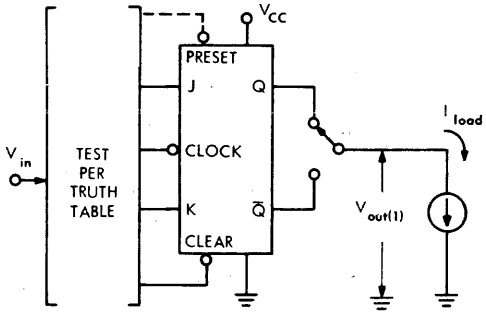
¶ Duration of this test should not exceed 1 second.

FIGURE 62



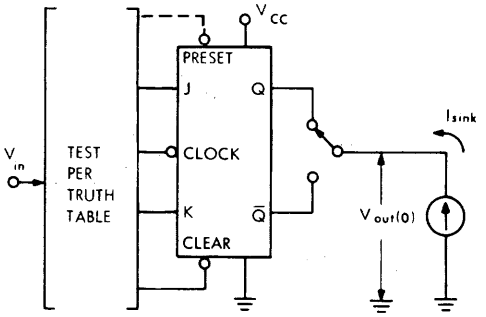
1. Each output is tested separately.

FIGURE 63



1. Each flip-flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for SN54H78/SN74H78 circuits only.

FIGURE 64



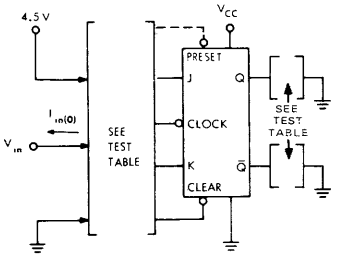
1. Each flip-flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for SN54H78/SN74H78 circuits only.

FIGURE 65

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



TEST TABLES
SN54H73, SN74H73
SN54H76, SN74H76, SN54H78, SN74H78

Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
Preset	None (See Note 5)	Clock and K
J	Q (See Note 3)	Clock and Clear
K	$\overline{Q}$ (See Note 3)	Clock and Clear

SN54H103, SN74H103

APPLY V_{in} TEST $I_{in(0)}$	APPLY GND	APPLY 4.5 V
Clock	Clear	J, K
Clear	None	Clock, J, K
J	Clear	Clock, K
K¶	$\overline{Q}$	Clock, Clear, J

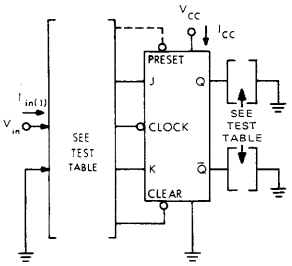
¶ Duration of this test should not exceed 1 second.

SN54H106, SN74H106
SN54H108, SN74H108

APPLY V_{in} TEST $I_{in(0)}$	APPLY GND	APPLY 4.5 V
Clock	Clear	J, K, Preset Note 6
Clock	Preset	J, K, Clear Note 6
Clear	None	Clock, Preset, J, K Note 6
Preset	None	Clock, Clear, J, K
J	Clear	Clock, K Preset
K	Preset	Clock, Clear, J

1. Each flip-flop is tested separately.
2. Apply momentary ground, then 4.5 V.
3. After application of momentary ground (< 1 second), Q and $\overline{Q}$ are left floating.
4. Ground all inputs of the unused flip-flop except where Note 6 is referenced.
5. Preset is not applicable for SN54H73 and SN74H73.
6. Apply the same conditions simultaneously to both flip-flops when testing the SN54H108 and SN74H108.

FIGURE 66



TEST TABLES
SN54H73, SN74H73
SN54H76, SN74H76, SN54H78, SN74H78

Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
Preset (See Note 1)	Clock and K	None
J (See Note 1)	Clock and Clear	Preset
K (See Note 1)	Clock and Preset	Clear

SN54H103, SN74H103

APPLY V_{in} TEST $I_{in(1)}$	APPLY GND	APPLY 4.5 V
Clock	Clear, J, K	None
Clear¶	Q, J, K	Clock
J	Clock	Clear, K
K	Clock, Clear	J

SN54H106, SN74H106
SN54H108, SN74H108

APPLY V_{in} TEST $I_{in(1)}$	APPLY GND	APPLY 4.5 V
Clock	Clear, J, K	Preset, Note 4
Clock	Preset, J, K	Clear Note 4
Clear¶	Q, J, K	Preset, Clock Note 4
Preset¶	$\overline{Q}$, J, K	Clear, Clock
J	Clock, Preset	Clear, K
K	Clock, Clear	Preset, J

¶ Duration of this test should not exceed 1 second.

1. Preset is not applicable to SN54H73, SN74H73, SN54H103, SN74H103.
2. I_{CC} is measured (simultaneously for both flip-flops) for the following conditions:
   a. J = K = Clock = Clear = Gnd.
      Preset (when applicable) = 4.5 V.
   b. For SN54H73, SN74H73, SN54H103, and SN74H103: J = Clear = 4.5 V, K = Gnd, and apply momentary 4.5 V, then Gnd, to Clock. For SN54H76, SN74H76, SN54H78, SN74H78, SN54H108, SN74H108: J = K = Clock = Preset = Gnd, and Clear = 4.5 V.
3. Each flip-flop is tested separately except where Note 4 is referenced.
4. Apply the same conditions to both flip-flops when testing the SN54H108 and SN74H108.

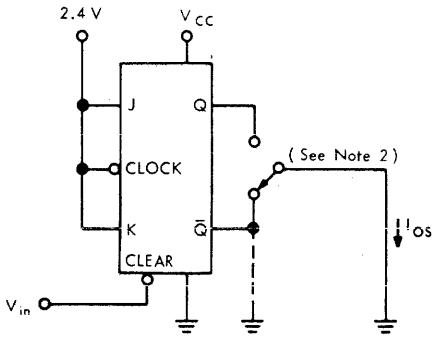
FIGURE 67

§ Arrows indicate actual direction of current flow.

7

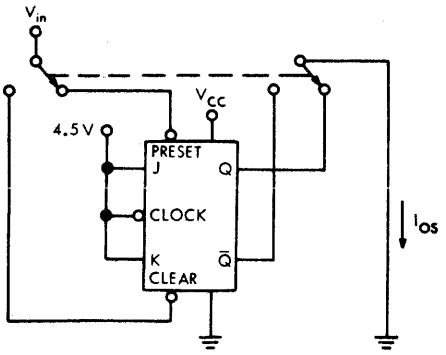
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each flip-flop is tested separately.
2. Test circuit shows setup for testing $\overline{Q}$. When testing Q, apply 4.5 V to Clear, ground $\overline{Q}$, and limit duration of test to 100 ms.

FIGURE 68



1. Each flip-flop is tested separately.

FIGURE 69

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

TEST TABLE

APPLY V_{in} (TEST $I_{in(1)}$)	CONDITIONS ON OTHER INPUTS AND OUTPUTS			
	4.5 V	S1	2 V	GND
Clock	None	Open	All K inputs	All J inputs and Preset
Clock	Preset	Closed	All J inputs	All K inputs, and momentarily GND Q, then open

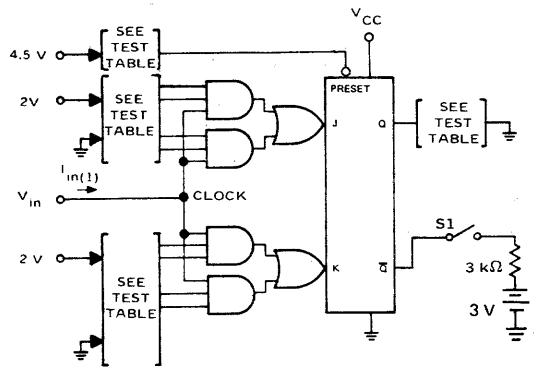


FIGURE 70

TEST TABLE

Apply V_{in} (TEST $I_{in(1)}$)	CONDITIONS ON OTHER INPUTS		
	4.5 V	2 V	GND
Clock	Clear	All K inputs	All J inputs and Preset
Clock	Preset	All J inputs	All K inputs and Clear

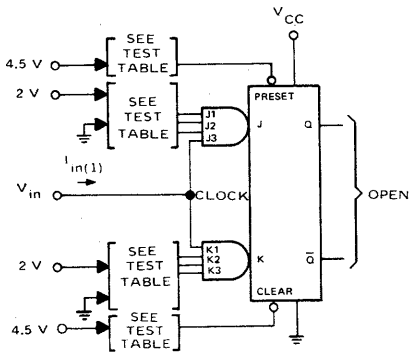


FIGURE 71

TEST TABLE

APPLY V_{in} (TEST $I_{in(1)}$)	CONDITIONS ON OTHER INPUTS AND OUTPUTS			
	4.5 V	S1	2 V	GND
Clock	None	Open	J	K and Clear
Clock	Clear	Closed	K	J, and momentarily GND A, then open

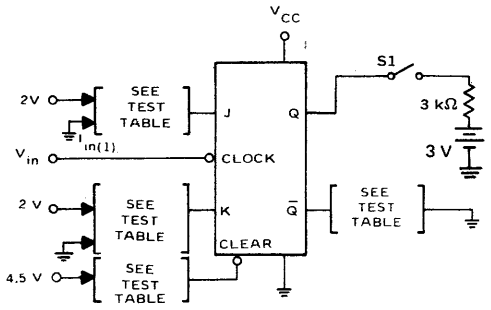


FIGURE 72

TEST TABLE

APPLY V_{in} (TEST $I_{in(1)}$)	CONDITIONS ON OTHER INPUTS		
	4.5 V	2 V	GND
Clock	Clear	K	J and Preset
Clock	Preset	J	K and Clear

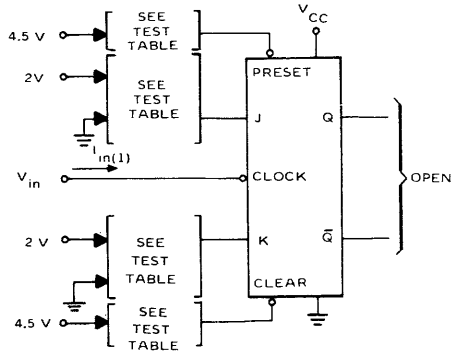


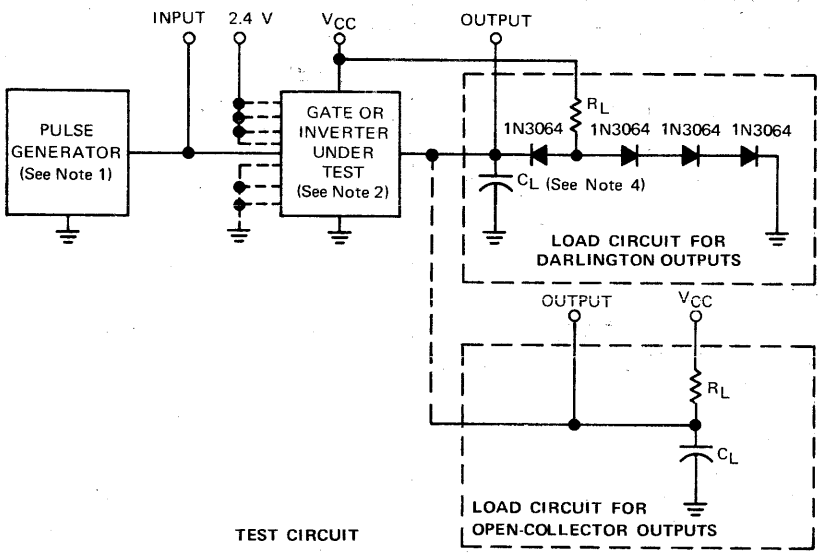
FIGURE 73

§Arrows indicate actual direction of current flow.

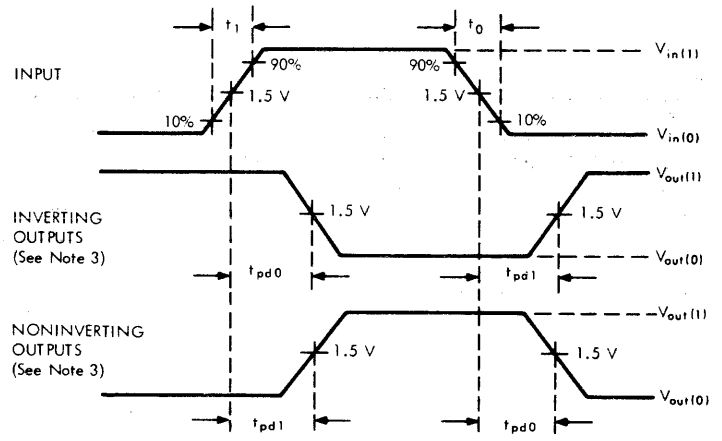
7

switching characteristics

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 7 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.

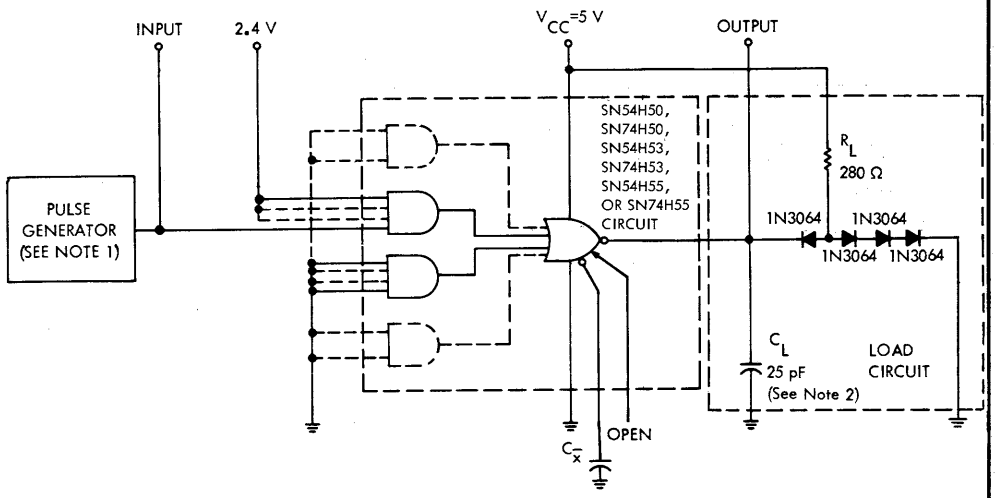
2. Input conditions are established for each gate as follows:
   a. Input pulse is applied to one input and 2.4 V is applied to all unused inputs of the SN54H00/SN74H00, SN54H01/SN74H01, SN54H04/SN74H04, SN54H05/SN74H05, SN54H10/SN74H10, SN54H11/SN74H11, SN54H20/SN74H20, SN54H21/SN74H21, SN54H22/SN74H22, SN54H30/SN74H30, or SN54H40/SN74H40 gate.
   b. Input pulse is applied to one input of one AND section, and 2.4 V is applied to all unused inputs of that AND section of the SN54H50/SN74H50, SN54H51/SN74H51, SN54H52/SN74H52, SN54H53/SN74H53, SN54H54/SN74H54, or SN54H55/SN74H55 gate. All inputs of all unused AND sections are grounded.
3. All gates are inverting except the SN54H11/SN74H11, SN54H21/SN74H21, and SN54H52/SN74H52 only.
4. C_L includes probe and jig capacitance.

FIGURE 74 – GATE PROPAGATION DELAY TIMES

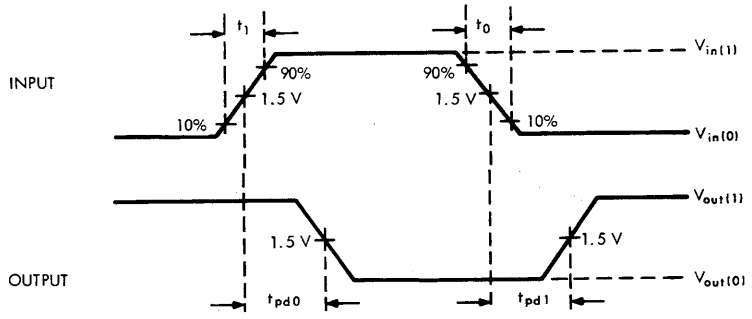
7

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

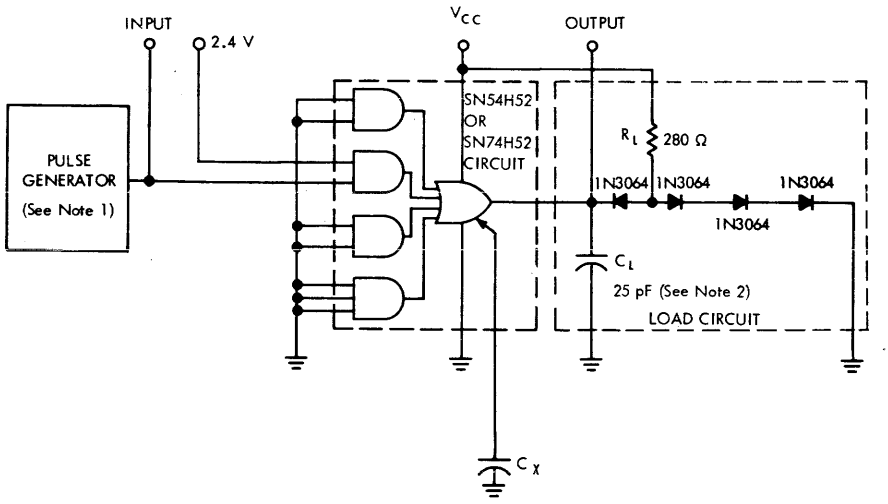
NOTES: 1. The generator has the following characteristics: $V_{in(1)} = 3$ V, $V_{in(0)} = 0$ V, $t_0 = t_1 = 7$ ns, duty cycle = 50%, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. C_x includes jig capacitance.

FIGURE 75 – SN54H50/SN74H50, SN54H53/SN74H53, SN54H55/SN74H55
PROPAGATION DELAY TIMES

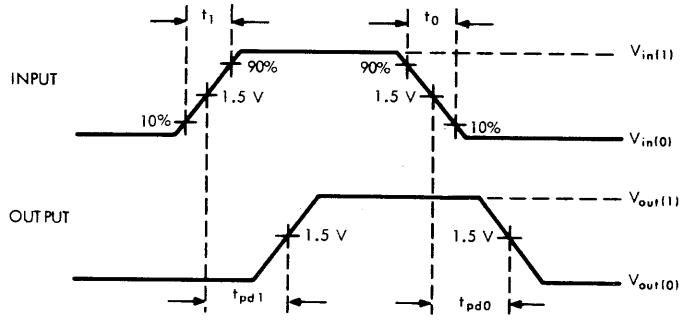
7

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

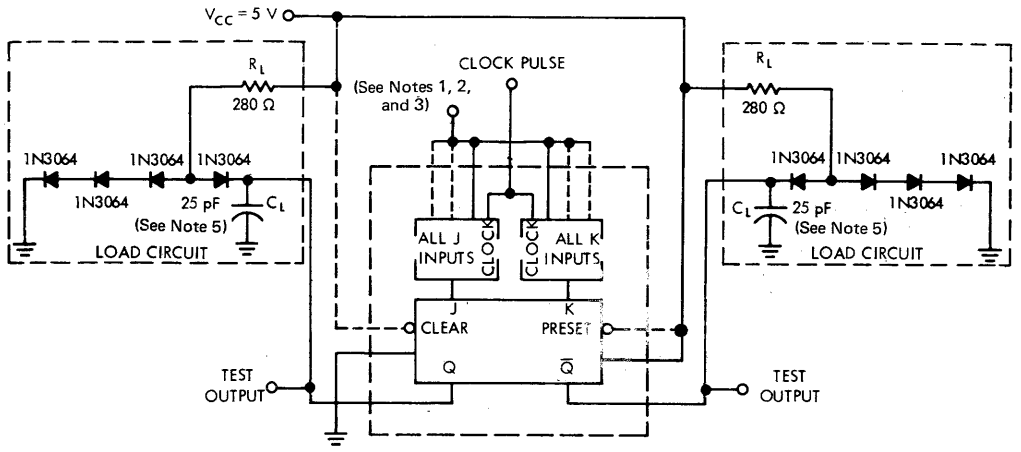
NOTES: 1. The generator has the following characteristics: $V_{in(1)} = 3$ V, $V_{in(0)} = 0$ V, $t_0 = t_1 = 7$ ns, duty cycle = 50%, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. C_X includes jig capacitance.

FIGURE 76 – SN54H52/SN74H52 PROPAGATION DELAY TIMES

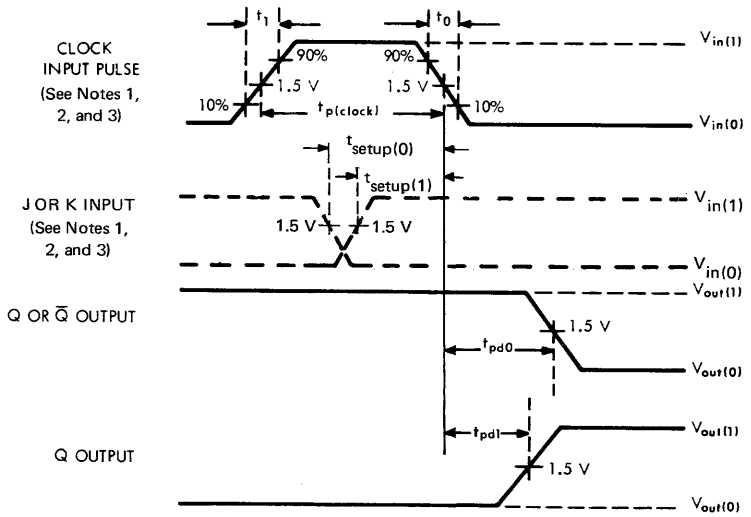
7

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. When testing t_{pd0} and t_{pd1} (all types), the clock input pulse characteristics are: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 7ns, $t_{p(clock)}$ = 20 ns, and PRR = 1 MHz. When testing SN54H71/SN74H71, SN54H72/SN74H72, SN54H73/SN74H73, SN54H76/SN74H76, and SN54H78/SN74H78, all J and K inputs are at 2.4 V. When testing SN54H101/SN74H101, SN54H102/SN74H102, SN54H103/ SN74H103, SN54H106/SN74H106, and SN54H108/SN74H108, conditions are established to ensure that minimum setup times are verified.

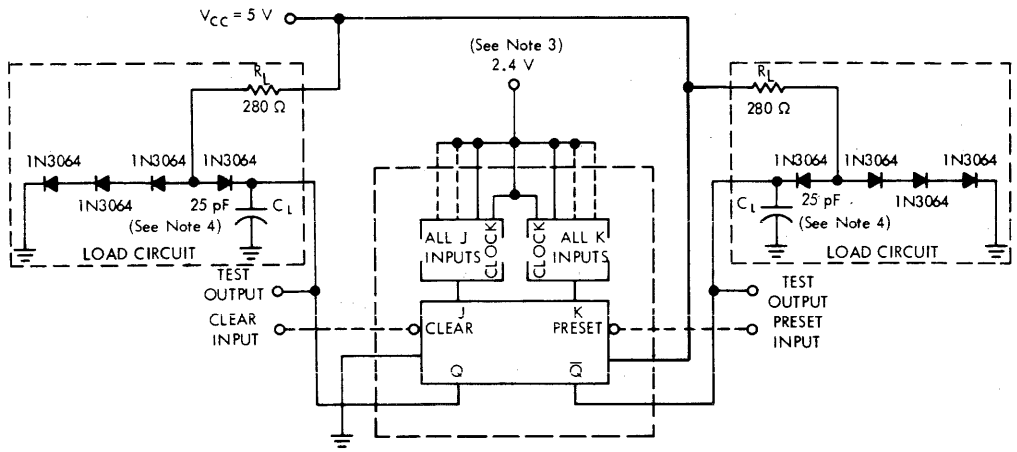
2. When testing f_{clock} of SN54H71/SN74H71, SN54H72/SN74H72, SN54H73/SN74H73, SN54H76/SN74H76, and SN54H78/SN74H78, the clock input characteristics are: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 3 ns, $t_{p(clock)}$ = 12 ns, and PRR = 25 MHz. All J and K inputs are at 2.4 V.
3. When testing f_{clock} of SN54H101/SN74H101, SN54H102/SN74H102, SN54H103/SN74H103, SN54H106/SN74H106, and SN54H108/SN74H108, the clock input characteristics are: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0, $t_1 = t_0$ = 3 ns, $t_{p(clock)}$ = 10 ns, and PRR = 40 MHz. All J and K inputs are at 2.4 V.
4. See applicable circuit type for actual J and K input configuration and presence of preset or clear functions.
5. C_L includes probe and jig capacitance.

FIGURE 77—FLIP-FLOP PROPAGATION DELAY TIMES

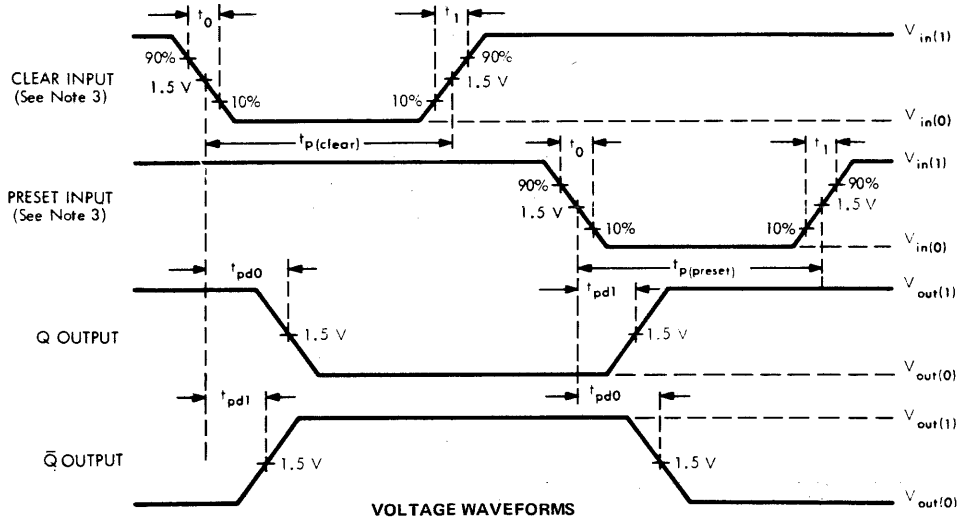
7

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



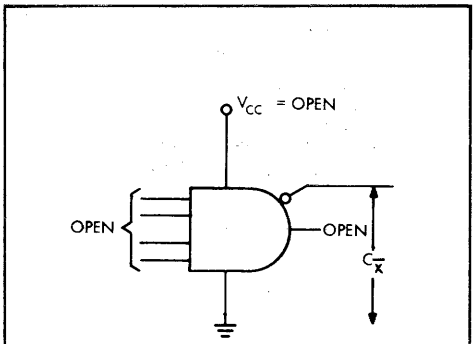
VOLTAGE WAVEFORMS

NOTES: 1. Clear or Preset inputs dominate regardless of the state of Clock or J-K inputs.
2. Clear or Preset input pulse characteristics: $V_{in(1)} = 3$ V, $V_{in(0)} = 0$ V, $t_1 = t_0 = 7$ ns, $t_{p(clear)} = t_{p(preset)} = 16$ ns, and PRR = 1 MHz.
3. See applicable circuit type for actual J and K input configuration and presence of Preset or Clear junctions.
4. C_L includes probe and jig capacitance.

FIGURE 78—FLIP-FLOP PRESET/CLEAR PROPAGATION DELAY TIMES

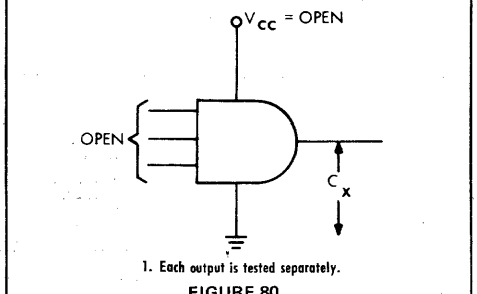
PARAMETER MEASUREMENT INFORMATION

switching time data test circuits



1. Each output is tested separately.

FIGURE 79

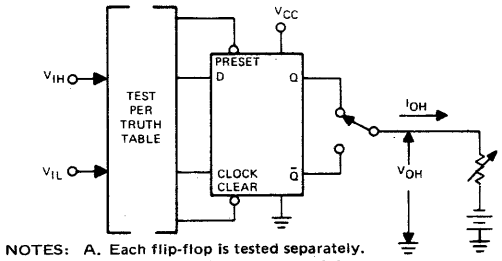


1. Each output is tested separately.

FIGURE 80

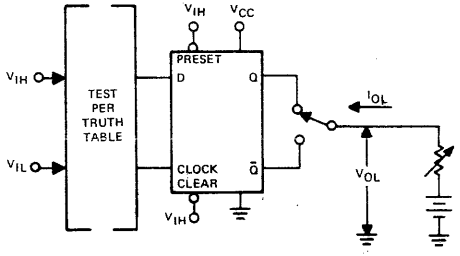
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



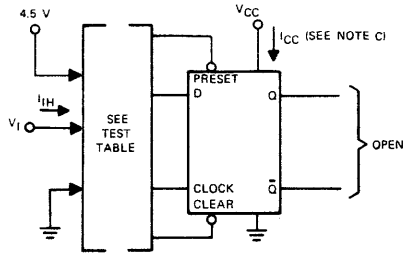
NOTES: A. Each flip-flop is tested separately.
B. Each output is tested separately.
C. V_{OH} is also tested using Clear and Preset inputs.

FIGURE 81–V_{IH}, V_{IL}, V_{OH}



NOTES: A. Each flip-flop is tested separately.
B. Each output is tested separately.

FIGURE 82–V_{IH}, V_{IL}, V_{OL}



TEST TABLE

APPLY V_I (TEST I_{IH})	APPLY 4.5 V	APPLY GND
Clock	Clear and D	Preset
Clock	Preset and D	Clear
Preset	Clear and D	Clock (See Note B)
Clear	Preset	Clock, D, and Q
Clear	Preset	D and Clock (See Note B)
D	Preset and Clock	Clear

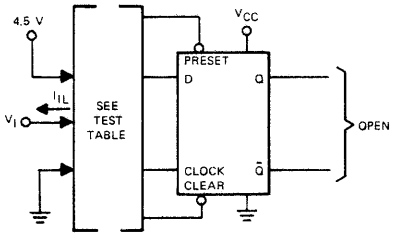
NOTES: A. Each input of each flip-flop is tested separately for I_{IH}.
B. GND is momentarily applied to Clock, then 4.5 V.
C. I_{CC} is measured simultaneously for both flip-flops with D, Clock, and Preset at GND; then with D, Clock, and Clear at GND.

FIGURE 83–I_{IH}, I_{CC}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



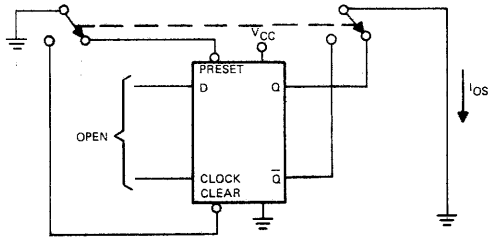
TEST TABLE

APPLY V_{in} (TEST I_{IL})	APPLY 4.5 V	APPLY GND
Clock	Clear	Preset and D
Preset	Clear	Clock and D
Clear	Clock, D, and Preset	None
D	Clear and Clock	Preset

NOTES: A. Each flip-flop is tested separately.
B. Each input is tested separately.

FIGURE 84–I_{IL}

7



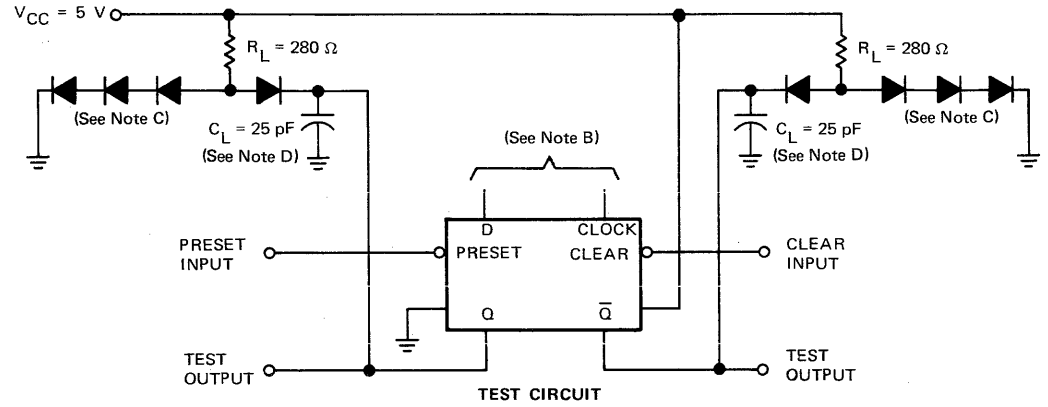
NOTE: Each output is tested separately.

FIGURE 85–I_{OS}

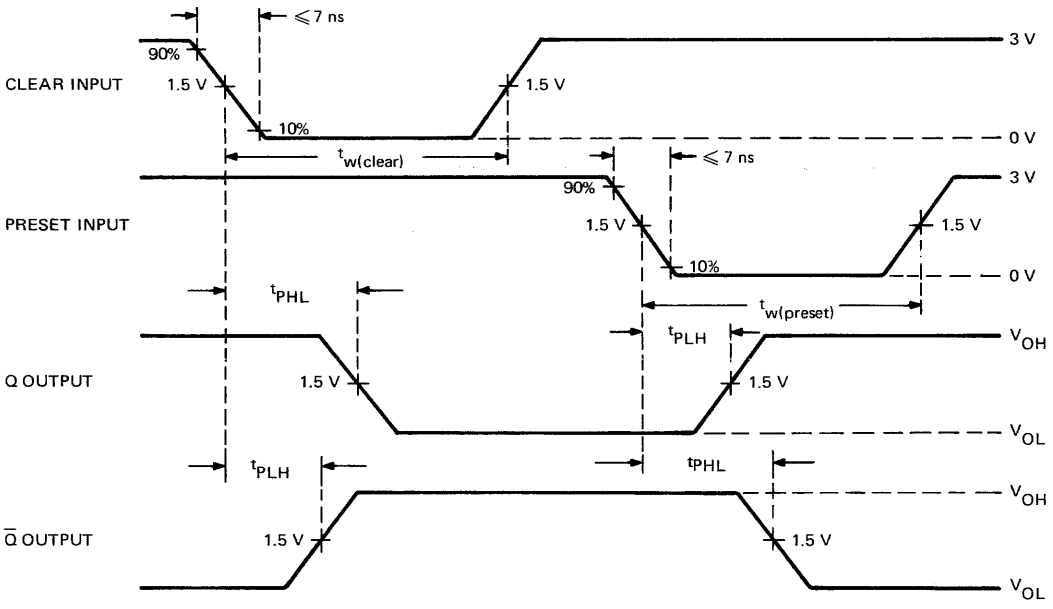
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



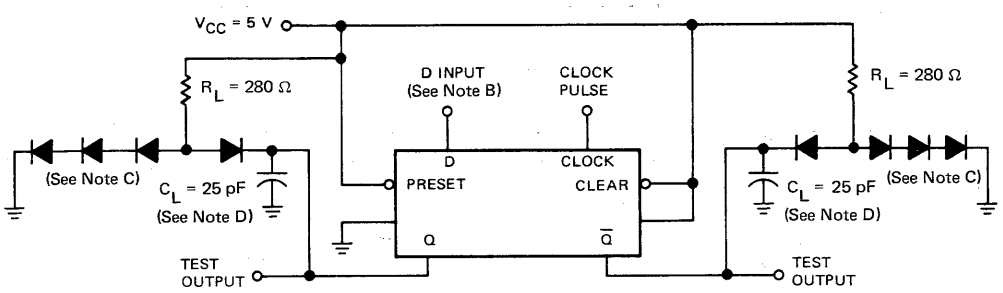
VOLTAGE WAVEFORMS

NOTES: A. Clear or Preset input pulse characteristics: $t_{w(clear)} = t_{w(preset)}$ = 25 ns, PRR = 1 MHz.
B. Clear and Preset inputs dominate regardless of the state of Clock or D inputs.
C. All diodes are 1N3064.
D. C_L includes probe and jig capacitance.

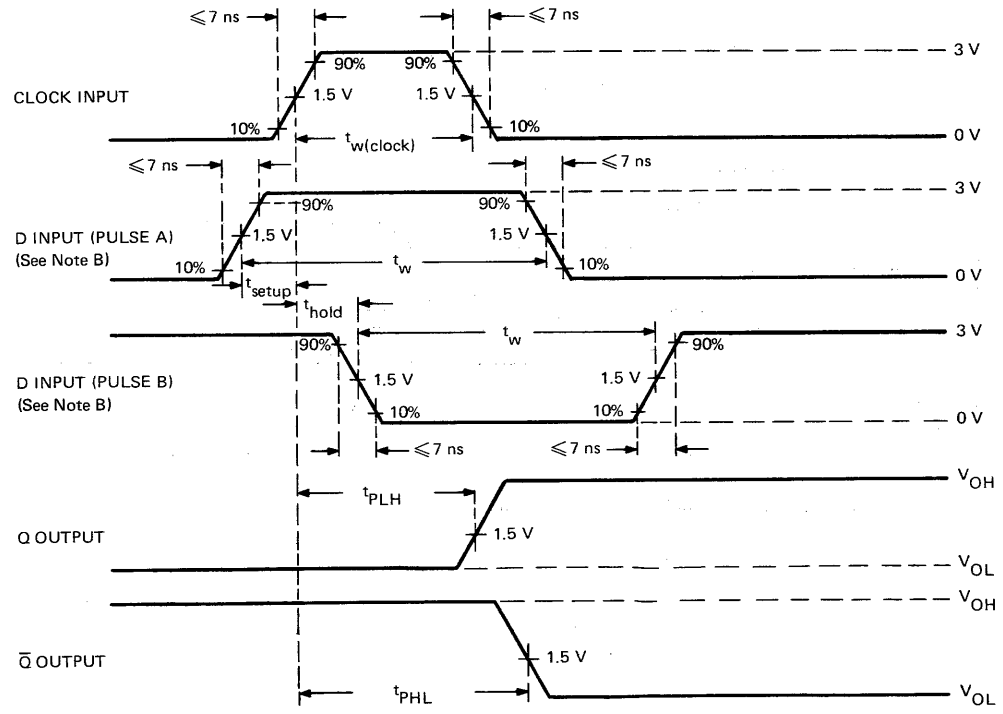
FIGURE 86–ASYNCHRONOUS INPUTS SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



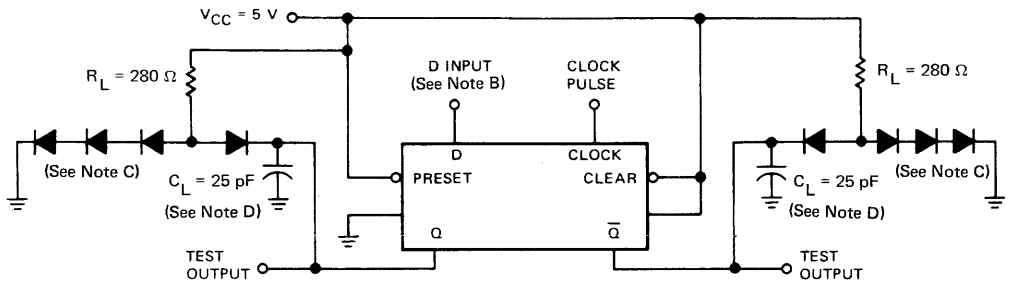
VOLTAGE WAVEFORMS

NOTES: A. Clock input pulse has the following characteristics: $t_{w(clock)}$ = 20 ns and PRR = 1 MHz. When testing f_{clock}, vary PRR.
B. D input (pulse A) has the following characteristics: t_{setup} = 10 ns, t_w = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 0 ns, t_w = 60 ns, and PRR is 50% of the clock PRR.
C. All diodes are 1N3064.
D. C_L includes probe and jig capacitance.

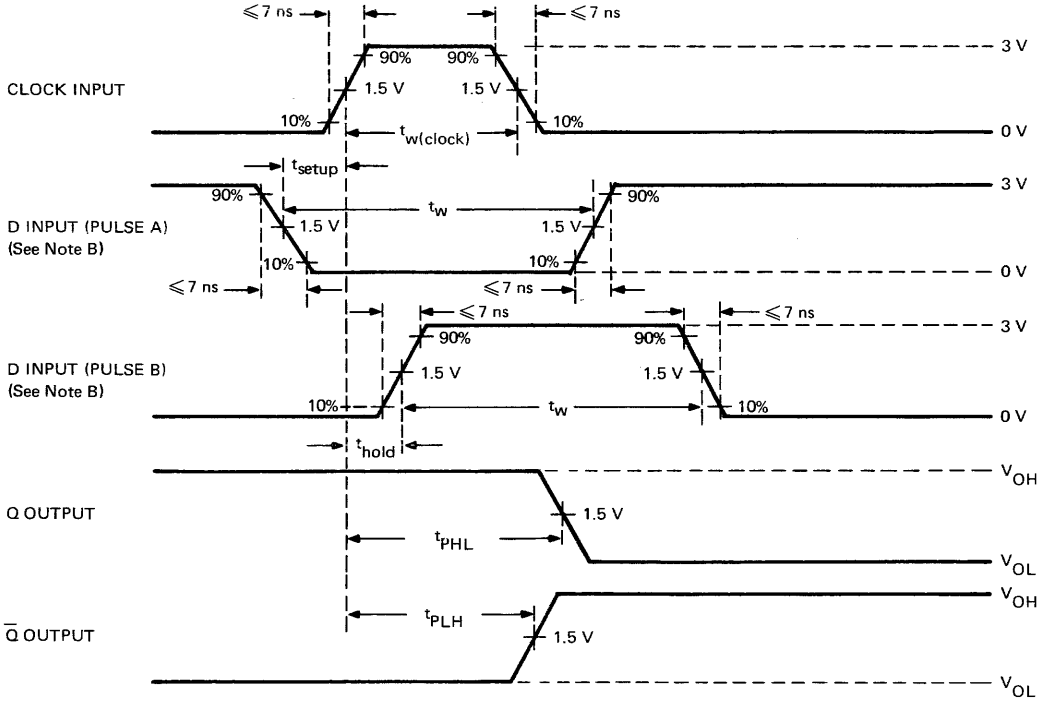
FIGURE 87–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS (HIGH-LEVEL DATA)

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



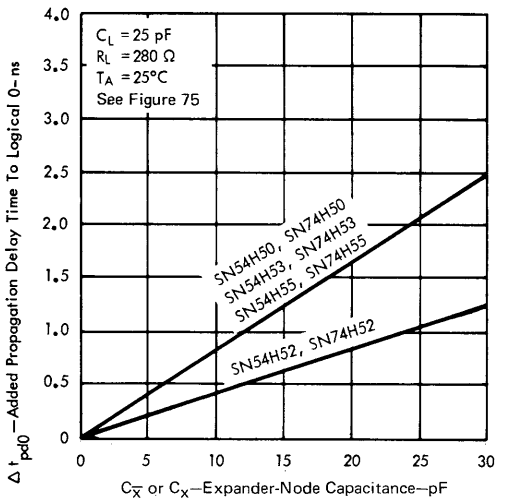
VOLTAGE WAVEFORMS

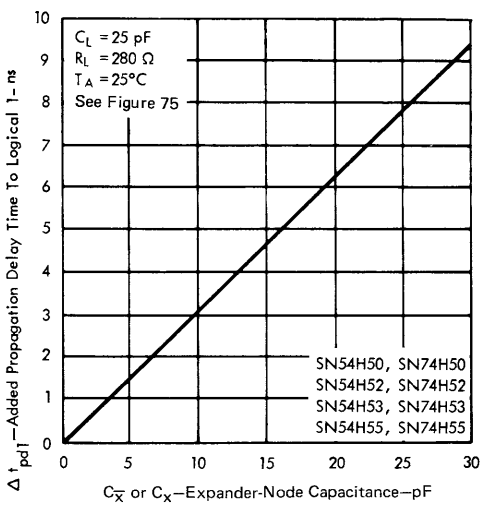
NOTES: A. Clock input pulse has the following characteristics: t_w = 20 ns and PRR = 1 MHz. When testing f_{clock}, vary PRR.
B. D input (pulse A) has the following characteristics: t_{setup} = 15 ns, t_w = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 0 ns, t_w = 60 ns, and PRR is 50% of the clock PRR.
C. All diodes are 1N3064.
D. C_L includes probe and jig capacitance.

FIGURE 88–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS (LOW-LEVEL DATA)

TYPICAL CHARACTERISTICS

ADDED PROPAGATION DELAY TIME vs EXPANDER-NODE CAPACITANCE





7

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Series 54L/74L Circuits

Series 54L/74L
Low Power TTL
Integrated Circuits

- Over 14 MSI Functions
- All Popular Package Configurations
- Fast Delivery to MIL-STD-883 for Military and Space Applications.

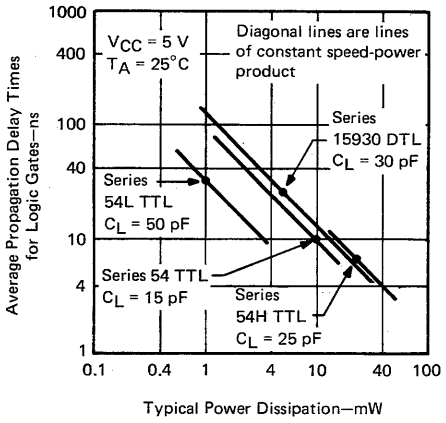
LOW-POWER TRANSISTOR-TRANSISTOR LOGIC CIRCUITS FOR AEROSPACE, MILITARY, OR INDUSTRIAL COMPUTER AND CONTROL SYSTEM APPLICATIONS

description

Series 54L/74L integrated circuits have been designed for aerospace, military, and industrial applications where high d-c noise margin, low power dissipation, improved speed-power relationships, and high reliability are important system considerations. This logic family includes small-scale integration (SSI) circuits and medium-scale integration (MSI) circuits needed to perform most functions of general-purpose digital systems. Definitive specifications for Series 54L/74L SSI circuits (gates and flip-flops) are provided in this section, and 54L/74L MSI circuits are included in Section 9.

Series 54L circuits are characterized for operation over the full military temperature range of −55°C to 125°C, and Series 74L circuits are characterized for operation over the temperature range of 0°C to 70°C.

SPEED-POWER RELATIONSHIPS OF DIGITAL IC FAMILIES†



†Typical saturated logic gate from the indicated families

features

CHOICE OF PACKAGES

- available in flat (T) and dual-in-line package (J or N)
- maximum number of circuits per package through use of 14-lead package

OPTIMUM CIRCUIT PERFORMANCE

- very low power dissipation—typically 1 mW per gate at 50% duty cycle
- relatively high speed—typically gate propagation delay time of 33 ns
- high d-c noise margin—typically one volt at $T_A = 25°C$
- low output impedance provides low a-c noise susceptibility
- waveform integrity over full range of loading and temperature conditions
- fan-out—10 Series 54L loads
  - —1 Series 54 load and 2 Series 54L loads
  - —1 Series 54H load
- a standard Series 54 output will drive 40 Series 54L loads
- logic levels are compatible with most bipolar saturated integrated circuits

8

SERIES 54L/74L
FEATURING 1 mW AND 33 ns PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	–55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
NAND/NOR GATES						
Quadruple 2-Input Positive NAND Gates	SN54L00	SN74L00	J	N	T	8-4
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN54L01	SN74L01	J	N	T	8-5
Quadruple 2-Input Positive NOR Gates	SN54L02	SN74L02	J	N	T	8-6
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN54L03	SN74L03	J	N	T	8-5
Hex Inverters	SN54L04	SN74L04	J	N	T	8-9
Triple 3-Input Positive NAND Gates	SN54L10	SN74L10	J	N	T	8-10
Dual 4-Input Positive NAND Gates	SN54L20	SN74L20	J	N	T	8-11
8-Input Positive NAND Gates	SN54L30	SN74L30	J	N	T	8-12
AND-OR-INVERT GATES						
Dual 2-Wide AND-OR-INVERT Gates	SN54L51	SN74L51	J	N	T	8-13
4-Wide 3-2-2-3-Input AND-OR-INVERT Gates	SN54L54	SN74L54	J	N	T	8-14
2-Wide 4-Input AND-OR-INVERT Gates	SN54L55	SN74L55	J	N	T	8-15
FLIP-FLOPS						
R-S Master-Slave Flip-Flops	SN54L71	SN74L71	J	N	T	8-16
J-K Master-Slave Flip-Flops	SN54L72	SN74L72	J	N	T	8-19
Dual J-K Master-Slave Flip-Flops	SN54L73	SN74L73	J	N	T	8-22
Dual D-Type Edge-Triggered Flip-Flops	SN54L74	SN74L74	J	N	T	8-25
Dual J-K Master-Slave Flip-Flops (Common Clock)	SN54L78	SN74L78	J	N	T	8-28
Retriggerable Monostable Multivibrators with Clear	SN54L122	SN74L122	J	N	T	8-31

SEE PAGES 9-1, 9-2, AND 9-3 FOR LISTING OF TTL MSI CIRCUITS

*For outline drawings of all packages, see Section 1.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	8 V
Input Voltage, V_{in} (See Notes 1 and 2)	5.5 V
Operating Free-Air Temperature Range: Series 54L	−55°C to 125°C
Series 74L	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

logic definition

Series 54L and 74L logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

HIGH VOLTAGE = LOGICAL 1
LOW VOLTAGE = LOGICAL 0

unused gates

Inputs of unused gates should be connected to ground. This sets the gate output to logical 1 to ensure minimum power dissipation.

unused inputs of NAND/AND gates

Unused inputs, including preset and clear, must be maintained at a positive voltage greater than 2.4 V but not to exceed the absolute maximum rating of 5.5 V.

Some possible ways of handling unused inputs are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between 2.4 V and 3.5 V.
b. Connect unused inputs, except preset or clear, to a used input of the same gate if maximum fan-out of the driving output will not be exceeded.
c. Connect unused inputs to the logical 1 output of an unused gate.
d. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor.

input-current requirements

Input-current requirements reflect worst-case V_{CC} and temperature conditions. Each input of the multiple-emitter input transistor requires no more than a 0.18-mA flow out of the input at a logical 0 voltage level; therefore, one load (N=1) is −0.18 mA maximum. Each input, except the clock inputs of the flip-flops, requires current into the terminal at a logical 1 voltage level. This current is 10 μA maximum for each. See fan-out capabilities (below) and typical characteristics (page 8-47) for flip-flop clock input current requirements. Currents into the input terminals are specified as positive values.

8

fan-out capability

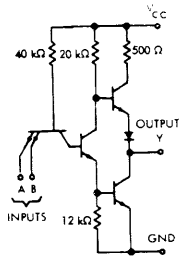
Fan-out (N) reflects the ability of an output to sink current from a number of Series 54L and 74L loads at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each Series 54L output is capable of sinking current or supplying current to 10 Series 54L loads (N=10), or one Series 54/74 load and two 54L loads. Each Series 74L output is capable of sinking current or supplying current to 20 Series 74L loads (N=20), or two Series 54/74 loads and two 74L loads. Load currents (out of the output terminal) are specified as negative values.

A Series 54 or 74 output is capable of sinking current or supplying current to 40 Series 54L or 74L loads (N=40). The Series 54/74 buffer gate circuit (SN5440/SN7440) is capable of driving 120 Series 54L/74L loads. The carry outputs of the Series 54/74 adders are capable of driving 20 Series 54L/74L loads and the A★ and B★ nodes of the SN5480/SN7480 may be used to drive 12 loads.

When fanning out into Series 54L/74L flip-flop clock inputs, no load current (I_{load}) is drawn at $V_{in(clock)}$ = 2.4 V. Therefore, the fan-out limitation is the I_{sink} capability of the driving output. A Series 54/74 output will sink sufficient current to drive 44 clock inputs (88 loads), and the SN5440/SN7440 circuit will sink sufficient current to drive 133 clock inputs (266 loads). The Series 54L output is capable of driving five 54L clock inputs and one additional load. The Series 74L output is capable of driving ten 74L clock inputs.

CIRCUIT TYPES SN54L00, SN74L00
QUADRUPLE 2-INPUT POSITIVE NAND GATES

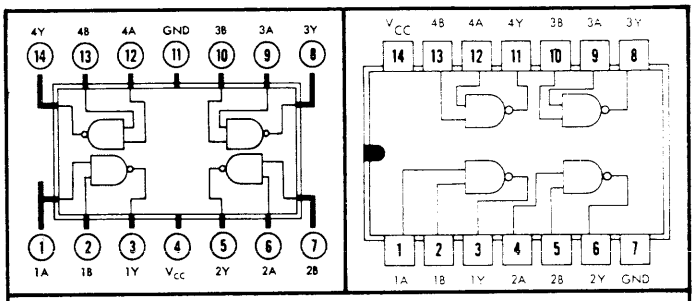
schematic (each gate)



NOTE: Component values shown are nominal.

T
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L00 Circuits	4.5	5	5.5	V
SN74L00 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L00 Circuits	−55	25	125	°C
SN74L00 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1		2		V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2			0.7	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{os}	Short-circuit output current	5	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 5 V		0.51	mA
$I_{CC(1)}$	Logical 1 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 0		0.2	mA

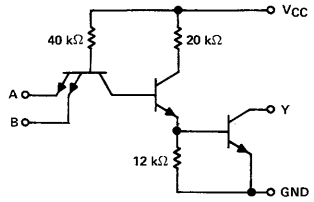
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		31	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

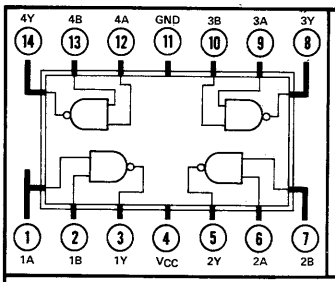
CIRCUIT TYPES SN54L01, SN54L03, SN74L01, SN74L03
QUADRUPLE 2-INPUT POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

schematic (each gate)

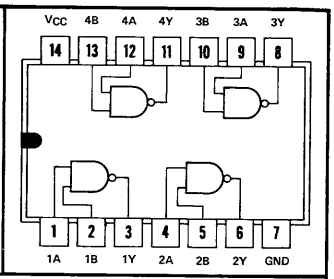


Resistor values shown are nominal.

SN54L01, SN74L01
T FLAT PACKAGE
(TOP VIEW)



SN54L03, SN74L03
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	SN54L01 SN54L03			SN74L01 SN74L03			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.6	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.6 V, V_{OH} = 5.5 V		50	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V		100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V		10	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX, All inputs grounded		0.2	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX, All inputs at 5 V		0.51	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

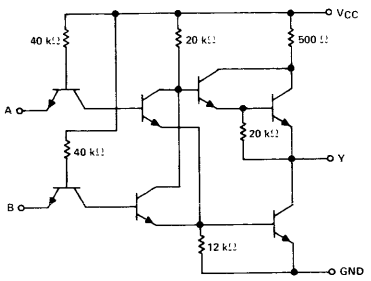
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 4 kΩ, See Figure 35		90	ns
t_{PHL}	Propagation delay time, high-to-low-level output			60	

8

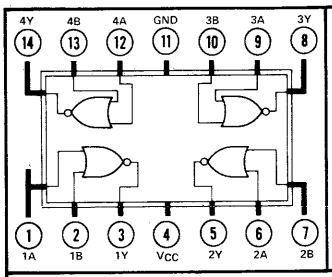
CIRCUIT TYPES SN54L02, SN74L02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

schematic (each gate)

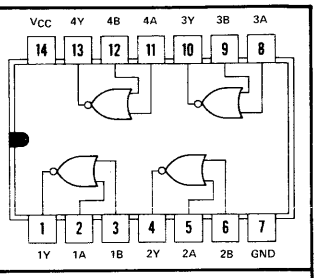


Resistor values shown are nominal.

T FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{A + B}$

recommended operating conditions

	SN54L02			SN74L02			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.7	V
V_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.7 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V		100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V		10	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX	−3	−15	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX, See Note 3		0.4	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX, See Note 4		0.65	mA

NOTES: 3. I_{CCH} is measured with all inputs grounded and outputs open.
4. I_{CCL} is measured with one input of each gate at 5 V, the remaining inputs grounded, and outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 4 kΩ, See Figure 35		31	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	60	

APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-AND function, and simultaneously, will drive from one to nine Series 54L/74L loads. When no other open-collector gates are paralleled, this gate may be used to drive ten Series 54L/74L loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available while the output is high. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the low level even if one of the paralleled outputs is sinking all the currents.

In both conditions (low and high level) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

high-level (off-state) circuit calculations (see figure A)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the V_{OH} level required at the load:

$$V_{RL} = V_{CC} - V_{OH\ min}$$

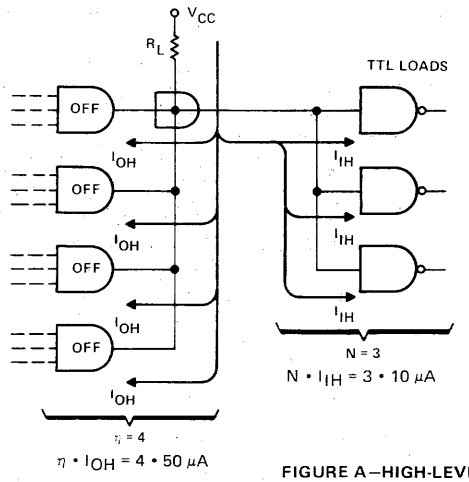
The total current through the load resistor (I_{RL}) is the sum of the load currents (I_{IH}) and off-state reverse currents (I_{OH}) through each of the wire-AND-connected outputs:

$$I_{RL} = \eta \cdot I_{OH} + N \cdot I_{IH} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\ min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

where η = number of gates wire-AND-connected, and N = number of Series 54L/74L loads.



Calculation:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\ min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

$$R_{L(max)} = \frac{5 - 2.4}{0.0002 + 0.00003}\ \Omega = \frac{2.6}{0.00023}\ \Omega = 11\,300\ \Omega$$

FIGURE A—HIGH-LEVEL CIRCUIT CONDITIONS

8

SERIES 54L/74L
OPEN-COLLECTOR OUTPUT APPLICATION DATA

APPLICATION DATA

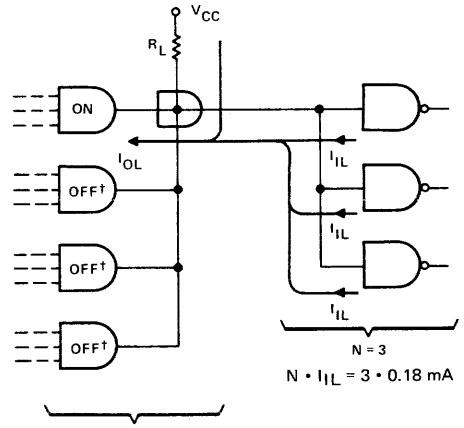
low-level (on-state) circuit calculations (see figure B)

The current through the resistor must be limited to the maximum sink current of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during low-level periods, the current must be limited to 2 mA, the maximum current which will ensure a low-level maximum of 0.3 volt.

Also, fan-out must be considered. Part of the 2 mA will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{IL}}$$



Calculation:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{IL}}$$

$$R_{L(min)} = \frac{5 - 0.3}{0.002 - 0.00054}\ \Omega = \frac{4.7}{0.00146}\ \Omega = 3\,220\ \Omega$$

†Current into OFF outputs is negligible at the low logic level.

FIGURE B–LOW-LEVEL CIRCUIT CONDITIONS

driving series 54L/74L loads and combining outputs

Table 1 provides minimum and maximum resistor values, calculated from equations shown above, for driving one to ten Series 54L/74L loads and wire-AND connecting two to ten parallel outputs. Each value shown for one wire-AND output is determined by the fan-out plus the cutoff current of a single output transistor. Extension beyond ten wire-AND connections is permitted with fan-outs of five or less if a valid minimum and maximum R_L is possible. When fanning-out to ten Series 54L/74L loads, the calculation for the minimum value of R_L indicates that a value greater than the maximum value of R_L should be used; however, the use of a resistor having a value between 15.6 kΩ and 17.3 kΩ in this case will satisfy the high level condition and limit the low level to less than 0.31 volt.

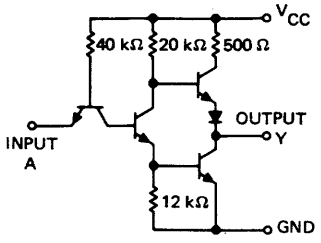
TABLE 1

FAN-OUT TO 54L/74L LOADS	WIRE-AND OUTPUTS										
	1	2	3	4	5	6	7	8	9	10	1 TO 10
1	43.3	23.6	16.2	12.4	10.0	8.38	7.22	6.34	5.65	5.10	2.55
2	37.2	21.6	15.3	11.8	9.63	8.13	7.03	6.20	5.53	5.00	2.87
3	32.5	20.0	14.5	11.3	9.29	7.88	6.85	6.05	5.42	4.90	3.22
4	28.9	18.6	13.7	10.8	8.96	7.65	6.67	5.91	5.31	4.82	3.67
5	26.0	17.3	13.0	10.4	8.66	7.44	6.50	5.78	5.20	4.73	4.29
6	23.6	16.2	12.4	10.0	8.38	7.22	6.34	5.65	X	X	5.20
7	21.6	15.3	11.8	9.63	8.13	7.03	X	X	X	X	6.35
8	20.0	14.5	11.3	9.29	X	X	X	X	X	X	8.40
9	18.6	13.7	X	X	X	X	X	X	X	X	12.4
10	17.3	X	X	X	X	X	X	X	X	X	15.6§
	MAXIMUM										MIN
	LOAD, RESISTOR VALUE IN KILOHMS										

All values in the table are based on:
High-level condition: V_{CC} = 5 V, $V_{OH\ min}$ = 2.4 V
Low-level condition: V_{CC} = 5 V, $V_{OL\ max}$ = 0.3 V
X–Not recommended or not possible
§The theoretical value is 23.5 kΩ. See explanation in text.

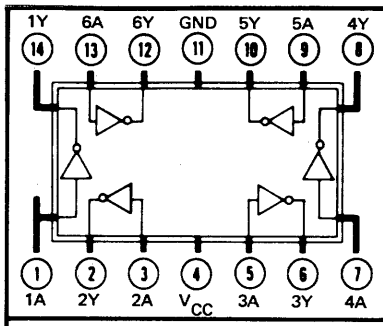
8

schematic (each inverter)

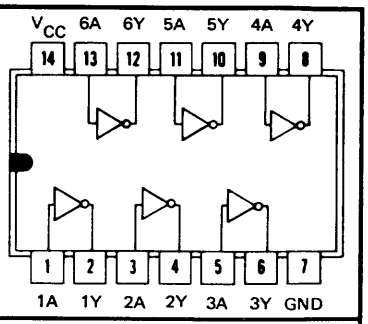


Component values shown are nominal.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic
$Y = \overline{A}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L04 Circuits	4.5	5	5.5	V
SN74L04 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L04 Circuits	−55	25	125	°C
SN74L04 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	7		2		V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 level at output	8			0.7	V
$V_{out(1)}$	Logical 1 output voltage	8	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = − 100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	7	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current	9	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current	10	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	
I_{OS}	Short-circuit output current	11	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current (Average per inverter)	12	V_{CC} = MAX, V_{in} = 5 V		0.51	mA
$I_{CC(1)}$	Logical 1 level supply current (Average per inverter)	12	V_{CC} = MAX, V_{in} = 0		0.2	mA

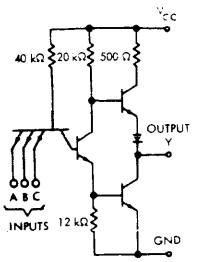
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		31	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

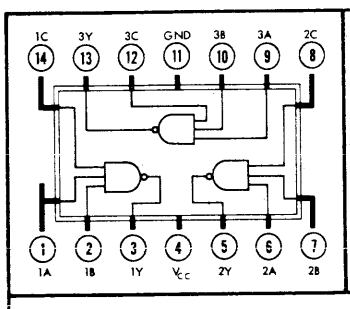
CIRCUIT TYPES SN54L10, SN74L10
TRIPLE 3-INPUT POSITIVE NAND GATES

schematic (each gate)

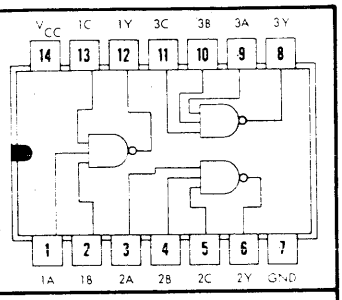


NOTE: Component values shown are nominal.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$Y = \overline{ABC}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L10 Circuits	4.5	5	5.5	V
SN74L10 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L10 Circuits	−55	25	125	°C
SN74L10 Circuits	0	25	70	°C

8

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1		2		V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2			0.7	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{OS}	Short-circuit output current	5	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 5 V		0.51	mA
$I_{CC(1)}$	Logical 1 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 0		0.2	mA

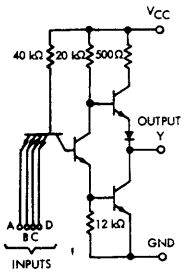
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		31	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

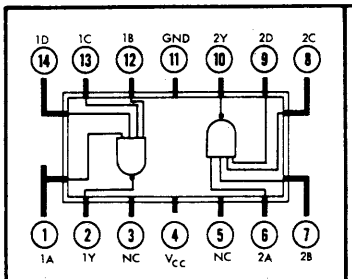
CIRCUIT TYPES SN54L20, SN74L20
DUAL 4-INPUT POSITIVE NAND GATES

schematic (each gate)

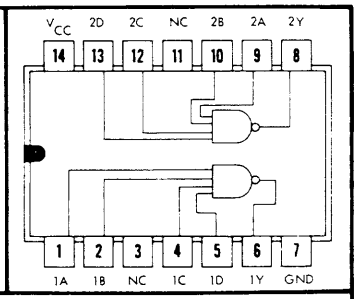


NOTES: 1. Component values shown are nominal.
2. NC — No internal connection.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$Y = \overline{ABCD}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L20 Circuits	4.5	5	5.5	V
SN74L20 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L20 Circuits	−55	25	125	°C
SN74L20 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1		2		V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2			0.7	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{OS}	Short-circuit output current	5	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 5 V		0.51	mA
$I_{CC(1)}$	Logical 1 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 0		0.2	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

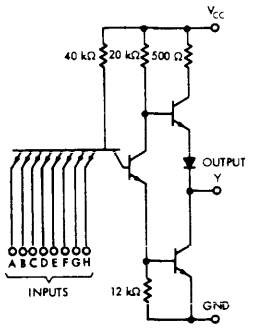
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		31	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

8

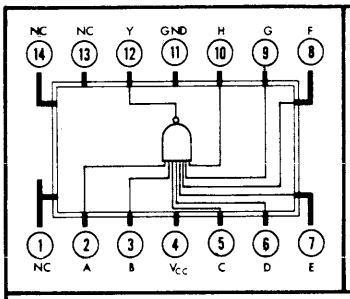
CIRCUIT TYPES SN54L30, SN74L30
8-INPUT POSITIVE NAND GATES

schematic

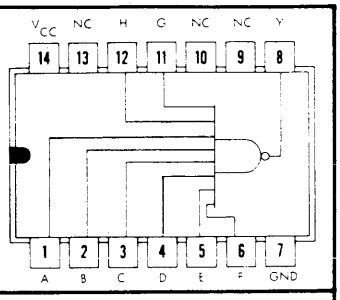


NOTES: 1. Component values shown are nominal.
2. NC — No internal connection

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$Y = \overline{ABCDEFGH}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L30 Circuits	4.5	5	5.5	V
SN74L30 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L30 Circuits	−55	25	125	°C
SN74L30 Circuits	0	25	70	°C

8

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

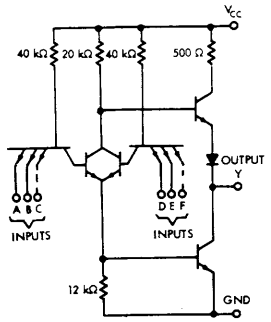
PARAMETER	TEST FIGURE	TEST CONDITIONS†		MIN	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1			2		V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2				0.7	V
$V_{out(1)}$ Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA		2.4		V
$V_{out(0)}$ Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA			0.3	V
$I_{in(0)}$ Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.3 V			−0.18	mA
$I_{in(1)}$ Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			10	μA
		V_{CC} = MAX, V_{in} = 5.5 V			100	μA
I_{OS} Short-circuit output current	5	V_{CC} = MAX, V_{in} = 0, V_{out} = 0		−3	−15	mA
$I_{CC(0)}$ Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			0.51	mA
$I_{CC(1)}$ Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0	SN54L30		0.33	mA
			SN74L30		0.2	

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0} Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		70	100	ns
t_{pd1} Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns

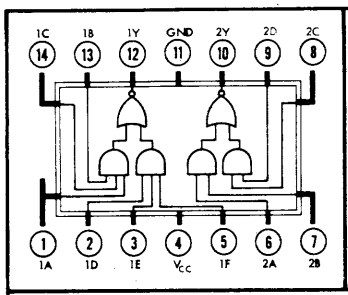
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

schematic (each gate)

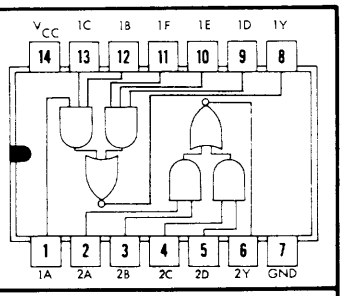


NOTES: 1. Component values shown are nominal.
2. Inputs C and F are available on gate 1 only.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$$

$$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L51 Circuits	4.5	5	5.5	V
SN74L51 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L51 Circuits	−55	25	125	°C
SN74L51 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of either AND section to ensure logical 0 at output	13		2		V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	14			0.7	V
$V_{out(1)}$	Logical 1 output voltage	14	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	13	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	15	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	16	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{os}	Short-circuit output current	17	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current (average per gate)	18	V_{CC} = MAX, V_{in} = 5 V		0.65	mA
$I_{CC(1)}$	Logical 1 level supply current (average per gate)	18	V_{CC} = MAX, V_{in} = 0		0.4	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

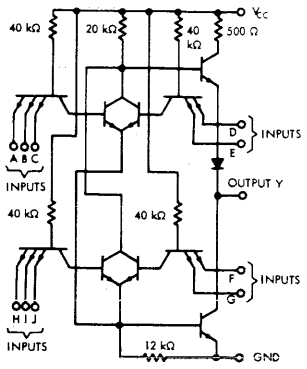
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		50	90	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

8

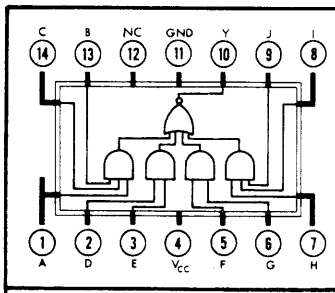
CIRCUIT TYPES SN54L54, SN74L54
4-WIDE 3-2-2-3-INPUT AND-OR-INVERT GATES

schematic



NOTE: 1. Component values shown are nominal.
2. NC — No internal connection

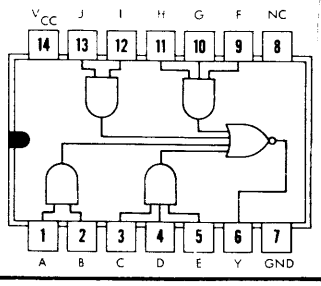
T
FLAT PACKAGE (TOP VIEW)



positive logic

$Y = \overline{(ABC) + (DE) + (FG) + (HIJ)}$

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic:

$Y = \overline{(AB) + (CDE) + (FGH) + (IJ)}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L54 Circuits	4.5	5	5.5	V
SN74L54 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L54 Circuits	−55	25	125	°C
SN74L54 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

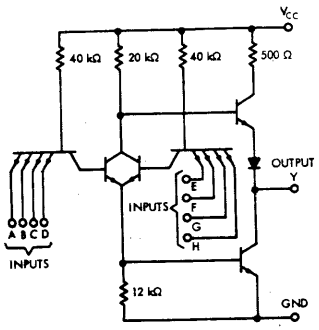
PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals of one AND section to ensure logical 0 at output	13		2		V
$V_{in(0)}$ Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	14			0.7	V
$V_{out(1)}$ Logical 1 output voltage	14	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$ Logical 0 output voltage	13	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$ Logical 0 level input current (each input)	15	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$ Logical 1 level input current (each input)	16	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
		V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{OS} Short-circuit output current	17	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$ Logical 0 level supply current	18	V_{CC} = MAX, V_{in} = 5 V		0.99	mA
$I_{CC(1)}$ Logical 1 level supply current	18	V_{CC} = MAX, V_{in} = 0		0.8	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0} Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns
t_{pd1} Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		50	90	ns

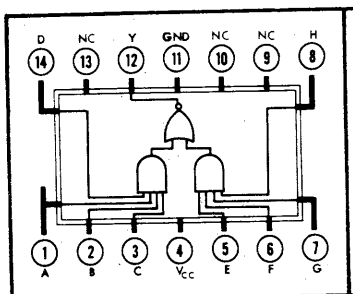
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

schematic

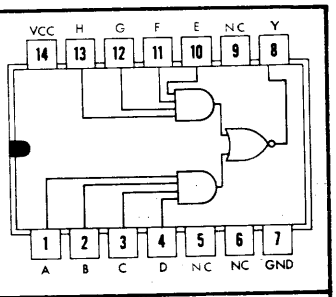


NOTE: 1. Component values shown are nominal.
2. NC — No internal connection

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$Y = \overline{(ABCD) + (EFGH)}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L55 Circuits	4.5	5	5.5	V
SN74L55 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L55 Circuits	−55	25	125	°C
SN74L55 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of either AND section to ensure logical 0 at output	13		2		V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	14			0.7	V
$V_{out(1)}$	Logical 1 output voltage	14	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	13	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	15	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	16	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{os}	Short-circuit output current	17	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current	18	V_{CC} = MAX, V_{in} = 5 V		0.65	mA
$I_{CC(1)}$	Logical 1 level supply current	18	V_{CC} = MAX, V_{in} = 0		0.4	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		50	90	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

8

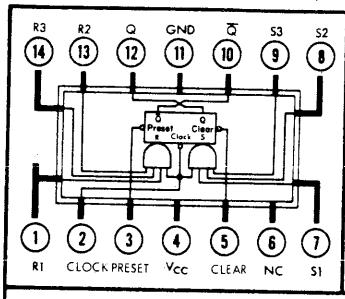
CIRCUIT TYPES SN54L71, SN74L71
R-S MASTER-SLAVE FLIP-FLOPS

logic

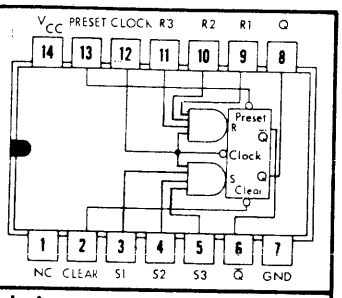
TRUTH TABLE		
t_n		t_{n+1}
R	S	Q
0	0	Q_n
0	1	1
1	0	0
1	1	indeterminate

NOTES: 1. R = R1 • R2 • R3
2. S = S1 • S2 • S3
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. NC — No internal connection.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

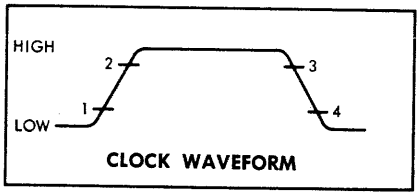


positive logic
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These R-S flip-flop circuits are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.



CLOCK WAVEFORM

8

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L71 Circuits	4.5	5	5.5	V
SN74L71 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See figure 36)	200			ns
Width of Preset Pulse, $t_{p(preset)}$ (See figure 37)	100			ns
Width of Clear Pulse, $t_{p(clear)}$ (See figure 37)	100			ns
Input Setup Time, t_{setup} (See figure 36)	100			ns
Input Hold Time, t_{hold}	0			
Operating Free-Air Temperature Range, T_A: SN54L71 Circuits	−55	25	125	°C
SN74L71 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	19 and 20		2		V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal except clock	19 and 20			0.7	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at clock input terminal	19 and 20			0.6	V
$V_{out(1)}$	Logical 1 output voltage	19	V_{CC} = MIN, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	20	V_{CC} = MIN, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current at R1, R2, R3, S1, S2, or S3	21	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	21	V_{CC} = MAX, V_{in} = 0.3 V		−0.36∫	mA
$I_{in(1)}$	Logical 1 level input current at R1, R2, R3, S1, S2, or S3	22	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
$I_{in(1)}$	Logical 1 level input current at preset or clear	22	V_{CC} = MAX, V_{in} = 2.4 V		20	μA
			V_{CC} = MAX, V_{in} = 5.5 V		200	μA
$I_{in(1)}$	Logical 1 level input current at clock	22	V_{CC} = MAX, V_{in} = 2.4 V	0∫	−0.2∫	mA
			V_{CC} = MAX, V_{in} = 5.5 V		200∫	μA
I_{os}	Short-circuit output current	23	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
I_{CC}	Supply current	22	V_{CC} = MAX, $V_{in(clock)}$ = 0		1.44	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
∫For typical clock input current see page 8-47.

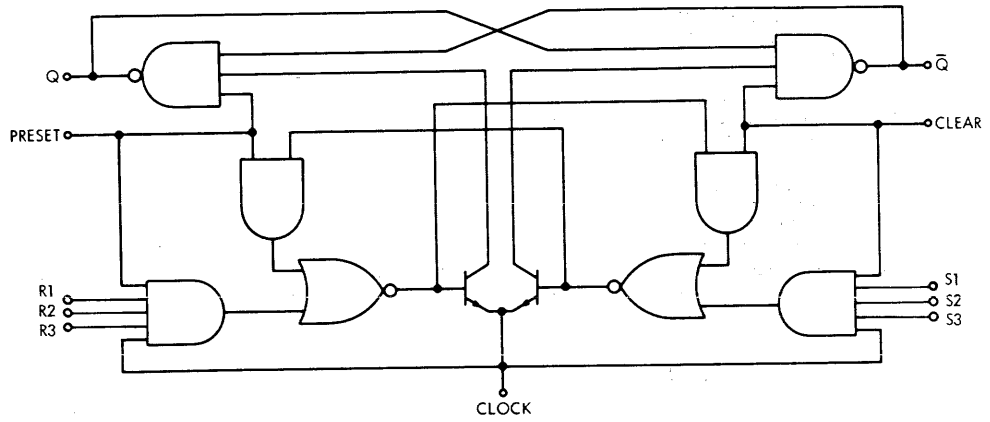
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	36	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	37	C_L = 50 pF, R_L = 4 kΩ		35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	37	C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 2.4 V		60	150	ns
			C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 0 V			200	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	60	150	ns

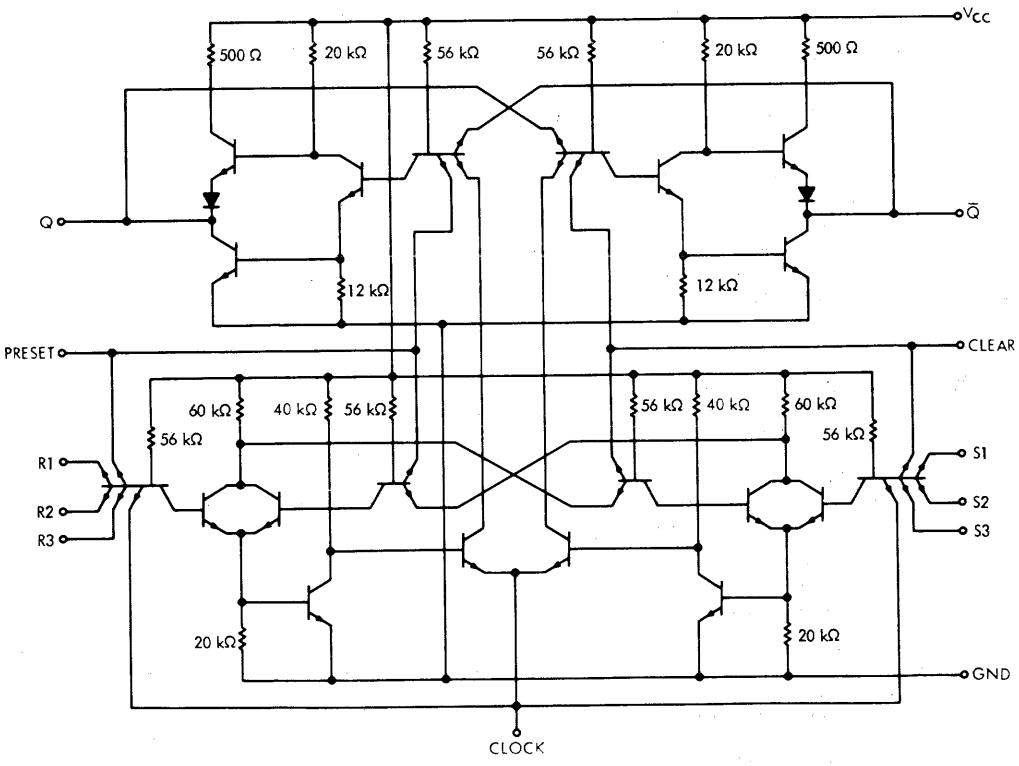
8

CIRCUIT TYPES SN54L71, SN74L71
R-S MASTER-SLAVE FLIP-FLOPS

functional block diagram



schematic



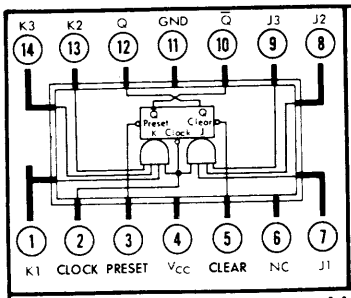
Component values shown are nominal.

logic

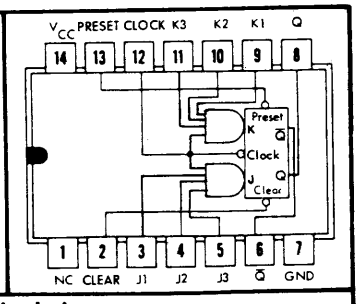
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. $J = J1 \bullet J2 \bullet J3$
2. $K = K1 \bullet K2 \bullet K3$
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. NC — No internal connection.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



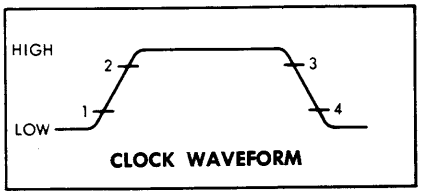
positive logic
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These J-K flip-flop circuits are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L72 Circuits	4.5	5	5.5	V
SN74L72 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See figure 36)	200			ns
Width of Preset Pulse, $t_{p(preset)}$ (See figure 37)	100			ns
Width of Clear Pulse, $t_{p(clear)}$ (See figure 37)	100			ns
Input Setup Time, t_{setup} (See figure 36)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			
Operating Free-Air Temperature Range, T_A: SN54L72 Circuits	−55	25	125	°C
SN74L72 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	24 and 25		2		V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal except clock	24 and 25			0.7	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at clock input terminal	24 and 25			0.6	V
$V_{out(1)}$	Logical 1 output voltage	24	V_{CC} = MIN, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	25	V_{CC} = MIN, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, or K3	26	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	26	V_{CC} = MAX, V_{in} = 0.3 V		−0.36‡	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	27	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
$I_{in(1)}$	Logical 1 level input current at preset or clear	27	V_{CC} = MAX, V_{in} = 2.4 V		20	μA
			V_{CC} = MAX, V_{in} = 5.5 V		200	μA
$I_{in(1)}$	Logical 1 level input current at clock	27	V_{CC} = MAX, V_{in} = 2.4 V		−0.2‡	mA
			V_{CC} = MAX, V_{in} = 5.5 V		200‡	μA
I_{os}	Short-circuit output current	28	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
I_{CC}	Supply current	27	V_{CC} = MAX, $V_{in(clock)}$ = 0		1.44	mA

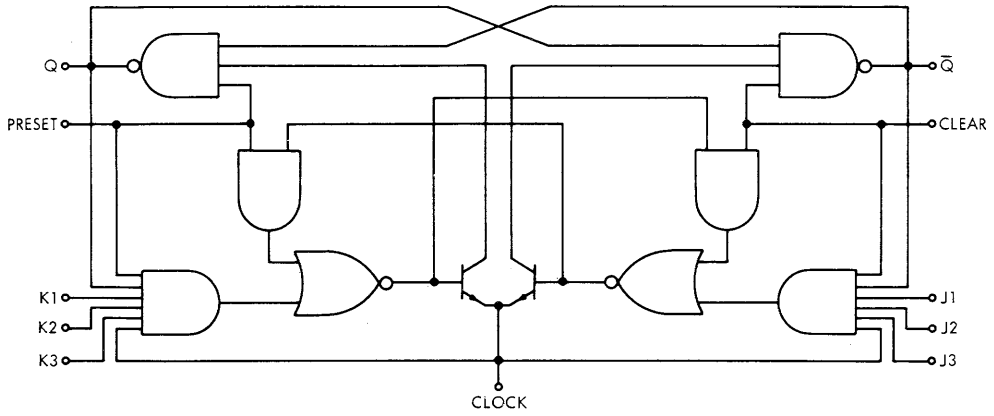
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

‡For typical clock input current see page 8-47.

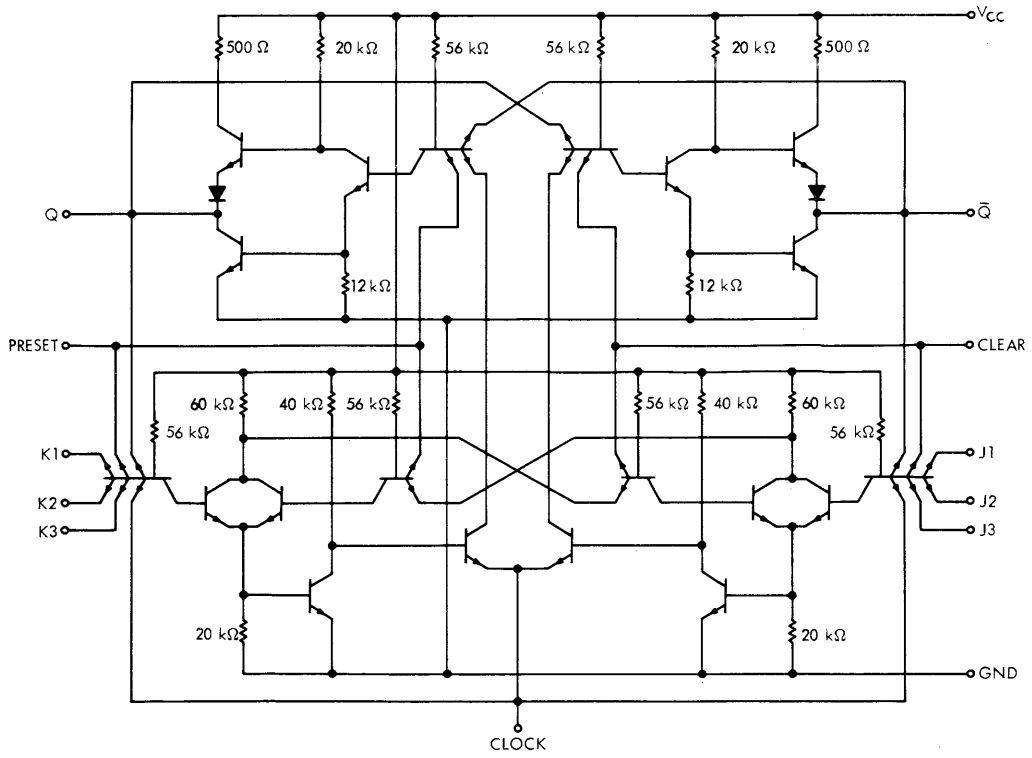
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	36	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	37	C_L = 50 pF, R_L = 4 kΩ		35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	37	C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 2.4 V		60	150	ns
			C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 0 V			200	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	60	150	ns

functional block diagram



schematic



Component values shown are nominal.

8

CIRCUIT TYPES SN54L73, SN74L73
DUAL J-K MASTER-SLAVE FLIP-FLOPS

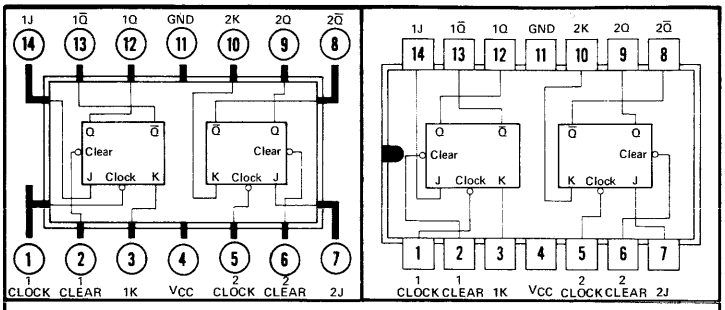
logic

TRUTH TABLE		
t_n		$t_n + 1$
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. $t_n + 1$ = Bit time after clock pulse.

T
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



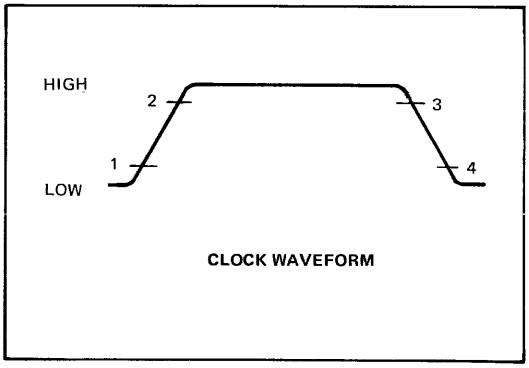
positive logic:
Low input to clear sets Q to logical 0
Clear is independent of clock

description

These J-K flip-flop circuits are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	SN54L73			SN74L73			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Width of clock pulse, $t_{p(clock)}$ (See Figure 36)	200			200			ns
Width of preset pulse, $t_{p(preset)}$ (See Figure 37)	100			100			ns
Width of clear pulse, $t_{p(clear)}$ (See Figure 37)	100			100			ns
Input setup time, t_{setup} (See Figure 36)	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input hold time, t_{hold}	0			0			
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	29 and 30		2		V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal except clock	29 and 30			0.7	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at clock input terminal	29 and 30			0.6	V
$V_{out(1)}$	Logical 1 output voltage	29	V_{CC} = MIN, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	30	V_{CC} = MIN, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current at J or K	31	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	31	V_{CC} = MAX, V_{in} = 0.3 V		−0.36∫	mA
$I_{in(1)}$	Logical 1 level input current at J or K	32	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
$I_{in(1)}$	Logical 1 level input current at clear	32	V_{CC} = MAX, V_{in} = 2.4 V		20	μA
			V_{CC} = MAX, V_{in} = 5.5 V		200	μA
$I_{in(1)}$	Logical 1 level input current at clock	32	V_{CC} = MAX, V_{in} = 2.4 V	0∫	−0.2∫	mA
			V_{CC} = MAX, V_{in} = 5.5 V		200∫	μA
I_{os}	Short-circuit output current	33	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
I_{CC}	Supply current (average per flip-flop)	32	V_{CC} = MAX, $V_{in(clock)}$ = 0		1.44	mA

†For conditons shown as MIN or MAX, use the appropriate value specified under recommended operating conditons for the applicable circuit type.

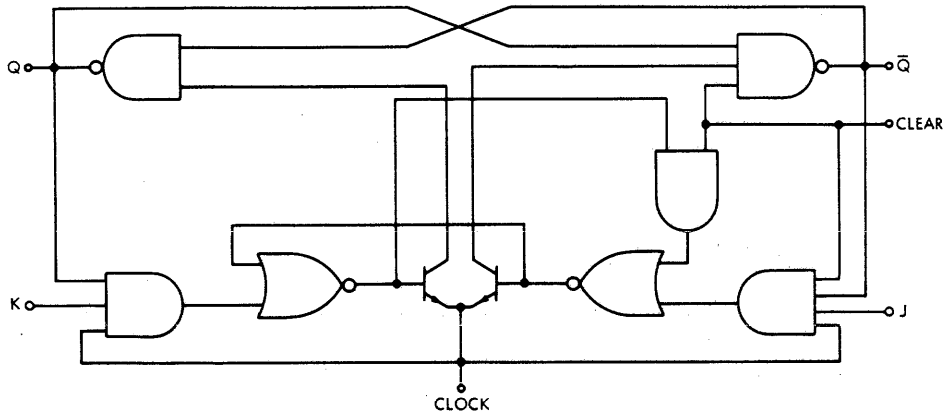
∫For typical clock input current see page 8-47.

8

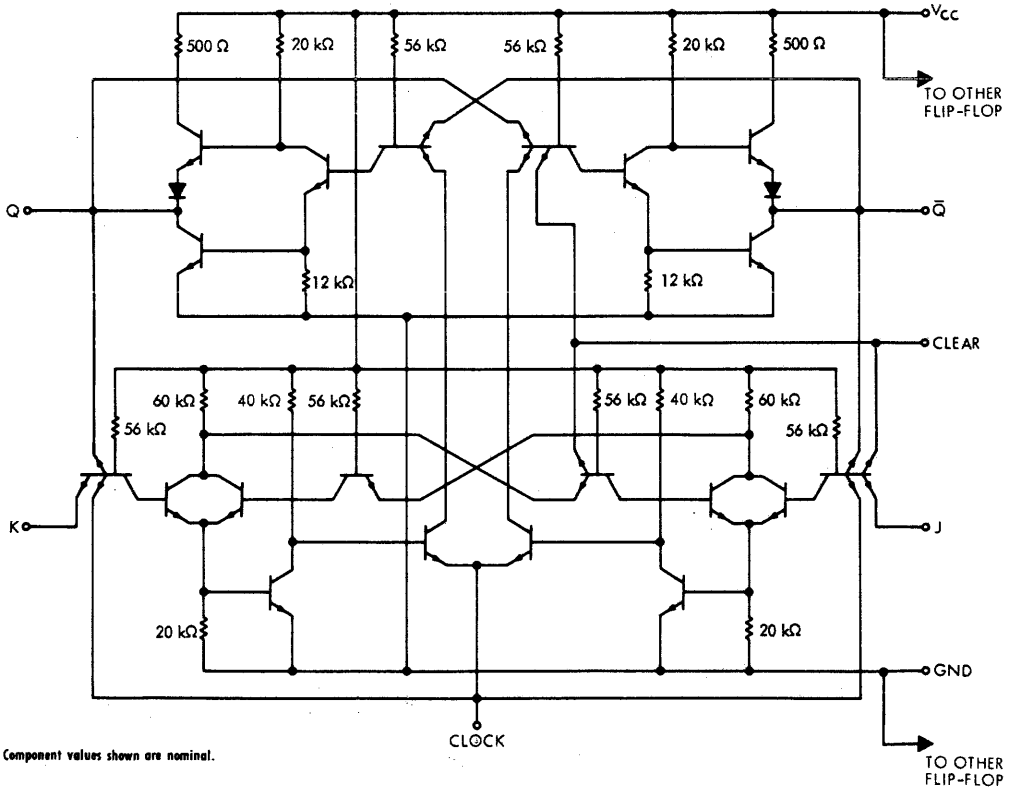
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	36	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	37	C_L = 50 pF, R_L = 4 kΩ		35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	37	C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 2.4 V		60	150	ns
			C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 0 V			200	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	60	150	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	35	75	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

CIRCUIT TYPES SN54L74, SN74L74
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- Typical Maximum Clock Frequency . . . 3 MHz
- Positive-Edge Triggering
- Fully Compatible with Most TTL and DTL Circuits
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs

logic

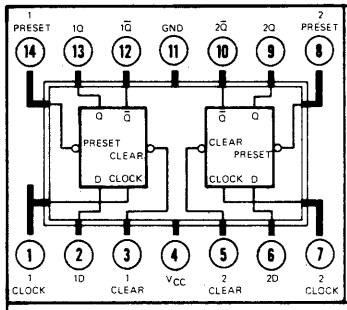
TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT	OUTPUTS	
D	Q	$\overline{Q}$
L	L	H
H	H	L

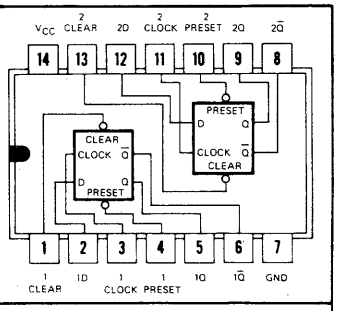
H = high level, L = low level

NOTES: A. t_n = bit time before clock pulse.
B. t_{n+1} = bit time after clock pulse.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



asynchronous inputs: Low input to preset sets Q to high level
Low input to clear sets Q to low level
Preset and clear are independent of clock

description

These monolithic, low-power, dual, edge-triggered flip-flops utilize TTL circuitry to perform D-type flip-flop logic. Each flip-flop has individual clear and preset inputs, and complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL circuits. A full fan-out to 10 normalized Series 54L/74L loads is available from each of the outputs. Maximum clock frequency is typically 3 megahertz, with a typical power dissipation of 4.25 milliwatts per flip-flop.

The SN54L74 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L74 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)	8 V
Input voltage (see Notes 1 and 2)	5.5 V
Operating free-air temperature range: SN54L74 Circuits	−55°C to 125°C
SN74L74 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN54L74			SN74L74			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Width of clock pulse, $t_{w(clock)}$ (see Figure 7 or 8)	200			200			ns
Width of preset pulse, $t_{w(preset)}$ (see Figure 6)	100			100			ns
Width of clear pulse, $t_{w(clear)}$ (see Figure 6)	100			100			ns
Input setup time for either high- or low-level data, t_{setup} (see Note 3 and Figure 7 and 8)	30			30			ns
Input hold time, t_{hold} (See Note 3 and Figure 7 and 8)	0			0			ns
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

NOTES: 3. Setup time is the interval immediately preceding the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

4. Hold time is the interval immediately following the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS‡	MIN	MAX	UNIT
V_{IH}	High-level input voltage	35, 36		2		V
V_{IL}	Low-level input voltage	35, 36			0.7	V
V_{OH}	High-level output voltage	35	V_{CC} = MIN, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	36	V_{CC} = MIN, I_{OL} = 2 mA		0.3	V
I_{IH}	High-level input current into D	37	V_{CC} = MAX, V_I = 2.4 V		10	μA
			V_{CC} = MAX, V_I = 5.5 V		100	μA
I_{IH}	High-level input current into preset or clock	37	V_{CC} = MAX, V_I = 2.4 V		20	μA
			V_{CC} = MAX, V_I = 5.5 V		200	μA
I_{IH}	High-level input current into clear	37	V_{CC} = MAX, V_I = 2.4 V		30	μA
			V_{CC} = MAX, V_I = 5.5 V		300	μA
I_{IL}	Low-level input current into preset or D	38	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{IL}	Low-level input current into clear or clock	38	V_{CC} = MAX, V_I = 0.3 V		−0.36	mA
I_{OS}	Short-circuit output current§	39	V_{CC} = MAX	−3	−15	mA
I_{CC}	Supply current (each flip-flop)	37	V_{CC} = MAX		1.5	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

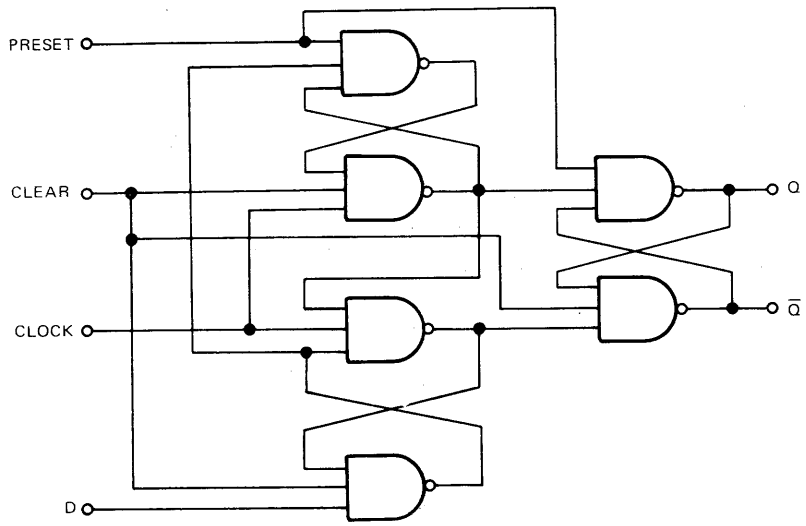
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

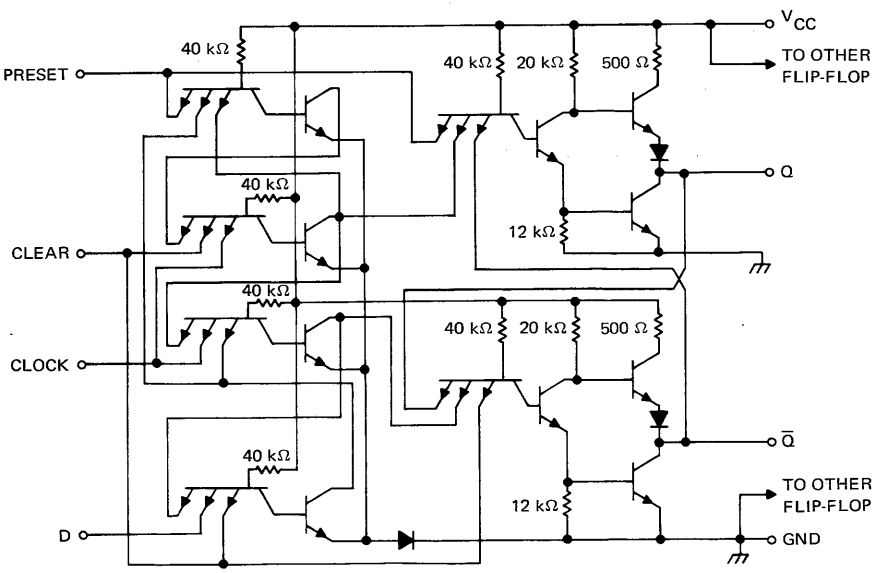
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	44, 45	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset inputs	43			50	75	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset inputs	43			80	150	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock input	44, 45		10	65	100	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock input	44, 45		10	65	150	ns

8

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

8

CIRCUIT TYPES SN54L78, SN74L78
DUAL J-K MASTER-SLAVE FLIP-FLOPS

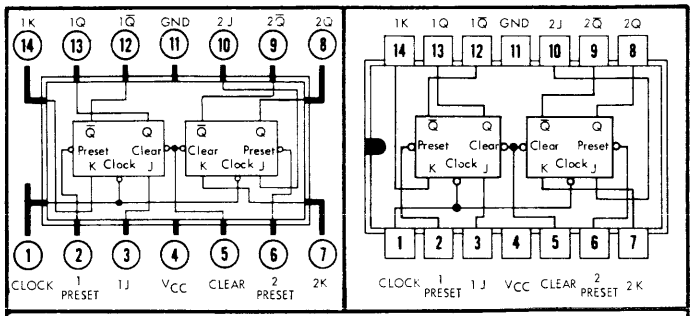
logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

T
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



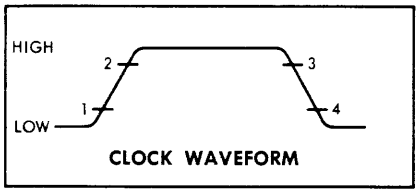
positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These J-K flip-flop circuits are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L78 Circuits	4.5	5	5.5	V
SN74L78 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 36)	200			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 37)	100			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 37)	100			ns
Input Setup Time, t_{setup} (See Figure 36)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			
Operating Free-Air Temperature Range, T_A: SN54L78 Circuits	−55	25	125	°C
SN74L78 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	29 and 30		2		V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal except clock	29 and 30			0.7	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at clock input terminal	29 and 30			0.6	V
$V_{out(1)}$	Logical 1 output voltage	29	V_{CC} = MIN, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	30	V_{CC} = MIN, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current at J or K	31	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(0)}$	Logical 0 level input current at preset	31	V_{CC} = MAX, V_{in} = 0.3 V		−0.36	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	31	V_{CC} = MAX, V_{in} = 0.3 V		−0.72	mA
$I_{in(1)}$	Logical 1 level input current at J or K	32	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
$I_{in(1)}$	Logical 1 level input current at preset	32	V_{CC} = MAX, V_{in} = 2.4 V		20	μA
			V_{CC} = MAX, V_{in} = 5.5 V		200	μA
$I_{in(1)}$	Logical 1 level input current at clear	32	V_{CC} = MAX, V_{in} = 2.4 V		40	μA
			V_{CC} = MAX, V_{in} = 5.5 V		400	μA
$I_{in(1)}$	Logical 1 level input current at clock	32	V_{CC} = MAX, V_{in} = 2.4 V	0§	−0.4§	mA
			V_{CC} = MAX, V_{in} = 5.5 V		400§	μA
I_{os}	Short-circuit output current	34	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
I_{CC}	Supply current (average per flip-flop)	32	V_{CC} = MAX, $V_{in(clock)}$ = 0		1.44	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

§For typical clock input current see page 8-47.

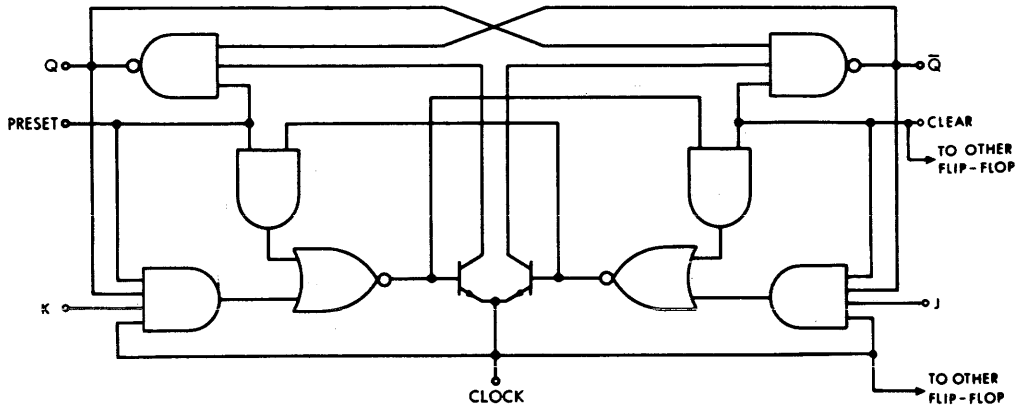
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	36	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{pd0}	Propagation delay time to logical 0 level from clear to output	37	C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 2.4 V		60	150	ns
			C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 0 V			200	ns
t_{pd1}	Propagation delay time to logical 1 level from clear to output	37	C_L = 50 pF, R_L = 4 kΩ		35	75	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	60	150	ns

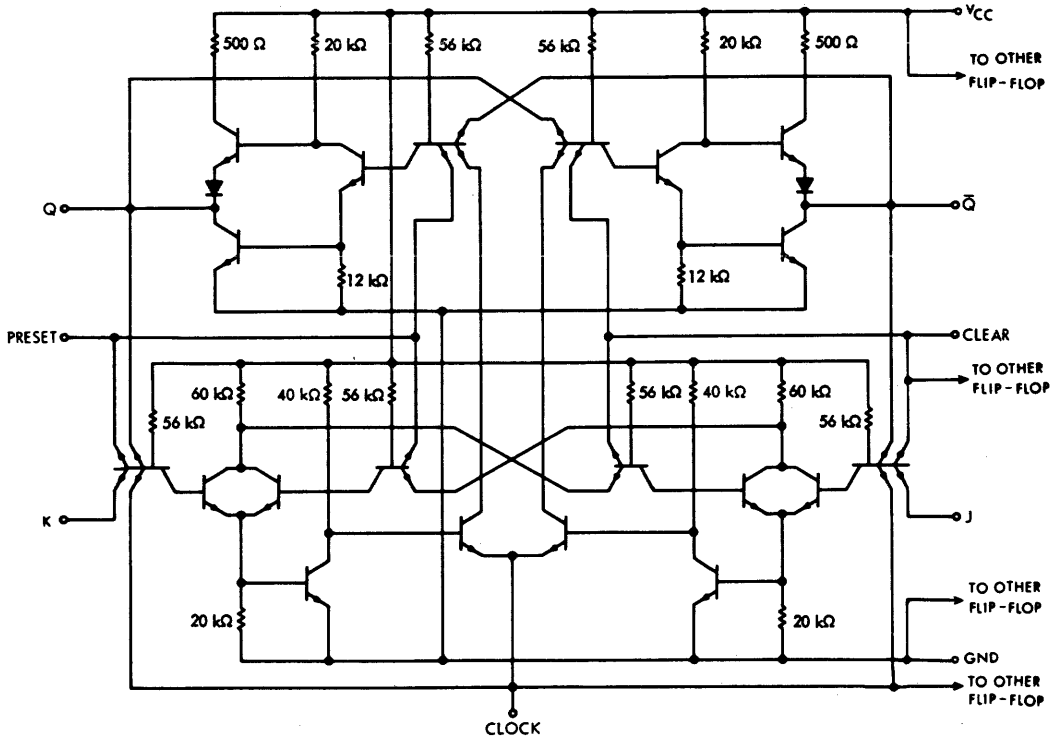
8

CIRCUIT TYPES SN54L78, SN74L78
DUAL J-K MASTER-SLAVE FLIP-FLOPS

functional block diagram (each flip-flop)



schematic (each flip-flop)



Component values shown are nominal.

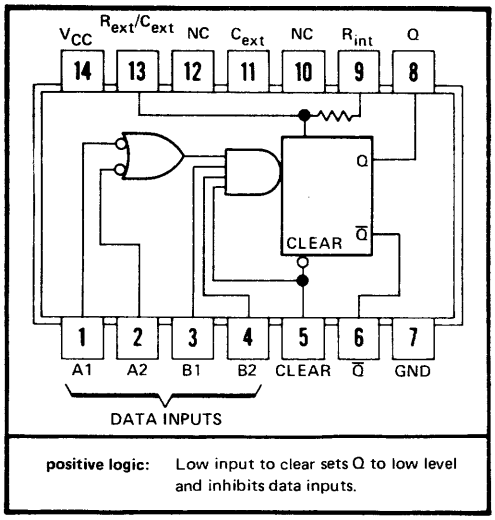
CIRCUIT TYPES SN54L122, SN74L122
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- D-C Triggered from High- or Low-Level Gated Logic inputs
- Typical Power Dissipation, 50% Duty Cycle . . . . 55 mW
- Typical Average Propagation Delay to Output Q . . . . 40 ns
- Diode-Clamped Inputs
- Fully Compatible with Most TTL and DTL Circuits

TRUTH TABLE
(See Note A)

INPUTS				OUTPUTS	
A1	A2	B1	B2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎏
L	X	H	↑	⎍	⎏
X	L	H	H	L	H
X	L	↑	H	⎍	⎏
X	L	H	↑	⎍	⎏
H	↓	H	H	⎍	⎏
↓	↓	H	H	⎍	⎏
↓	H	H	H	⎍	⎏

J OR N DUAL-IN-LINE OR
T FLAT PACKAGE (TOP VIEW)†
(See Note B thru F)



†Pin assignments for these circuits are the same for all packages.

NOTES: A. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎏ = one low-level pulse, X = irrelevant (any input, including transitions).
B. NC = no internal connection.
C. To use the internal timing resistor of SN54L122/SN74L122 (20 kΩ), connect R_{int} to V_{CC}.
D. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
E. For accurate repeatable pulse widths, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
F. To obtain variable pulse width, connect external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.

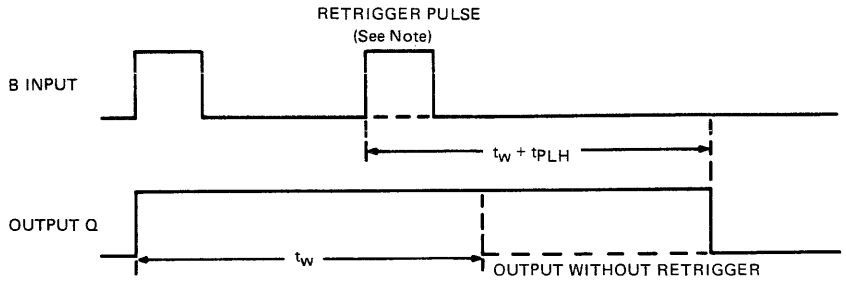
8

CIRCUIT TYPES SN54L122, SN74L122
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

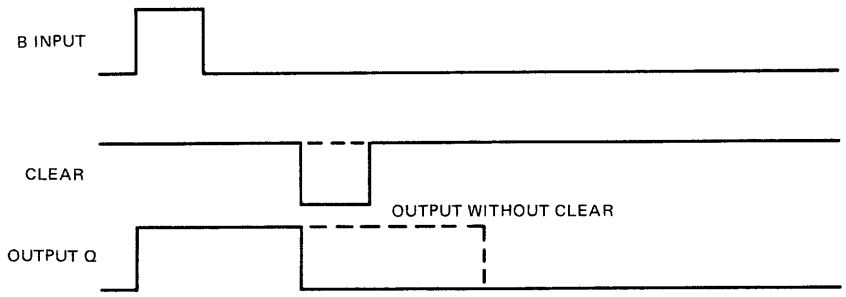
description

These monolithic TTL retriggerable monostable multivibrators feature d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. A full fan-out to 40 normalized Series 54L/74L gate loads is available from each of the outputs. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C.

Figure A below illustrates triggering the one-shot with the high-level-active (B) inputs.



OUTPUT PULSE CONTROL USING RETRIGGER PULSE



OUTPUT PULSE CONTROL USING CLEAR INPUT

FIGURE A–TYPICAL INPUT/OUTPUT PULSES

NOTE: Retrigger pulse must not start before 0.22 C_{ext} (in picofarads) nanoseconds after previous trigger pulse.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

description (continued)

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. The SN54L122/SN74L122 has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse width (t_w) is defined as:

$$t_w = 0.32\ R_T C_{ext} \left(1 + \frac{0.7}{R_T}\right)$$

where

R_T is in kΩ (either internal or external timing resistor)
C_{ext} is in pF
t_w is in ns

For pulse widths when $C_{ext} \leq 1000$ pF, see Figure 2.

These circuits are fully compatible with most TTL or DTL families. Inputs are diode-clamped to minimize reflections due to transmission-line effects, which simplifies design. Typical power dissipation per one-shot is 55 milliwatts; typical average propagation delay time to the Q output is 40 nanoseconds. The SN54L122 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L122 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage, SN54L122 Circuits only (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54L122 Circuits . . . . . −55°C to 125°C
SN74L122 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

8

			SN54L122			SN74L122			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	Series 54L/74L Gates				40			40	
	Series 54L/74L Gates with 8-kΩ base resistors¶	High logic level			20			20	
		Low logic level			10			10	
Input data setup time, t_{setup} (see Note 3 and Figure 1)			50			50			ns
Input data hold time, t_{hold} (see Note 4 and Figure 1)			50			50			ns
Width of clear pulse, $t_{w(clear)}$			50			50			ns
External timing resistance			5		25	5		50	kΩ
External capacitance			No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal					50			50	pF
Operating free-air temperature, T_A			−55		125	0		70	°C

¶This applies for all data inputs of circuit types SN54L122 and SN74L122.

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For the SN54L122/SN74L122 circuit, this rating applies to each A input with respect to the other and to each B input with respect to the other.
3. Setup time for a dynamic input is the interval immediately preceding the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure recognition of the transition.
4. Hold time for a dynamic input is the interval immediately following the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure continued recognition of the transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, See Note 5	I_{OH} = −400 μA,	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, See Note 5	I_{OL} = 8 mA,			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	data inputs	V_{CC} = MAX,	V_I = 2.4 V			20	μA
		clear input					40	
I_{IL}	Low-level input current	data inputs	V_{CC} = MAX,	V_I = 0.4 V			−0.8	mA
		clear input					−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX,	See Note 5	−5		−2.0	mA
I_{CC}	Supply current (quiescent or triggered)		V_{CC} = MAX,	See Notes 6 and 7		11	14	mA

†For conditions shown as MIN or MAX, use the value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

NOTES: 5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
6. Quiescent I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} is open.
7. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} is open.

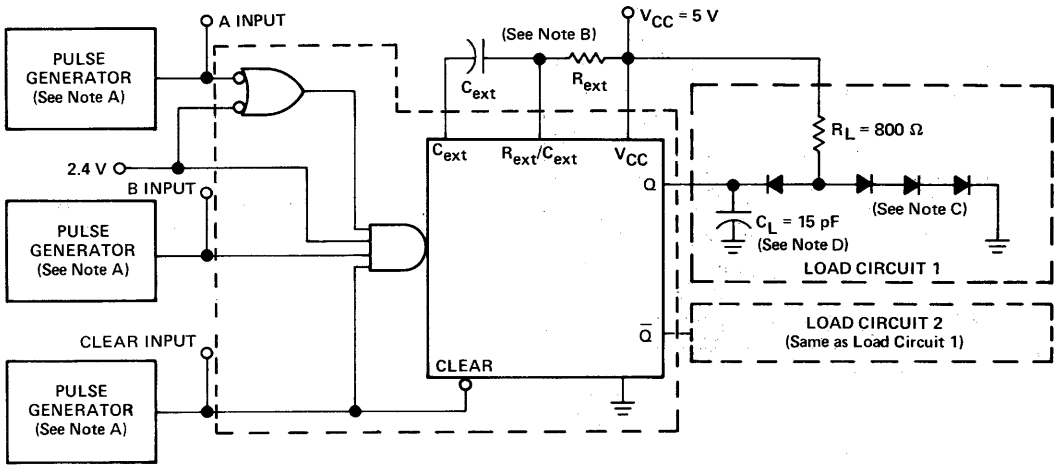
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either A input	C_{ext} = 0, C_L = 15 pF, See Figure 1	R_{ext} = 5 kΩ, R_L = 800 Ω,		44	66	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either B input				38	56	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either A input				60	80	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either B input				54	72	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output, from clear input				36	54	ns
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}$ output, from clear input				60	80	ns
$t_{w(min)}$	Minimum width of Q output pulse				90	130	ns
t_w	Width of Q output pulse	C_{ext} = 400 pF, C_L = 15 pF,	R_{ext} = 10 kΩ, R_L = 800 Ω	1.7	1.9	2.1	μs

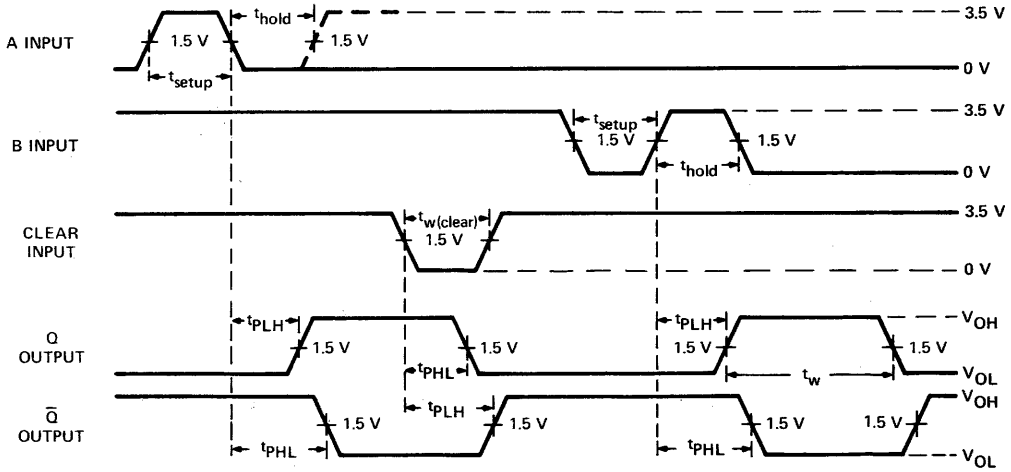
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $t_r \leq 10$ ns (10% to 90% level), $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$.
B. See Test Conditions, switching characteristics table, page 3, for values of R_{ext} and C_{ext}.
C. All diodes are 1N916.
D. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES

8

TYPICAL CHARACTERISTICS

OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE

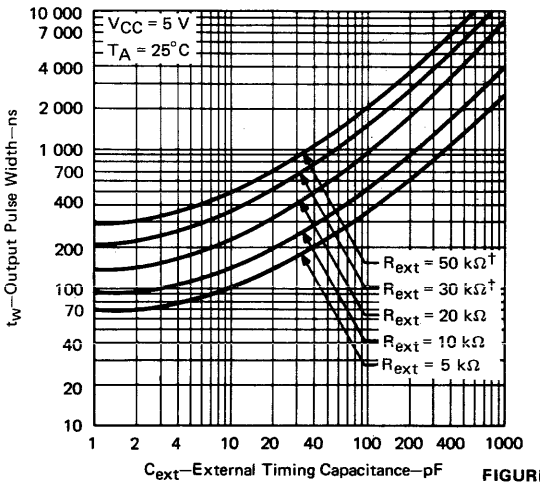
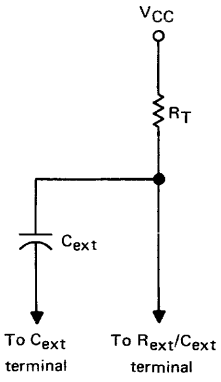


FIGURE 2

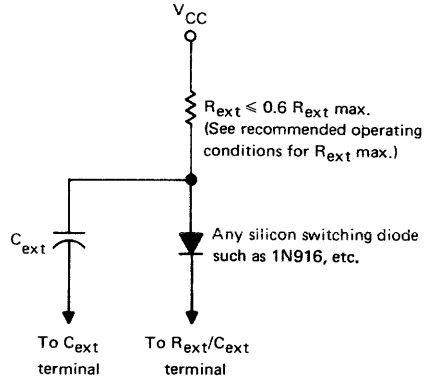
†These values of resistance exceed the maximums recommended for use over the full temperature range of the SN54L122.

TYPICAL APPLICATION DATA



TIMING COMPONENT CONNECTIONS WHEN $C_{ext} \leq$ 1000 pF

FIGURE B



TIMING COMPONENT CONNECTIONS WHEN C_{ext} > 1000 pF AND CLEAR IS USED

FIGURE C

To prevent reverse voltage across C_{ext}, it is recommended that the method shown in Figure C be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse width is:

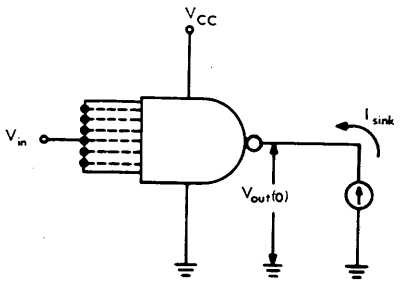
$$t_w = 0.28\ R_{ext}C_{ext}\left(1 + \frac{0.7}{R_{ext}}\right)$$

where

R_{ext} is in kΩ
C_{ext} is in pF
t_w is in ns

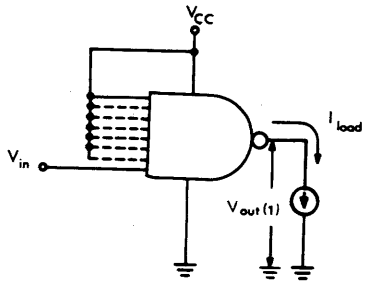
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



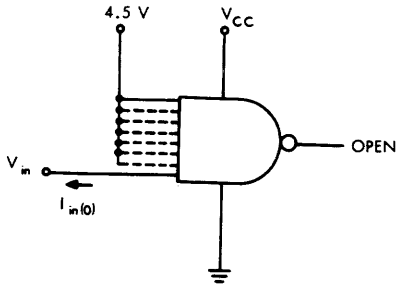
1. All inputs are tested simultaneously.

FIGURE 1



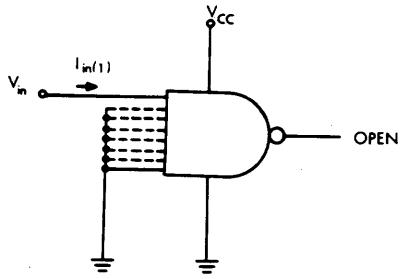
1. Each input is tested separately.

FIGURE 2



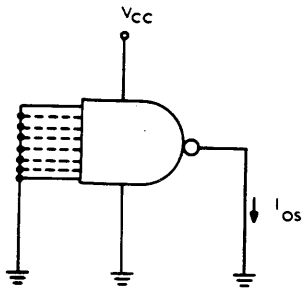
1. Each input is tested separately.

FIGURE 3



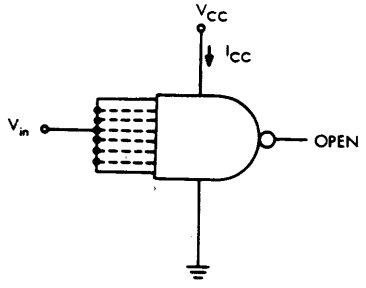
1. Each input is tested separately.

FIGURE 4



1. Each gate is tested separately.

FIGURE 5



1. Logical 0 and logical 1 conditions are tested.
2. All gates are tested simultaneously.

$$\text{Average-per-gate value} = \frac{I_{CC}\ \text{total}}{\text{number of gates in package}}.$$

FIGURE 6

§Arrows indicate actual direction of current flow.

8

PARAMETER MEASUREMENT INFORMATION

d-c test circuits §

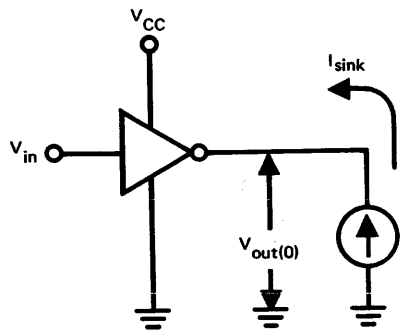


FIGURE 7

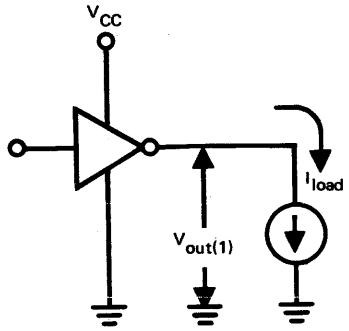


FIGURE 8

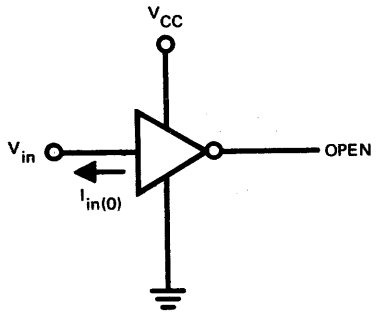


FIGURE 9

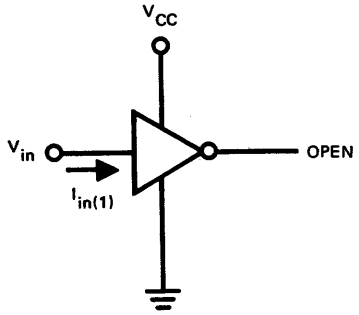
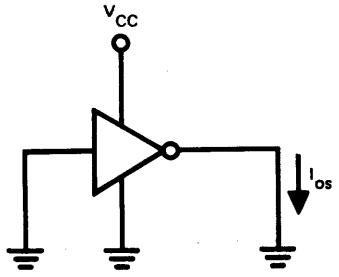
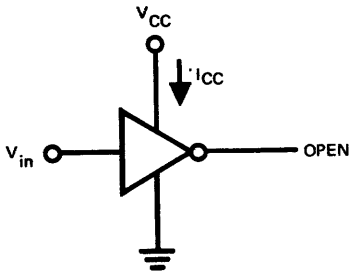


FIGURE 10



1. Each inverter is tested separately.

FIGURE 11



1. All inverters are tested simultaneously.
2. For SN54L04/SN74L04 the average-per-inverter value = $\frac{I_{CC}\ \text{total}}{\text{number of inverters in package}}$

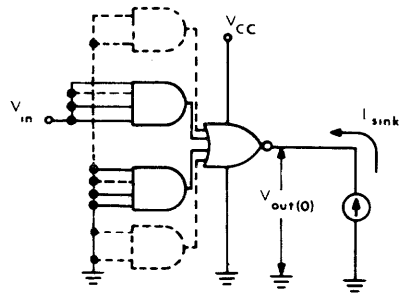
FIGURE 12

§ Arrows indicate actual direction of current flow.

8

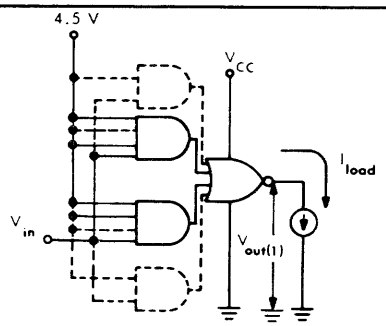
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



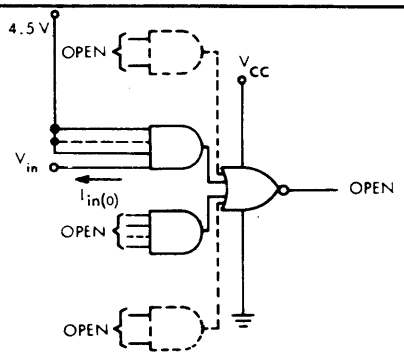
1. Each AND section is tested separately.

FIGURE 13



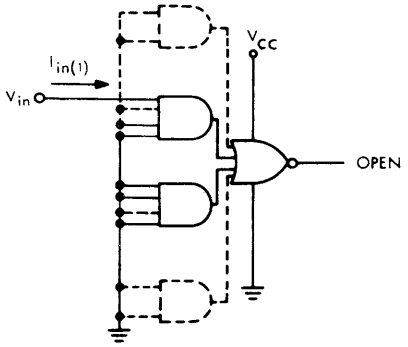
1. Each set of inputs is tested separately.

FIGURE 14



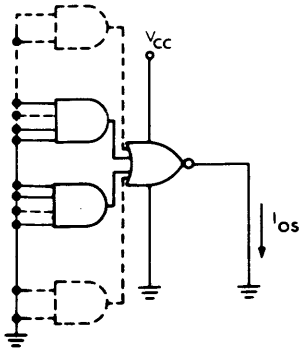
1. Each input is tested separately.

FIGURE 15



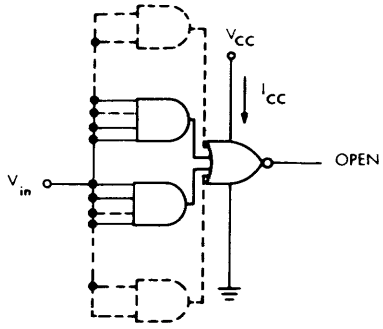
1. Each input is tested separately.

FIGURE 16



1. Each gate is tested separately.

FIGURE 17



1. All gates are tested simultaneously.

$$\text{Average-per-gate value} = \frac{I_{CC\ total}}{\text{number of gates in package}}$$

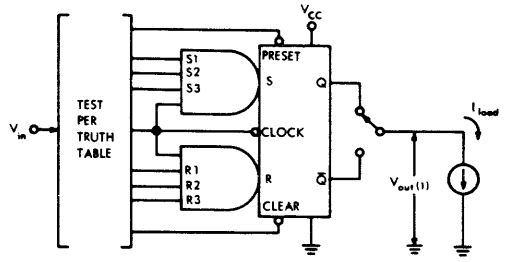
FIGURE 18

§Arrows indicate actual direction of current flow.

8

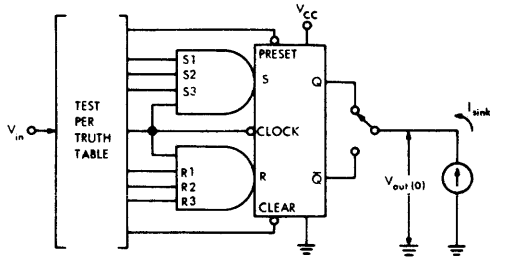
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



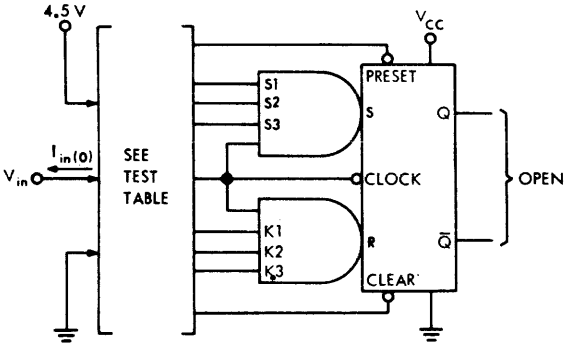
1. Each output is tested separately.

FIGURE 19



1. Each input is tested separately.

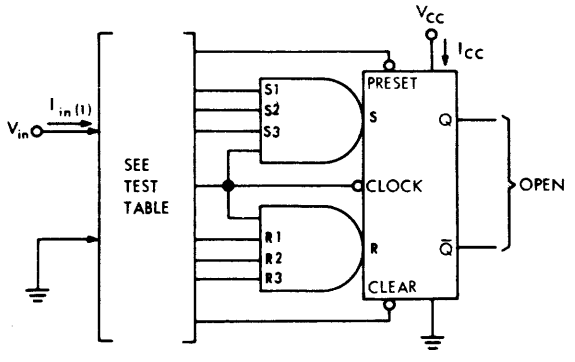
FIGURE 20



TEST TABLE	
Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V
Clock	Preset, R1, R2, R3, S1, S2, and S3
Clock	Clear, R1, R2, R3, S1, S2, and S3
Preset	R1, R2, R3, S1, S2, and S3
Clear	R1, R2, R3, S1, S2, and S3
R1	Preset, Clock, R2, and R3
R2	Preset, Clock, R1, and R3
R3	Preset, Clock, R1, and R2
S1	Clear, Clock, S2, and S3
S2	Clear, Clock, S1, and S3
S3	Clear, Clock, S1, and S2

1. Each input is tested separately.

FIGURE 21



TEST TABLE	
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, R1, R2, R3, S1, S2, and S3
Preset	Clock, R1, R2, and R3
Clear	Clock, S1, S2, and S3
R1	Clock, Preset, R2, and R3
R2	Clock, Preset, R1, and R3
R3	Clock, Preset, R1, and R2
S1	Clock, Clear, S2, and S3
S2	Clock, Clear, S1, and S3
S3	Clock, Clear, S1, and S2

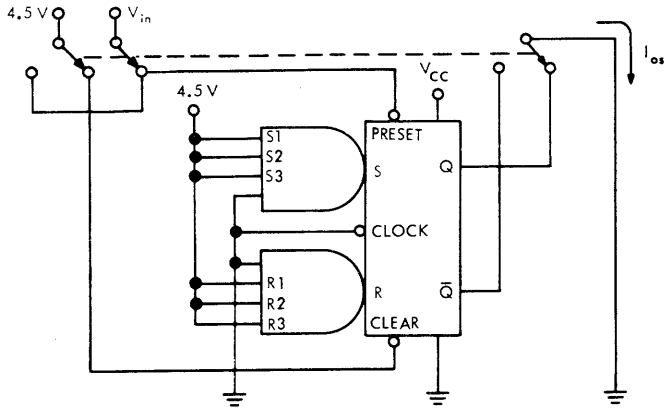
1. Each input is tested separately.

FIGURE 22

§Arrows indicate actual direction of current flow.

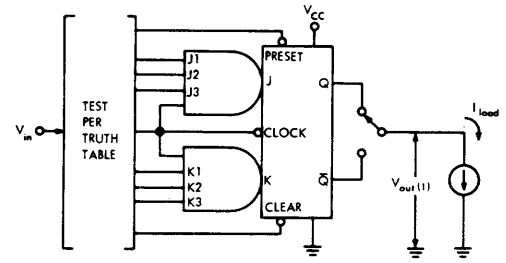
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



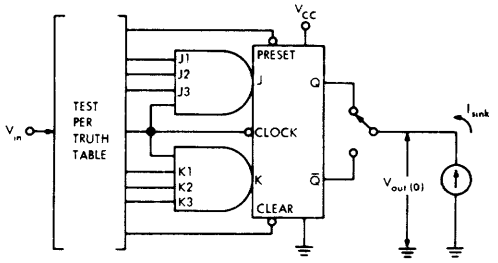
1. Each output is tested separately.

FIGURE 23



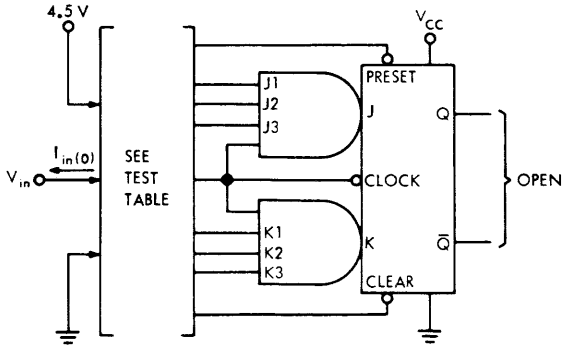
1. Each output is tested separately.

FIGURE 24



1. Each output is tested separately.

FIGURE 25



TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND, then 4.5 V	Apply 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

1. Each input is tested separately.

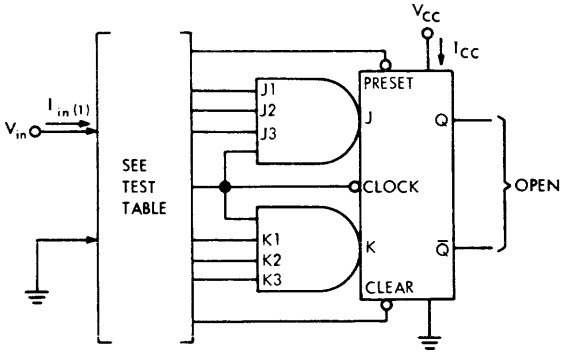
FIGURE 26

§Arrows indicate actual direction of current flow.

8

PARAMETER MEASUREMENT INFORMATION

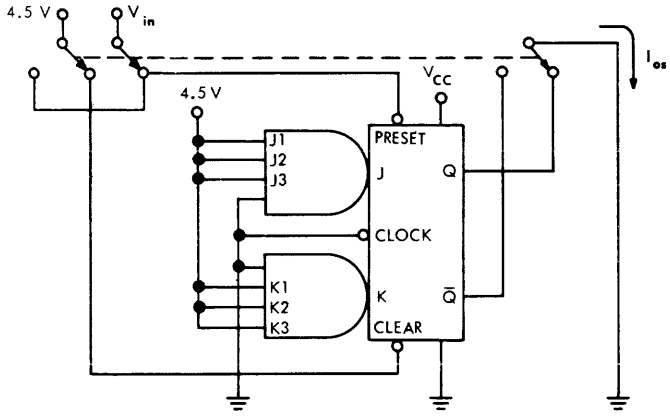
d-c test circuits § (continued)



TEST TABLE	
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2, and K3
Clear	Clock, J1, J2, and J3
J1	Clock, Clear, J2, and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

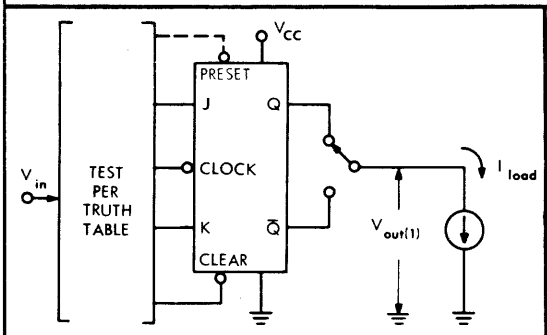
1. Each input is tested separately.

FIGURE 27



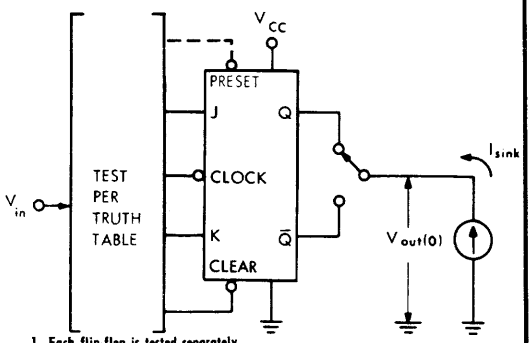
1. Each output is tested separately.

FIGURE 28



1. Each flip-flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for SN54L78/SN74L78 circuits only.

FIGURE 29



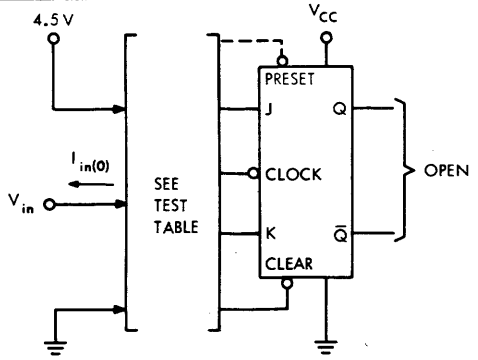
1. Each flip-flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for SN54L78/SN74L78 circuits only.

FIGURE 30

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

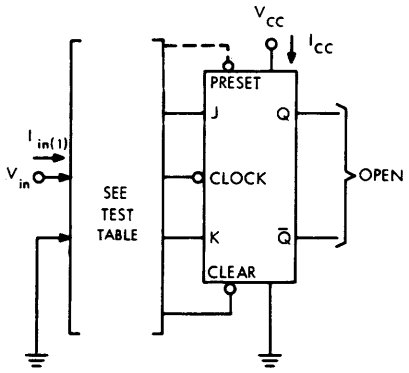
d-c test circuits§ (continued)



TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
Preset	None (See Note 5)	Clock and K
J	Q (See Note 3)	Clock and Clear
K	$\overline{Q}$ (See Note 3)	Clock and Clear

1. Each flip-flop is tested separately.
2. Apply momentary ground, then 4.5 V.
3. After application of momentary ground, Q and $\overline{Q}$ are left floating.
4. Ground all inputs of the unused flip-flop.
5. Preset is applicable for SN54L78/SN74L78 circuits only.

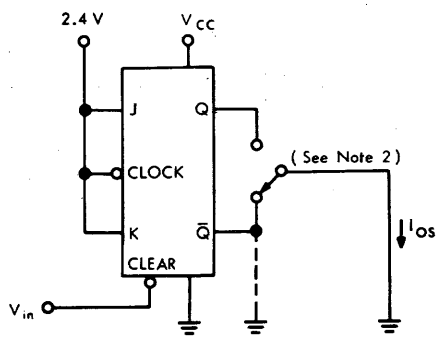
FIGURE 31



TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
Preset (See Note 1)	Clock and K	None
J (See Note 1)	Clock and Clear	Preset
K (See Note 3)	Clock and Preset	Clear

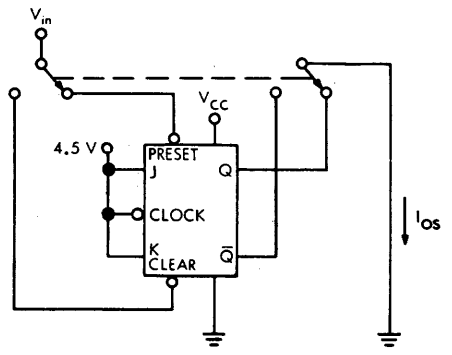
1. Preset is applicable for SN54L78/SN74L78 circuits only.
2. I_{CC} is measured (simultaneously for both flip-flops) for the following conditions:
   a. J = K = Clock = Clear = Gnd. For SN54L78/SN74L78, Preset = 4.5 V.
   b. For SN54L73/SN74L73: J = Clear = 4.5 V, K = Gnd, and apply momentary 4.5 V, then Gnd, to Clock.
   For SN54L78/SN74L78: J = K = Clock = Preset = Gnd and Clear = 4.5 V.
   Average per flip-flop = $\frac{I_{CC\ total}}{2}$.
3. Each flip-flop is tested separately for $I_{in(1)}$

FIGURE 32



1. Each flip-flop is tested separately.
2. Test circuit shows setup for testing $\overline{Q}$. When testing Q, open all inputs and ground $\overline{Q}$.

FIGURE 33



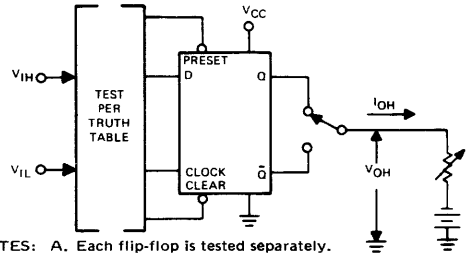
1. Each flip-flop is tested separately.

FIGURE 34

8

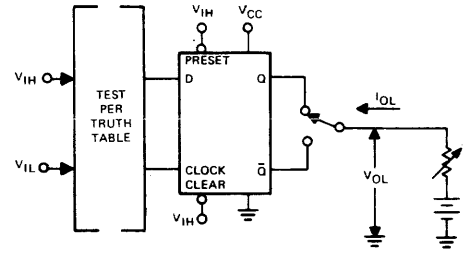
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



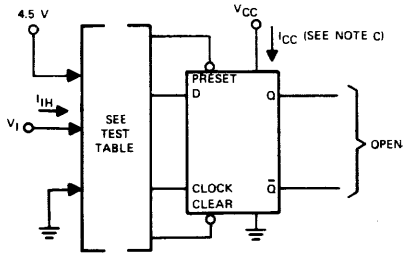
NOTES: A. Each flip-flop is tested separately.
B. Each output is tested separately.
C. V_{OH} is also tested using Clear and Preset inputs.

FIGURE 35–V_{IH}, V_{IL}, V_{OH}



NOTES: A. Each flip-flop is tested separately.
B. Each output is tested separately.

FIGURE 36–V_{IH}, V_{IL}, V_{OL}



TEST TABLE

APPLY V_I (TEST I_{IH})	APPLY 4.5 V	APPLY GND
Clock	Clear and D	Preset
Clock	Preset and D	Clear
Preset	Clear and D	Clock (See Note B)
Clear	Preset	Clock, D, and Q
Clear	Preset	D and Clock (See Note B)
D	Preset and Clock	Clear

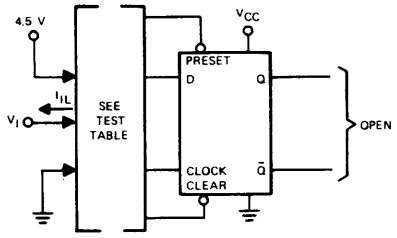
NOTES: A. Each input of each flip-flop is tested separately for I_{IH}.
B. GND is momentarily applied to Clock, then 4.5 V.
C. I_{CC} is measured simultaneously for both flip-flops with D, Clock, and Preset at GND; then with D, Clock, and Clear at GND.

FIGURE 37–I_{IH}, I_{CC}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



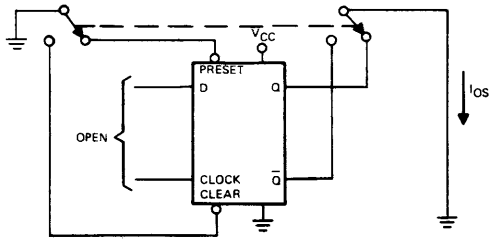
TEST TABLE

APPLY V_I (TEST I_{IL})	APPLY 4.5 V	APPLY GND
Clock	Clear	Preset and D
Preset	Clear	Clock and D
Clear	Clock, D, and Preset	None
D	Clear and Clock	Preset

NOTES: A. Each flip-flop is tested separately.
B. Each input is tested separately.

FIGURE 38–I_{IL}

8



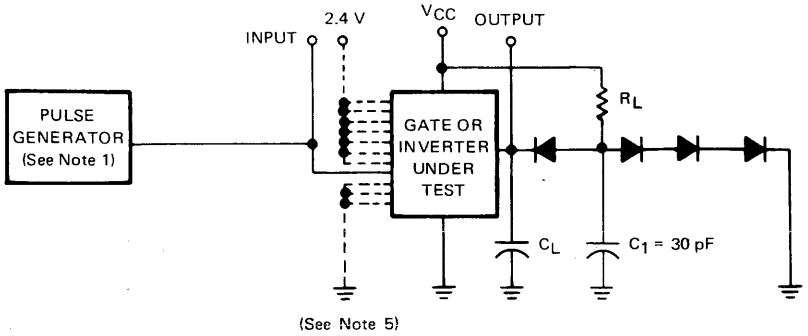
NOTE: Each output is tested separately.

FIGURE 39–I_{OS}

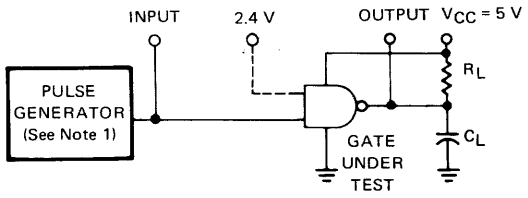
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

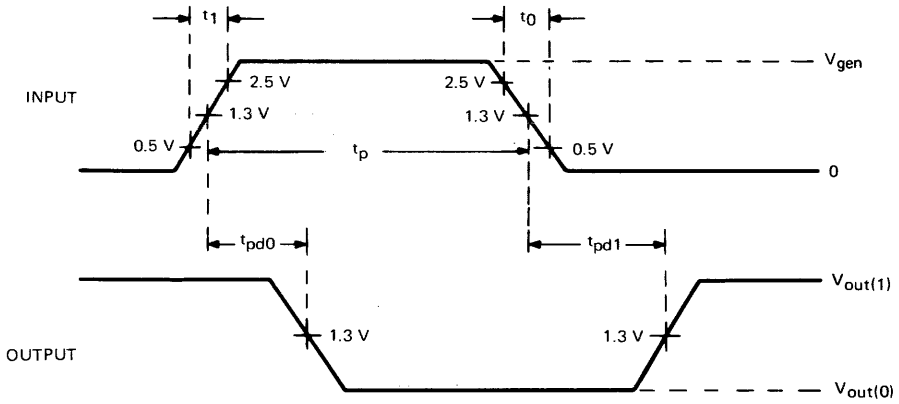
switching characteristics



TEST CIRCUIT FOR SN54L00, SN54L02, SN54L04, SN54L10, SN54L20, SN54L30, SN54L51, SN54L54, SN54L55, SN74L00, SN74L02, SN74L04, SN74L10, SN74L20, SN74L30, SN74L51, SN74L54, AND SN74L55



TEST CIRCUIT FOR SN54L01, SN54L03, SN74L01, SN74L03



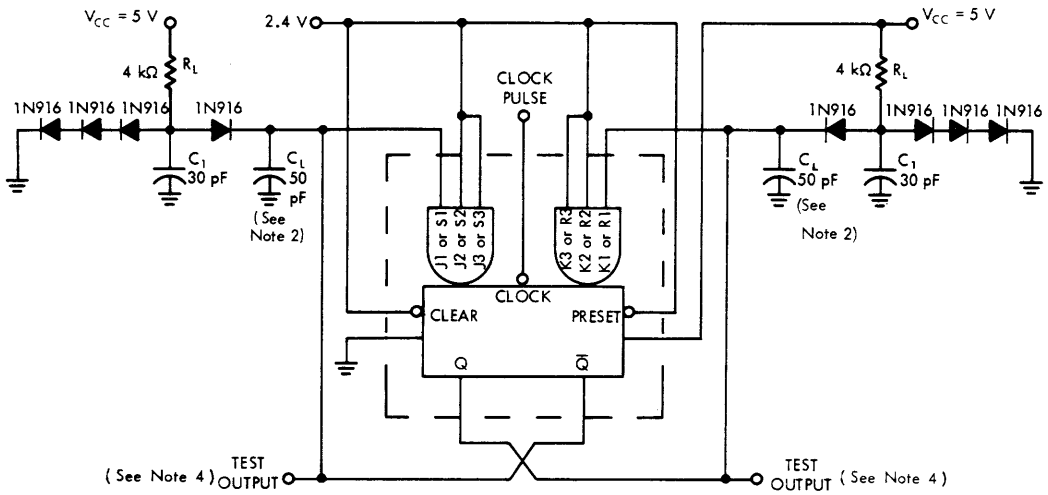
VOLTAGE WAVEFORMS

NOTES:
1. The generator has the following characteristic: V_{gen} = 3 V, t_0 = 60 ns, t_1 = 60 ns, t_p = 1 μs, PRR ≤ 500 kHz, Z_{out} ≈ 50 Ω.
2. All diodes are 1N916 or equivalent.
3. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
4. C_L includes probe and jig capacitance.
5. When testing the SN54L00/SN74L00 through SN54L30/SN74L30 (except SN54L02/SN74L02), connect all unused inputs to 2.4 V. When testing the SN54L02/SN74L02 or SN54L51/SN74L51 through SN54L55/SN74L55, apply the input pulse to one input of one AND section and 2.4 V to all unused inputs of that AND section. All inputs of unused AND sections are grounded.

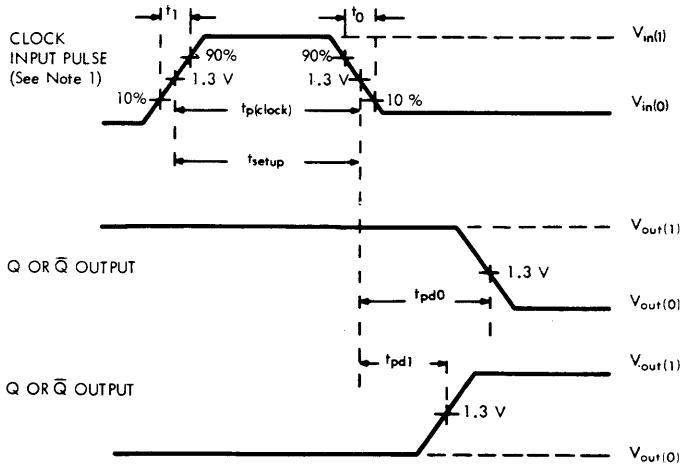
FIGURE 40–GATE PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

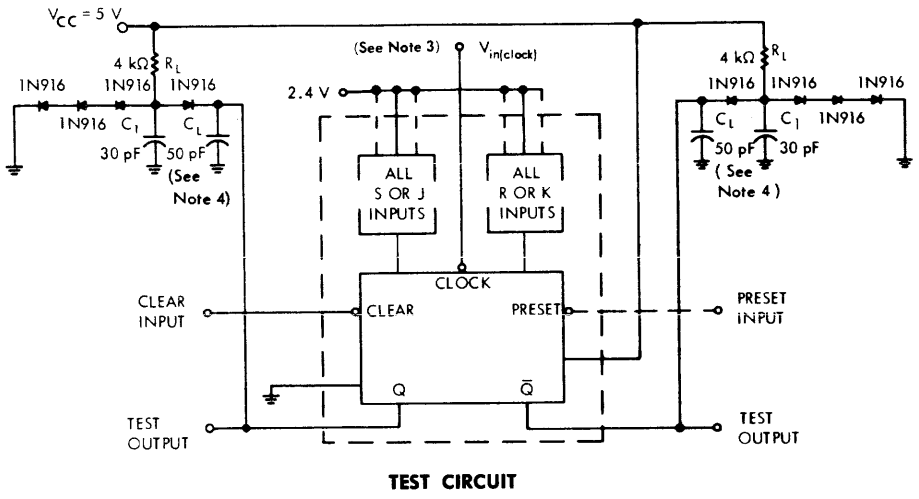
NOTES: 1. Clock input characteristics: $V_{in(0)} \leq 0.4$ V, $V_{in(1)} \geq 2.4$ V, $t_1 = t_0 = 15$ ns, $t_p \geq 200$ ns, and PRR = 500 kHz. When testing f_{max}, vary PRR.
2. C_L includes probe and jig capacitance.
3. For SN54L73/SN74L73 and SN54L78/SN74L78, J = K = 2.4 V.
4. Load is applied only to output under test.

FIGURE 41—FLIP-FLOP CIRCUITS SYNCHRONOUS INPUTS SWITCHING TIMES

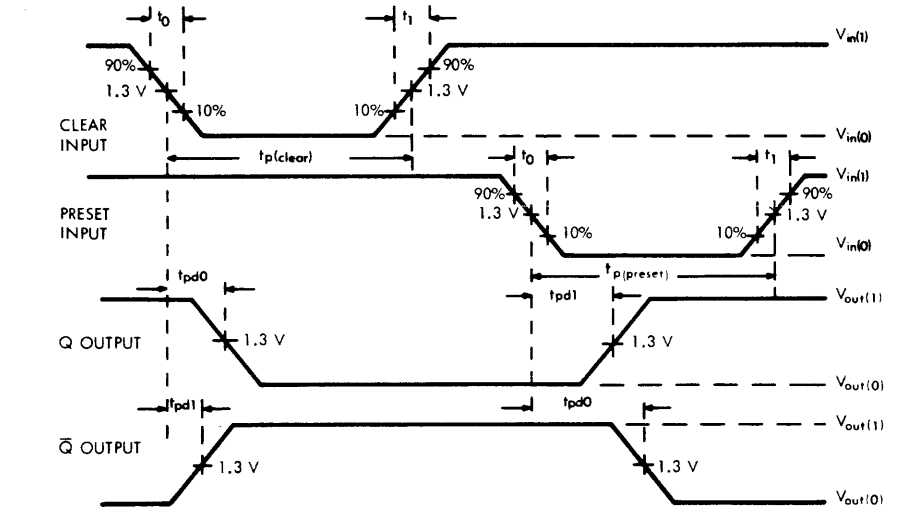
8

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



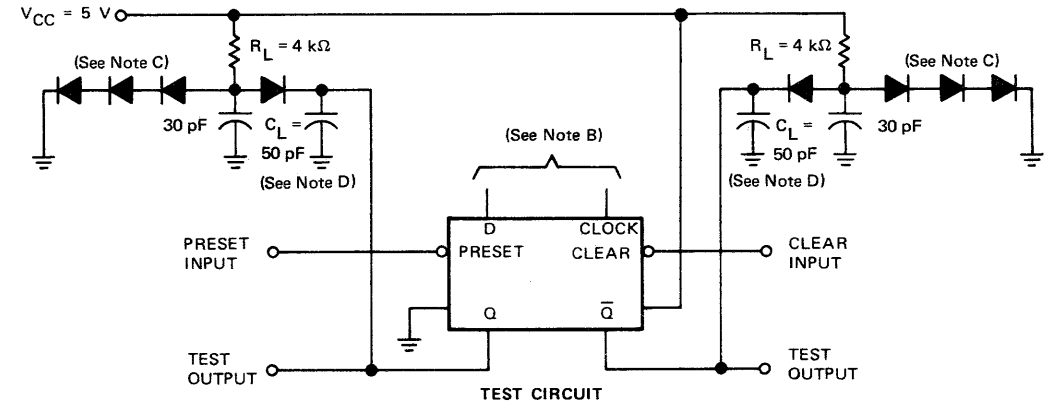
VOLTAGE WAVEFORMS

NOTES: 1. Clear or preset inputs dominate regardless of the state of clock or logic inputs.
2. Clear or preset input pulse characteristics: $V_{in(0)} \leq 0.4$ V, $V_{in(1)} \geq 2.4$ V, $t_1 = t_0 = 15$ ns, $t_{p(clear)} = t_{p(preset)} \geq 100$ ns, and PRR $\leq$ 500 kHz.
3. See applicable circuit type for actual synchronous and asynchronous input configurations.
4. C_L includes probe and jig capacitance.

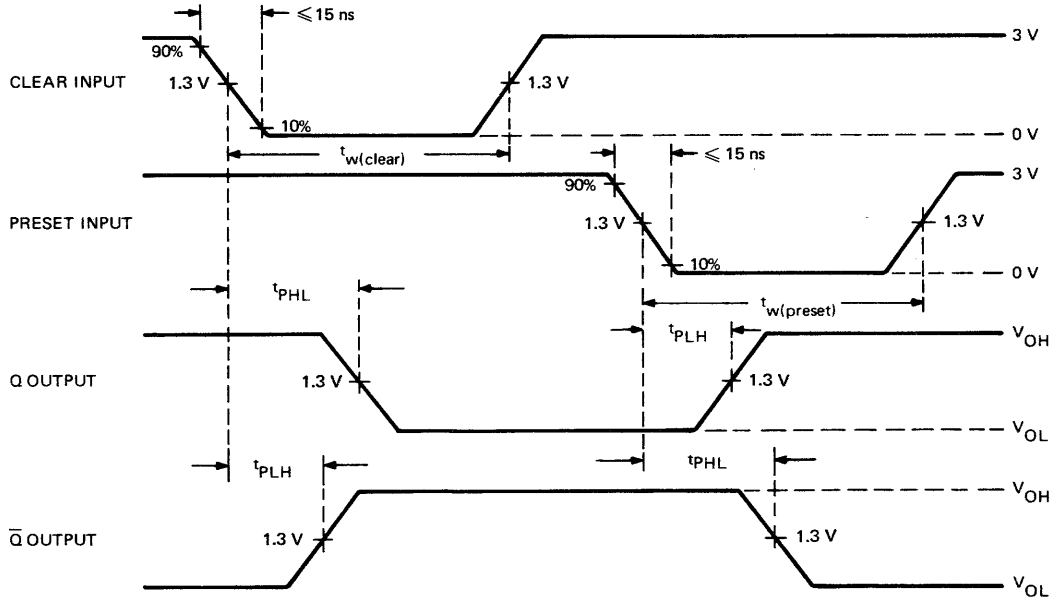
FIGURE 42—FLIP-FLOP CIRCUITS ASYNCHRONOUS INPUTS SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

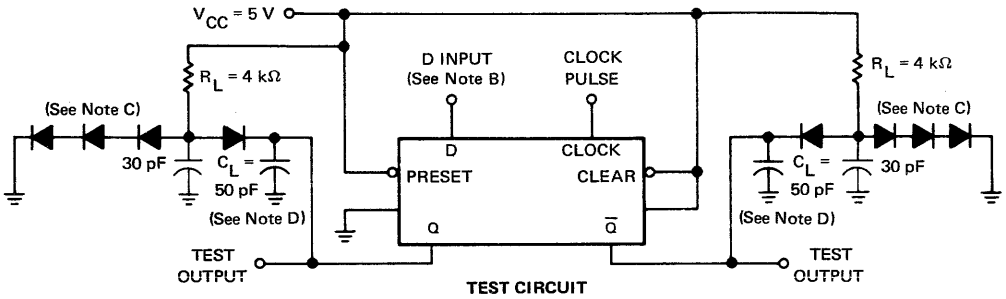
NOTES: A. Clear or Preset input pulse characteristics: $t_{w(clear)} = t_{w(preset)} \geq 100$ ns, PRR ≤ 500 kHz.
B. Clear and Preset inputs dominate regardless of the state of Clock or D inputs.
C. All diodes are 1N916.
D. C_L includes probe and jig capacitance.

FIGURE 43—ASYNCHRONOUS INPUTS SWITCHING CHARACTERISTICS

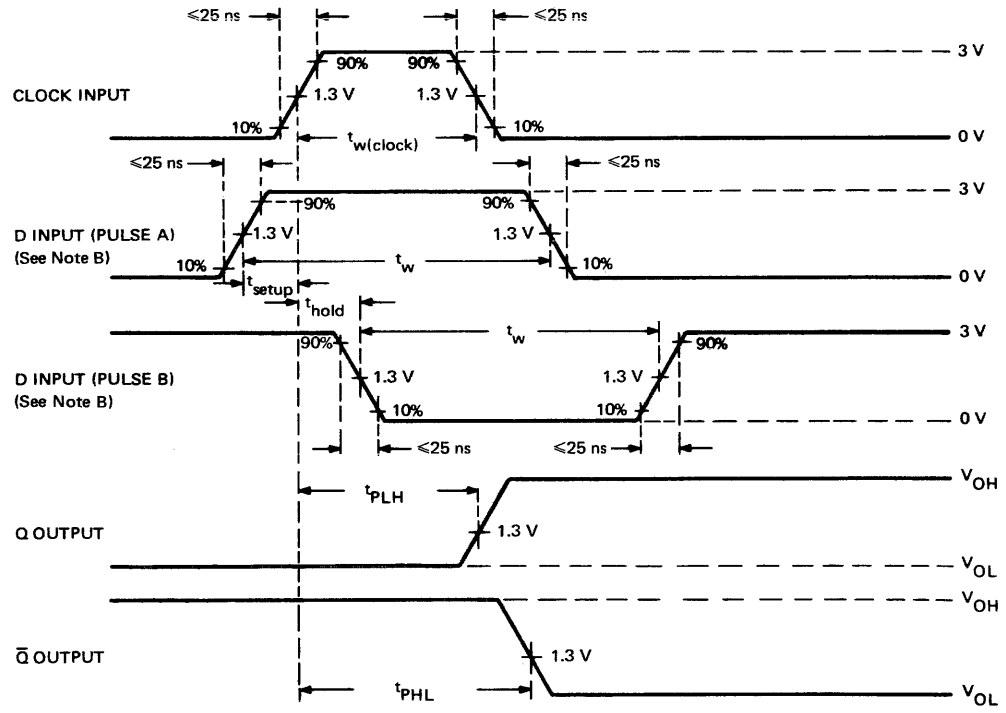
8

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



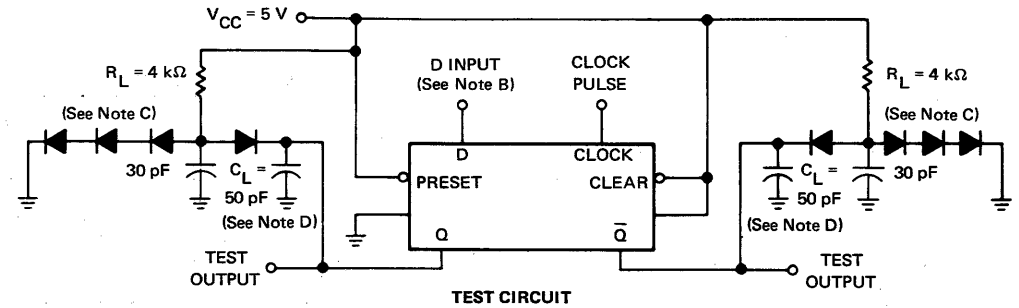
VOLTAGE WAVEFORMS

NOTES: A. Clock input pulse has the following characteristics: $t_{w(clock)} \geq 200$ ns and PRR $\leq$ 500 kHz. When testing f_{max}, vary PRR.
B. D input (pulse A) has the following characteristics: t_{setup} = 30 ns, t_w = 100 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 0 ns, t_w = 80 ns, and PRR is 50% of the clock PRR.
C. All diodes are 1N916.
D. C_L includes probe and jig capacitance.

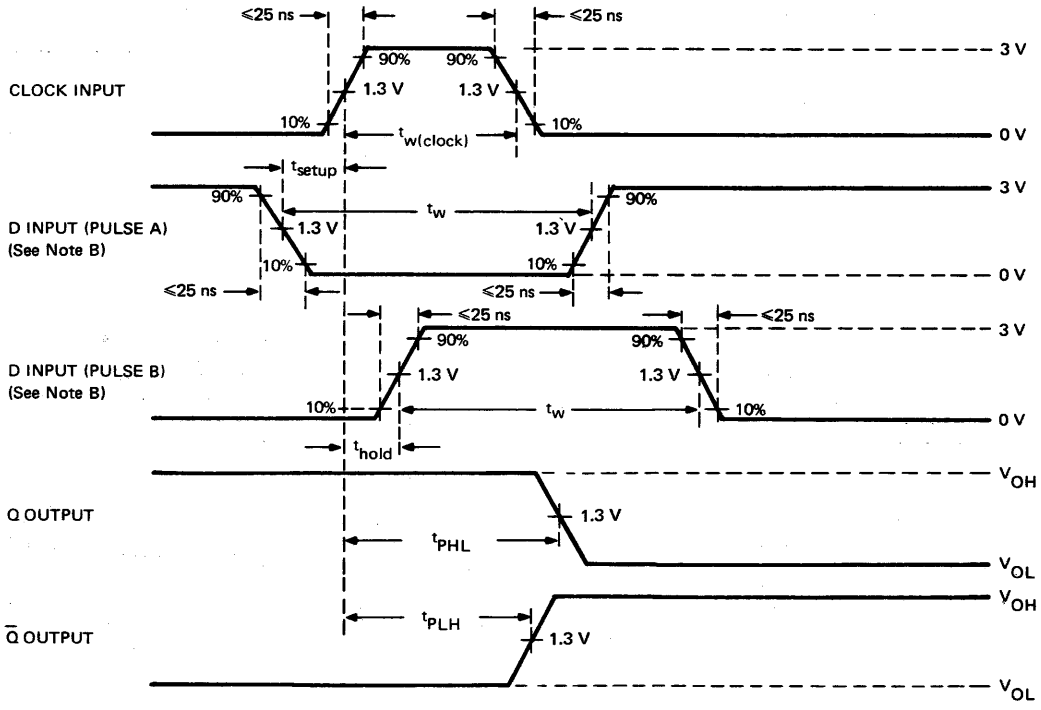
FIGURE 44–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS (HIGH-LEVEL DATA)

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

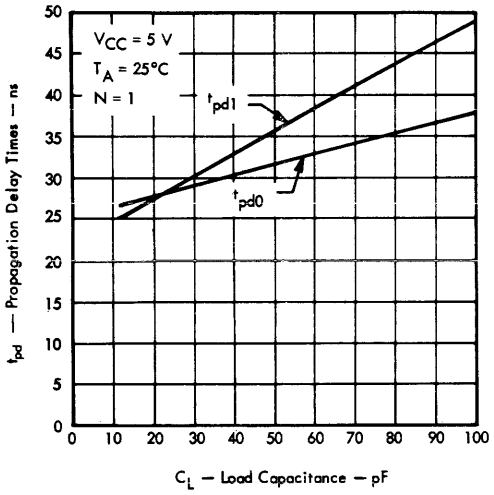
NOTES: A. Clock input pulse has the following characteristics: $t_w \geq 200$ ns and PRR ≤ 500 kHz. When testing f_{max}, vary PRR.
B. D input (pulse A) has the following characteristics: t_{setup} = 30 ns, t_w = 100 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 0 ns, t_w = 80 ns, and PRR is 50% of the clock PRR.
C. All diodes are 1N916.
D. C_L includes probe and jig capacitance.

FIGURE 45–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS (LOW-LEVEL DATA)

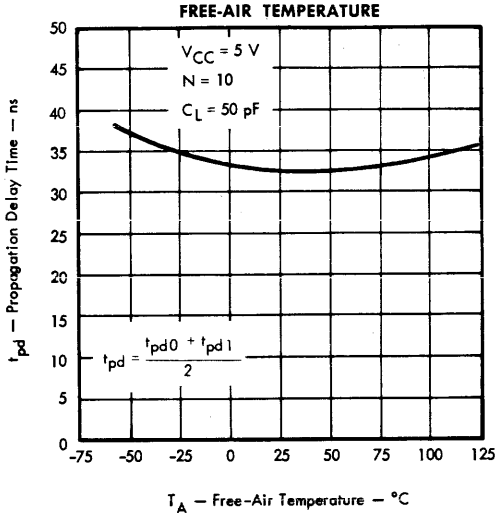
8

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

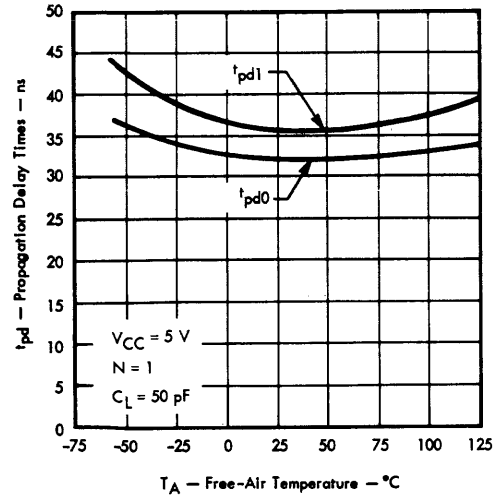


PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

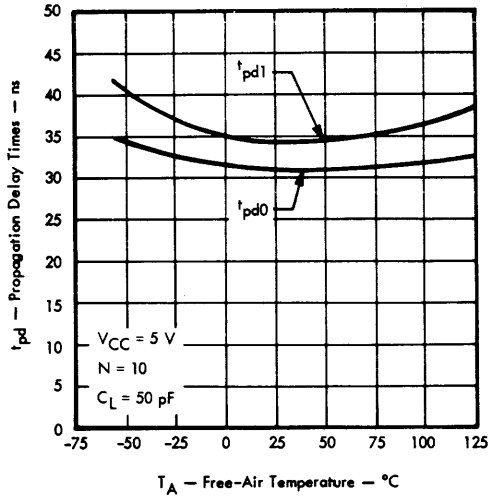


8

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE



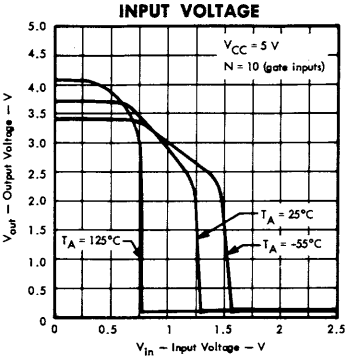
PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE



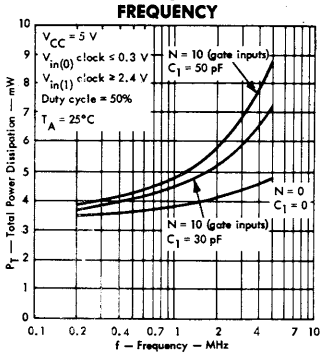
†SN54L00/SN74L00, SN54L10/SN74L10, and SN54L20/SN74L20. Data for temperatures below 0°C and above 70°C is applicable to Series 54L circuits only.

TYPICAL CHARACTERISTICS†

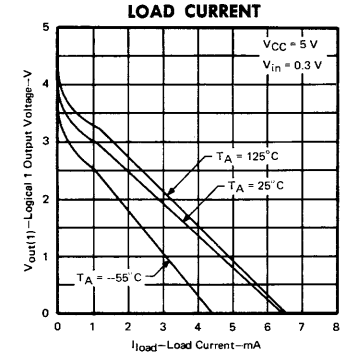
OUTPUT VOLTAGE vs INPUT VOLTAGE



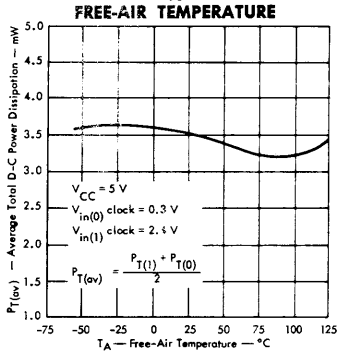
TOTAL POWER DISSIPATION‡ vs FREQUENCY



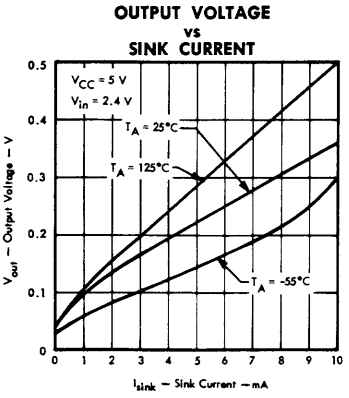
OUTPUT VOLTAGE vs LOAD CURRENT



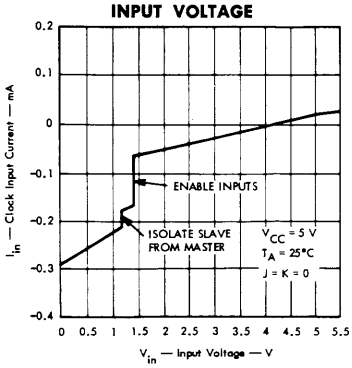
AVERAGE TOTAL D-C POWER DISSIPATION‡ § vs FREE-AIR TEMPERATURE



OUTPUT VOLTAGE vs SINK CURRENT



CLOCK INPUT CURRENT ‡ § vs INPUT VOLTAGE



† Data for temperatures below 0°C and above 70°C is applicable to Series 54L circuits only.

‡Each flip-flop.
§Value of I_{in} for SN54L78 and SN74L78 is twice the amount shown.

8

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TTL MSI Circuits

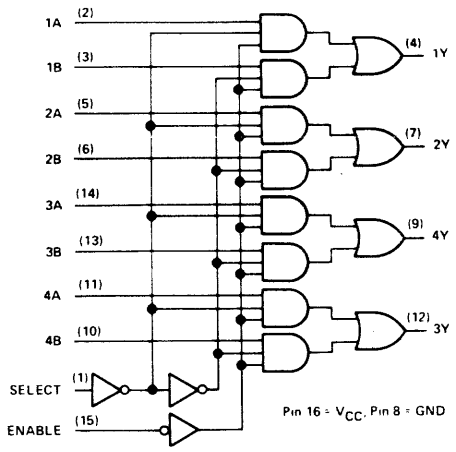
New TTL/MSI Now Available

SN54/74157 Quad 2-Line-To-1-Line Data Selector/Multiplexer With Strobe Control

- Pin-for-pin replacement for 9322-type multiplexers
- Selects bused data from one of two sources
- Ideal for controlling accumulator inputs
- Use to expand any data input point
- Generates four functions of two variables (one variable is common)
- Source programmable counters

LOGIC

SN54/74157



Pin (16) = V_{CC}, Pin (8) = GND

TYPICAL POWER: 125 mW
TYPICAL PROPAPATION DELAY
TIME 20 ns (SELECT TO OUTPUT)

Available in 16-pin
J, N, and W packages

TTL
MEDIUM SCALE INTEGRATION (MSI)

FUNCTION	OPERATING TEMPERATURE RANGE –55°C to 125°C	OPERATING TEMPERATURE RANGE 0°C to 70°C	PACKAGES* Dual-In-Line	PACKAGES* Flat	SEC.-PAGE
ASYNCHRONOUS COUNTERS					
Decade Counters	SN5490	SN7490	J	N	W	9-4
Decade Counters (Low Power)	SN54L90	SN74L90	J	N	T	9-9
Divide-by-Twelve Counters	SN5492	SN7492	J	N	W	9-14
4-Bit Binary Counters	SN5493	SN7493	J	N	W	9-19
4-Bit Binary Counters (Low Power)	SN54L93	SN74L93	J	N	T	9-24
50-MHz Preset Table Decade Counters/Latches	SN54196	SN74196	J	N	W	9-29
50-MHz Preset Table 4-Bit Binary Counters/Latches	SN54197	SN74197	J	N	W	9-29
SYNCHRONOUS COUNTERS					
Synchronous 6-Bit Binary Rate Multiplier		SN7497	J	N	W	9-35
Sychronous Decade Counters	SN54160	SN74160	J	N	W	9-41
Synchronous 4-Bit Binary Counters	SN54161	SN74161	J	N	W	9-41
Fully Synchronous Decade Counters	SN54162	SN74162	J	N	W	9-41
Fully Synchronous 4-Bit Binary Counters	SN54163	SN74163	J	N	W	9-41
Synchronous Decade Decimal Rate Multiplier		SN74167	J	N	W	9-35
Synchronous Up/Down Decade Counters (Single Clock Line)	SN54190	SN74190	J	N	W	9-49
Synchronous Up/Down 4-Bit Binary Counters (Single Clock Line)	SN54191	SN74191	J	N	W	9-49
Synchronous Up/Down Decade Counters (Two Clock Lines)	SN54192	SN74192	J	N	W	9-57
Synchronous Up/Down 4-Bit Binary Counters (Two Clock Lines)	SN54193	SN74193	J	N	W	9-57
4-BIT, 5-BIT, 6-BIT SHIFT/STORAGE REGISTERS					
4-Bit Shift Registers (Parallel-In, Serial-Out)	SN5494	SN7494	J	N	W	9-58
4-Bit Universal Shift Registers (Parallel-In, Parallel-Out)	SN5495A	SN7495A	J	N	W	9-72
4-Bit Universal Shift Registers (Parallel-In, Parallel-Out) (Low Power)	SN54L95	SN74L95	J	N	T	9-79
5-Bit Shift Registers (Dual-Parallel-In, Parallel-Out)	SN5496	SN7496	J	N	W	9-86
4-Bit Data Selectors/Storage Registers (Low Power)	SN54L98	SN74L98	J	N		9-90
4-Bit Right-Shift Registers with J $\overline{K}$ and D (Low Power)	SN54L99	SN74L99	J	N		9-96
4-Bit Parallel-In, Parallel-Out Bidirectional Shift Registers	SN54194	SN74194	J	N	W	9-104
4-Bit Parallel-In, Parallel-Out Shift Register (J-$\overline{K}$ Inputs to First Stage)	SN54195	SN74195	J	N	W	9-108

*For outline drawings of all packages, see Section 1.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

TTL MSI INDEX

TTL
MEDIUM SCALE INTEGRATION (MSI)

FUNCTION	OPERATING TEMPERATURE RANGE –55°C to 125°C	OPERATING TEMPERATURE RANGE 0°C to 70°C	PACKAGES* Dual-In-Line	PACKAGES* Flat	SEC.-PAGE
8-BIT SHIFT REGISTERS					
8-Bit Shift Registers	SN5491A	SN7491A	J	N W	9-112
8-Bit Shift Registers (Low Power)	SN54L91	SN74L91	J	N T	9-117
8-Bit Parallel-Out Shift Registers	SN54164	SN74164	J	N W	9-122
8-Bit Parallel-Out Shift Registers (Low Power)	SN54L164	SN74L164	J	N T	9-126
Parallel-Load 8-Bit Shift Registers	SN54165	SN74165	J	N W	9-130
Parallel-Load 8-Bit Shift Registers	SN54166	SN74166	J	N W	9-134
8-Bit Parallel-In, Parallel-Out Bidirectional Shift Registers	SN54198	SN74198	J	N W	9-134
8-Bit Parallel-In, Parallel-Out Shift Registers (J-$\overline{K}$ Inputs to First Stage)	SN54199	SN74199	J	N W	9-134
CODE CONVERTERS					
BCD-to-Binary Converters	SN54184	SN74184	J	N W	9-142
Binary-to-BCD Converters	SN54185A	SN74185A	J	N W	9-142
DECODERS/DEMULTIPLEXERS					
BCD-to-Decimal Decoders	SN5442	SN7442	J	N W	9-148
BCD-to-Decimal Decoders (Low Power)	SN54L42	SN74L42	J	N	9-154
Excess-3-to-Decimal Decoders	SN5443	SN7443	J	N W	9-148
Excess-3-to-Decimal Decoders (Low Power)	SN54L43	SN74L43	J	N	9-154
Excess-3-Gray-to-Decimal Decoders	SN5444	SN7444	J	N W	9-148
Excess-3-Gray-to-Decimal Decoders (Low Power)	SN54L44	SN74L44	J	N W	9-154
4-Line-to-16-Line (1 of 16) Decoders/Demultiplexers	SN54154	SN74154	J	N W	9-160
Dual 2-Line-to-4-Line Decoders/Demultiplexers	SN54155	SN74155	J	N W	9-167
Dual 2-Line-to-4-Line Decoders/Demultiplexers (with Open-Collector Output)	SN54156	SN74156	J	N W	9-167
DECODERS/LAMP DRIVERS/BUFFERS					
BCD-to-Decimal Decoders/Drivers with 30-V Output	SN5445	SN7445	J	N W	9-175
BCD-to-Decimal Decoders/Drivers with 15-V Output	SN54145	SN74145	J	N W	9-175
BCD-to-Seven-Segment Decoders/Drivers with 30-V Output	SN5446A	SN7446A	J	N W	9-181
BCD-to-Seven-Segment Decoders/Drivers with 30-V Output (Low Power)	SN54L46	SN74L46	J	N	9-198
BCD-to-Seven-Segment Decoders/Drivers with 15 V Output	SN5447A	SN7447A	J	N W	9-181
BCD-to-Seven-Segment Decoders/Drivers with 15-V Output (Low Power)	SN54L47	SN74L47	J	N	9-198
BCD-to-Seven-Segment Decoders	SN5448	SN7448	J	N W	9-181
BCD-to-Seven-Segment Decoders (14-pin Function)	SN5449	SN7449	J	N W	9-181
BCD-to-Decimal Decoder/Driver		SN74141	J	N W	9-208

*For outline drawings of all packages, see Section 1.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TTL
MEDIUM SCALE INTEGRATION (MSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
LATCHES						
Quadruple Bistable Latches	SN5475	SN7475	J	N	W	9-213
Quadruple Bistable Latches (14-pin Function)	SN5477	SN7477			W	9-213
8-Bit Bistable Latches	SN54100	SN74100	J	N	W	9-213
MEMORIES						
16-Bit Random-Access Memories (16W by 1B)	SN5481	SN7481	J	N	W	9-221
16-Bit Random-Access Memories with Gated Write Inputs (16W by 1B)	SN5484	SN7484	J	N	W	9-221
64-Bit Random-Access Memory (16W by 4B)		SN7489	J	N	W	9-230
256-Bit Read-Only Memories (32W by 8B)	SN5488A	SN7488A		N		9-235
1024-Bit Read-Only Memories (256W by 4B)	SN54187	SN74187	J	N	W	9-244
4-By-4 Register Files	SN54170	SN74170	J	N	W	9-248
ARITHMETIC ELEMENTS						
Gated Full Adders	SN5480	SN7480	J	N	W	9-255
2-Bit Binary Full Adders	SN5482	SN7482	J	N	W	9-264
4-Bit Binary Full Adders	SN5483	SN7483	J	N	W	9-271
4-Bit Binary Full Adders (Low-Power Schottky)	SN54LS83	SN74LS83	J	N		9-279
4-Bit Magnitude Comparators	SN5485	SN7485	J	N	W	9-286
4-Bit Magnitude Comparators (Low Power)	SN54L85	SN74L85	J	N		9-289
Quadruple 2-Input Exclusive-OR Gates	SN5486	SN7486	J	N	W	9-296
Quadruple 2-Input Exclusive-OR Gates (Low Power)	SN54L86	SN74L86	J	N	T	9-300
4-Bit True/Complement Zero-One Elements	SN54H87	SN54H87	J	N	W	9-304
8-Bit Odd/Even Parity Generators/Checkers	SN54180	SN74180	J	N	W	9-309
4-Bit Arithmetic Logic Unit (ALU) and Function Generators	SN54181	SN74181	J	N	W	9-315
Look-Ahead Carry Generators (for ALU)	SN54182	SN74182	J	N	W	9-326
Dual Carry-Save Full Adders	SN54H183	SN74H183	J	N	W	9-332
DATA SELECTORS/MULTIPLEXERS						
16-Bit Data Selectors/Multiplexers	SN54150	SN74150	J	N	W	9-339
8-Bit Data Selectors/Multiplexers with Strobe	SN54151	SN74151	J	N	W	9-339
8-Bit Data Selectors/Multiplexers	SN54152	SN74152			W	9-339
Dual 4-Line-to-1-Line Data Selectors/Multiplexers	SN54153	SN74153	J	N	W	9-351
Dual 4-Line-to-1-Line Data Selectors/Multiplexers (Low Power)	SN54L153	SN74L153	J	N		9-358
LOGIC DIODE MATRICES						
Series TIDM1, TIDM2 Monolithic Diode Matrices			J		F, W	9-365

*For outline drawings of all packages, see Section 1.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

CIRCUIT TYPES SN5490, SN7490
DECADE COUNTERS

MSI TTL HIGH-SPEED DECADE COUNTERS

for applications in

- **Digital Computer Systems**
- **Data-Handling Systems**
- **Control Systems**

logic

TRUTH TABLES

BCD COUNT SEQUENCE
(See Note 1)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

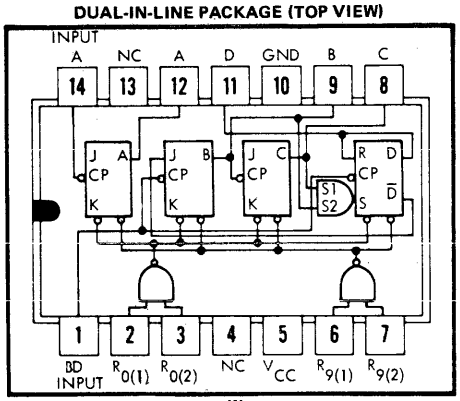
RESET/COUNT (See Note 2)

RESET INPUTS				OUTPUT
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

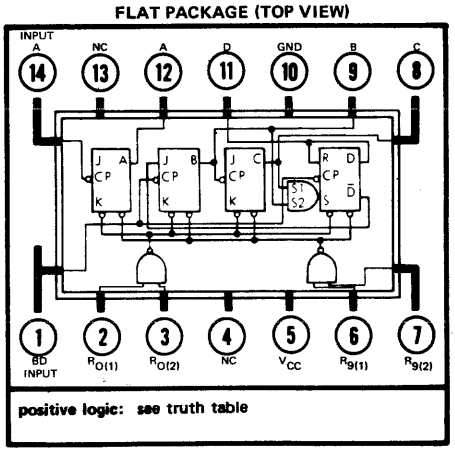
NC—No Internal Connection

NOTES: 1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 or a logical 0 may be present.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



W
FLAT PACKAGE (TOP VIEW)



positive logic: see truth table

description and typical count configurations

These high-speed, monolithic decade counters consist of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to zero or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

1. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional zero reset, inputs are provided to reset a BCD count for nine's complement decimal applications.

2. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.

3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 160 mW.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 3) . . . . . 7 V
Input Voltage, V_{in} (See Notes 3 and 4) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5490 Circuits . . . . . −55°C to 125°C
SN7490 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3): SN5490 Circuits	4.5	5	5.5	V
SN7490 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output (See Note 5)			10	
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

NOTE 5. Fan-out from output A to input BD and to 10 additional Series 54/74 loads is permitted.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at input A	3	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at input BD	3	V_{CC} = MAX, V_{in} = 2.4 V				160	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at input A	4	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BD	4	V_{CC} = MAX, V_{in} = 0.4 V				−6.4	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN5490	−20		−57	mA
				SN7490	−18		−57	mA
I_{CC}	Supply current	3	V_{CC} = MAX	SN5490		32	46	mA
				SN7490		32	53	mA

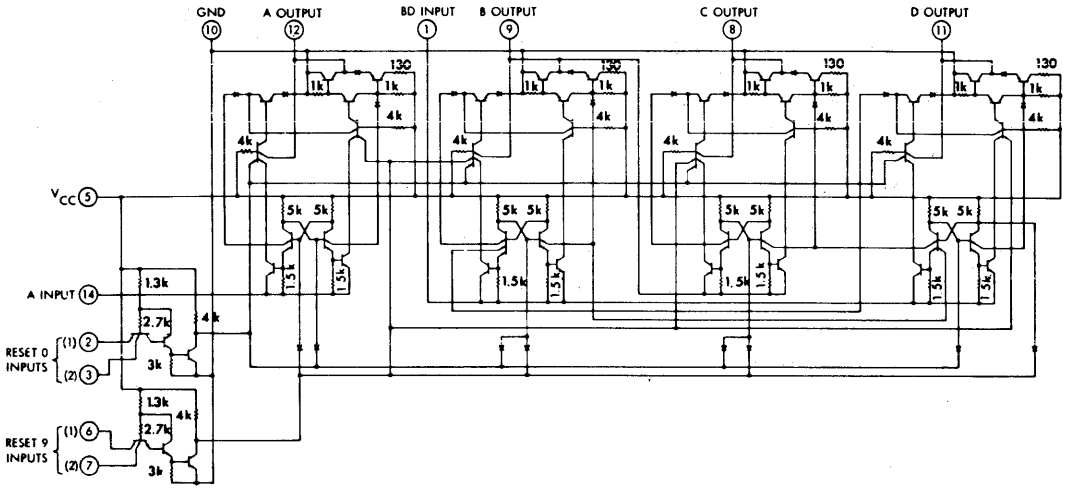
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C
§ Not more than one output should be shorted at a time.

9

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses		C_L = 15 pF, R_L = 400 Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output C	6	C_L = 15 pF, R_L = 400 Ω		60	100	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output C	6	C_L = 15 pF, R_L = 400 Ω		60	100	ns

schematic

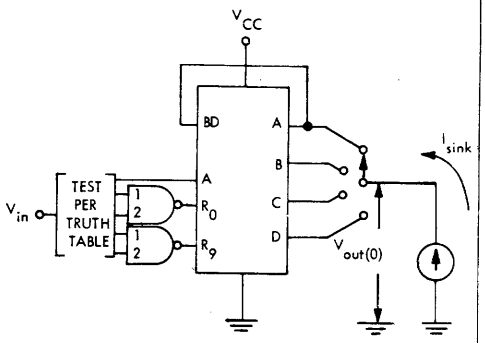


Component values shown are nominal.
Resistor values are in ohms.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

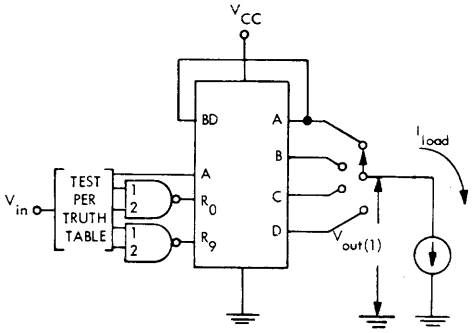
d-c test circuits†

PARAMETER MEASUREMENT INFORMATION



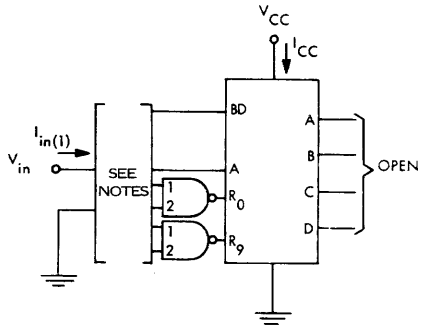
1. Each output is tested in the logical 0 state.

FIGURE 1



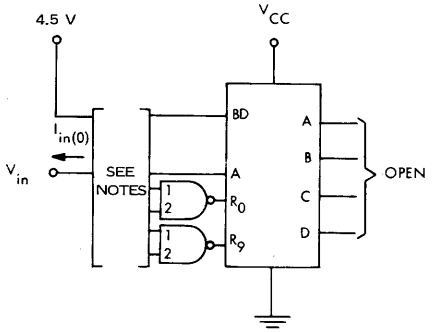
1. Each output is tested in the logical 1 state.

FIGURE 2



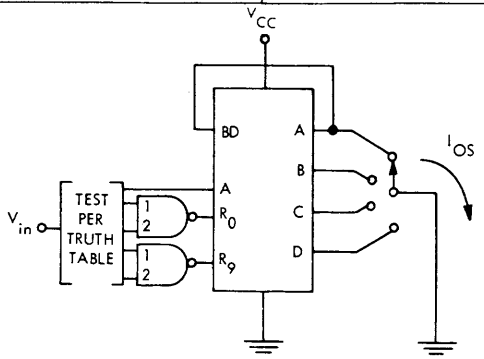
1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$, ground $R_{0(2)}$ or $R_{9(2)}$, respectively, and vice versa.
3. When testing I_{CC} reset all outputs to logical 0, ground all inputs, then measure I_{CC}.

FIGURE 3



1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$, apply 4.5 V to $R_{0(2)}$ or $R_{9(2)}$, respectively, and vice versa.

FIGURE 4



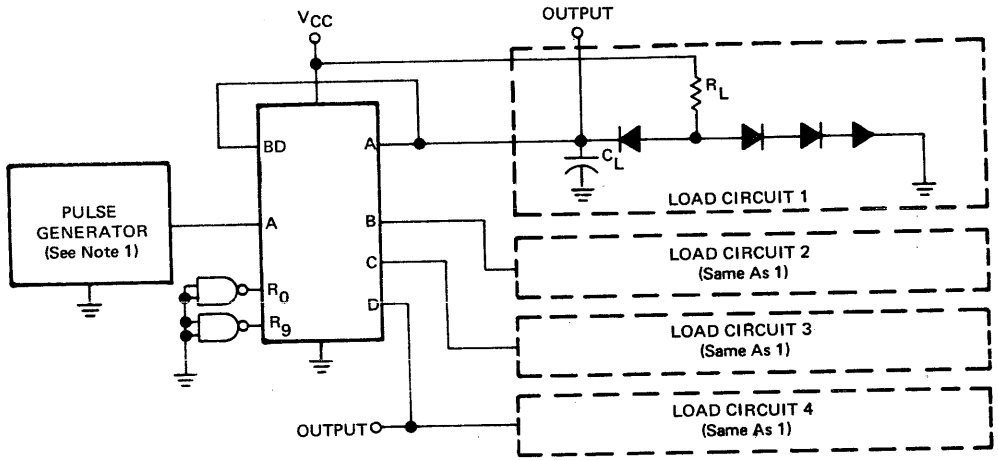
1. Each output is tested in the logical 1 state.

FIGURE 5

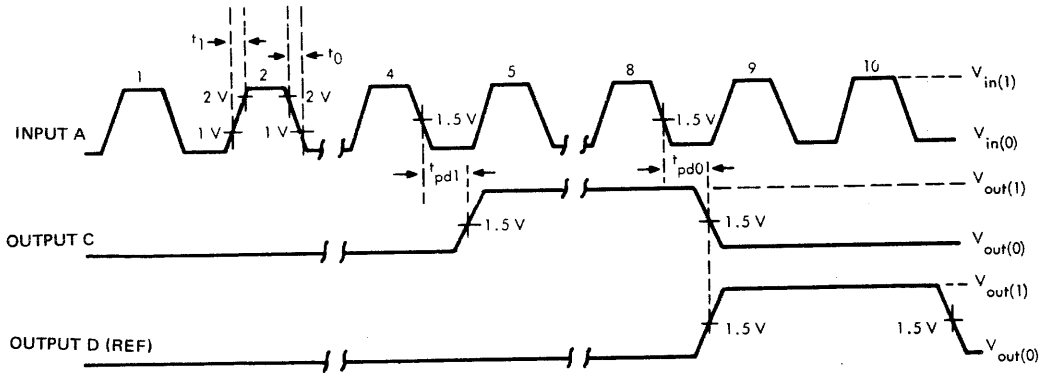
† Arrows indicate actual direction of current flow.

9

switching characteristics PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. C_L includes probe and jig capacitance.
4. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
5. Voltage values are with respect to ground terminal.

FIGURE 6-SWITCHING TIMES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54L90, SN74L90
DECADE COUNTERS

for applications in

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

TRUTH TABLES

BCD COUNT SEQUENCE
(See Note A)

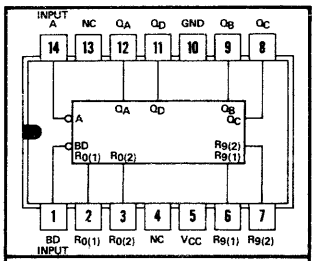
COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

NOTES: A. Output Q_A is connected to input BD for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. H = high level, L = low level, X = irrelevant

J OR N DUAL-IN-LINE OR
T FLAT PACKAGE (TOP VIEW)†



positive logic: See truth tables

NC—No internal connection
†Pin assignments for these circuits are the same for all packages.

RESET/COUNT FUNCTION TABLE

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	OUTPUT D	C	B	A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

description and typical count configurations

These low-power monolithic decade counters consist of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to zero or to a binary-coded-decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the counter may be operated in any one of three independent count modes:

9

1. When used as a binary-coded-decimal decade counter, the BD input must be externally connected to the Q_A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional zero reset, inputs are provided to reset a BCD count for nine's complement decimal applications.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the Q_D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary truth table above.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

These circuits are compatible with most TTL and DTL logic families. Power dissipation is typically 20 mW. The SN54L90 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L90 is characterized for operation from 0°C to 90°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range: SN54L90 Circuits . . . . . −55°C to 125°C
SN74L90 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN54L90			SN74L90			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Input count frequency, f_{count}	0			0			MHz
Normalized fan-out from each output, N (see Note 3)			10			10	
Width of input count pulse, $t_{w(count)}$ (see Figure 6)	200			200			ns
Width of reset pulse, $t_{w(reset)}$	200			200			ns
Operating free-air temperature, T_A	−55	25	125	0	25	70	°C

NOTE 3: Fan-out capability from output Q_A to input BD and ten additional TTL loads is guaranteed.

electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST FIGURE	TEST CONDITIONS†		MIN	MAX	UNIT
V_{IH}	High-level input voltage		1 and 2			2		V
V_{IL}	Low-level input voltage						0.7	V
V_{OH}	High-level output voltage		2	V_{CC} = MIN, V_{IH} = 2 V,	I_{OH} = −100 μA, V_{IL} = 0.7 V	2.4		V
V_{OL}	Low-level output voltage		1	V_{CC} = MIN, V_{IH} = 2 V,	I_{OL} = 2 mA, V_{IL} = 0.7 V		0.3	V
I_I	Input current at maximum input voltage	Any reset input	3	V_{CC} = MAX,	V_I = 5.5 V		100	μA
		A input					300	
		BD input					600	
I_{IH}	High-level input current	Any reset input	3	V_{CC} = MAX,	V_I = 2.4 V		10	μA
		A input					30	
		BD input					60	
I_{IL}	Low-level input current	Any reset input	4	V_{CC} = MAX,	V_I = 0.3 V		−0.18	mA
		A input					−0.54	
		BD input					−1.08	
I_{OS}	Short-circuit output current§		5	V_{CC} = MAX		−3	−15	mA
I_{CC}	Supply current		3	V_{CC} = MAX			7.2	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
§Not more than one output should be shorted at a time.

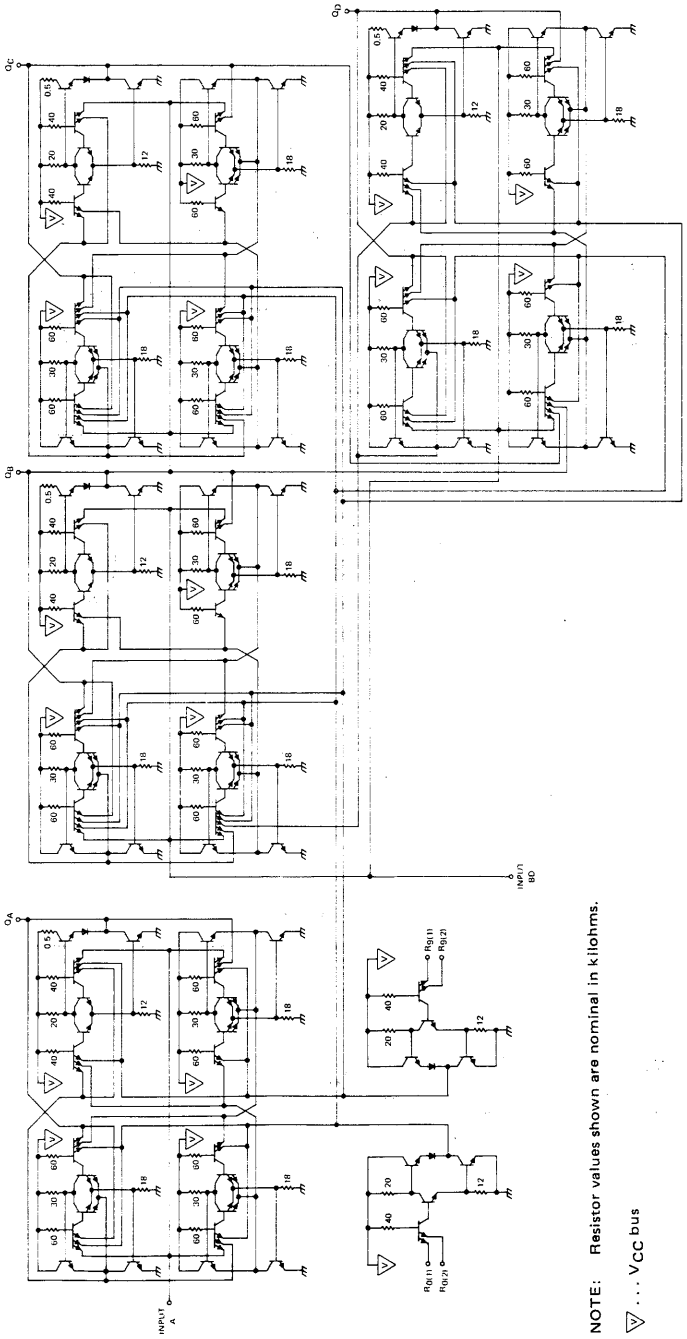
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency				3		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from input A	6	C_L = 50 pF, R_L = 4 kΩ			340	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from input A	6				340	ns

See mechanical data and ordering instructions starting on page 1-1 of TTL Integrated Circuits Catalog (CC201) or page S1-1 of TTL Catalog Supplement (CC301).

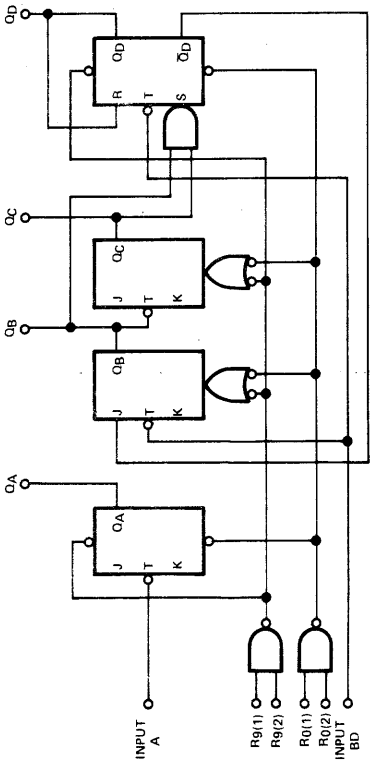
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

schematic and functional block diagram



NOTE: Resistor values shown are nominal in kilohms.

▷ ... V_{CC} bus



9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

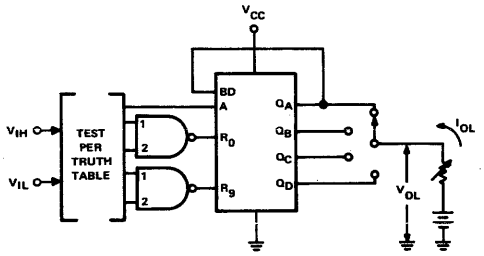


FIGURE 1–V_{IH}, V_{IL}, V_{OL}

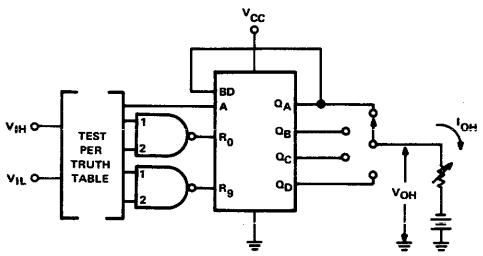
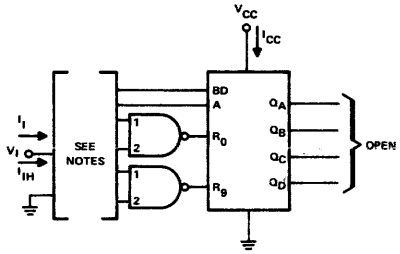
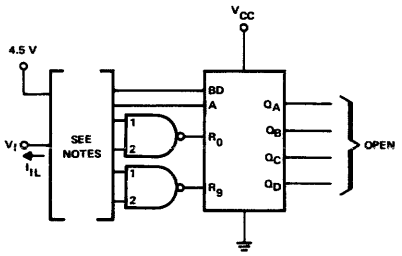


FIGURE 2–V_{IH}, V_{IL}, V_{OH}



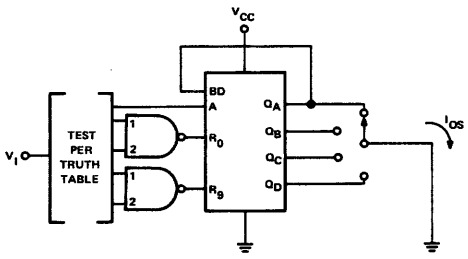
NOTES: A. Each input is tested separately.
B. When testing $R_{0(1)}$ or $R_{9(1)}$, ground $R_{0(2)}$ or $R_{9(2)}$ respectively and vice versa.
C. When testing I_{CC}, reset all outputs to low level, then ground all inputs and measure I_{CC}.

FIGURE 3–I_I, I_{IH}, I_{CC}



NOTES: A. Each input is tested separately.
B. When testing $R_{0(1)}$ or $R_{9(1)}$, apply 4.5 V to $R_{0(2)}$ or $R_{9(2)}$ respectively and vice versa.

FIGURE 4–I_{IL}



Each output is tested at the high level.

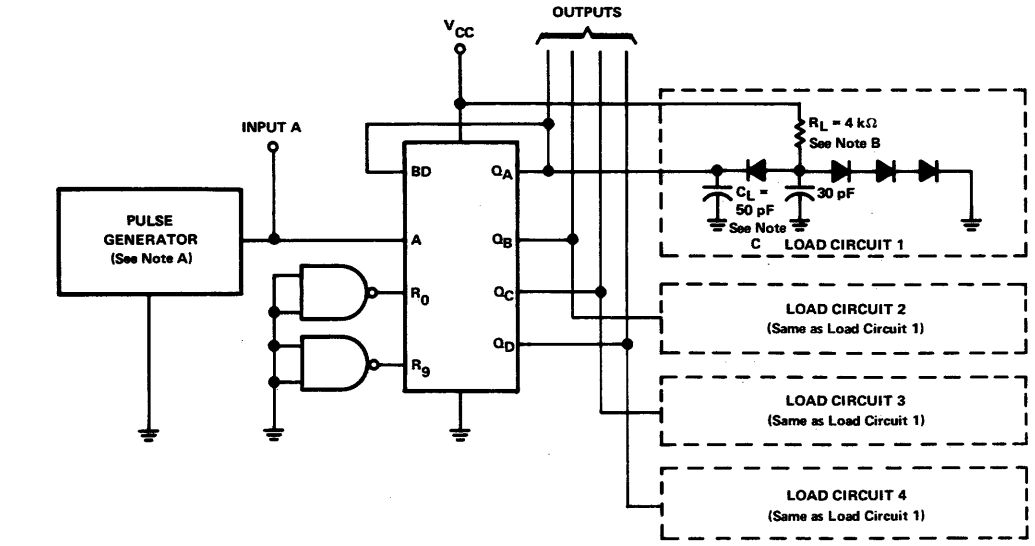
FIGURE 5–I_{OS}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

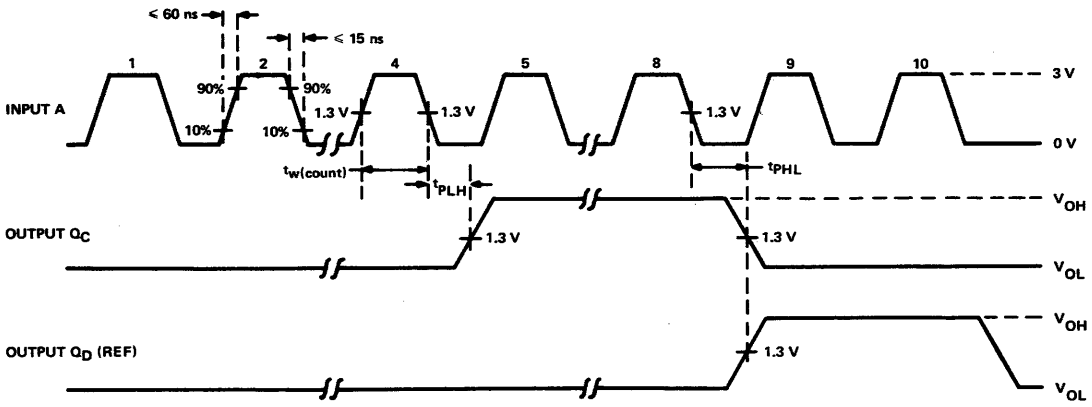
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 1 μs, PRR = 500 kHz, $Z_{out} \approx 50\ \Omega$.
B. All diodes are 1N3064.
C. C_L includes probe and jig capacitance.

FIGURE 6–SWITCHING TIMES

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5492,SN7492
DIVIDE-BY-TWELVE COUNTERS
(DIVIDE-BY-TWO AND DIVIDE-BY-SIX)

MSI TTL HIGH-SPEED COUNTERS

for applications in

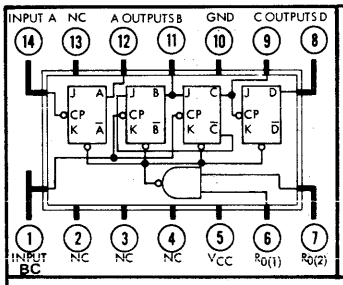
- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

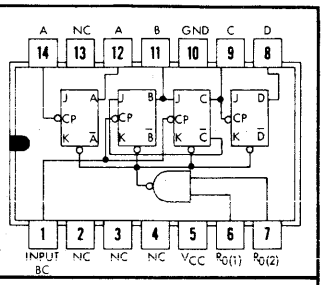
TRUTH TABLE (See Notes 1, 2, and 3)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

NC—No Internal Connection

NOTES: 1. Output A connected to input B
2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a logical 0 to count.

description

These high-speed, monolithic 4-bit binary counters consist of four master slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops, the counter may be operated in two independent modes:

9

1. When used as a divide-by-twelve counter, output A must be externally connected to input BC. The input count pulses are applied to input A. Simultaneous divisions of 2, 6, and 12 are performed at the A, C, and D outputs as shown in the truth table above.

2. When used as a divide-by-six counter, the input count pulses are applied to input BC. Simultaneously, frequency divisions of 3 and 6 are available at the C and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 155 mW.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 4) . . . . . 7 V
Input Voltage V_{in} (See Notes 4 and 5) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5492 Circuits . . . . . −55°C to 125°C
SN7492 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 4. These voltage values are with respect to network ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 4): SN5492 Circuits	4.5	5	5.5	V
SN7492 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output (See Note 6)			10	
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

NOTE: 6. Fan-out from output A to input BC and to 10 additional Series 54/74 loads is permitted.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at input A	3	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at input BC	3	V_{CC} = MAX, V_{in} = 2.4 V				160	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current input A	4	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BC	4	V_{CC} = MAX, V_{in} = 0.4 V				−6.4	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX, V_{out} = 0	SN5492	−20		−57	mA
				SN7492	−18		−57	mA
I_{CC}	Supply current	3	V_{CC} = MAX, V_{in} = 4.5 V	SN5492		31	44	mA
				SN7492		31	51	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

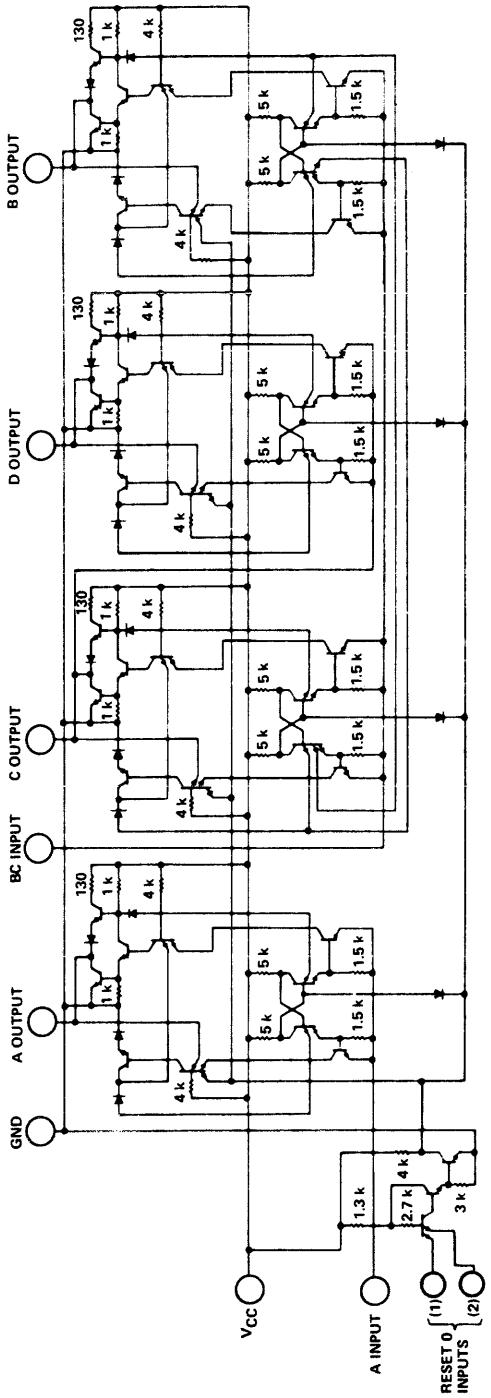
9

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses		C_L = 15 pF, R_L = 400 Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	6	C_L = 15 pF, R_L = 400 Ω		60	100	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D	6	C_L = 15 pF, R_L = 400 Ω		60	100	ns

CIRCUIT TYPES SN5492,SN7492
DIVIDE-BY-TWELVE COUNTERS
(DIVIDE-BY-TWO AND DIVIDE-BY-SIX)

schematic

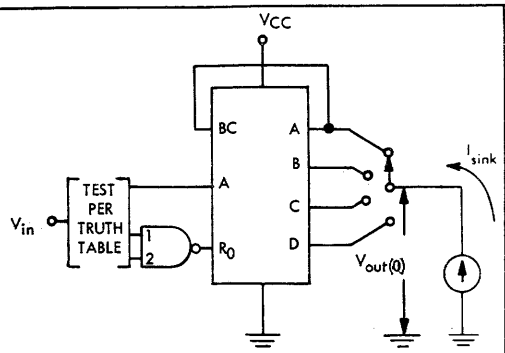


Component values shown are nominal.
Resistor values are in ohms.

9

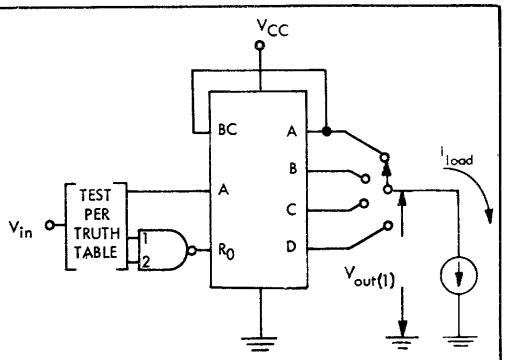
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



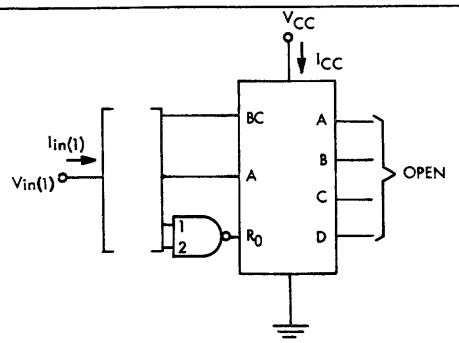
1. Each output is tested in the logical 0 state.

FIGURE 1



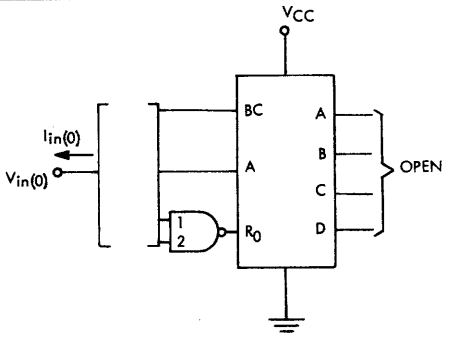
1. Each output is tested in the logical 1 state.

FIGURE 2



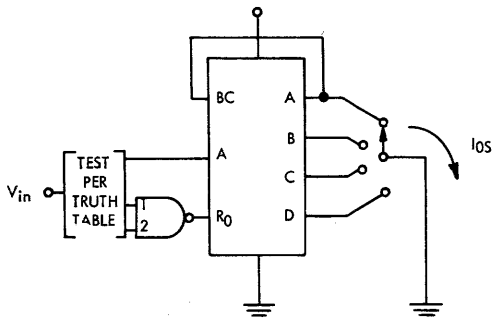
1. Each input is tested separately.
2. When testing $R_{0(1)}$ ground $R_{0(2)}$.
3. When testing $R_{0(2)}$ ground $R_{0(1)}$.
4. When testing I_{CC} reset all outputs to logical 0, ground all inputs, then measure I_{CC}.

FIGURE 3



1. Each input is tested separately.
2. When testing $R_{0(1)}$ apply 4.5 V to $R_{0(2)}$.
3. When testing $R_{0(2)}$ apply 4.5 V to $R_{0(1)}$.

FIGURE 4



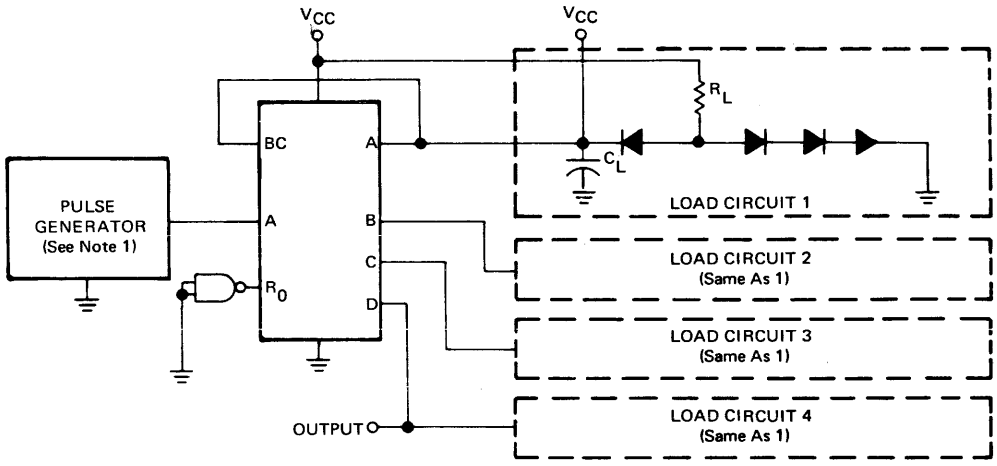
1. Each output is tested in the logical 1 state.

FIGURE 5

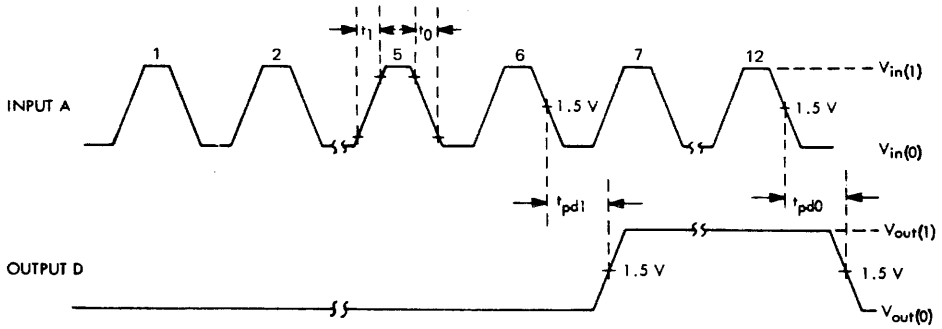
†Arrows indicate actual direction of current flow

switching characteristics

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leqslant 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. C_L includes probe and jig capacitance.
4. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
5. Voltage values are with respect to ground terminal.

FIGURE 6–SWITCHING TIMES

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5493, SN7493
4-BIT BINARY COUNTERS

MSI TTL HIGH-SPEED RIPPLE-THROUGH COUNTERS

for applications in

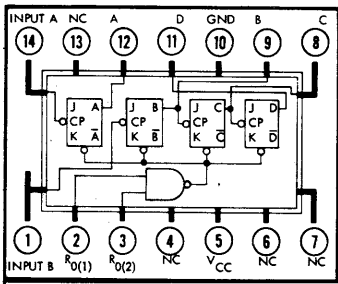
- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

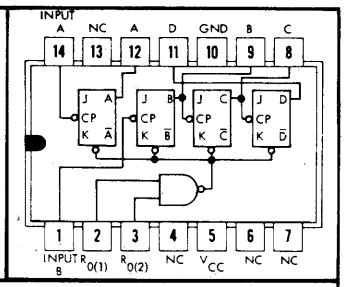
TRUTH TABLE (See Notes 1, 2, and 3)

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

NC—No Internal Connection

NOTES: 1. Output A connected to input B
2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a logical 0 to count.

description

These high-speed, monolithic 4-bit binary counters consist of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table above.

2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 40 mW per flip-flop (160 mW total).

9

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 4) . . . . . 7 V
Input Voltage, V_{in} (See Notes 4 and 5) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5493 Circuits . . . . . −55°C to 125°C
SN7493 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 4. These voltage values are with respect to network ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 4): SN5493 Circuits	4.5	5	5.5	V
SN7493 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output (See Note 6)			10	
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

NOTE: 6. Fan-out from output A to input B and to 10 additional Series 54/74 loads is permitted.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

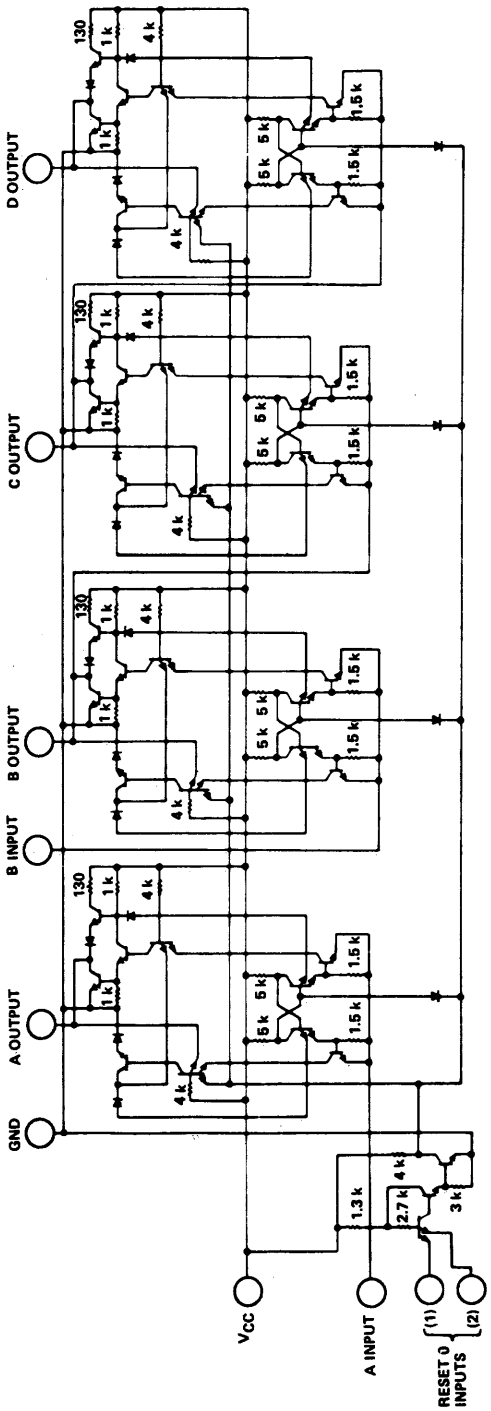
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at A or B inputs	3	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at A or B inputs	4	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX, V_{out}=0	SN5493	−20		−57	mA
				SN7493	−18		−57	mA
I_{CC}	Supply current	3	V_{CC} = MAX, V_{in} = 4.5 V	SN5493		32	46	mA
				SN7493		32	53	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses		C_L = 15 pF, R_L = 400 Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	6	C_L = 15 pF, R_L = 400 Ω		75	135	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D	6	C_L = 15 pF, R_L = 400 Ω		75	135	ns

schematic

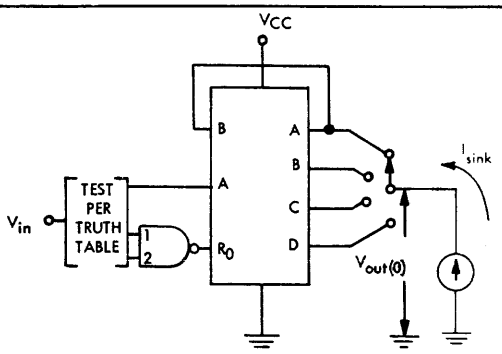


Component values shown are nominal.
Resistor values are in ohms.

9

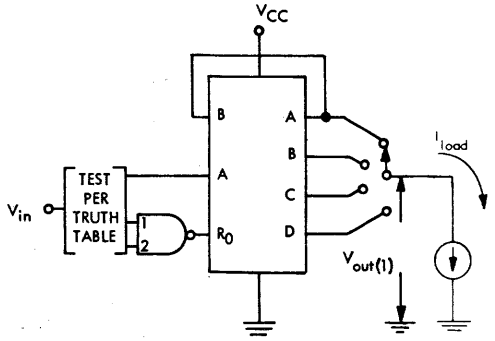
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



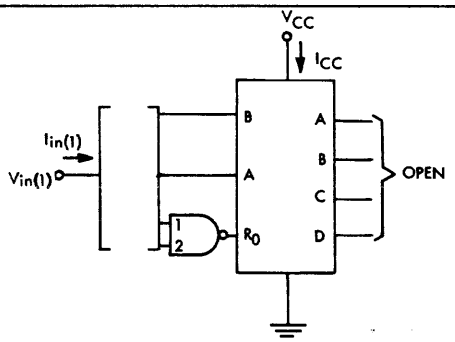
1. Each output is tested in the logical 0 state.

FIGURE 1



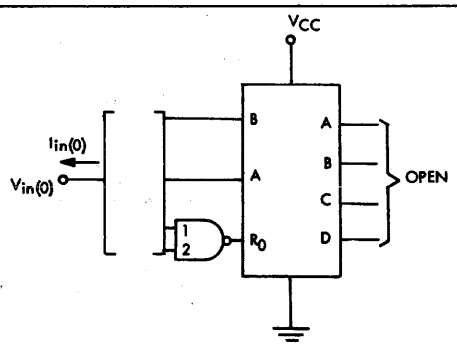
1. Each output is tested in the logical 1 state.

FIGURE 2



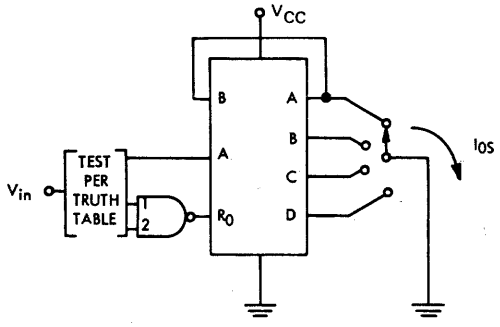
1. Each input is tested separately.
2. When testing $R_{0(1)}$ ground $R_{0(2)}$.
3. When testing $R_{0(2)}$ ground $R_{0(1)}$.
4. When testing I_{CC} all inputs and outputs are open.

FIGURE 3



1. Each input is tested separately.
2. When testing $R_{0(1)}$ apply 4.5 V to $R_{0(2)}$.
3. When testing $R_{0(2)}$ apply 4.5 V to $R_{0(1)}$.

FIGURE 4



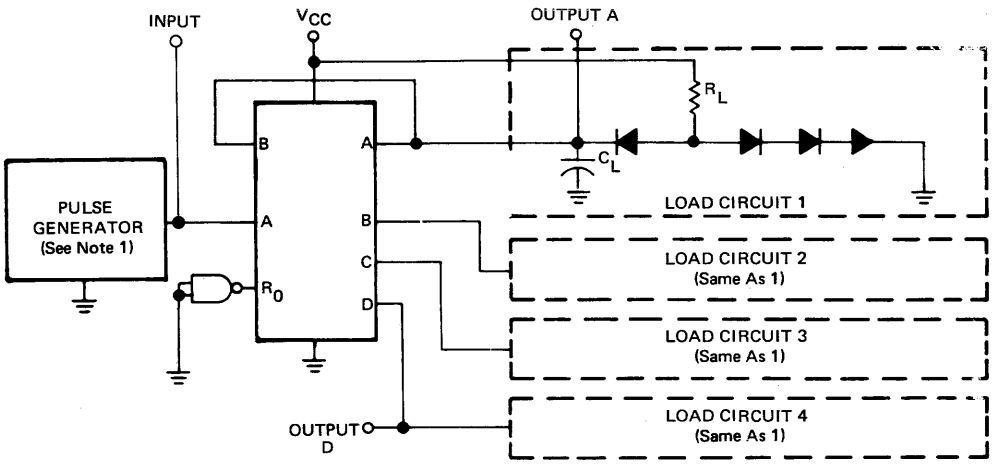
1. Each output is tested in the logical 1 state.

FIGURE 5

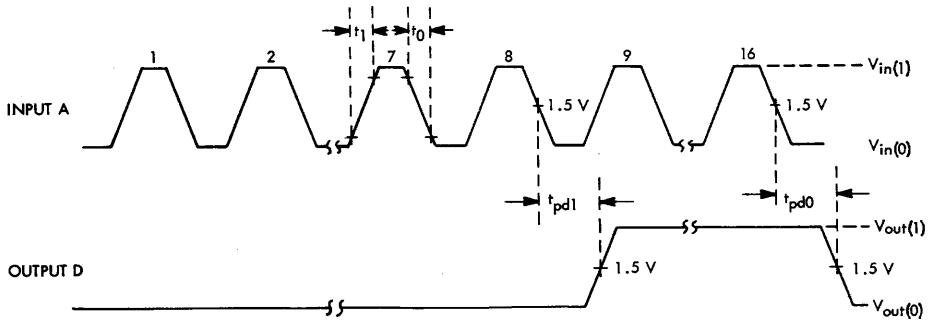
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leqslant 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064
3. C_L includes probe and jig capacitance.
4. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
5. Voltage values are with respect to ground terminal.

FIGURE 6–SWITCHING TIMES

9

CIRCUIT TYPES SN54L93, SN74L93
4-BIT BINARY COUNTERS

A SERIES 54L/74L TTL LOW-POWER RIPPLE-THROUGH COUNTER FOR APPLICATIONS IN

● Digital Computer Systems ● Data-Handling Systems ● Control Systems

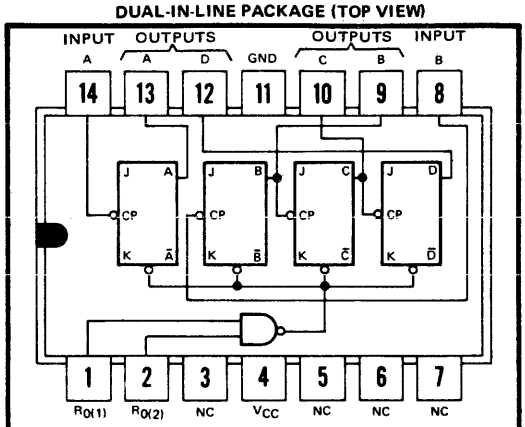
logic

TRUTH TABLE (See Notes 1 and 2)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

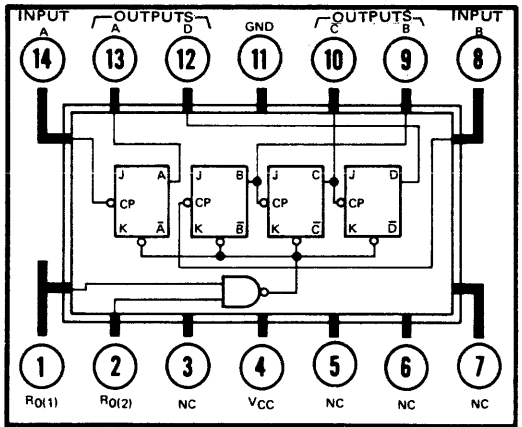
NOTES: 1. Output A connected to input B.
2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$. Inputs must be at a logical 1.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a logical 0 to count.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

T FLAT PACKAGE (TOP VIEW)



positive logic: see truth table

NC—No Internal Connection

description

The SN54L93/SN74L93 are low-power TTL monolithic 4-bit binary counters consisting of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table above.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

The SN54L93/SN74L93 is completely compatible with TTL and DTL logic families. Average power dissipation is typically 16 mW.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 4) . . . . . 8 V
Input Voltage, V_{in} (See Notes 4 and 5) . . . . . 5.5 V
Operating Free Air Temperature Ranges: SN54L93 Circuits . . . . . −55°C to 125°C
SN74L93 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 4. These voltage values are with respect to network ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

Supply Voltage V_{CC}: SN54L93 Circuits . . . . . 4.5 V to 5.5 V
SN74L93 Circuits . . . . . 4.75 V to 5.25 V
Maximum Normalized Fan-Out From Each Output (See Note 6) 10
Width of Input Count Pulse, $t_{p(in)}$ . . . . . ⩾ 200 ns
Width of Reset Pulse, $t_{p(reset)}$ . . . . . ⩾ 200 ns

NOTE: 6. Fan-out from output A to input B and to 10 additional Series 54L/74L loads is permitted.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 of any input	1		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 of any input	2				0.7	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, I_{load} = −100 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, I_{sink} = 2 mA			0.3	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	3	V_{CC} = MAX, V_{in} = 2.4 V			10	μA
			V_{CC} = MAX, V_{in} = 5.5 V			100	μA
$I_{in(1)}$	Logical 1 level input current at A or B inputs	3	V_{CC} = MAX, V_{in} = 2.4 V			20	μA
			V_{CC} = MAX, V_{in} = 5.5 V			200	μA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	4	V_{CC} = MAX, V_{in} = 0.3 V			−0.18	mA
$I_{in(0)}$	Logical 0 level input current at A or B inputs	4	V_{CC} = MAX, V_{in} = 0.3 V			−0.36	mA
I_{OS}	Short-circuit output current	5	V_{CC} = MAX, V_{out} = 0	−3		−15	mA
I_{CC}	Supply current	3	V_{CC} = MAX		3.2	6.6	mA

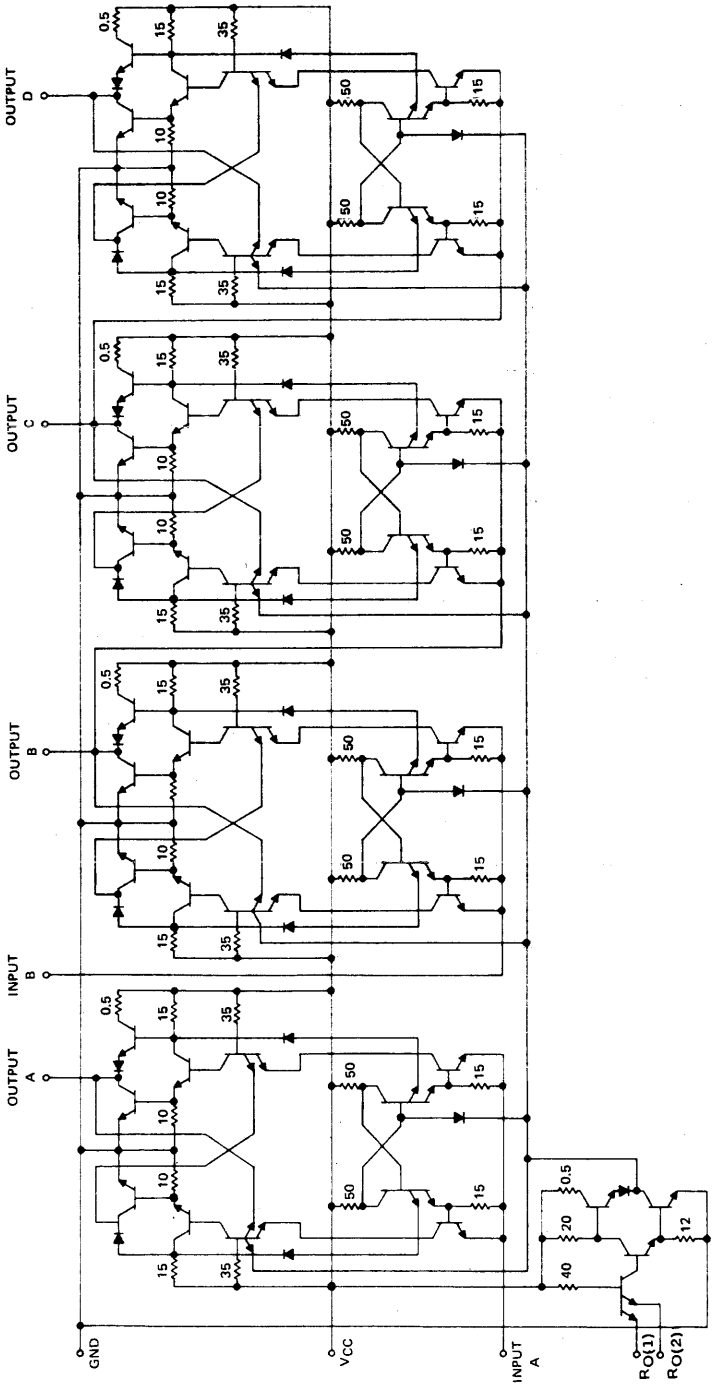
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ These typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses		C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	6	C_L = 50 pF, R_L = 4 kΩ		280	450	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to ouput D	6	C_L = 50 pF, R_L = 4 kΩ		280	450	ns

9

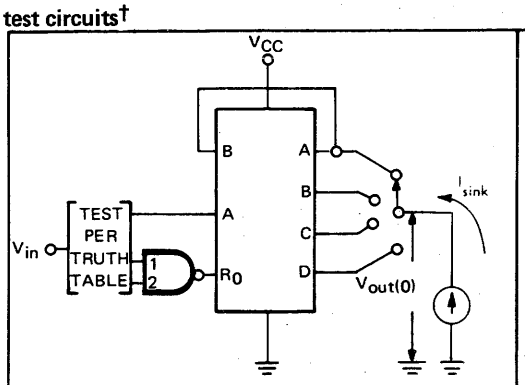
schematic



NOTES: 1. Component values shown are nominal.
2. All resistor values are in kΩ.

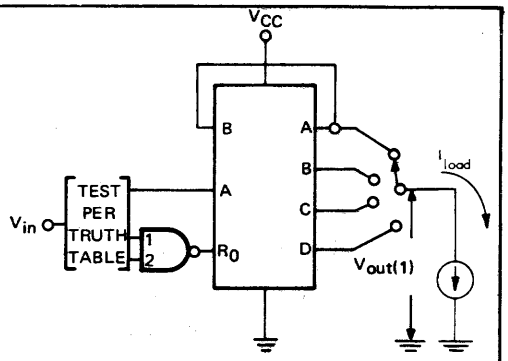
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



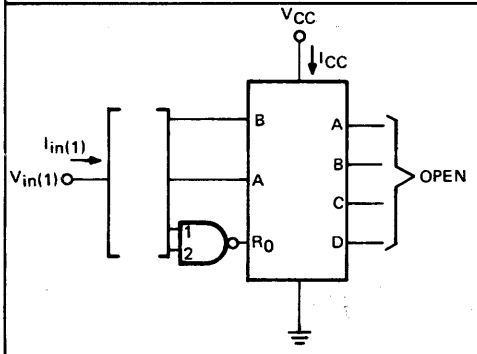
1. Each output is tested in the logical 0 state.

FIGURE 1



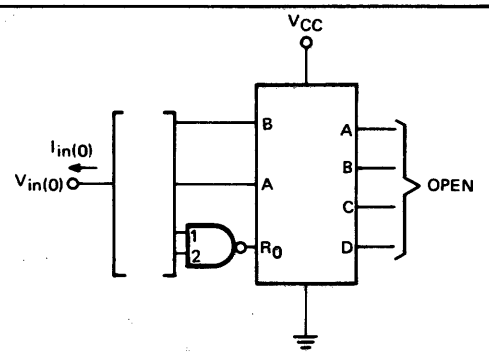
1. Each output is tested in the logical 1 state.

FIGURE 2



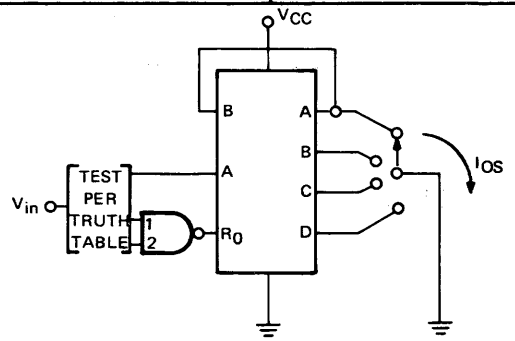
1. Each input is tested separately.
2. When testing $R_{0(1)}$ ground $R_{0(2)}$.
3. When testing $R_{0(2)}$ ground $R_{0(1)}$.
4. When testing I_{CC} all inputs and outputs are open.

FIGURE 3



1. Each input is tested separately.
2. When testing $R_{0(1)}$ apply 4.5 V to $R_{0(2)}$.
3. When testing $R_{0(2)}$ apply 4.5 V to $R_{0(1)}$.

FIGURE 4



1. Each output is tested in the logical 1 state.

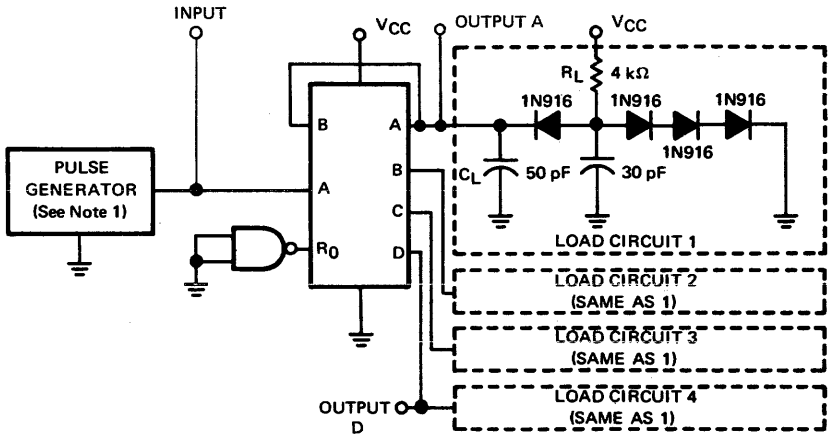
FIGURE 5

† Arrows indicate actual direction of current flow.

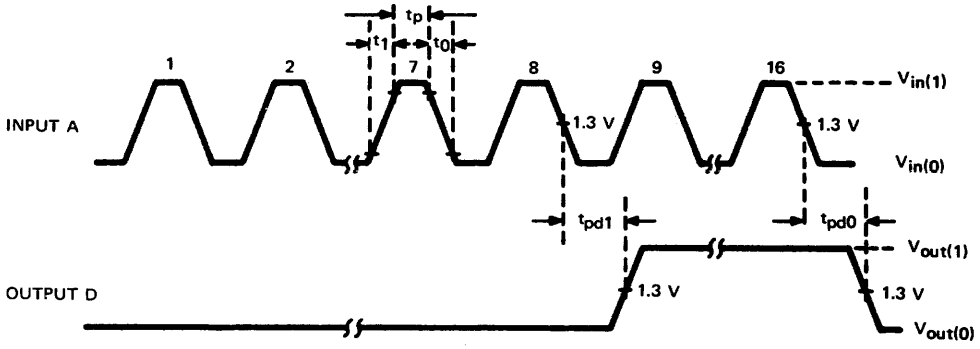
9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: $t_0 = t_1 = 15$ ns, PRR $\leq$ 500 kHz, $t_p \geq 200$ ns, and $Z_{out} \approx 50\ \Omega$.
2. Voltage values are with respect to network ground terminal.
3. C_L includes probe and jig capacitance.

FIGURE 6 – SWITCHING TIMES

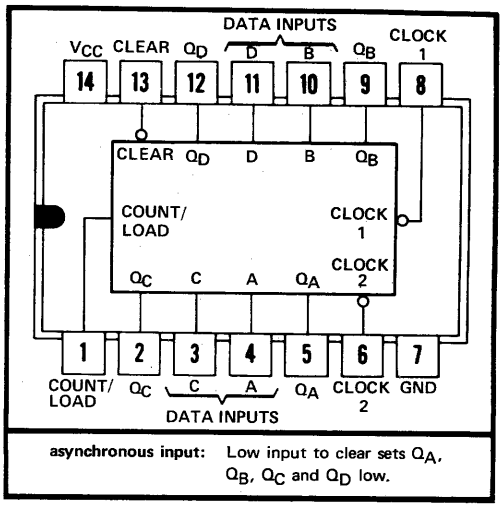
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54196, SN54197, SN74196, SN74197
50-MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

CIRCUIT TYPES SN54196, SN54197, SN74196, SN74197
BULLETIN NO. DL-S 7111369, OCTOBER 1970
REVISED JANUARY 1971

- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Guaranteed to Count at Input Frequencies from 0 to 50 MHz
- Input Clamping Diodes Simplify System Design
- Output Q_A Will Drive Clock-2 Input Plus Ten Series 54/74 Loads

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



asynchronous input: Low input to clear sets Q_A, Q_B, Q_C and Q_D low.

†Pin assignments for these circuits are the same for all packages.

description

These high-speed monolithic counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (SN54196, SN74196) or a divide-by-two and a divide-by-eight counter (SN54197, SN74197). These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

These high-speed counters will accept count frequencies of 0 to 50 megahertz at the clock-1 input and 0 to 25 megahertz at the clock-2 input. During the count operation, transfer of information to the ouputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which, when taken low, sets all outputs low regardless of the states of the clocks.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. These circuits are compatible with most TTL and DTL logic families. Typical power dissipation is 240 milliwatts. The SN54196 and SN54197 circuits are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74197 and SN74197 circuits are characterized for operation from 0°C to 70°C.

typical count configurations

SN54196 and SN74196

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a binary-coded-decimal decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown at the right.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary truth table above.

SN54196, SN74196
TRUTH TABLES

DECADE (BCD)
(See Note A)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

NOTES: A. Output Q_A connected to clock-2 input.
B. Output Q_D connected to clock-1 input.

3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

SN54197 and SN74197

The output of flip-flop A is not internally connected to the succeeding flip-flops, therefore the counter may be operated in two independent modes:

1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C, Q_D output as shown in the truth table at right.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

SN54197, SN74197
TRUTH TABLE
(See Note A)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE A: Output Q_A connected to clock-2 input.

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings (over operating free-air temperature range unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54196, SN54197 Circuits . . . . . −55°C to 125°C
SN74196, SN74197 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the clear and count/load inputs.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	SN54196, SN54197	4.5	5	5.5	V
	SN74196, SN74197	4.75	5	5.25	
Normalized fan-out from each output, N	High logic level			20	
	Low logic level			10	
Count frequency (see Figure 1)	Clock-1 input	0		50	MHz
	Clock-2 input	0		25	
Pulse width, t_w (see Figure 1)	Clock-1 input	10			ns
	Clock-2 input	20			
	Clear	15			
	Load	20			
Input hold time, t_{hold} (see Figure 1)	High-level data	$t_{w(load)}$			
	Low-level data	$t_{w(load)}$			
Input setup time, t_{setup} (see Figure 1)	High-level data	10			ns
	Low-level data	15			
Count enable time, t_{enable} (see Note 3 and Figure 1)		20			ns
Clock input pulse fall time, t_f (see Figure 1)				75	ns
Operating free-air temperature range, T_A	SN54196, SN54197	−55	25	125	°C
	SN74196, SN74197	0	25	70	

NOTE 3: Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must be both high to ensure counting.

9

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54196, SN74196			SN54197, SN74197			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MAX, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶				0.4			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	data, count/load	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
		clear, clock 1					80			80	
		clock 2					120			80	
I_{IL}	Low-level input current	data, count/load	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
		clear					−3.2			−3.2	
		clock 1					−4.8			−4.8	
		clock 2					−6.4			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54196, SN54197	−20		−57	−20		−57	mA
				SN74196, SN74197	−18		−57	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 4			48	59		48	59	mA

NOTE 4: I_{CC} is measured with all inputs grounded and all outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while fanning out to 10 Series 54/74 loads.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, R_L = 400 Ω, C_L = 15 pF, T_A = 25°C, N = 10, see figure 1

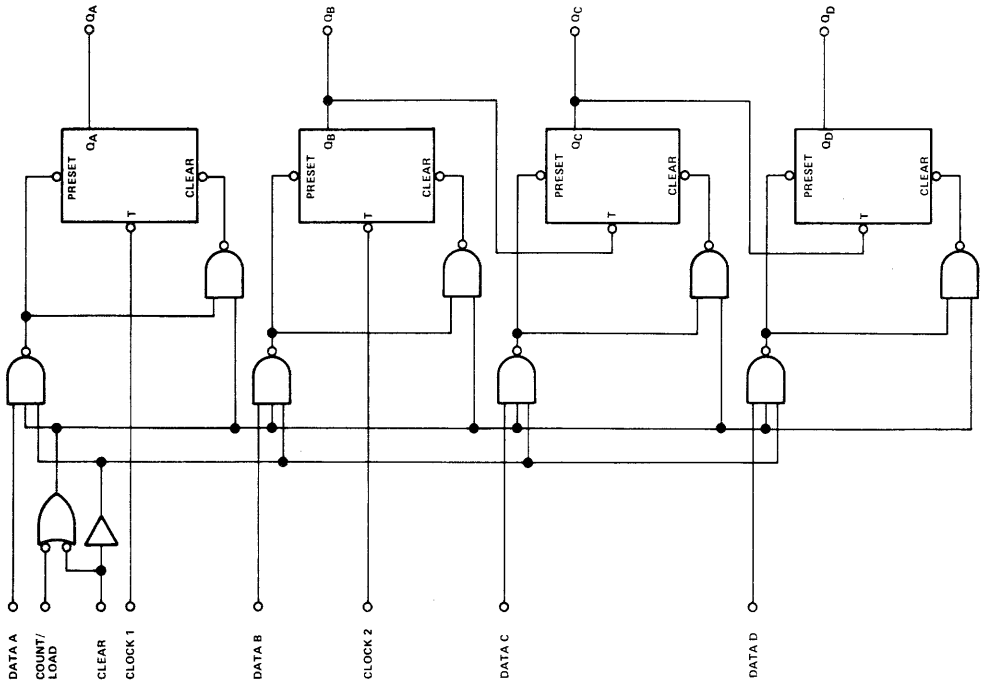
PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	SN54196, SN74196			SN54197, SN74197			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			50	70		50	70		MHz
t_{PLH}	Clock 1	Q_A		7	12		7	12	ns
t_{PHL}				10	15		10	15	
t_{PLH}	Clock 2	Q_B		12	18		12	18	ns
t_{PHL}				14	21		14	21	
t_{PLH}	Clock 2	Q_C		24	36		24	36	ns
t_{PHL}				28	42		28	42	
t_{PLH}	Clock 2	Q_D		14	21		36	54	ns
t_{PHL}				12	18		42	63	
t_{PLH}	A, B, C, D	Q_A, Q_B, Q_C, Q_D		16	24		16	24	ns
t_{PHL}				25	38		25	38	
t_{PLH}	Load	Any		22	33		22	33	ns
t_{PHL}				24	36		24	36	
t_{PHL}	Clear	Any		25	37		25	37	ns

◇f_{max} is maximum input count frequency
t_{PLH} is propagation delay time, low-to-high-level output
t_{PHL} is propagation delay time, high-to-low-level output

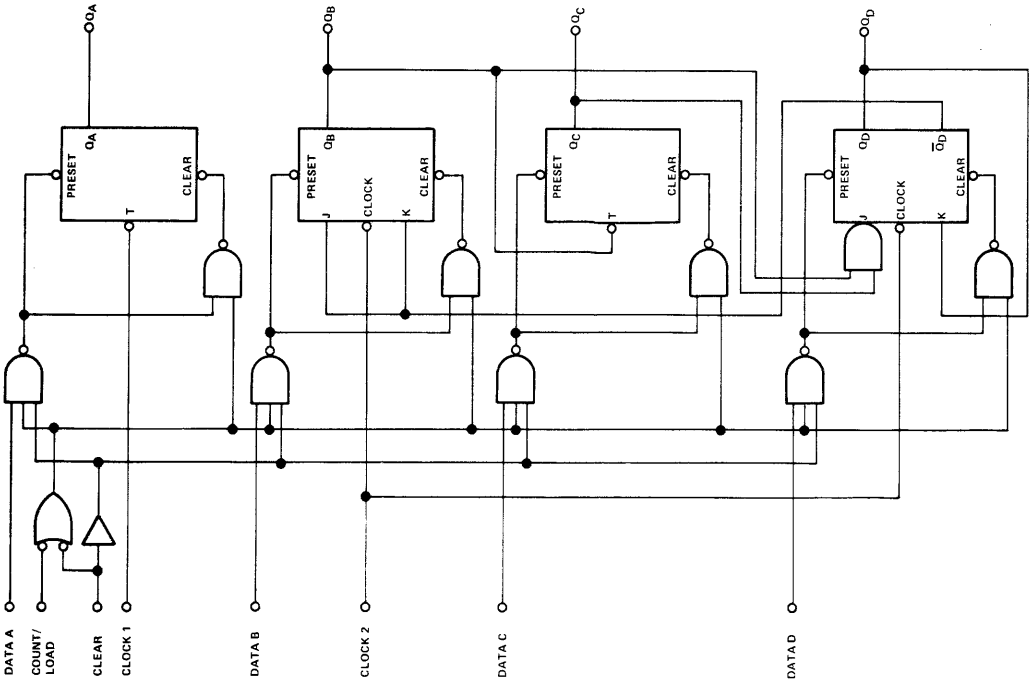
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagrams

SN54197, SN74197



SN54196, SN74196



9

070

PARAMETER MEASUREMENT INFORMATION

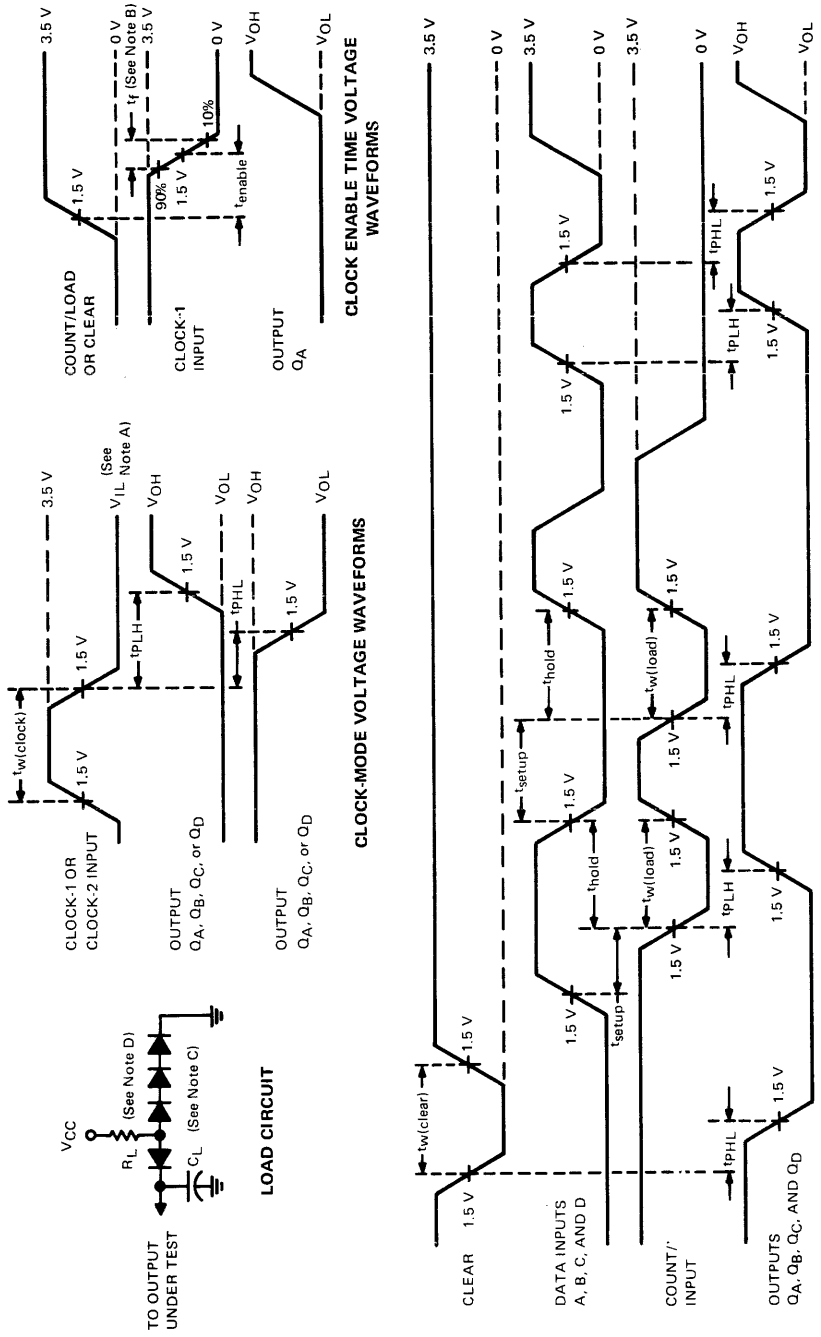


FIGURE 1

NOTES: A. The input pulse generator has the following characteristics: for testing f_{max}, $V_{IL} = 0.3 \pm 0.1$ V, duty cycle = 50%, $t_r < 5$ ns, and $t_f < 5$ ns; for all other measurements, $V_{IL} = 0$, PRR ≤ 1 MHz, duty cycle ≤ 50%, $t_r < 5$ ns, and unless otherwise specified, $t_f < 5$ ns.
B. Fall time of clock 1 is measured with count/load and clear high. When measuring clock enable time, $t_f < 5$ ns.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N3064.
E. Unless otherwise specified, Q_A is connected to clock 2.

9

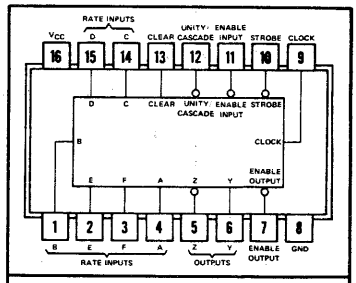
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN7497, SN74167
SYNCHRONOUS RATE MULTIPLIERS

SN7497 . . . 6-BIT BINARY MULTIPLIER
SN74167 . . . DECADE MULTIPLIER

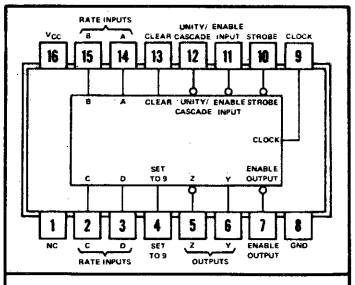
- Perform Fixed-Rate or Variable-Rate Frequency Division
- For Applications in Arithmetic, Radar, Digital-to-Analog (D/A), Analog-to-Digital (A/D), and other Conversion Operations
- Typical Maximum Clock Frequency . . . 32 Megahertz

SN7497
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See description

SN74167
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See description

NC—No internal connection

†Pin assignments for these circuits are the same for all packages.

description

These monolithic, fully synchronous, programmable counters utilize Series 54/74 TTL circuitry to achieve 32-megahertz typical maximum operating frequencies. The SN7497 is a six-bit serial binary counter; the SN74167 is a decade counter. These devices have buffered clock, clear, and enable inputs to control the operation of the counter, and a strobe input to enable or inhibit the rate input/decoding AND-OR-INVERT gates. The SN74167 also has a buffered set-to-nine input. The outputs have additional gating for cascading and transferring unity-count rates.

The counter is enabled when the clear, strobe, and enable inputs are low (for the decade counters, set-to-nine is also low). With the counter enabled the output frequency is equal to the input frequency multiplied by the rate input M and divided either by 64 (SN7497) or by 10 (SN74167), ie.:

$$\text{SN7497:}\quad f_{out} = \frac{M \cdot f_{in}}{64}$$

where: $M = F \cdot 2^5 + E \cdot 2^4 + D \cdot 2^3 + C \cdot 2^2 + B \cdot 2^1 + A \cdot 2^0$

$$\text{SN74167:}\quad f_{out} = \frac{M \cdot f_{in}}{10}$$

where: $M = D \cdot 2^3 + C \cdot 2^2 + B \cdot 2^1 + A \cdot 2^0$ for decimal zero through nine.

When the rate input is binary 0 (all rate inputs low), Z remains high. In order to cascade devices to perform 12-bit rate multiplication with the SN7497, or two-decade rate multiplication with the SN74167, the enable output is connected to the enable and strobe inputs of the next stage, the Z output of each stage is connected to the unity/cascade input of the other stage, and the sub-multiple frequency is taken from the Y output.

The unity/cascade input, when connected to the clock input, may be utilized to pass the clock frequency (inverted) to the Y output when the rate input/decoding gates are inhibited by the strobe. The unity/cascade input may also be used as a control for the Y output.

All of the inputs of these counters are diode-clamped, and each input, except the clock input, represents one normalized Series 54/74 load. The buffered clock input, used with the strobe gate, is only two Series 54/74 loads. Full fan-out to 10 Series 54/74 loads is available from each of the outputs. These devices are completely compatible with most TTL and DTL families. Typical power dissipation is 345 milliwatts for the SN7497, and 270 milliwatts for the SN74167. The SN7497 and SN74167 are characterized for operation from 0°C to 70°C.

description (continued)

SN7497

STATE AND/OR RATE TABLE (See Note A)

INPUTS										OUTPUTS			
			BINARY RATE							LOGIC LEVEL OR NUMBER OF PULSES			
CLEAR	ENABLE	STROBE	F	E	D	C	B	A	NUMBER OF CLOCK PULSES	UNITY/ CASCADE	Y	Z	ENABLE	NOTES
H	X	H	X	X	X	X	X	X	X	H	L	H	H	B
L	L	L	L	L	L	L	L	L	64	H	L	H	1	C
L	L	L	L	L	L	L	L	H	64	H	1	1	1	C
L	L	L	L	L	L	L	H	L	64	H	2	2	1	C
L	L	L	L	L	L	H	L	L	64	H	4	4	1	C
L	L	L	L	L	H	L	L	L	64	H	8	8	1	C
L	L	L	L	H	L	L	L	L	64	H	16	16	1	C
L	L	L	H	L	L	L	L	L	64	H	32	32	1	C
L	L	L	H	H	H	H	H	H	64	H	63	63	1	C
L	L	L	H	H	H	H	H	H	64	L	H	63	1	E
L	L	L	H	L	H	L	L	L	64	H	40	40	1	F

SN74167

STATE AND/OR RATE TABLE (See Note A)

INPUTS								OUTPUTS			
			BCD RATE					LOGIC LEVEL OR NUMBER OF PULSES			
CLEAR	ENABLE	STROBE	D	C	B	A	NUMBER OF CLOCK PULSES	UNITY/ CASCADE	Y	Z	ENABLE	NOTES
H	X	H	X	X	X	X	X	H	L	H	H	B
L	L	L	L	L	L	L	10	H	L	H	1	C
L	L	L	L	L	L	H	10	H	1	1	1	C
L	L	L	L	L	H	L	10	H	2	2	1	C
L	L	L	L	L	H	H	10	H	3	3	1	C
L	L	L	L	H	L	L	10	H	4	4	1	C
L	L	L	L	H	L	H	10	H	5	5	1	C
L	L	L	L	H	H	L	10	H	6	6	1	C
L	L	L	L	H	H	H	10	H	7	7	1	C
L	L	L	H	L	L	L	10	H	8	8	1	C
L	L	L	H	L	L	H	10	H	9	9	1	C
L	L	L	H	L	H	L	10	H	8	8	1	C, D
L	L	L	H	L	H	H	10	H	9	9	1	C, D
L	L	L	H	H	L	L	10	H	8	8	1	C, D
L	L	L	H	H	L	H	10	H	9	9	1	C, D
L	L	L	H	H	H	L	10	H	8	8	1	C, D
L	L	L	H	H	H	H	10	H	9	9	1	C, D
L	L	L	H	L	L	H	10	L	H	9	1	E

NOTES: A. H = high level, L = low level, X = irrelevant. All remaining entries are numeric counts.

B. This is a simplified illustration of the clear function. The states of clock and strobe can affect the logic level of Y and Z. A low (L) unity/cascade will cause output Y to remain high.

C. Each rate illustrated assumes a constant value at rate inputs; however, these illustrations in no way prohibit variable-rate inputs.

D. These input conditions exceed the range of the decimal rate inputs.

E. Unity/cascade is used to inhibit output Y.

F. $f_{out} = \frac{M \cdot f_{in}}{64} = \frac{(8 + 32)\, f_{in}}{64} = \frac{40\, f_{in}}{64} = 0.625\, f_{in}$

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Normalized fan-out from output, N				10	
Input clock frequency, f_{clock}		0		25	MHz
Width of clock pulse, $t_{w(clock)}$		20			ns
Width of clear pulse, $t_{w(clear)}$		15			ns
Width of set-to-nine pulse $t_{w(set\text{-}to\text{-}9)}$	SN74167	15			ns
Setup time, t_{setup}:	(See Figure 1)				
From positive-going transition of clock pulse		25			ns
From negative-going transition of previous clock pulse		0		$t_{w(clock)}-10$	ns
Hold time, t_{hold}:	(See Figure 1)				
From positive-going transition of clock pulse		0		$t_{w(clock)}-10$	ns
From negative-going transition of previous clock pulse		0		$t_{cp}-10$	ns
Operating free-air temperature, T_A		0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	clock input	V_{CC} = MAX, V_I = 2.4 V				80	μA
		other inputs					40	
I_{IL}	Low-level input current	clock inputs	V_{CC} = MAX, V_I = 0.4 V				−3.2	mA
		other inputs					−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−18		−55	mA
I_{CCH}	Supply current, high-level output		V_{CC} = MAX, See Note 2	SN7497		58		mA
				SN74167		43		
I_{CCL}	Supply current, low-level output		V_{CC} = MAX, See Note 3	SN7497		80	120	mA
				SN74167		65	99	

NOTES: 2. I_{CCH} is measured with outputs open and all inputs low.
3. I_{CCL} is measured with outputs open and all inputs high except the set-to-nine input of the SN74167, which is low.

†For test conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

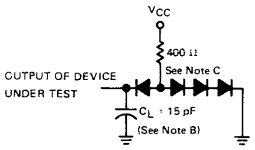
PARAMETER¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	32		MHz
t_{PLH}	Enable	Enable			13	20	ns
t_{PHL}					14	21	
t_{PLH}	Strobe	Z			12	18	ns
t_{PHL}					15	23	
t_{PLH}	Clock	Y			26	39	ns
t_{PHL}					20	30	
t_{PLH}	Clock	Z			12	18	ns
t_{PHL}					17	26	
t_{PLH}	Rate	Z			9	14	ns
t_{PHL}					6	10	
t_{PLH}	Unity/Cascade	Y			9	14	ns
t_{PHL}					6	10	
t_{PLH}	Strobe	Y			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clock	Enable			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clear	Y			24	36	ns
t_{PHL}		Z			15	23	
t_{PHL} (SN74167 only)	Set-to-9	Enable			18	27	ns
t_{PLH}	Any Rate Input	Y			15	23	ns
t_{PHL}					15	23	

¶f_{max} is maximum input clock frequency.
t_{PLH} is propagation delay time, low-to-high-level output.
t_{PHL} is propagation delay time, high-to-low-level output.

9

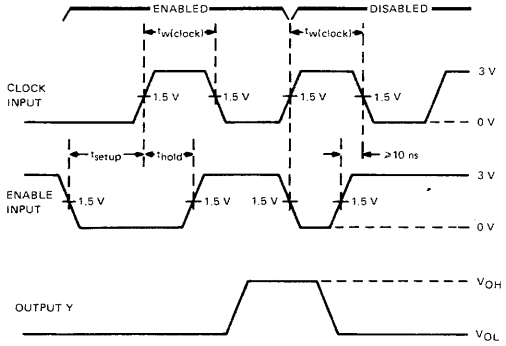
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

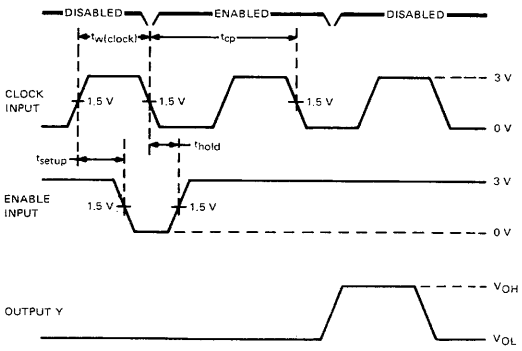


All three outputs are loaded during testing

LOAD CIRCUIT

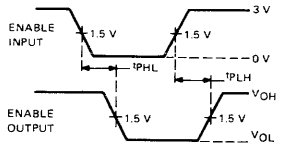


ENABLING FROM POSITIVE-GOING TRANSITION OF CLOCK PULSE



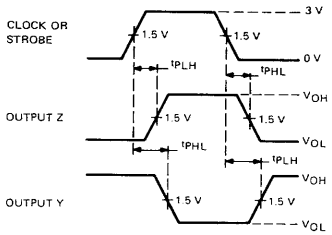
ENABLING FROM NEGATIVE-GOING TRANSITION OF PREVIOUS CLOCK PULSE

1. Unity/cascade and rate inputs are high, other inputs are low, and flip-flops are at any count other than maximum or one count before maximum.
2. Setup and hold times are illustrated for enabling a single clock pulse (count). Continued application of the enable function will enable subsequent clock pulses (counts) until disabling occurs (enable goes high). The total number of counts will be determined by the total number of positive-going clock transitions enabled.



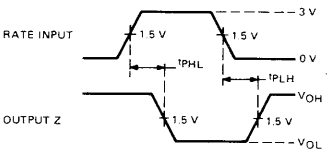
Flip-flops are at the maximum count. Other inputs are low.

PROPAGATION DELAY TIMES, ENABLE INPUT TO ENABLE OUTPUT



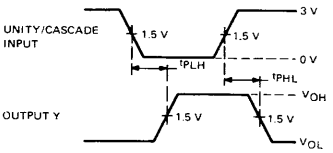
Unity/cascade and rate inputs are high, other inputs are low, and flip-flops are at any count other than maximum.

PROPAGATION DELAY TIMES, CLOCK TO Z AND Y, AND STROBE INPUT TO Z AND Y



Flip-flops are at a count so that all other inputs to the gate under test are high all other inputs, including other rate inputs, are low.

PROPAGATION DELAY TIMES, RATE INPUT TO Z



Output Z is high.

PROPAGATION DELAY TIMES, UNITY/CASCADE INPUT TO Y

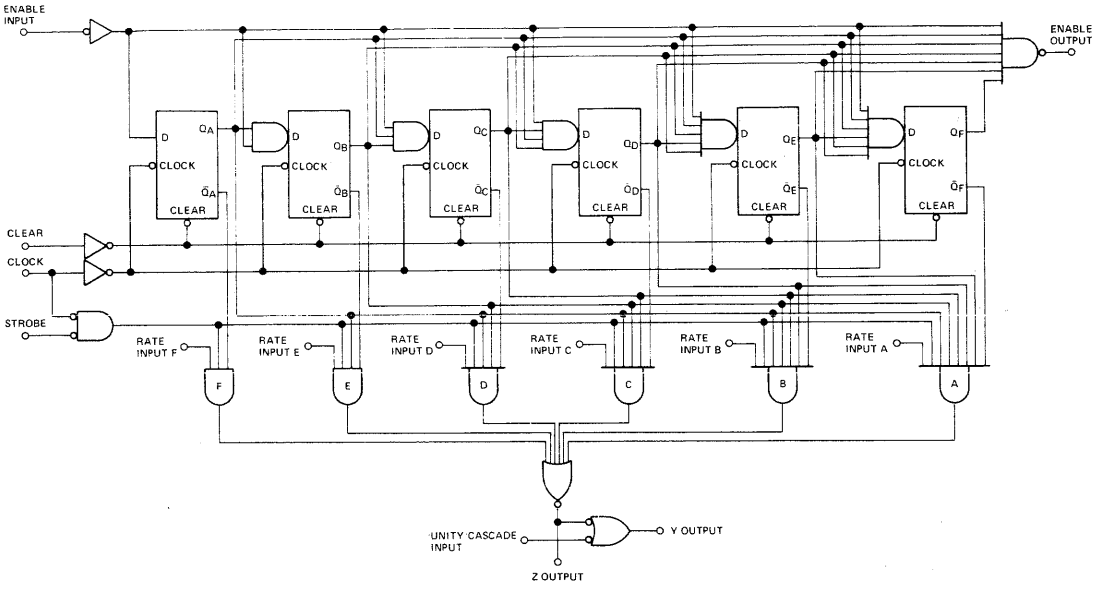
NOTES: A. The input pulse generator has the following characteristics: $t_{w(clock)} = 20$ ns, $t_{TLH} \leq 10$ ns, $t_{THL} \leq 10$ ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 1–SWITCHING TIMES

CIRCUIT TYPES SN7497, SN74167
SYNCHRONOUS RATE MULTIPLIERS

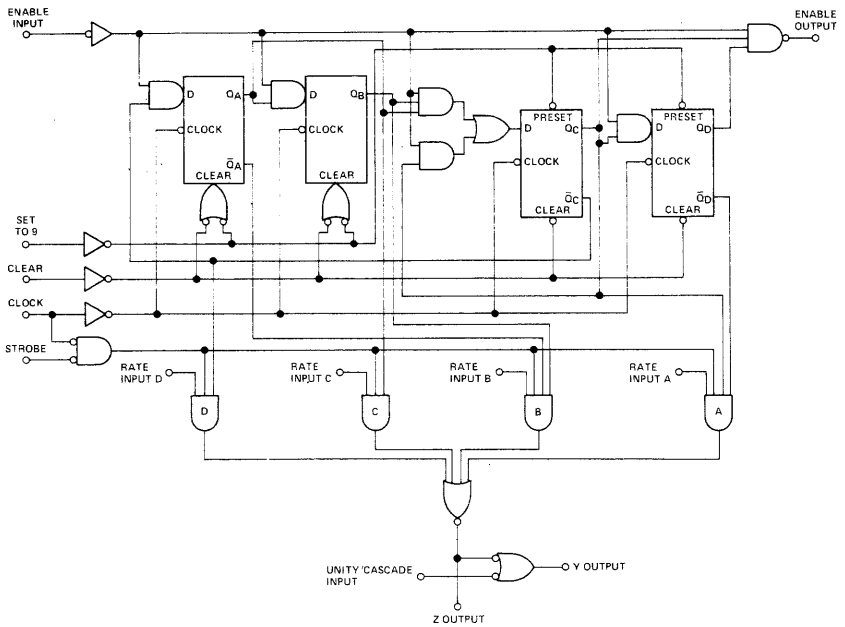
SN7497 BINARY COUNTER

functional block diagram



SN74167 DECADE COUNTER

functional block diagram



9

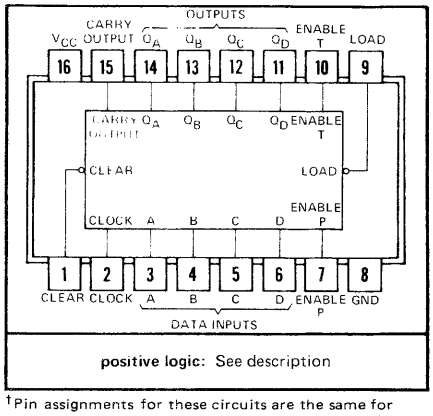
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54160 THRU SN54163, SN74160 THRU SN74163
SYNCHRONOUS 4-BIT COUNTERS

SN54160, SN54161, SN74160, SN74161, . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
SN54162, SN54163, SN74162, SN74163 . . . FULLY SYNCHRONOUS COUNTERS

- Internal Look-Ahead for Fast Counting Schemes
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs
- Typical Maximum Input Clock Frequency . . . 32 MHz

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See description

†Pin assignments for these circuits are the same for all packages.

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting schemes. The SN54160, SN54162, SN74160, and SN74162 are decade counters and the SN54161, SN54163, SN74161, and SN74163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either state. As presetting is synchronous, placing a low level on the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse. The clear function for the SN54160, SN54161, SN74160, and SN74161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the state of the clock. The clear function for the SN54162, SN54163, SN74162, and SN74163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously set the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q_A output. This positive overflow carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs should occur only when the clock input is high.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. A full fan-out to ten normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs to used inputs. Input clock frequency is typically 32 megahertz and power dissipation is typically 325 milliwatts.

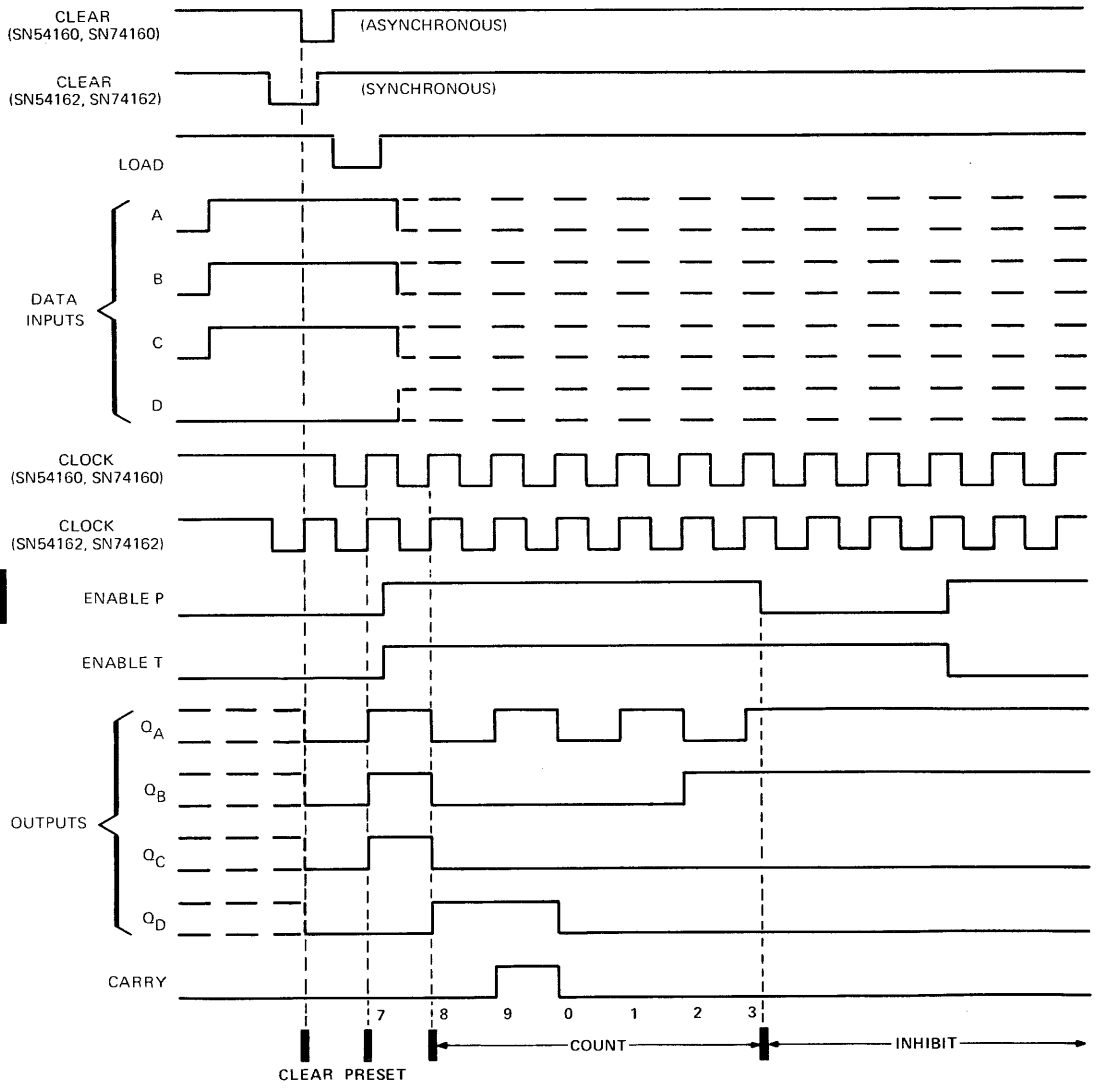
Series 54 circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 circuits are characterized for operation from 0°C to 70°C.

SN54160, SN54162, SN74160, SN74162 SYNCHRONOUS DECADE COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit



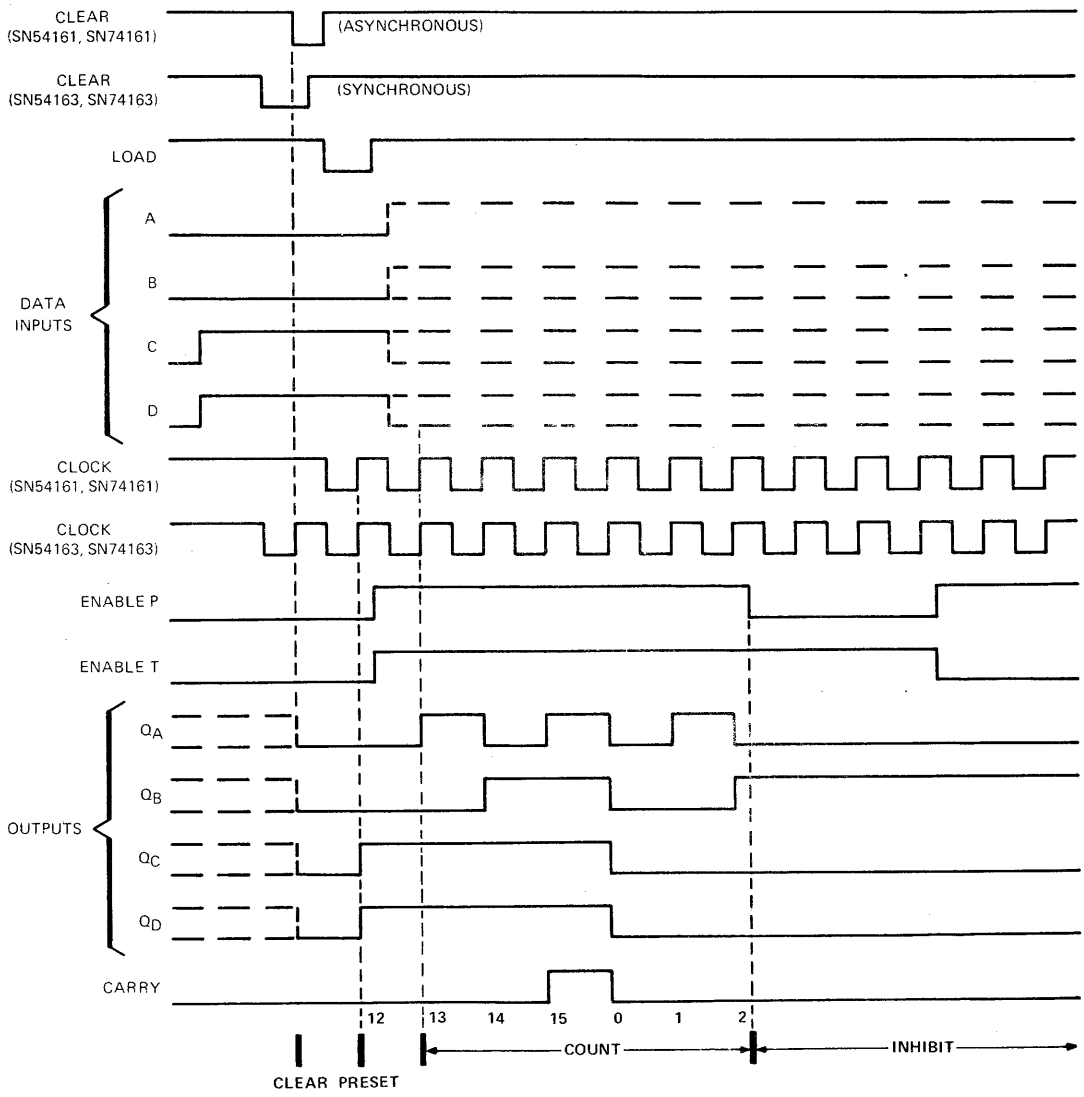
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SN54161, SN54163, SN74161, SN74163 SYNCHRONOUS BINARY COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.



9

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range:
SN54160, SN54161, SN54162, SN54163 Circuits . . . . . −55°C to 125°C
SN74160, SN74161, SN74162, SN74163 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.

recommended operating conditions

		SN54160, SN54161, SN54162, SN54163			SN74160, SN74161, SN74162, SN74163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{setup} (see Figures 1 and 3)	Data inputs A, B, C, D	15			15			ns
	Enable P	20			20			
	Load	15			15			
	Clear◇	20			20			
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

◇This applies only for SN54162, SN54163, SN74162, and SN74163 which have synchronous clear inputs.

electrical characteristics over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER			TEST CONDITIONS†	SN54160, SN54161, SN54162, SN54163			SN74160, SN74161, SN74162, SN74163			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MAX, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Clock or enable T	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	Clock or enable T	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
		Other inputs				−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = MAX, See Note 3		59	85		59	94	mA
I_{CCL}	Supply current, all outputs low		V_{CC} = MAX, See Note 4		63	91		63	101	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

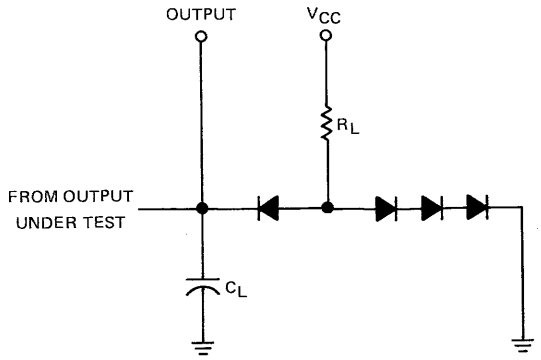
NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	1,2	C_L = 15 pF, R_L = 400 Ω	25	32		MHz
t_{PLH}	Propagation delay time, low-to-high-level carry output from clock	1,2			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from clock	1,2			23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from clock	1,2			13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clock	1,2			15	23	ns
t_{PLH}	Propagation delay time, low-to-high-level carry output from enable T	1,3			8	13	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from enable T	1,3			10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clear	1,3			20	30	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.

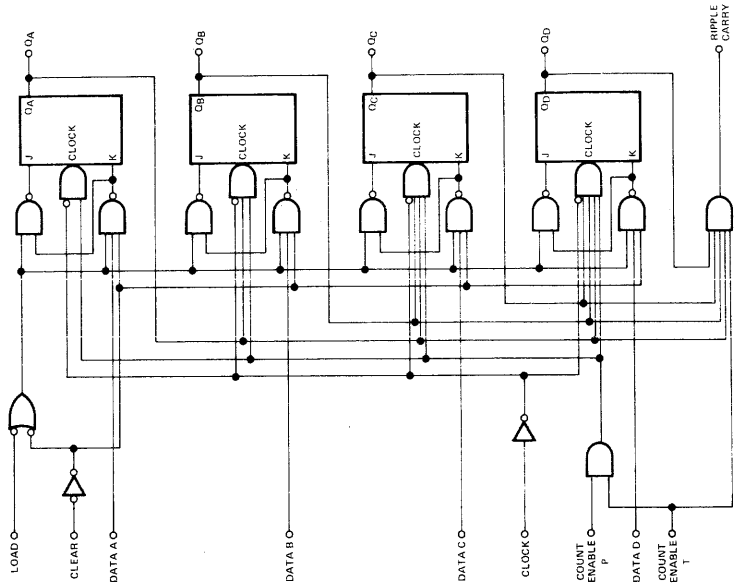
LOAD CIRCUIT FOR SWITCHING TESTS
FIGURE 1

9

functional block diagrams

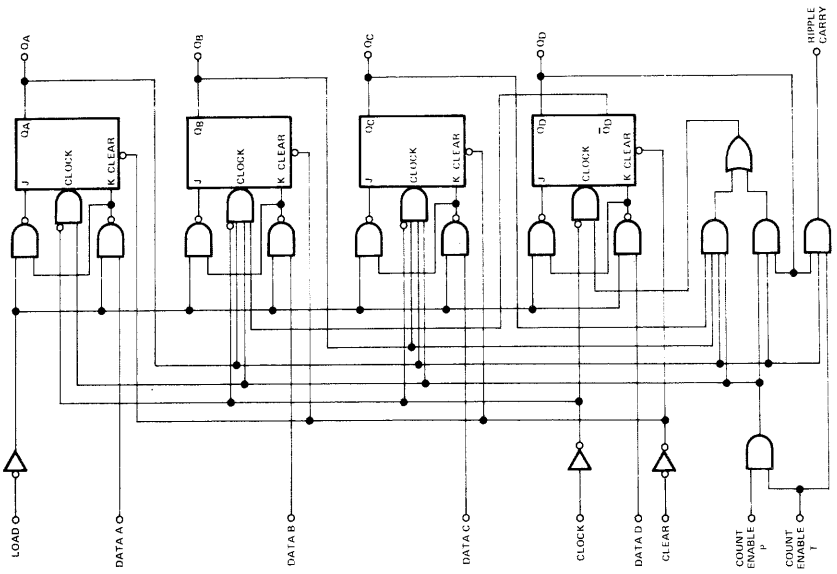
SN54163, SN74163 SYNCHRONOUS BINARY COUNTERS

SN54161, SN74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54160, SN74160 decade counters at left.



SN54160, SN74160 SYNCHRONOUS DECADE COUNTERS

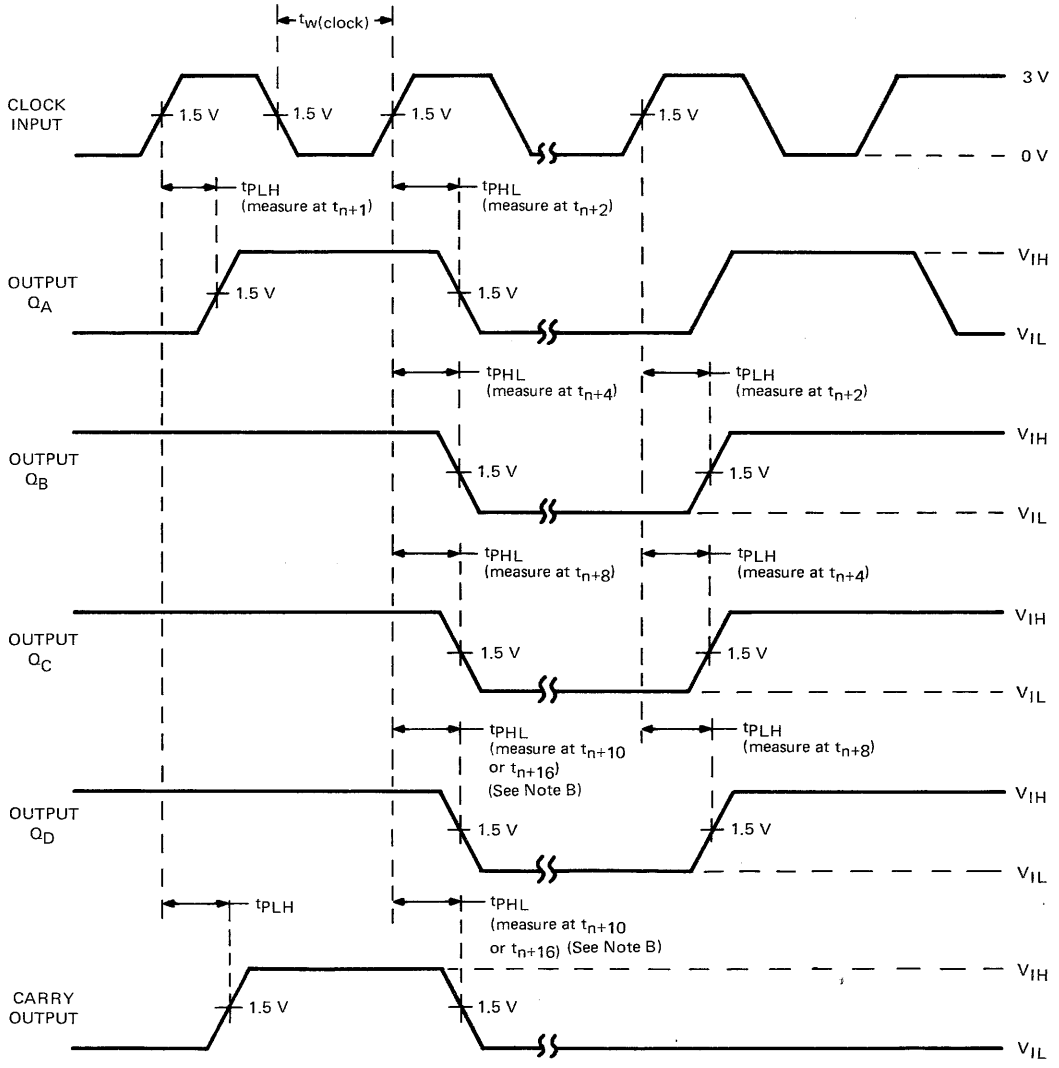
SN54162, SN74162 synchronous decade counters are similar; however the clear is synchronous as shown for the SN54163, SN74163 binary counters at right.



9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

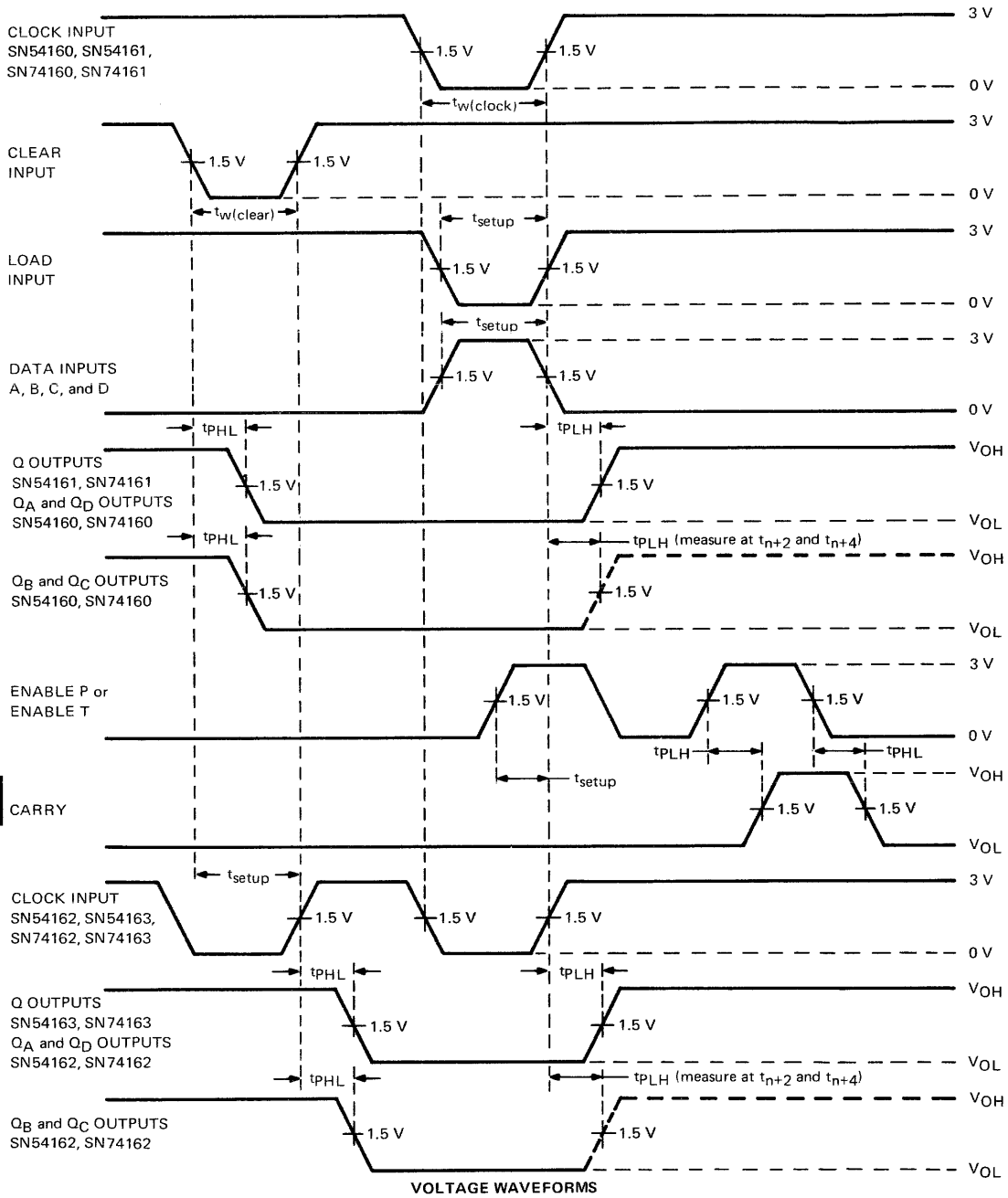
NOTES: A. The input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\ \Omega$. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} for the SN54160, SN54162, SN74160, and SN74162, and at t_{n+16} for the SN54161, SN54163, SN74161, and SN74163, where t_n is the bit time when all outputs are low.

FIGURE 2–SWITCHING TIMES

9

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\ \Omega$.

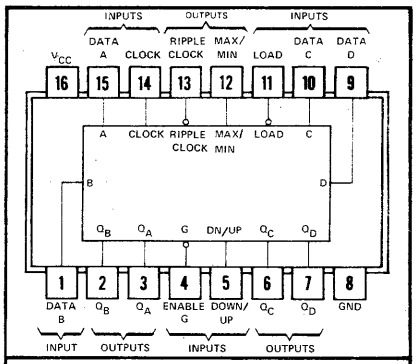
B. Enable P and enable T setup times are measured at $t_n = 0$.

FIGURE 3–SWITCHING TIMES

CIRCUIT TYPES SN54190, SN54191, SN74190, SN74191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

- Counts 8-4-2-1 BCD or Binary
- Single Down/Up Count Control Line
- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presettable with Load Control
- Parallel Outputs
- Cascadable for n-Bit Applications
- Typical Average Propagation Delay (Clock to Q Output) . . . 20 ns
- Typical Power Dissipation . . . 325 mW
- Typical Maximum Clock Frequency . . . 25 MHz

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



asynchronous inputs: Low input to load sets Q_A=A, Q_B = B, Q_C = C, and Q_D = D

†Pin assignments for these circuits are the same for all packages.

description

The SN54190, SN54191, SN74190, and SN74191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The SN54191 and SN74191 are 4-bit binary counters and the SN54190 and SN74190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation will eliminate the output counting spikes which are normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the state of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the state of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Input buffers have been used to lower the fan-in requirement to only one normalized Series 54/74 load at all inputs except enable. This is important when the output of the driving circuitry is somewhat limited.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Power dissipation is typically 325 milliwatts for either the decade or binary version. Maximum input clock frequency is typically 25 megahertz and is guaranteed to be at least 20 megahertz.

The SN54190 and SN54191 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74190 and SN74191 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54190, SN54191 . . . . . −55°C to 125°C
SN74190, SN74191 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

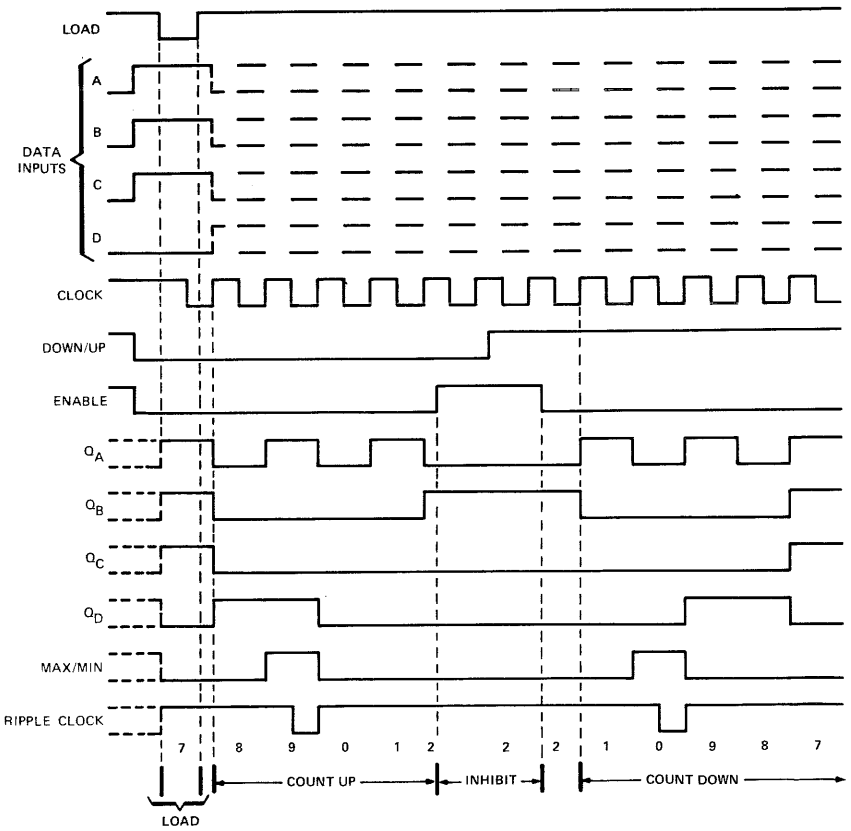
NOTE 1: Voltage values are with respect to network ground terminal.

SN54190, SN74190 DECADE COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

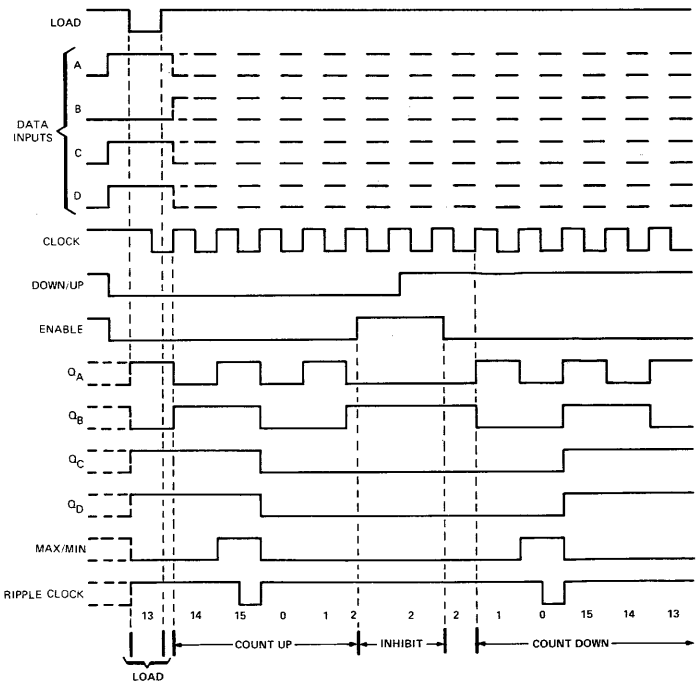
		SN54190, SN54191			SN74190, SN74191			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$		25			25			ns
Width of load input pulse, $t_{w(load)}$		35			35			ns
Data setup time, t_{setup} (See Figures 1 and 2)		20			20			ns
Data hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

SN54191, SN74191 BINARY COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



9

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54190, SN54191			SN74190, SN74191			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	V_{CC} = MIN	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = MIN			0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_I	High-level input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current at any input except enable	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IH}	High-level input current at enable input				120			120	μA
I_{IL}	Low-level input current at any input except enable	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{IL}	Low-level input current at enable input				−4.8			−4.8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−65	−18		−65	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		65	105		65	105	mA

†For conditions shown as MAX or MIN, use appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

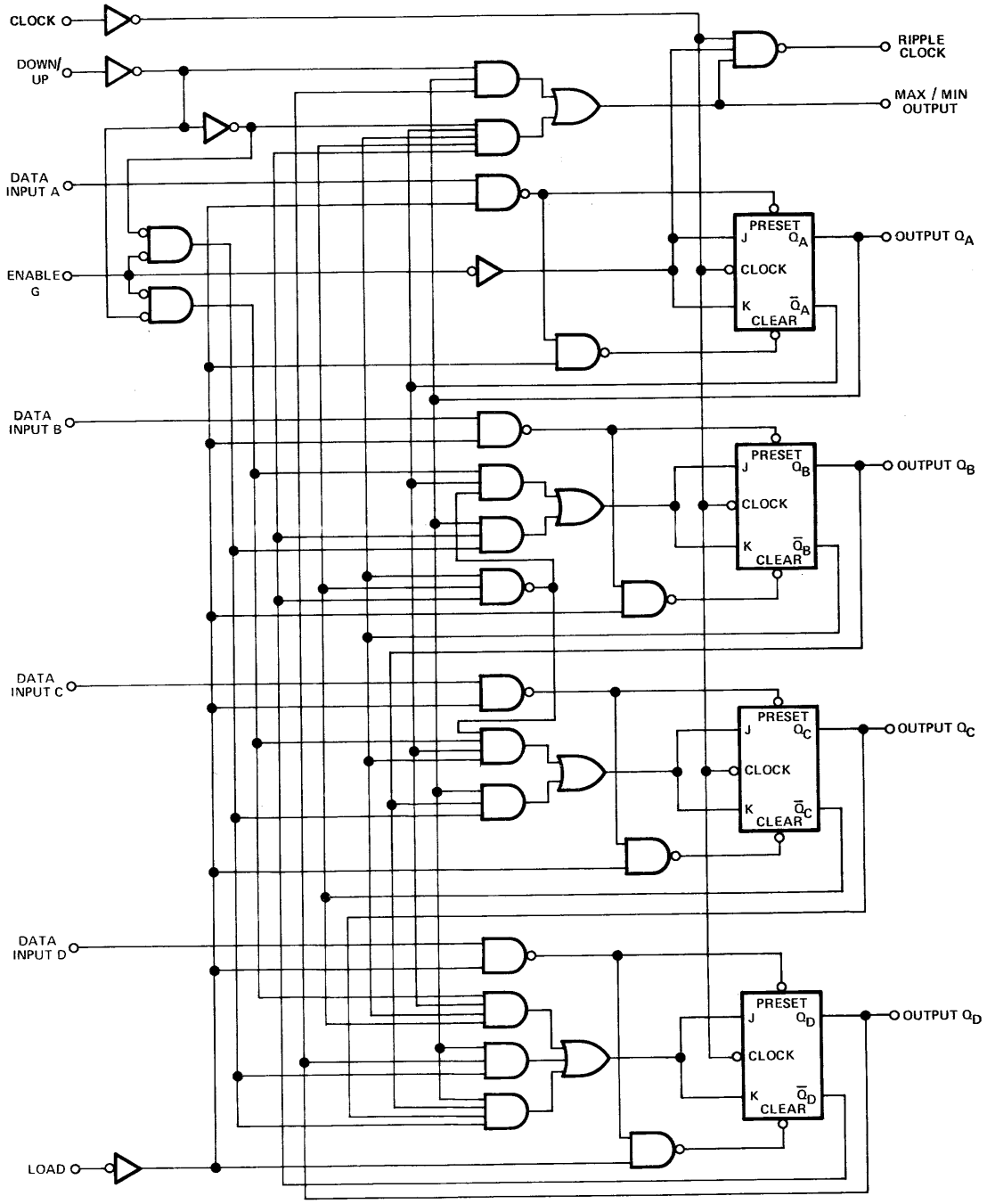
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figure 1 and Figures 3 thru 7	20	25		MHz
t_{PLH}	Load	Q_A, Q_B, Q_C, Q_D			22	33	ns
t_{PHL}					33	50	
t_{PLH}	Data A, B, C, D	Q_A, Q_B, Q_C, Q_D			14	22	ns
t_{PHL}					35	50	
t_{PLH}	Clock	Ripple Clock			13	20	ns
t_{PHL}					16	24	
t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D			16	24	ns
t_{PHL}					24	36	
t_{PLH}	Clock	Max/Min			28	42	ns
t_{PHL}					37	52	
t_{PLH}	Down/Up	Ripple Clock			30	45	ns
t_{PHL}					30	45	
t_{PLH}	Down/Up	Max/Min			21	33	ns
t_{PHL}					22	33	

¶f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

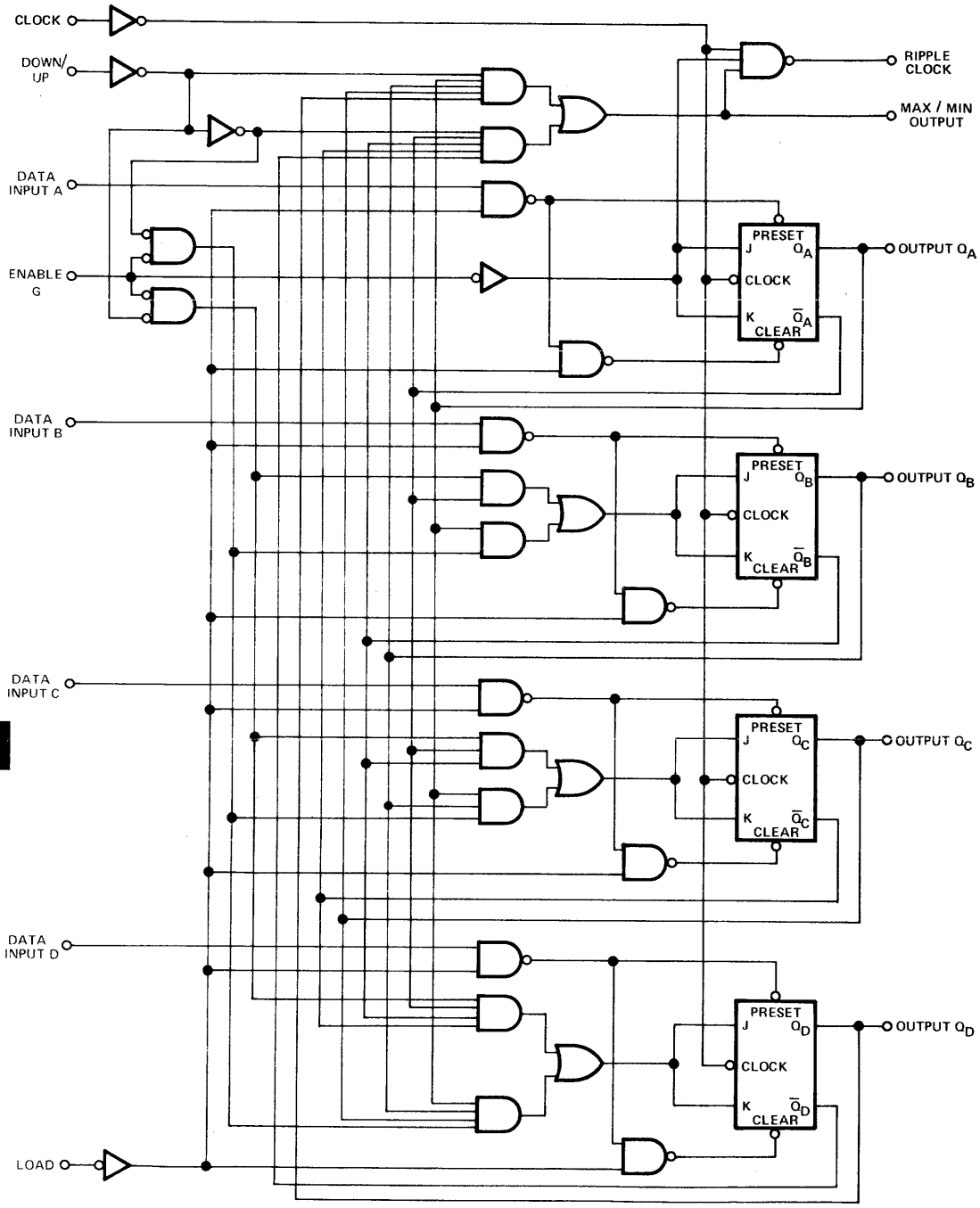
functional block diagram SN54190, SN74190 DECADE COUNTERS



9

functional block diagram

SN54191, SN74191 BINARY COUNTERS



9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

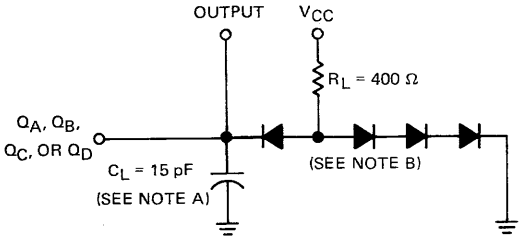


FIGURE 1–LOAD CIRCUIT
FOR SWITCHING TIME MEASUREMENT

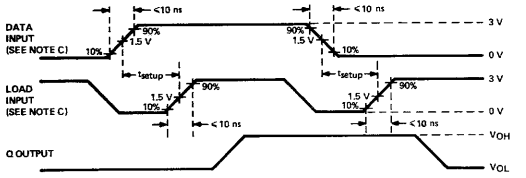
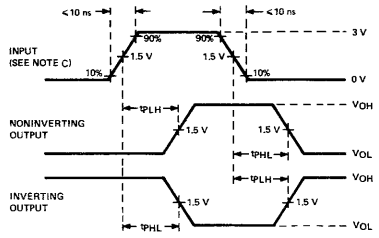


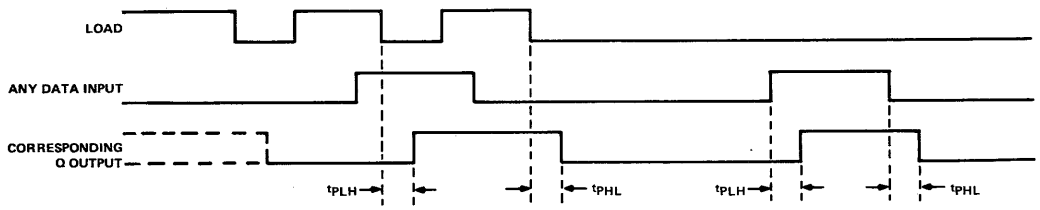
FIGURE 2–SETUP TIME VOLTAGE WAVEFORMS



See waveform sequences in figures 4 through 7 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in figures 4 through 7.

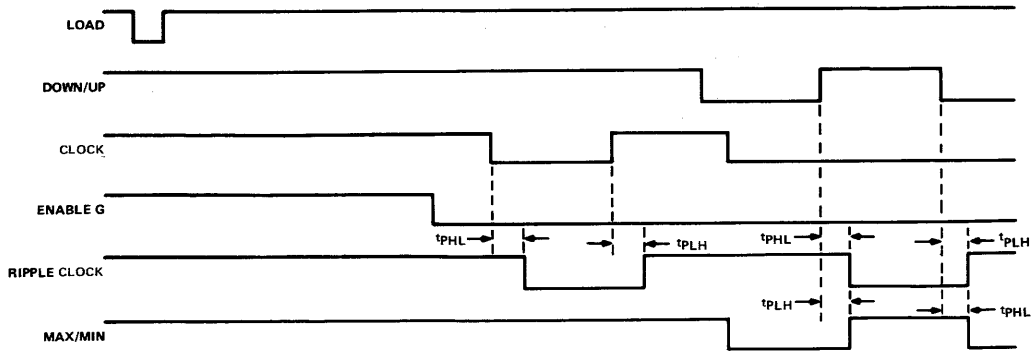
FIGURE 3–GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.
C. The input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 50%, PRR ≤ 1 MHz.



NOTE D: Conditions on other inputs are irrelevant.

FIGURE 4–LOAD TO OUTPUT AND DATA TO OUTPUT



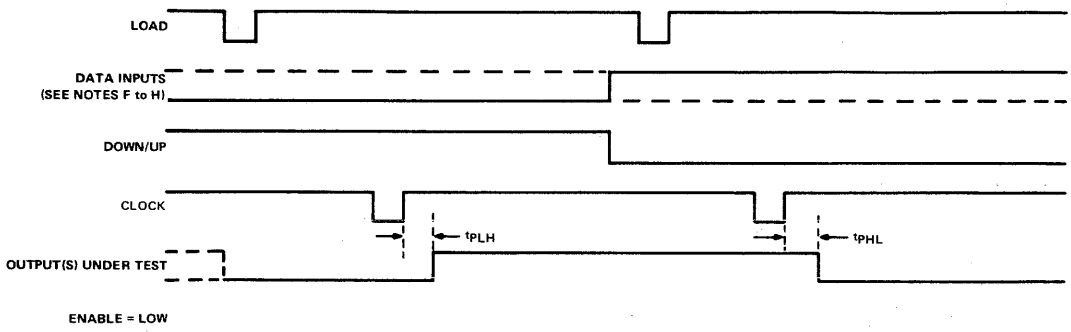
NOTE E: All data inputs are low.

FIGURE 5–ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO RIPPLE CLOCK, AND DOWN/UP TO MAX/MIN

9

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

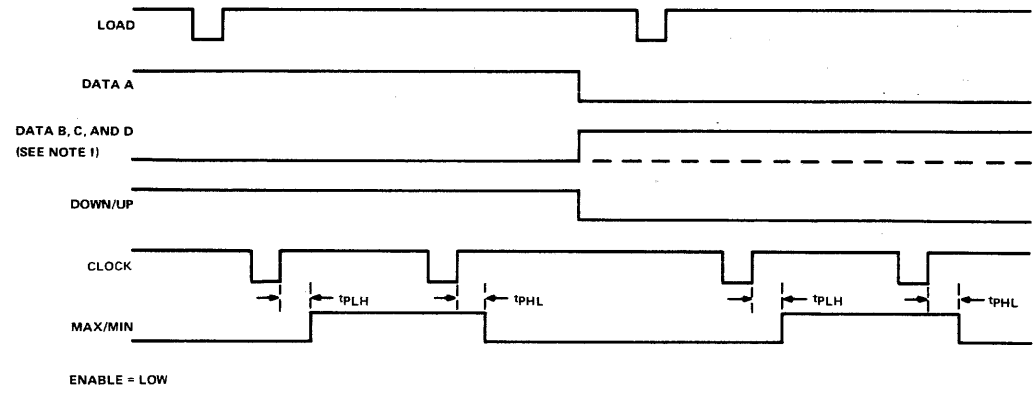


NOTES: F. To test Q_A, Q_B, and Q_C outputs of SN54190: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.

G. To test Q_D output of SN54190: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the low logic level.

H. To test Q_A, Q_B, Q_C, and Q_D outputs of SN54191: All four data inputs are shown by the solid line.

FIGURE 6–CLOCK TO OUTPUT



NOTE I: Data inputs B and C are shown by the dashed line for SN54190 and the solid line for SN54191. Data input D is shown by the solid line for both devices.

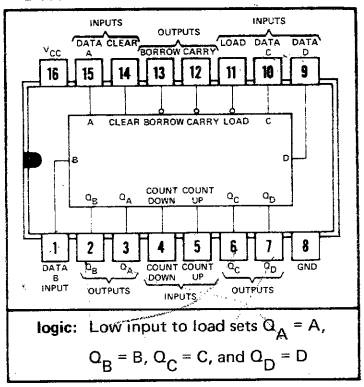
FIGURE 7–CLOCK TO MAX/MIN

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54192, SN54193, SN74192, SN74193
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

- Cascading Circuitry Provided Internally
- Synchronous Operation
- Individual Preset to Each Flip-Flop
- Fully Independent Clear Input
- Typical Maximum Input Count Frequency . . . 32 MHz

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

description

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The SN54192 and SN74192 are BCD counters and the SN54193 and SN74193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, the outputs may be preset to any state by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. An input buffer has been placed on the clear, count, and load inputs to lower the drive requirements to one normalized Series 54/74 load. This is important when the output of the driving circuitry is somewhat limited.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

Power dissipation is typically 325 milliwatts for either the decade or binary version. Maximum input count frequency is typically 32 megahertz and is guaranteed to be 25 MHz minimum. All inputs are buffered and represent only one normalized Series 54/74 load. Input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design. The SN54192 and SN54193 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74192 and SN74193 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Operating free-air temperature range: SN54192 and SN54193 Circuits	−55°C to 125°C
SN74192 and SN74193 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

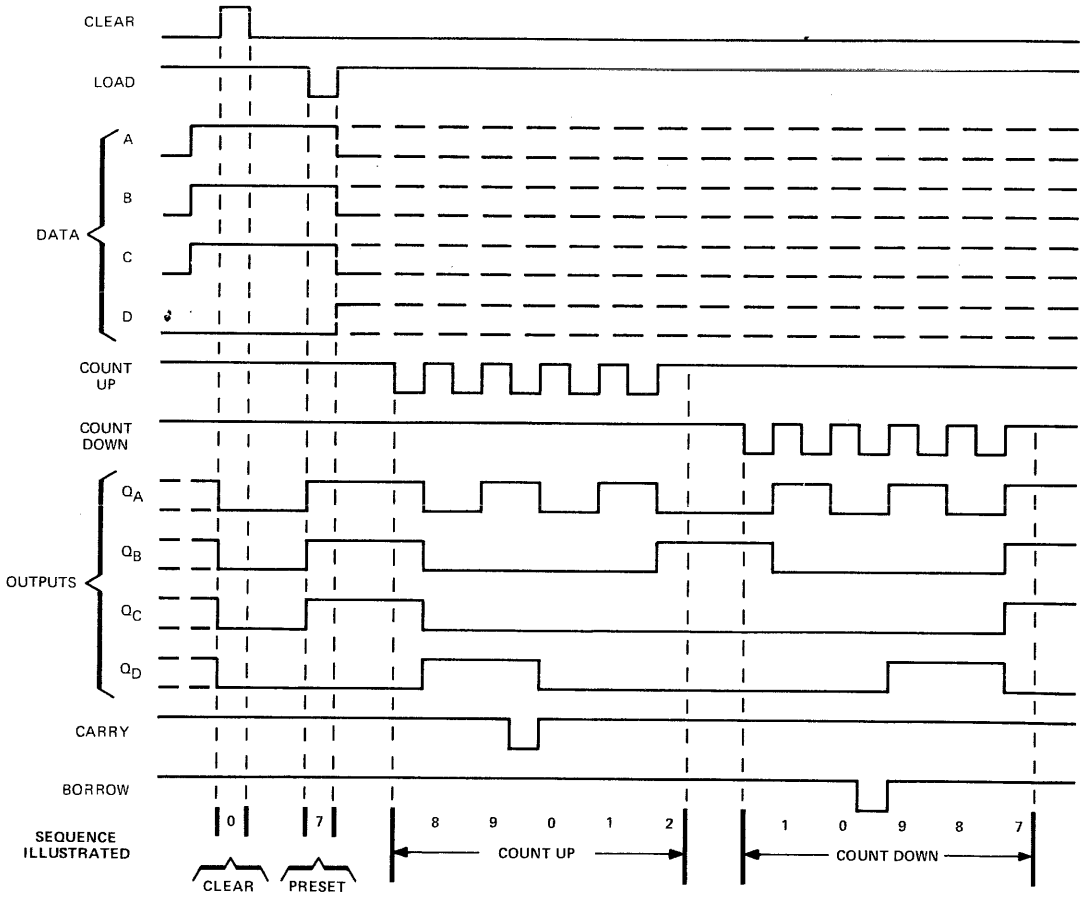
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SN54192, SN74192 DECADE COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

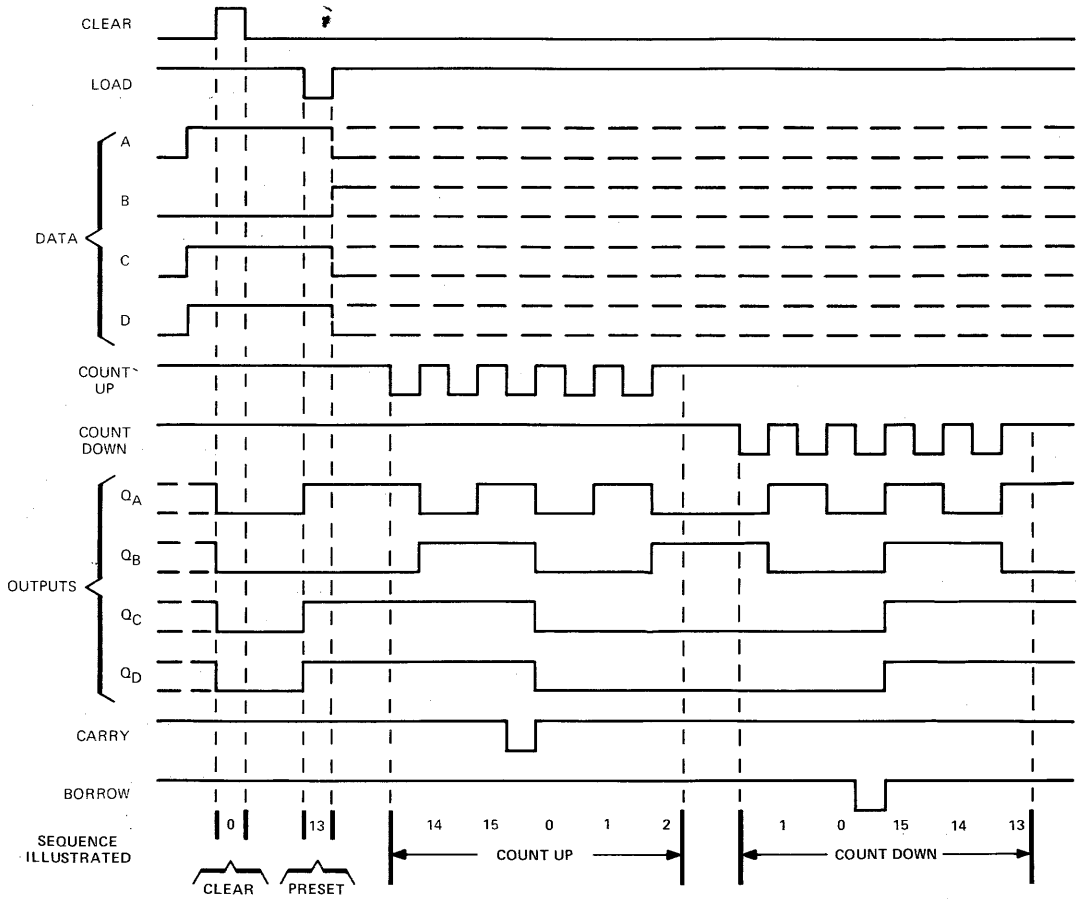
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SN54193, SN74193 BINARY COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

CIRCUIT TYPES SN54192, SN54193, SN74192, SN74193
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

recommended operating conditions

	SN54192, SN54193			SN74192, SN74193			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Input count frequency, f_{count}	0		25	0		25	MHz
Width of any input pulse, t_w	20			20			ns
Data setup time, t_{setup} (see Figure 7 and Note 2)	20			20			ns
Data hold time, t_{hold} (see Note 3)	0			0			ns
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

NOTES: 2. Setup time is the interval immediately preceding the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

3. Hold time is the interval immediately following the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	SN54192, SN54193			SN74192, SN74193			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1 and 2		2			2			V
V_{IL}	Low-level input voltage	1 and 2				0.8			0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_{IH}	High-level input current	3	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IL}	Low-level input current	4	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	−20		−65	−18		−65	mA
I_{CC}	Supply current	6	V_{CC} = MAX		65	89		65	102	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

9

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER¶	FROM INPUT	TO OUTPUT	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				C_L = 15 pF, R_L = 400 Ω	25	32		MHz
t_{setup}			7			14	20	ns
t_{PLH}	Count-up	Carry	8			17	26	ns
t_{PHL}						16	24	
t_{PLH}	Count-down	Borrow	8			16	24	ns
t_{PHL}						16	24	
t_{PLH}	Either Count	Q	8			25	38	ns
t_{PHL}						31	47	
t_{PLH}	Load	Q	7			27	40	ns
t_{PLH}						29	40	
t_{PHL}	Clear	Q	7			22	35	ns

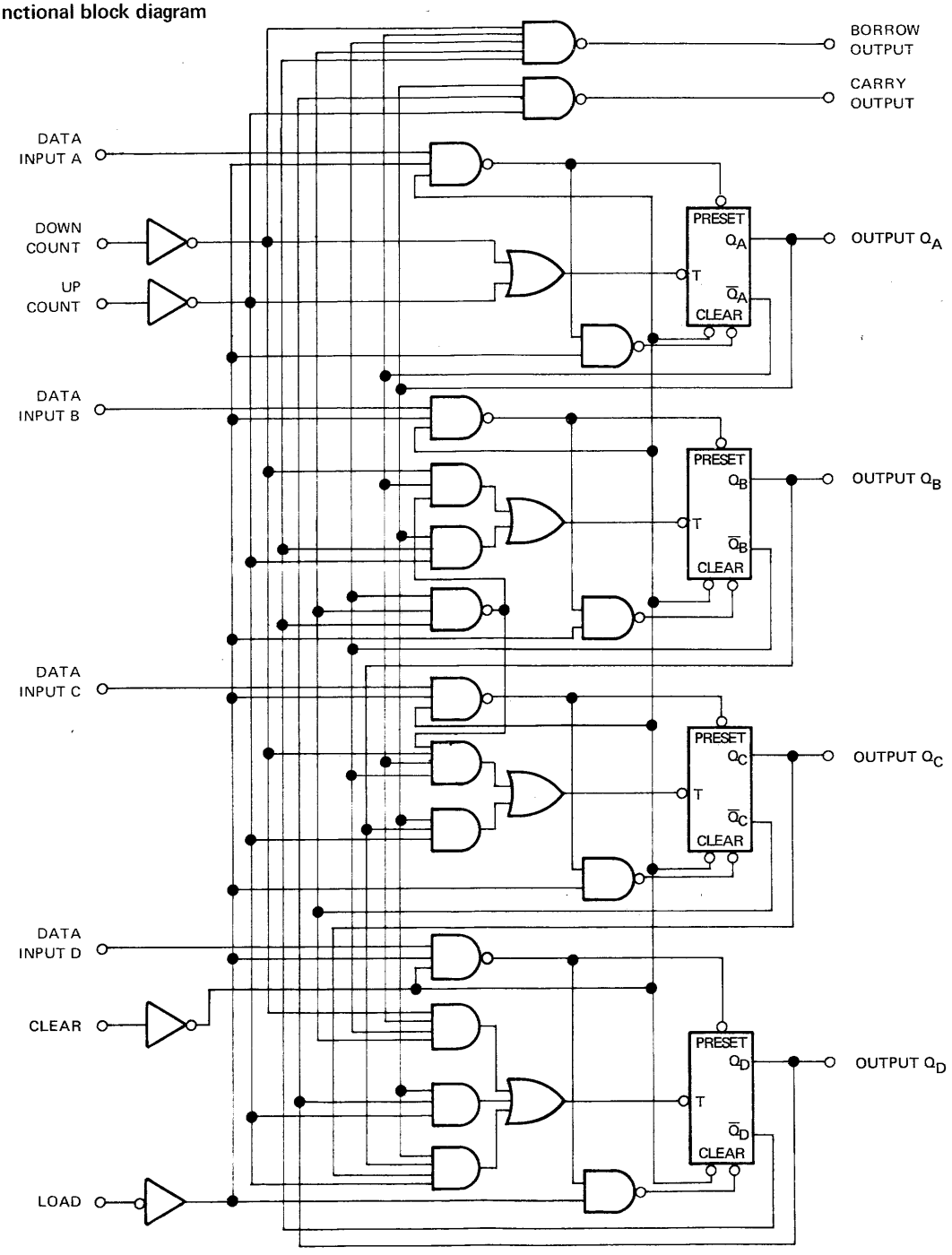
¶f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

17

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SN54192, SN74192 DECADE COUNTER

functional block diagram

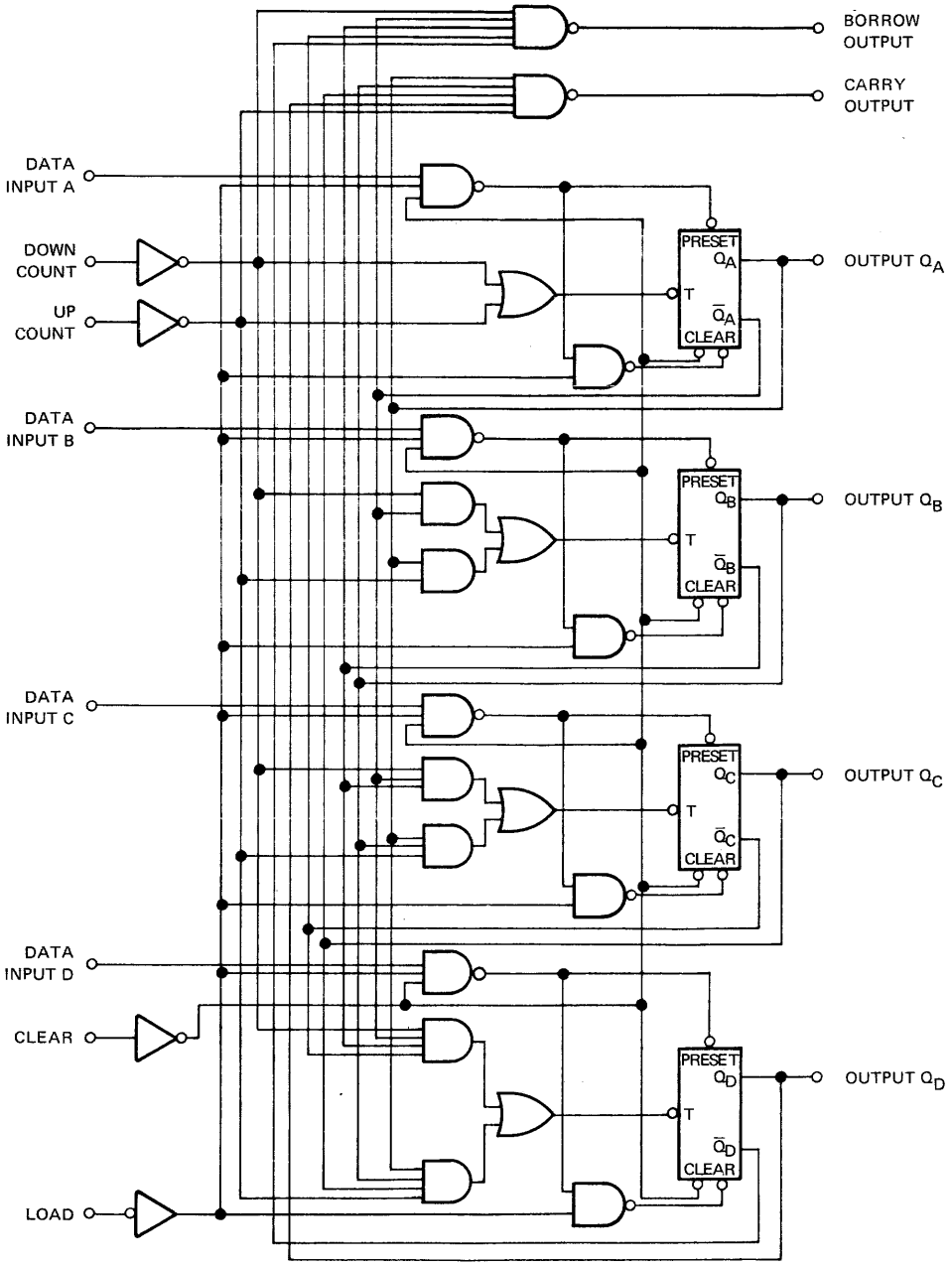


9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SN54193, SN74193 BINARY COUNTER

functional block diagram

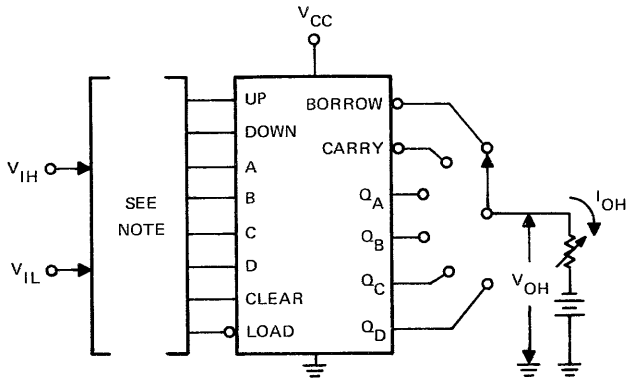


9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

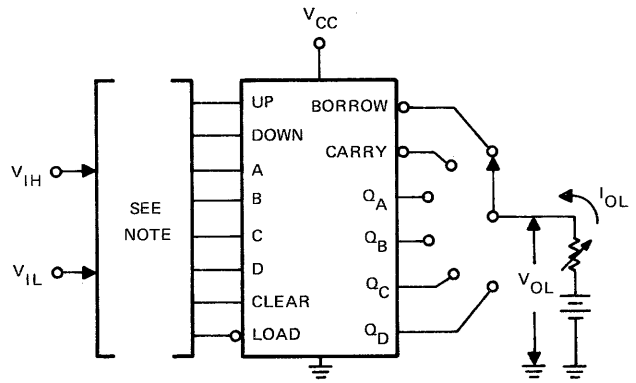
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶



Each output is tested separately.

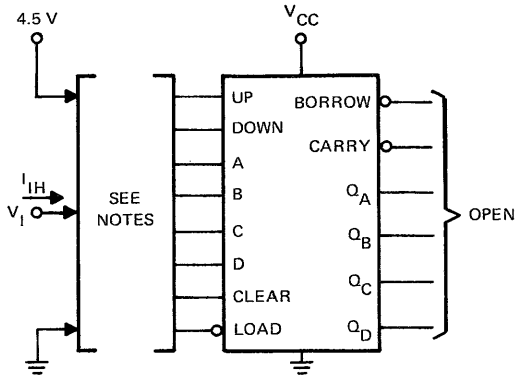
FIGURE 1–V_{IH}, V_{IL}, V_{OH}



Each output is tested separately.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}

9



NOTES: A. Each input is tested separately.

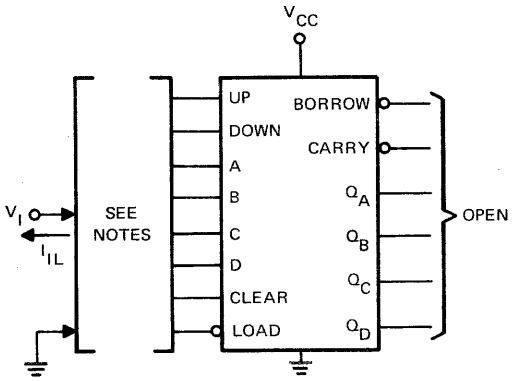
B. Apply V_I to input under test, and ground other inputs except when testing data inputs, apply 4.5 V to clear and load inputs.

FIGURE 3–I_{IH}

¶Arrows indicate actual direction of current flow. Current into a ter. inal is a positive value.

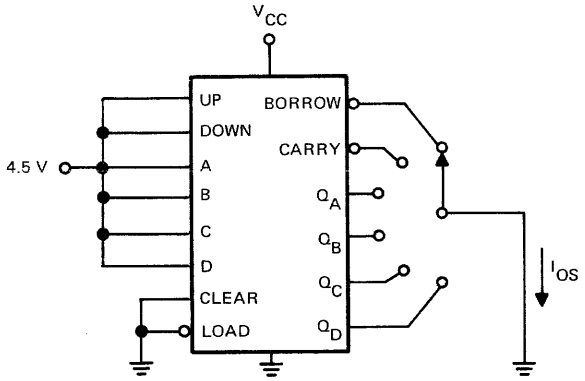
PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)¶



NOTES: A. Each input is tested separately.
B. Apply V_I to input under test and ground other inputs.

FIGURE 4–I_{IL}



Each output is tested separately in the high-level state.

FIGURE 5–I_{OS}

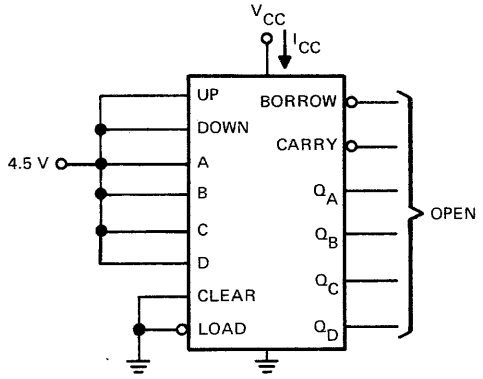


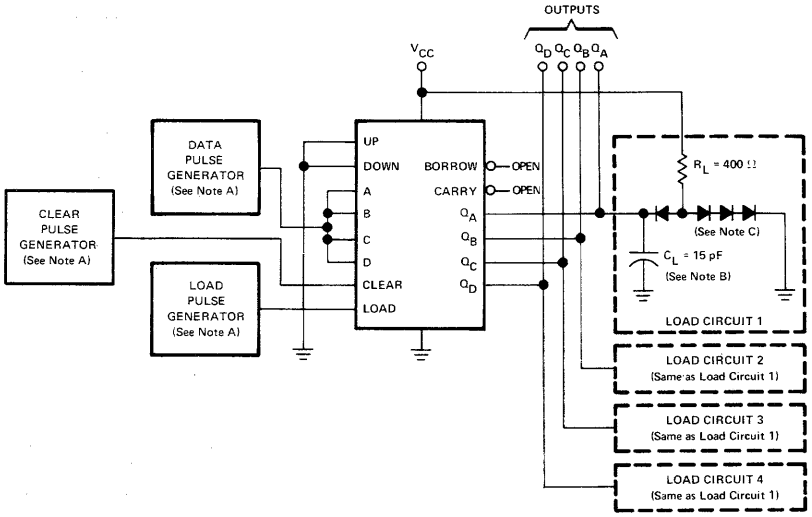
FIGURE 6–I_{CC}

¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

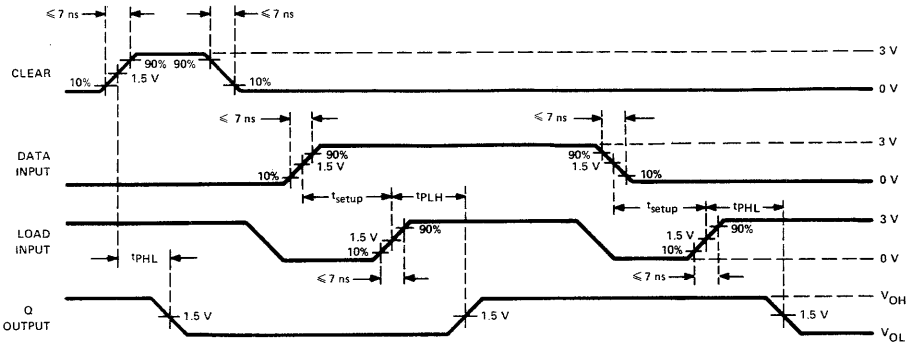
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

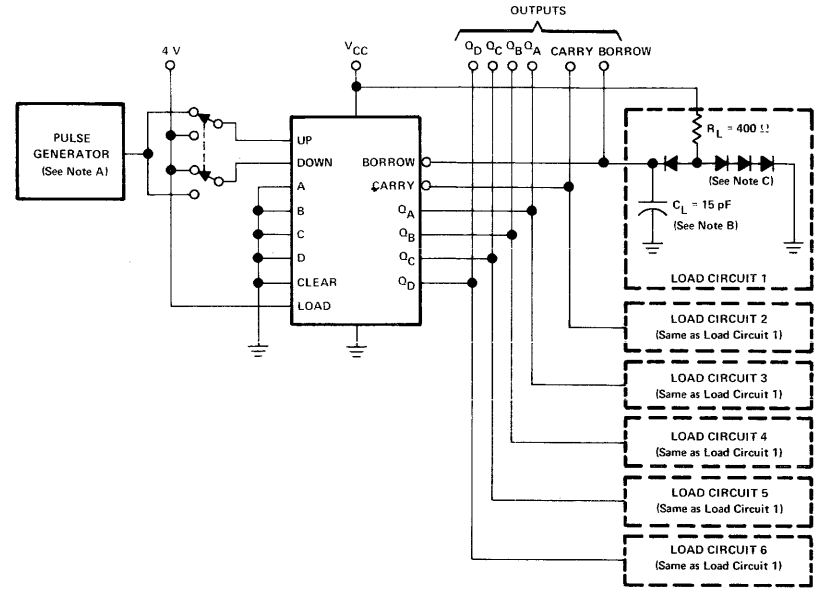
NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$; for the data pulse generator, PRR = 500 kHz, duty cycle = 50%; for the load pulse generator, PRR = 1 MHz, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 7–CLEAR, SETUP, AND LOAD TIMES

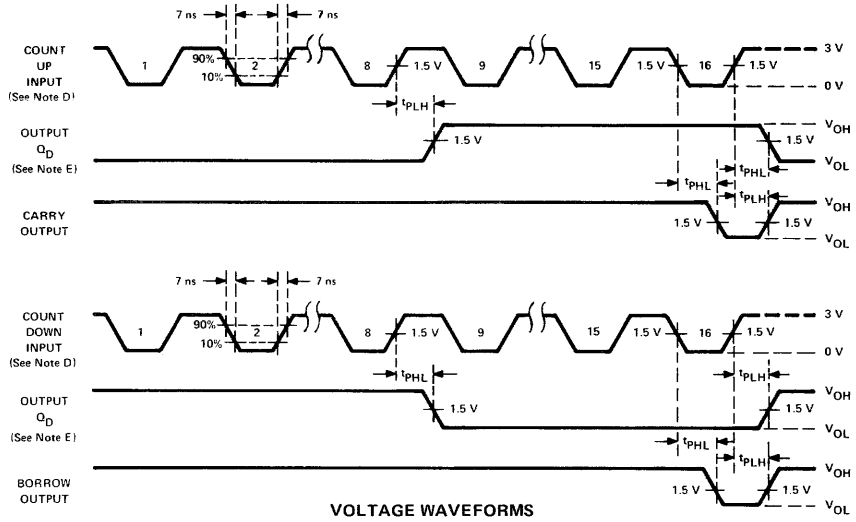
9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. Count-up and count-down pulses shown are for the SN54193/SN74193 binary counters. Count cycle for SN54192 decade counter is 1 through 10.
E. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.

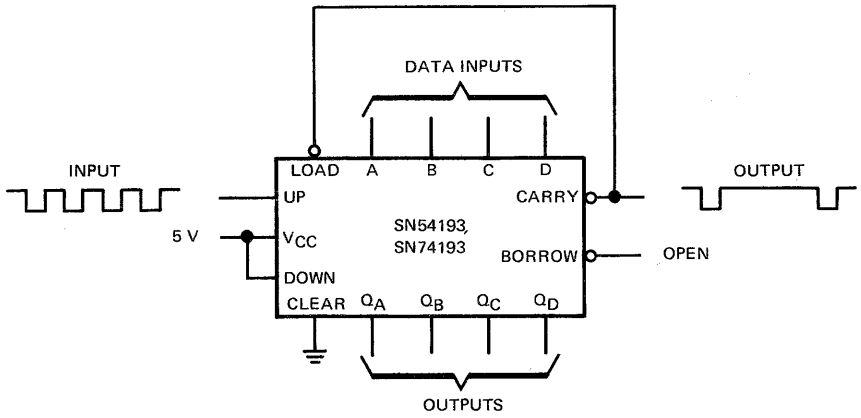
FIGURE 8–PROPAGATION DELAY TIMES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATION DATA

modulo-N divider

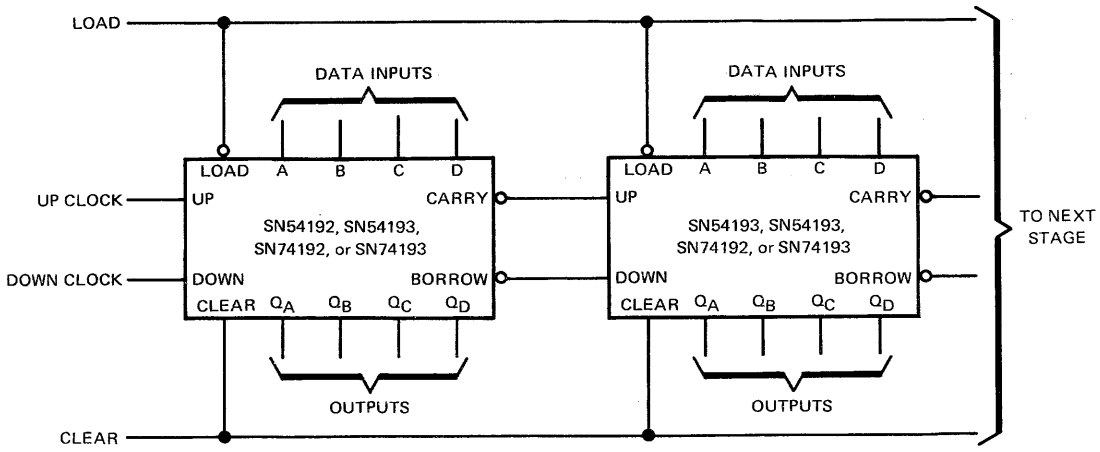
The SN54193/SN74193 can be used to divide an incoming count frequency by any integral number (N) from one to 16. This is done by modifying the count frequency occurring at the carry output by presetting the data inputs to 16 minus N. By connecting the carry output to the load input, the counter will count to the maximum state (15) and the data inputs will then be enabled on the succeeding clock pulse. The counter outputs are then preset to the levels applied at the data inputs and the count sequence is repeated.



The SN54192/SN74192 may be used in the same manner to perform division by any number from 1 to 10.

cascading

Circuitry is provided internally for cascading these counters. The mode of cascading shown below is ripple borrow/carry. No external components are required.



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

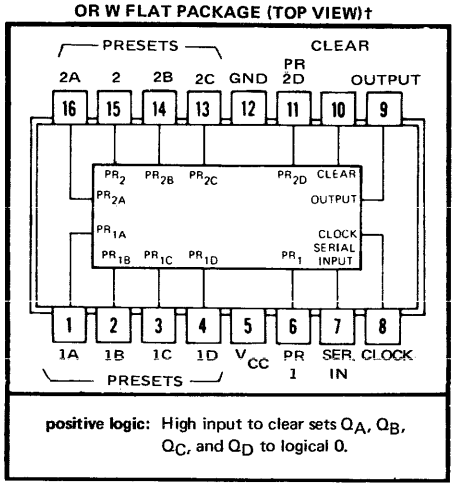
CIRCUIT TYPES SN5494, SN7494
4-BIT SHIFT REGISTERS

TTL MSI PARALLEL-IN SERIAL-OUT REGISTERS

for application as

- Dual-Source, Parallel-To-Serial Converter
- Serial-In Serial-Out Register

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: High input to clear sets Q_A, Q_B, Q_C, and Q_D to logical 0.

†Pin assignments for these circuits are the same for all packages.

description

This monolithic shift register, utilizing transistor-transistor logic (TTL) circuits in the familiar Series 74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

All flip-flops are simultaneously set to the logical 0 state by applying a logical 1 voltage to the clear input. This condition may be applied independent of the state of the clock input, but not independent of state of the preset input. Preset input is independent of the clock and clear states.

The flip-flops are simultaneously set to the logical 1 state from either of two preset input sources. Preset inputs 1A through 1D are activated during the time that a positive pulse is applied to preset 1 if preset 2 is at a logical 0 level. When the logic levels at preset 1 and preset 2 are reversed, preset inputs 2A through 2D are active.

Transfer of information to the outputs occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop. The outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input, preset 1, and preset 2 must be at a logical 0 when clocking occurs.

This register is completely compatible for use with TTL and DTL logic circuits and when used with other TTL circuits, noise margins are typically one volt. Typical average power dissipation is 175 milliwatts, and propagation delay times from clock to output are typically 25 nanoseconds.

9

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)		7 V
Input Voltage V_{in} (See Notes 1 and 2)		5.5 V
Operating Free-Air Temperature Range:	SN5494 Circuits	−55°C to 125°C
	SN7494 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTES: 1. The voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	SN5494 Circuits	4.5	5	5.5	V
	SN7494 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Output				10	
Width of Clock Pulse, $t_{p(clock)}$		35			ns
Width of Clear Pulse, $t_{p(clear)}$		30			ns
Width of Preset Pulse, $t_{p(preset)}$		30			ns
Serial Input Setup Time: $t_{setup(1)}$		35			ns
$t_{setup(0)}$		25			ns
Serial Input Hold Time, t_{hold}		0			

NOTE: 1. These voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(1)}$	Logical 1 level input current at any input except preset 1 and preset 2	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset 1 and preset 2	V_{CC} = MAX, V_{in} = 2.4 V				160	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at any input except preset 1 and preset 2	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset 1 and preset 2	V_{CC} = MAX, V_{in} = 0.4 V				−6.4	mA
I_{OS}	Short-circuit input current§	V_{CC} = MAX, V_{out} = 0	SN5494	−20		−57	mA
			SN7494	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX	SN5494		35	50	mA
			SN7494		35	58	mA

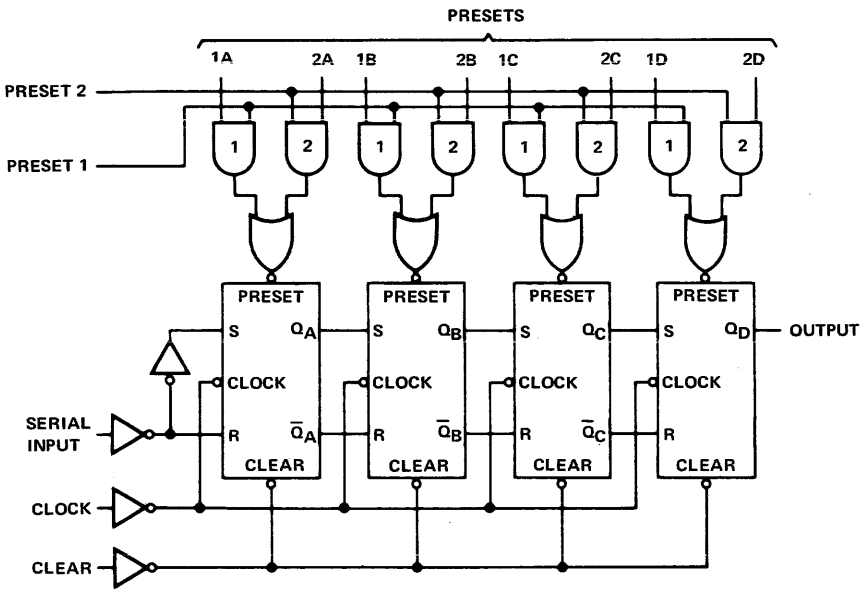
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

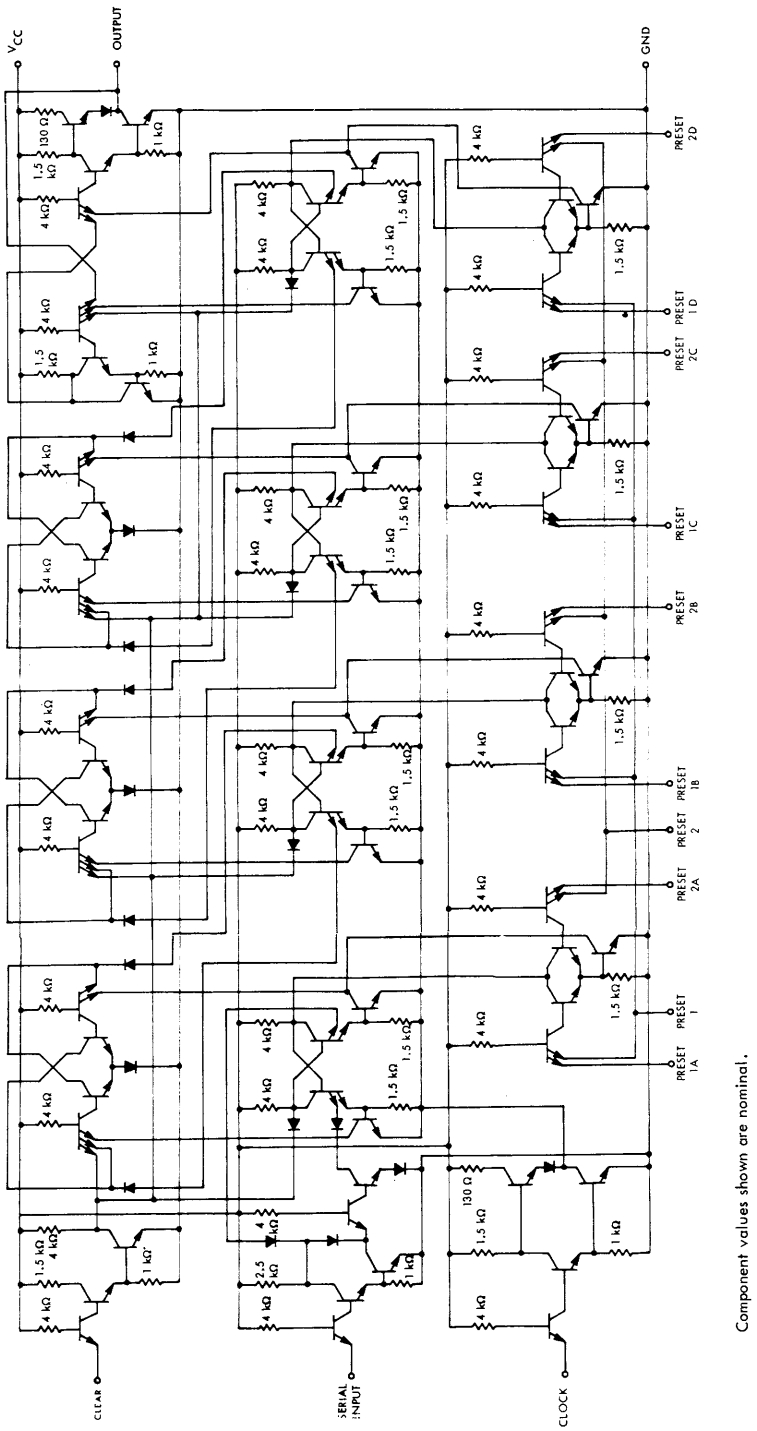
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω	10			MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15 pF, R_L = 400 Ω			40	ns

9

functional block diagram



schematic



Component values shown are nominal.

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5495A, SN7495A
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS

A TTL MSI PARALLEL-IN PARALLEL-OUT REGISTER

for application as

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

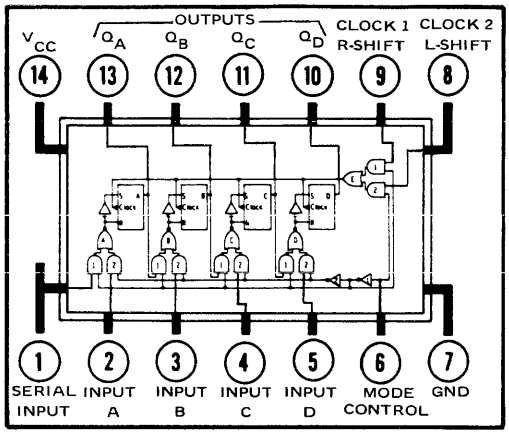
description

This monolithic shift register, utilizing transistor-transistor-logic (TTL) circuits in the familiar Series 54/74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, one AND-OR gate, and six inverters-drivers. Internal interconnections of these functions provide a versatile register which will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an n-bit right-shift or left-shift register. This register can also be used as a parallel-in, parallel-out storage register with gate (mode) control.

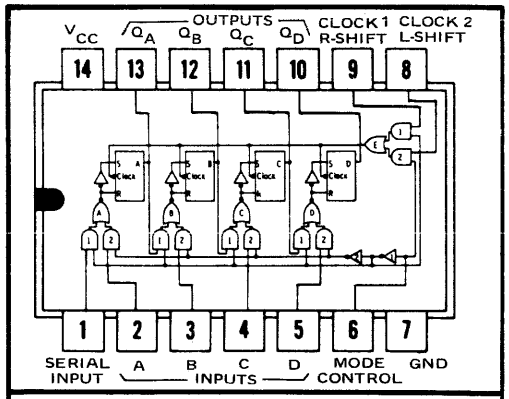
When a logical 0 level is applied to the mode control input, the number-1 AND gates are enabled and the number-2 AND gates are inhibited. In this mode the output of each flip-flop is coupled to the R-S inputs of the succeeding flip-flop and right-shift operation is performed by clocking at the clock 1 input. In this mode, serial data is entered at the serial input. Clock 2 and parallel inputs A through D are inhibited by the number-2 AND gates.

When a logical 1 level is applied to the mode control input, the number-1 AND gates are inhibited (decoupling the outputs from the succeeding R-S inputs to prevent right-shift) and the number-2 AND gates are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register, or with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, and etc.), and serial data is entered at input D.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

Mode control = 0 for right shift
Mode control = 1 for left shift or parallel load

Clocking for the shift register is accomplished through the AND-OR gate E which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and clock 2. Information must be present at the R-S inputs of the master-slave flip-flops prior to clocking. Transfer of information to the output pins occurs when the clock input goes from a logical 1 to a logical 0.

This shift register is completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is typically 195 milliwatts. The SN5495A and SN7495A are unilaterally interchangeable with and replace SN5495 and SN7495, respectively, but offer diode-clamped inputs, improved speed, and reduced power dissipation.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5495A Circuits . . . . . −55°C to 125°C
SN7495A Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5495A Circuits	4.5	5	5.5	V
SN7495A Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output: High logic level			20	
Low logic level			10	
Width of Clock Pulse $t_{p(clock)}$ (See Figure 9): SN5495A Circuits	20	10		ns
SN7495A Circuits	15	10		ns
Setup Time Required at Serial, A, B, C, or D Inputs t_{setup} (See Figure 9)	10			ns
Hold Time Required at Serial, A, B, C, or D Inputs t_{hold} (See Figure 9)	0			ns
Logical 0 Level Setup Time Required at Mode Control (t1 in Figure 10) (With Respect to Clock 1 input)	15			ns
Logical 1 Level Setup Time Required at Mode Control (t2 in Figure 10) (With Respect to Clock 2 input)	15			ns
Logical 0 Level Setup Time Required at Mode Control (t3 in Figure 10) (With Respect to Clock 2 input)	5			ns
Logical 1 Level Setup Time Required at Mode Control (t4 in Figure 10) (With Respect to Clock 1 input)	5			ns

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

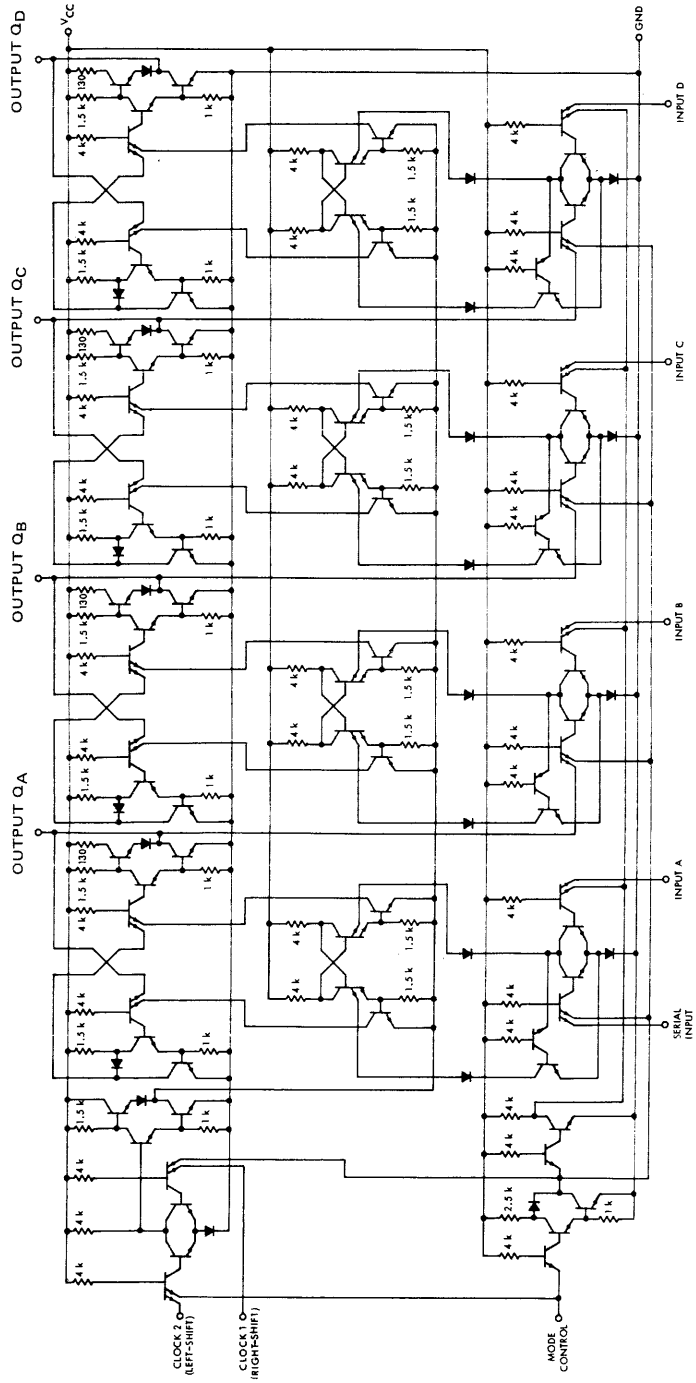
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 3		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2 and 4				0.8	V
$V_{out(1)}$	Logical 1 output voltage	1 and 3	V_{CC} = MIN, I_{load} = −800 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	2 and 4	V_{CC} = MIN, I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at any input except mode control	5	V_{CC} = MAX, V_{in} = 0.4 V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at mode control	5	V_{CC} = MAX, V_{in} = 0.4 V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except mode control	6	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at mode control	6	V_{CC} = MAX, V_{in} = 2.4 V			80	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current§	7	V_{CC} = MAX	−18		−57	mA
I_{CC}	Supply current	8	V_{CC} = MAX	39		63	mA

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency	9	C_L = 15 pF, R_L = 400 Ω	25	36		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock 1 or clock 2 to outputs	9	C_L = 15 pF, R_L = 400 Ω		18	27	ns
t_{pd0}	Propagation delay time to logical 0 level from clock 1 or clock 2 to outputs	9	C_L = 15 pF, R_L = 400 Ω		21	32	ns

schematic



NOTES: 1. Resistor values are in ohms.
2. Component values shown are nominal.

d-c test circuits†

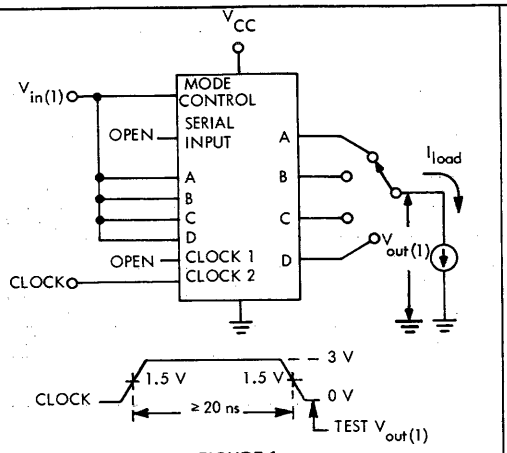


FIGURE 1

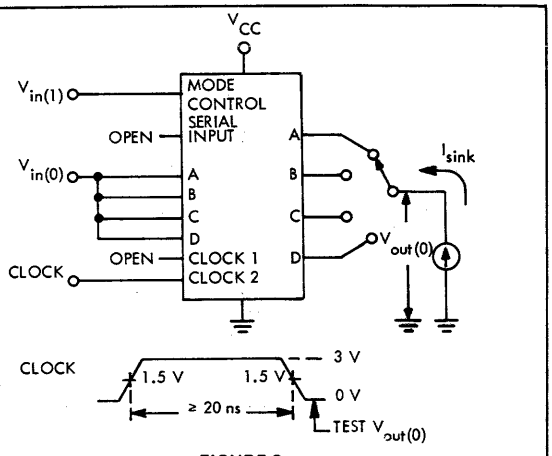


FIGURE 2

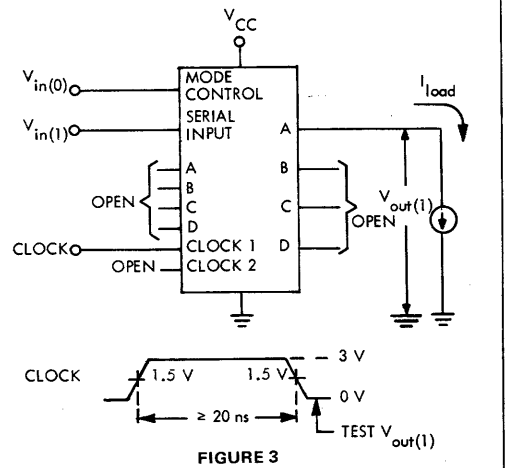


FIGURE 3

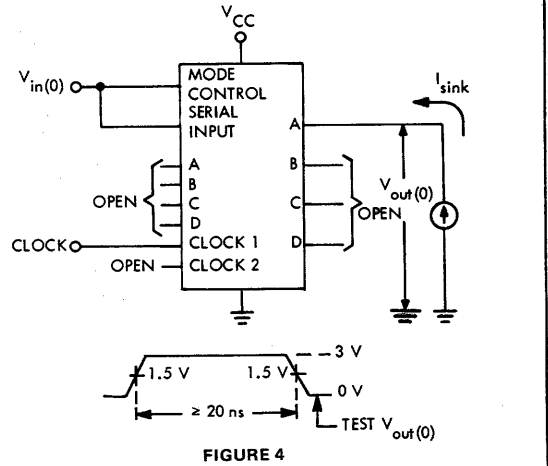
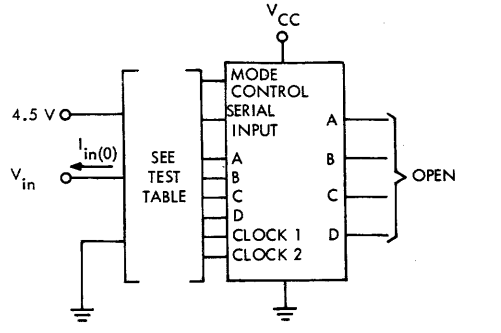


FIGURE 4



1. Each input is tested separately.

TEST TABLE

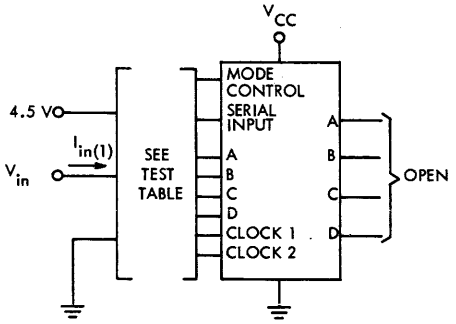
TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	CLOCK 2	NONE
SERIAL INPUT	NONE	MODE CONTROL
INPUT A	MODE CONTROL	NONE
INPUT B	MODE CONTROL	NONE
INPUT C	MODE CONTROL	NONE
INPUT D	MODE CONTROL	NONE
CLOCK 1	NONE	MODE CONTROL
CLOCK 2	MODE CONTROL	NONE

FIGURE 5

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

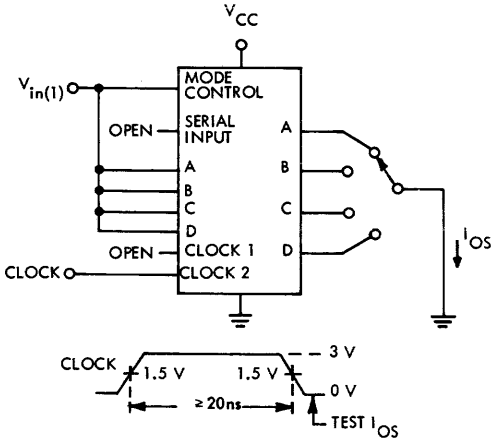
d-c test circuits† (continued)



TEST TABLE

TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	NONE	CLOCK 2
SERIAL INPUT	MODE CONTROL	NONE
INPUT A	NONE	MODE CONTROL
INPUT B	NONE	MODE CONTROL
INPUT C	NONE	MODE CONTROL
INPUT D	NONE	MODE CONTROL
CLOCK 1	MODE CONTROL	NONE
CLOCK 2	NONE	MODE CONTROL

FIGURE 6



1. Each output is tested separately.

FIGURE 7

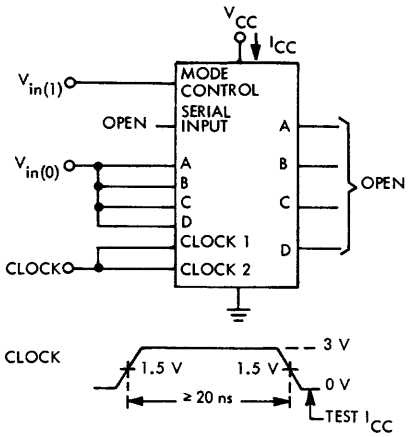
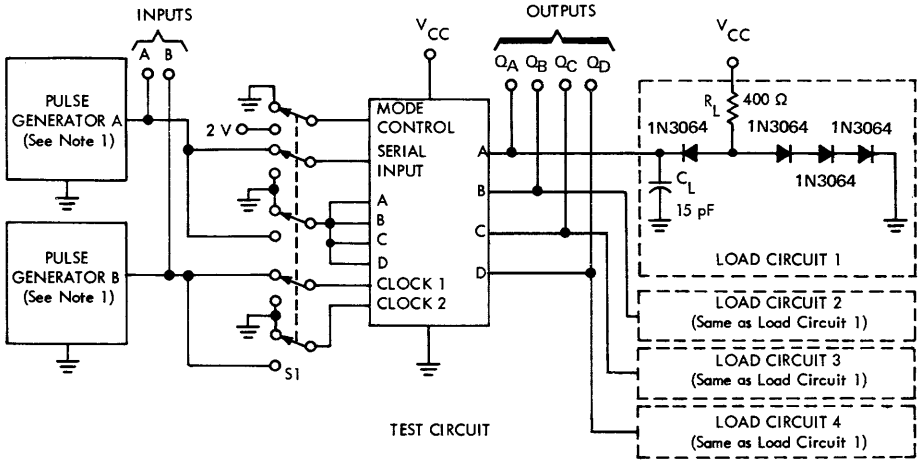


FIGURE 8

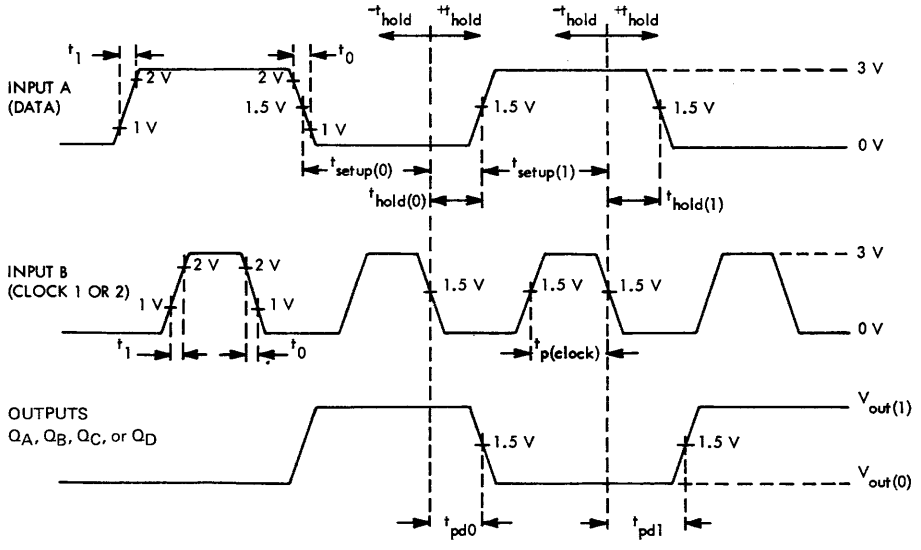
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching charateristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leq$ 10 ns, and $Z_{out} \approx 50\ \Omega$. For pulse generator A : $t_p \geq$ 20 ns and PRR = 500 kHz. For pulse generator B : $t_p \geq$ 15 ns and PRR = 1 MHz. When testing f_{max} vary PRR.

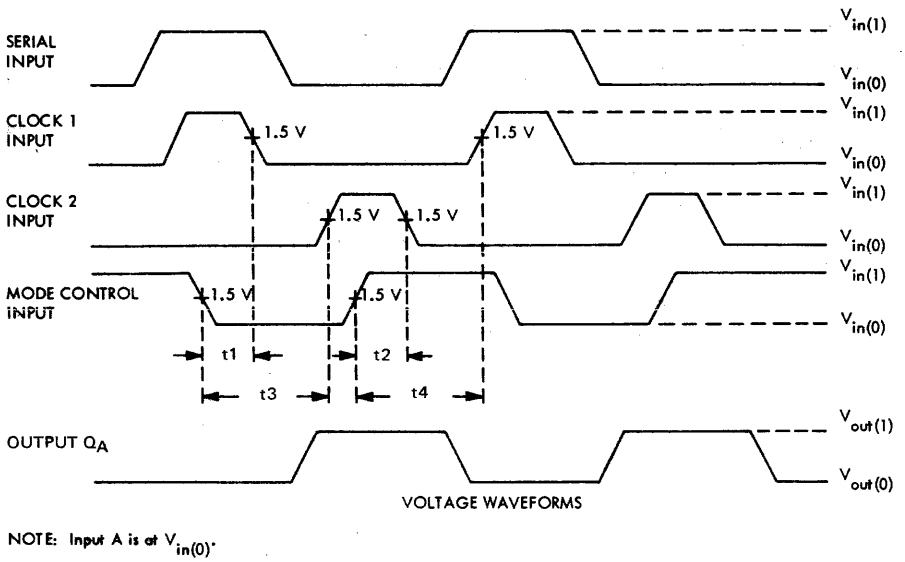
2. Voltage values are with respect to network ground terminal.
3. C_L includes probe and jig capacitance.

FIGURE 9–SWITCHING TIMES

9

PARAMETER MEASUREMENT INFORMATION

recommended mode control setup times



NOTE: Input A is at $V_{in(0)}$.

FIGURE 10–MODE CONTROL SETUP TIMES

9

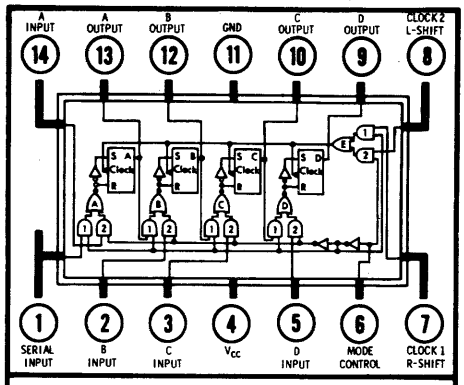
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54L95, SN74L95
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS

A SERIES 54L/74L PARALLEL-IN PARALLEL-OUT REGISTER
for application as

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

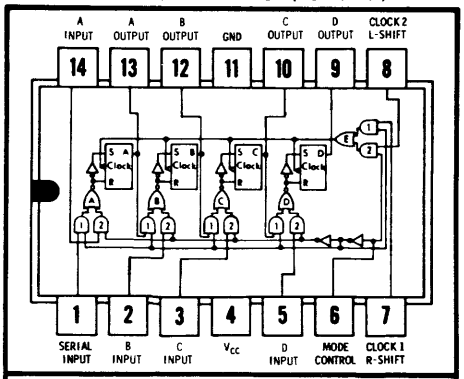
T
FLAT PACKAGE (TOP VIEW)



positive logic

Mode Control = 0 for right shift
Mode Control = 1 for left shift or parallel load

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

Mode Control = 0 for right shift
Mode Control = 1 for left shift or parallel load

description

This monolithic shift register, utilizing transistor-transistor logic (TTL) circuits in the familiar Series 54L/74L configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, one AND-OR gate, and six inverter-drivers. Internal interconnections of these functions provide a versatile register which will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an n-bit right-shift or left-shift register. This register can also be used as a parallel-in, parallel-out storage register with gate (mode) control.

When a logical 0 level is applied to the mode control input, the number 1 AND gates are enabled and the number 2 AND gates are inhibited. In this mode the output of each flip-flip is coupled to the R-S inputs of the succeeding flip-flop, right-shift operation is performed by clocking at the clock 1 input, and serial data is entered at the serial input. Clock 2 and parallel inputs A through D are inhibited by the number 2 AND gates.

When a logical 1 level is applied to the mode-control input, the number 1 AND gates are inhibited (decoupling the outputs from the succeeding R-S inputs to prevent right-shift) and the number 2 AND gates are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register or, with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop (D output to input C, and etc.), and serial data is entered at input D.

Clocking for the shift register is accomplished through the AND-OR gate E which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and clock 2. Information must be present at the R-S inputs of the master-slave flip-flops prior to clocking.

The shift register is completely compatible for use with TTL and DTL logic families. Average power dissipation is typically 19 milliwatts.

9

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 8 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN54L95 Circuits . . . . . -55°C to 125°C
SN74L95 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . -65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN54L95 Circuits	4.5	5	5.5	V
SN74L95 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 9)	200			ns
Logical 1 Setup Time Required at Serial, A, B, C, or D Inputs, $t_{setup(1)}$ (See Figure 9)	100			ns
Logical 0 Setup Time Required at Serial, A, B, C, or D Inputs, $t_{setup(0)}$	120			ns
Hold Time Required at Serial, A, B, C, or D Inputs, t_{hold} (See Figure 9)	0			ns
Logical 0 Level Setup Time Required at Mode Control (t1 in Figure 10) (With Respect to Clock 1 Input)	225			ns
Logical 1 Level Setup Time Required at Mode Control (t2 in Figure 10) (With Respect to Clock 2 Input)	200			ns
Logical 0 Level Setup Time Required at Mode Control (t3 in Figure 10) (With Respect to Clock 2 Input)	0			ns
Logical 1 Level Setup Time Required at Mode Control (t4 in Figure 10) (With Respect to Clock 1 Input)	100			ns

NOTE: 1. Voltage values are with respect to network ground terminal.

electrical characteristics (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS †	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 3		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2 and 4				0.7	V
$V_{out(1)}$	Logical 1 output voltage	1 and 3	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.7 V, I_{load} = −100 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	2 and 4	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.7 V, I_{sink} = 2 mA		0.16	0.3	V
$I_{in(0)}$	Logical 0 level input current at any input except mode control	5	V_{CC} = MAX, V_{in} = 0.3 V			-0.18	mA
$I_{in(0)}$	Logical 0 level input current at mode control	5	V_{CC} = MAX, V_{in} = 0.3 V			-0.36	mA
$I_{in(1)}$	Logical 1 level input current at any input except mode control	6	V_{CC} = MAX, V_{in} = 2.4 V			10	μA
			V_{CC} = MAX, V_{in} = 5.5 V			100	μA
$I_{in(1)}$	Logical 1 level input current at mode control	6	V_{CC} = MAX, V_{in} = 2.4 V			20	μA
			V_{CC} = MAX, V_{in} = 5.5 V			200	μA
I_{OS}	Short-circuit output current §	7	V_{CC} = MAX, V_{in} = 4.5 V	-3		-15	mA
I_{CC}	Supply current	8	V_{CC} = MAX, $V_{in(1)}$ = 4.5 V, $V_{in(0)}$ = 0		3.8	9	mA

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions for the applicable device type.

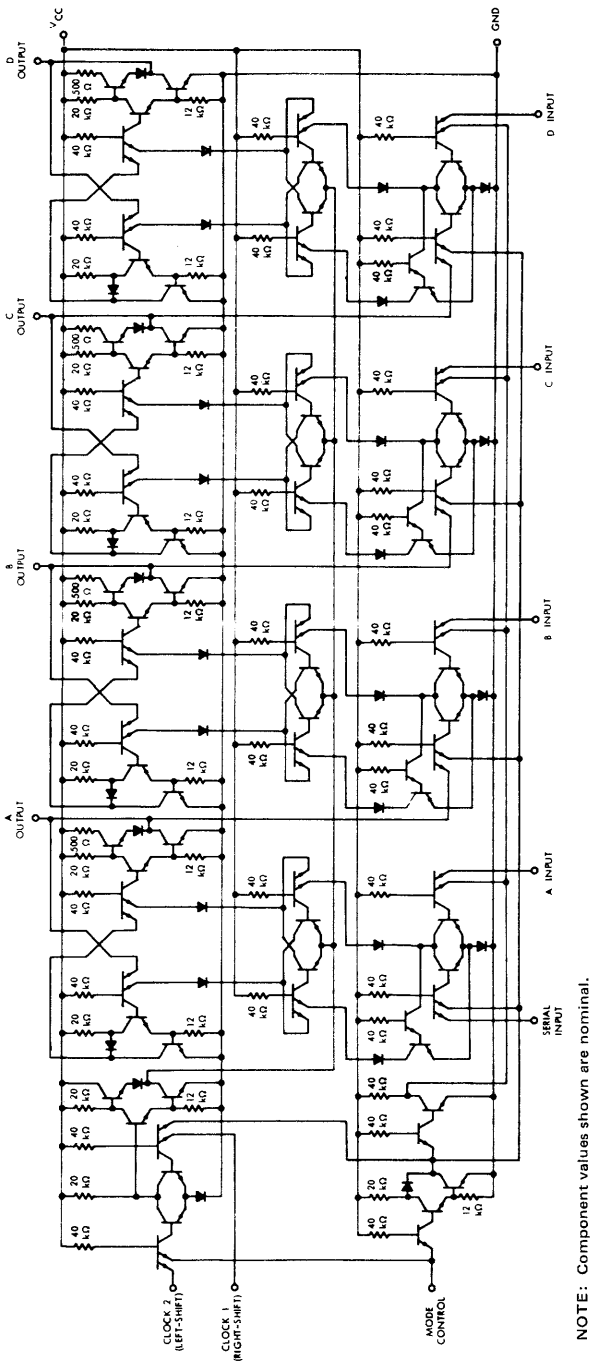
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency	9	C_L = 50 pF, R_L = 4 kΩ	3	5		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock 1 or clock 2 to outputs	9	C_L = 50 pF, R_L = 4 kΩ		115	200	ns
t_{pd0}	Propagation delay time to logical 0 level from clock 1 or clock 2 to outputs	9	C_L = 50 pF, R_L = 4 kΩ		125	200	ns

schematic

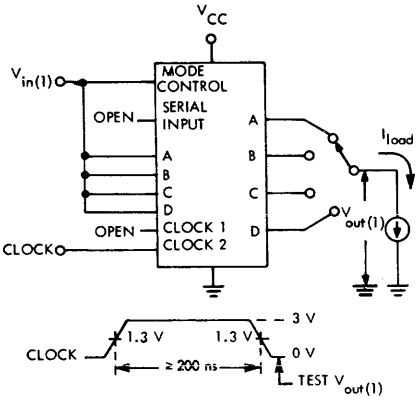


NOTE: Component values shown are nominal.

9

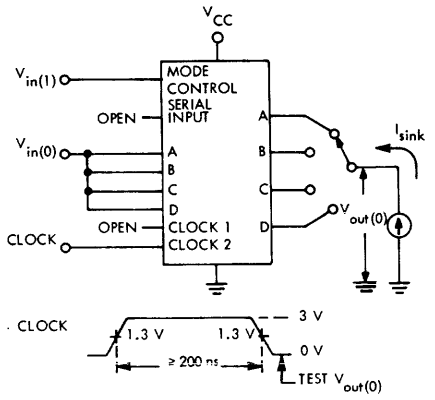
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



1. Each output is tested separately.

FIGURE 1



1. Each output is tested separately.

FIGURE 2

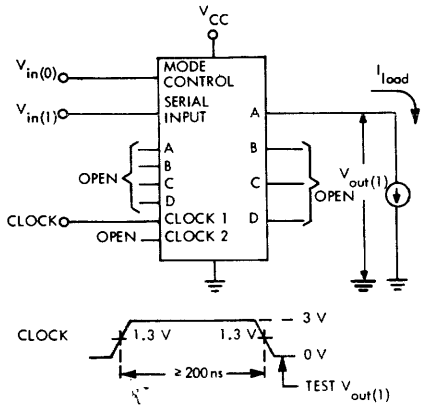


FIGURE 3

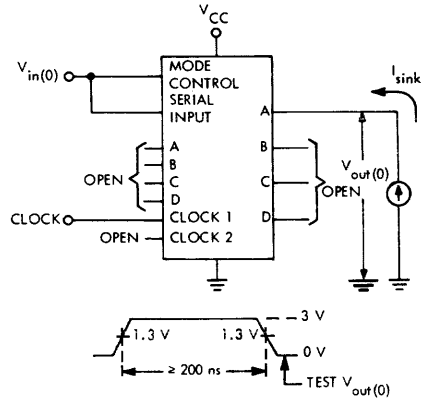
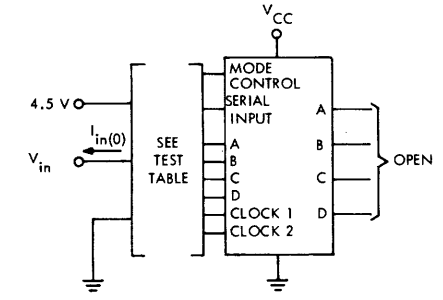


FIGURE 4



TEST TABLE

TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	CLOCK 2	NONE
SERIAL INPUT	NONE	MODE CONTROL
A INPUT	MODE CONTROL	NONE
B INPUT	MODE CONTROL	NONE
C INPUT	MODE CONTROL	NONE
D INPUT	MODE CONTROL	NONE
CLOCK 1	NONE	MODE CONTROL
CLOCK 2	MODE CONTROL	NONE

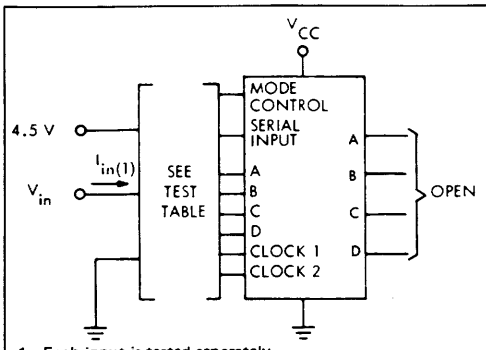
1. Each input is tested separately.

FIGURE 5

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

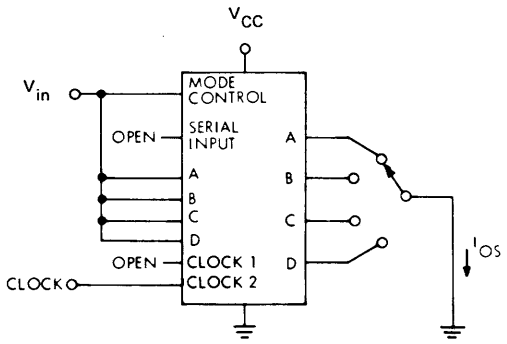


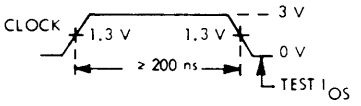
TEST TABLE

TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	NONE	CLOCK 2
SERIAL INPUT	MODE CONTROL	NONE
A INPUT	NONE	MODE CONTROL
B INPUT	NONE	MODE CONTROL
C INPUT	NONE	MODE CONTROL
D INPUT	NONE	MODE CONTROL
CLOCK 1	MODE CONTROL	NONE
CLOCK 2	NONE	MODE CONTROL

1. Each input is tested separately.

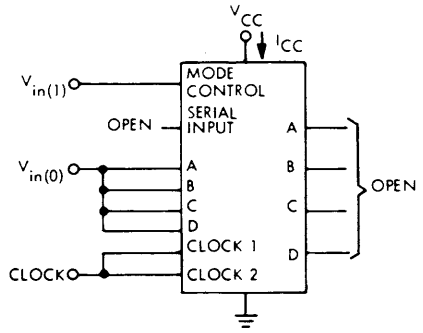
FIGURE 6





1. Each output is tested separately.

FIGURE 7



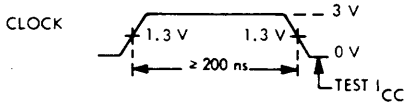


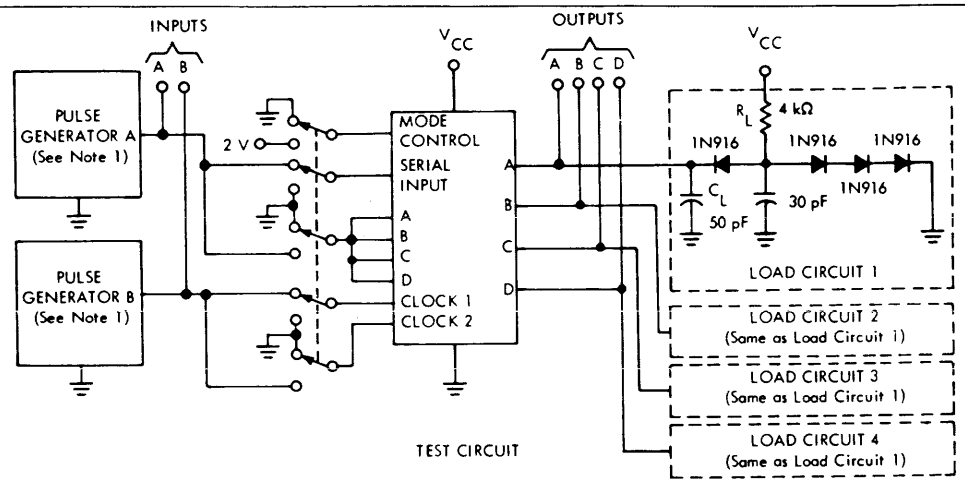
FIGURE 8

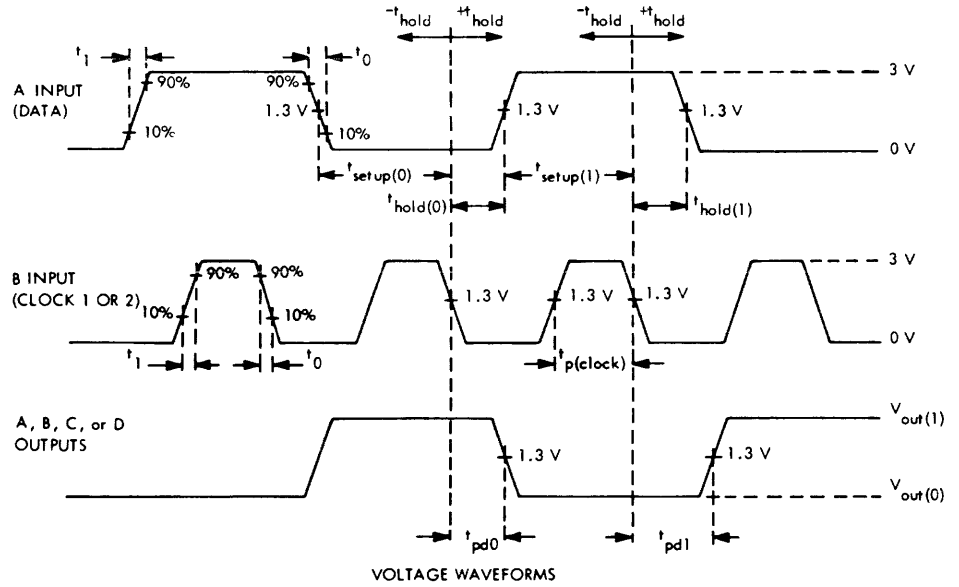
† Arrows indicate actual direction of current flow.

9

PARAMETER MEASUREMENT INFORMATION

switching characteristics





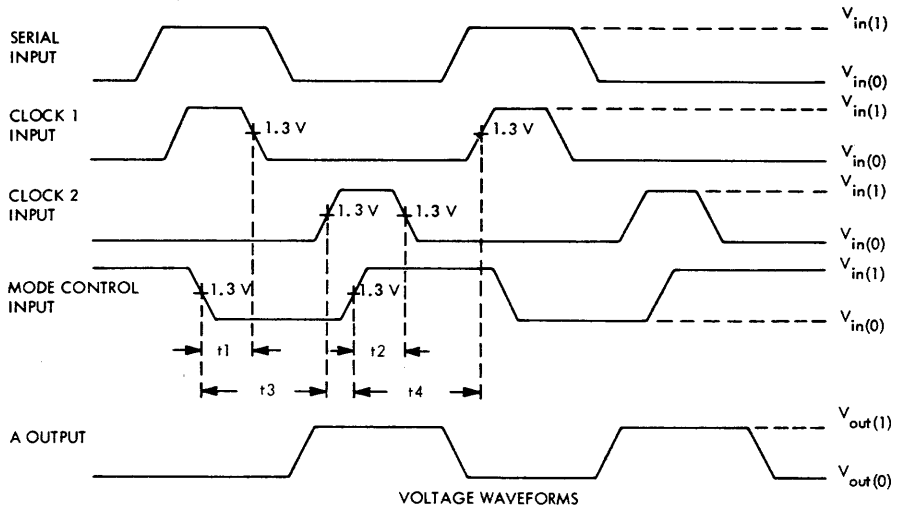
NOTES: 1. The pulse generators have the following characteristics: t_1 = 10 ns to 12 ns, t_0 = 10 ns to 12 ns, and $Z_{out} \approx 50\ \Omega$.
For pulse generator A : $t_p \geq 150$ ns and PRR $\leq$ 500 kHz. For pulse generator B : $t_p \geq 10$ ns and PRR $\leq$ 1 MHz.
When testing f_{max}, vary PRR.
2. Voltage values are with respect to network ground terminal.
3. C_L includes probe and jig capacitance.

FIGURE 9 – SWITCHING TIMES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

recommended mode control setup times



NOTE: A Input is at $V_{in(0)}$.

FIGURE 10–MODE CONTROL SETUP TIMES

9

CIRCUIT TYPES SN5496, SN7496
5-BIT SHIFT REGISTERS

TTL MSI MULTIFUNCTION SHIFT REGISTERS

for application as

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

description

This shift register consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

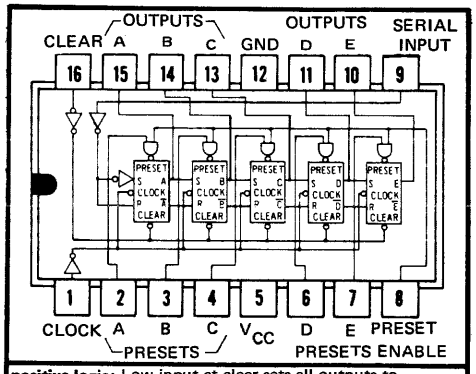
All flip-flops are simultaneously set to the logical 0 state by applying a logical 0 voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flops may be independently set to the logical 1 state by applying a logical 1 to both the preset input of the specific flip-flop and the common preset input. The preset-enable input is provided to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is also independent of the state of the clock input or clear input.

Transfer of information to the output pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a logical 1 and the preset input must be at a logical 0 when clocking occurs.

This shift register is completely compatible with Series 54/74 TTL and DTL logic families. Typically, average power dissipation is 240 milliwatts, and propagation delay time is 25 nanoseconds.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input at clear sets all outputs to logical 0.

9

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)		7 V
Input Voltage, V_{in} (See Notes 1 and 2)		5.5 V
Operating Free-Air Temperature Range:	SN5496 Circuits	−55°C to 125°C
	SN7496 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5496 Circuits	4.5	5	5.5	V
SN7496 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output			10	
Width of Clock Pulse, $t_{p(clock)}$	35			ns
Width of Clear Pulse, $t_{p(clear)}$	30			ns
Width of Preset Pulse, $t_{p(preset)}$	30			ns
Serial Input Setup Time, t_{setup}	30			ns
Serial Input Hold Time, t_{hold}	0			ns

NOTE 1: This voltage value is with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage			2			V
$V_{in(0)}$	Logical 0 input voltage					0.8	
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(1)}$	Logical 1 level input current at any input except preset-enable	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset-enable	V_{CC} = MAX, V_{in} = 2.4 V				200	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at any input except preset-enable	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset-enable	V_{CC} = MAX, V_{in} = 0.4 V				−8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_{out} = 0	SN5496	−20		−57	mA
			SN7496	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX	SN5496		48	68	mA
			SN7496		48	79	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

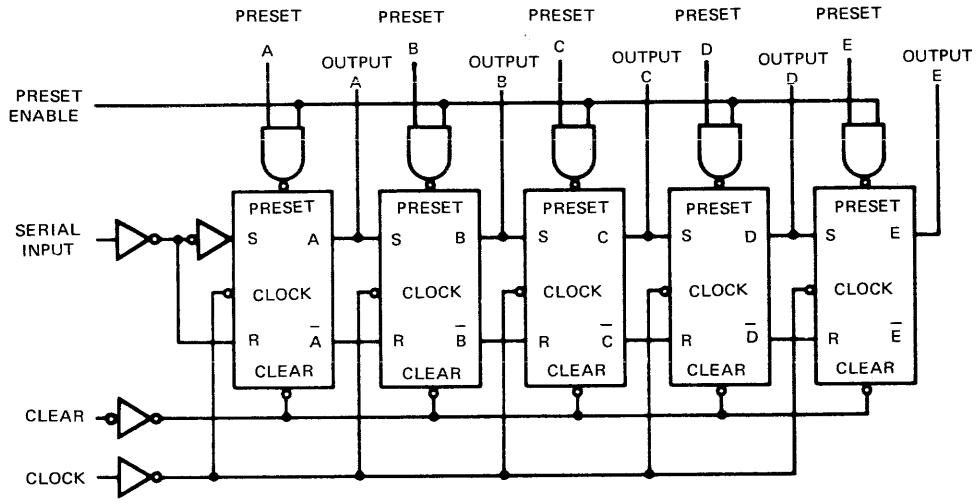
§ Not more than one output should be shorted at a time.

9

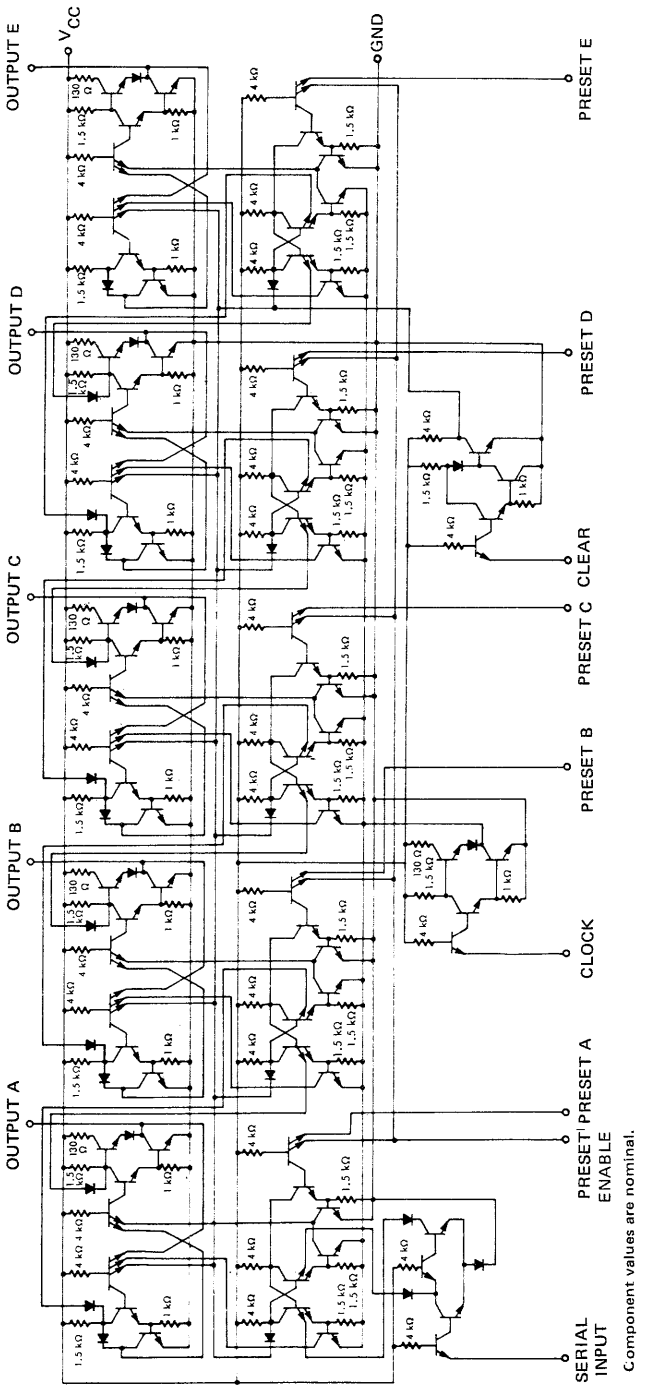
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω	10			MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from preset or preset-enable to output	C_L = 15 pF, R_L = 400 Ω		28	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15 pF, R_L = 400 Ω			55	ns

functional block diagram



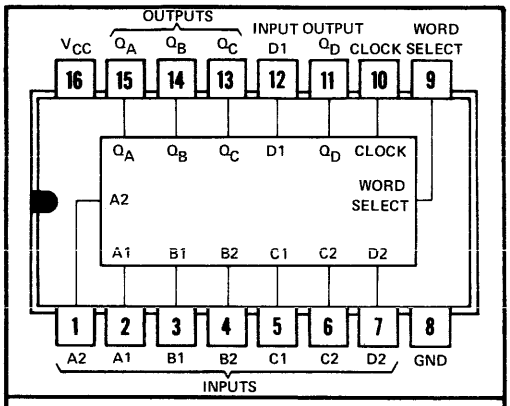
schematic



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54L98, SN74L98
4-BIT DATA SELECTORS/STORAGE REGISTERS

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: See description

description

These monolithic data selectors/storage registers are composed of four S-R master-slave flip-flops, four AND-OR-INVERT gates, one buffer, and six inverter/drivers.

When the word select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is shifted to the output terminals on the negative-going edge of the clock pulse.

Typical power dissipation is 25 mW. The SN54L98 is characterized for operation over the full military temperature range of –55°C to 125°C; the SN74L98 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 8 V
Input voltage (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range: SN54L98 Circuits . . . . . –55°C to 125°C
SN74L98 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

9

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

		SN54L98			SN74L98			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N				10			10	
Width of clock pulse, $t_{w(clock)}$ (see Figure 6)		200			200			ns
Setup time for high-level data, $t_{setup(H)}$ (see Note 3 and Figure 6)	at A, B, C, or D	100			100			ns
	at word select	150			150			
Setup time for low-level data, $t_{setup(L)}$ (see Note 3 and Figure 6)	at A, B, C, or D	120			120			ns
	at word select	100			100			
Operating free-air temperature range, T_A		–55	25	125	0	25	70	°C

NOTE 3: Setup time is the interval immediately preceding the negative-going edge of the clock pulse, during which interval the data to be recognized must be maintained at the input to ensure its recognition.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2		2		V
V_{IL}	Low-level input voltage	1 and 2			0.7	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, I_{OL} = 2 mA		0.3	V
I_{IH}	High-level input current into any input except word select	3	V_{CC} = MAX, V_I = 2.4 V		10	μA
			V_{CC} = MAX, V_I = 5.5 V		100	
I_{IH}	High-level input current into word select	3	V_{CC} = MAX, V_I = 2.4 V		20	μA
			V_{CC} = MAX, V_I = 5.5 V		200	
I_{IL}	Low-level input current into any input except word select	3	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{IL}	Low-level input current into word select	3	V_{CC} = MAX, V_I = 0.3 V		−0.36	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX	−3	−15	mA
I_{CC}	Supply current	5	V_{CC} = MAX		9	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

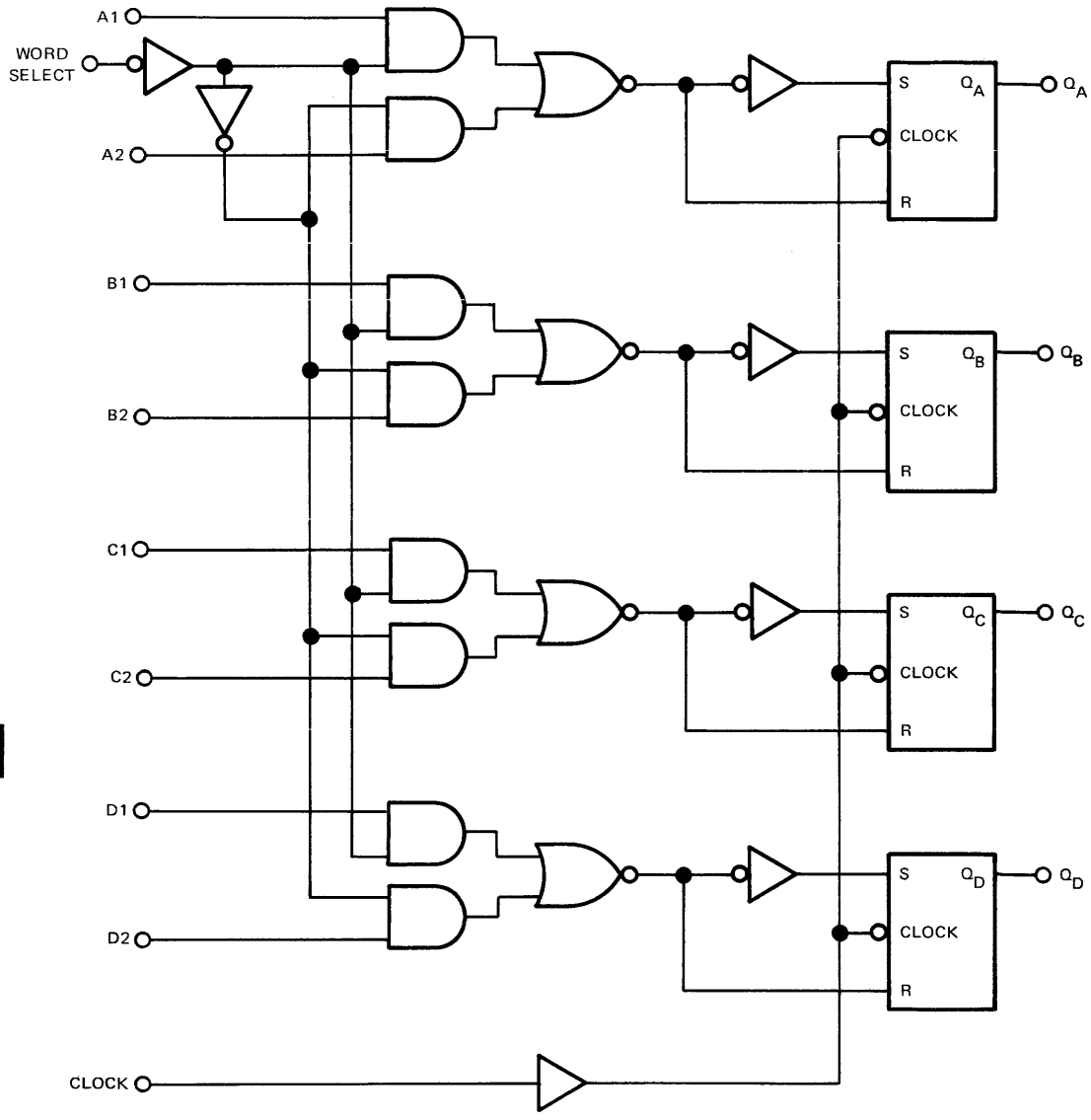
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	6	C_L = 50 pF, R_L = 4 kΩ	3	5		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clock input				115	200	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock input				125	200	ns

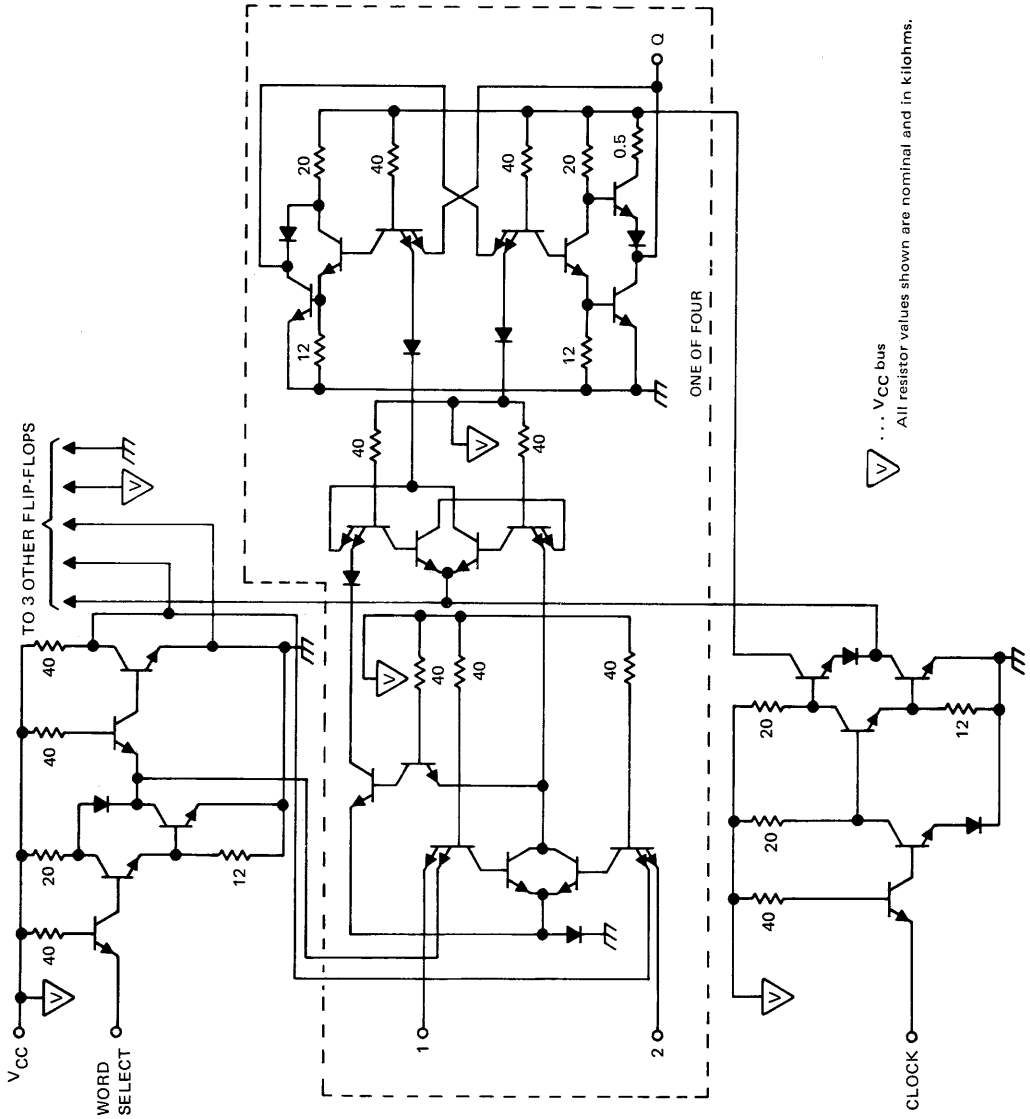
9

functional block diagram



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

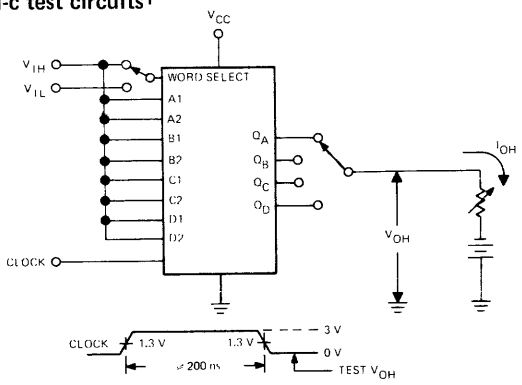
schematic


Q
ONE OF FOUR
TO 3 OTHER FLIP-FLOPS
V_{CC}
WORD SELECT
1
2
CLOCK
. . . V_{CC} bus
All resistor values shown are nominal and in kilohms.

9

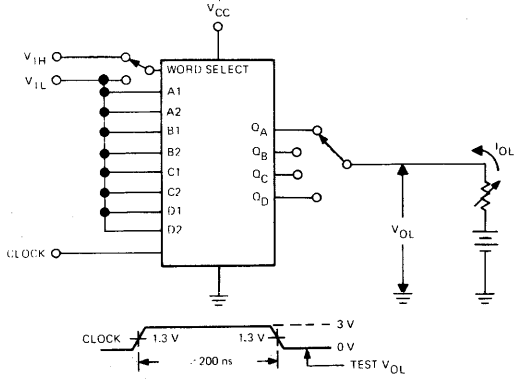
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



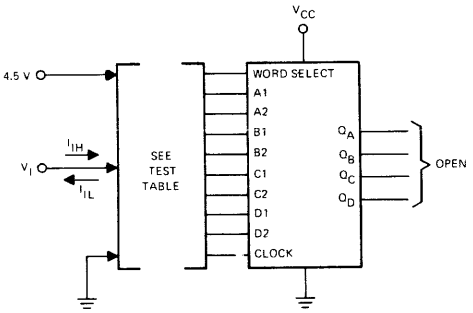
Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



Each output is tested separately.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}

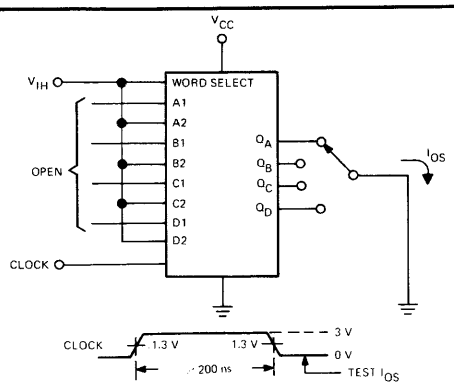


TEST TABLE

APPLY V_I	TEST I_{IH}		TEST I_{IL}	
	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND
A1, B1, C1, D1	WORD SELECT	NONE	NONE	WORD SELECT
A2, B2, C2, D2	NONE	WORD SELECT	WORD SELECT	NONE
WORD SELECT	NONE	NONE	NONE	NONE
CLOCK	NONE	NONE	NONE	NONE

FIGURE 3–I_{IH}, I_{IL}

9



Each output is tested separately.

FIGURE 4–I_{OS}

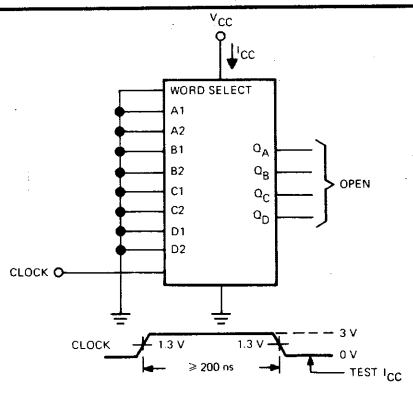


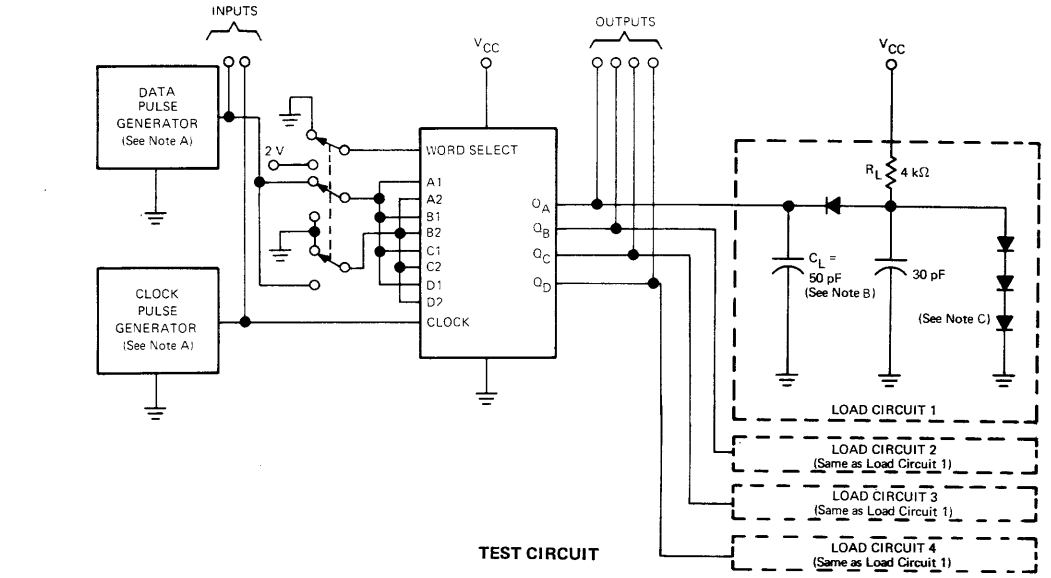
FIGURE 5–I_{CC}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

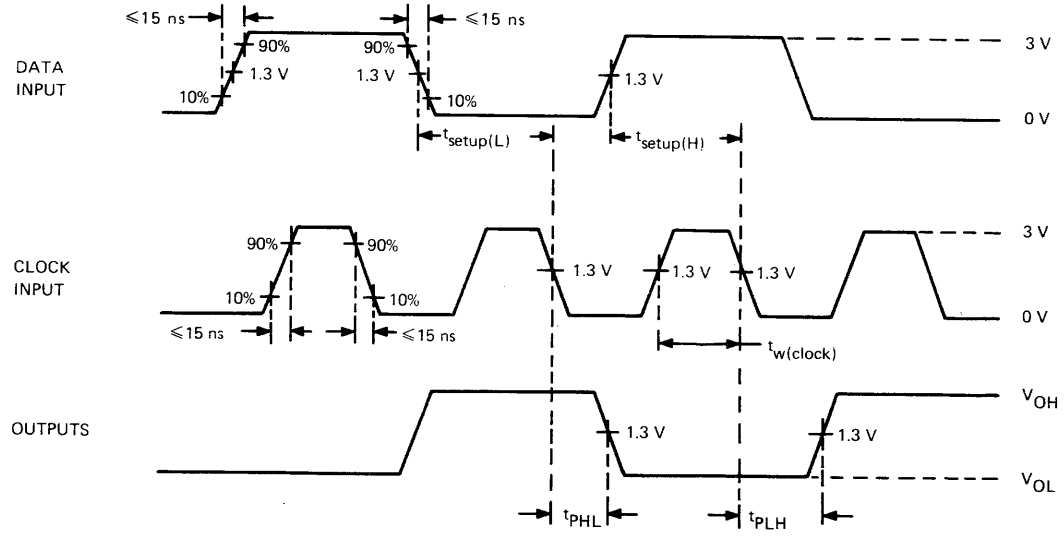
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$. For data pulse generator: $t_w \geq 150$ ns, PRR ≤ 500 kHz, $t_{setup(L)} = 120$ ns, and $t_{setup(H)} = 100$ ns. For clock pulse generator: $t_w \geq 200$ ns and PRR ≤ 1 MHz. When testing f_{max}, vary PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N916.

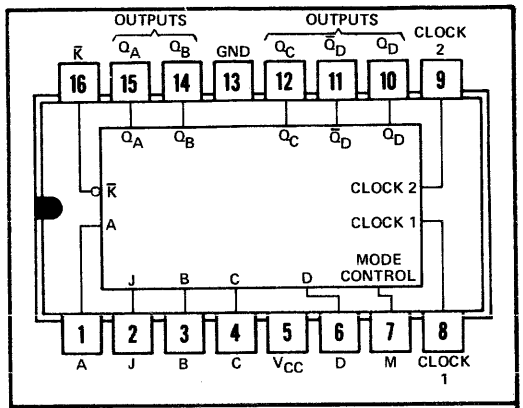
FIGURE 6–SWITCHING TIMES

9

CIRCUIT TYPES SN54L99, SN74L99
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS

- N-Bit Serial-to-Parallel Converter
- N-Bit Parallel-to-Serial Converter
- N-Bit Storage Register
- J-$\overline{K}$ Serial Input

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic:
Mode control low for right-shift or serial loading
Mode control high for left-shift or parallel loading

description

This monolithic integrated circuit, utilizing transistor-transistor logic (TTL) in the familiar Series 54L/74L configuration, is composed of four master-slave flip-flops and the necessary gating to provide a versatile shift register or parallel-in, parallel-out storage register. The circuit has J and $\overline{K}$ inputs externally available. This permits the first stage to act as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the following table. For additional examples, see the function tables on the last page of this data sheet.

Inputs at t_n			Outputs at t_{n+1}				
M	J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level, L = low level
NOTES: A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse
C. Q_{An} = state of Q_A at t_n

When a low-level input is applied to the mode control, the number 1 AND gates (see functional block diagram) are enabled and the number 2 AND gates are inhibited. In this mode, the output of each flip-flop is coupled to the S-R inputs of the succeeding flip-flop and right-shift operation is performed by clocking at the clock 1 input. Serial data is entered at the J-$\overline{K}$ inputs. Clock 2 and parallel inputs A through D are inhibited by the number 2 AND gates.

When a high-level input is applied to the mode control, the number 1 AND gates are inhibited (decoupling the outputs from the succeeding S-R inputs to prevent right-shift) and the number 2 AND gates are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register or, with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, and etc.), and serial data is entered at input D.

Clocking for the shift register is accomplished through an AND-OR gate which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and 2. An inverted output is available from the last flip-flop.

This shift register is compatible for use with most TTL and DTL logic families. A number of these registers may be connected in series to form an n-bit right-shift or left-shift register. Average power dissipation is typically 19 mW.

9

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 8 V
Input voltage (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range: SN54L99 Circuits . . . . . −55°C to 125°C
SN74L99 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

	SN54L99			SN74L99			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Fan-out from each output, N			10			10	
Width of clock pulse, $t_{w(clock)}$ (see Figure 10)	200			200			ns
Setup time for high-level data at J, $\overline{K}$, A, B, C, or D inputs, $t_{setup(H)}$ (see Note 3 and Figure 10)	100			100			ns
Setup time for low-level data at J, $\overline{K}$, A, B, C, or D inputs, $t_{setup(L)}$ (see Note 3 and Figure 10)	120			120			ns
Hold time required at J, $\overline{K}$, A, B, C, or D inputs, t_{hold} (see Note 4 and Figure 10)	0			0			ns
Time to enable clock 1, $t_{enable\ 1}$ (see Figure 9)	225			225			ns
Time to enable clock 2, $t_{enable\ 2}$ (see Figure 9)	200			200			ns
Time to inhibit clock 1, $t_{inhibit\ 1}$ (see Figure 9)	100			100			ns
Time to inhibit clock 2, $t_{inhibit\ 2}$ (see Figure 9)	0			0			ns
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

NOTES: 3. Setup time is the interval immediately preceeding the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

4. Hold time is the interval immediately following the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS‡	MIN	TYP§	MAX	UNIT
V_{IH}	High-level input voltage	1 thru 3		2			V
V_{IL}	Low-level input voltage	2 thru 4				0.7	V
V_{OH}	High-level output voltage	1 and 2	V_{CC} = MIN, I_{OH} = −100 μA	2.4			V
V_{OL}	Low-level output voltage	3 and 4	V_{CC} = MIN, I_{OL} = 2 mA			0.3	V
I_{IH}	High-level input current into any input except M or A	5	V_{CC} = MAX, V_I = 2.4 V			10	μA
			V_{CC} = MAX, V_I = 5.5 V			100	
I_{IH}	High-level input current into M or A	5	V_{CC} = MAX, V_I = 2.4 V			20	μA
			V_{CC} = MAX, V_I = 5.5 V			200	
I_{IL}	Low-level input current into any input except M or A	6	V_{CC} = MAX, V_I = 0.3 V			−0.18	mA
I_{IL}	Low-level input current into M or A	6	V_{CC} = MAX, V_I = 0.3 V			−0.36	mA
I_{OS}	Short-circuit output current¶	7	V_{CC} = MAX	−3		−15	mA
I_{CC}	Supply current	8	V_{CC} = MAX		3.8	9	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

§This typical value is at V_{CC} = 5 V, T_A = 25°C.

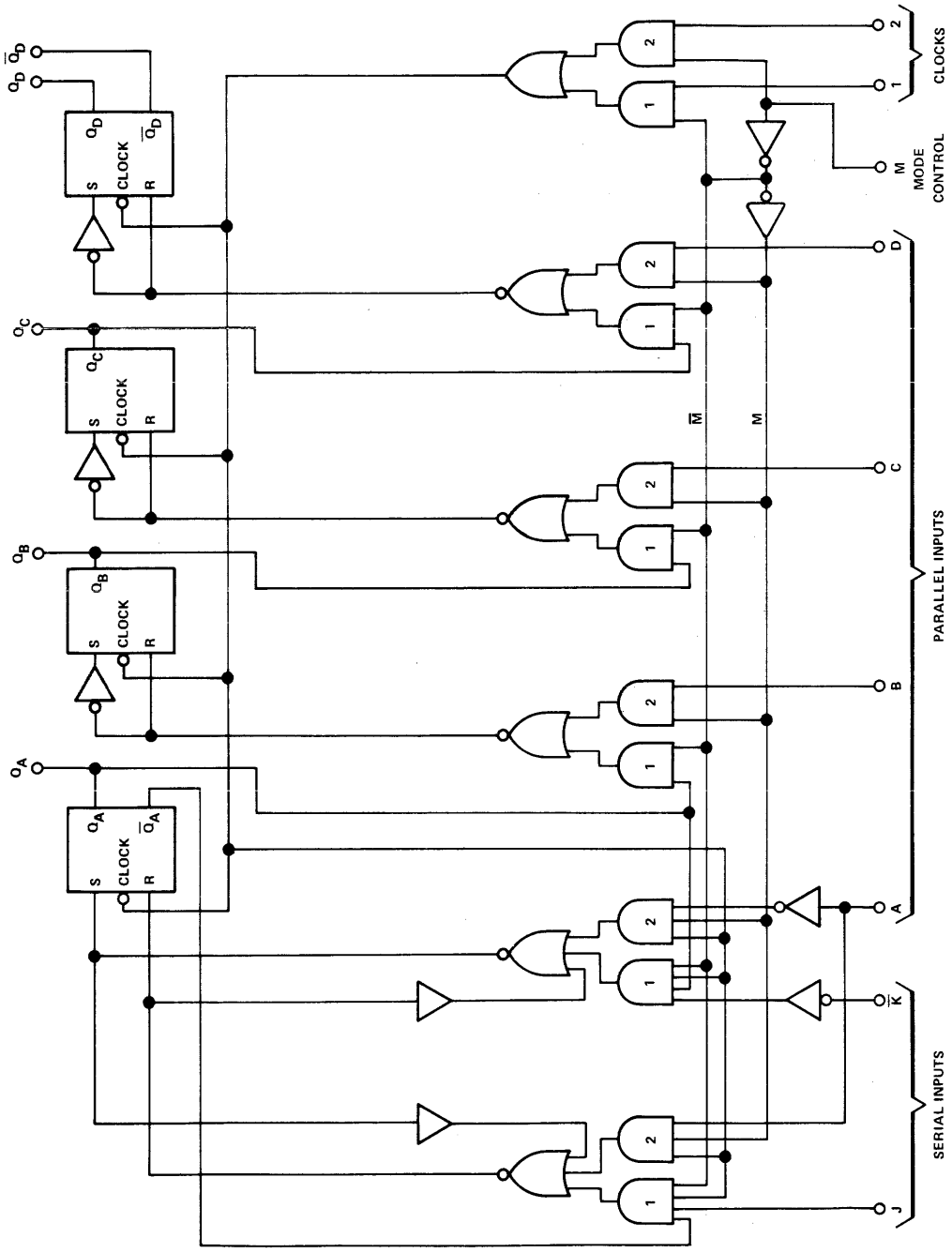
¶Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	10	C_L = 50 pF, R_L = 4 kΩ	3	5		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clock 1 or clock 2				115	200	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock 1 or clock 2				125	200	ns

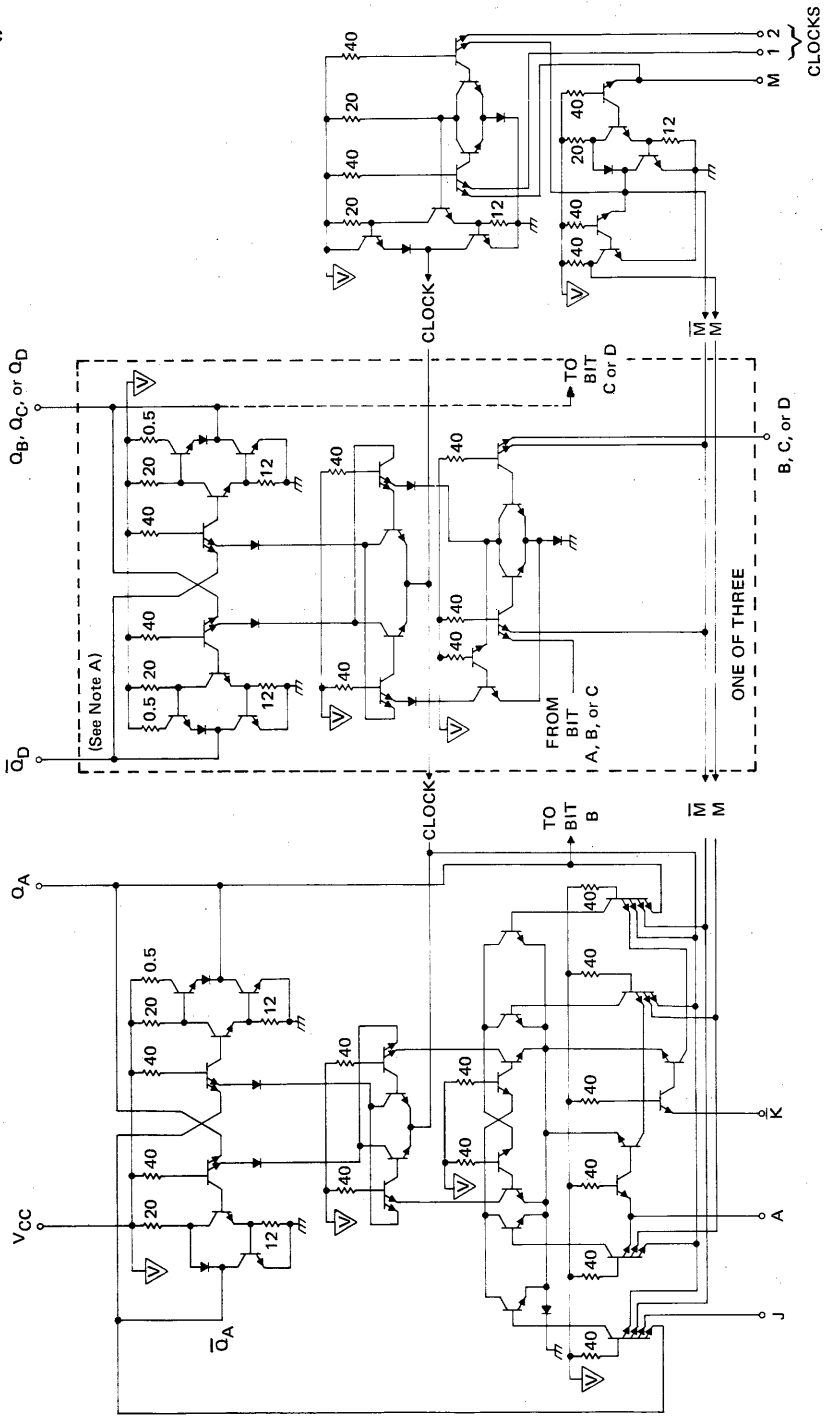
9

functional block diagram



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

schematic

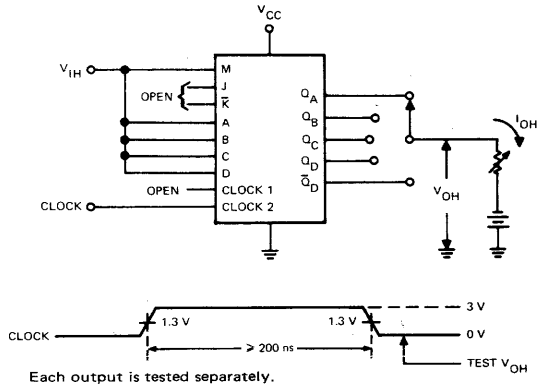


NOTES: A. Internal outputs $\bar{Q}_B$ and $\bar{Q}_C$ are as shown for $\bar{Q}_A$; i.e., they are not of the active-pullup type.
B. Resistor values shown are nominal in kilohms.
▽ . . . V_{CC} bus

9

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



Each output is tested separately.

FIGURE 1–V_{IH}, V_{OH}

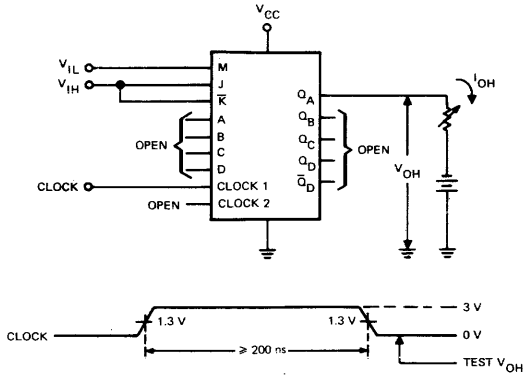
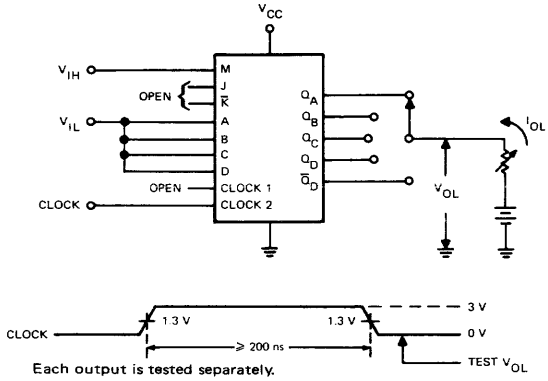


FIGURE 2–V_{IH}, V_{IL}, V_{OH}



Each output is tested separately.

FIGURE 3–V_{IH}, V_{IL}, V_{OL}

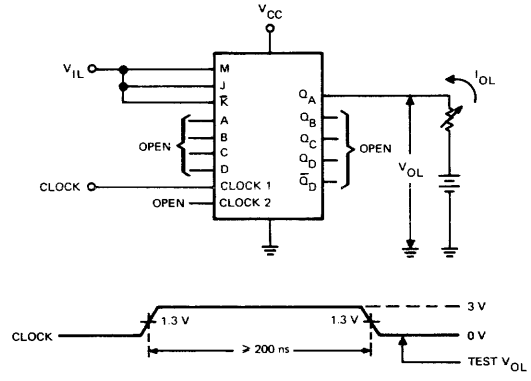
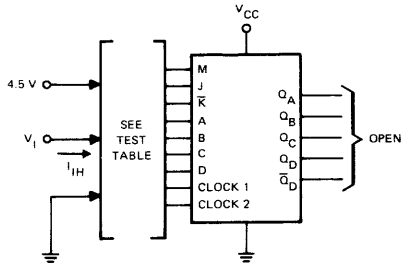


FIGURE 4–V_{IL}, V_{OL}



Each input is tested separately.

TEST TABLE

APPLY V_I	APPLY 4.5 V	APPLY GND
M	NONE	CLOCK 2
J	M and A	CLOCK 2 (Note)
$\overline{K}$	NONE	NONE
INPUT A	NONE	M and CLOCK 1
INPUTS B, C, or D	NONE	M
CLOCK 1	M	NONE
CLOCK 2	NONE	M

NOTE: Apply momentary high, then ground.

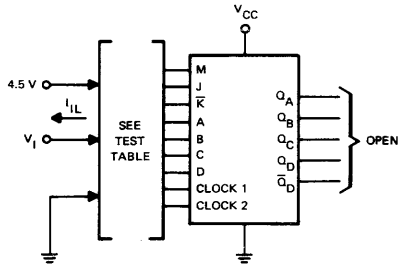
FIGURE 5–I_{IH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

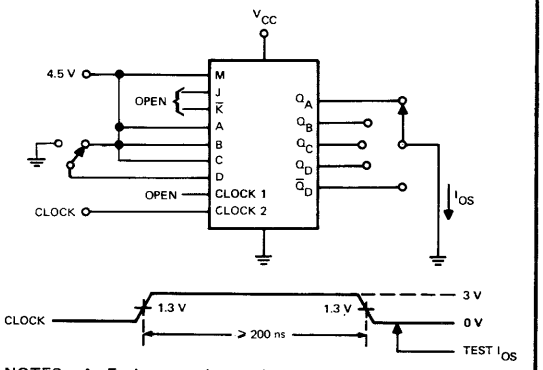


Each input is tested separately.

TEST TABLE

APPLY V_I	APPLY 4.5 V	APPLY GND
M	CLOCK 2	NONE
J	CLOCK 1	Q_A and M
$\overline{K}$	NONE	NONE
INPUT A	M and CLOCK 2	NONE
INPUTS B, C, or D	M	NONE
CLOCK 1	NONE	M
CLOCK 2	M	NONE

FIGURE 6–I_{IL}



NOTES: A. Each output is tested separately.
B. When testing Q_D or $\overline{Q}_D$, input D is connected to 4.5 V or ground, respectively.

FIGURE 7–I_{OS}

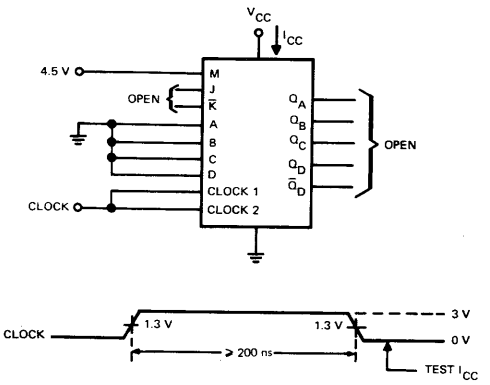
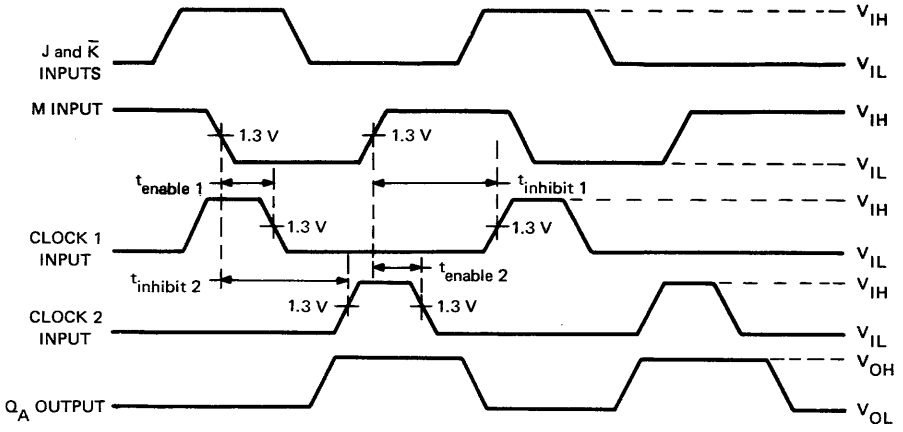


FIGURE 8–I_{CC}

recommended clock enable/input times



NOTE: A input is at the low level.

VOLTAGE WAVEFORMS

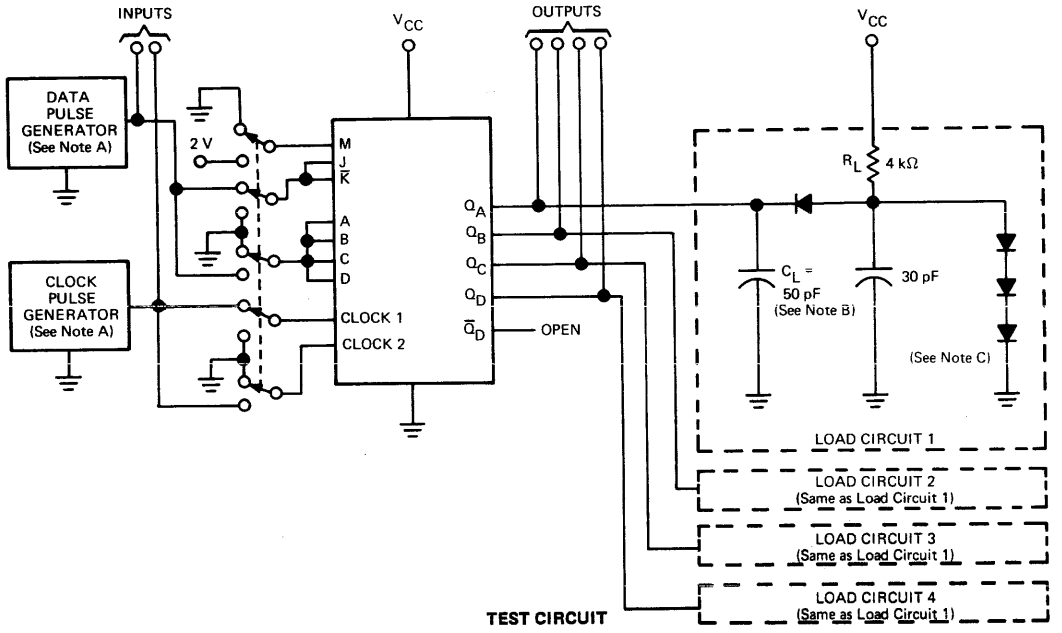
FIGURE 9–CLOCK ENABLE/INHIBIT TIMES

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

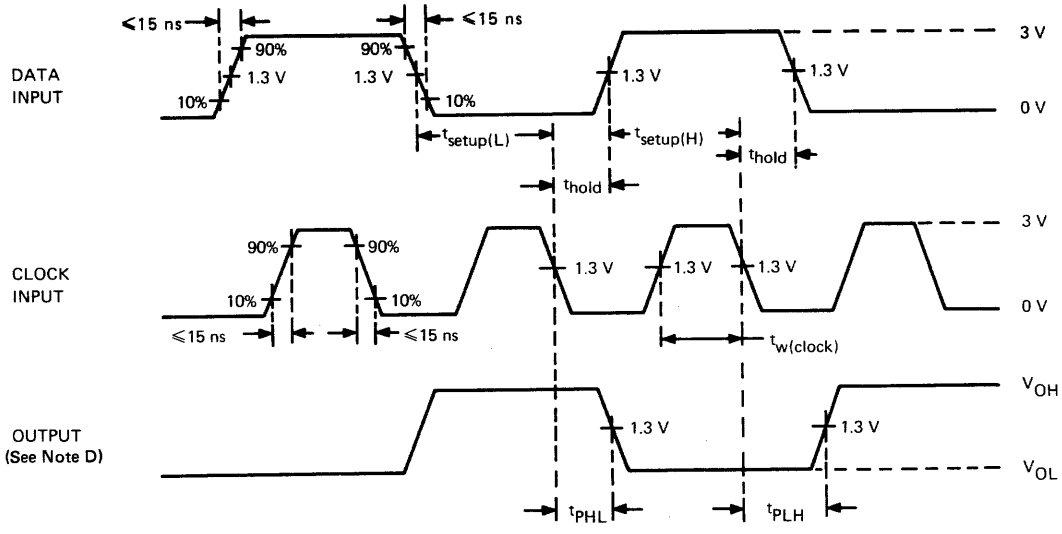
9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$. For data pulse generator: $t_w \geq 150$ ns, PRR ≤ 500 kHz, $t_{setup(L)} = 120$ ns, and $t_{setup(H)} = 100$ ns. For clock pulse generator: $t_w \geq 200$ ns and PRR ≤ 1 MHz. When testing f_{max}, vary PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N916.

D. When data input is applied to J and $\overline{K}$ inputs, the output waveform applies only to output Q_A.

FIGURE 10—SWITCHING TIMES

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

FUNCTION TABLES

BIT TIME	OPERATION AT NEXT BIT TIME	MODE CONTROL M	PARALLEL INPUTS A	B	C	D	SERIAL INPUTS J	$\overline{K}$	OUTPUTS Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
TABLE 1–PARALLEL LOADING													
n	Parallel load	H	A_n	B_n	C_n	D_n	X	X	X	X	X	X	X
n+1	Parallel load	H	A_{n+1}	B_{n+1}	C_{n+1}	D_{n+1}	X	X	A_n	B_n	C_n	D_n	$\overline{D}_n$
n+2	Parallel load	H	H	H	L	H	X	X	A_{n+1}	B_{n+1}	C_{n+1}	D_{n+1}	$\overline{D}_{n+1}$
n+3	Determined by M	X	X	X	X	X	X	X	H	H	L	H	L
TABLE 2–J-$\overline{K}$ SERIAL LOADING AND RIGHT SHIFT													
n	S.R., hold Q_A	L	X	X	X	X	L	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	$\overline{Q}_{Dn}$
n+1	S.R., set Q_A lo	L	X	X	X	X	L	L	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
n+2	S.R., set Q_A hi	L	X	X	X	X	H	H	L	Q_{An}	Q_{An}	Q_{Bn}	$\overline{Q}_{Bn}$
n+3	S.R., set Q_A hi	L	X	X	X	X	H	H	H	L	Q_{An}	Q_{An}	$\overline{Q}_{An}$
n+4	S.R., set Q_A lo	L	X	X	X	X	L	L	H	H	L	Q_{An}	$\overline{Q}_{An}$
n+5	S.R., set Q_A lo	L	X	X	X	X	L	L	L	H	H	L	H
n+6	S.R., toggle Q_A	L	X	X	X	X	H	L	L	L	H	H	L
n+7	S.R., toggle Q_A	L	X	X	X	X	H	L	H	L	L	H	L
n+8	Determined by M	X	X	X	X	X	X	X	L	H	L	L	H
TABLE 3–SERIAL LOADING WITH D INPUT AND LEFT SHIFT (See Figure 11)													
n	S.L., set Q_D to D_n	H	Q_{Bn}	Q_{Cn}	Q_{Dn}	D_n	X	X	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	$\overline{Q}_{Dn}$
n+1	S.L., set Q_D lo	H	Q_{Cn}	Q_{Dn}	D_n	L	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	D_n	$\overline{D}_n$
n+2	S.L., set Q_D hi	H	Q_{Dn}	D_n	L	H	X	X	Q_{Cn}	Q_{Dn}	D_n	L	H
n+3	S.L., set Q_D hi	H	D_n	L	H	H	X	X	Q_{Dn}	D_n	L	H	L
n+4	S.L., set Q_D lo	H	L	H	H	L	X	X	D_n	L	H	H	L
n+5	Determined by M	X	X	X	X	X	X	X	L	H	H	L	H

H = high level, L = low level, X = irrelevant
A_n = state of input A at bit time n
S.R. = shift right, S.L. = shift left
Q_{An} = state of output Q_A at bit time n

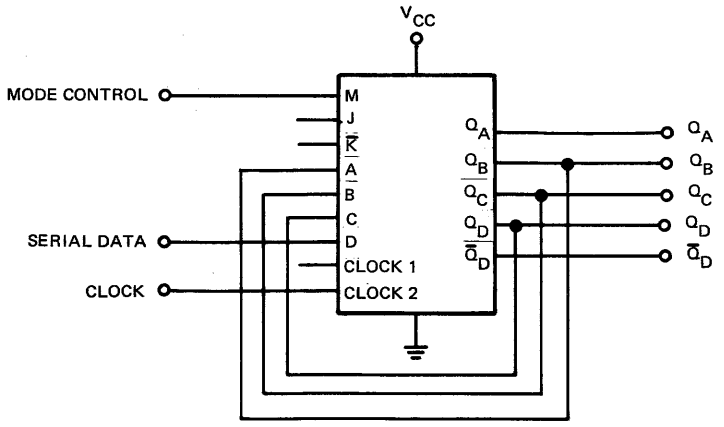


FIGURE 11–CONNECTIONS FOR LEFT SHIFT

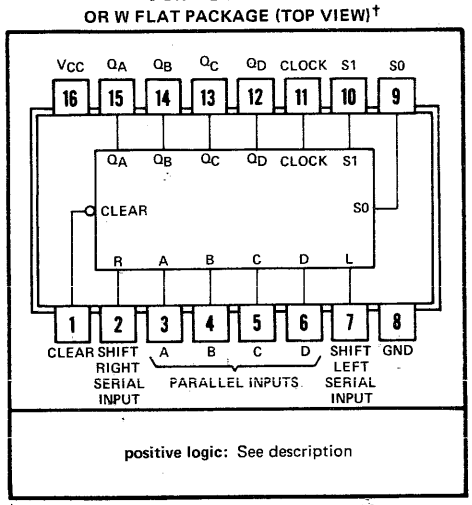
9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54194, SN74194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

- Parallel Inputs and Outputs
- Four Operating Modes:
  - Synchronous Parallel Load
  - Left Shift
  - Right Shift
  - Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

	MODE CONTROL	
	S1	S0
Parallel (Broadside) Load	H	H
Shift Right (In the direction Q_A toward Q_D)	L	H
Shift Left (In the direction Q_D toward Q_A)	H	L
Inhibit Clock (Do nothing)	L	L

9

In the parallel-load mode, data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. Clocking of the flip-flops is inhibited when both mode-control inputs are low. The mode controls should be changed only while the clock input is high.

These four-bit shift registers are compatible with most other TTL and DTL logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 36 megahertz and power dissipation is typically 195 mW.

The SN54194 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74194 is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54194 Circuits . . . . . −55°C to 125°C
SN74194 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54194			SN74194			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{setup} (see Figure 1)	Mode control	30			30			ns
	Serial and parallel data	20			20			ns
	Clear inactive-state	25			25			ns
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54194	−20		−57	mA
			SN74194	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			39	63	mA

NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5 V, applied to clock.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

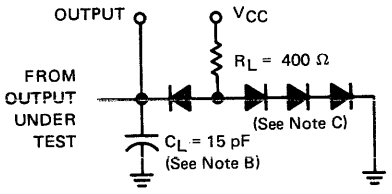
§Not more than one output should be shorted at a time.

9

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		7	14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		7	17	26	

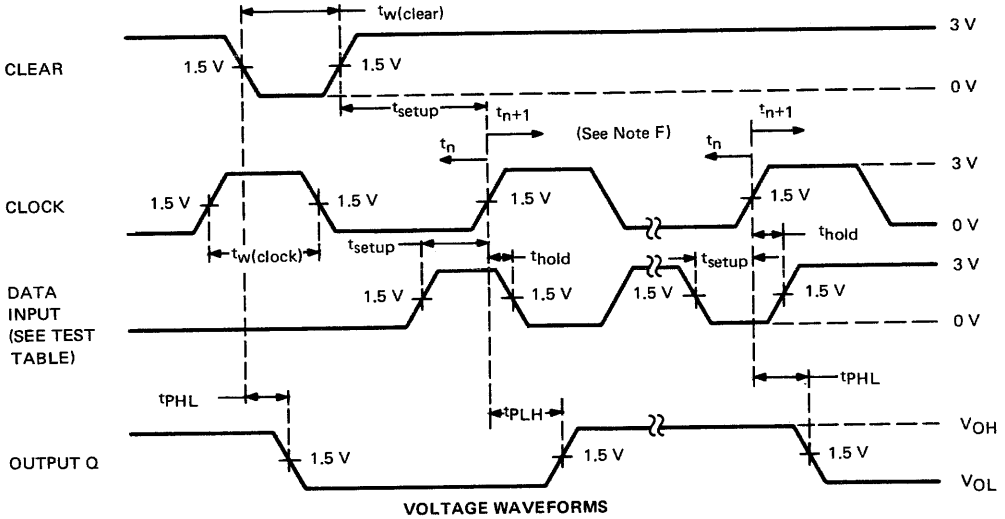
PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5 V	4.5 V	Q_A at t_{n+1}
B	4.5 V	4.5 V	Q_B at t_{n+1}
C	4.5 V	4.5 V	Q_C at t_{n+1}
D	4.5 V	4.5 V	Q_D at t_{n+1}
L Serial Input	4.5 V	0 V	Q_A at t_{n+4}
R Serial Input	0 V	4.5 V	Q_D at t_{n+4}



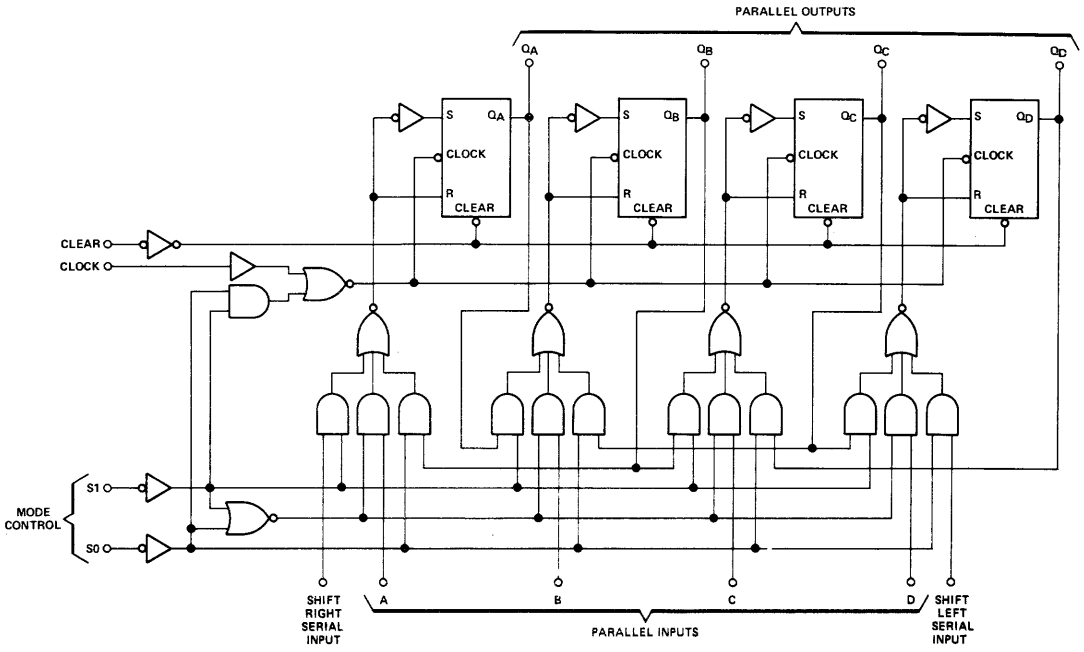
VOLTAGE WAVEFORMS

NOTES
A. The clock pulse has the following characteristics: $t_{w(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq 20$ ns and t_{hold} = 0 ns. When testing f_{max}, vary the clock PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. A clear pulse is applied prior to each test.
E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+4} with a functional test.
F. t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+4} = bit time after four clocking transitions.

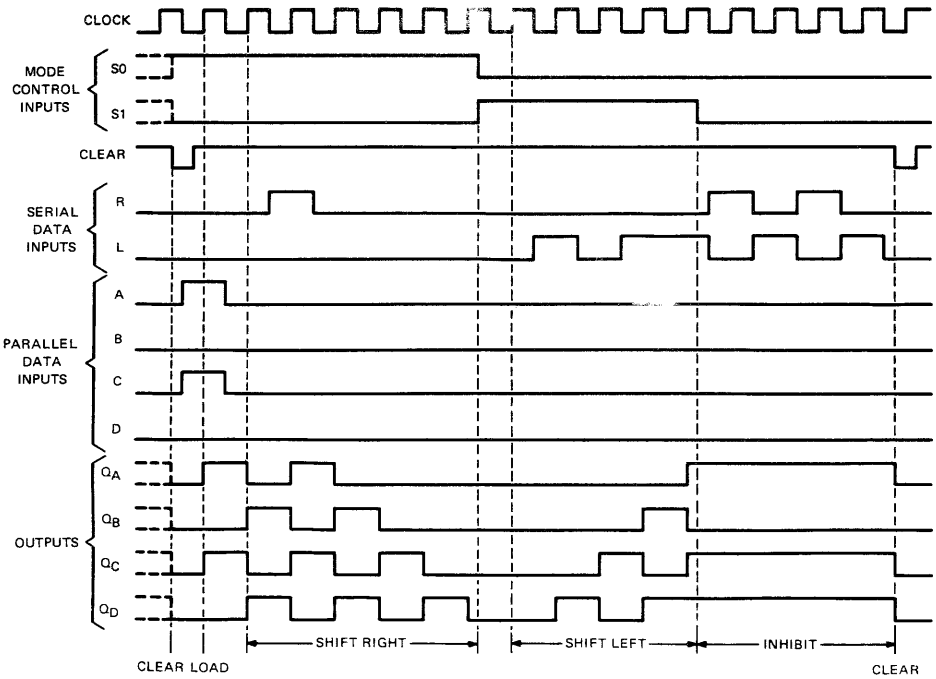
FIGURE 1–SWITCHING TIMES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram



typical clear, load, right-shift, left-shift, inhibit, and clear sequences



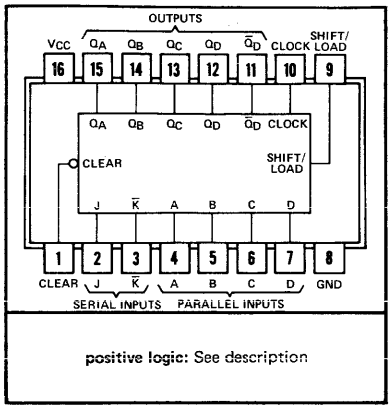
9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54195, SN74195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

- Synchronous Parallel Load
- Positive Edge-Triggered Clocking
- Parallel Inputs and Outputs from Each Flip-Flop
- Direct Overriding Clear
- J and $\overline{K}$ Inputs to First Stage
- Complementary Outputs from Last Stage

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

Parallel (Broadside) Load

Shift (In direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the truth table.

9

These shift registers are fully compatible with most other TTL and DTL families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, including the clock input. Maximum input clock frequency is typically 39 megahertz and power dissipation is typically 195 milliwatts. The SN54195 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74195 is characterized for operation from 0°C to 70°C.

TRUTH TABLE

Inputs at t_n		Outputs at t_{n+1}				
J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level, L = low level
NOTES: A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse
C. Q_{An} = state of Q_A at t_n

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54195 Circuits . . . . . −55°C to 125°C
SN74195 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54195			SN74195			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock input pulse, $t_{w(clock)}$		16			16			ns
Width of clear input pulse, $t_{w(clear)}$		12			12			ns
Setup time, t_{setup} (see Figure 1)	Shift/load	25			25			ns
	Serial and parallel data	15			15			
	Clear inactive-state	25			25			
Shift/load release time, $t_{release}$ (see Figure 1)				10			10	ns
Serial and parallel data hold time, t_{hold} (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54195	−20		−57	mA
			SN74195	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			39	63	mA

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear, and then applying a momentary ground, followed by 4.5 V, to clock.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

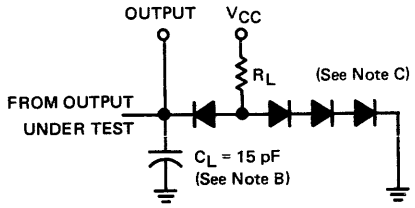
§Not more than one output should be shorted at a time.

9

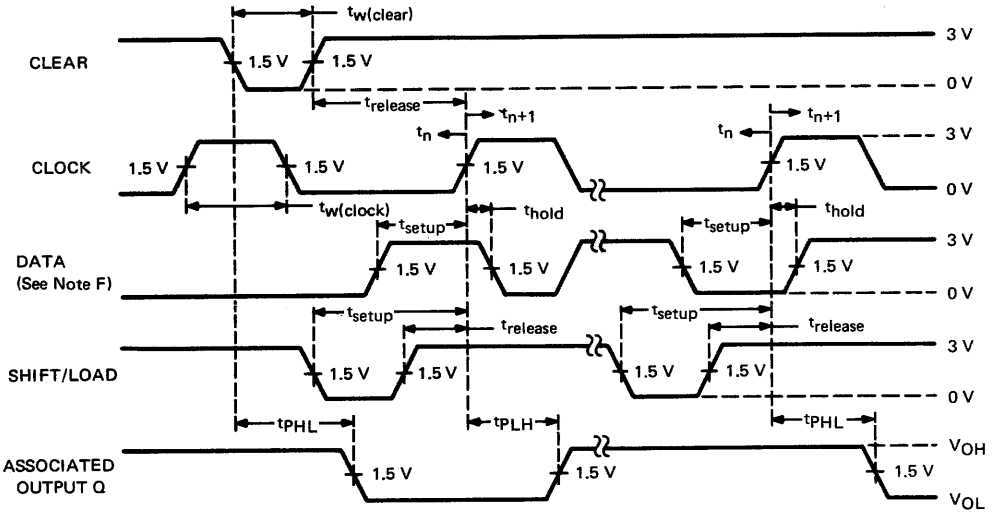
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	30	39		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		6	14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		7	17	26	ns

PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST



VOLTAGE WAVEFORMS

NOTES: A. The clock pulse has the following characteristics: $t_{w(clock)} \geq$ 16 ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq$ 12 ns and t_{hold} = 0 ns. When testing f_{max}, vary the clock PRR.

B. C_L inlcudes probe and jig capacitance.

C. All diodes are 1N3064.

D. A clear pulse is applied prior to each test.

E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+4} with a functional test.

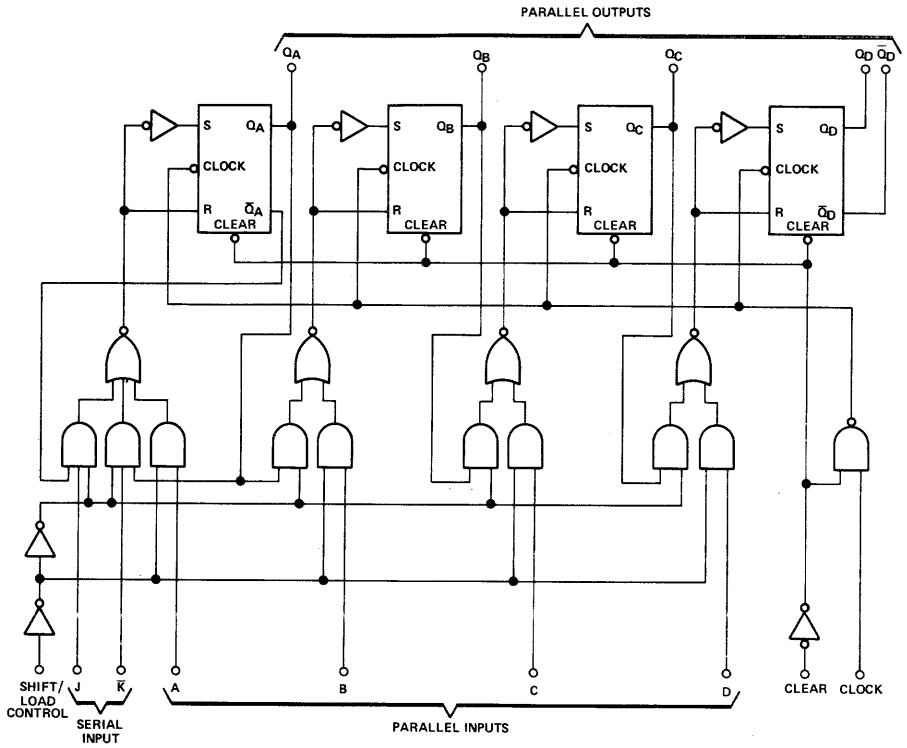
F. J and $\overline{K}$ inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.

G. t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+4} = bit time after four clocking transitions.

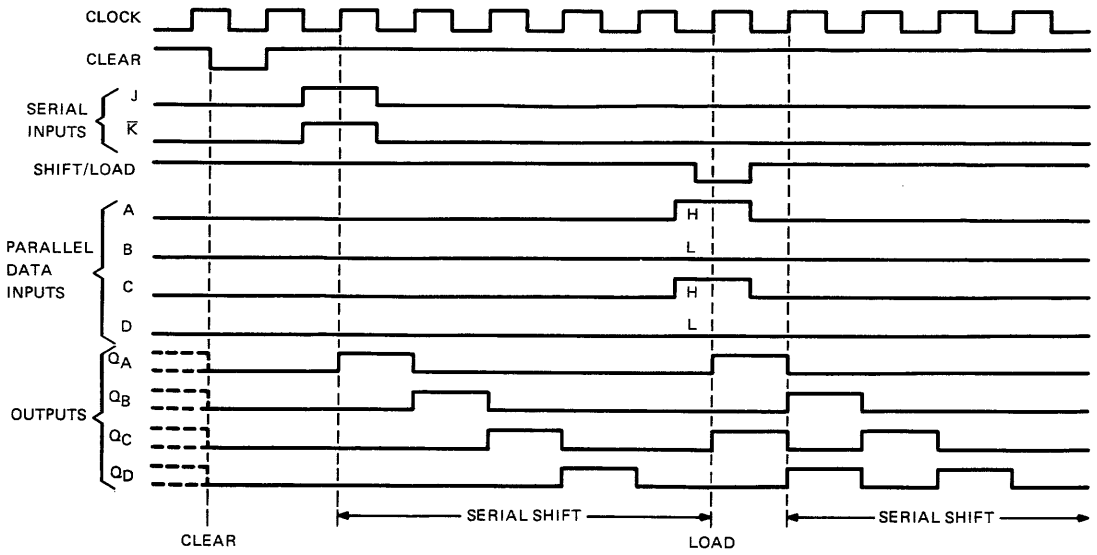
FIGURE 1–SWITCHING TIMES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram



typical clear, shift, and load sequences



9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5491A, SN7491A
8-BIT SHIFT REGISTERS

MSI TTL SHIFT REGISTERS
for applications in

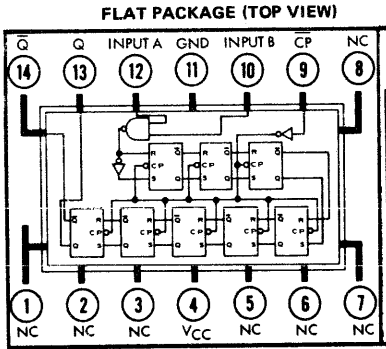
- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

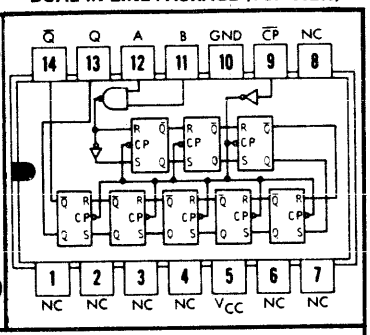
t_n		t_{n+8}
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

NOTES:
1. t_n = bit time before clock.
2. t_{n+8} = bit time after 8 clock pulses.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See Truth Table

NC—No Internal Connection

description

These monolithic serial-in, serial-out, 8-bit shift registers utilizing transistor-transistor logic (TTL) circuits, are composed of eight R-S master-slave flip-flops, input gating, and a clock driver. The register is capable of storing and transferring data at clock rates up to 18 MHz while maintaining a typical noise-immunity level of 1 volt. Power dissipation is typically 175 milliwatts, and a full fan-out of 10 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B,and $\overline{CP}$) appear as only one TTL input load.

The clock pulse inverter/driver causes these circuits to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift-register to be fully compatible with other edge-triggered synchronous functions.

9

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 3) . . . . . 7 V
Input Voltage, V_{in} (See Notes 3 and 4) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5491A Circuits . . . . . −55°C to 125°C
SN7491A Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3): SN5491A Circuits	4.5	5	5.5	V
SN7491A Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 7)	25			ns
Input Setup Time, t_{setup} (See Figure 7)	25			ns
Input Hold Time, t_{hold} (See Figure 7)	0			

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics over operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	2	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX, V_{out} = 0	SN5491A	−20		−57	mA
				SN7491A	−18		−57	mA
I_{CC}	Supply current	6	V_{CC} = MAX, V_{in} = 4.5 V	SN5491A		35	50	mA
				SN7491A		35	58	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

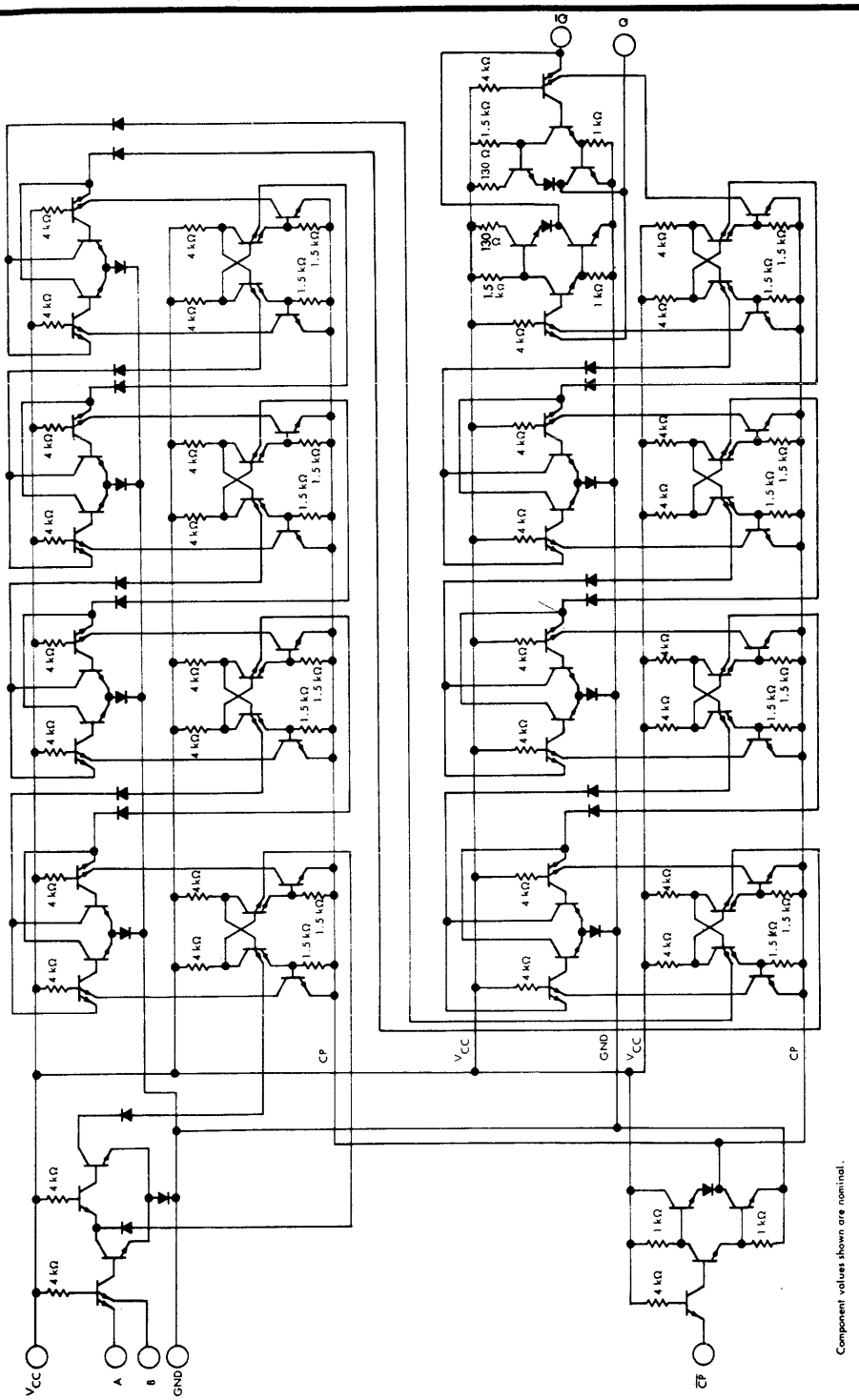
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency		C_L = 15 pF, R_L = 400 Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	7	C_L = 15 pF, R_L = 400 Ω		24	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	7	C_L = 15 pF, R_L = 400 Ω		27	40	ns

9

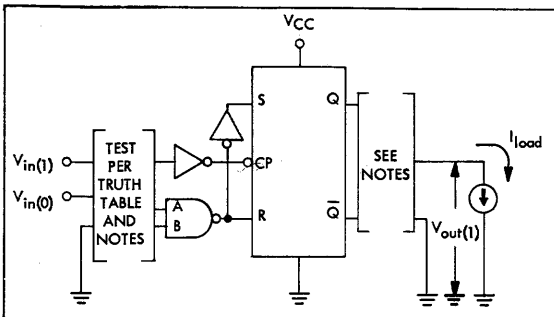
schematic



Component values shown are nominal.

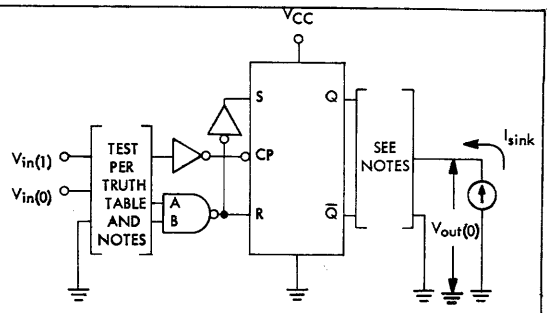
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



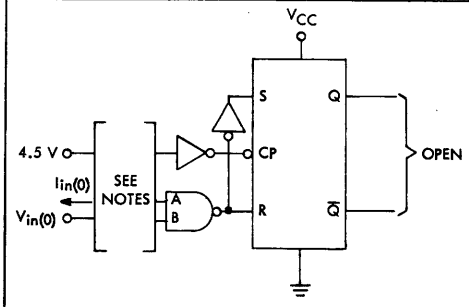
1. Each output is tested separately.
2. When testing $V_{out(1)}$ and I_{load}, ground all inputs and the unused output, then measure parameters specified.

FIGURE 1



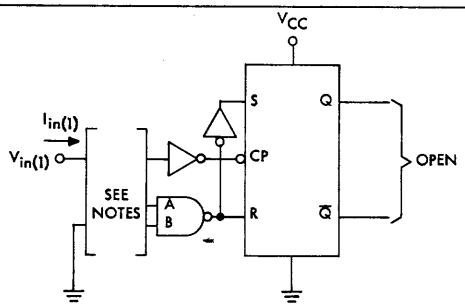
1. Each output is tested separately.
2. When testing $V_{out(0)}$ and I_{sink}, ground all inputs. Apply a momentary ground to the output to be tested then measure parameters specified.

FIGURE 2



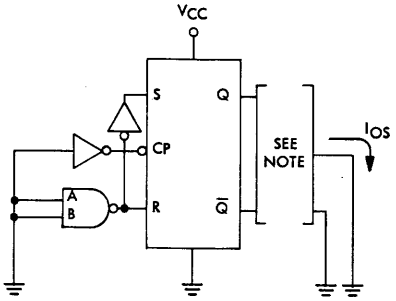
1. When testing input A apply 4.5 V to input B.
2. When testing input B apply 4.5 V to input A.

FIGURE 3



1. When testing input A ground input B.
2. When testing input B ground input A.

FIGURE 4



1. Ground the unused output then measure parameter specified.

FIGURE 5

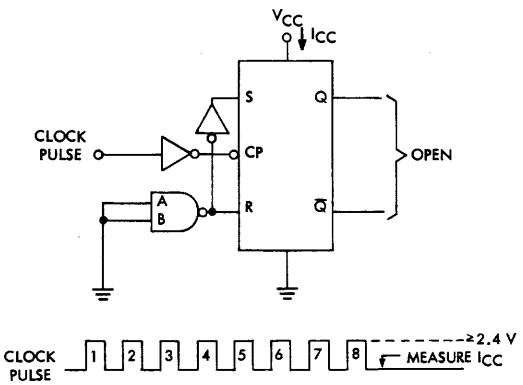


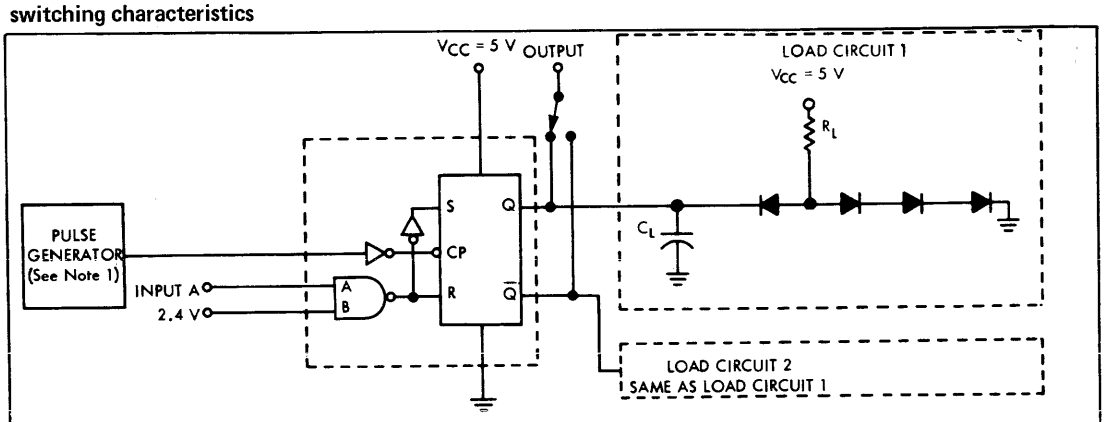
FIGURE 6

† Arrows indicate actual direction of current flow.

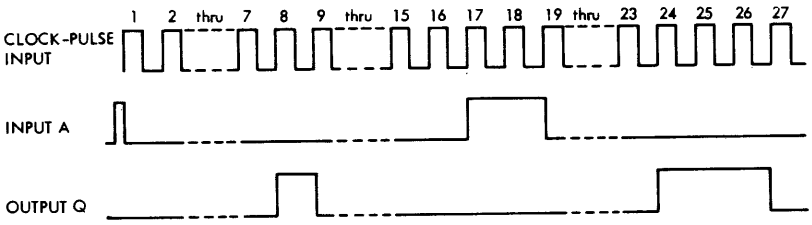
9

PARAMETER MEASUREMENT INFORMATION

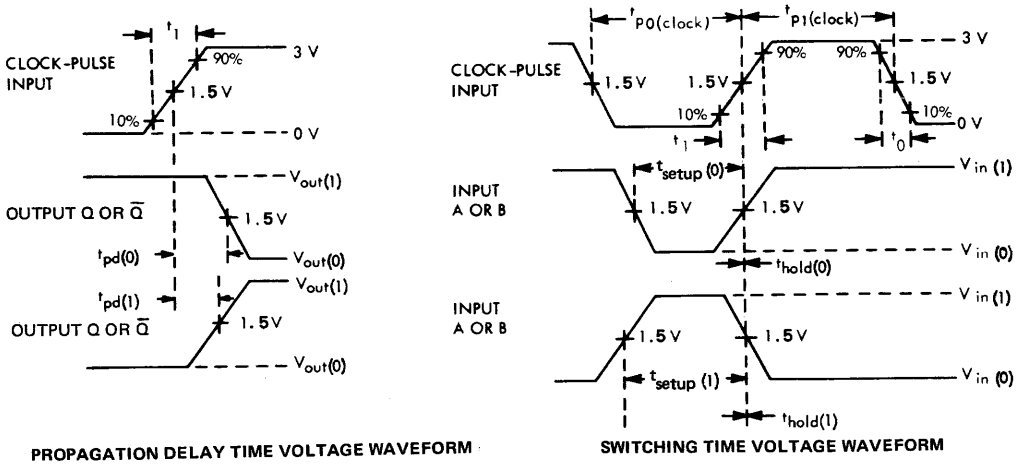
switching characteristics



TEST CIRCUIT



TYPICAL INPUT/OUTPUT WAVEFORMS



PROPAGATION DELAY TIME VOLTAGE WAVEFORM

SWITCHING TIME VOLTAGE WAVEFORM

NOTES: 1. The generator has the following characteristics: $V_{in(0)} \leq 0.3$ V, $V_{in(1)} \geq 2.4$ V, $t_1 = t_0 = 10$ ns, $t_{p1(clock)} = 500$ ns, $t_{p0(clock)} = 500$ ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. All diodes are 1N3064.

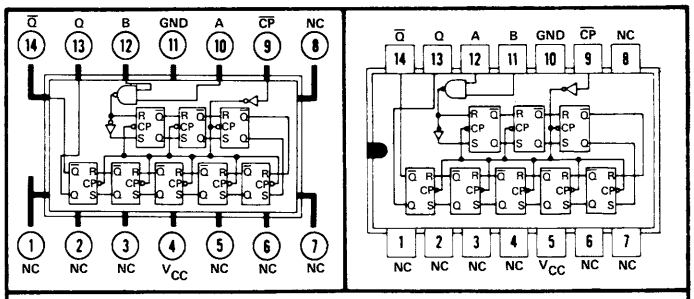
FIGURE 7 – SN5491A/SN7491A SWITCHING TIMES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54L91, SN74L91
8-BIT SHIFT REGISTERS

T
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic

TRUTH TABLE		
t_n		t_{n+8}
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

NOTES:
1. t_n = Bit time before clock pulse.
2. t_{n+8} = Bit time after 8 clock pulses.
3. NC — No internal connection.

positive logic: see truth table

description

This monolithic serial-in, serial-out, 8-bit shift register utilizes low-power transistor-transistor logic (TTL) circuits. The shift register, composed of eight R-S master-slave flip-flops, includes input gating and a clock driver. The register is capable of storing and transferring data at typical clock rates of 6.5 MHz while maintaining a typical noise-immunity level of 0.9 volt. Power dissipation is typically 17.5 milliwatts, and full fan-out of 10 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B, and clock) appear as only one low-power TTL input load.

The clock pulse inverter/driver causes the register to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift register to be fully compatible with edge-triggering flip-flops.

9

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L91 Circuits	4.5	5	5.5	V
SN74L91 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Input Setup Time, t_{setup} (See Figure 7)	120			ns
Input Hold Time, t_{hold} (See Figure 7)	0			
Width of Logical 0 Level Clock Pulse, $t_{p0(clock)}$ (See Figure 7)	150			ns
Width of Logical 1 Level Clock Pulse, $t_{p1(clock)}$ (See Figure 7)	100			ns
Operating Free-Air Temperature Range, T_A: SN54L91 Circuits	−55	25	125	°C
SN74L91 Circuits	0	25	70	°C

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 8 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN54L91 Circuits . . . . . −55°C to 125°C
SN74L91 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

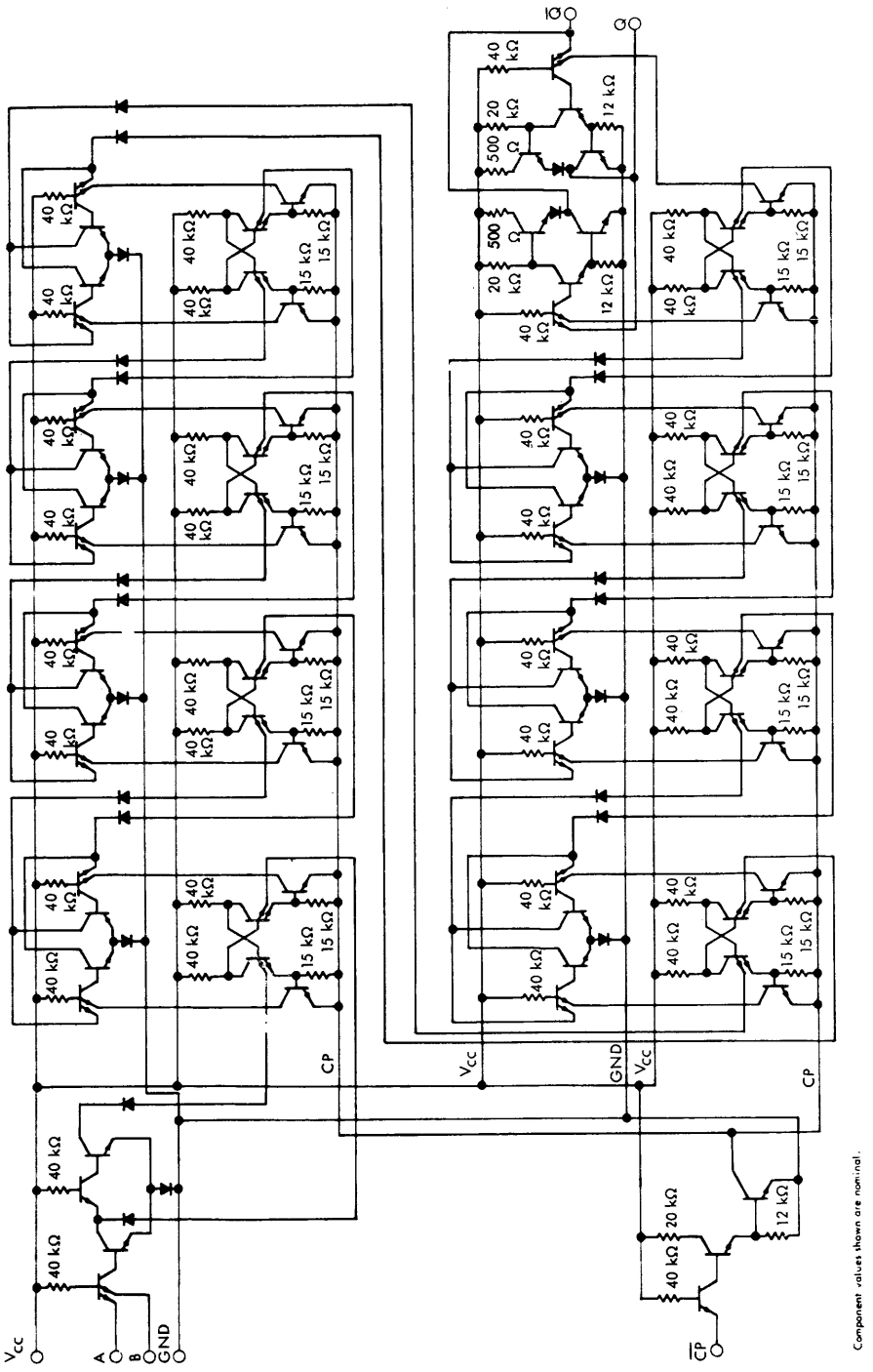
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1		2		V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2			0.7	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	2	V_{CC} = MIN, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current	3	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current	4	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{OS}	Short-circuit output current	5	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
I_{CC}	Supply current	6	V_{CC} = MAX, V_{in} = 5 V		6.6	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{p0(clock)}$	Minimum width of logical 0 level clock pulse	7	C_L = 50 pF, R_L = 4 kΩ		105		ns
$t_{p1(clock)}$	Minimum width of logical 1 level clock pulse	7	C_L = 50 pF, R_L = 4 kΩ		45		ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	7	C_L = 50 pF, R_L = 4 kΩ		100	150	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	7	C_L = 50 pF, R_L = 4 kΩ		55	100	ns

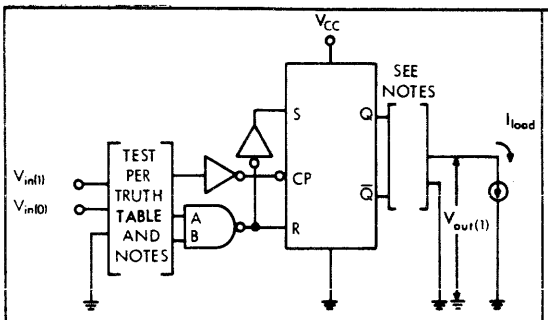
schematic



Component values shown are nominal.

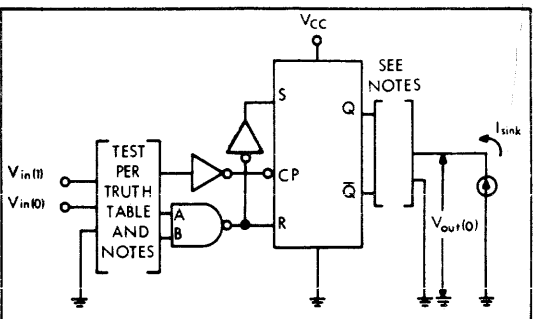
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



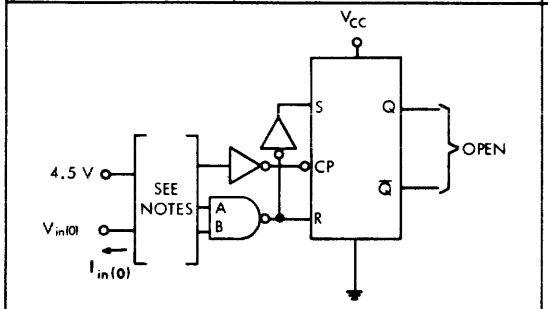
1. Each output is tested separately.
2. When testing $V_{out(1)}$ and I_{load}, ground all inputs and momentarily ground the unused output, then measure parameters specified.

FIGURE 1



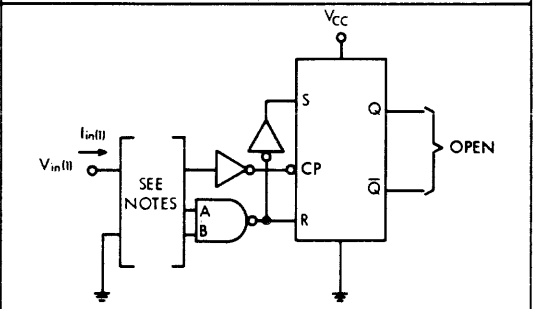
1. Each output is tested separately.
2. When testing $V_{out(0)}$ and I_{sink}, ground all inputs. Apply a momentary ground to the output to be tested, then measure parameters specified.

FIGURE 2



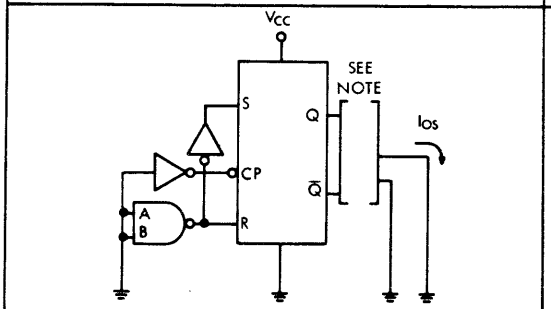
1. When testing input A apply 4.5 V to input B.
2. When testing input B apply 4.5 V to input A.

FIGURE 3



1. When testing input A ground input B.
2. When testing input B ground input A.

FIGURE 4



1. Ground the unused output, then measure parameters specified.

FIGURE 5

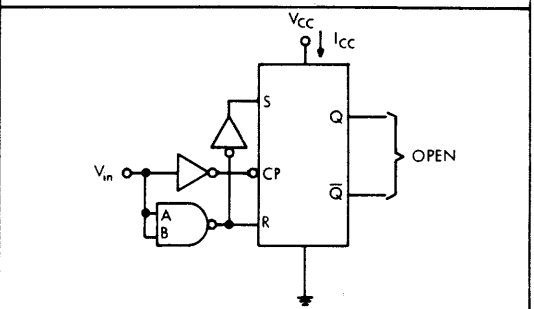
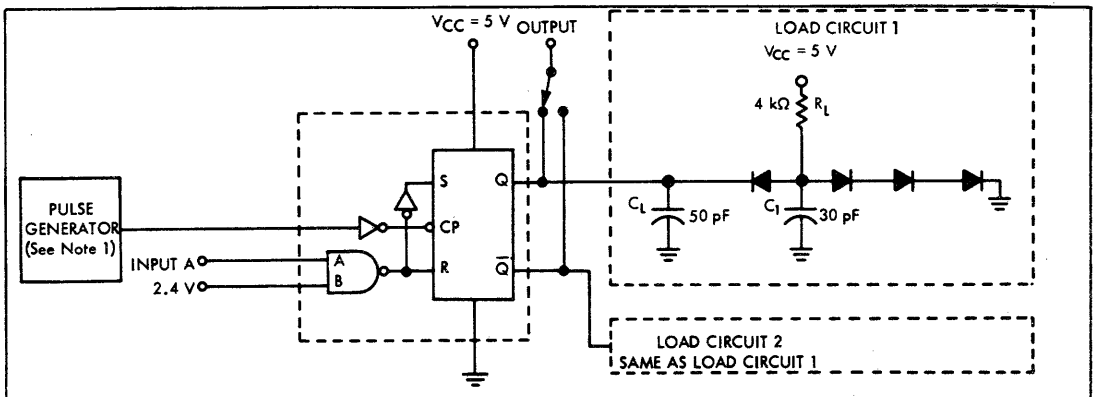


FIGURE 6

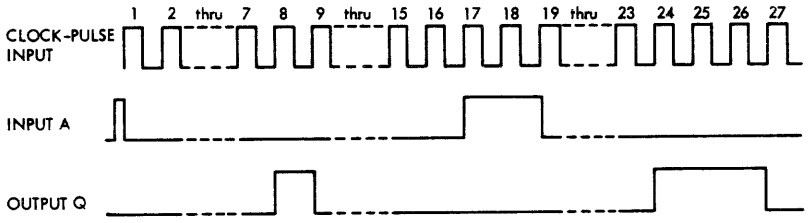
§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

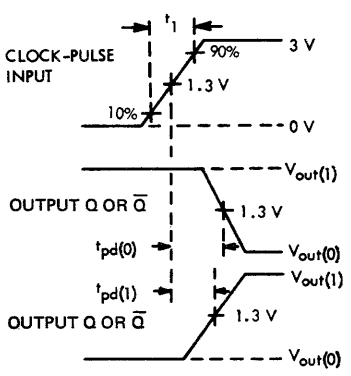
switching characteristics



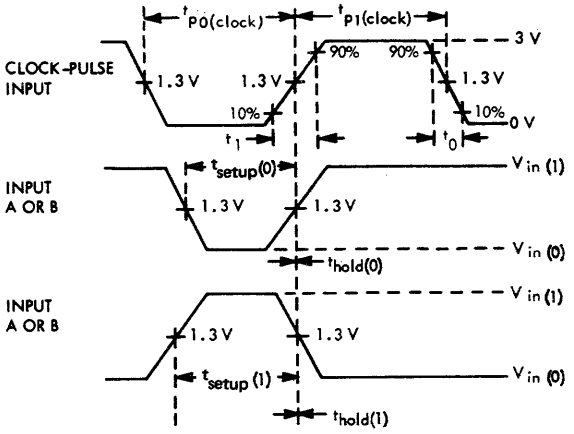
TEST CIRCUIT



TYPICAL INPUT/OUTPUT WAVEFORMS



PROPAGATION DELAY TIME VOLTAGE WAVEFORMS



SWITCHING TIME VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: $V_{in(0)} \leq 0.3$ V, $V_{in(1)} \geq 2.4$ V, $t_r = t_f = 15$ ns, $t_{p1(clock)} = 500$ ns, $t_{p0(clock)} = 500$ ns, PRR $\leq$ 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. All diodes are 1N916.

FIGURE 7 – SN54L91/SN74L91 SWITCHING TIMES

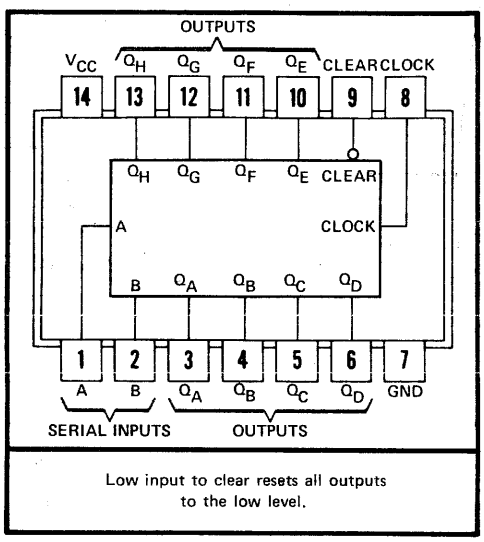
9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54164, SN74164
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

- Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear
- Typical Maximum Input Clock Frequency . . . 36 MHz

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

TRUTH TABLE
SERIAL INPUTS A AND B

INPUTS AT t_n		OUTPUT AT t_{n+1}
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

All inputs are diode-clamped to minimize transmission-line effects, and are buffered to represent only one Series 54/74 load which simplifies system design. Power dissipation is typically 21 milliwatts per bit. Maximum input clock frequency is typically 36 megahertz.

The SN54164 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74164 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54164 Circuits . . . . . −55°C to 125°C
SN74164 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

		SN54164			SN74164			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			10			10	
	Low logic level			5			5	
Input clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear input pulse, t_w		20			20			ns
Data setup time, t_{setup} (see Figure 1)		15			15			ns
Data hold time, t_{hold} (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54164			SN74164			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 8 mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−10		−27.5	−9		−27.5	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	$V_{I(clock)}$ = 0.4 V		30			30		mA
			$V_{I(clock)}$ = 2.4 V		37	54		37	54	

NOTE 2: I_{CC} is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5 V, applied to clear.

†For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

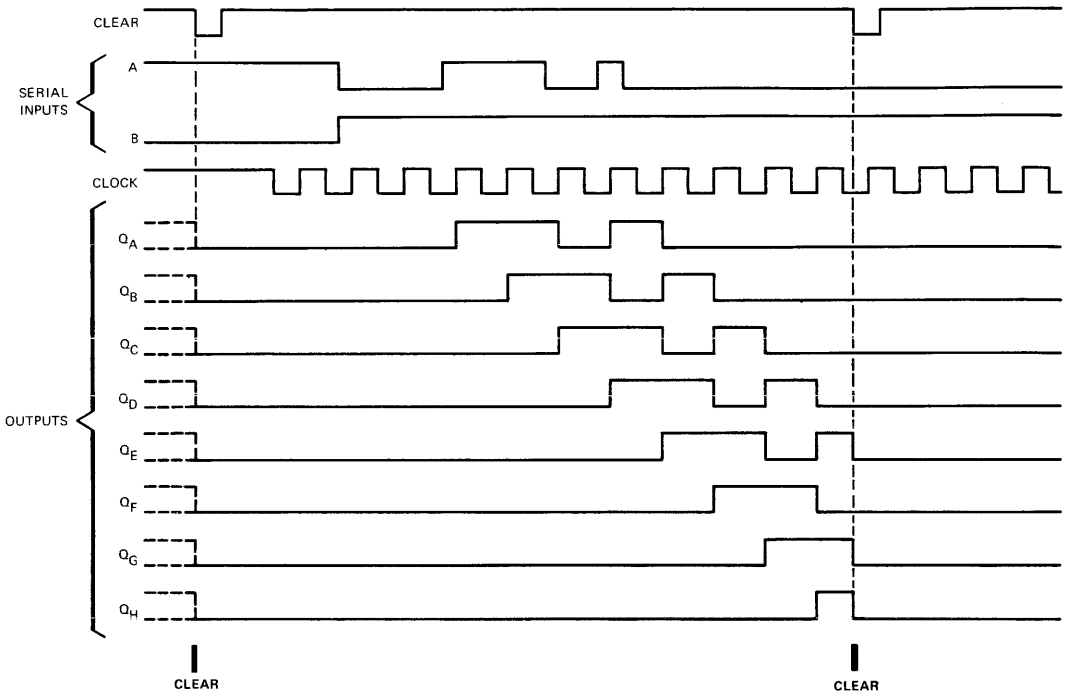
§Not more than two outputs should be shorted at a time.

9

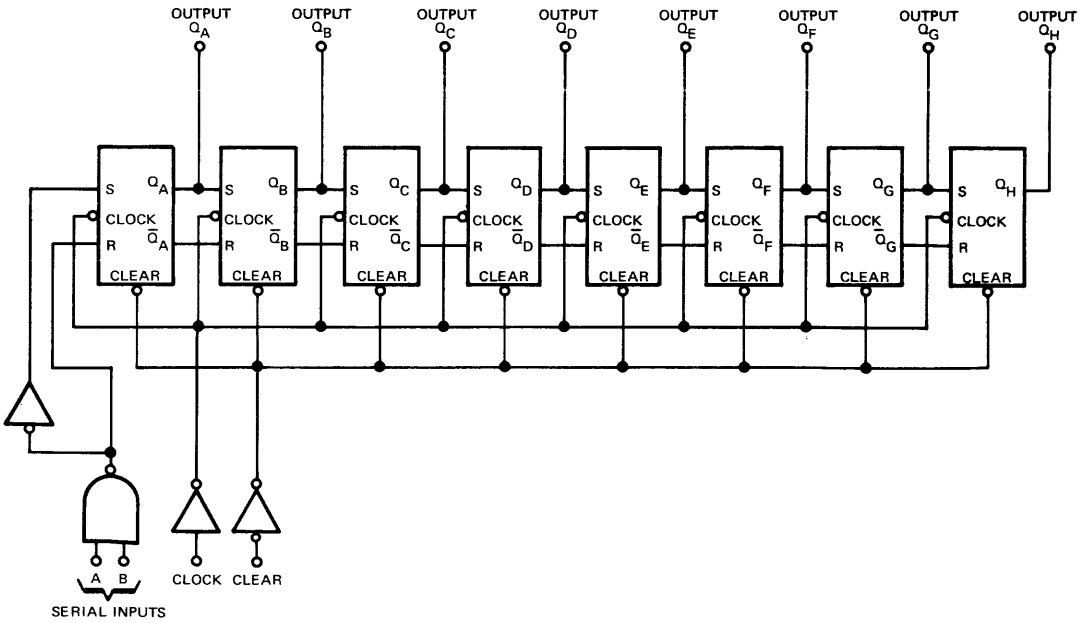
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 5

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	R_L = 800 Ω, See Figure 1	C_L = 15 pF	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input		C_L = 15 pF		24	36	ns
			C_L = 50 pF		28	42	
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input		C_L = 15 pF	8	17	27	ns
			C_L = 50 pF	10	20	30	
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clock input		C_L = 15 pF	10	21	32	ns
			C_L = 50 pF	10	25	37	

typical clear, inhibit, shift, clear, and inhibit sequences



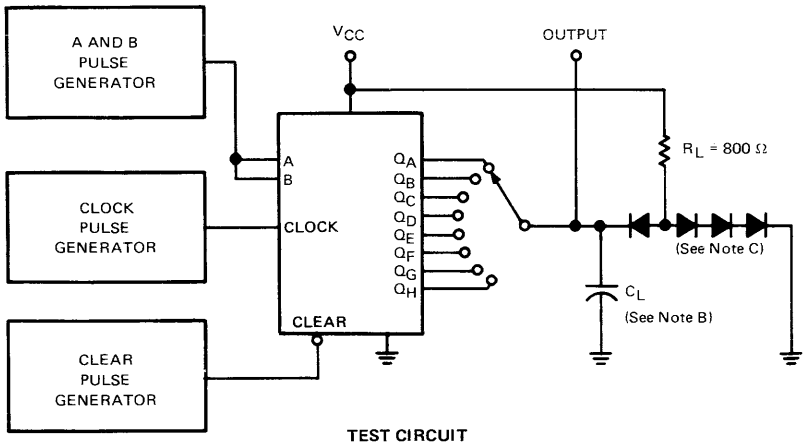
functional block diagram



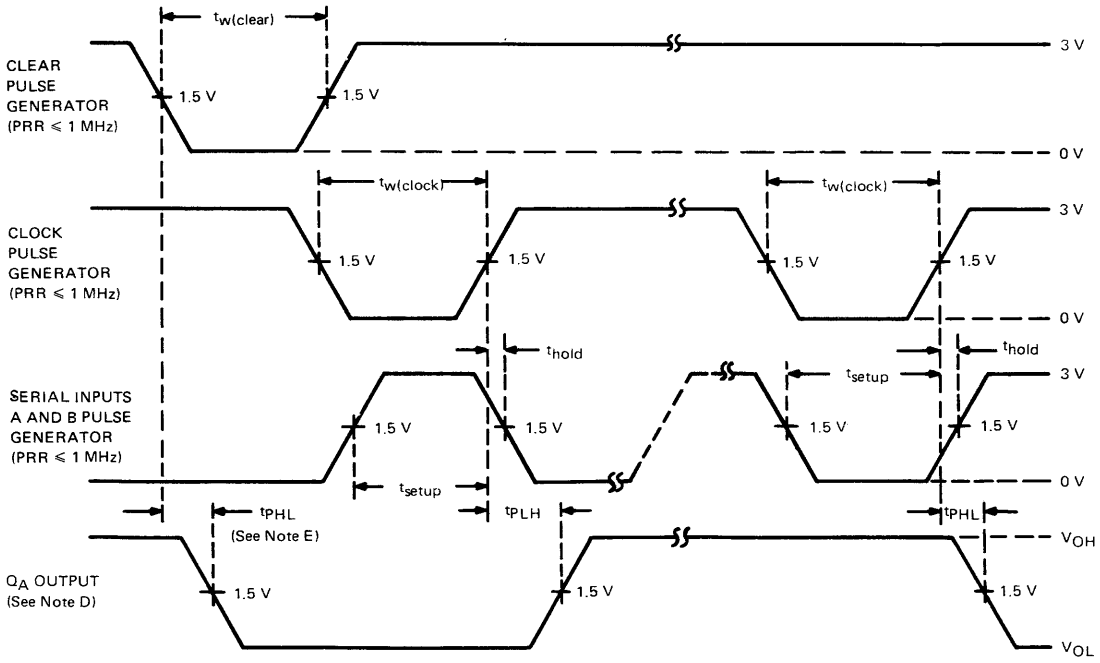
9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

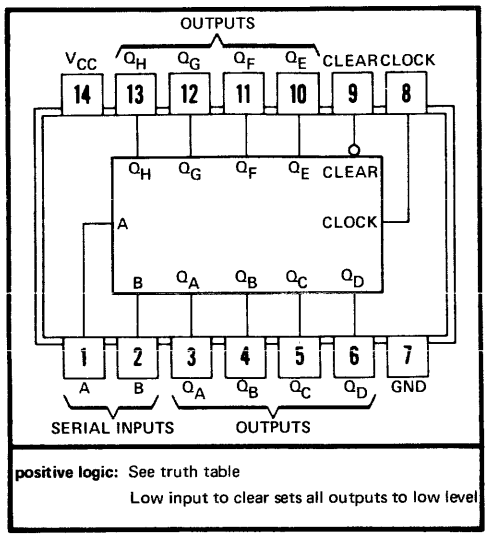
NOTES: A. The pulse generators have the following characteristics: $t_r \leqslant 10$ ns, $t_f \leqslant 10$ ns, duty cycle ⩽ 50%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
E. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.

FIGURE 1–SWITCHING TIMES

CIRCUIT TYPES SN54L164, SN74L164
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

- Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear
- Typical Maximum Input Clock Frequency . . . 18 MHz
- Typical Power Dissipation . . . 11 mW per Bit

J OR N DUAL-IN-LINE
OR T FLAT PACKAGE (TOP VIEW)†



positive logic: See truth table
Low input to clear sets all outputs to low level

†Pin assignments for these circuits are the same for all packages.

TRUTH TABLE
SERIAL INPUTS A AND B

INPUTS AT t_n		OUTPUT AT t_{n+1}
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

The circuit is the same as for the SN54164/SN74164 except that all resistor values are doubled. All inputs are diode-clamped to minimize transmission-line effects, and are buffered to represent only one-half of one normalized Series 54/74 load, or approximately five Series 54L/74L loads at a low logic level, two Series 54L/74L loads at a high logic level. Power dissipation is typically 11 milliwatts per bit. Maximum input clock frequency is typically 18 megahertz.

The SN54L164 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L164 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54L164 Circuits . . . . . −55°C to 125°C
SN74L164 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

			SN54L164			SN74L164			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	Series 54L/74L Gates				20			20	
	Series 54L/74L Gates with 8-kΩ base resistors¶	High logic level			10			10	
		Low logic level			5			5	
Input clock frequency, f_{clock}			0		12	0		12	MHz
Width of clock or clear input pulse, t_w			40			40			ns
Data setup time, t_{setup} (see Figure 1)			30			30			ns
Data hold time, t_{hold} (see Figure 1)			0			0			ns
Operating free-air temperature, T_A			−55		125	0		70	°C

¶ This applies for all inputs of circuit types SN54L164 and SN74L164.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54L164			SN74L164			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −200 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 4 mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−0.8			−0.8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−5		−20	−4		−20	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			27			27	mA

NOTE 2: I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V, applied to clear.

†For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

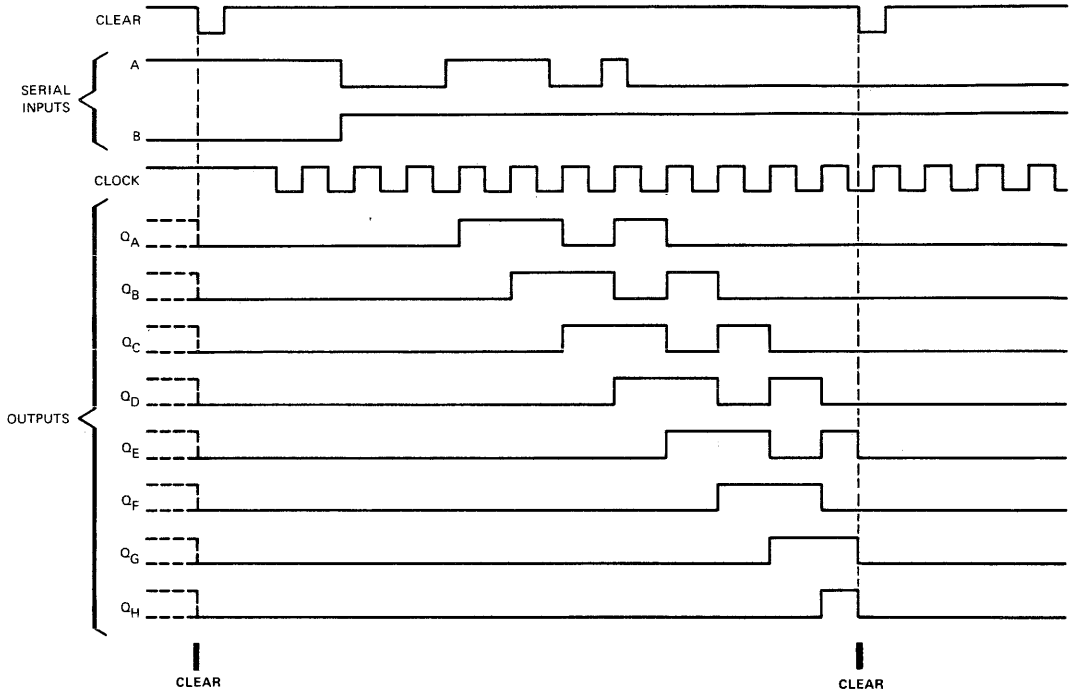
§Not more than two outputs should be shorted at a time.

9

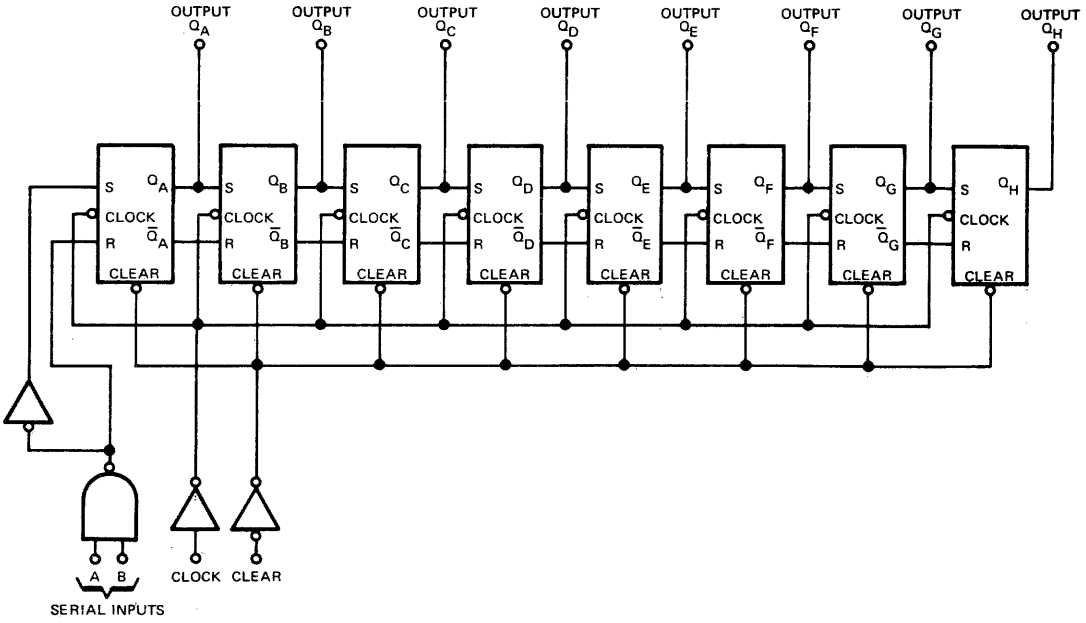
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 5

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	R_L = 800 Ω, See Figure 1	C_L = 15 pF	12	18		MHz
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input		C_L = 15 pF			72	ns
			C_L = 50 pF			84	
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input		C_L = 15 pF	8		54	ns
			C_L = 50 pF	10		60	
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clock input		C_L = 15 pF	10		64	ns
			C_L = 50 pF	10		74	

typical clear, inhibit, shift, clear, and inhibit sequences

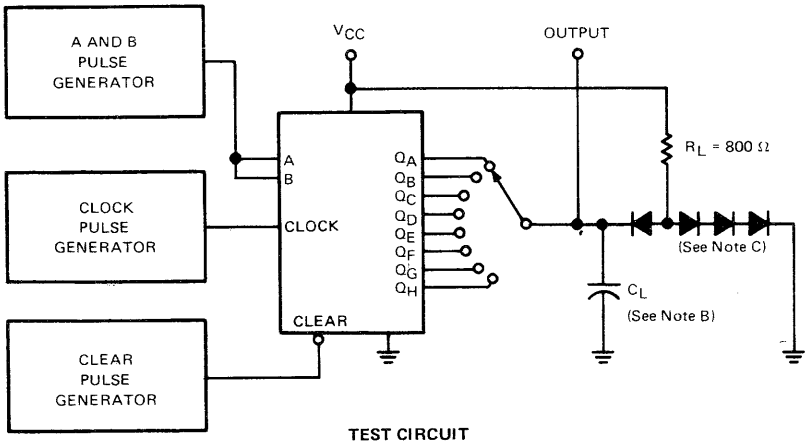


functional block diagram

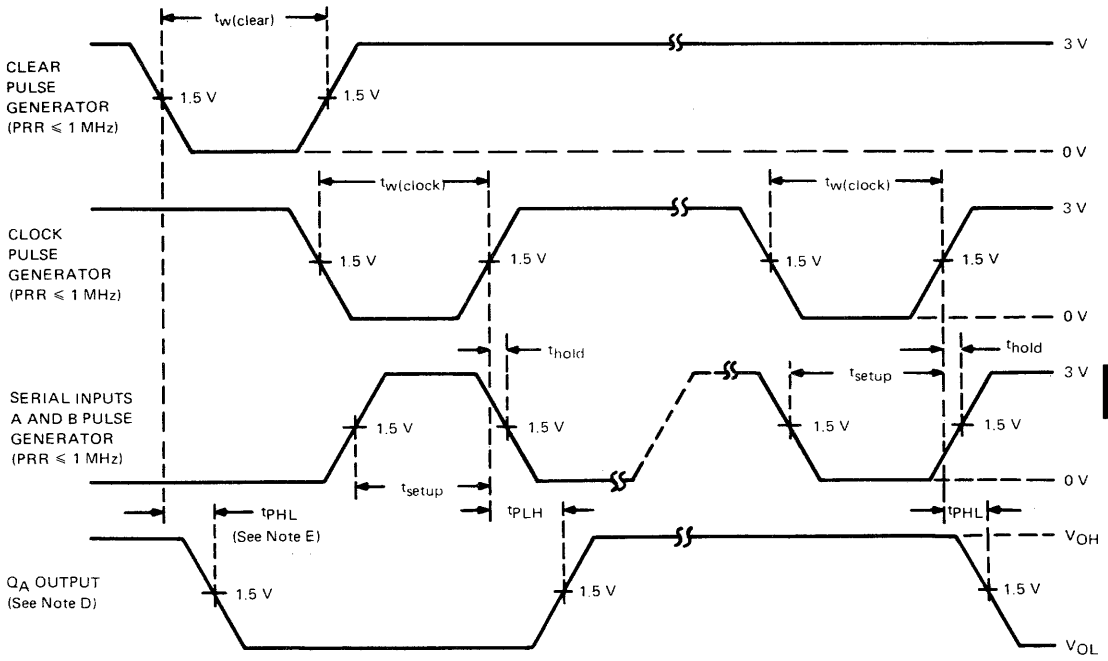


TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916.
D. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
E. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.

FIGURE 1–SWITCHING TIMES

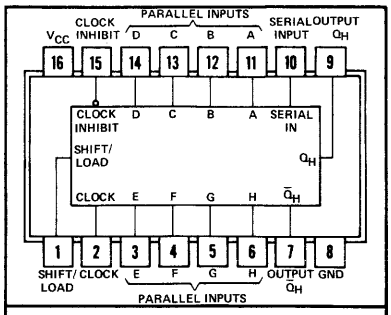
9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54165, SN74165
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

- Typical Maximum Input Clock Frequency . . . 26 MHz
- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see description

†Pin assignments for these circuits are the same for all packages.

description

The SN54165 and SN74165 are 8-bit serial shift registers which shift the data to the right when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. When taken low, data at the parallel inputs are loaded directly into the register independently of the state of the clock.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Power dissipation is typically 210 milliwatts and maximum input clock frequency is typically 26 megahertz. The SN54165 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74165 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54165 Circuits . . . . . −55°C to 125°C
SN74165 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to the shift/load input in conjunction with the clock or clock-inhibit inputs.

recommended operating conditions

		SN54165			SN74165			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$		25			25			ns
Width of load input pulse, $t_{w(load)}$		15			15			ns
Clock-enable setup time, t_{setup} (see Figure 1)		30			30			ns
Parallel input setup time, t_{setup} (see Figure 1)		10			10			ns
Serial input setup time, t_{setup} (see Figure 2)		20			20			ns
Shift setup time, t_{setup} (see Figure 2)		45			45			ns
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54165			SN74165			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MAX, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Load input	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	Load input	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
		Other inputs				−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		42	63		42	63	mA

NOTE 3: With the outputs open, clock inhibit and shift/load at 4.5 V, and a clock pulse applied to the clock input, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

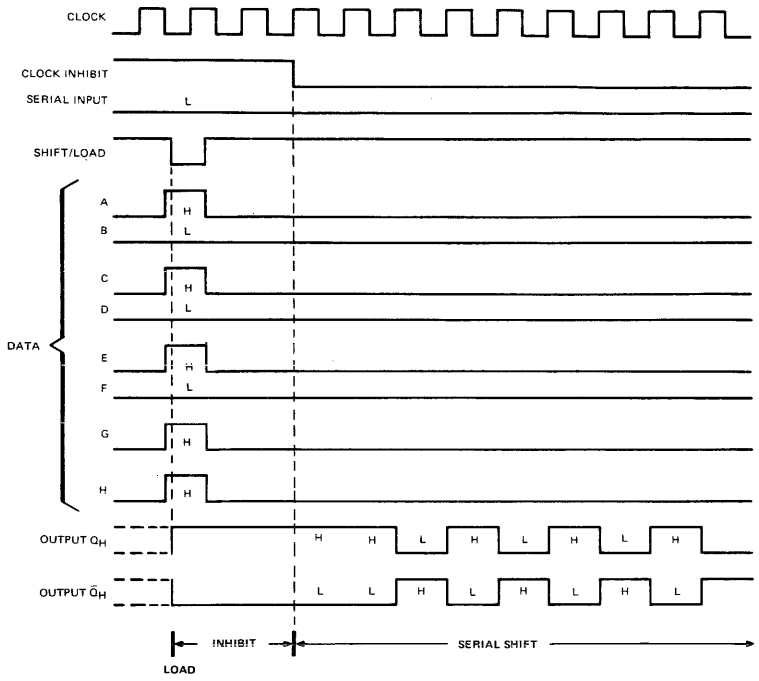
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See figures 1 thru 3	20	26		MHz
t_{PLH}	Load	Any			21	31	ns
t_{PHL}					27	40	
t_{PLH}	Clock	Any			16	24	ns
t_{PHL}					21	31	
t_{PLH}	H	Q_H			11	17	ns
t_{PHL}					24	36	
t_{PLH}	H	$\overline{Q}_H$			18	27	ns
t_{PHL}					18	27	

¶f_{max} ≡ Maximum input count frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

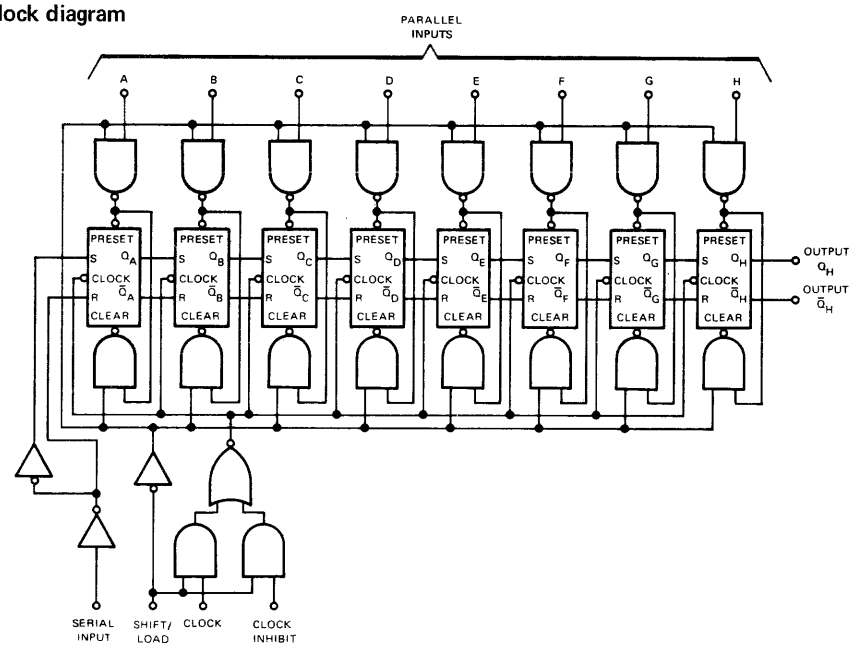
9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

typical shift, load, and inhibit sequences



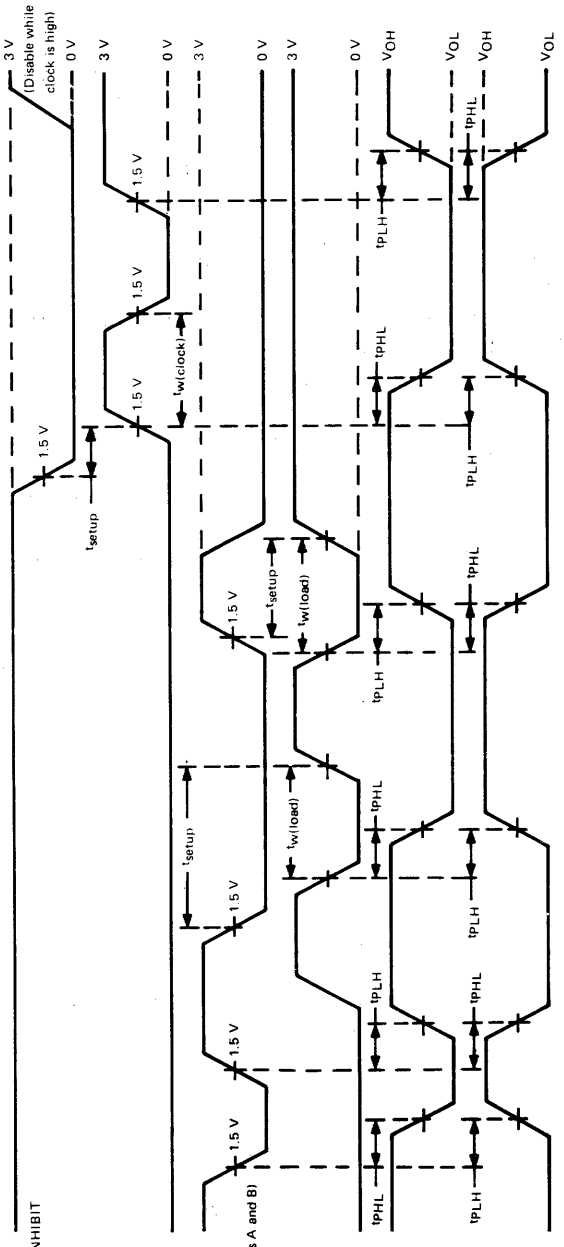
functional block diagram



9

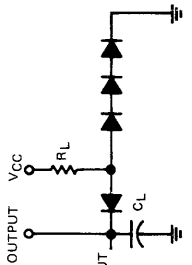
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION



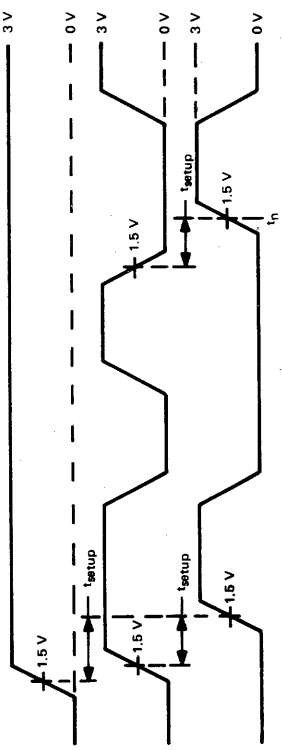
NOTES: A. The remaining six data inputs and the serial input are low.
B. Prior to test, high-level data is loaded into H input.
C. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\ \Omega$. When testing f_{max}, vary clock PRR.

FIGURE 1–VOLTAGE WAVEFORMS



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are IN3064.

FIGURE 3–LOAD CIRCUIT FOR SWITCHING TESTS



NOTES: A. The eight data inputs and the clock-inhibit input are low. Results are monitored at output Q_H at t_{n+7}.
B. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\ \Omega$.

FIGURE 2–VOLTAGE WAVEFORMS

9

070

CIRCUIT TYPES SN54166, SN74166, SN54198, SN74198, SN54199, SN74199
8-BIT SHIFT REGISTERS

description

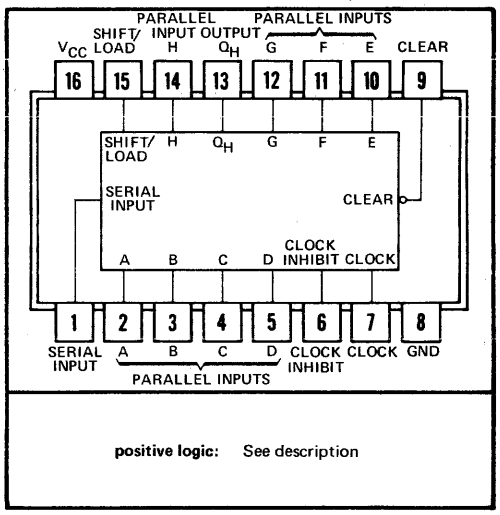
These 8-bit shift registers are compatible with most other TTL, DTL, and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

All Series 54 devices are characterized for operation over the full military temperature range of −55°C to 125°C; all Series 74 devices are characterized for operation from 0°C to 70°C.

SN54166 and SN74166

These parallel-in or serial-in, serial-out shift registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the gate input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock and sets all flip-flops to zero. Average power dissipation per gate is typically 4.7 mW.

SN54166 and SN74166
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See description

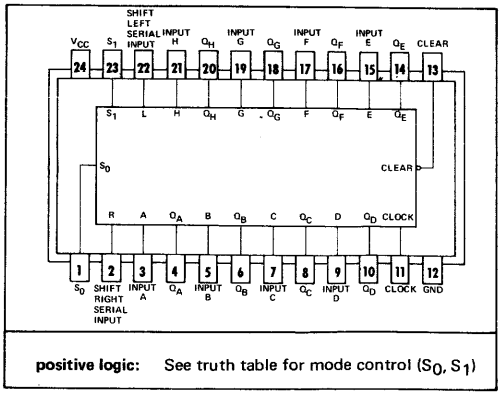
SN54198 and SN74198

The bidirectional registers are designed to incorporate virtually all of the features a system designer may want in a shift register. These circuits contains 87 equivalent gates and feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (Broadside) Load
Shift Right (In the direction Q_A toward Q_H)
Shift Left (In the direction Q_H toward Q_A)
Inhibit Clock (Do nothing)

Synchronous parallel loading is accomplished by applying the eight bits of data and taking both mode control inputs, S_0 and S_1, high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

SN54198 and SN74198
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See truth table for mode control (S_0, S_1)

†Pin assignments for these circuits are the same for all packages.

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SN54198 and SN74198 (continued)

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls should be changed only while the clock input is high.

Average power dissipation per gate is typically 4.15 mW.

SN54198/SN74198
OPERATION OF MODE CONTROL

INPUTS		MODE
S_1	S_0	
L	L	INHIBIT CLOCK
L	H	SHIFT RIGHT
H	L	SHIFT LEFT
H	H	PARALLEL LOAD

SN54199 and SN74199

These synchronous 8-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, a direct overriding clear line, and gated clock inputs. The register has three modes of operation:

Parallel (Broadside) Load
Shift (In the direction Q_A toward Q_H)
Inhibit Clock (Do nothing)

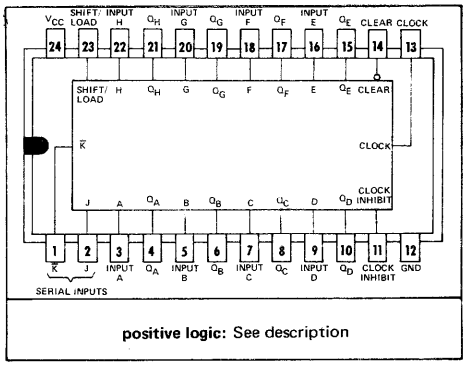
Parallel loading is accomplished by applying the eight bits of data and taking the shift/load control input low when the clock input is not inhibited. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when shift/load is high and the clock input is not inhibited. Serial data for this mode is entered at the J-$\overline{K}$ inputs. See the J-$\overline{K}$ inputs truth table for states required to enter serial data into the first flip-flop.

Both of the clock inputs are identical in function and may be used interchangeably to serve as clock or clock-inhibit inputs. Holding either high inhibits clocking, but when one is held low, a clock input applied to the other input is passed to the eight flip-flops of the register. The clock-inhibit input should be changed to the high level only while the clock input is high.

These shift registers contain the equivalent of 79 TTL gates. Average power dissipation per gate is typically 4.55 mW.

SN54199 and SN74199
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See description

†Pin assignments for these circuits are the same for all packages.

SN54199/SN74199
TRUTH TABLE
J-$\overline{K}$ INPUTS

INPUTS at t_n		OUTPUT t_{n+1}
J	$\overline{K}$	Q_A
L	H	Q_{An}
L	L	L
H	H	H
H	L	$\overline{Q}_{An}$

H = high level, L = low level

NOTES: A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse

9

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range:
SN54166, SN54198, and SN54199 Circuits . . . . . −55°C to 125°C
SN74166, SN74198, and SN74199 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54166 SN54198 SN54199			SN74166 SN74198 SN74199			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input count frequency, f_{count}		0		25	0		25	MHz
Width of clock or clear pulse, t_w (see Figure 1)		20			20			ns
Mode-control setup time, t_{setup}		30			30			ns
Data setup time, t_{setup} (see Figure 1)		20			20			ns
Hold time at any input, t_{hold} (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54166 SN54198 SN54199			SN74166 SN74198 SN74199			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Table Below		72	104		72	116	mA

9

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

TEST CONDITIONS FOR I_{CC}
(ALL OUTPUTS ARE OPEN.)

TYPE	APPLY 4.5 V	FIRST GROUND, THEN APPLY 4.5 V	GROUND
SN54166, SN74166	Serial Input	Clock	All other inputs
SN54198, SN74198	Serial Input, S_0, S_1	Clock	Clear, Inputs A thru H
SN54199, SN74199	J, $\overline{K}$, Inputs A thru H	Clock	Clock Inhibit, Clear, Shift/Load

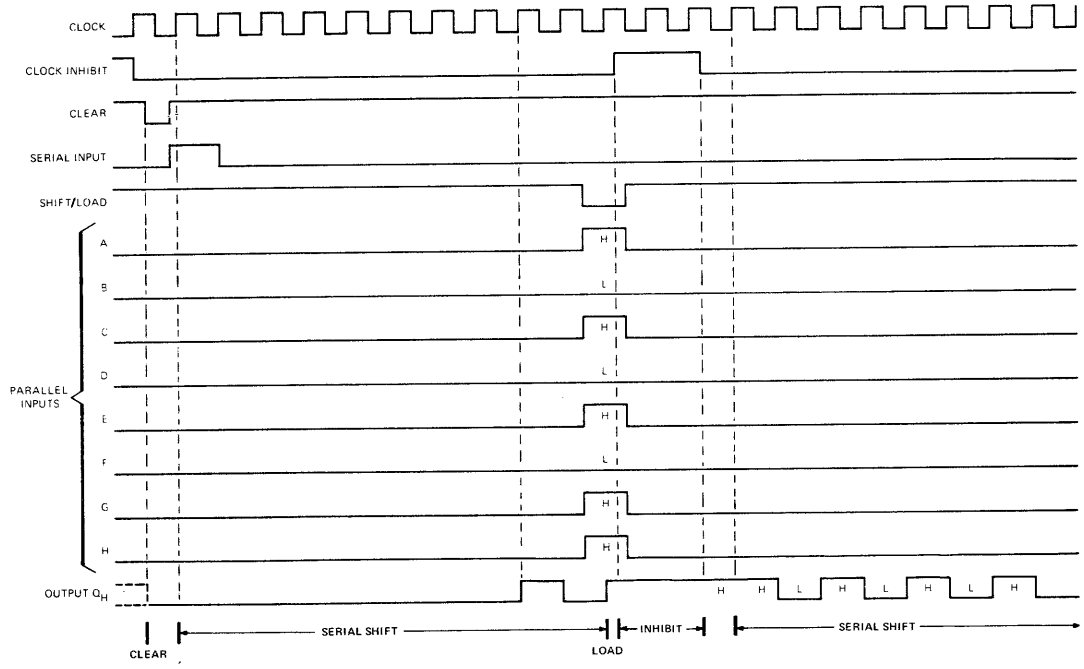
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		8	20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		8	17	26	ns

SN54166, SN74166

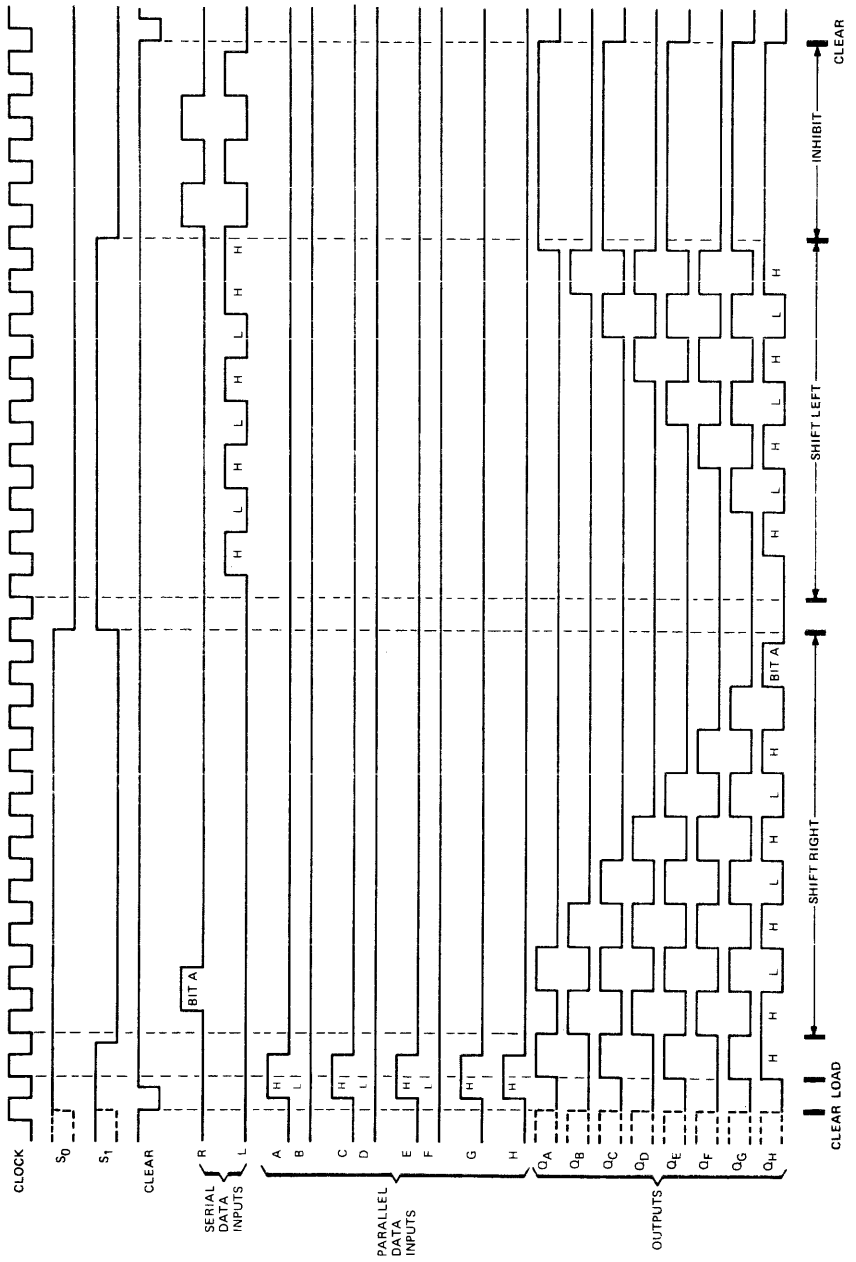
typical clear, shift, load, inhibit, and shift sequences



9

SN54198, SN74198

typical clear, load, right-shift, left-shift, inhibit, and clear sequences

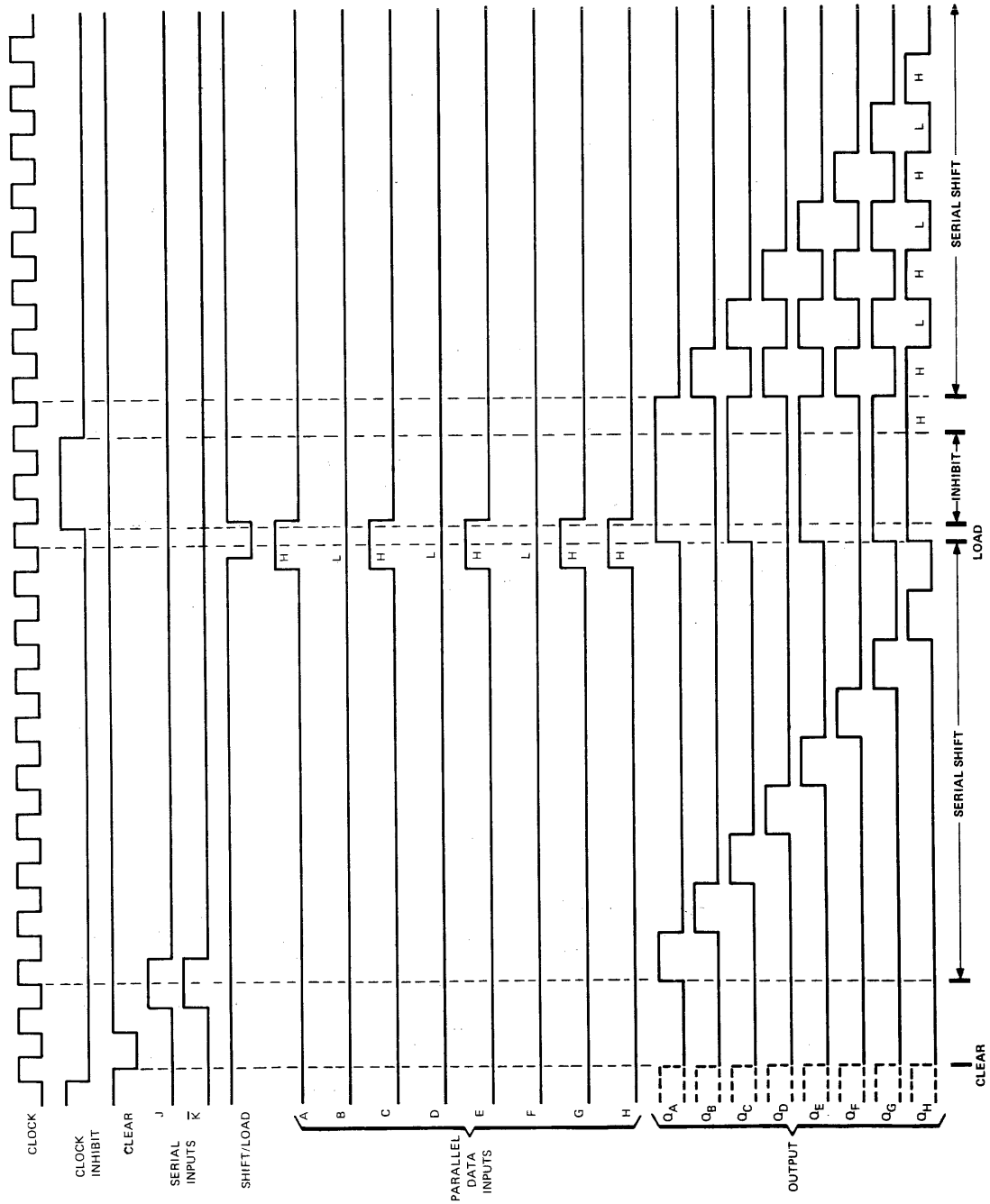


9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SN54199, SN74199

typical clear, shift, load, and inhibit sequences

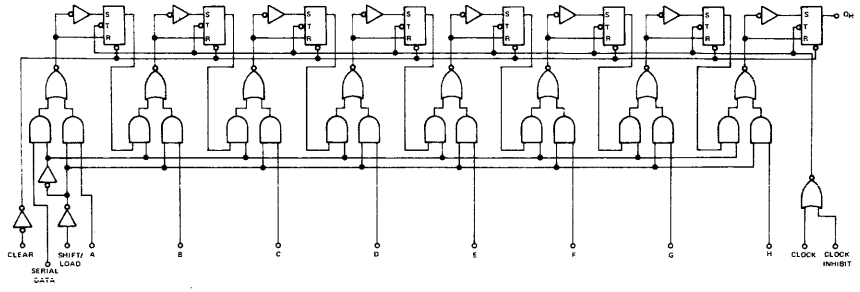


9

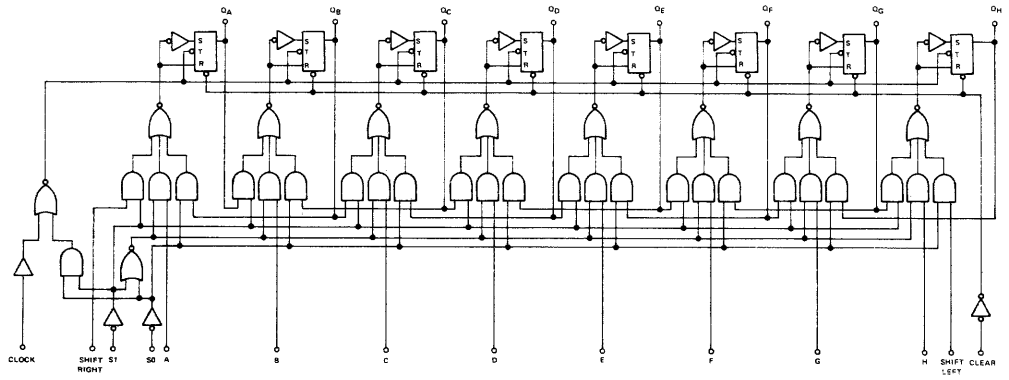
070

functional block diagrams

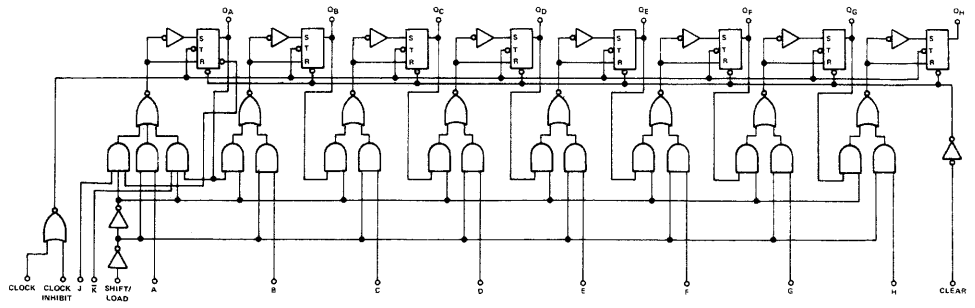
SN54166, SN74166



SN54198, SN74198



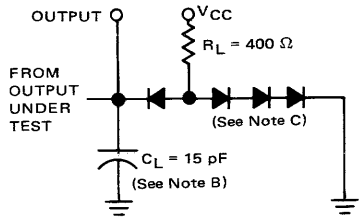
SN54199, SN74199



9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

SN54166, SN74166
TEST TABLE FOR SYNCHRONOUS INPUTS

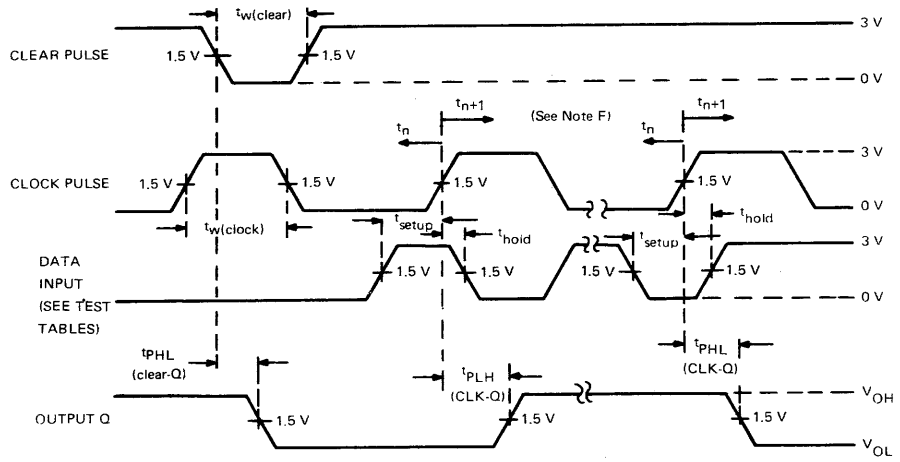
DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTE E)
H	0 V	Q_H at t_{n+1}
Serial Input	4.5 V	Q_H at t_{n+8}

SN54198, SN74198
TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S_1	S_0	OUTPUT TESTED (SEE NOTE E)
A	4.5 V	4.5 V	Q_A at t_{n+1}
B	4.5 V	4.5 V	Q_B at t_{n+1}
C	4.5 V	4.5 V	Q_C at t_{n+1}
D	4.5 V	4.5 V	Q_D at t_{n+1}
E	4.5 V	4.5 V	Q_E at t_{n+1}
F	4.5 V	4.5 V	Q_F at t_{n+1}
G	4.5 V	4.5 V	Q_G at t_{n+1}
H	4.5 V	4.5 V	Q_H at t_{n+1}
L Serial Input	4.5 V	0 V	Q_A at t_{n+8}
R Serial Input	0 V	4.5 V	Q_H at t_{n+8}

SN54199, SN74199
TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTE E)
A	0 V	Q_A at t_{n+1}
B	0 V	Q_B at t_{n+1}
C	0 V	Q_C at t_{n+1}
D	0 V	Q_D at t_{n+1}
E	0 V	Q_E at t_{n+1}
F	0 V	Q_F at t_{n+1}
G	0 V	Q_G at t_{n+1}
H	0 V	Q_H at t_{n+1}
J and $\overline{K}$	4.5 V	Q_H at t_{n+8}



VOLTAGE WAVEFORMS

NOTES: A. The clock pulse has the following characteristics: $t_{w(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq 20$ ns and $t_{hold} = 0$ ns. When testing f_{max}, vary the clock PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. A clear pulse is applied prior to each test.
E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.
F. t_n = bit time before clocking transition
t_{n+1} = bit time after one clocking transition
t_{n+8} = bit time after eight clocking transitions

FIGURE 1

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

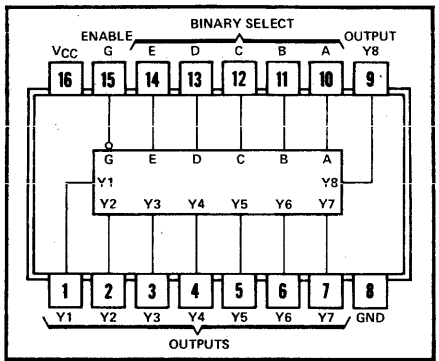
CIRCUIT TYPES SN54184, SN54185A, SN74184, SN74185A
BCD-TO-BINARY AND BINARY-TO-BCD CONVERTERS

SN54184, SN74184 BCD-TO-BINARY CONVERTERS
SN54185A, SN74185A BINARY-TO-BCD CONVERTERS

description

These monolithic converters are derived from the custom MSI 256-bit read-only memories SN5488 and SN7488. Emitter connections are made to provide direct read-out of converted codes at outputs Y8 through Y1 as shown in the truth tables. These converters demonstrate the versatility of a read-only memory in that an unlimited number of reference tables or conversion tables may be built into a system using economical, customized read-only memories. Both of these converters comprehend that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter as illustrated in the typical applications. This means that a 6-bit converter is produced in each case. Both devices are cascadable to N bits.

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



positive logic: See Truth Table

†Pin assignments for these circuits are the same for all packages.

An overriding enable input is provided on each converter which, when taken high inhibits the function, causing all outputs to go high. For this reason, and to minimize power consumption, unused outputs Y7 and Y8 of the SN54185A and SN54185A, and all "don't care" conditions of the SN54184 and SN74184 are programmed high. The outputs are of the open-collector type.

9

The SN54184 and SN54185A are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74184 and SN74185A are characterized for operation from 0°C to 70°C.

SN54184 and SN74184 BCD-to-binary converters

The 6-bit BCD-to-binary function of the SN54184 and SN74184 is analogous to the algorithm:

a. Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.
b. Shift right, examine, and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.

TABLE I
SN54184, SN74184
PACKAGE COUNT AND DELAY TIMES
FOR BCD-TO-BINARY CONVERSION

INPUT (DECADES)	PACKAGES REQUIRED	TOTAL DELAY TIMES (ns)	
		TYP	MAX
2	2	50	80
3	6	125	200
4	11	175	280
5	19	250	400
6	28	325	520

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SN54185A and SN74185A binary-to-BCD converters

The function performed by these 6-bit binary-to-BCD converters is analogous to the algorithm:

a. Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.
b. Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.
c. Repeat step b until the least-significant binary bit is in the least-significant BCD location.

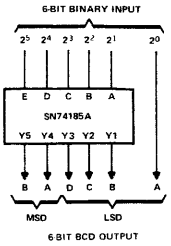
TABLE II

SN54185A, SN74185A

PACKAGE COUNT AND DELAY TIMES FOR BINARY-TO-BCD CONVERSION

INPUT (BITS)	PACKAGES REQUIRED	TOTAL DELAY TIME (ns)	
		TYP	MAX
4 to 6	1	25	40
7 or 8	3	50	80
9	4	75	120
10	6	100	160
11	7	125	200
12	8	125	200
13	10	150	240
14	12	175	280
15	14	175	280
16	16	200	320
17	19	225	360
18	21	225	360
19	24	250	400
20	27	275	440

6-BIT CONVERTER



TRUTH TABLE

BINARY WORDS	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0 - 1	L	L	L	L	L	L	H	H	L	L	L	L	L	L
2 - 3	L	L	L	L	H	L	H	H	L	L	L	L	L	H
4 - 5	L	L	L	H	L	L	H	H	L	L	L	L	H	L
6 - 7	L	L	L	H	H	L	H	H	L	L	L	L	H	H
8 - 9	L	L	H	L	L	L	H	H	L	L	L	H	L	L
10 - 11	L	L	H	L	H	L	H	H	L	L	H	L	L	L
12 - 13	L	L	H	H	L	L	H	H	L	L	H	L	L	H
14 - 15	L	L	H	H	H	L	H	H	L	L	H	L	H	L
16 - 17	L	H	L	L	L	L	H	H	L	L	H	L	H	H
18 - 19	L	H	L	L	H	L	H	H	L	L	H	H	L	L
20 - 21	L	H	L	H	L	L	H	H	L	H	L	L	L	L
22 - 23	L	H	L	H	H	L	H	H	L	H	L	L	L	H
24 - 25	L	H	H	L	L	L	H	H	L	H	L	L	H	L
26 - 27	L	H	H	L	H	L	H	H	L	H	L	L	H	H
28 - 29	L	H	H	H	L	L	H	H	L	H	L	H	L	L
30 - 31	L	H	H	H	H	L	H	H	L	H	H	L	L	L
32 - 33	H	L	L	L	L	L	H	H	L	H	H	L	L	H
34 - 35	H	L	L	L	H	L	H	H	L	H	H	L	H	L
36 - 37	H	L	L	H	L	L	H	H	L	H	H	L	H	H
38 - 39	H	L	L	H	H	L	H	H	L	H	H	H	L	L
40 - 41	H	L	H	L	L	L	H	H	H	L	L	L	L	L
42 - 43	H	L	H	L	H	L	H	H	H	L	L	L	L	H
44 - 45	H	L	H	H	L	L	H	H	H	L	L	L	H	L
46 - 47	H	L	H	H	H	L	H	H	H	L	L	L	H	H
48 - 49	H	H	L	L	L	L	H	H	H	L	L	H	L	L
50 - 51	H	H	L	L	H	L	H	H	H	L	H	L	L	L
52 - 53	H	H	L	H	L	L	H	H	H	L	H	L	L	H
54 - 55	H	H	L	H	H	L	H	H	H	L	H	L	H	L
56 - 57	H	H	H	L	L	L	H	H	H	L	H	L	H	H
58 - 59	H	H	H	L	H	L	H	H	H	L	H	H	L	L
60 - 61	H	H	H	H	L	L	H	H	H	H	L	L	L	L
62 - 63	H	H	H	H	H	L	H	H	H	H	L	L	L	H
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54184, SN54185A . . . . . −55°C to 125°C
SN74184, SN74185A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

	SN54184, SN54185A			SN74184, SN74185A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55	25	125	0	25	70	°C

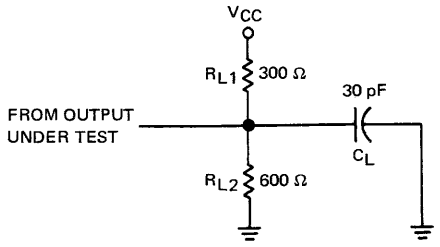
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	V_{OH} = 5.5 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 12 mA			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.4 V			−1	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX			50		mA
I_{CCL}	Supply current, all programmed outputs low				62	104	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from enable G	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from enable G			22	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from binary select			25	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output from binary select			20	32	ns



C_L includes probe and jig capacitance.

LOAD CIRCUIT

9

TYPICAL APPLICATION DATA
SN54184, SN74184

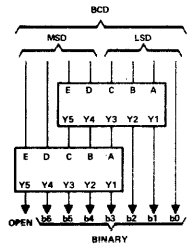


FIGURE 1—BCD-TO-BINARY CONVERTER FOR TWO BCD DECADES

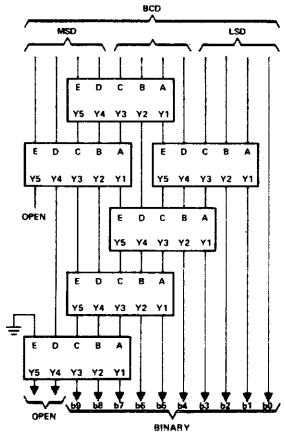


FIGURE 2—BCD-TO-BINARY CONVERTER FOR THREE BCD DECADES

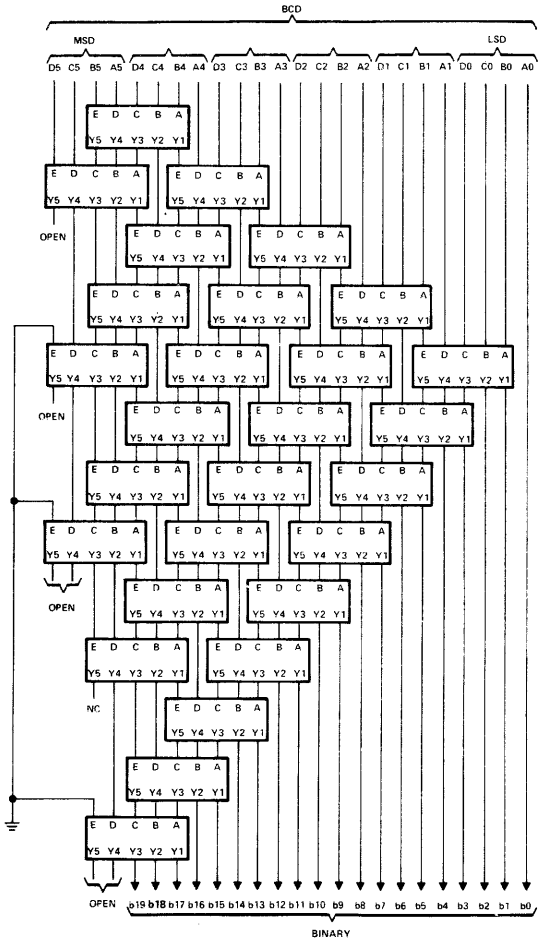


FIGURE 3—BCD-TO-BINARY CONVERTER FOR SIX BCD DECADES

MSD—most significant decade
LSD—least significant decade
Each rectangle represents an SN54184 or SN74184.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATION DATA
SN54185A, SN74185A

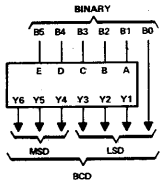


FIGURE 4–6-BIT BINARY-TO-BCD CONVERTER

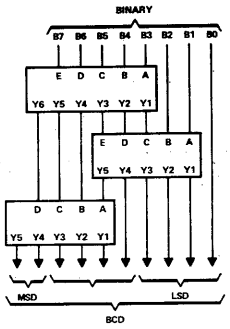


FIGURE 5–8-BIT BINARY-TO-BCD CONVERTER

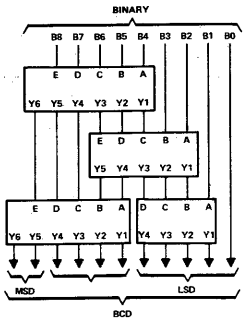


FIGURE 6–9-BIT BINARY-TO-BCD CONVERTER

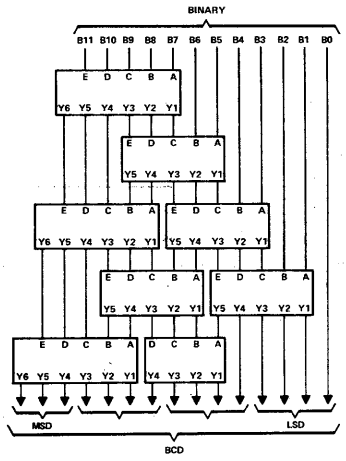


FIGURE 7–12-BIT BINARY-TO-BCD CONVERTER

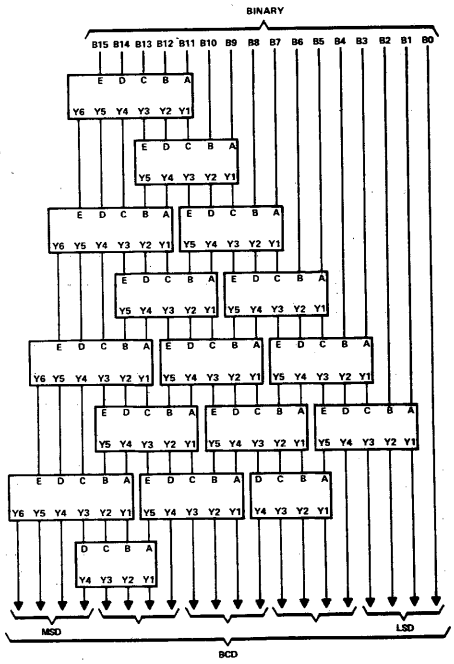


FIGURE 8–16-BIT BINARY-TO-BCD CONVERTER

MSD—Most significant decade
LSD—Least significant decade
Each rectangle represents an SN54185A or an SN74185A.

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5442, SN5443, SN5444, SN7442, SN7443, SN7444
4-LINE-TO-10-LINE DECODERS (1-OF-10)

- BCD-to-Decimal
- Excess-3-to-Decimal
- Excess-3-Gray-to-Decimal

Also for applications as

- 4-Line-to-16-Line Decoders
- 3-Line to 8-Line Decoders

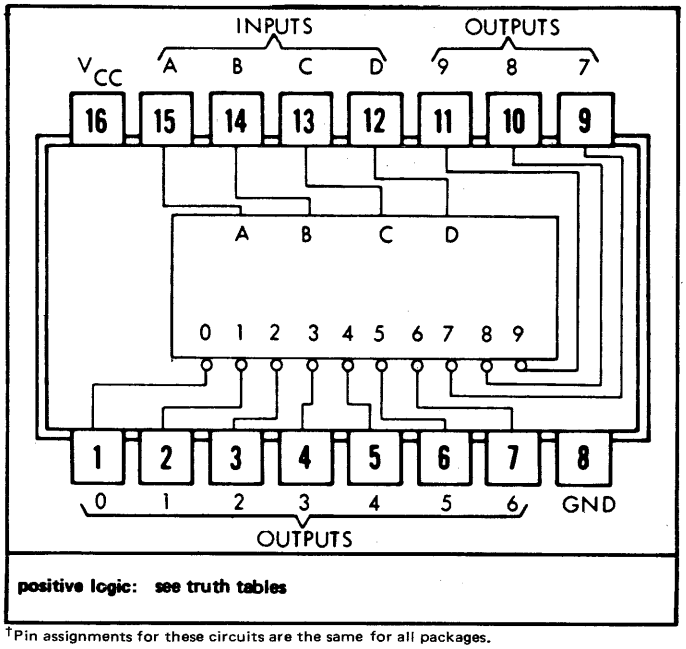
- featuring diode-clamped inputs

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The SN5442/SN7442 BCD-to-decimal, SN5443/SN7443 excess-3-to-decimal, and SN5444/SN7444 excess-3-gray-to-decimal decoders feature familiar transistor-transistor-logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt and power dissipation is typically 140 milliwatts. Full fan-out of 10 is available at all outputs.

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see truth tables

†Pin assignments for these circuits are the same for all packages.

SN5442/SN7442 BCD INPUT				SN5443/SN7443 EXCESS 3 INPUT				SN5444/SN7444 EXCESS 3 GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	0	0	1	0	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	0	1	1	1	0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	0	0	0	1	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	0	0	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Note 1) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5442, SN5443, SN5444 Circuits . . . . . −55°C to 125°C
SN7442, SN7443, SN7444 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5442, SN5443, SN5444 Circuits	4.5	5	5.5	V
SN7442, SN7443, SN7444 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output (N)			10	

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN5442, SN5443, SN5444	−20		−55	mA
				SN7442, SN7443, SN7444	−18		−55	mA
I_{CC}	Supply current	4	V_{CC} = MAX	SN5442, SN5443, SN5444		28	41	mA
				SN7442, SN7443, SN7444		28	56	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

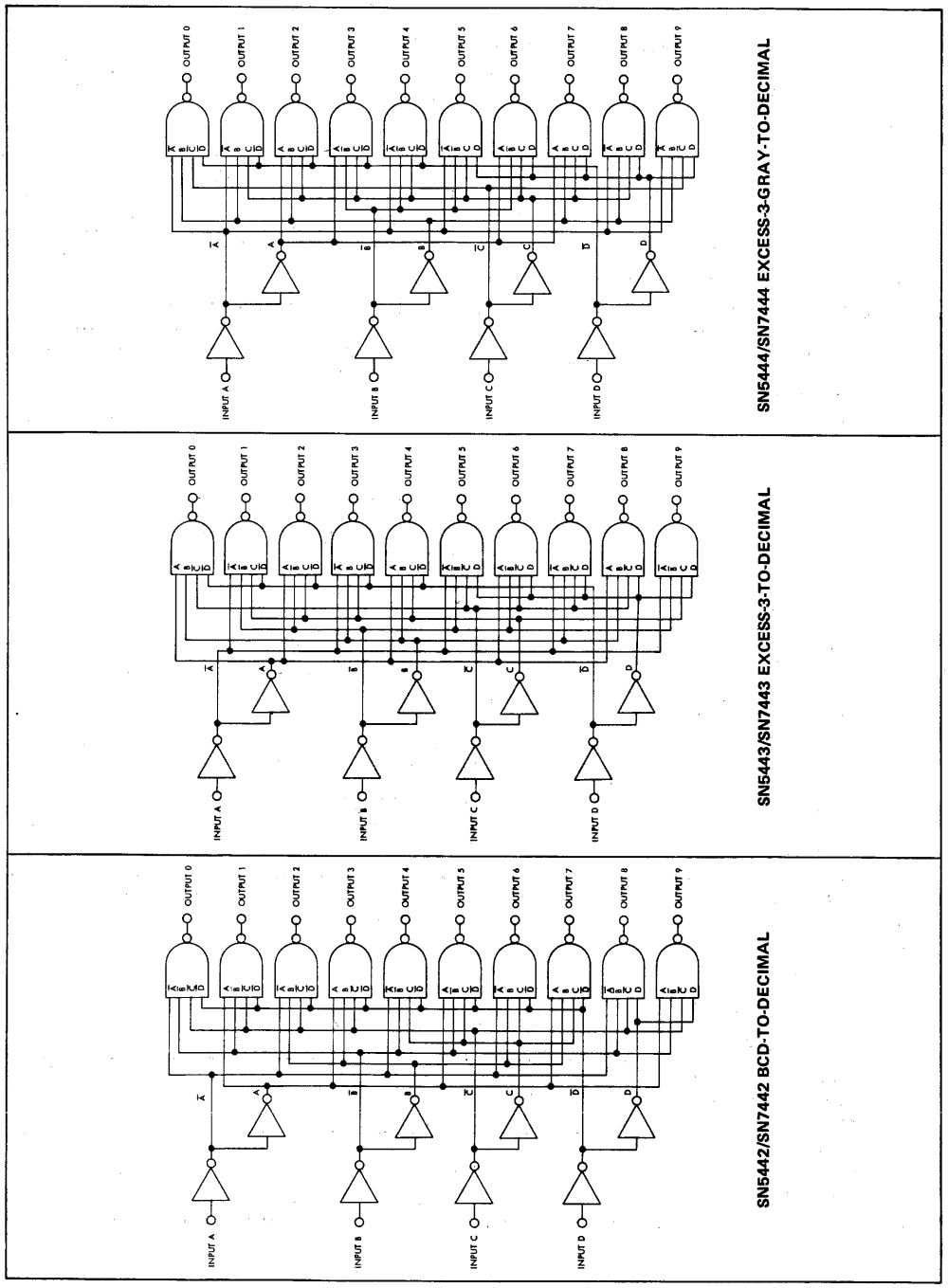
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level through two logic levels	6	C_L = 15 pF, R_L = 400 Ω	10	22	30	ns
t_{pd0}	Propagation delay time to logical 0 level through three logic levels	6	C_L = 15 pF, R_L = 400 Ω		23	35	ns
t_{pd1}	Propagation delay time to logical 1 level through two logic levels	6	C_L = 15 pF, R_L = 400 Ω	10	17	25	ns
t_{pd1}	Propagation delay time to logical 1 level through three logic levels	6	C_L = 15 pF, R_L = 400 Ω		26	35	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

9

CIRCUIT TYPES SN5442, SN5443, SN5444, SN7442, SN7443, SN7444
4-LINE-TO-10-LINE DECODERS (1-OF-10)

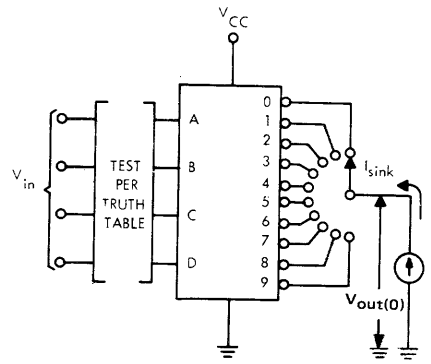
functional block diagrams



9

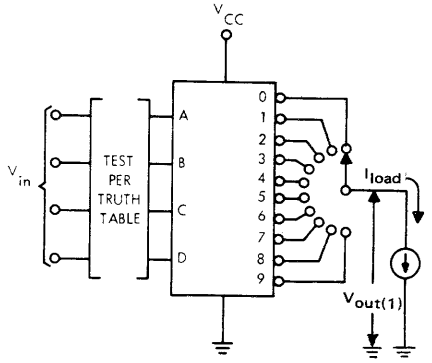
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



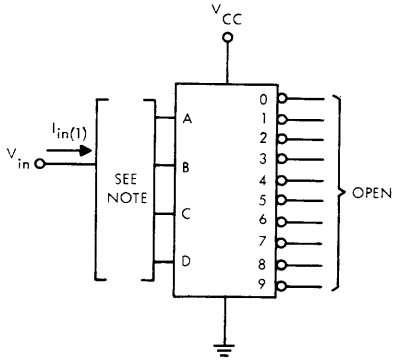
1. Each output is tested separately.

FIGURE 1



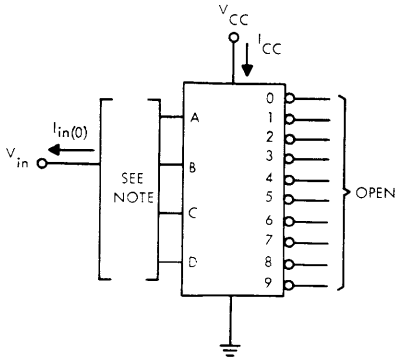
1. Each output is tested separately.

FIGURE 2



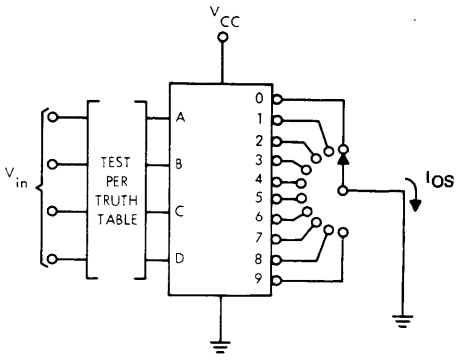
1. Each input is tested separately.

FIGURE 3



1. When testing $I_{in(0)}$ each input is tested separately.
2. When testing I_{CC} all inputs are grounded and outputs are open.

FIGURE 4



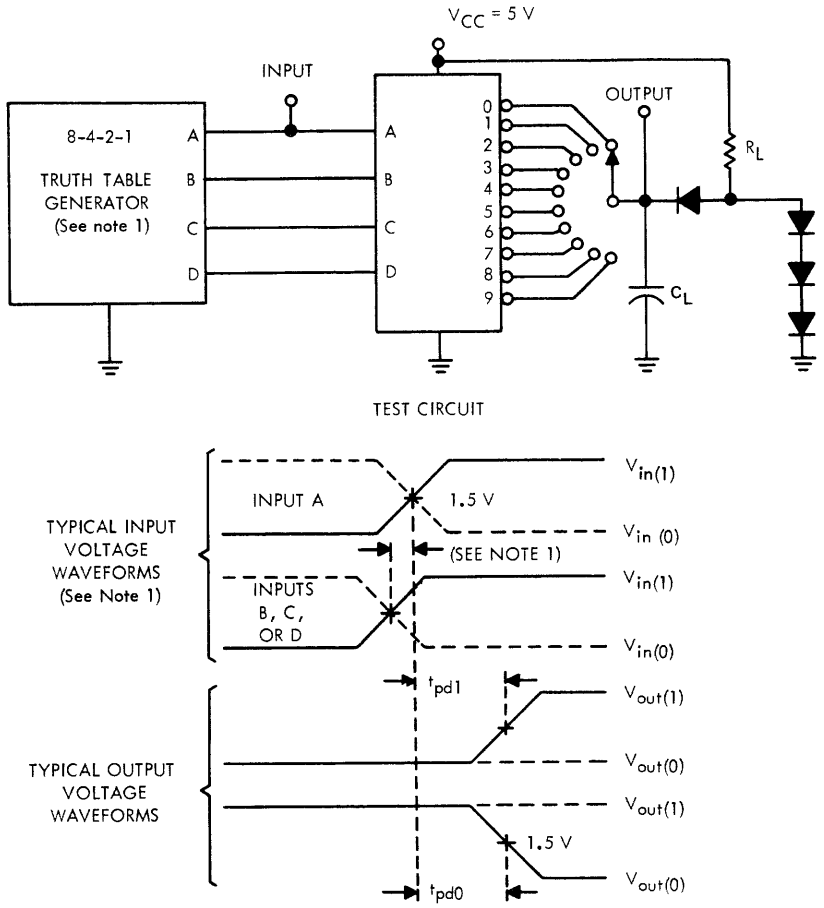
1. Each output is tested separately.

FIGURE 5

†Arrows indicate actual direction of current flow

9

switching characteristics



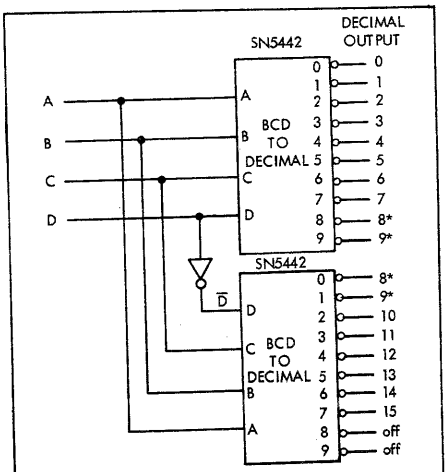
NOTES: 1. The truth table generator has the following characteristics: $V_{out(1)} \geq 2.4$ V, $V_{out(0)} \leq 0.4$ V, t_r and $t_f < 10$ ns, and PRR = 1 MHz. Input B, C, and D transitions occur simultaneously with or prior to input A transistions.
2. C_L includes probe and jig capacitance.
3. All diodes are 1N3064.

FIGURE 6–SWITCHING TIMES

TYPICAL APPLICATIONS

decoding binary-to-decimal with SN5442/SN7442,

Figure A demonstrates a method for utilizing two SN5442/SN7442 decoders to perform 4-wire to 16-wire (1-of-16) decoding. Inputs A, B, and C of the two decoders are paralleled, D is applied to one decoder, and $\overline{D}$ is applied to the other as shown in figure A. Decimal equivalents are available as indicated. Note that decimal 8 and 9 are available from both decoders.



*These decimal outputs are available from both decoders.

FIGURE A

decoding 3-wire binary-to-octal

This application demonstrates a method for decoding 3-wire binary-to-octal using the SN5442/SN7442. See figure B. The binary code ABC is applied to the A, B, and C inputs and the D input is used as a strobe. When the strobe is taken to a logical 0 the octal data may be taken from outputs 0 through 7. Note that decimal outputs 8 and 9 are not used. See BCD truth table.

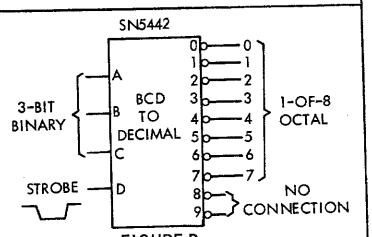


FIGURE B

This application demonstrates a method for decoding 3-wire binary-to-octal using the SN5444/SN7444. See figure C. The binary code ABC is applied to the A, B, and D inputs respectively and the C input is used as a strobe. When the strobe is taken to a logical 1 the octal data (as identified in figure C) may be taken from outputs 1 through 8. Note that outputs 0 and 9 are not used.

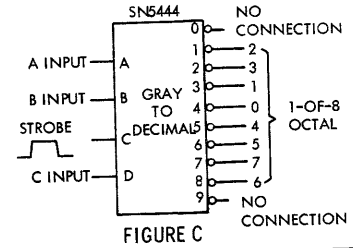


FIGURE C

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54L42, SN54L43, SN54L44, SN74L42, SN74L43, SN74L44 4-LINE-TO-10-LINE DECODERS (1-OF-10)

SN54L42, SN74L42 . . . BCD-TO-DECIMAL

SN54L43, SN74L43 . . . EXCESS-3-TO-DECIMAL

SN54L44, SN74L44 . . . EXCESS-3-GRAY-TO-DECIMAL

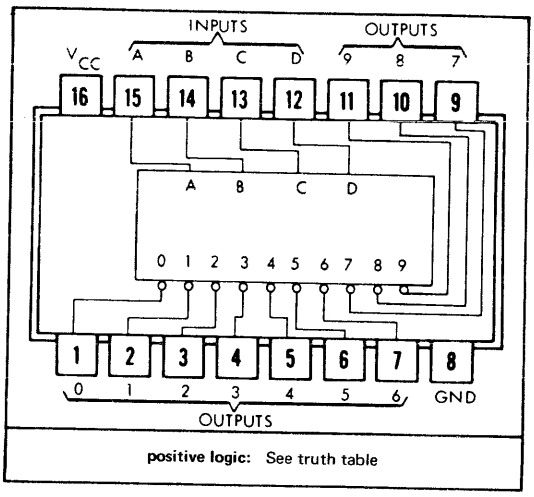
- Also for Applications as
  - 4-Line-to-16-Line Decoders
  - 3-Line-to-8-Line Decoders
- Diode-Clamped Inputs

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The SN54L42/SN74L42 BCD-to-decimal, SN54L43/SN74L43 excess-3-to-decimal, and SN54L44/SN74L44 excess-3-gray-to-decimal decoders feature familiar transistor-transistor logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt and power dissipation is typically 70 milliwatts. The diode-clamped inputs represent only one-half of one normalized Series 54/74 load, or approximately five Series 54L/74L gate loads at a low logic level, or two Series 54L/74L gate loads at a high logic level.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See truth table

TRUTH TABLE

SN54L42/SN74L42 BCD INPUT				SN54L43/SN74L43 EXCESS-3-INPUT				SN54L44/SN74L44 EXCESS-3-GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	L	L	L	H	H	L	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	H	L	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	L	L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
H	H	H	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54L42, SN54L43, SN54L44 Circuits . . . . . −55°C to 125°C
SN74L42, SN74L43, SN74L44 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54L42, SN54L43, SN54L44			SN74L42, SN74L43, SN74L44			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	Series 54L/74L gates				40			40	
	Series 54L/74L inputs with 8-kΩ base resistors¶	High logic level			20			20	
		Low logic level			10			10	
Operating free-air temperature, T_A			−55		125	0		70	°C

¶ This applies to all inputs of all the circuit types on this data sheet.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2		V
V_{IL}	Low-level input voltage	1 and 2				0.8	V
V_I	Input clamp voltage	3	V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.4		V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA			0.4	V
I_I	Input current at maximum input voltage	3	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	3	V_{CC} = MAX, V_I = 2.4 V			20	μA
I_{IL}	Low-level input current	3	V_{CC} = MAX, V_I = 0.4 V			−0.8	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX		−9	−28	mA
I_{CC}	Supply current	5	V_{CC} = MAX	SN54L42, SN54L43, SN54L44		22	mA
				SN74L42, SN74L43, SN74L44		28	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

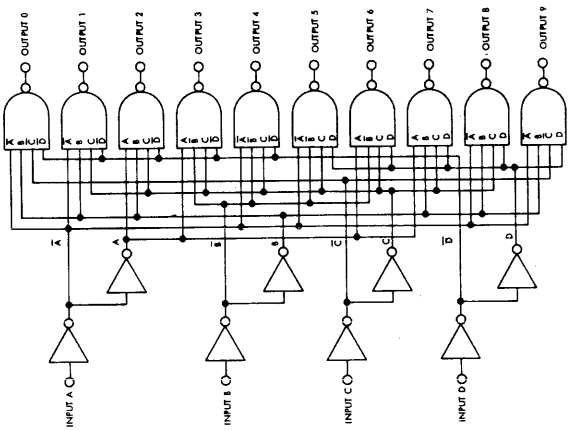
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic	6	C_L = 15 pF, R_L = 400 Ω	10	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic				70	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic			10	50	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic				70	ns

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions for the applicable device type.

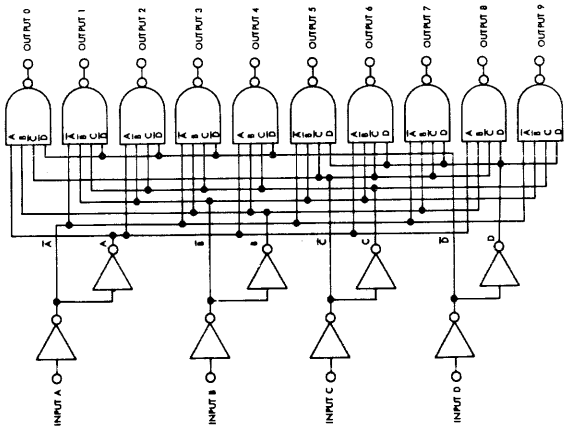
§ Not more than one output should be shorted at a time.

9

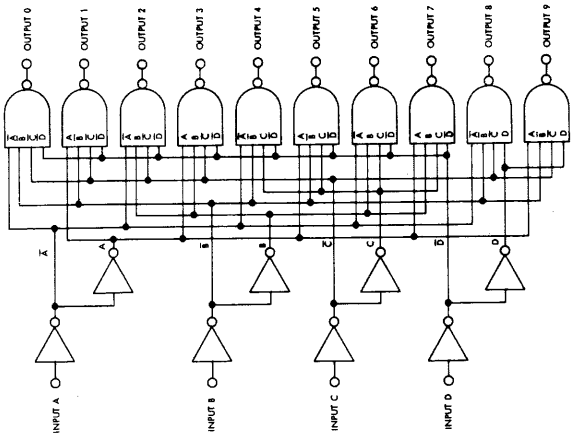
functional block diagrams



SN54L44/SN74L44 EXCESS-3-GRAY-TO-DECIMAL



SN54L43/SN74L43 EXCESS-3-TO-DECIMAL



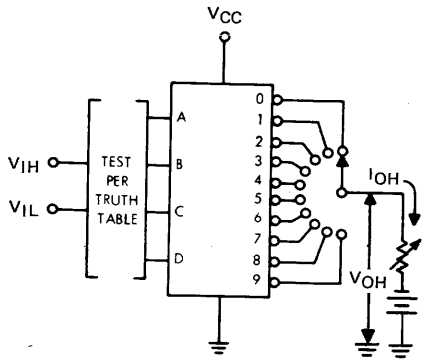
SN54L42/SN74L42 BCD-TO-DECIMAL

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

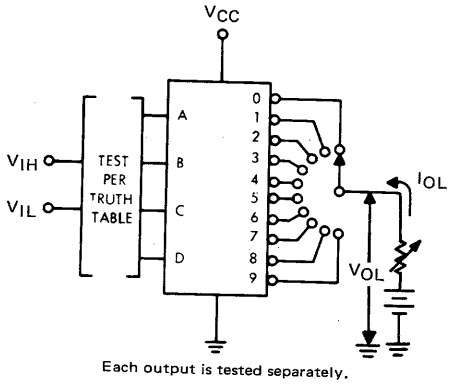
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



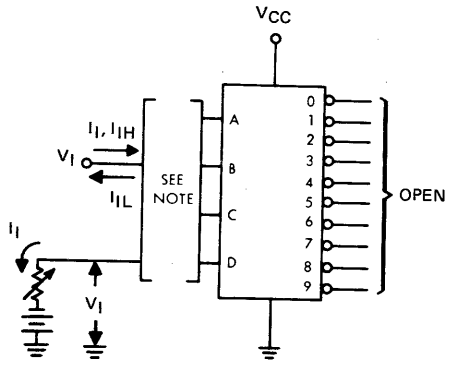
Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



Each output is tested separately.

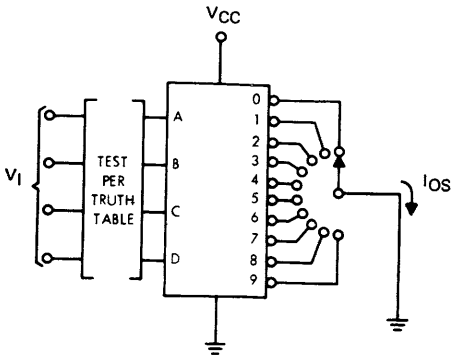
FIGURE 2–V_{IH}, V_{IL}, V_{OL}



Each input is tested separately for V_I, I_I, I_{IH}, and I_{IL}. Inputs not under test are grounded.

FIGURE 3–V_I, I_I, I_{IH}, I_{IL}

9



Each output is tested separately.

FIGURE 4–I_{OS}

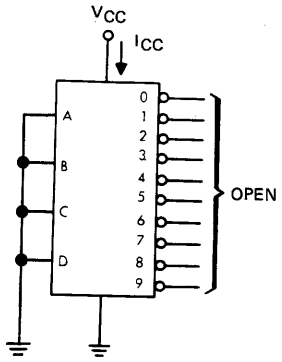
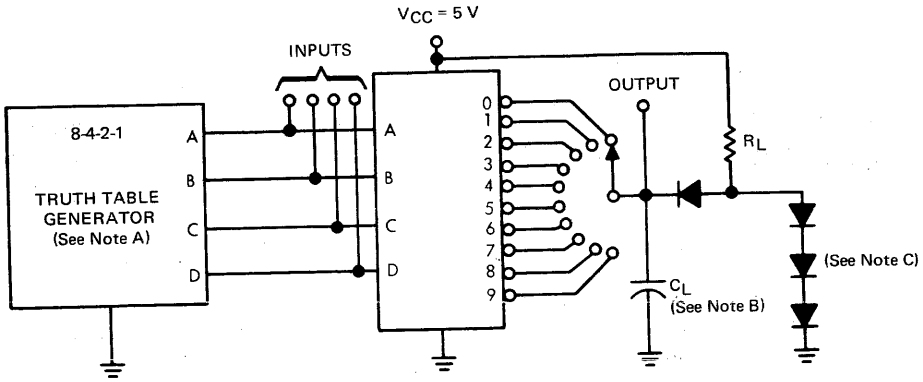


FIGURE 5–I_{CC}

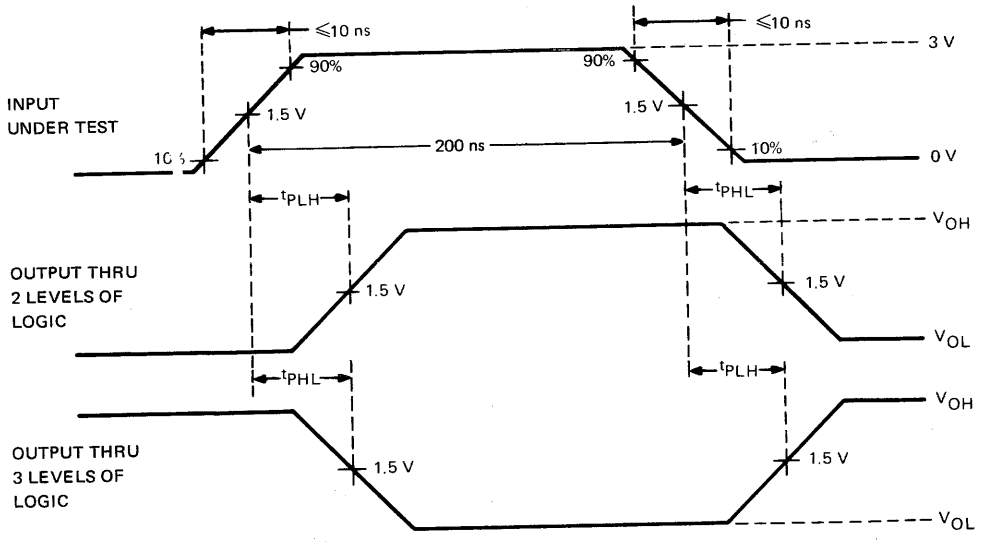
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The truth table generator has the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$. Transition of the input under test must occur simultaneously with or following the transition of the other inputs.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N914.

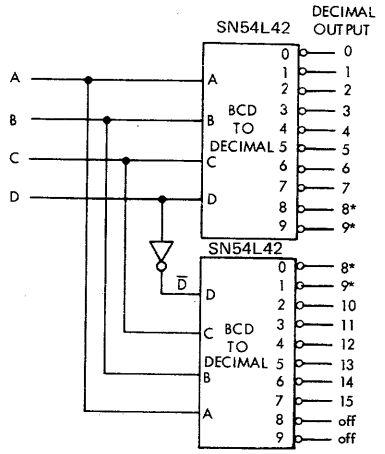
FIGURE 6–SWITCHING TIMES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATIONS

decoding binary-to-decimal with SN54L42/SN74L42

Figure A demonstrates a method for utilizing two SN54L42/SN74L42 decoders to perform 4-wire-to-16-wire (1-of-16) decoding. Inputs A, B, and C of the two decoders are paralleled, D is applied to one decoder, and $\overline{D}$ is applied to the other. Decimal equivalents are available as indicated. Note that decimal 8 and 9 are available from both decoders.



*These decimal outputs are available from both decoders.

FIGURE A

decoding 3-wire binary-to-octal

Figure B demonstrates a method for decoding 3-wire binary-to-octal using the SN54L42/SN74L42. The binary code ABC is applied to the A, B, and C inputs and the D input is used as a strobe. When the strobe is taken to a low level, the octal data may be taken from outputs 0 through 7. Note that decimal outputs 8 and 9 are not used. See BCD truth table.

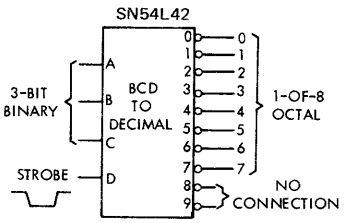


FIGURE B

Figure C demonstrates a method for decoding 3-wire binary-to-octal using the SN54L44/SN74L44. The binary code ABC is applied to the A, B, and D inputs, respectively, and the C input is used as a strobe. When the strobe is taken to a high level, the octal data (as identified in figure C) may be taken from outputs 1 through 8. Note that outputs 0 and 9 are not used.

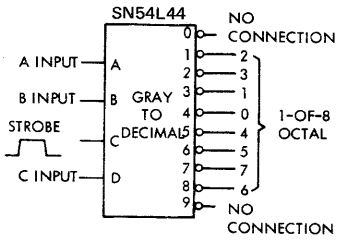


FIGURE C

9

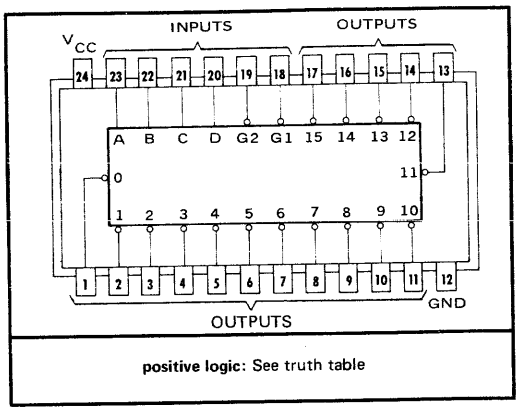
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54154, SN74154
4-LINE-TO-16-LINE DECODERS/DEMULTIPLEXERS

FOR APPLICATIONS IN COMMUNICATIONS EQUIPMENT,
COMPUTERS, AND ELECTRONIC INSTRUMENTATION

- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical average propagation delay times:
  23 ns through 3 levels of logic
  19 ns from strobe input
- Typical power dissipation . . . 170 mW
- Fully compatible with most TTL, DTL, and MSI circuits

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See truth table

†Pin assignments for these circuits are the same for all packages.

description

Each of these monolithic, 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high.

9

These circuits are fully compatible for use with most other TTL and DTL circuits. Input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized Series 54/74 load. A fan-out to 10 normalized Series 54/74 loads in the low-level state and 20 in the high-level state is available from each of the sixteen outputs. Typical power dissipation is 170 mW.

The SN54154 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74154 is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

logic

TRUTH TABLE

INPUTS						OUTPUTS														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high, L = low, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54154 Circuits . . . . . −55°C to 125°C
SN74154 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

9

recommended operating conditions

		SN54154			SN74154			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_{IH}	High-level input current (each input)	3	V_{CC} = MAX, V_I = 2.4 V				40	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (each input)	3	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX	SN54154	−20		−55	mA
				SN74154	−18		−57	
I_{CC}	Supply current	5	V_{CC} = MAX	SN54154		34	49	mA
				SN74154		34	56	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

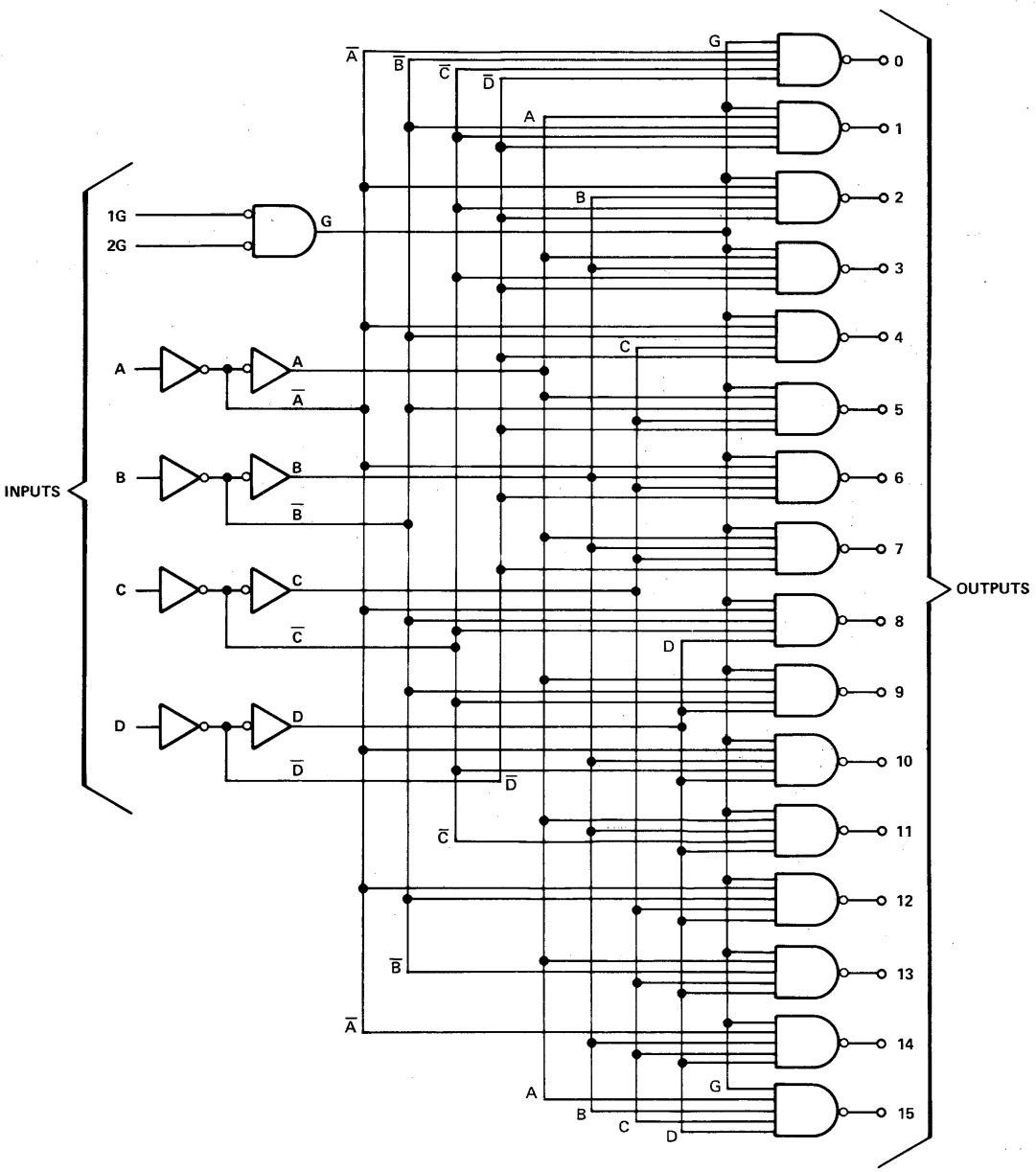
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic	6	C_L = 15 pF, R_L = 400 Ω		24	36	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic				22	33	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from either strobe input				20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from either strobe input				18	27	ns

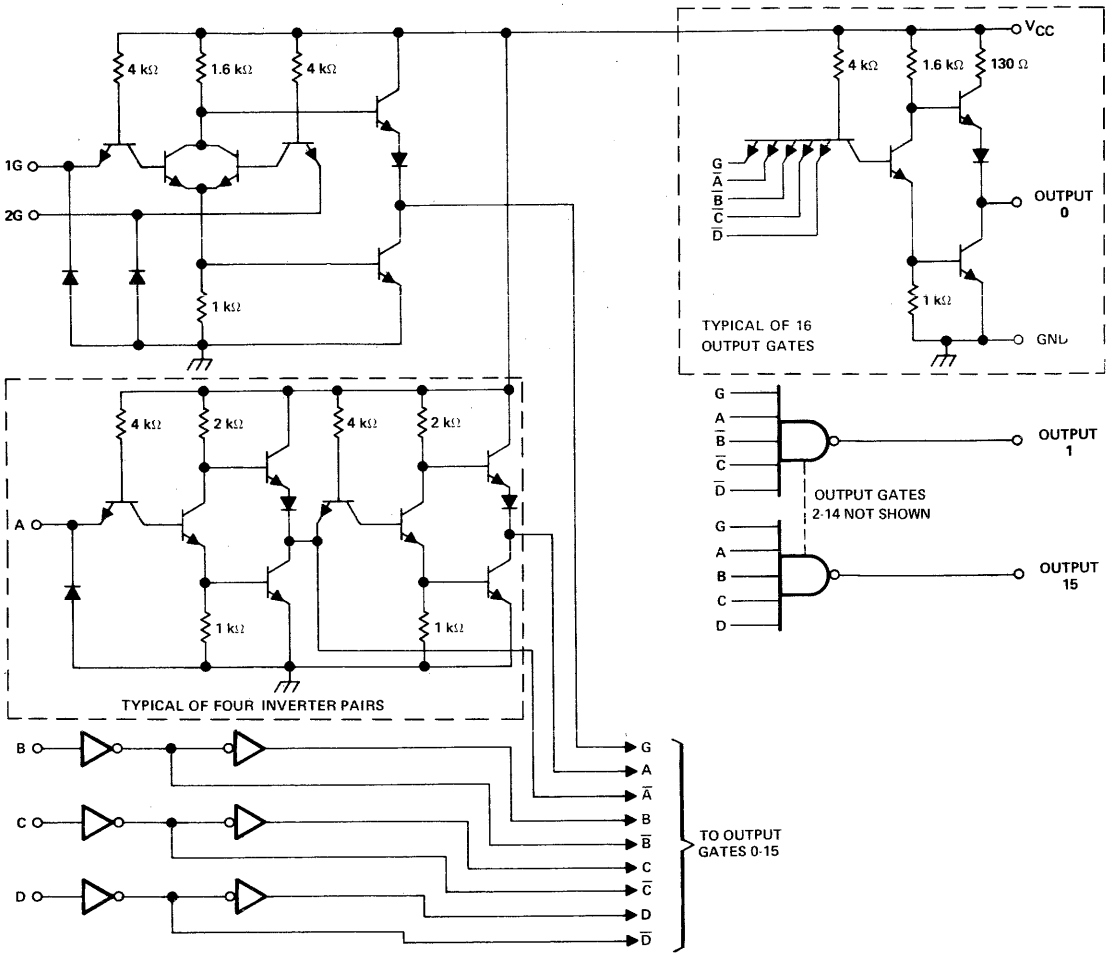
9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram



schematic

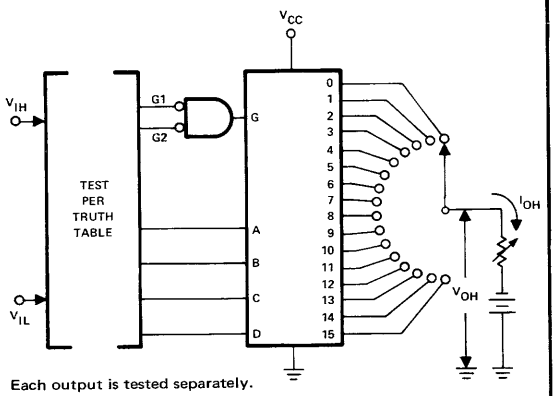


Component values shown are nominal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

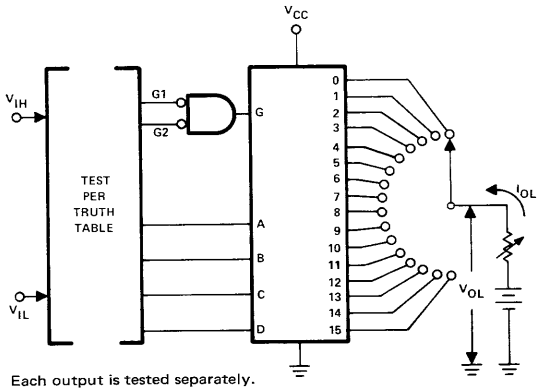
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



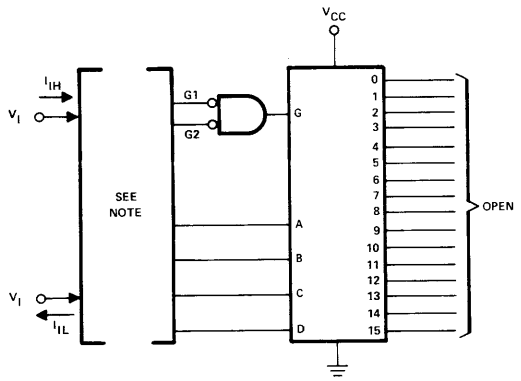
Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



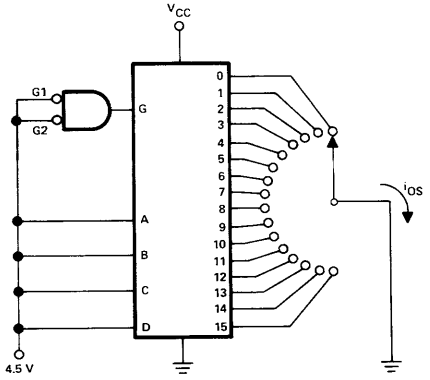
Each output is tested separately.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}



Each input is tested separately for both I_{IH} and I_{IL}. Inputs not under test are grounded, with the exception that when testing I_{IL} of a strobe input, the other strobe is at 2.4 V.

FIGURE 3–I_{IH}, I_{IL}



Each output is tested separately.

FIGURE 4–I_{OS}

9

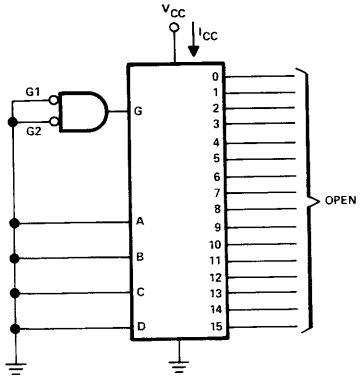
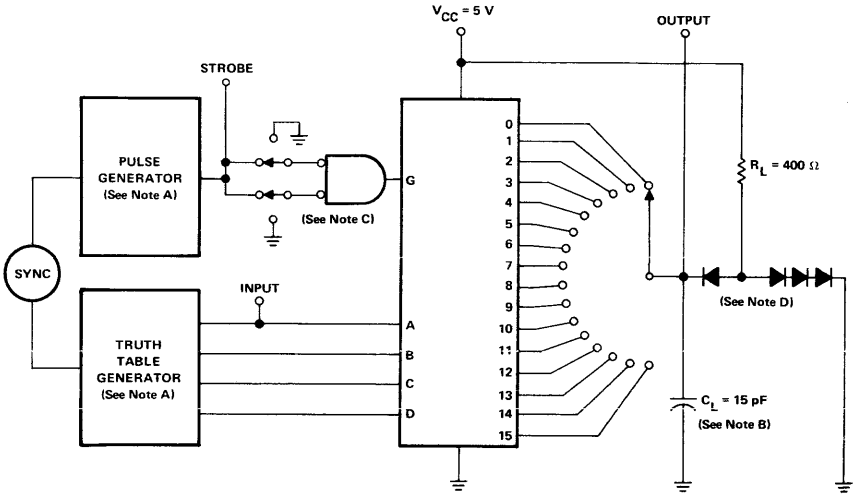


FIGURE 5–I_{CC}

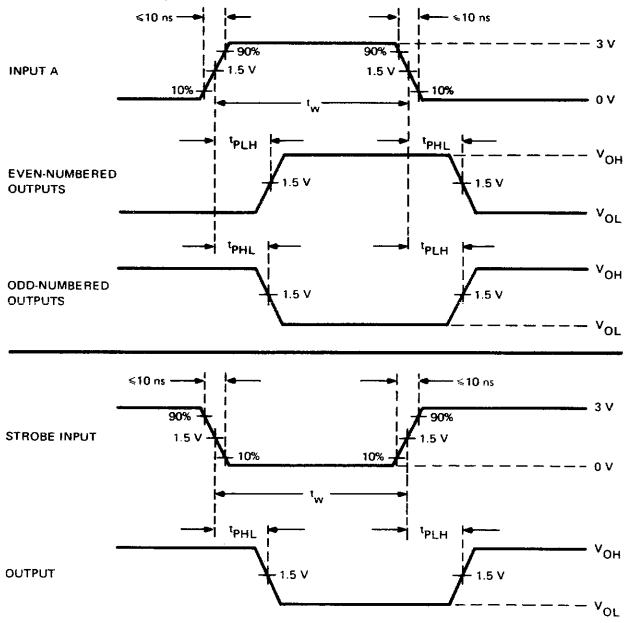
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The truth table generator and the pulse generator have the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$, t_w = 100 ns.
B. C_L includes probe and jig capacitance.
C. When measuring select-input-to-output times the strobe inputs are grounded. When measuring strobe-input-to-output times, the untested strobe input is grounded. Select inputs determine output under test through truth table generator.
D. All diodes are 1N3064.

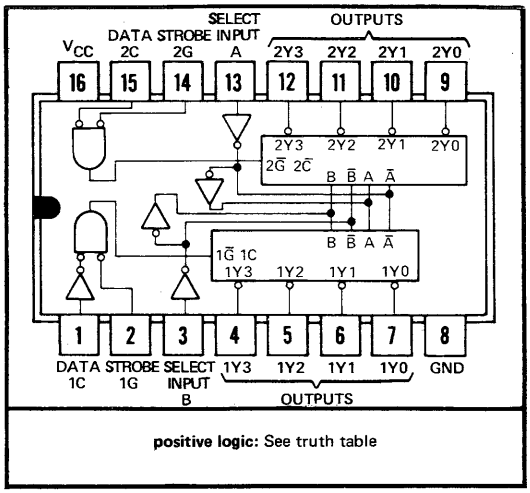
FIGURE 6–SWITCHING TIMES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54155, SN54156, SN74155, SN74156
DUAL 2-LINE-TO-4-LINE DECODERS/DEMULTIPLEXERS

- Applications:
  - Dual 2-to-4-Line Decoder
  - Dual 1-to-4-Line Demultiplexer
  - 3-to-8-Line Decoder
  - 1-to-8-Line Demultiplexer
- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words
- Input Clamping Diodes Simplify System Design
- Choice of Outputs:
  - Totem Pole (SN54155, SN74155)
  - Open-Collector (SN54156, SN74156)
- Typical Average Propagation Delay Times:
  - 16 ns through 2 levels of logic
  - 21 ns through 3 levels of logic
- Typical Power Dissipation . . . 125 mW

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. See typical applications data and the truth tables for more details.

9

The SN54155/SN74155 circuits, with totem-pole outputs, are rated to fan-out to 10 normalized Series 54/74 loads in the low-level output state, and to 20 loads in the high-level output state. The SN54156/SN74156 circuits, with open-collector outputs, are rated to sink 16 milliamperes at a low-level output voltage of less than 0.4 volt. Input-clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design. Typical power dissipation is 125 milliwatts. Typical average propagation delay times are 16 nanoseconds through 2 levels of logic and 21 nanoseconds through 3 levels of logic for the SN54155/SN74155.

The SN54155 and SN54156 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74155 and SN74156 are characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

truth tables (H = high level, L = low level, X = irrelevant)

2-LINE-TO-4-LINE DECODER OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE-TO-8-LINE DECODER TO 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54155, SN54156 Circuits . . . . . −55°C to 125°C
SN74155, SN74156 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54155			SN74155			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

	SN54156			SN74156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN54155, SN74155			UNIT
					MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −800 μA		2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_{IH}	High-level input current (each input)	4	V_{CC} = MAX, V_I = 2.4 V				40	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (each input)	4	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN54155	−20		−55	mA
				SN74155	−18		−57	
I_{CC}	Supply current	6	V_{CC} = MAX	SN54155		25	35	mA
				SN74155		25	40	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN54156, SN74156			UNIT
					MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	2 and 3			2			V
V_{IL}	Low-level input voltage	2					0.8	V
I_{OH}	High-level output current	3	V_{CC} = MIN, V_I = 2 V, V_{OH} = 5.5 V				250	μA
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_{IH}	High-level input current (each input)	4	V_{CC} = MAX, V_I = 2.4 V				40	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (each input)	4	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{CC}	Supply current	6	V_{CC} = MAX	SN54156		25	35	mA
				SN74156		25	40	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

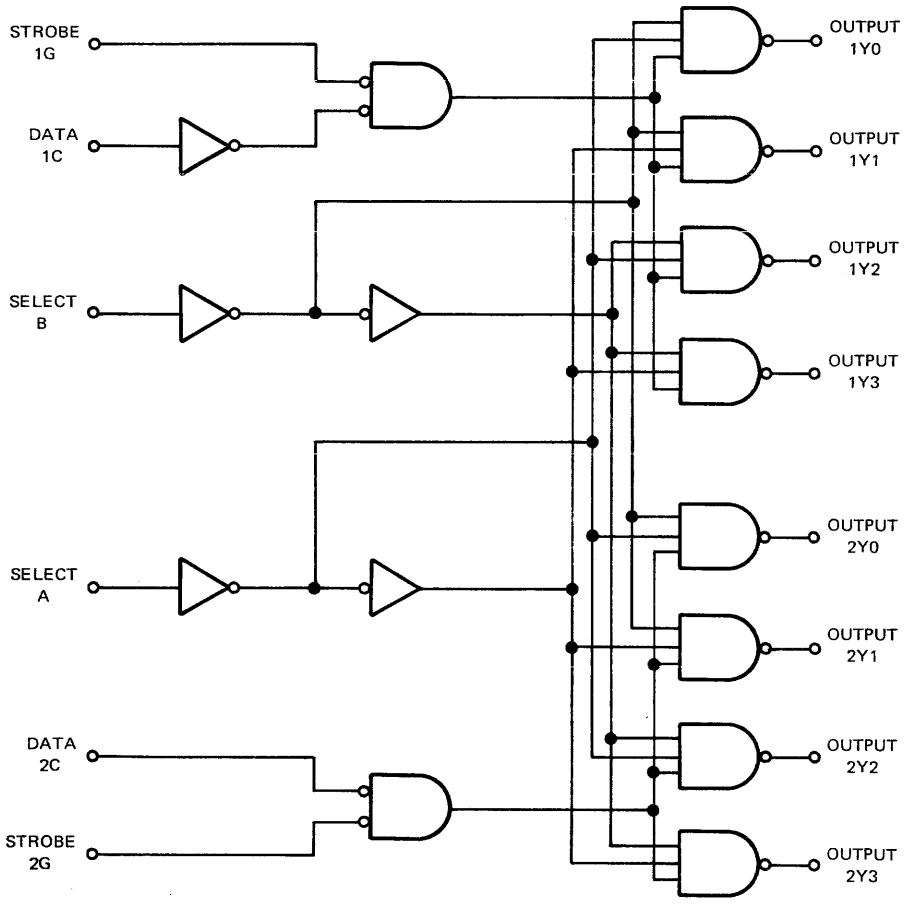
9

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST FIGURE	TEST CONDITIONS	SN54155 SN74155			SN54156 SN74156			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A, B, 2C, 1G, or 2G	Y	2	7	C_L = 15 pF, R_L = 400 Ω		13	20		15	23	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2				18	27		20	30	ns
t_{PLH}	A or B	Y	3				21	32		23	34	ns
t_{PHL}	A or B	Y	3				21	32		23	34	ns
t_{PLH}	1C	Y	3				16	24		18	27	ns
t_{PHL}	1C	Y	3				20	30		22	33	ns

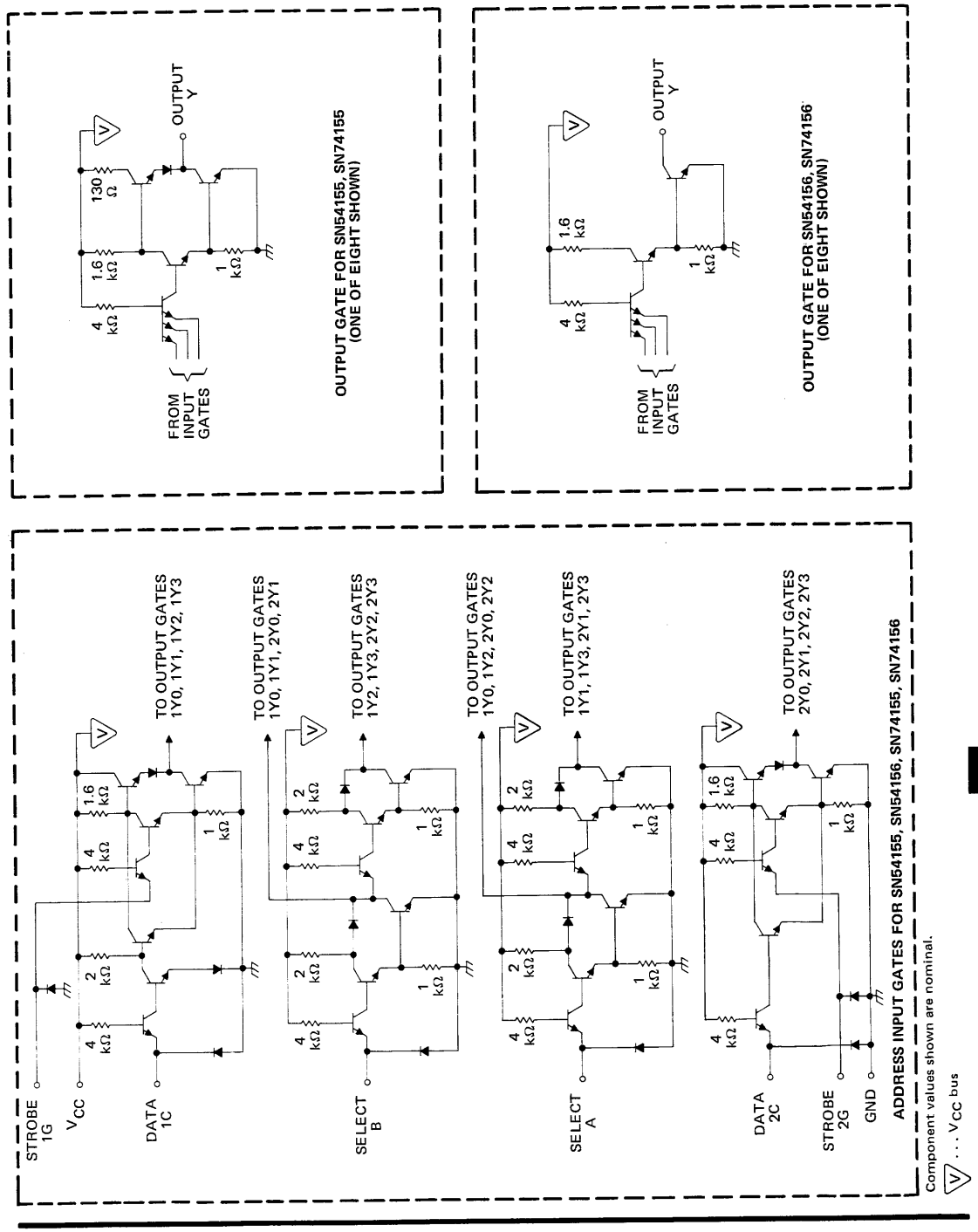
¶t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

functional block diagram



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

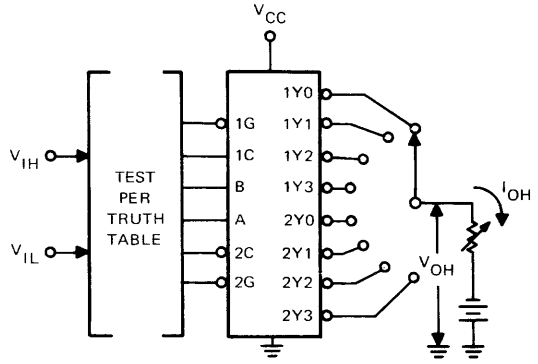
schematic


OUTPUT GATE FOR SN54155, SN74155
(ONE OF EIGHT SHOWN)
OUTPUT Y
130 Ω
1.6 kΩ
4 kΩ
1 kΩ
FROM INPUT GATES
OUTPUT GATE FOR SN54156, SN74156
(ONE OF EIGHT SHOWN)
OUTPUT Y
1.6 kΩ
4 kΩ
1 kΩ
FROM INPUT GATES
ADDRESS INPUT GATES FOR SN54155, SN54156, SN74155, SN74156
TO OUTPUT GATES 1Y0, 1Y1, 1Y2, 1Y3
TO OUTPUT GATES 1Y0, 1Y1, 2Y0, 2Y1
TO OUTPUT GATES 1Y2, 1Y3, 2Y2, 2Y3
TO OUTPUT GATES 1Y0, 1Y2, 2Y0, 2Y2
TO OUTPUT GATES 1Y1, 1Y3, 2Y1, 2Y3
TO OUTPUT GATES 2Y0, 2Y1, 2Y2, 2Y3
1.6 kΩ
2 kΩ
4 kΩ
1 kΩ
STROBE 1G
VCC
DATA 1C
SELECT B
SELECT A
DATA 2C
STROBE 2G
GND
Component values shown are nominal.
. . . VCC bus

9

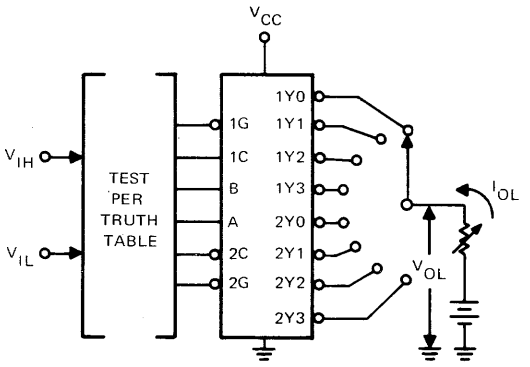
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



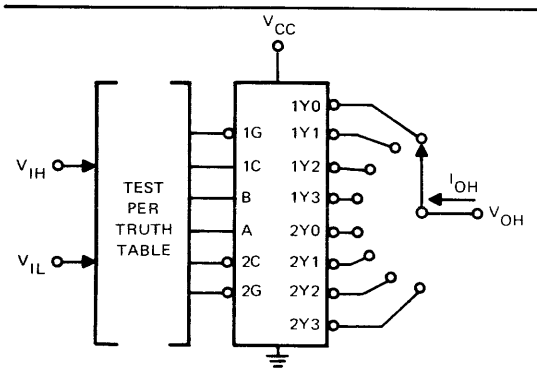
Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



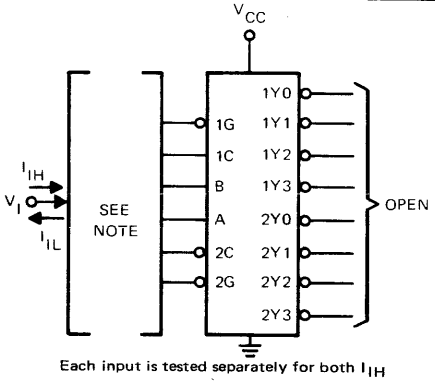
Each output is tested separately.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}



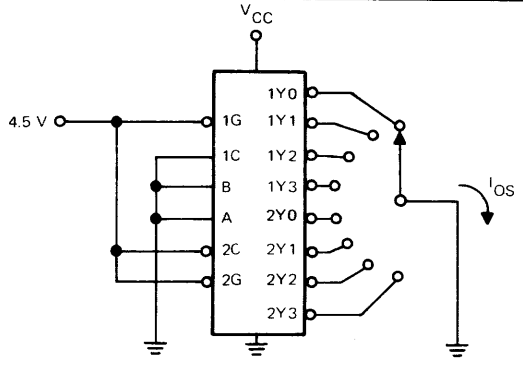
Each output is tested separately.

FIGURE 3–V_{IH}, V_{IL}, I_{OH}



Each input is tested separately for both I_{IH} and I_{IL}. Inputs not under test are grounded.

FIGURE 4–I_{IH}, I_{IL}



Each output is tested separately.

FIGURE 5–I_{OS}

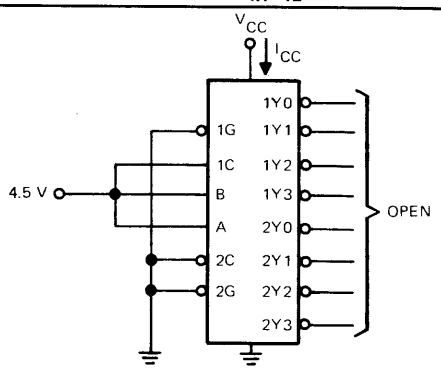


FIGURE 6–I_{CC}

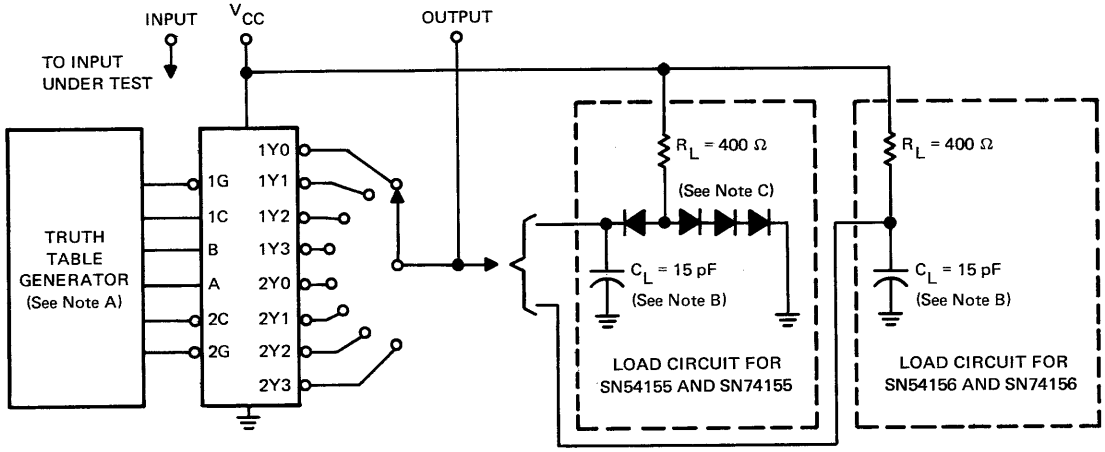
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

9

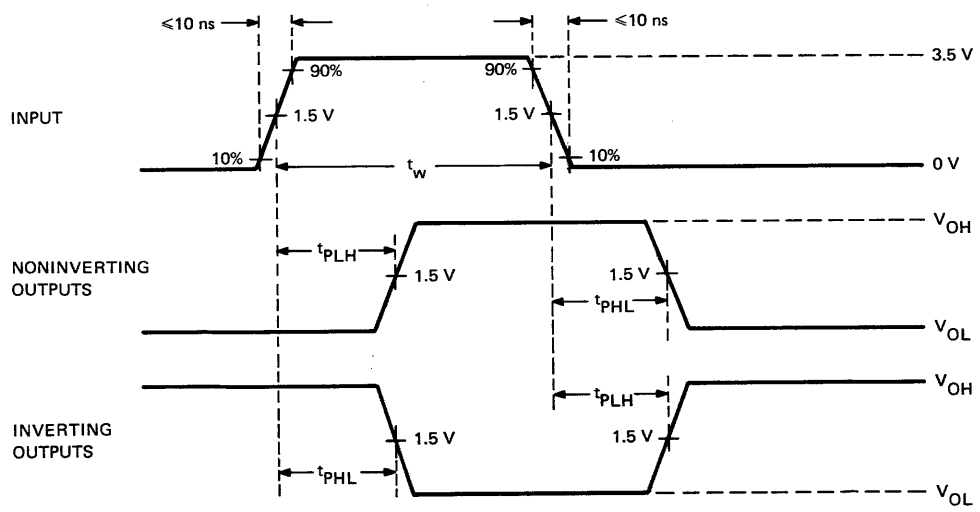
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The truth table generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$, t_w = 100 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

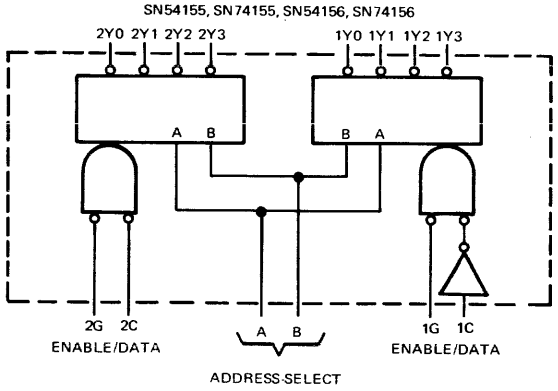
FIGURE 7–PROPAGATION DELAY TIME

TYPICAL APPLICATION DATA

THE SN54155, SN74155, SN54156, or SN74156 may be used as a dual 2-line-to-4-line decoder or a 1-line-to-4-line demultiplexer. These applications are identical except as follows:

When decoding, the 2-line code is applied to select inputs A and B. The 4-line output section (1Y0, 1Y1, 1Y2, 1Y3) is enabled by taking strobe 1G low and input 1C high. The other 4-line output section (2Y0, 2Y1, 2Y2, 2Y3) is enabled by taking both strobe 2G and input 2C low. Note that the separate enable lines permit the user complete flexibility in decoding at either or both of the output sections. The strobe also permits cascading and allows disabling of the circuits until the addressing transients have passed.

When demultiplexing, the serial data is applied to the data inputs 1C and 2C and distribution to the outputs is controlled by the A and B select inputs. Again, the separate strobe inputs, 1G and 2G, permit demultiplexing to occur at either or both output sections, and cascading.

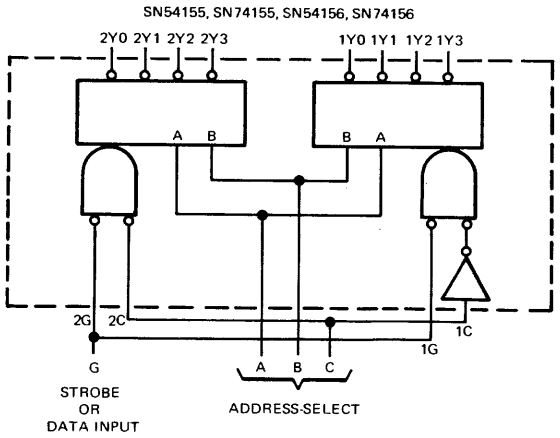


DUAL 2-LINE-TO-4-LINE DECODER/1-TO-4-LINE DEMULTIPLEXER

Any of these circuits may also be used as a 3-line-to-8-line decoder or a 1-line-to-8-line demultiplexer.

When used as a decoder, data inputs 1C and 2C are connected together and serve as the third (C) select line. The strobes are also connected together and are used for enabling and/or cascading.

When used as a demultiplexer, the common strobe line serves as the data input.



3-LINE-TO-8-LINE DECODER/1-TO-8-LINE DEMULTIPLEXER

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5445, SN54145, SN7445, SN74145
BCD-TO-DECIMAL DECODER/DRIVERS

TTL MSI LAMP, LOGIC, OR MOS DRIVERS
featuring

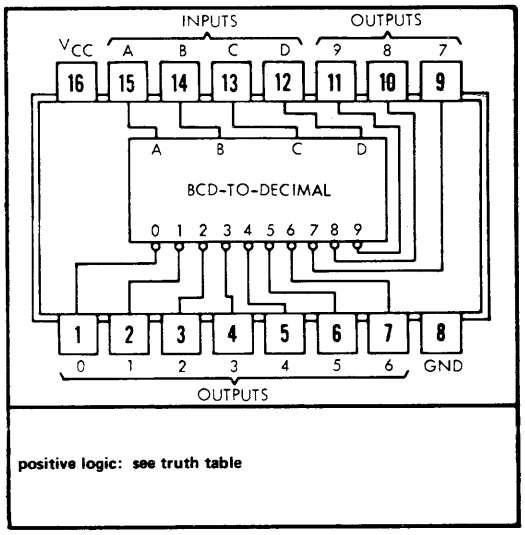
- Full Decoding of Input Logic
- 80 mA Sink-Current Capability

logic

TRUTH TABLE

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature TTL inputs and high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (SN5445, SN7445 = 30 volts and SN54145, SN74145 = 15 volts) will sink up to 80 milliamperes of current. Each input is one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Note 1) . . . . . 5.5 V
Maximum Current into each Output (See Note 2) . . . . . 1 mA
Operating Free-Air Temperature Range: SN5445, SN54145 Circuits . . . . . −55°C to 125°C
SN7445, SN74145 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. This rating applies when the output is off.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5445, SN54145 Circuits	4.5	5	5.5	V
SN7445, SN74145 Circuits	4.75	5	5.25	V
Voltage on any Output (See Note 2): SN5445, SN7445 Circuits			30	V
SN54145, SN74145 Circuits			15	V

electrical characteristics over recommended operating temperature range (unless otherwise noted)

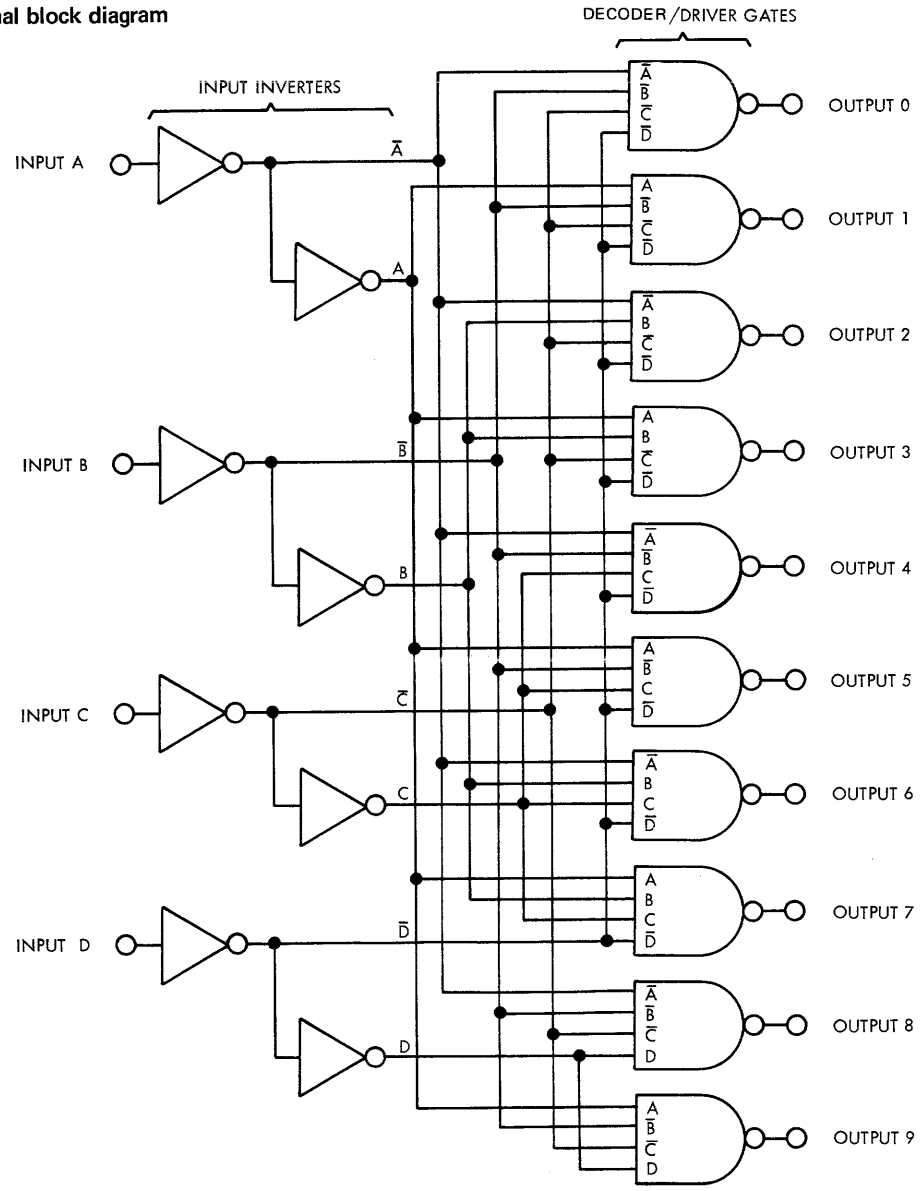
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2					0.8	V
V_{on}	On-state output voltage	1	V_{CC} = MIN, I_{sink} = 80 mA			0.5	0.9	V
			V_{CC} = MIN, I_{sink} = 20 mA				0.4	V
V_{off}	Off-state output voltage (SN5445 or SN7445)	2	V_{CC} = MAX, I_{off} = 250 μA		30			V
V_{off}	Off-state output voltage (SN54145 or SN74145)	2	V_{CC} = MAX, I_{off} = 250 μA		15			V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
I_{CC}	Supply current	4	V_{CC} = MAX	SN5445, SN54145		43	62	mA
				SN7445, SN74145		43	70	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

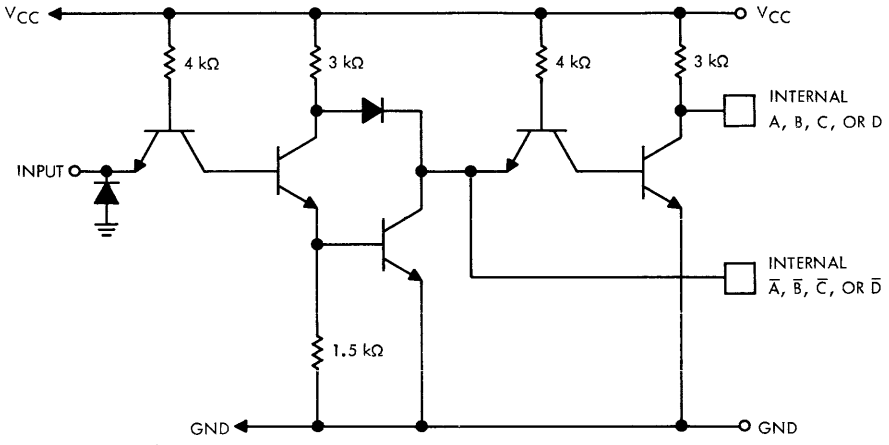
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level	5	C_L = 15 pF, R_L = 100 Ω			50	ns
t_{pd0}	Propagation delay time to logical 0 level	5	C_L = 15 pF, R_L = 100 Ω			50	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

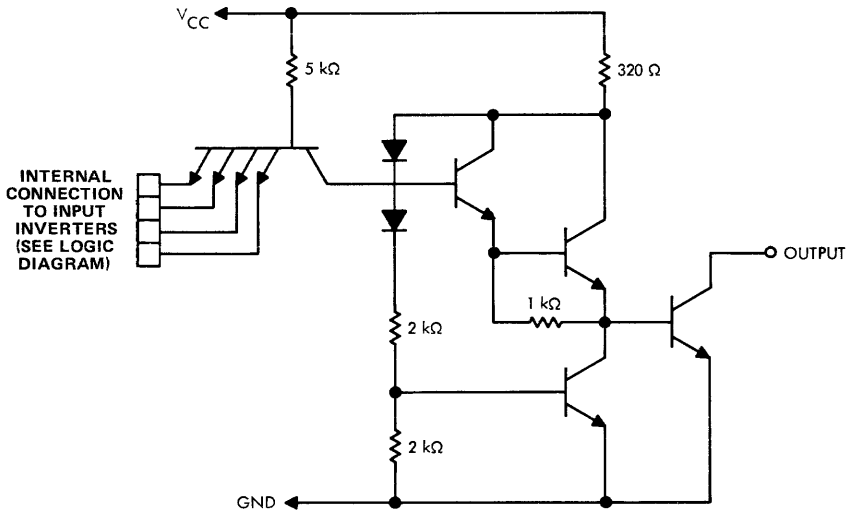
functional block diagram



schematic



EACH PAIR OF INPUT INVERTERS



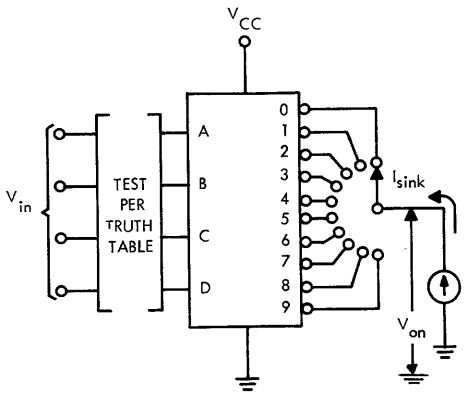
EACH DECODER/DRIVER GATE

NOTE: 1. Component values shown are nominal.

9

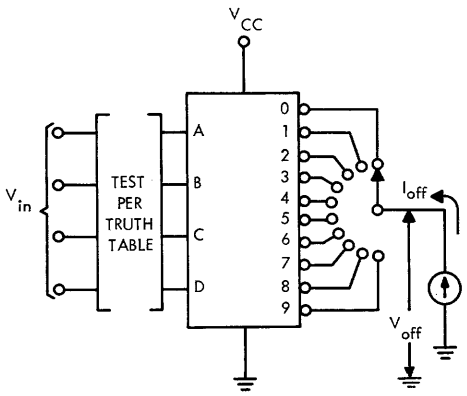
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



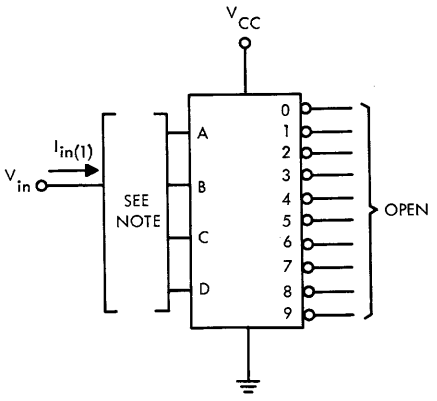
1. Each output is tested separately in the ON state.

FIGURE 1



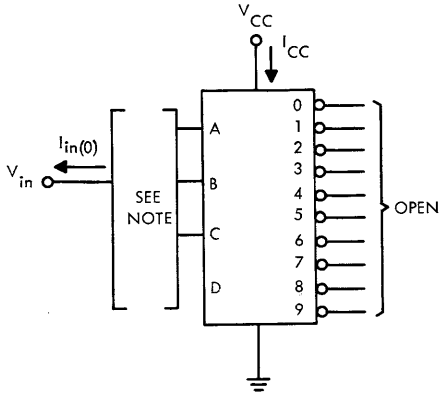
1. Each output is tested separately in the OFF state.

FIGURE 2



1. Each input is tested separately.

FIGURE 3



1. When testing $I_{in(0)}$ each input is tested separately.
2. When testing I_{CC} all inputs are grounded and outputs are open.

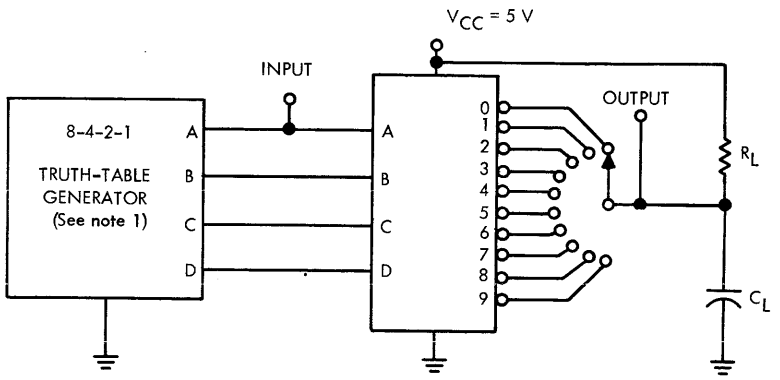
FIGURE 4

† Arrows indicate actual direction of current flow

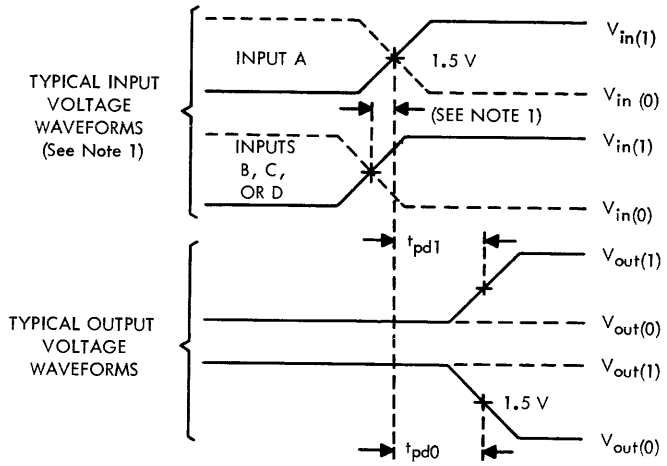
9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



NOTES: 1. The truth-table generator has the following characteristics: $V_{out(1)} \geq 2.4$ V, $V_{out(0)} \leq 0.4$ V, t_r and $t_f < 10$ ns, and PRR = 1 MHz. Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions.
2. C_L includes probe and jig capacitance.

FIGURE 5-SWITCHING TIMES

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5446A, SN5447A, SN5448, SN5449
SN7446A, SN7447A, SN7448, SN7449
BCD-TO-SEVEN-SEGMENT DECODER/DRIVERS

SN5446A, SN5447A, SN7446A, SN7447A
featuring

- DIRECT DRIVE FOR INDICATORS
- OPEN-COLLECTOR OUTPUTS
- LAMP-TEST PROVISION
- LEADING/TRAILING ZERO SUPPRESSION
- CERAMIC OR PLASTIC DUAL-IN-LINE PACKAGES

SN5448, SN7448
featuring

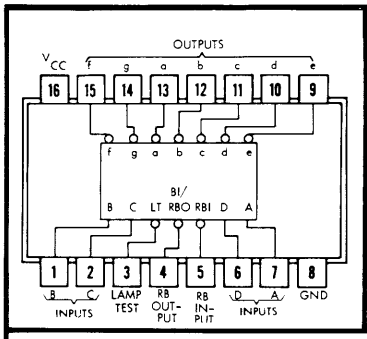
- PASSIVE PULL-UP OUTPUTS
- LAMP-TEST PROVISION
- LEADING/TRAILING ZERO SUPPRESSION
- CERAMIC OR PLASTIC DUAL-IN-LINE PACKAGES

SN5449, SN7449
featuring

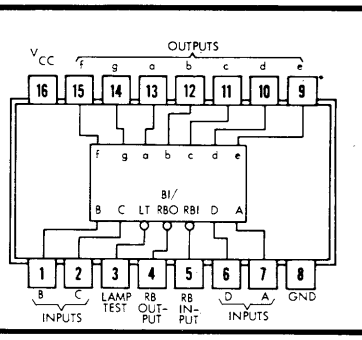
- OPEN-COLLECTOR OUTPUTS
- BLANKING INPUT
- WELDED FLAT PACKAGE

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†

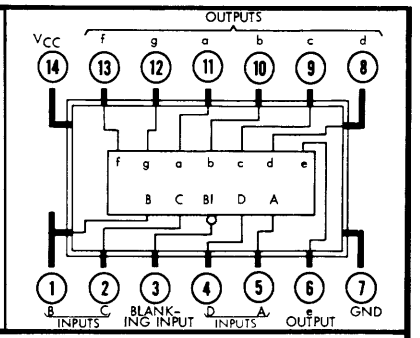
SN5446A, SN5447A, SN7446A, SN7447A



SN5448, SN7448



SN5449, SN7449
W FLAT PACKAGE (TOP VIEW)



positive logic: see truth tables

†Pin assignments for these circuits are the same for all packages.

ALL CIRCUIT TYPES FEATURE:

- TTL-DTL COMPATIBILITY
- FULL DECODING OF ALL 16 INPUT COMBINATIONS
- LAMP INTENSITY MODULATION CAPABILITY

9

description

These monolithic, TTL, BCD-to-seven-segment decoder/drivers consist of NAND gates, input buffers, and seven AND-OR-INVERT gates. Three configurations offer active-low, high-sink-current outputs (SN5446A and SN5447A) for driving indicators directly; active-high, passive-pull-up outputs, (SN5448) and active-high, open-collector outputs (SN5449) for current-sourcing applications to drive logic circuits or discrete, active components. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates, and the remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output, and ripple-blanking input for the SN5446A, SN5447A and SN5448. Four NAND gates and four input buffers provide BCD data and its complement and a buffer provides blanking input for the SN5449. See functional block diagrams.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a seven-segment display indicator (SN5446A and SN5447A) or other components (SN5448, SN5449). The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the SN5446A and SN5447A are designed to withstand the relatively high voltages required for seven segment indicators. The SN5446A outputs will withstand 30 volts, and the SN5447A will withstand 15 volts, with a maximum reverse current of 250 microamperes. Indicator segments requiring up to 40 milliamperes of current may be driven directly from the SN5446A or SN5447A high-performance output transistors. Segment identification with resultant displays are shown in Figure A. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

description (continued)

The SN5446A, SN5447A, and SN5448 circuits incorporate automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is a logical 1. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity or to inhibit the outputs. All inputs except the BI/RBO nodes are one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs. Power dissipation is typically 320 milliwatts (SN5446A, SN5447A, and SN5448) or 165 milliwatts (SN5449).

The SN5446A, SN5447A, SN5448 and SN5449 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7446A, SN7447A, SN7448, and SN7449 (electrically identical to the corresponding Series 54 types) are for operation over the temperature range of 0°C to 70°C.

TRUTH TABLE SN5446A, SN5447A, SN7446A, SN7447A

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1
1	1	X	0	0	0	1	1	1	0	0	1	1	1	1	1
2	1	X	0	0	1	0	1	0	0	1	0	0	1	0	
3	1	X	0	0	1	1	1	0	0	0	0	1	1	0	
4	1	X	0	1	0	0	1	1	0	0	1	1	0	0	
5	1	X	0	1	0	1	1	0	1	0	0	1	0	0	
6	1	X	0	1	1	0	1	1	1	0	0	0	0	0	
7	1	X	0	1	1	1	1	0	0	0	1	1	1	1	
8	1	X	1	0	0	0	1	0	0	0	0	0	0	0	
9	1	X	1	0	0	1	1	0	0	0	1	1	0	0	
10	1	X	1	0	1	0	1	1	1	1	0	0	1	0	
11	1	X	1	0	1	1	1	1	1	0	0	1	1	0	
12	1	X	1	1	0	0	1	1	0	1	1	1	0	0	
13	1	X	1	1	0	1	1	0	1	1	0	1	0	0	
14	1	X	1	1	1	0	1	1	1	1	0	0	0	0	
15	1	X	1	1	1	1	1	1	1	1	1	1	1	1	
BI	X	X	X	X	X	X	0	1	1	1	1	1	1	1	2
RBI	1	0	0	0	0	0	0	1	1	1	1	1	1	1	3
LT	0	X	X	X	X	X	1	0	0	0	0	0	0	0	4

NOTES:
1. BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input (BI) must be open or held at a logical 1 when output functions 0 through 15 are desired, and the ripple-blanking input (RBI) must be open or at a logical 1 if blanking of a decimal 0 is not desired. X = input may be high or low.
2. When a logical 0 is applied directly to the blanking input (forced condition) all segment outputs go to a logical 0 regardless of the state of any other input condition.
3. When the ripple-blanking input (RBI) and inputs A, B, C, and D are at logical 0, with the lamp test input at logical 1, all segment outputs go to a logical 1 and the ripple-blanking output (RBO) goes to a logical 0 (response condition).
4. When the blanking input/ripple-blanking output (BI/RBO) is open or held at a logical 1, and a logical 0 is applied to the lamp-test input, all segment outputs go to a logical 0.

TRUTH TABLE SN5448, SN7448

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	1	X	0	0	0	1	1	0	1	1	0	0	0	0	1
2	1	X	0	0	1	0	1	1	1	0	1	1	0	1	
3	1	X	0	0	1	1	1	1	1	1	1	0	0	1	
4	1	X	0	1	0	0	1	0	1	1	0	0	1	1	
5	1	X	0	1	0	1	1	1	0	1	1	0	1	1	
6	1	X	0	1	1	0	1	0	0	1	1	1	1	1	
7	1	X	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	X	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	X	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	X	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	X	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	X	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	X	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	X	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	X	1	1	1	1	1	0	0	0	0	0	0	0	
BI	X	X	X	X	X	X	0	0	0	0	0	0	0	0	2
RBI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3
LT	0	X	X	X	X	X	1	1	1	1	1	1	1	1	4

NOTES: 1. BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input (BI) must be open or held at a logical 1 when output functions 0 through 15 are desired, and the ripple-blanking input (RBI) must be open or at a logical 1 if blanking of a decimal 0 is not desired. X = input may be high or low.

2. When a logical 0 is applied directly to the blanking input (forced condition) all segment outputs go to a logical 0 regardless of the state of any other input condition.

3. When the ripple-blanking input (RBI) and inputs A, B, C, and D are at logical 0, with the lamp test at logical 1, all segment outputs go to a logical 0 and the ripple-blanking output (RBO) goes to a logical 0 (response condition).

4. When the blanking input/ripple-blanking output (BI/RBO) is open or held at a logical 1, and a logical 0 is applied to the lamp-test input, all segment outputs go to a logical 1.

TRUTH TABLE SN5449, SN7449

	INPUTS					OUTPUTS							
DECIMAL OR FUNCTION	D	C	B	A	BI	a	b	c	d	e	f	g	NOTE
0	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	1	0	1	1	0	0	0	0	
2	0	0	1	0	1	1	1	0	1	1	0	1	
3	0	0	1	1	1	1	1	1	1	0	0	1	
4	0	1	0	0	1	0	1	1	0	0	1	1	
5	0	1	0	1	1	1	0	1	1	0	1	1	
6	0	1	1	0	1	0	0	1	1	1	1	1	
7	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	1	1	1	1	0	0	0	0	0	0	0	
BI	X	X	X	X	0	0	0	0	0	0	0	0	2

NOTES: 1. The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired.

2. When a logical 0 is applied to the blanking input all segment outputs go to a logical 0 regardless of the state of any other input condition.
X = input may be high or low.

9

CIRCUIT TYPES SN5446A, SN5447A, SN5448, SN5449
SN7446A, SN7447A, SN7448, SN7449
BCD-TO-SEVEN-SEGMENT DECODER/DRIVERS

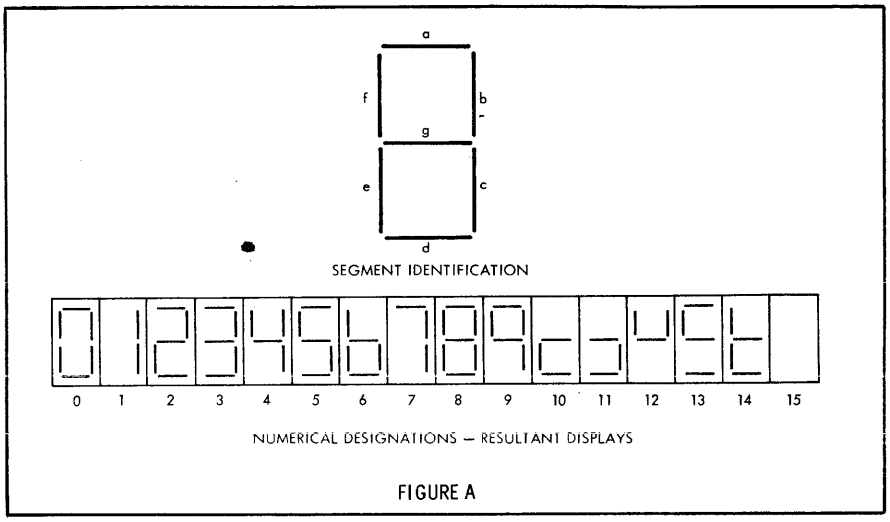


FIGURE A

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Current Into any Output of SN5446A, SN7446A, SN5447A, SN7447A, SN5449, SN7449 Circuits (See Note 3) 1 mA
Operating Case Temperature Range: SN5449 Circuits . . . . . –55°C to 125°C
Operating Free-Air Temperature Range:
SN5446A, SN5447A, SN5448 Circuits . . . . . –55°C to 125°C
SN7446A, SN7447A, SN7448, SN7449 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . –65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.
3. This rating applies when the output is off.

9

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):				
SN5446A, SN5447A, SN5448, SN5449 Circuits	4.5	5	5.5	V
SN7446A, SN7447A, SN7448, SN7449 Circuits	4.75	5	5.25	V
Continuous Voltage at Outputs a through g:				
SN5446A, SN7446A Circuits			30	V
SN5447A, SN7447A Circuits			15	V
SN5449, SN7449 Circuits			5.5	V
Normalized Fan-Out From Outputs a through g to Series 54/74 Loads:				
SN5446A, SN7446A, SN5447A, SN7447A Circuits			24	
SN5448, SN7448 Circuits			4	
SN5449, SN7449 Circuits			6	
Normalized Fan-Out From BI/RBO Node to Series 54/74 Loads:				
SN5446A, SN7446A, SN5447A, SN7447A, SN5448, SN7448 Circuits			5	
Output Sink Current, I_{sink}:				
SN5446A, SN7446A, SN5447A, SN7447A Outputs a through g			40	mA
SN5448, SN7448 Outputs a through g			6.4	mA
SN5449, SN7449 Outputs a through g			10	mA
SN5446A, SN7446A, SN5447A, SN7447A, SN5448, SN7448 BI/RBO Node			8	mA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input	1 and 2			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input	1 and 2					0.8	V
V_{on}	On-state output voltage at outputs a through g	1	V_{CC}=MIN, I_{sink}=40 mA			0.3	0.4	V
$V_{out(0)}$	Logical 0 output voltage at BI/RBO node	1	V_{CC}=MIN, I_{sink}=8 mA			0.3	0.4	V
V_{off}	Off-state output voltage at outputs a through g (SN5446A and SN7446A only)	2	V_{CC}=MAX, I_{off}=250 µA		30			V
V_{off}	Off-state output voltage at outputs a through g (SN5447A and SN7447A only)	2	V_{CC}=MAX, I_{off}=250 µA		15			V
$V_{out(1)}$	Logical 1 output voltage at BI/RBO node	2	V_{CC}=MIN, I_{load}=-200 µA		2.4	3.7		V
$I_{in(0)}$	Logical 0 level input current at any input except BI/RBO node	3	V_{CC}=MAX, V_{in}=0.4 V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at BI/RBO node	3	V_{CC}=MAX, V_{in}=0.4 V				-4.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except BI/RBO node	4	V_{CC}=MAX, V_{in}=2.4 V				40	µA
			V_{CC}=MAX, V_{in}=5.5 V				1	mA
I_{OS}	Short-circuit output current at BI/RBO node	5	V_{CC}=MAX				-4	mA
I_{CC}	Supply current	4	V_{CC}=MAX	SN5446A, SN5447A		64	85	mA
				SN7446A, SN7447A		64	103	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

9

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from A input to any output	6	C_L=15 pF, R_L=120 Ω			100	ns
t_{pd0}	Propcgation delay time to logical 0 level from A input to any output	6	C_L=15 pF, R_L=120 Ω			100	ns
t_{pd1}	Propagation delay time to logical 1 level from RBI input to any output	6	C_L=15 pF, R_L=120 Ω			100	ns
t_{pd0}	Propagation delay time to logical 0 level from RBI input to any output	6	C_L=15 pF, R_L=120 Ω			100	ns

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS †		MIN	TYP ‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input	1 and 2			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input	1 and 2		SN5449			0.6	V
				All others			0.8	
$V_{out(0)}$	Logical 0 output voltage at any output (SN5448, SN7448 only)	1	V_{CC} = MIN, I_{sink} = MAX			0.27	0.4	V
V_{on}	On-state output voltage at any output (SN5449, SN7449 only)	1	V_{CC} = MIN, I_{sink} = MAX			0.27	0.4	V
$V_{out(1)}$	Logical 1 level output voltage at outputs a through g (SN5448, SN7448)	2	V_{CC} = MIN, I_{load} = -400 μA		2.4	4.2		V
$V_{out(1)}$	Logical 1 level output at BI/RBO node (SN5448, SN7448 only)	2	V_{CC} = MIN, I_{load} = -200 μA		2.4	3.7		V
I_{load}	Load current available at outputs a through g (SN5448, SN7448 only)	2	V_{CC} = MIN, V_{out} = 0.85 V		-1.3	-2		mA
V_{off}	Off-state output voltage at any output (SN5449, SN7449 only)	2	V_{CC} = MAX, I_{off} = 250 μA		5.5			V
$I_{in(0)}$	Logical 0 level input current at any input (except BI/RBO node of SN5448, SN7448)	3	V_{CC} = MAX, V_{in} = 0.4 V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at BI/RBO node (SN5448, SN7448 only)	3	V_{CC} = MAX, V_{in} = 0.4 V				-4.2	mA
$I_{in(1)}$	Logical 1 level input current at any input (except BI/RBO node of SN5448, SN7448)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current at any output (except outputs a through g of SN5449, SN7449)	5	V_{CC} = MAX				-4	mA
I_{CC}	Supply current	4		SN5448		53	76	mA
				SN7448		53	90	mA
				SN5449		33	47	mA
				SN7449		33	56	mA

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ These typical values are at V_{CC} = 5 V, T_A = 25°C

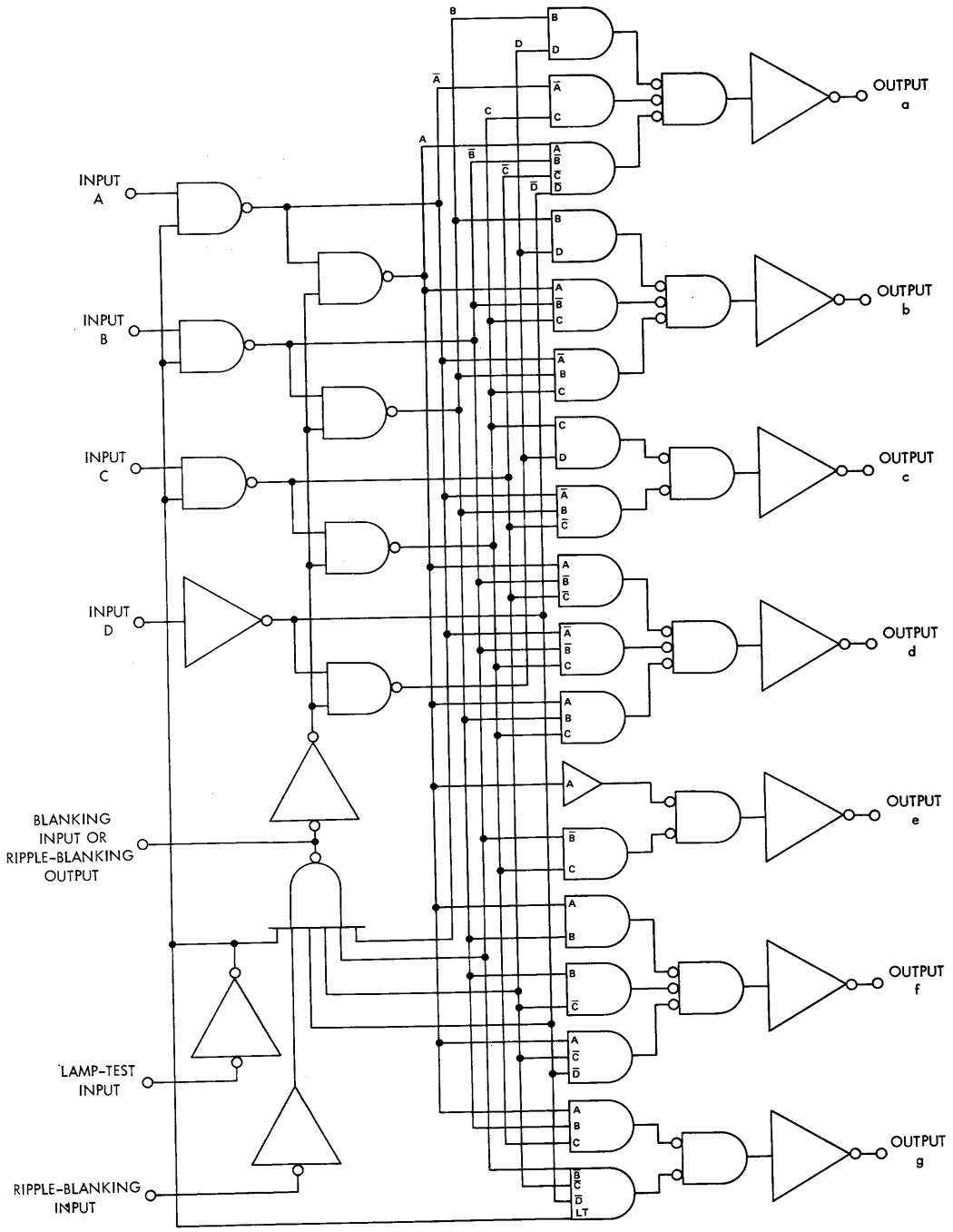
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS §	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from A input to any output	6	C_L = 15 pF			100	ns
t_{pd0}	Propagation delay time to logical 0 level from A input to any output	6	C_L = 15 pF			100	ns
t_{pd1}	Propagation delay time to logical 1 level from RBI input to any output	6	C_L = 15 pF			100	ns
t_{pd0}	Propagation delay time to logical 0 level from RBI input to any output	6	C_L = 15 pF			100	ns

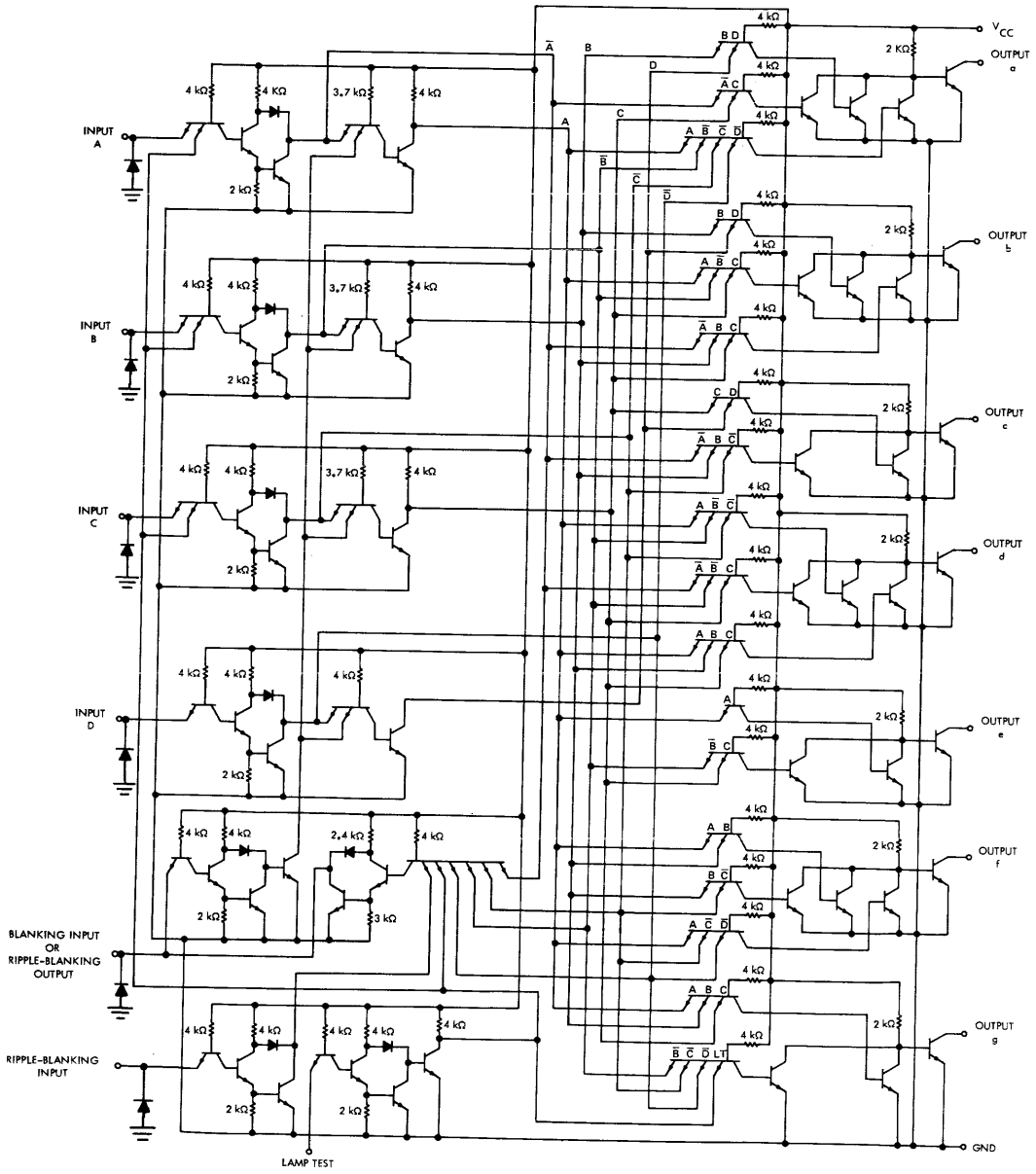
§ R_L = 1 kΩ for SN5448 and SN5449; R_L = 667 Ω for SN7448 and SN7449.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

functional block diagram

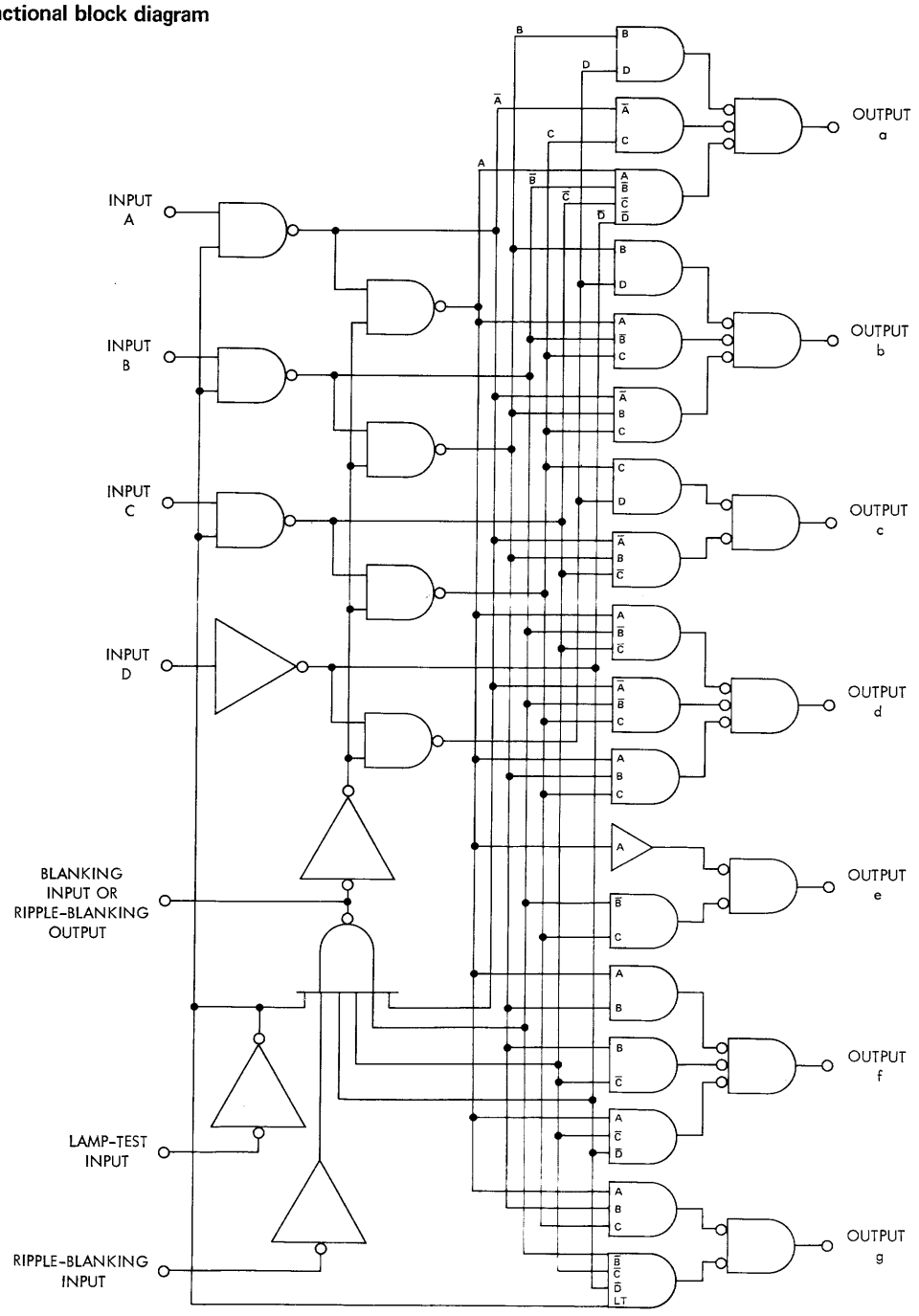


schematic diagram

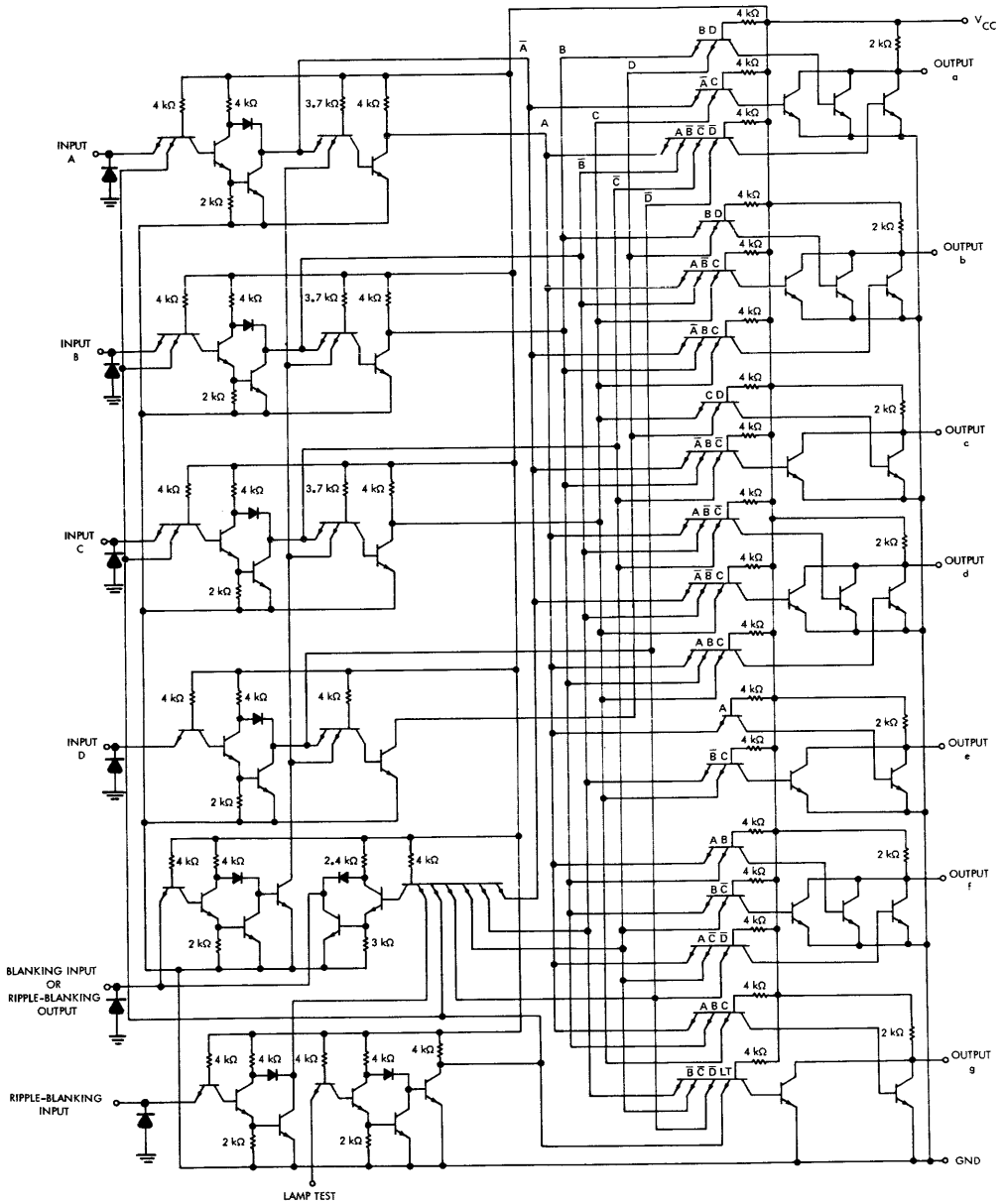


Component values shown are nominal

functional block diagram

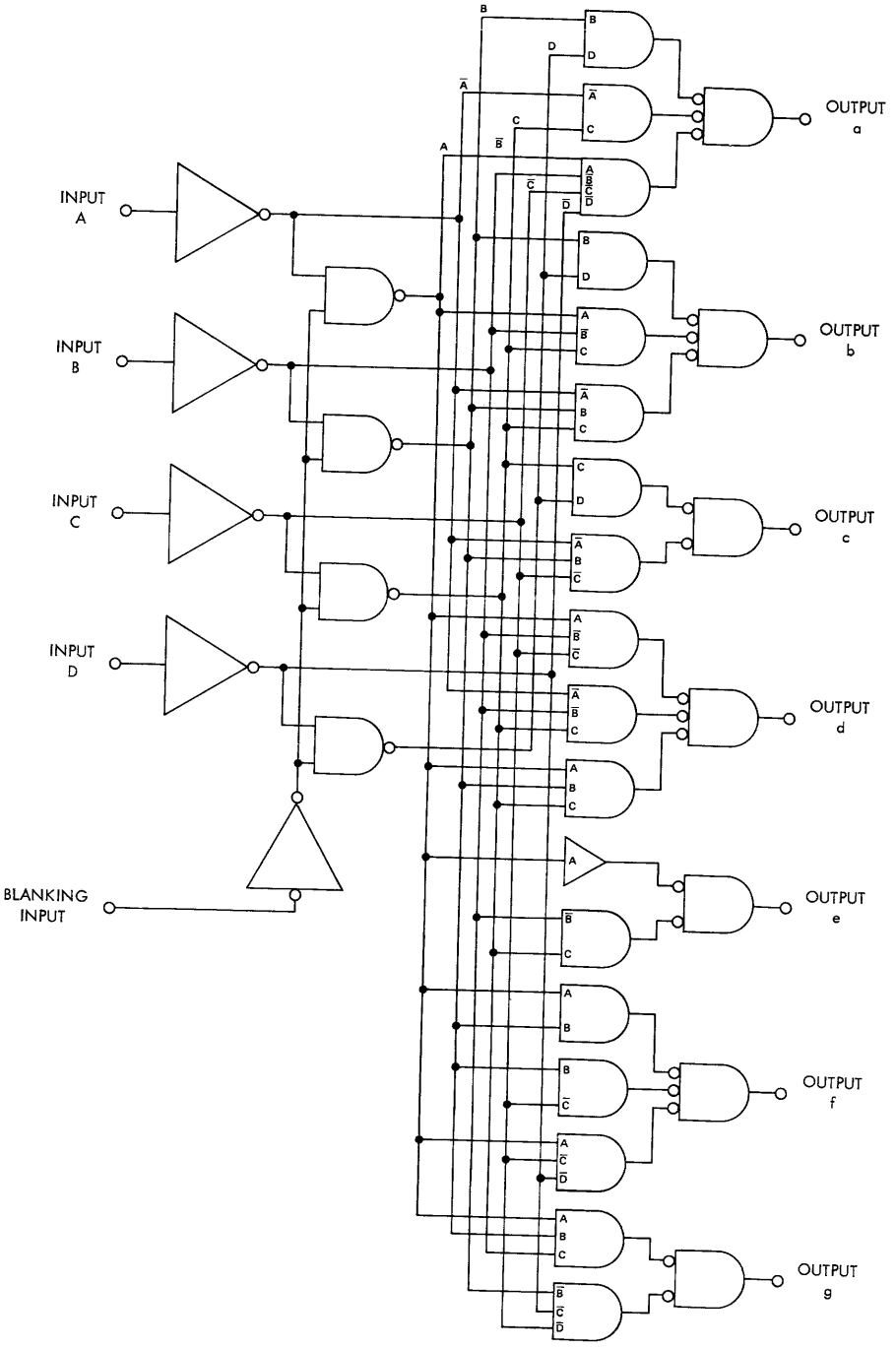


schematic diagram

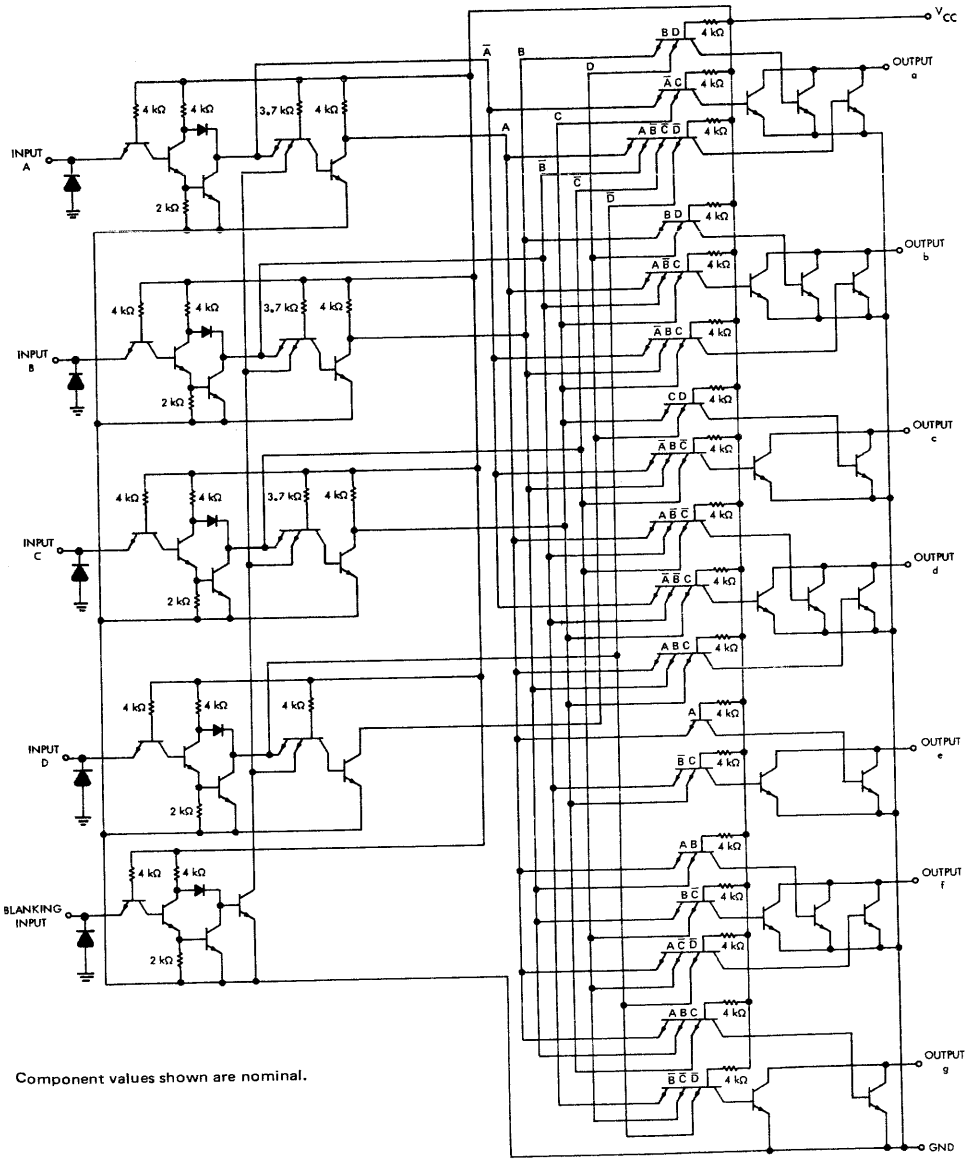


Compenent values shown are nominal

functional block diagram



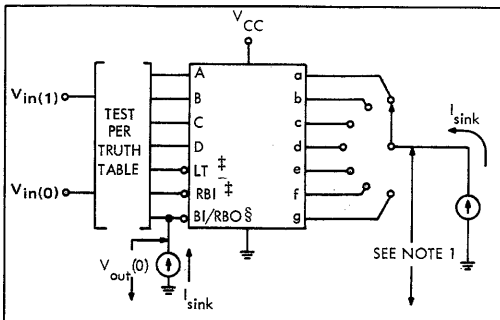
schematic diagram



Component values shown are nominal.

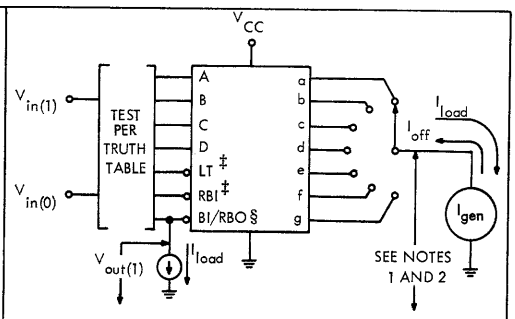
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



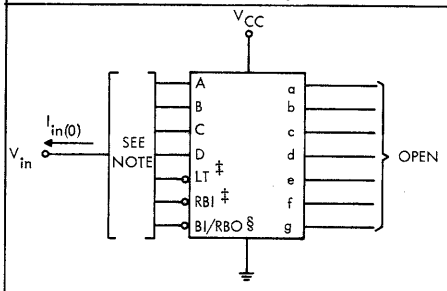
1. Measure V_{on} for SN5446A, SN5447A, SN5449, SN7446A, SN7447A, and SN7449. Measure $V_{out(0)}$ for SN5448 and SN7448.

FIGURE 1



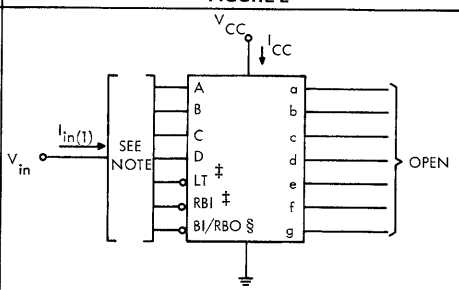
1. Measure V_{off} for SN5446A, SN5447A, SN5449, SN7446A, SN7447A, and SN7449.
2. Measure $V_{out(1)}$ for SN5448 and SN7448.

FIGURE 2



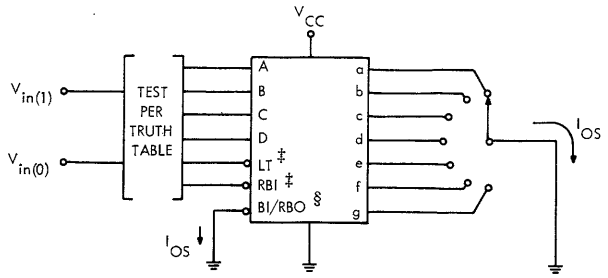
1. Each input is tested separately.

FIGURE 3



1. Each input is tested separately for $I_{in(1)}$.

FIGURE 4



1. Each output is tested separately.

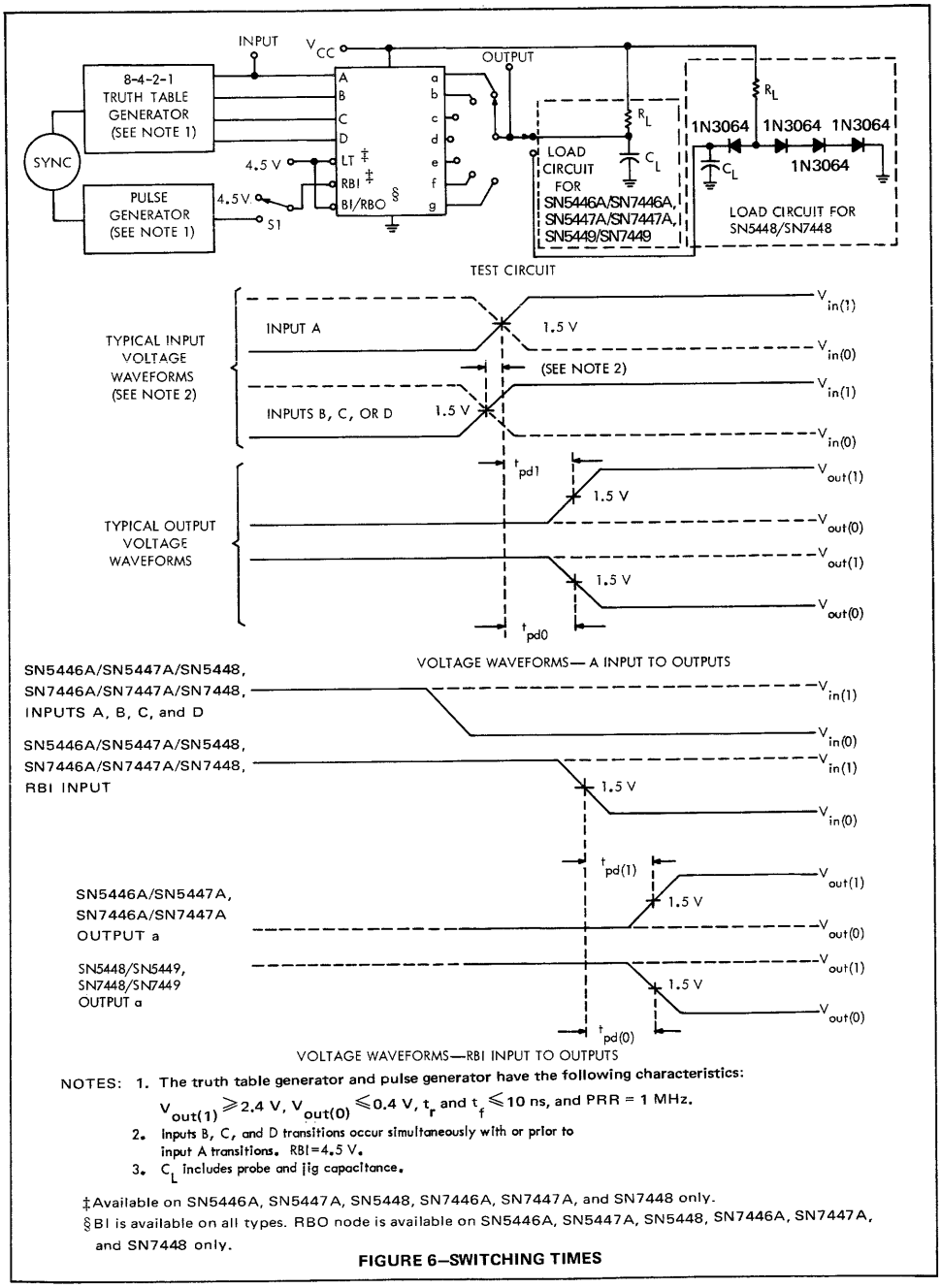
FIGURE 5

†Arrows indicate actual direction of current flow. Logic symbol used is representative for all types.
‡Available on SN5446A, SN5447A, SN5448, SN7446A, SN7447A, and SN7448 only.
§BI is available on all types. RBO node is available on SN5446A, SN5447A, SN5448, SN7446A, SN7447A, and SN7448 only.

9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



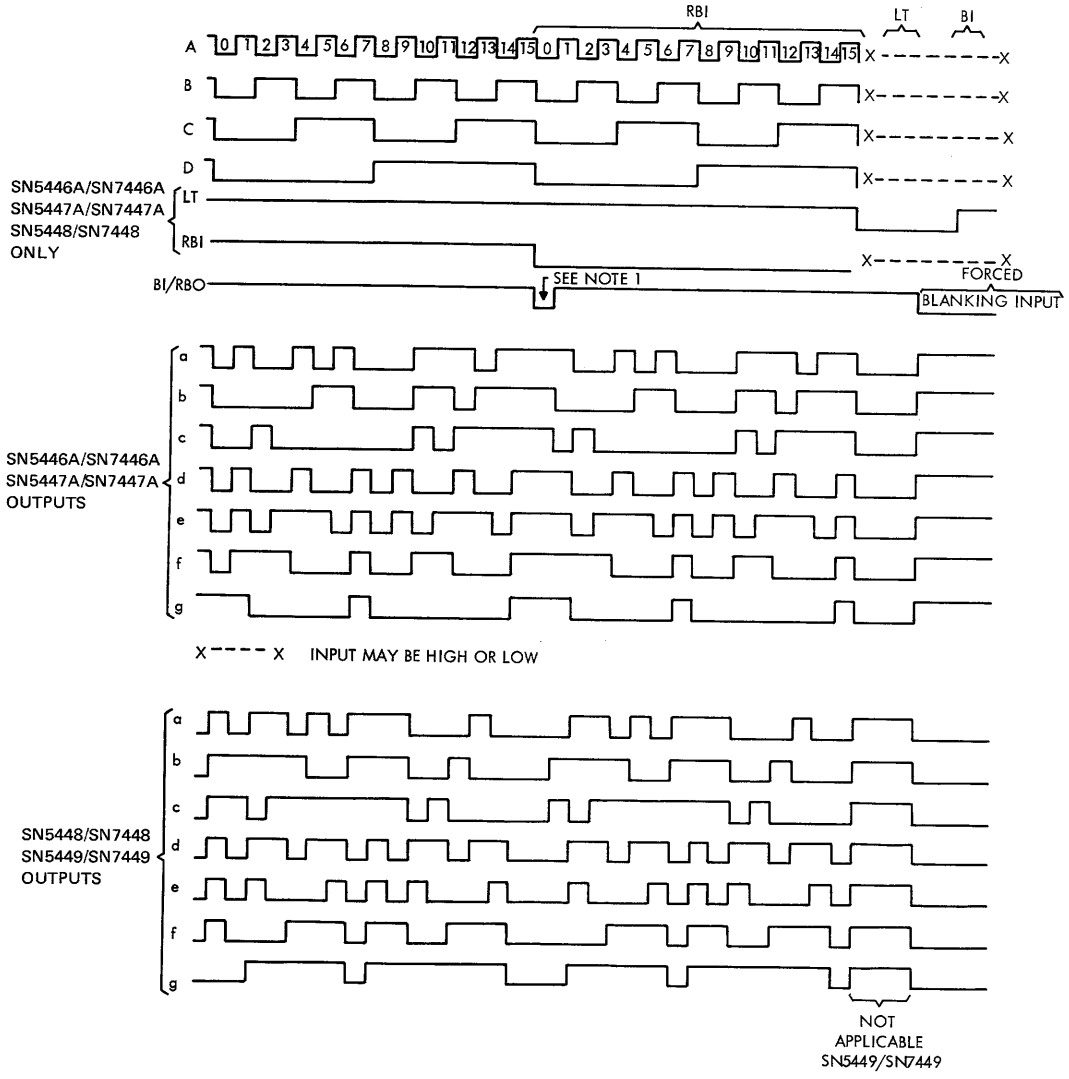
NOTES: 1. The truth table generator and pulse generator have the following characteristics: $V_{out(1)} \geq 2.4$ V, $V_{out(0)} \leq 0.4$ V, t_r and $t_f \leq 10$ ns, and PRR = 1 MHz.
2. Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions. RBI=4.5 V.
3. C_L includes probe and jig capacitance.

‡Available on SN5446A, SN5447A, SN5448, SN7446A, SN7447A, and SN7448 only.
§BI is available on all types. RBO node is available on SN5446A, SN5447A, SN5448, SN7446A, SN7447A, and SN7448 only.

FIGURE 6—SWITCHING TIMES

9

TYPICAL INPUT/OUTPUT VOLTAGE WAVEFORMS



NOTE 1: For the SN5446A, SN5447A, SN5448, SN7446A, SN7447A, and SN7448 this logical 0 represents the RBO response. For the SN5449 and SN7449 a logical 0 pulse is applied to the blanking input.

9

APPLICATIONS DATA

driving indicators directly (see Figure B)

This application demonstrates how the SN5446A or SN5447A may be used to drive seven-segment indicators directly. The output transistors of these two circuit types will sink up to 40 milliamperes of current; therefore, external components are not required.

Also illustrated is how the quadruple latch (SN5475) and decade counter (SN5490) may be utilized to acquire and store the numeral to be displayed. The method shown is typical of a single stage and a number of methods are possible for distributing the BCD data from the decade counter to the quadruple latch.

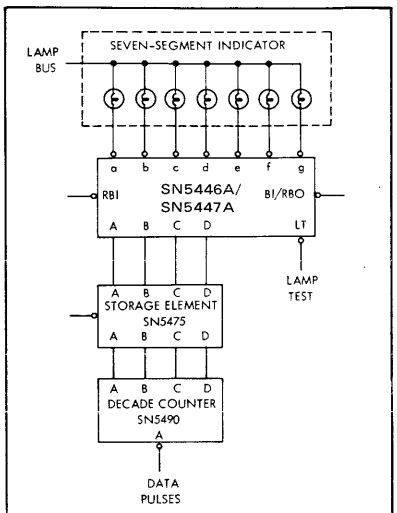


FIGURE B

n-digit display with leading-and trailing-edge blanking (see Figure C)

This application demonstrates a method for driving incandescent, seven-segment, display indicators directly from the output of the SN5446A, or SN5447A decoder with provisions for leading-edge and trailing-edge zero-blanking, intensity control, and lamp test.

Leading-edge and trailing-edge zero blanking is illustrated for a six-digit mixed integer with zero indications suppressed for the two most-significant decades (MSD) of the whole number and the two least-significant decades (LSD). This scheme causes the number to be displayed in its easily identified, common form. Blanking is accomplished by grounding RBI inputs of most-significant and least-significant decades and interconnecting the BI/BRO nodes of these two decades to the ripple-blanking inputs of the adjacent decades. This improves readability by inhibiting suppression of zeros occurring on either side of the decimal point. The ripple-blanking inputs of the decades on either side of the fixed decimal point are inhibited by connecting to a 5-volt d-c source.

Intensity control is accomplished at all six of the decoder/drivers by modulating the blanking input with a multivibrator. Best results are obtained with a modulation source in which the duty cycle can be varied. Individual drivers are required as they are wire-OR connected with the ripple-blanking functions.

As the lamp-test input is only one load, a number (up to ten) of these may be driven from a single Series 54/74 circuit.

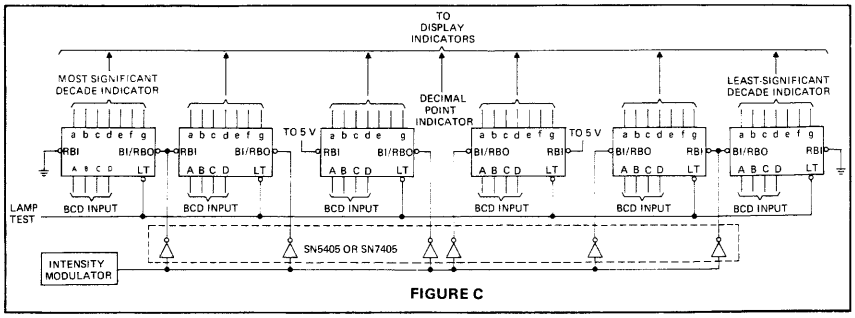


FIGURE C

APPLICATIONS DATA

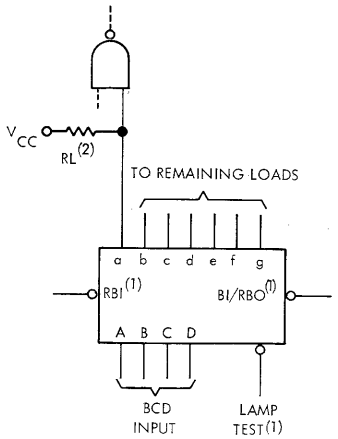
driving logic circuits (see Figure D)

These decoder/drivers may be used to drive other logic circuits. (See Figure D.) Value of the pull-up resistor (required on the open-collector outputs) may be calculated using the methods given for the SN5401 open-collector NAND gate.

driving buffer transistors (see Figures E and F)

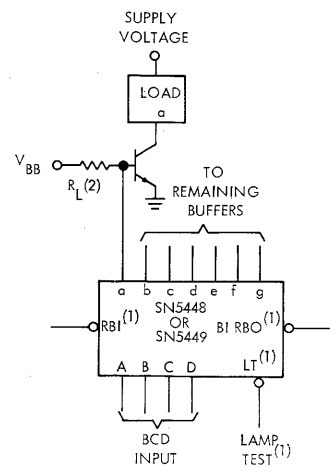
For applications requiring increased drive currents these decoder/drivers may be used with discrete drivers. A universal method of supplying base drive for a buffer transistor is illustrated in Figure E. Value of the base resistor (required on the open-collector outputs) may be calculated using the methods similar to those given for the SN5401 open-collector NAND gate. Increased base drive from the SN5448 is possible with the employment of external base resistor.

Circuitry for employing SCR's to drive electro-luminescent displays is illustrated in Figure F.



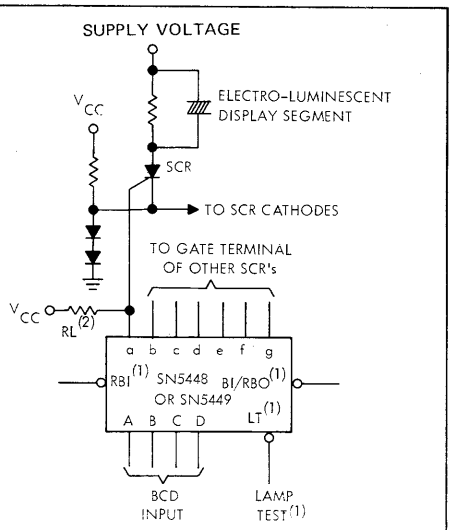
1. Available on SN5446A, SN5447A, SN5448, SN7446A, SN7447A, and SN7448 only.
2. Pull-up resistor is required with SN5446A, SN5447A, SN5449, SN7446A, SN7447A or SN7449, and is optional with SN5448 or SN7448.

FIGURE D



1. Available on SN5448 and SN7448 only.
2. Pull-up resistor is required with SN5449 or SN7449, and is optional with SN5448 or SN7448.

FIGURE E



1. Available on SN5448 and SN7448 only.
2. Pull-up resistor is required with SN5449 or SN7449, and is optional with SN5448 or SN7448.

FIGURE F

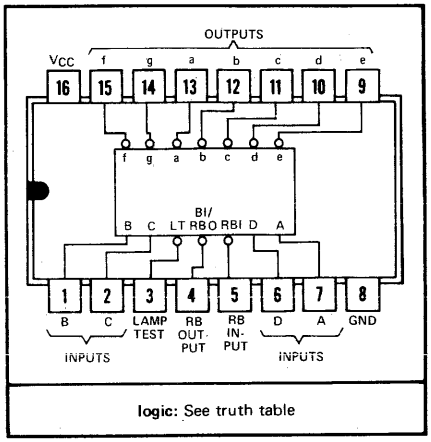
9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54L46, SN54L47, SN74L46, SN74L47
BCD-TO-SEVEN-SEGMENT DECODER/DRIVERS

- Direct Drive for Indicators
- Open-Collector Outputs
- Lamp-Test Provision
- Lamp Intensity Modulation Capability
- Full Decoding of All 16 Input Combinations
- Leading/Trailing Zero Suppression
- Fully Compatible with Most TTL and DTL Circuits
- Low Power Dissipation . . . 133 mW Typical

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: See truth table

description

These monolithic, TTL, BCD-to-seven-segment decoder/drivers consist of NAND gates, input buffers, and seven AND-OR-INVERT gates. These devices offer high-sink-current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make binary-coded-decimal (BCD) data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test blanking input/ripple-blanking output, and ripple-blanking inputs.

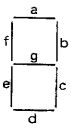
These circuits accept four-bit BCD data and, depending on the levels at the auxiliary inputs, decode this data to drive seven-segment display indicators. The output states, as well as conditions required at the auxiliary inputs, are shown in the truth table. The output circuitry is designed to withstand the relatively high voltages required for seven-segment indicators. The SN54L46/SN74L46 outputs will withstand 30 volts, and the SN54L47/SN74L47 outputs will withstand 15 volts, with a maximum reverse current of 250 microamperes. Indicator segments requiring up to 20 milliamperes of current may be driven directly from the outputs. Segment identification with resultant displays are shown in the figure on the following page. Display patterns for binary input counts above nine are unique symbols to authenticate input conditions.

These devices contain an overriding blanking input (BI) which can be used to control the lamp intensity (See Figure B of typical application data) or to inhibit the outputs. They also incorporate leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) may be performed at any time when the BI/RBO node is at a high level. All inputs except the BI/RBO node are one-half of one normalized Series 54/74 load, or approximately five Series 54L/74L gate loads at a low logic level, two Series 54L/74L gate loads at a high logic level. The SN54L46 and SN54L47 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L46 and SN74L47 are characterized for operation from 0°C to 70°C.

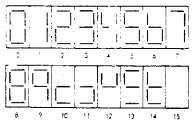
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TRUTH TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	1
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4



SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the state of any other input condition.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Peak output current ($t_w \leq 1$ ms, duty cycle $\leq 10\%$) . . . . . 200 mA
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN54L46, SN54L47 Circuits . . . . . −55°C to 125°C
SN74L46, SN74L47 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54L46, SN54L47			SN74L46, SN74L47			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$, outputs a thru g	SN54L46, SN74L46			30			30	V
	SN54L47, SN74L47			15			15	
On-state output current, $I_{O(on)}$	a thru g			20			20	mA
Low-level output current, I_{OL}	BI/RBO			4			4	
Operating free-air temperature, T_A		−55		125	0		70	C

9

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage		1 and 2		2		V
V_{IL}	Low-level input voltage		1 and 2			0.8	V
V_I	Input clamp voltage		3	V_{CC} = MIN, I_I = −12 mA		−1.5	V
V_{OH}	High-level output voltage	BI/RBO	1	V_{CC} = MIN, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	BI/RBO	2	V_{CC} = MIN, I_{OL} = 4 mA		0.4	V
$I_{O(off)}$	Off-state output current	a thru g	1	V_{CC} = MAX, $V_{O(off)}$ = MAX		250	μA
$V_{O(on)}$	On-state output voltage	a thru g	2	V_{CC} = MIN, $I_{O(on)}$ = 20 mA		0.4	V
I_I	Input current at maximum input voltage	any input except BI/RBO	4	V_{CC} = MAX, V_I = 5.5 V		1	mA
I_{IH}	High-level input current	any input except BI/RBO	4	V_{CC} = MAX, V_I = 2.4 V		20	μA
I_{IL}	Low-level input current	any input except BI/RBO	3	V_{CC} = MAX, V_I = 0.4 V		−0.8	mA
		BI/RBO				−2.1	
I_{OS}	Short-circuit output current	BI/RBO	5	V_{CC} = MAX		−4	mA
I_{CC}	Supply current	SN54L46, SN54L47	6	V_{CC} = MAX		43	mA
		SN74L46, SN74L47				52	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

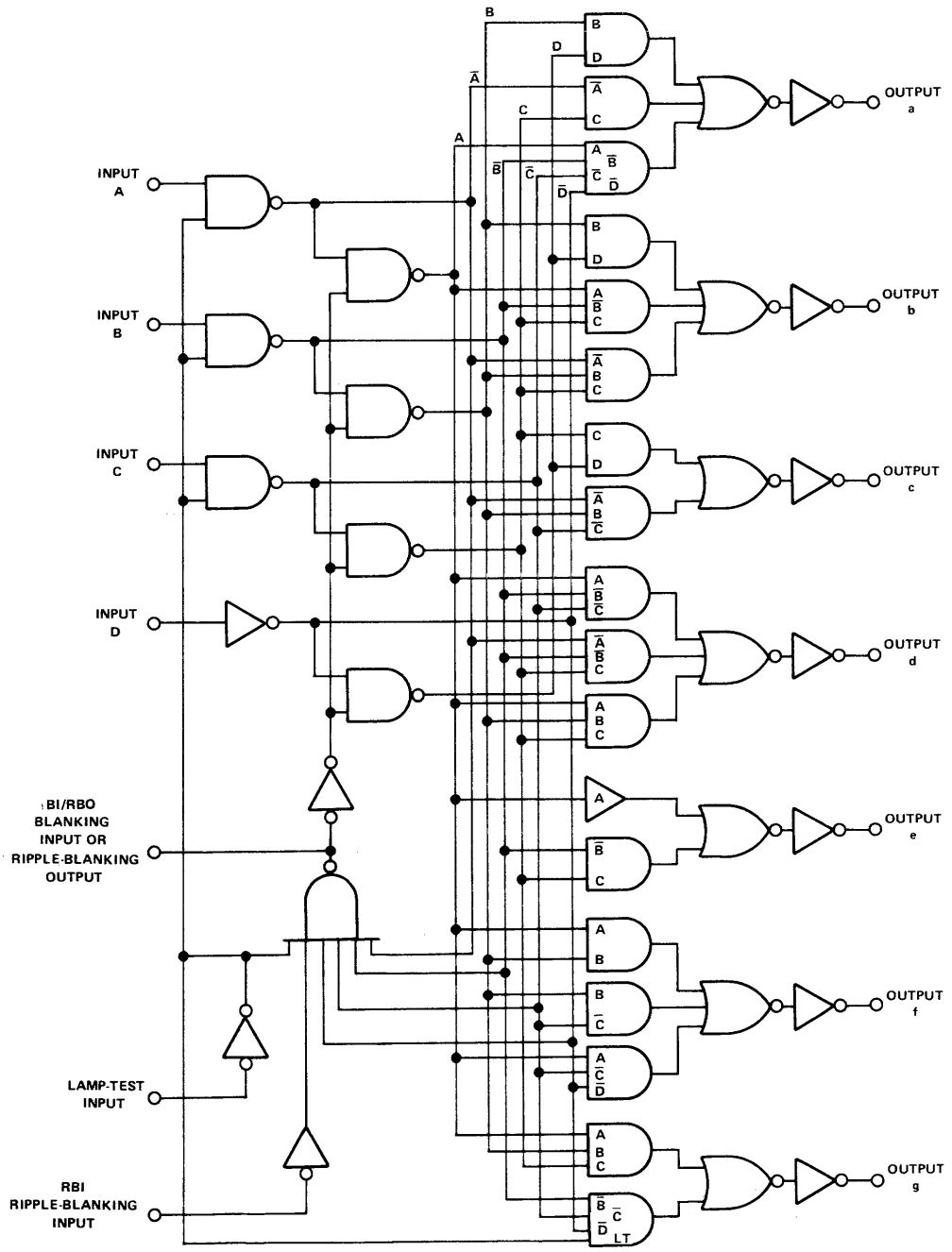
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{off}	Turn-off time from A input	7	C_L = 15 pF, R_L = 280 Ω		200	ns
t_{on}	Turn-on time from A input				200	ns
t_{off}	Turn-off time from RBI input				200	ns
t_{on}	Turn-on time from RBI input				200	ns

9

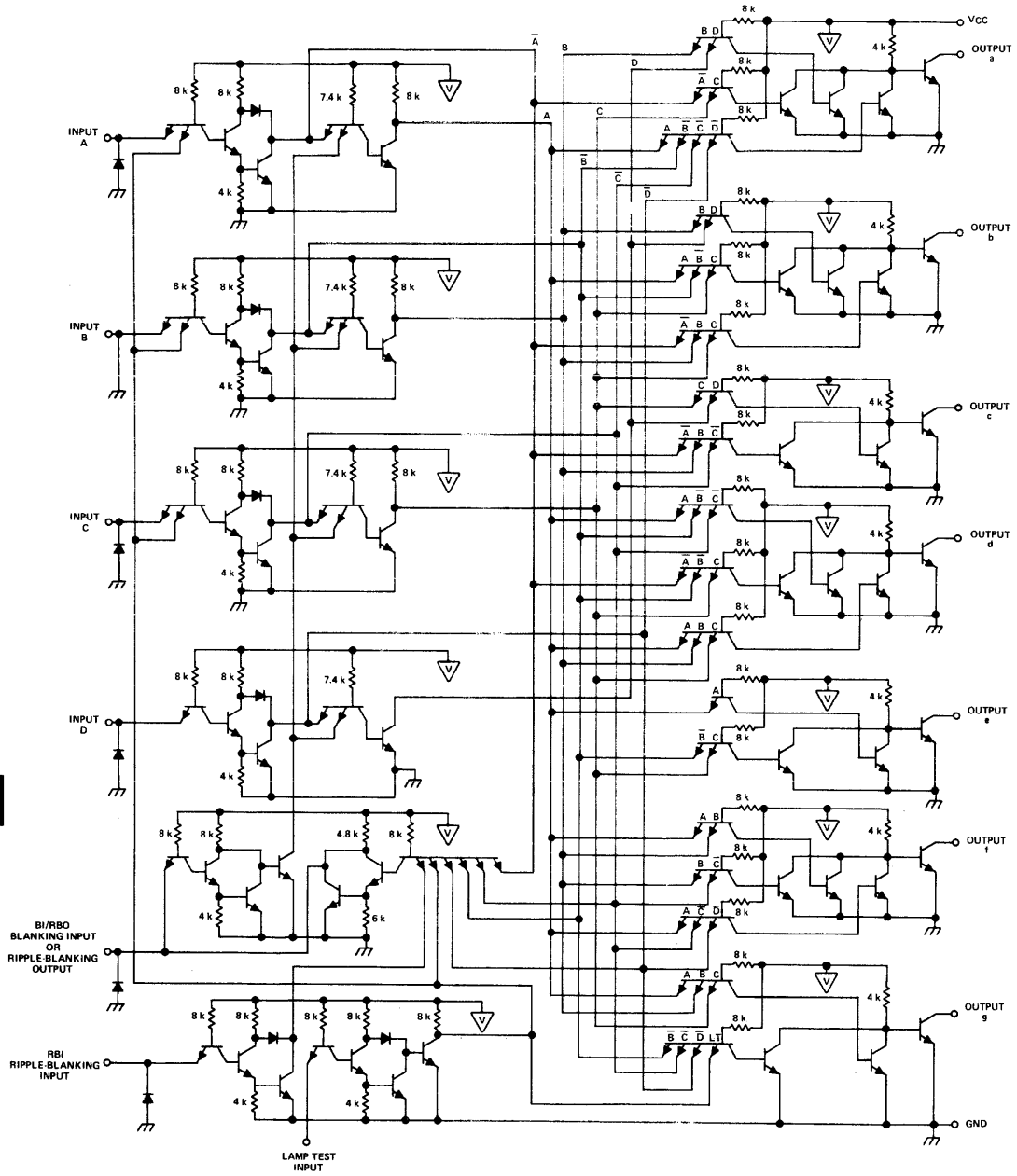
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram



9

schematic diagram



Resistor values shown are nominal in ohms.
▽ ...V_{CC} bus

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

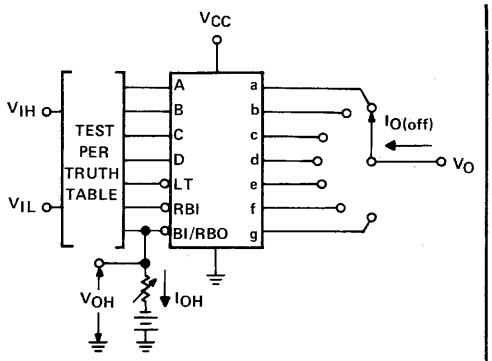


FIGURE 1

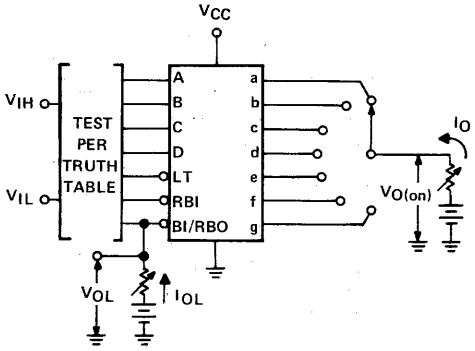
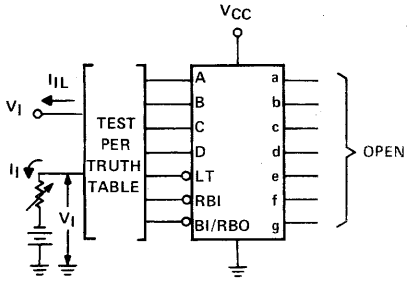
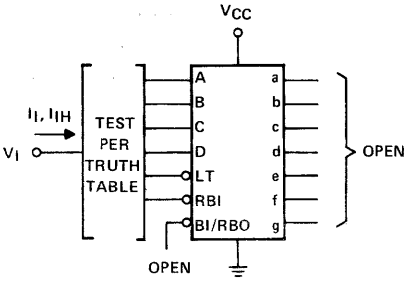


FIGURE 2



Each input is tested separately.

FIGURE 3



Each input is tested separately.

FIGURE 4

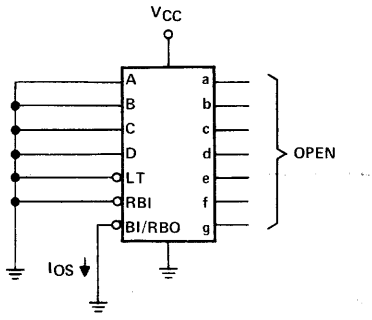


FIGURE 5

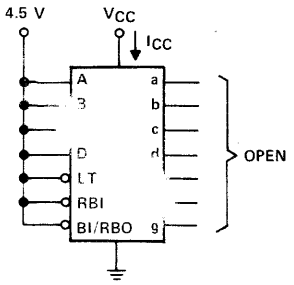


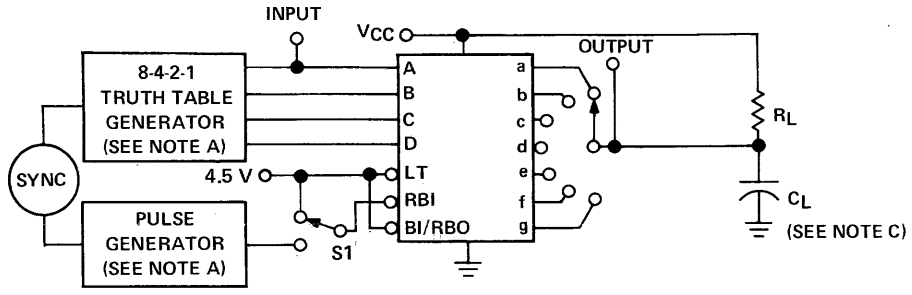
FIGURE 6

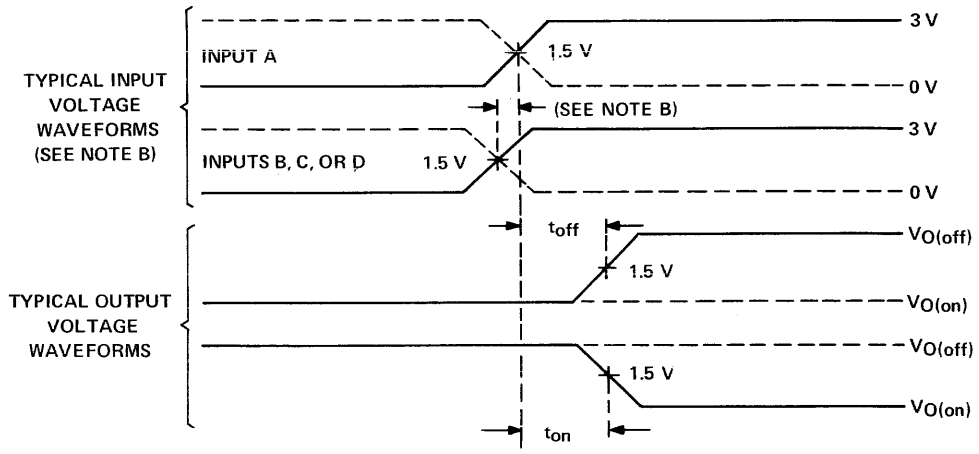
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

9

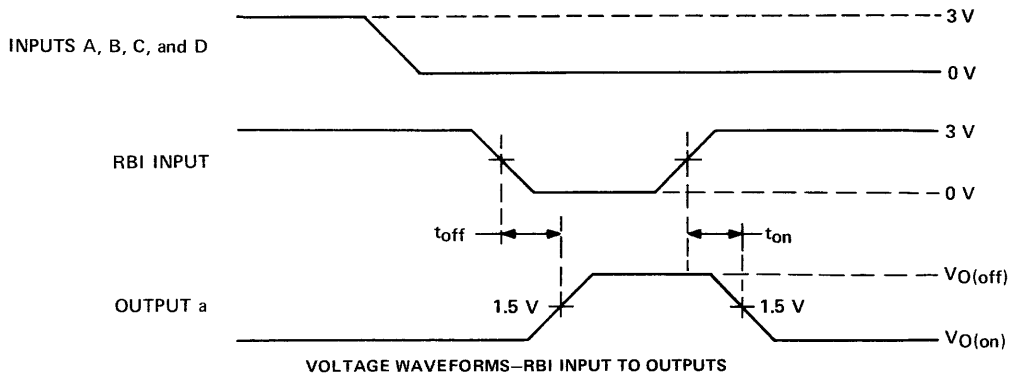
PARAMETER MEASUREMENT INFORMATION

switching characteristics





VOLTAGE WAVEFORMS—A INPUT TO OUTPUTS



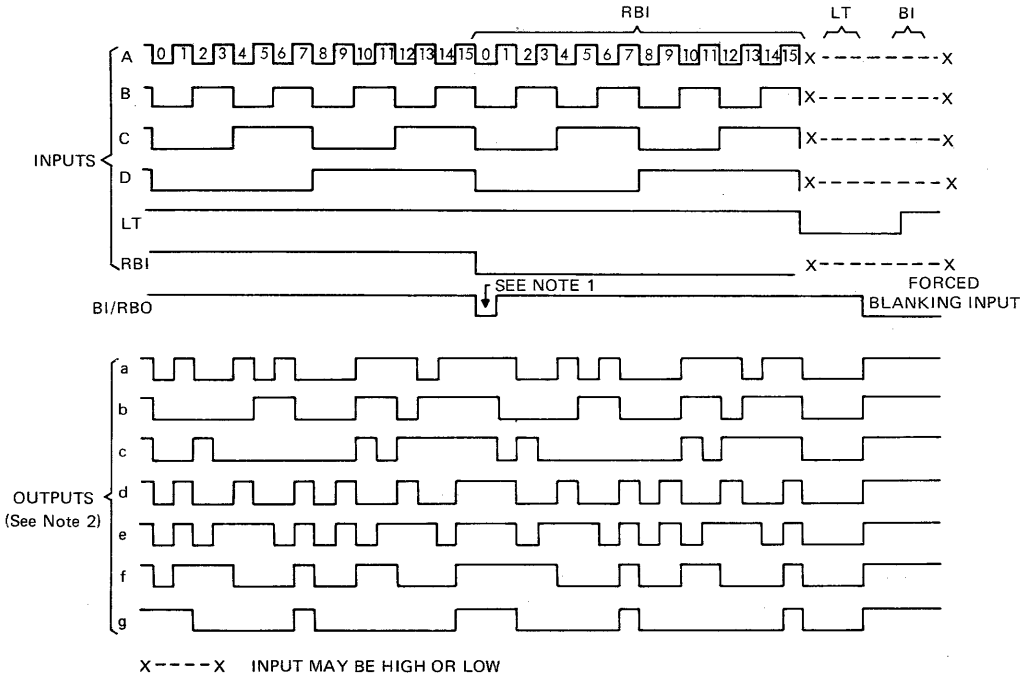
VOLTAGE WAVEFORMS—RBI INPUT TO OUTPUTS

NOTES: A. The truth table generator and pulse generator have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, and PRR ≤ 1 MHz, $Z_{out} = 50\ \Omega$.
B. Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions. RBI = 4.5 V.
C. C_L includes probe and jig capacitance.

FIGURE 7—SWITCHING TIMES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL INPUT/OUTPUT VOLTAGE WAVEFORMS



NOTES: 1. This low-level pulse represents the RBO response.
2. For the outputs, a high level indicates the off state and a low level represents the on state.

TYPICAL APPLICATION DATA

driving indicators directly (see Figure A)

This application demonstrates how the SN54L46 or SN54L47 may be used to drive seven-segment indicators directly. The output transistors of these two circuit types will sink up to 20 milliamperes of current; therefore, external components are not required.

Also illustrated is how the quadruple latch (SN5475) and decade counter (SN54L90) may be utilized to acquire and store the numeral to be displayed. The method shown is typical of a single stage and a number of methods are possible for distributing the BCD data from the decade counter to the quadruple latch.

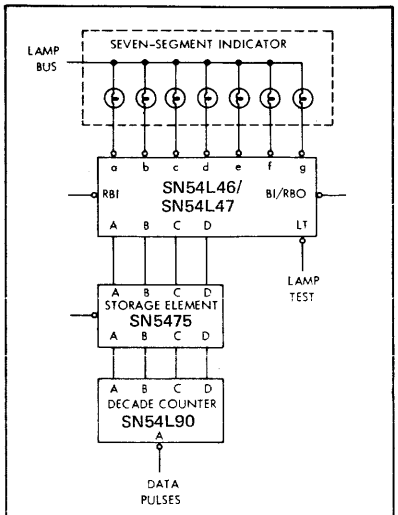


FIGURE A

n-digit display with leading and trailing-edge blanking (see Figure B)

This application demonstrates a method for driving seven-segment incandescent display indicators directly from the output of the SN54L46, or SN54L47 decoder with provisions for leading-edge and trailing-edge zero-blanking, intensity control, and lamp test.

Leading-edge and trailing-edge zero blanking is illustrated for a six-digit mixed integer with zero indications suppressed for the two most-significant decades (MSD) of the whole number and the two least-significant decades (LSD). This scheme causes the number to be displayed in its easily identified, common form. Blanking is accomplished by grounding RBI inputs of most-significant and least-significant decades and interconnecting the BI/BRO nodes of these two decades to the ripple-blanking inputs of the adjacent decades. This improves readability by inhibiting suppression of zeros occurring on either side of the decimal point. The ripple-blanking inputs of the decades on either side of the fixed decimal point are inhibited by connecting to a 5-volt d-c source.

9

Intensity control is accomplished at all six of the decoder/drivers by modulating the blanking input with a multivibrator. Best results are obtained with a modulation source in which the duty cycle can be varied. Individual drivers are required as they are wire-OR connected with the ripple blanking functions.

As the lamp-test input is only one load, any number of these (up to 20) may be driven from a single Series 54/74 circuit.

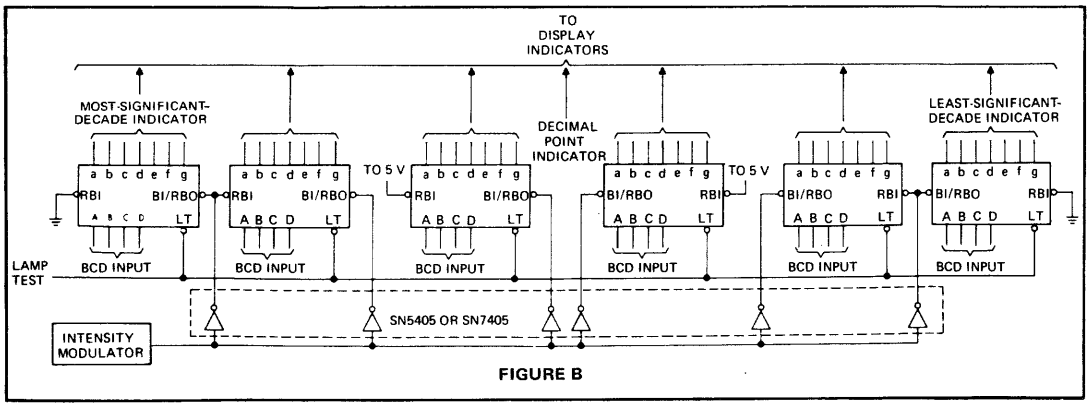


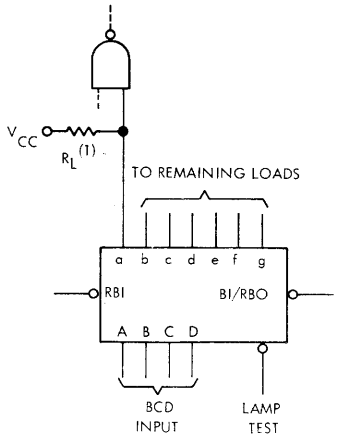
FIGURE B

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATION DATA

driving logic circuits (see Figure C)

These decoder/drivers may be used to drive other logic circuits. (See Figure C.) Value of the pull-up resistor (required on the open-collector outputs) may be calculated using the methods given for the SN54L01 open-collector NAND gate.



Pull-up resistor is required with open-collector outputs.

FIGURE C

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE SN74141
BCD-TO-DECIMAL DECODER/DRIVER

- Drives gas-filled cold-cathode indicator tubes directly
- Fully decoded inputs ensure all outputs are off for invalid codes
- Input clamping diodes minimize transmission-line effects
- Power dissipation typically 55 mW

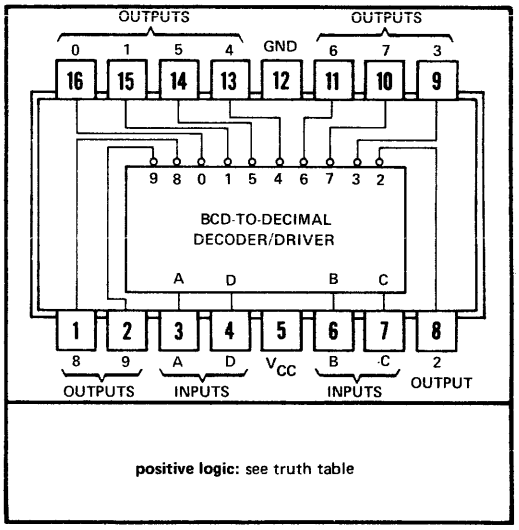
logic

TRUTH TABLE

INPUT				OUTPUT
D	C	B	A	ON†
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	NONE
H	L	H	H	NONE
H	H	L	L	NONE
H	H	L	H	NONE
H	H	H	L	NONE
H	H	H	H	NONE

H = high level, L = low level
†All other outputs are off

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

The SN74141 is a second-generation BCD-to-decimal decoder designed specifically to drive cold-cathode indicator tubes. This decoder demonstrates an improved capability to minimize switching transients in order to maintain a stable display.

Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the SN74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display as shown in the typical application data. The ten high-performance, n-p-n output transistors have a maximum reverse current of 50 microamperes at 55 volts.

Low-forward-impedance diodes are also provided for each input to clamp negative-voltage transitions in order to minimize transmission-line effects. Power dissipation is typically 55 milliwatts, which is about one-half the power requirement of earlier designs. The SN74141 is characterized for operation over the temperature range of 0°C to 70°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Current into any output (off-state) . . . . . 2 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage V_{CC} (see Note 1)	4.75	5	5.25	V
Output voltage (see Notes 1 and 2)			65	V
Operating free-air temperature range	0	25	70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

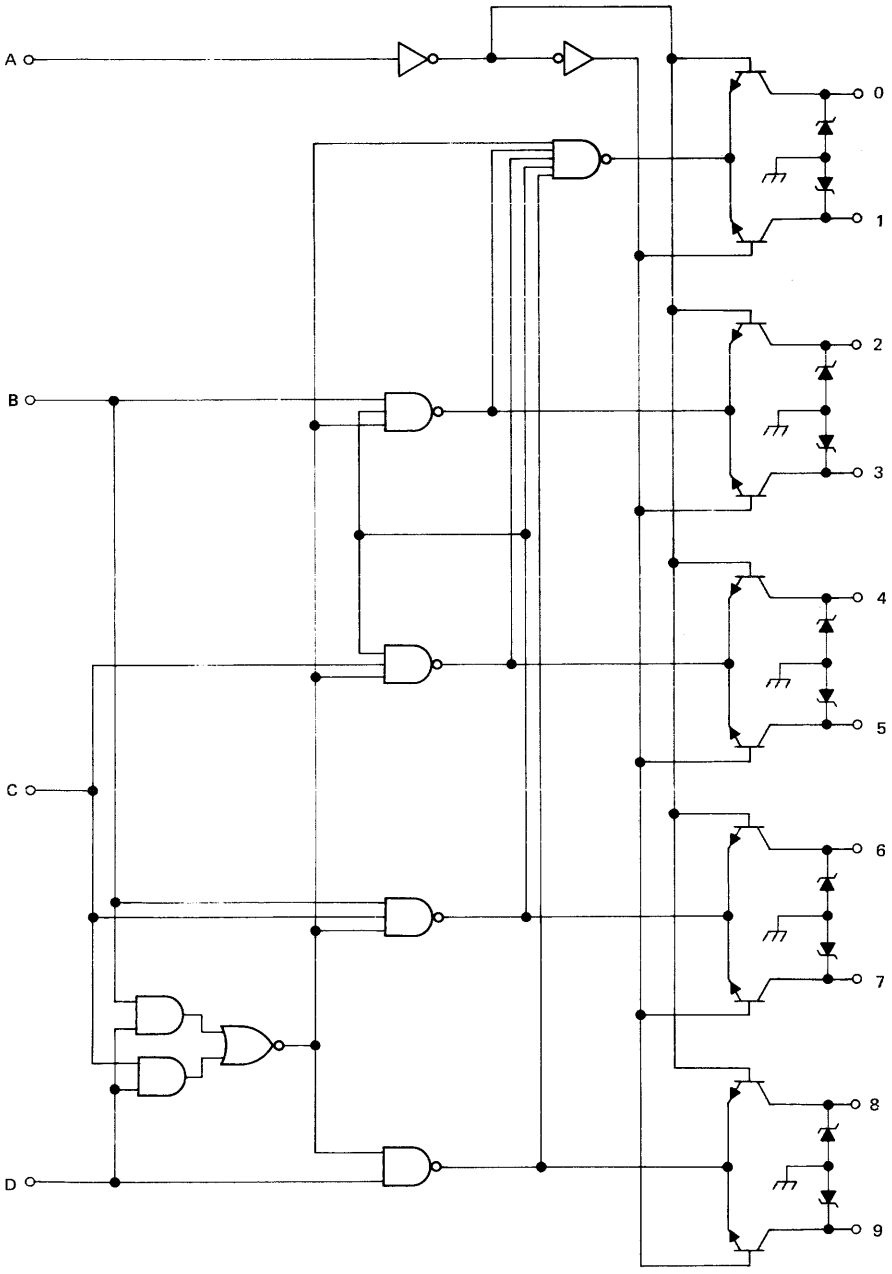
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2		2			V
V_{IL}	Low-level input voltage	1 and 2				0.8	V
$V_{O(on)}$	On-state output voltage	1	V_{CC} = MIN, I_O = 7 mA			2.5	V
$V_{O(off)}$	Off-state output voltage for input counts 0 thru 9	2	V_{CC} = MAX, I_O = 0.5 mA	60			V
$I_{O(off)}$	Off-state reverse current	2	V_{CC} = MAX, V_O = 55 V			50	μA
$I_{O(off)}$	Off-state reverse current for input counts 10 thru 15	2	V_{CC} = MAX, V_O = 30 V			5	μA
I_{IH}	High-level input current at A	3	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current at B, C, or D	3	V_{CC} = MAX, V_I = 2.4 V			80	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current into A	4	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{IL}	Low-level input current into B, C, or D					−3.2	mA
I_{CC}	Supply current	3	V_{CC} = MAX		16	25	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡This typical value is at V_{CC} = 5 V, T_A = 25°C.

9

CIRCUIT TYPE SN74141
BCD-TO-DECIMAL DECODER/DRIVER

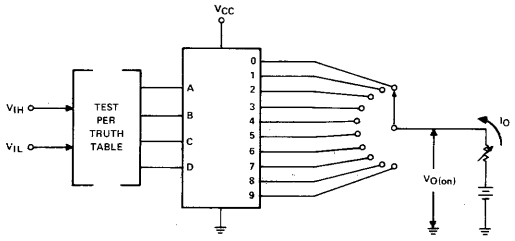
functional block diagram



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

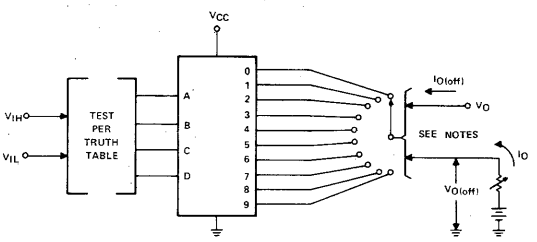
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



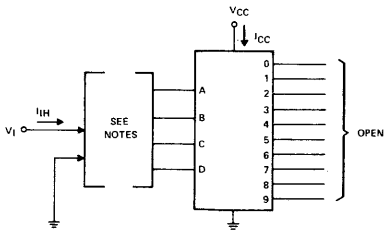
Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, $V_{O(on)}$



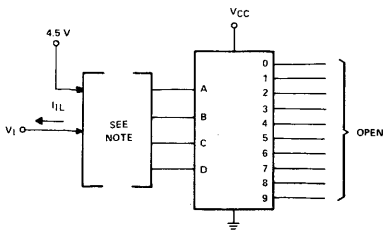
A. Each output is tested separately.
B. $V_{O(off)}$ is tested at I_O = 0.5 mA and $I_{O(off)}$ is tested at V_O = 55 V for all input counts. $I_{O(off)}$ is tested also at V_O = 30 V for input counts 10 through 15.

FIGURE 2–V_{IH}, V_{IL}, $I_{O(off)}$, $V_{O(off)}$



A. When testing I_{IH}, each input is tested separately with all other inputs grounded.
B. When testing I_{CC}, all inputs are grounded.

FIGURE 3–I_{IH}, I_{CC}



Each input is tested separately, with all other inputs at 4.5 V.

FIGURE 4–I_{IL}

§ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

9

CIRCUIT TYPE SN74141
BCD-TO-DECIMAL DECODER/DRIVER

TYPICAL APPLICATION DATA

general

When these decoder/drivers are used in close proximity (on the same circuit board) with standard digital integrated circuits, care should be exercised to ensure that the impedance of the ground bus (including interconnections) is sufficiently low to absorb the normal energy levels resulting from switching the tube elements.

driving indicator tubes

As shown in figure A, the SN74141 requires no external components for driving cold-cathode indicator tubes. The versatility here is limited only by the system capability to control the data inputs.

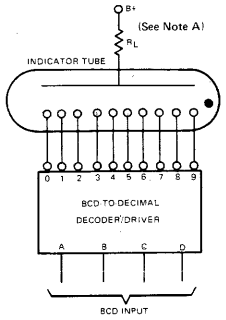


FIGURE A

A suggested method for blanking extraneous zeros is shown in figure B. Any input count above decimal 9 may be used for blanking. In the following application decimal 12 is used. When the most-significant bit (MSB) or the least-significant bit (LSB) is decimal 0(0000), that indicator is blanked while decimal 12 (binary 1100) is applied to the SN74141 inputs causing all the outputs to be off. If the MSB or LSB is decimal 0 and being blanked, this signal is gated with and blanks the next smaller digit. This scheme is easily expandable to n-digits.

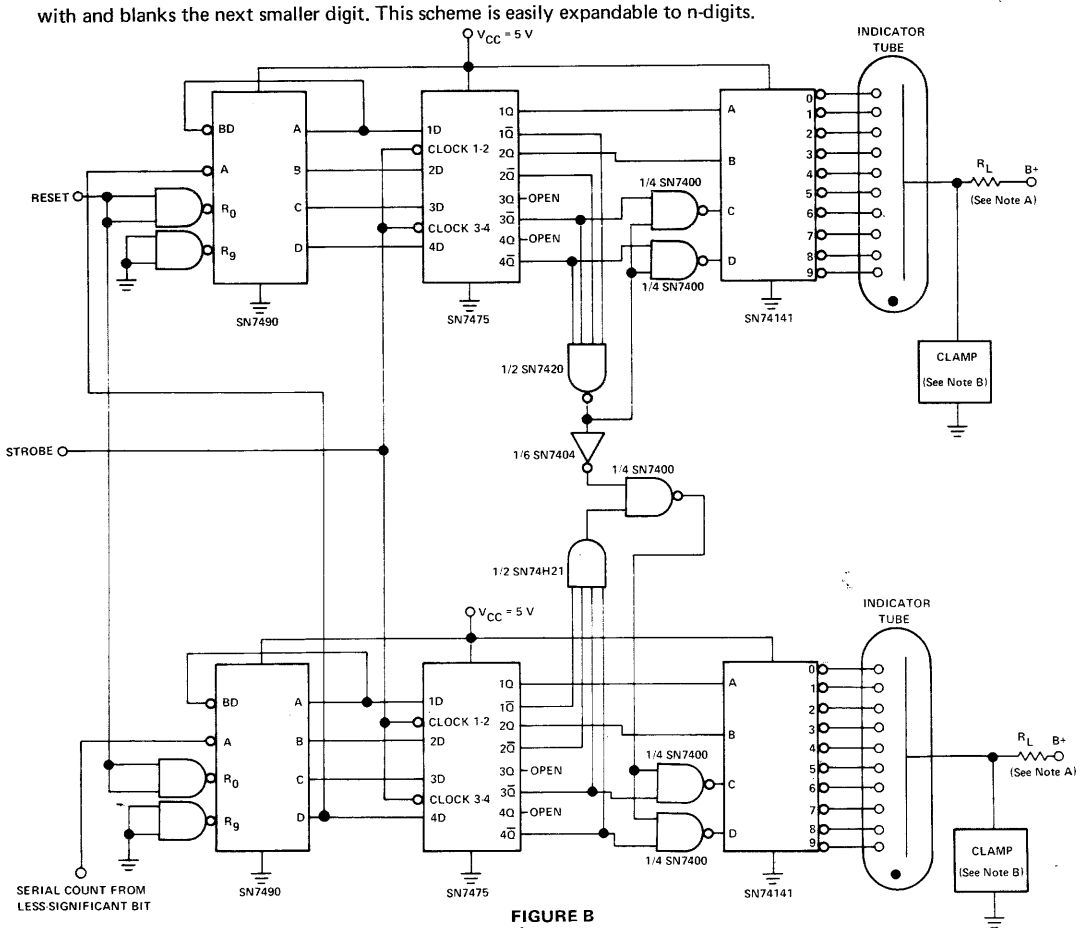


FIGURE B

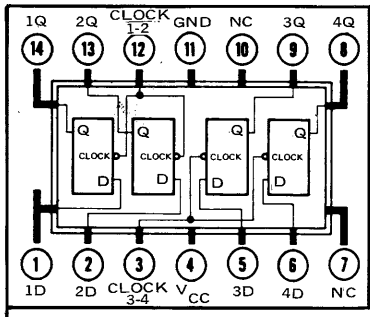
NOTES: A. Values for B+ and R_L are as specified by the tube manufacturer.
B. Blanking is assured only if the anode of the indicator tube is clamped at 150 volts maximum.

9

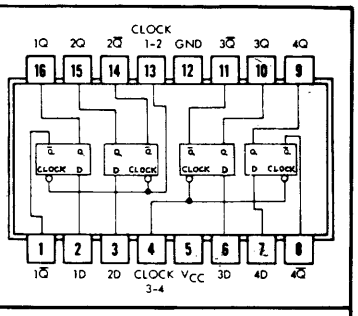
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5475, SN5477, SN54100, SN7475, SN7477, SN74100
8-BIT AND 4-BIT BISTABLE LATCHES

SN5477/SN7477
W FLAT PACKAGE
(TOP VIEW)



SN5475/SN7475
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see truth table

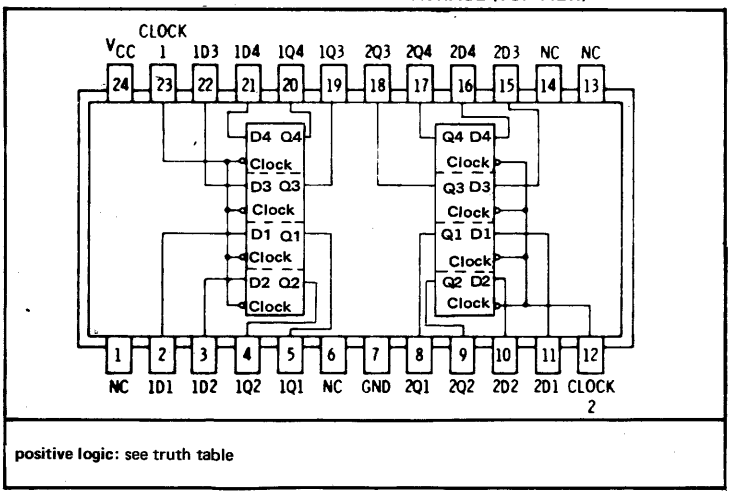
logic

TRUTH TABLE (Each Latch)	
t_n	t_{n+1}
D	Q
1	1
0	0

NOTES: 1. t_n = bit time before clock negative-going transition.
2. t_{n+1} = bit time after clock negative-going transition.

NC—No internal connection

SN54100/SN74100
J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see truth table

†Pin assigments for these circuits are the same for all packages

description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

The SN5475/SN7475 features complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and is available in the 16-pin packages. For higher component density applications the SN5477/SN7477 4-bit latch is available in the 14-pin flat package. The SN54100/SN74100 features two independent quadruple latches in a single 24-pin dual-in-line package.

These circuits are completely compatible with all popular TTL or DTL families. Typical power dissipation is 40 milliwatts per latch. The Series 54 circuits are characterized for operation over the full military temperature range of −55°C to 125°C and Series 74 circuits are characterized for operation from 0°C to 70°C.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage, V_{CC} (See Note 3) . . . . . 7 V
Input Voltage, V_{in} (See Notes 3 and 4) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5475 Circuits . . . . . −55°C to 125°C
SN7475 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3): SN5475, SN5477, SN54100	4.5	5	5.5	V
SN7475, SN7477, SN74100	4.75	5	5.25	V
Normalized Fan-Out From Outputs			10	

NOTE: 3. These voltages are with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	1 and 2	V_{CC} = MIN, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1 and 2	V_{CC} = MIN, I_{sink} = 16 mA				0.4	V
$I_{in(0)}$	Logical 0 level input current at D	3	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	3	V_{CC} = MAX,	SN5475, SN5477, SN7475, SN7477			−6.4	mA
				SN54100, SN74100			−12.8	mA
$I_{in(1)}$	Logical 1 level input current at D	3	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at clock	3	V_{CC} = MAX,	SN5475, SN5477, SN7475, SN7477			160	μA
			V_{in} = 2.4 V,	SN54100, SN74100			320	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX, V_{out} = 0	SN5475, SN5477, SN54100	−20		−57	mA
				SN7475, SN7477, SN74100	−18		−57	mA
I_{CC}	Supply current	5	V_{CC} = MAX,	SN5475, SN5477		32	46	mA
				SN54100		64	92	mA
				SN7475, SN7477		32	53	mA
				SN74100		64	106	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

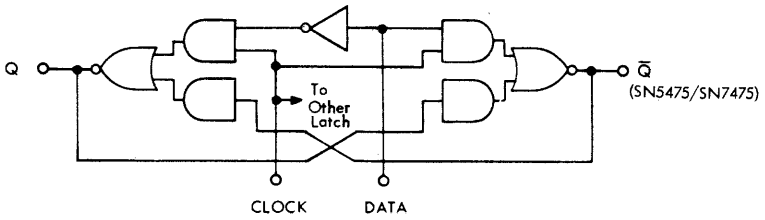
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

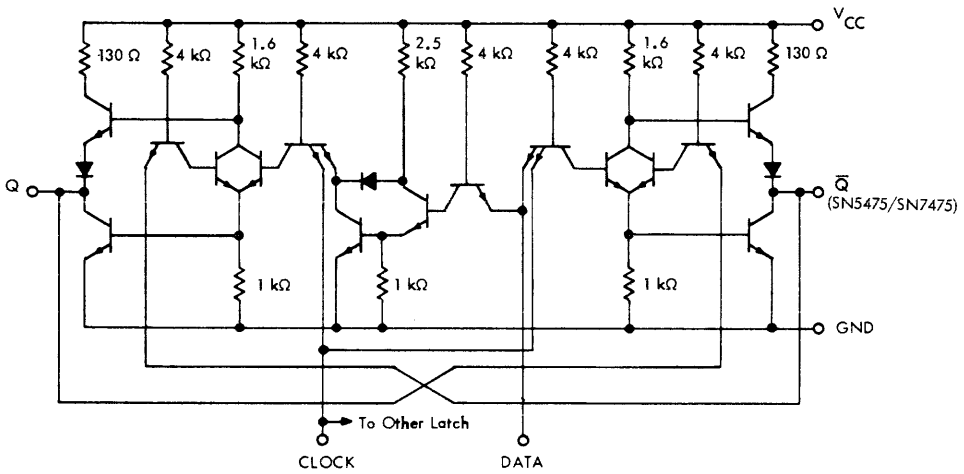
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{setup1}	Minimum logical 1 level input setup time at D input	6	C_L = 15 pF, R_L = 400 Ω		7	20	ns
t_{setup0}	Minimum logical 0 level input setup time at D input	6	C_L = 15 pF, R_L = 400 Ω		14	20	ns
t_{hold1}	Maximum logical 1 level input hold time required at D input	6	C_L = 15 pF, R_L = 400 Ω	0	15¶		ns
t_{hold0}	Maximum logical 0 level input hold time required at D input	6	C_L = 15 pF, R_L = 400 Ω	0	6¶		ns
$t_{pd1(D-Q)}$	Propagation delay time to logical 1 level from D input to Q output	6	C_L = 15 pF, R_L = 400 Ω		16	30	ns
$t_{pd0(D-Q)}$	Propagation delay time to logical 0 level from D input to Q output	6	C_L = 15 pF, R_L = 400 Ω		14	25	ns
$t_{pd1(D-\bar{Q})}$	Propagation delay time to logical 1 level from D input to $\bar{Q}$ output (SN5475, SN7475)	6	C_L = 15 pF, R_L = 400 Ω		24	40	ns
$t_{pd0(D-\bar{Q})}$	Propagation delay time to logical 0 level from D input to $\bar{Q}$ output (SN5475, SN7475,	6	C_L = 15 pF, R_L = 400 Ω		7	15	ns
$t_{pd1(C-Q)}$	Propagation delay time to logical 1 level from clock input to Q output	6	C_L = 15 pF, R_L = 400 Ω		16	30	ns
$t_{pd0(C-Q)}$	Propagation delay time to logical 0 level from clock input to Q output	6	C_L = 15 pF, R_L = 400 Ω		7	15	ns
$t_{pd1(C-\bar{Q})}$	Propagation delay time to logical 1 level from clock input to $\bar{Q}$ output (SN5475, SN7475)	6	C_L = 15 pF, R_L = 400 Ω		16	30	ns
$t_{pd0(C-\bar{Q})}$	Propagation delay time to logical 0 level from clock input to $\bar{Q}$ output (SN5475, SN7475)	6	C_L = 15 pF, R_L = 400 Ω		7	15	ns

¶ These typical times indicate that period occurring prior to the fall of clock pulse (t_0) below 1.5 V when data at the D input will still be recognized and stored.

functional block diagram (each latch)



schematic (each latch)

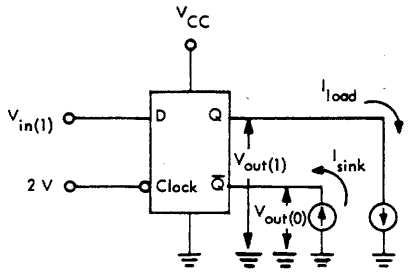


Component values shown are nominal.

9

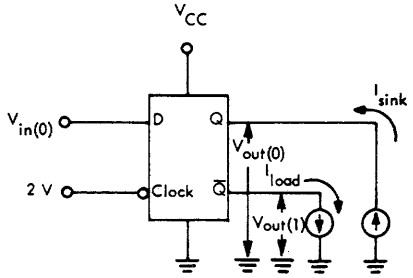
PARAMETER MEASUREMENT INFORMATION

d-c test circuits †



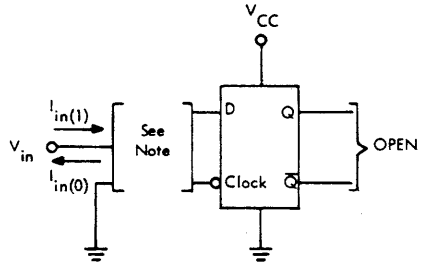
1. Each latch is tested separately.

FIGURE 1



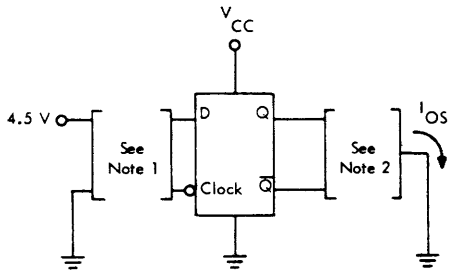
1. Each latch is tested separately.

FIGURE 2



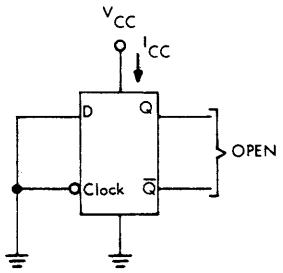
1. Each input is tested separately.
2. When testing $I_{in(1)}$ at D ground clock.
3. When testing $I_{in(1)}$ at clock ground all D inputs.

FIGURE 3



1. Input conditions are in accordance with truth table.
2. Each latch and each output is tested separately.

FIGURE 4



1. All latches are tested simultaneously.

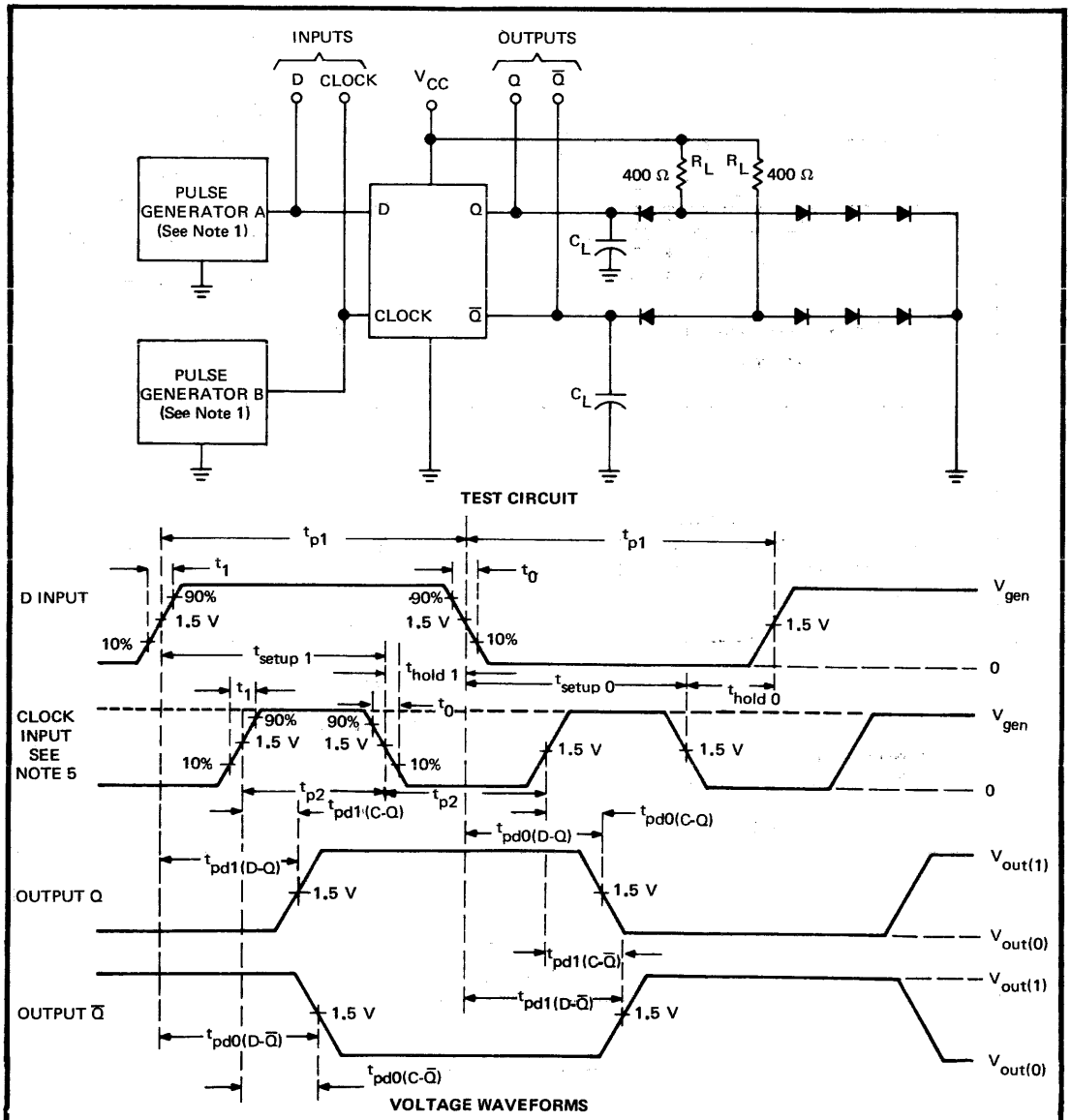
FIGURE 5

† Arrows indicate actual direction of current flow. Complementary $\overline{Q}$ outputs are available on the SN5475/SN7475.

9

PARAMETER MEASUREMENT INFORMATION

switching characteristics†



NOTES:
1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leqslant 10$ ns, and $Z_{out} \approx 50\ \Omega$. For pulse generator A t_{p1} = 1 μs and PRR = 500 kHz. For pulse generator B, t_{p2} = 500 ns and PRR = 1 MHz. Positions of D-input and clock-input pulses are varied with respect to each other to verify setup and hold times.
2. Each latch is tested separately.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N3064.
5. When measuring $t_{pd1(D-Q)}$ and $t_{pd0(D-Q)}$ (or $t_{pd0(D-\overline{Q})}$ and $t_{pd1(D-\overline{Q})}$ for the SN5475/SN7475), clock input must be held at logical 1.

FIGURE 6 – SWITCHING TIMES

†Complementary Q outputs are on the SN5475/SN7475 only.

TYPICAL APPLICATION

temporary storage of binary data

This application demonstrates the use of the SN7475 bistable latch as a temporary storage of binary-coded decimal data, from the SN7490 decade counter, which is to be decoded by the SN7441 decoder/driver. Temporary storage is desirable at this point for two reasons:

a. At counting frequencies above several cycles per second, it is sometimes desirable to eliminate the flicker on the display tube caused by reading an input count which is too fast to be recognized.

b. During the time that the latch is storing information the decade counter may start acquiring data for the next display.

A typical sequence of operation is illustrated (see Figure 7):

1. During t_1, reset decade counter to 0. At end of t_1, indicator will display "0".
2. During t_2, count BCD 3 at output of SN7490. Indicator still displays "0".
3. At start of t_3, indicator will display "3". At end of t_3, BCD 3 is committed to memory by SN7475 and the SN7490 may begin counting again.
4. During t_4, reset decade counter to 0 and count BCD 5 at output of SN7490. Indicator still displays "3".
5. At start of t_5, indicator will display "5". At end of t_5, BCD 5 is committed to memory by SN7475 and the SN7490 is released.

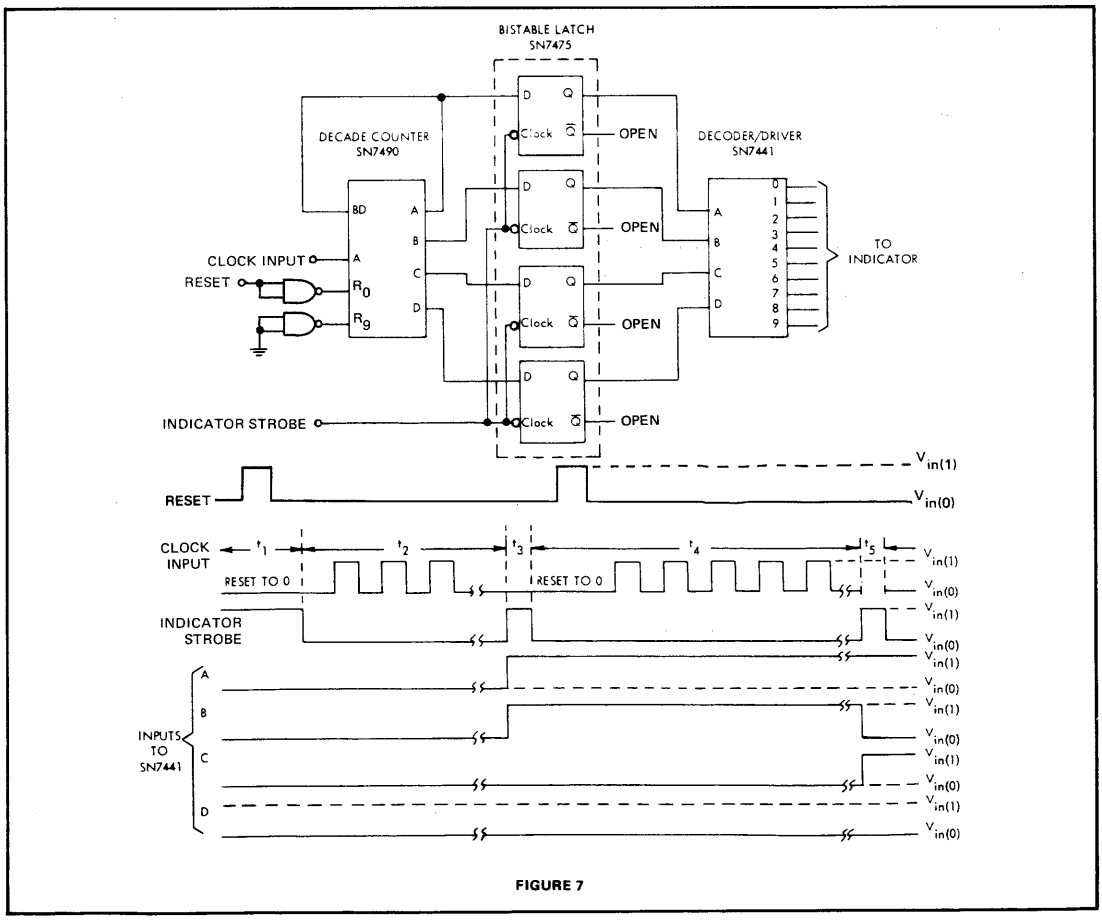


FIGURE 7

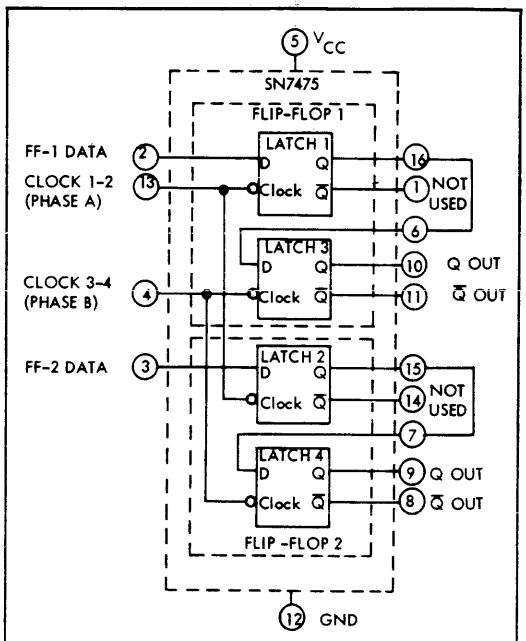
TYPICAL APPLICATION

dual D-type master-slave flip-flop

This application demonstrates the use of the SN7475 as a dual D-type master-slave flip-flop, provided that two-phase clocking is permissible. Each of the D-type flip-flops are formed by merely interconnecting the Q output of one of the latches (which serves as the master) to the data input of another latch (which serves as the slave). Each of these interconnected latches must have a separate clock line; therefore if a dual D-type master-slave flip-flop is constructed from a single package (see Figure 8) they must be operated synchronously.

A typical transfer of data is illustrated. Note that after the start of t_1 the data input is released to acquire new information as the master section has "locked up" the original data after clock pulse A_1. At the start of t_2 the data "locked up" in the master is transferred to the output, and at the end of t_2 (and for the duration of t_3) the slave retains the original data.

This type of flip-flop is desirable in applications where speed is not a primary requirement and where the additional clock skew, resulting from this delay between the two clock pulses, affords greater system reliability.



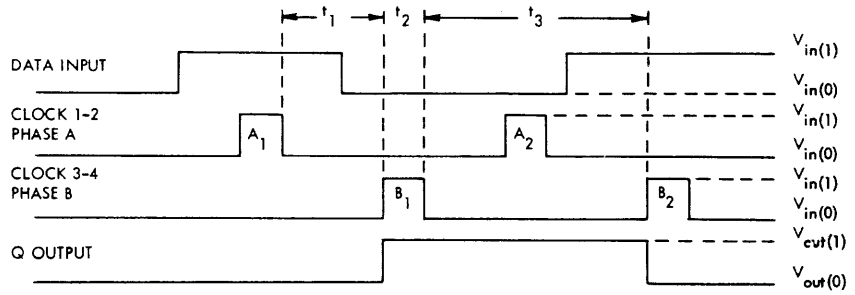


FIGURE 8

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

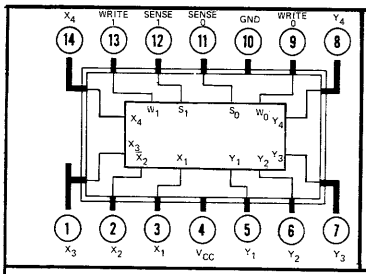
CIRCUIT TYPES SN5481, SN5484, SN7481, SN7484
16-BIT ACTIVE-ELEMENT MEMORIES

description

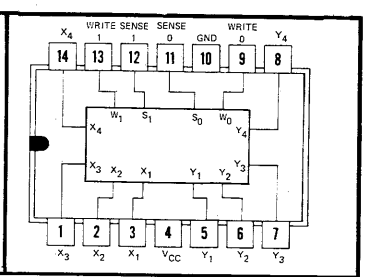
The 16-bit active-element memory is a monolithic, high-speed, transistor-transistor-logic (TTL) array of 16 flip-flops, and two write amplifiers interconnected to form a "scratch-pad" memory with direct-address and non-destructive read-out.

The flop-flops are arranged in a 4-by-4 matrix with each flip-flop representing one bit of 16 words. Four X-address lines and four Y-address lines permit the address of one bit at a time. Each flip-flop, composed of two cross-coupled 3-emitter transistors, is used to store one bit. To determine if a logical 1 or 0 has been stored, it is necessary to know which one of the two flip-flop transistors is conducting. One emitter of each of these transistors serves as the sensing output. All 16 of the logical 1 sensing outputs are connected to the sense logic 1 (S_1) amplifier input and all 16 of the logical0 sensing outputs are connected to the sense logical 0 (S_0) amplifier input. The two remaining emitters on each transistor are used to complete the matrix connections necessary for the X- and Y-address lines. Address line inputs are normally held low (logical 0) and currents from all conducting flip-flop transistors flow out these address lines.

SN5481/SN7481 CIRCUITS
W FLAT PACKAGE (TOP VIEW)

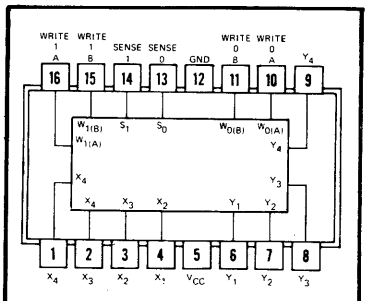


SN5481/SN7481 CIRCUITS
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see logic diagram

SN5484/SN7484 CIRCUITS
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see logic diagram

†Pin assignments for these circuits are the same for all packages.

To address a flip-flop both the X- and Y-address lines associated with that flip-flop are taken to a logical 1 voltage. Due to the matrix nature of the circuit, at least one address line of all flip-flops except the one being addressed will continue to remain at a logical 0 level and no change will occur on those flip-flops. But, in the addressed flip-flop, the current in the conducting transistor diverts from the address lines to the appropriate sense line and then to one of the sense amplifiers. Thus, either the sense amplifier associated with a logical 1 or the sense amplifier associated with a logical 0 is activated. When this occurs, the output of the activated sense amplifier drops from a logical 1 to a logical 0 level. The memory is non-destructive as the states of the flip-flops are not disturbed during sensing. The memory is volatile and information will be lost if the supply voltage is removed.

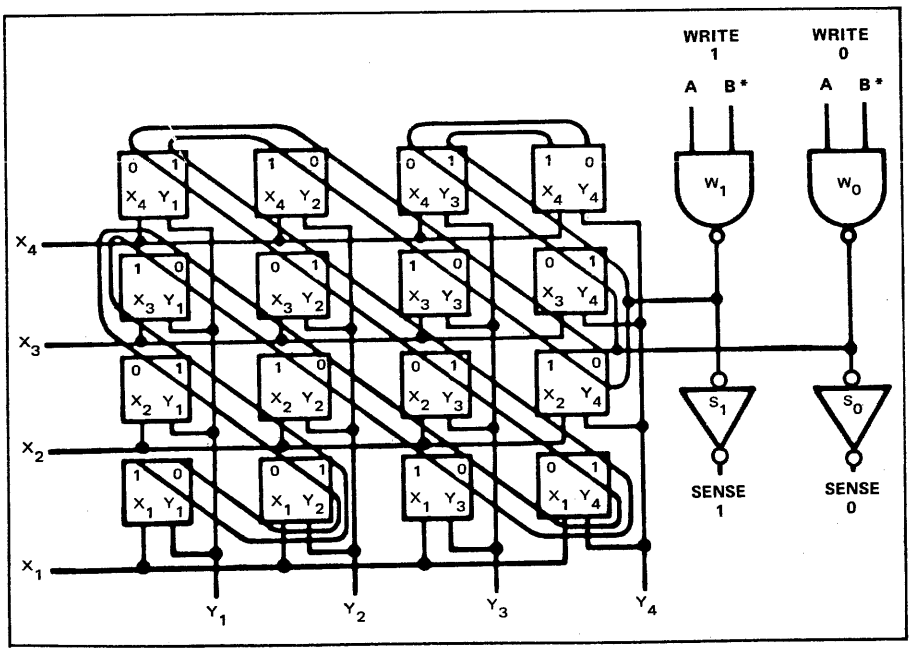
description (continued)

To store new information in a flip-flop, it is necessary to address it and apply logical 1 voltage to the appropriate write amplifier input. (The SN5484/SN7484 circuit has gated write-amplifier inputs). The output of the write amplifier responds by dropping to a logical 0 level. Since all logical 0 sense lines are connected to the output of the logical 0 write amplifier and all logical 1 sense lines are connected to the output of the logical 1 write amplifier, a logical 0 voltage on the output of a write amplifier will apply the same voltage to emitters of all flip-flop transistors connected to that amplifier. In all flip-flops except the one being addressed, this low voltage has no effect since at least one other emitter on each of the flip-flop transistors is held low by the address lines. But two possibilities exist with the flip-flop that is addressed. The flip-flop may already be in the desired state, in which case no change occurs. But if the flip-flop must be changed from one state to the other, the low voltage applied to the emitter of the transistor which is not conducting turns that transistor on causing the other transistor to turn off.

Since the connection between the output of the write amplifier and the sense line is common to the input of the sense amplifier, the memory cannot be used to provide information on the state of a bit while the write amplifiers are activated.

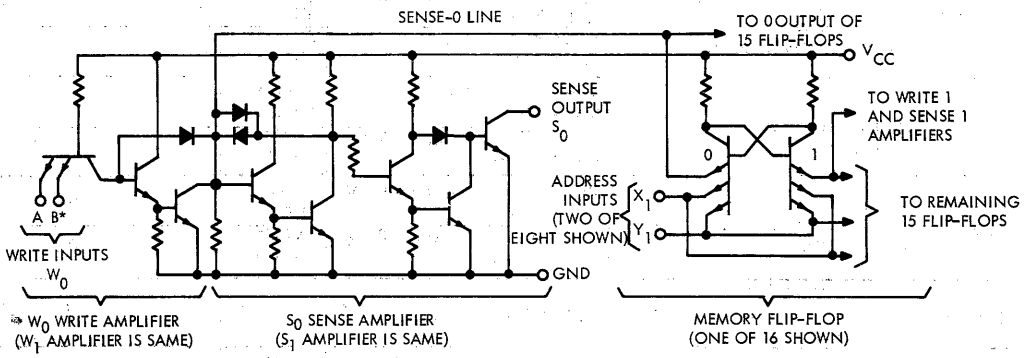
A number of active element memories may be paralleled to form the desired matrix size (number of words) and to form the desired word length (number of bits). Standard TTL circuitry, employed for the address line inputs, write amplifier inputs, and the saturating output transistors, provides complete TTL and DTL compatibility and maintains typical noise margins of one volt. Average power dissipation is 275 milliwatts (typical), and the open-collector outputs may be wire-OR connected to similar outputs. Internal circuitry of the write and sense amplifiers are operated within their linear range to improve speed. Sensing propagation delay times are typically 20 nanoseconds when operated at full fan-out and 30 picofarads of circuit capacitance.

logic diagram



*Gated inputs (as shown) are available on SN5484/SN7484 only.
The SN5481/SN7481 has one W_0 and one W_1 input.

schematic diagram



* Gated inputs (as shown) are available on SN5484/SN7484 only. The SN5481/SN7481 has one W_0 and one W_1 input.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5481, SN5484 Circuits . . . . . −55°C to 125°C
SN7481, SN7484 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

9

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5481, SN5484 Circuits	4.5	5	5.5	V
SN7481, SN7484 Circuits	4.75	5	5.25	V
Width of Write Pulse, $t_{p(write)}$ (See Figure 11)	25			ns
Address Lines Input Setup Time, t_{setup} (See Figure 11)	0			ns

NOTES: 1. These voltage values are with respect to ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
$V_{in(1)AW}$ or $V_{in(1)AS}$	Input voltage required at X or Y address lines to ensure writing or sensing	1	V_{CC} = MIN, I_{sink} = 20 mA	$V_{out(0)} \leq 0.4$ V,	SN5481, SN5484	2.1			V
			V_{CC} = MIN, I_{sink} = 40 mA	$V_{out(0)} \leq 0.4$ V,	SN7481, SN7484	2.1			V
$V_{in(1)W}$	Input voltage required at W_0 or W_1 inputs to ensure writing	1	V_{CC} = MIN, I_{sink} = 20 mA	$V_{out(0)} \leq 0.4$ V,	SN5481, SN5484	2			V
			V_{CC} = MIN, I_{sink} = 40 mA	$V_{out(0)} \leq 0.4$ V,	SN7481, SN7484	2			V
$V_{in(0)A\overline{W}}$	Input voltage required at X or Y address lines to prevent writing	2	V_{CC} = MIN, I_{sink} = 20 mA	$V_{out(0)} \leq 0.4$ V,	SN5481, SN5484			0.8	V
			V_{CC} = MIN, I_{sink} = 40 mA	$V_{out(0)} \leq 0.4$ V,	SN7481, SN7484			0.8	V
$V_{in(0)A\overline{S}}$	Input voltage required at X or Y address lines to prevent sensing	3	V_{CC} = MIN,	$I_{out(1)}$ = 250 μA	V_{out} = 5.5 V			1	V
$V_{in(0)\overline{W}}$	Input voltage required at W_0 or W_1 to prevent writing	1	V_{CC} = MIN, I_{sink} = 20 mA	$V_{out(0)} \leq 0.4$ V,	SN5481, SN5484			1	V
			V_{CC} = MIN, I_{sink} = 40 mA	$V_{out(0)} \leq 0.4$ V,	SN7481, SN7484			1	V
$V_{out(1)}$	Logical 1 output voltage	3	V_{CC} = MIN,	$I_{out(1)}$ = 250 μA		5.5			V
$V_{out(0)}$	Logical 0 output voltage (on level)	1 and 2	V_{CC} = MIN,	I_{sink} = 20 mA	SN5481, SN5484			0.4	V
			V_{CC} = MIN,	I_{sink} = 40 mA	SN7481, SN7484			0.4	V
$I_{in(0)}$	Logical 0 level input current at write 1 and write 0 (each input)	4	V_{CC} = MAX,	V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at all X or all Y address lines	5	V_{CC} = MAX,	V_{in} = 0.4 V				−11	mA
$I_{in(1)}$	Logical 1 level input current at write 1 and write 0 (each input)	6	V_{CC} = MAX,	V_{in} = 2.4 V				40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at each X and each Y address line	6	V_{CC} = MAX,	V_{in} = 4.5 V				400	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				3	mA
I_{CC}	Supply current	6	V_{CC} = MAX		SN5481, SN5484		55	78	mA
					SN7481, SN7484		55	91	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

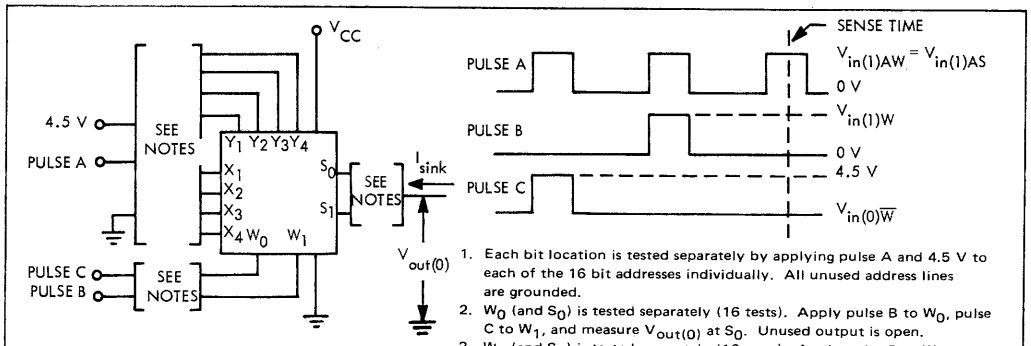
9

switching characteristics V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{WR}	Write recovery time	7	C_L = 15 pF, X_1 - Y_1 location addressed		30	60	ns
t_{pd0}	Propagation delay time to logical 0 level from address-line inputs to S_0 or S_1 outputs	7	C_L = 15 pF, X_1 - Y_1 location addressed		22	45	ns
			C_L = 200 pF, X_1 - Y_1 location addressed		27	55	ns
t_{pd1}	Propagation delay time to logical 1 level from address-line inputs to S_0 or S_1 outputs	7	C_L = 15 pF, X_1 - Y_1 location addressed		15	25	ns
			C_L = 200 pF, X_1 - Y_1 location addressed		20	35	ns
t_{pd0}	Propagation delay time to logical 0 level from address-line inputs to S_0 or S_1 outputs	7	C_L = 15 pF, X_1 through X_4 and Y_1 locations addressed		20	30	ns

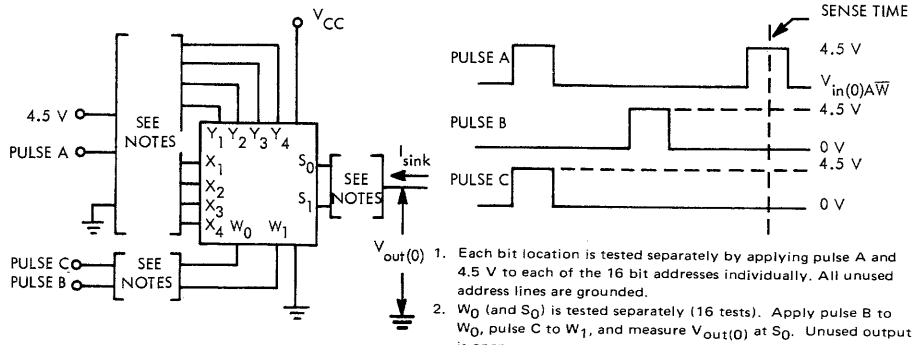
d-c test circuits†

PARAMETER MEASUREMENT INFORMATION



1. Each bit location is tested separately by applying pulse A and 4.5 V to each of the 16 bit addresses individually. All unused address lines are grounded.
2. W_0 (and S_0) is tested separately (16 tests). Apply pulse B to W_0, pulse C to W_1, and measure $V_{out(0)}$ at S_0. Unused output is open.
3. W_1 (and S_1) is tested separately (16 tests). Apply pulse B to W_1, pulse C to W_0, and measure $V_{out(0)}$ at S_1. Unused output is open.
4. For the SN5484/SN7484, each of the two W_0 or two W_1 inputs are tested separately. Apply 4.5 V to unused W_0 or W_1 inputs.

FIGURE 1



1. Each bit location is tested separately by applying pulse A and 4.5 V to each of the 16 bit addresses individually. All unused address lines are grounded.
2. W_0 (and S_0) is tested separately (16 tests). Apply pulse B to W_0, pulse C to W_1, and measure $V_{out(0)}$ at S_0. Unused output is open.
3. W_1 (and S_1) are tested separately (16 tests). Apply pulse B to W_1, pulse C to W_0, and measure $V_{out(0)}$ at S_1. Unused output is open.
4. For the SN5484/SN7484, each of the two W_0 or two W_1 inputs are tested separately. Apply 4.5 V to unused W_0 or W_1 inputs.

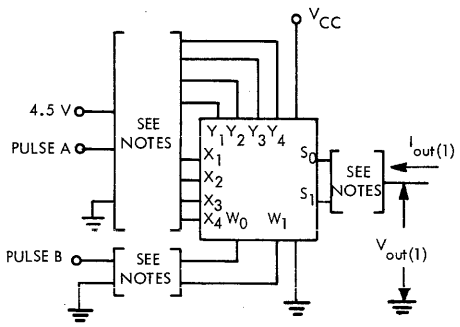
FIGURE 2

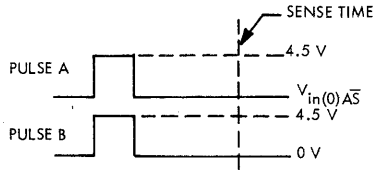
†Arrows indicate actual direction of current flow.

9

PARAMETER MEASUREMENT INFORMATION

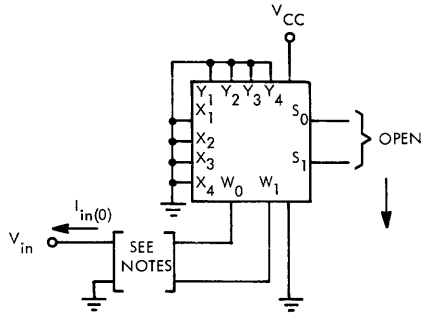
d-c test circuits† (continued)





1. Each bit location is tested separately by applying pulse A and 4.5 V to each of the 16 bit addresses individually. All unused address lines are grounded.
2. W_0 (and S_0) is tested separately (16 tests). Apply pulse B to W_0, ground W_1, and measure $V_{out(1)}$ at S_0. Unused output is open.
3. W_1 (and S_1) is tested separately (16 tests). Apply pulse B to W_1, ground W_0, and measure $V_{out(1)}$ at S_1. Unused output is open.
4. For the SN5484/SN7484, each of the two W_0 or two W_1 inputs are tested separately. Apply 4.5 V to the unused input of the gate under test and ground both inputs of the unused gate.

FIGURE 3



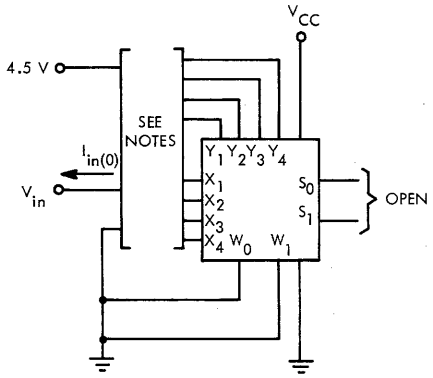
1. Each input is tested separately.
2. All unused inputs are grounded.

FIGURE 4

† Arrows indicate actual direction of current flow.

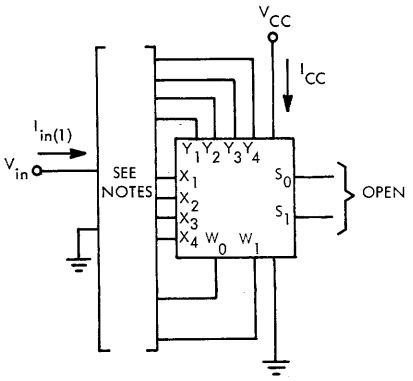
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



1. Each X input is tested separately with the other three X inputs grounded and 4.5 V applied to all Y inputs.
2. Each Y input is tested separately with the other three Y inputs grounded and 4.5 V applied to all Y inputs.
3. For the SN5484/SN7484, both W_0 and both W_1 inputs are grounded.

FIGURE 5



1. Each input is tested separately for $I_{in(1)}$ with all unused inputs grounded.
2. When measuring I_{CC} all inputs are grounded.

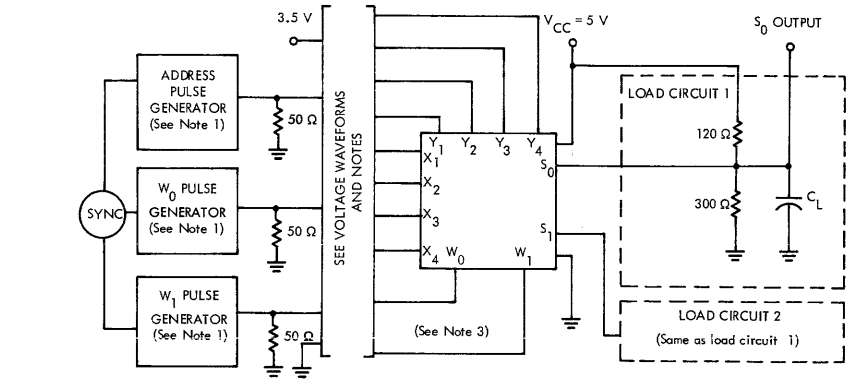
FIGURE 6

† Arrows indicate actual direction of current flow.

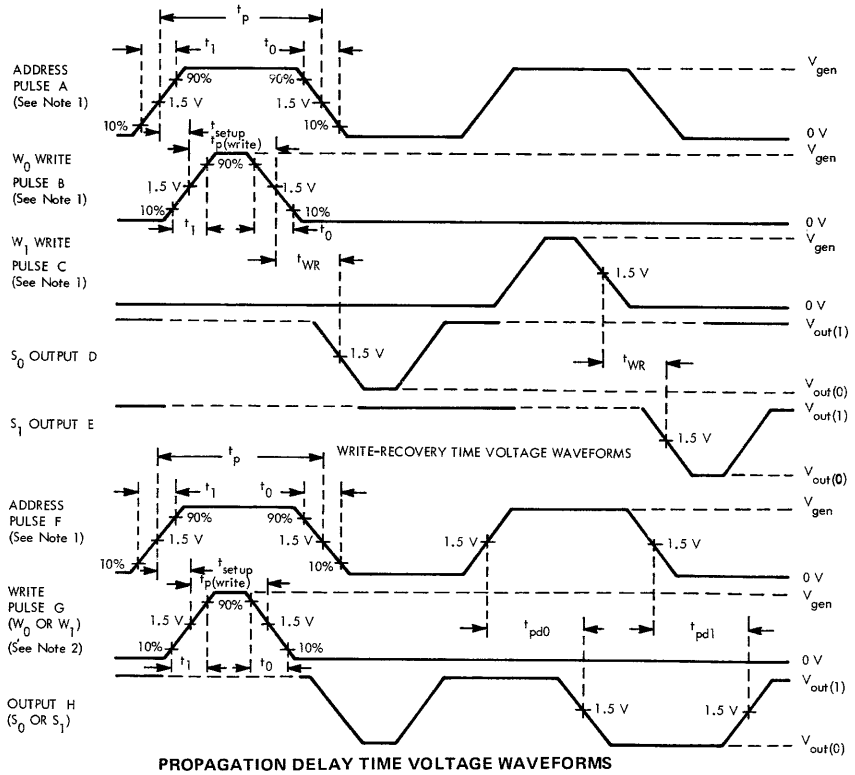
9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

NOTES: 1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 = t_0$ = 10 ns, t_{setup} = 0 to 10 ns. For the address pulse generator, t_p = 100 ns and PRR = 2 MHz. For the W_0 and W_1 pulse generators, t_p = 25 ns and PRR = 1 MHz.

2. C_L includes probe and jig capacitance.

3. For the SN5484/SN7484, unused W_0 and W_1 inputs are 3.5 V.

FIGURE 7 – SWITCHING CHARACTERISTICS

TYPICAL APPLICATIONS

This application demonstrates use of the 16-bit active element memory to form a high-speed, direct-address, scratch-pad memory having a storage capability of m-words (in multiples of 16) of n-bit length. For purposes of this discussion, a memory is illustrated which will store 64 words each having a length of 8-bits. See Figure A. This storage capability may be increased or decreased using the patterns shown.

In this example, each of the planes consist of four 16-bit memory circuits connected in an 8-by-8 matrix. This organization provides 64 addresses (words) of 8-bits (word length) or a total bit capability of 512 bits (64 X 8).

Each bit plane (B_0 through B_7) is formed by paralleling the W_0, W_1 inputs, S_0, S_1 outputs, and completing the X-Y matrix connections. The matrix is completed by paralleling the X lines of Circuits A-B and C-D and the Y lines of A-C then B-D, to form the 64 addresses of plane B_0. Two pull-up resistors, one for S_0 and one for S_1, should be provided for wired-OR outputs. The other seven planes are identical to B_0.

The X and Y lines of the eight planes are paralleled so that all bits of each word are addressed simultaneously. Addressing of a particular word is accomplished by the X-Y decoder/drivers. For this particular example, the decoder could be a 1-of-8 decoder (see SN7442 and SN7444 applications) and the drivers may consist of discrete transistors, each capable of supplying current for 16 address inputs. A number of decoding/driving schemes are possible.

The SN5484/SN7484 has gated W_0 and W_1 inputs which may be used to perform the write enable function. External gating may be employed if enabling functions are required with the SN5481/SN7481.

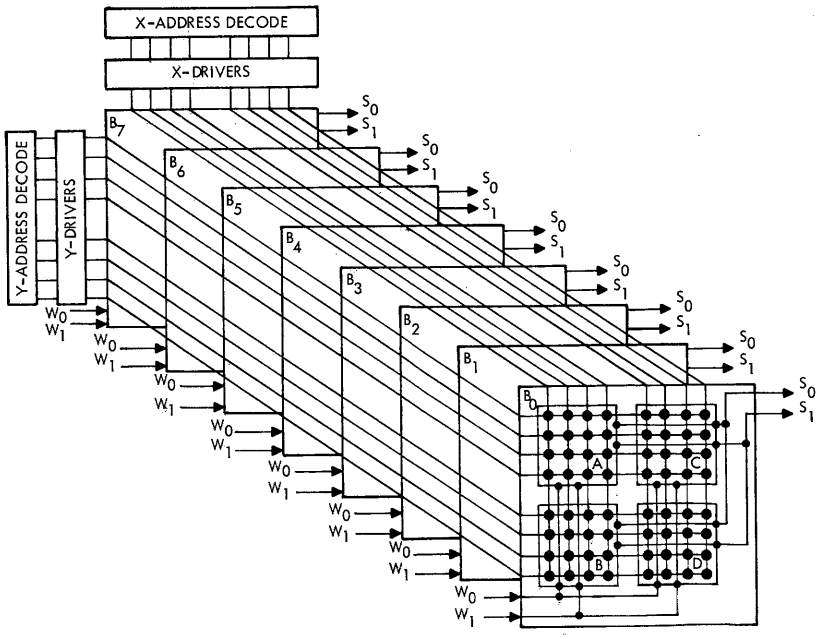


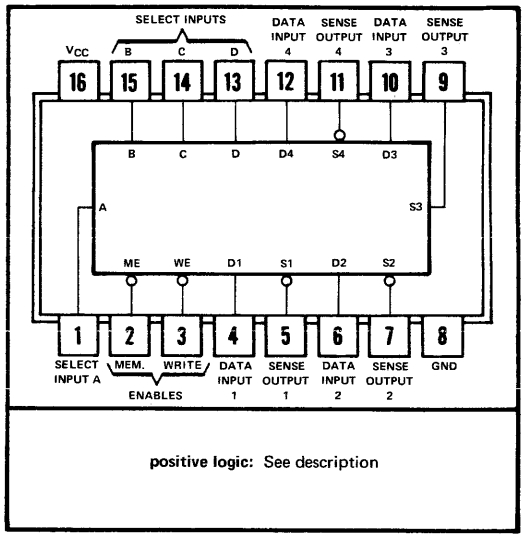
FIGURE A – TYPICAL MEMORY ORGANIZATION

9

CIRCUIT TYPE SN7489
64-BIT READ/WRITE MEMORY

- For Application as a "Scratch Pad" Memory with Nondestructive Read-Out
- Fully Decoded Memory Organized as 16 Words of Four Bits Each
- Fast Access Time . . . 33 ns Typical
- Diode-Clamped, Buffered Inputs
- Open-Collector Outputs Provide Wire-AND Capability
- Typical Power Dissipation . . . 375 mW
- Compatible with Most TTL and DTL Circuits

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See description

†Pin assignments for these circuits are the same for all packages.

description

This 64-bit active-element memory is a monolithic, high-speed, transistor-transistor logic (TTL) array of 64 flip-flop memory cells organized in a matrix to provide 16 words of four bits each. Each of the 16 words is addressed in straight binary with full on-chip decoding.

The buffered memory inputs consist of four address lines, four data inputs, a write enable, and a memory enable for controlling the entry and access of data. The memory has open-collector outputs which may be wire-AND connected to permit expansion up to 4704 words of N-bit length without additional output buffering. The open-collector outputs may be utilized to drive external loads directly; however, dynamic reponse of an output can, in most cases, be improved by using an external pull-up resistor in conjunction with a partially loaded output. Access time is typically 33 nanoseconds; power dissipation is typically 375 milliwatts.

FUNCTION TABLE

ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Storage	Complement of Data Inputs
H	H	Do Nothing	High

9

write operation

Information present at the data inputs is written into the memory by addressing the desired word and holding both the memory enable and write enable low. Since the internal output of the data input gate is common to the input of the sense amplifier, the sense output will assume the opposite state of the information at the data inputs when the write enable is low.

read operation

The complement of the information which has been written into the memory is nondestructively read out at the four sense outputs. This is accomplished by holding the memory enable low, the write enable high, and selecting the desired address.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
High-level output voltage, V_{OH} (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Width of write-enable pulse, t_w	40			ns
Setup time, data input with respect to write enable, t_{setup} (see Figure 1)	40			ns
Hold time, data input with respect to write enable (see Figure 1)	5			ns
Select input setup time with respect to write enable, t_{setup}	0			ns
Select input hold time after writing, t_{hold} (see Figure 1)	5			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			20	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OL} = 12 mA			0.4	V
			I_{OL} = 16 mA			0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3		75	105	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, f = 1 MHz	V_O = 2.4 V,		4		pF

NOTE 3: I_{CC} is measured with the memory enable grounded, all other inputs at 4.5 V, and all outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

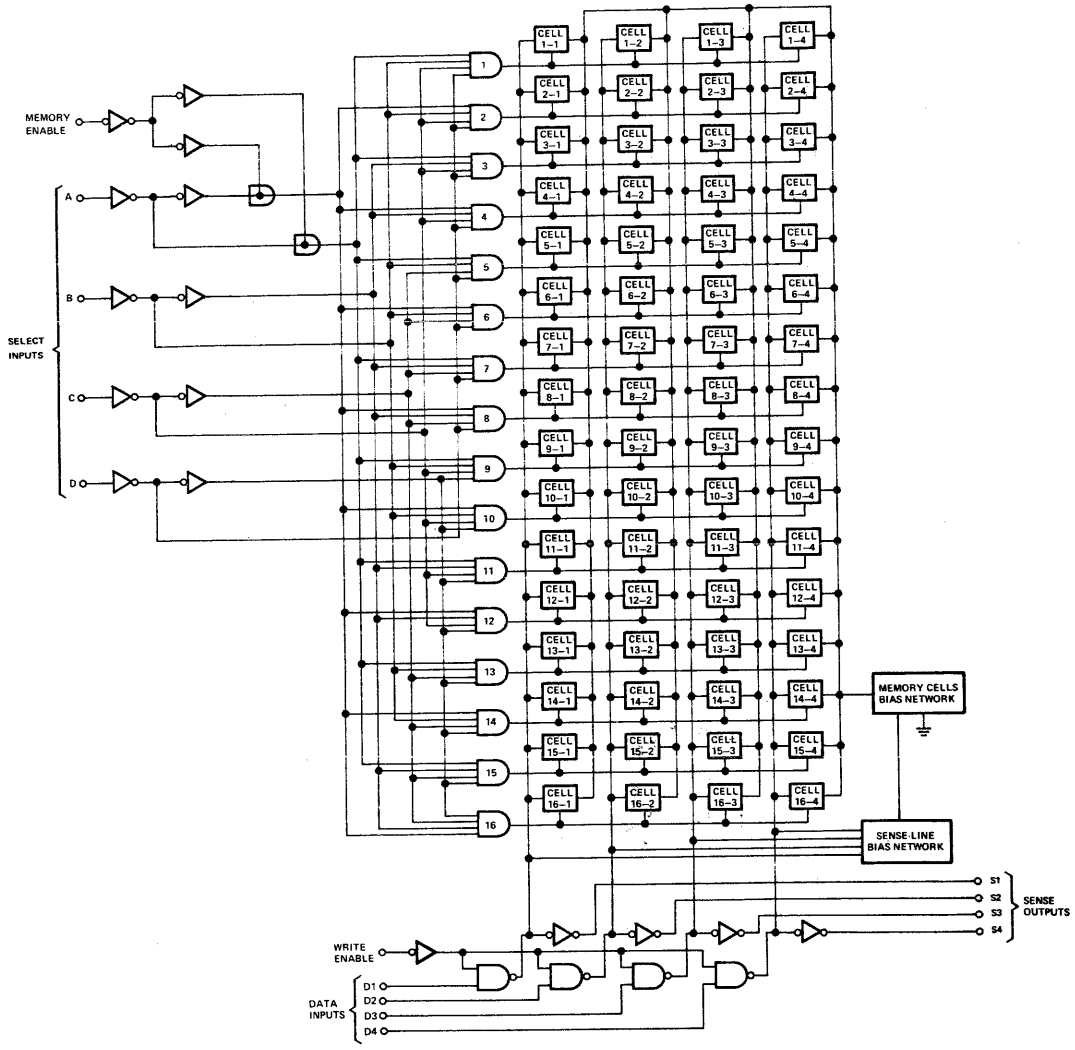
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from memory enable		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 1		26	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output from memory enable				33	50	
t_{PLH}	Propagation delay time, low-to-high-level output from select				30	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from select				35	60	
t_{SR}	Sense recovery time after writing	output initially high			39	70	ns
		output initially low			48	70	

9

CIRCUIT TYPE SN7489
64-BIT READ/WRITE MEMORY

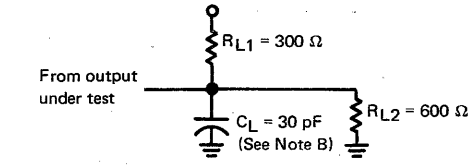
functional block diagram



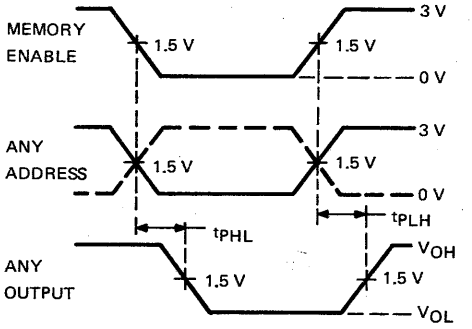
9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATION DATA

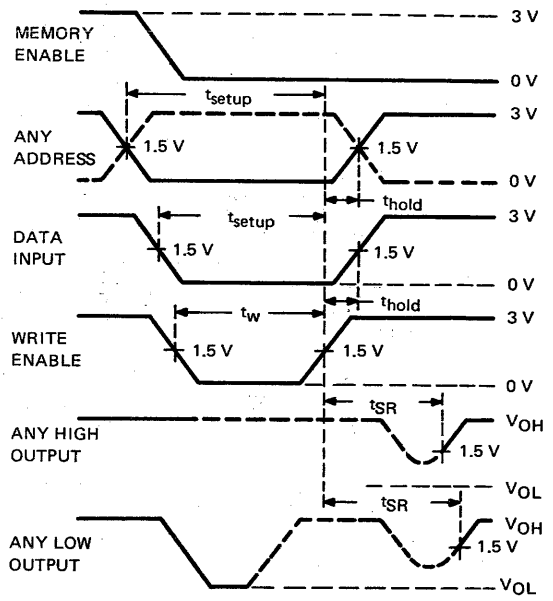


LOAD CIRCUIT



Write enable is high.

READ CYCLE



WRITE CYCLE FROM WRITE ENABLE

NOTES: A. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

INPUT CURRENT vs INPUT VOLTAGE

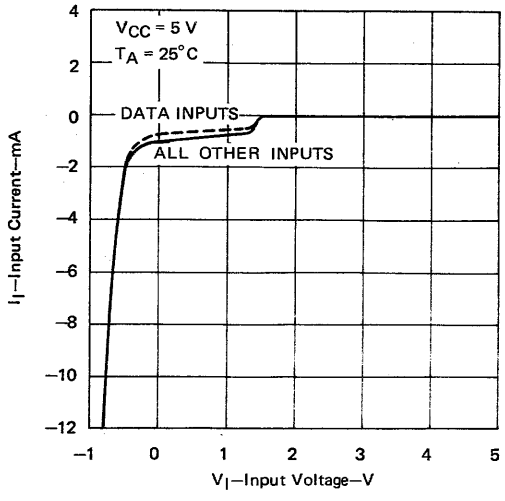


FIGURE 2

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

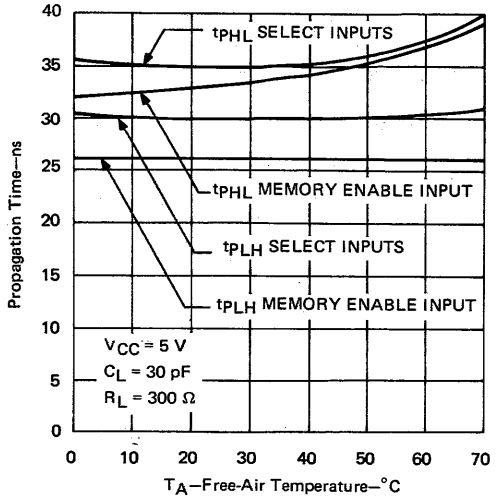
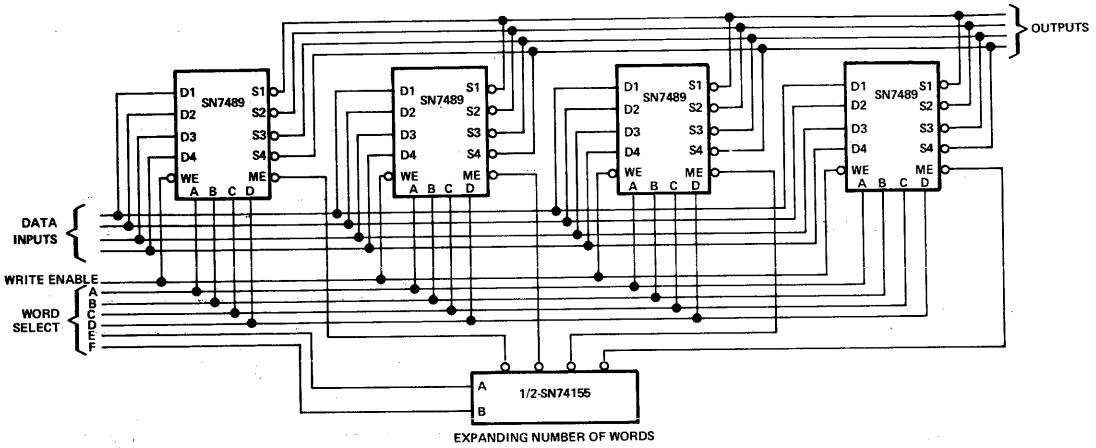


FIGURE 3

9

CIRCUIT TYPE SN7489
64-BIT READ/WRITE MEMORY

TYPICAL APPLICATION DATA



To increase word capacity, the outputs of a number of memories are wire-AND connected and each memory is enabled individually. The word capacity is limited only by the capability to wire-AND the outputs. In this case, the limiting parameter is the sink current capability of the memory, 12 milliamperes if the maximum low-level output voltage is limited to 0.4 V. Assuming that the output is driving only one Series 74 load (1.6 mA in the low state), the minimum value of the load resistor, R_L, will be 442 ohms.

$$R_L = \frac{V_{RL}}{I_{RL}} = \frac{V_{CC} - V_{OL}}{I_{sink} - I_{IL}(N_{TTL\ loads})} = \frac{5.0\ V - 0.4\ V}{0.012\ A - 0.0016\ A} = 442\ \Omega$$

In this case, the 442-ohm load resistor will supply sufficient high-level output current to wire-AND 292 outputs, providing a word capacity of 4672 words.

$$442 = \frac{V_{RL}}{I_{RL}} = \frac{V_{CC} - V_{OH}}{I_{OH}\,(N_{wire\text{-}ANDS}) + I_{IH}\,(N_{TTL\ loads})} = \frac{5.0\ V - 2.4\ V}{20\ \mu A\,(N_{wa}) + 40\ \mu A(1)}$$

therefore N_{wa} = 292 outputs

9

When driving one or more standard TTL loads, the possibilities are shown below in increments of standard loads for both 12-mA and 16-mA sink current.

WORD CAPACITY vs TTL LOADS FOR V_{OL} = 0.4 V MAX

LOADS	R_L VALUE (OHMS)	MAX NO. OF WIRE-ANDS	MAX NO. OF WORDS
1	442	292	4672
2	522	245	3920
3	638	197	3152
4	821	150	2400
5	1150	103	1648
6	1916	55	880
7	5750	8	128

WORD CAPACITY vs TTL LOADS FOR V_{OL} = 0.45 V MAX

LOADS	R_L VALUE (OHMS)	MAX NO. OF WIRE-ANDS	MAX NO. OF WORDS
1	316	409	6544
2	356	361	5776
3	406	314	5024
4	473	266	4256
5	569	218	3488
6	711	170	2720
7	948	123	1968
8	1422	75	1200
9	2844	27	432
10	4000	12	192

Where multiple SN7484 devices are used in a memory system, the memory enable input allows easy decoding of additional address bits.

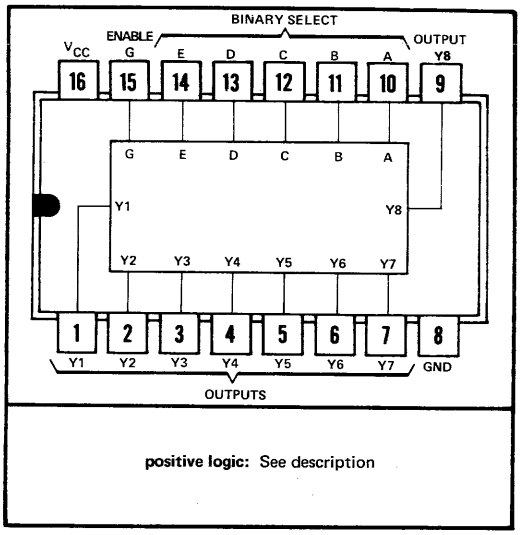
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5488A, SN7488A
256-BIT READ-ONLY MEMORIES

CIRCUIT TYPES SN5488A, SN7488A
BULLETIN NO. DL-S 7111445, JANUARY 1971
REPLACES BULLETIN NO. DL-S 7011299, FEBRUARY 1970

- Applications in Computer Subroutines
- Useful in Display Systems and Readouts
- Memory Organized as 32 Words of 8 Bits Each
- Input Clamping Diodes Simplify System Design
- Open-Collector Outputs Permit Wire-AND Capability
- Typical Access Time: 25 nanoseconds
- Typical Power Dissipation: 285 milliwatts
- Fully Compatible with Most TTL and DTL Circuits

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See description

description

These custom-programmed, 256-bit, read-only memories are organized as 32 words of eight bits each. Each monolithic, high-speed, transistor-transistor logic (TTL), 32-word memory array is addressed in straight 5-bit binary with full on-chip decoding. An overriding memory-enable input is provided which, when taken high, will inhibit the 32 address gates and cause all eight outputs to remain high. Data, as specified by the customer on the enclosed truth table/order blank, are permanently programmed into the monolithic structure for the 256 bit locations. This organization is expandable to n-words of N-bit length.

The address of an eight-bit word is accomplished through the buffered, binary select inputs which are decoded by the 32 five-input address gates. When the memory-enable input is high, all 32 gate outputs are low, turning off the eight output buffers.

Data are programmed into the memory at the emitters of 32 eight-emitter transistors. The programming process involves connecting or not connecting each of the 256 emitters. If an emitter is connected, a low-level voltage is read out of that bit location when its decoding gate is addressed. If the emitter is not connected, a high-level voltage is read when addressed. Those decoding-gate output emitters which are used are connected to their respective bit lines to drive the eight output buffers. Since only one decoding gate is addressed at a time, only one of the 32 transistors can supply current to the output buffers at a time.

This memory is fully compatible for use with most TTL or DTL circuits. Input clamping diodes are provided to minimize transmission-line effects and simplify system design. Input buffers lower the fan-in requirement to only one normalized Series 54/74 load for all inputs including enable (G). The open-collector outputs are capable of sinking 12 milliamperes of current and may be wire-AND connected to increase the number of words available. An external pull-up resistor from each output to the supply line (V_{CC}) is required to define the high-level output voltage. Where multiple SN7488 devices are used in a memory system, the enable input allows easy decoding of additional address bits. Access propagation delay time is typically 25 nanoseconds and power dissipation is typically 285 milliwatts.

The customer can specify the output level desired at each of the 256 bit locations by completing the enclosed truth table/order blank. Upon receipt of the order, Texas Instruments will assign a special device number to the device programmed according to the customer's order. The completed device will be marked with the TI special device number (not SN5488A or SN7448A). It is important that the customer specify not only the output levels desired at all 256-bit locations on the enclosed truth table/order blank, but also the other information requested.

Series 74 devices are characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5488A, SN7488A
256-BIT READ-ONLY MEMORIES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN5488A Circuits . . . . . 55°C to 125°C
SN7488A Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5488A			SN7488A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1			2			V
V_{IL}	Low-level input voltage	1					0.8	V
V_I	Input clamp voltage	2	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	1	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			40	μA
V_{OL}	Low-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OL} = 12 mA			0.4	V
I_{IH}	High-level input current (each input)	3	V_{CC} = MAX,	V_I = 2.4 V			25	μA
			V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IL}	Low-level-input current (each input)	2	V_{CC} = MAX,	V_I = 0.4 V			−1	mA
I_{CCH}	Supply current, all outputs high	4	V_{CC} = MAX			50		mA
I_{CCL}	Supply current, all outputs low (see Note 2)	5				64	80	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: All 32 words are addressed separately to ensure that the supply current does not exceed the stated maximum. The typical value shown is for the worst-case condition of all eight outputs driven low at one time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Enable	Any	6	C_L = 15 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω		22	35	ns
t_{PHL}	Enable	Any				22	35	
t_{PLH}	Select	Any				29	45	
t_{PHL}	Select	Any				23	40	

§t_{PLH} = Propagation delay time, low-to-high level output.
t_{PHL} = Propagation delay time, high-to-low level output.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TRUTH TABLE

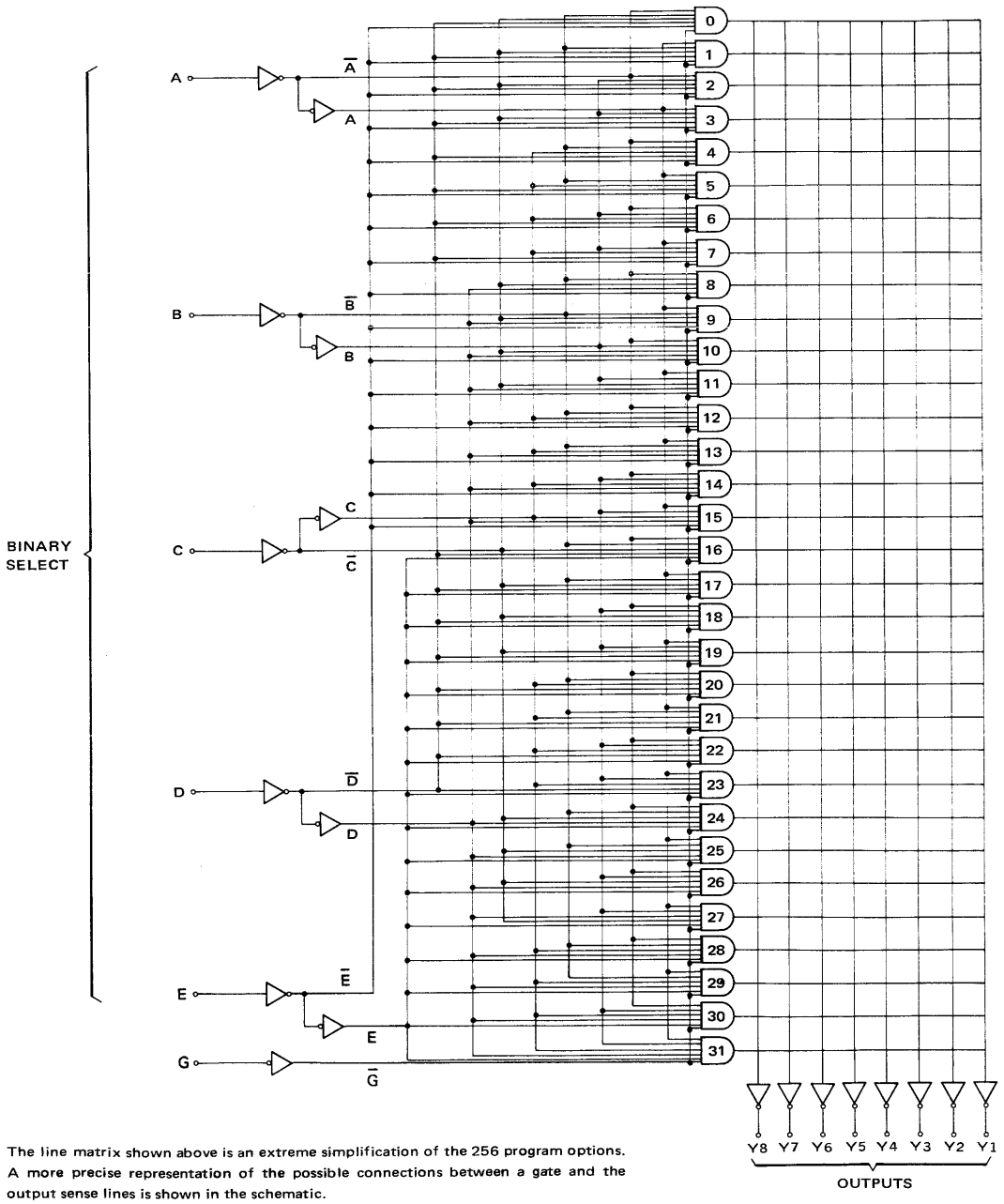
The output levels are not shown on the truth table since the customer specifies the output condition he desires at each of the eight outputs for each of the 32 words (256 bits). The customer does this by filling out the TRUTH TABLE/ORDER BLANK at the back of this data sheet, and sending it in with his purchase order. The copy of the truth table on this page may be filled out and retained by the customer for his reference.

WORD	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	L	L	L	L	L	L								
1	L	L	L	L	H	L								
2	L	L	L	H	L	L								
3	L	L	L	H	H	L								
4	L	L	H	L	L	L								
5	L	L	H	L	H	L								
6	L	L	H	H	L	L								
7	L	L	H	H	H	L								
8	L	H	L	L	L	L								
9	L	H	L	L	H	L								
10	L	H	L	H	L	L								
11	L	H	L	H	H	L								
12	L	H	H	L	L	L								
13	L	H	H	L	H	L								
14	L	H	H	H	L	L								
15	L	H	H	H	H	L								
16	H	L	L	L	L	L								
17	H	L	L	L	H	L								
18	H	L	L	H	L	L								
19	H	L	L	H	H	L								
20	H	L	H	L	L	L								
21	H	L	H	L	H	L								
22	H	L	H	H	L	L								
23	H	L	H	H	H	L								
24	H	H	L	L	L	L								
25	H	H	L	L	H	L								
26	H	H	L	H	L	L								
27	H	H	L	H	H	L								
28	H	H	H	L	L	L								
29	H	H	H	L	H	L								
30	H	H	H	H	L	L								
31	H	H	H	H	H	L								
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

9

functional block diagram (programming not shown)



The line matrix shown above is an extreme simplification of the 256 program options. A more precise representation of the possible connections between a gate and the output sense lines is shown in the schematic.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶

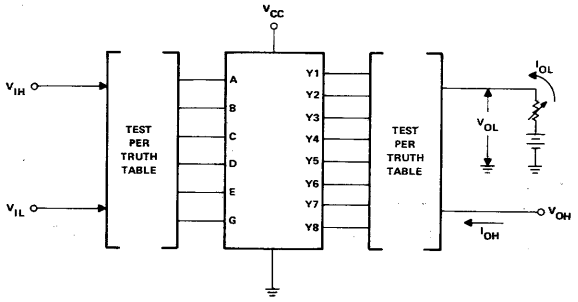
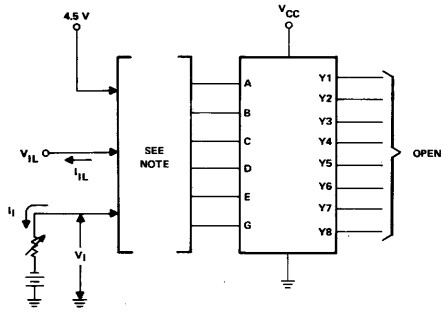
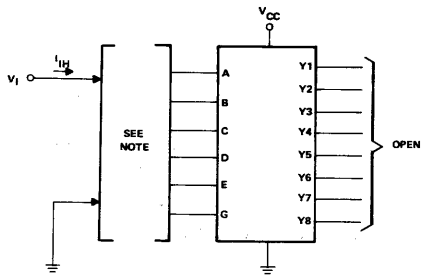


FIGURE 1–V_{IH}, V_{IL}, I_{OH}, V_{OL}



Each input is tested separately with all other inputs at 4.5 V.

FIGURE 2–V_I, I_{IL}



Each input is tested separately with all other inputs grounded.

FIGURE 3–I_{IH}

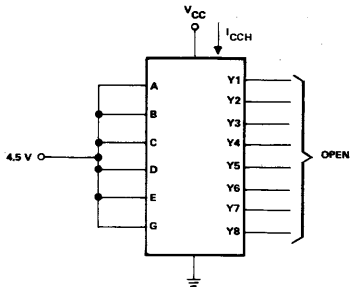
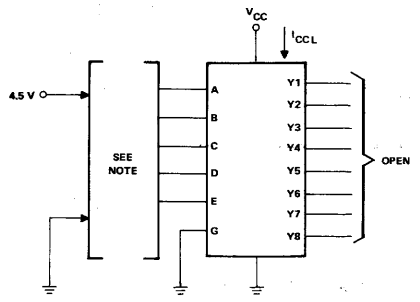


FIGURE 4–I_{CCH}



All 32 words are tested separately.

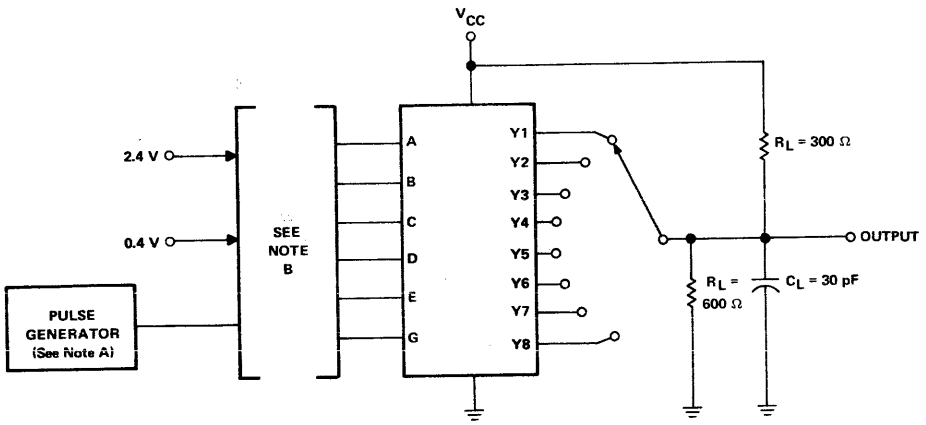
FIGURE 5–I_{CCL}

¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

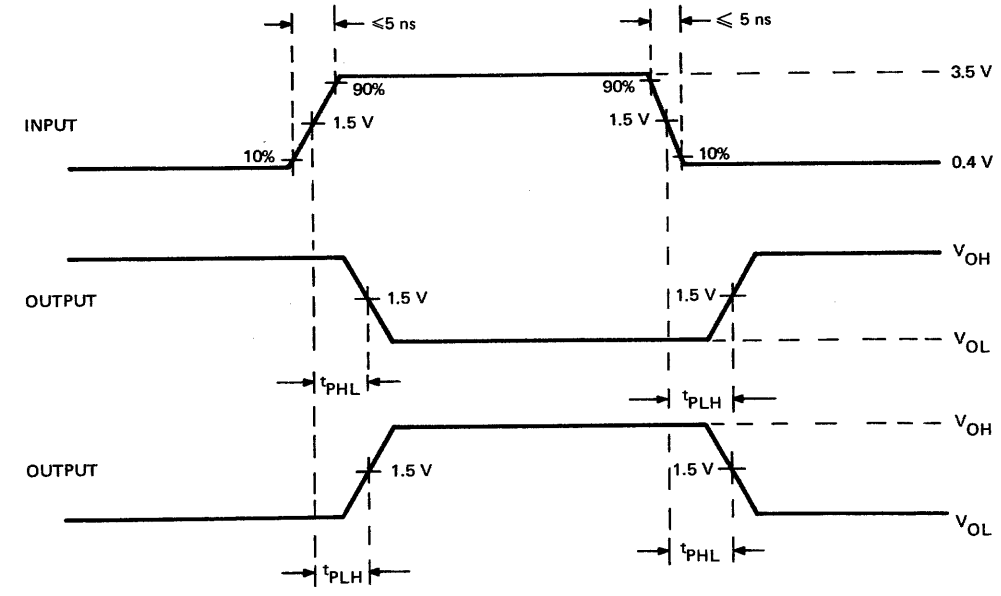
9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. The pulse generator is connected to the input under test. The other inputs, memory content permitting, are connected so that the input will switch the output under test.
C. C_L includes probe and jig capacitance.

FIGURE 6–PROPAGATION DELAY TIMES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATION DATA

operation

Interconnection of the address buffers and decoding gates is already committed in the circuit design. Each decoding gate corresponds to one of the 32 eight-bit words which is programmed into the memory.

When a decoding gate is addressed, all its output emitters are high. All of the emitters connected to a particular output line form dot-OR connections with one another; that is, one high emitter is necessary and sufficient to carry the line high. This high is then inverted by an output buffer to produce a low-level output.

Assume that the gate shown in the schematic diagram is gate 31 and that word 31 is to be 10000001 using positive logic. This requires a high-level voltage at outputs 1 and 8. Therefore, emitters 1 and 8 of gate 31 would be left unconnected while the remaining emitters would be connected to their corresponding output lines.

expansion

Figure A illustrates how two memories may be connected to provide 32 words of 16 bits each. This scheme may be utilized to form words of N-bit length. Figure B shows how the enable input may be utilized to selectively activate the memory in applications requiring a larger number of words. Although 8-bit words are shown in Figure B, each word may be lengthened by the method illustrated in Figure A. One obvious limiting factor in this expansion scheme is the fan-out capability of the binary select register. The capability for further expansion above 512 words is available by utilizing a selective method for enabling the SN54154 or SN74154 four-line-to-16-line decoder. For smaller memory systems, the SN54154 or SN74154 may be replaced with SN5442 or SN7442 or standard TTL NAND gates.

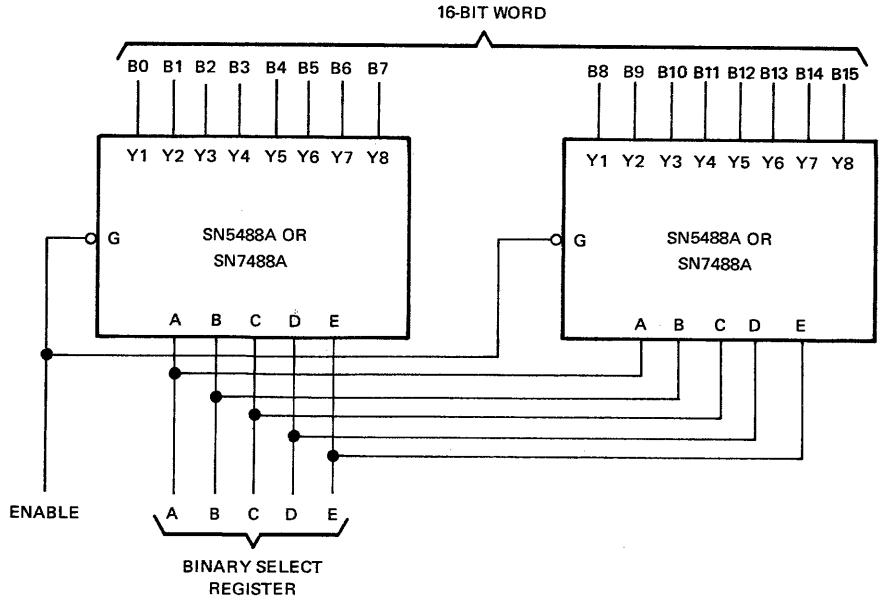


FIGURE A–INCREASING WORD LENGTH

9

TYPICAL APPLICATION DATA

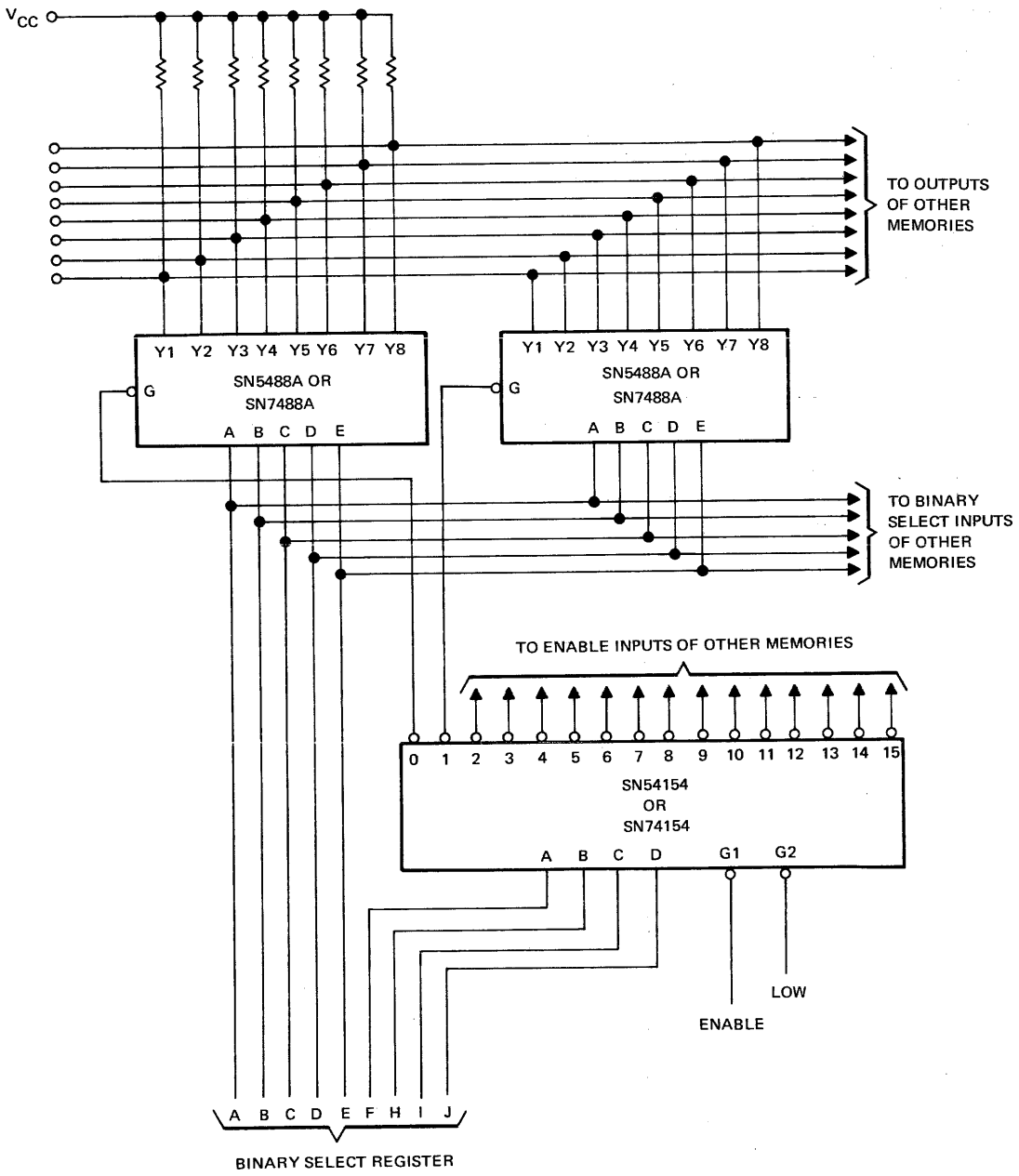


FIGURE B–INCREASING WORD CAPACITY

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TRUTH TABLE/ORDER BLANK

CUSTOMER _____

PURCHASE ORDER NO. _____

CUSTOMER PART NO. _____

THIS PORTION TO BE COMPLETED BY TI

TI PART NO.: _____

S.O. NO.: _____

DATE RECEIVED: _____

WORD	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	L	L	L	L	L	L								
1	L	L	L	L	H	L								
2	L	L	L	H	L	L								
3	L	L	L	H	H	L								
4	L	L	H	L	L	L								
5	L	L	H	L	H	L								
6	L	L	H	H	L	L								
7	L	L	H	H	H	L								
8	L	H	L	L	L	L								
9	L	H	L	L	H	L								
10	L	H	L	H	L	L								
11	L	H	L	H	H	L								
12	L	H	H	L	L	L								
13	L	H	H	L	H	L								
14	L	H	H	H	L	L								
15	L	H	H	H	H	L								
16	H	L	L	L	L	L								
17	H	L	L	L	H	L								
18	H	L	L	H	L	L								
19	H	L	L	H	H	L								
20	H	L	H	L	L	L								
21	H	L	H	L	H	L								
22	H	L	H	H	L	L								
23	H	L	H	H	H	L								
24	H	H	L	L	L	L								
25	H	H	L	L	H	L								
26	H	H	L	H	L	L								
27	H	H	L	H	H	L								
28	H	H	H	L	L	L								
29	H	H	H	L	H	L								
30	H	H	H	H	L	L								
31	H	H	H	H	H	L								
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

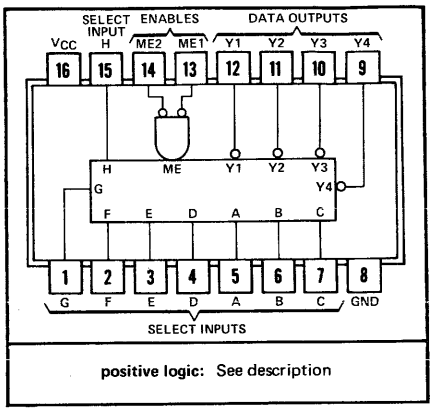
COMPLETE THE LOGIC DESIRED FOR 256 BITS.
INDICATE H FOR HIGH LEVEL OR L FOR LOW LEVEL.

H = high level, L = low level, X = irrelevant

CIRCUIT TYPES SN54187, SN74187
1024-BIT READ-ONLY MEMORIES

- Typical Access Time . . . 40 ns
- Typical Power Dissipation . . . 0.46 mW/Bit
- Organized as 256 Words by 4 Bits
- Ideal for Microprogramming, Reference Tables, and Code Converters
- Easily Expandable
- Fully Decoded, Buffered Inputs
- Diode-Clamped Inputs
- Full Fan-Out, Open-Collector Outputs
- Fully Compatible with Most TTL and DTL Circuits

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

The SN54187 and SN74187 circuits are custom-programmed, 1024-bit, read-only memories organized as 256 words of four bits each. These monolithic, high-speed transistor-transistor logic (TTL) memory arrays are addressed in straight eight-bit binary with full on-chip decoding. Two overriding memory-enable inputs are provided which, when either one or both are taken high, will inhibit the function causing all four outputs to remain high. Data, as specified by the customer, are permanently programmed into the monolithic structure for the 1024 bit locations. This organization is expandable to 41,472 words of n-bits with no additional output buffering.

The address of a four-bit word is accomplished through the buffered binary select inputs in coincidence with low-level voltages at both enable inputs. The most significant binary select inputs, D through H, are decoded internally in the X plane to select one-of-32 lines, and the least significant bits, A, B, and C, are internally decoded in the Y plane to accomplish one-of-eight decoding to drive the four output buffers. Where multiple SN54187 or SN74187 devices are used in a memory system, the enable input allows easy decoding of additional address bits.

Data are programmed into the memory cell at the emitters of 1024 transistors. The memory cell consists of a 32-by-32 matrix of transistors. In the X plane each of the 32 address decoding gate outputs supply common base drive to 32 transistors. In the Y plane the 32 transistors are arranged into four groups of eight. This permits each of the bit lines to be terminated in four one-of-eight decoders which achieves the four-bit word length.

The open-collector outputs are capable of sinking 16 milliamperes of current and may be wire-AND connected to increase the number of words available. The open-collector outputs may be utilized to drive external loads directly; however, dynamic response of the outputs can, in some cases, be improved by using an external pull-up resistor in conjunction with a partially loaded output.

The customer can specify the output logic level desired at each of the 1024 bit locations by completing the supplementary ordering data and a set of data cards punched in accordance with the data format shown under ordering instructions. Upon receipt of the order, Texas Instruments will assign a special device number to the device programmed according to the customer's order. The completed device will be marked with the TI special device number (not SN54187 or SN74187). It is important that the customer specify not only the output levels desired at all 1024 bit locations, but also the other information requested.

Access propagation delay time is typically 40 nanoseconds and power dissipation is typically 0.46 milliwatt per bit. The SN54187 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74187 is characterized for operation from 0°C to 70°C.

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) 7V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54187 Circuits . . . . . −55°C to 125°C
SN74187 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54187			SN74187			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 12 mA			0.4	V
			I_{OL} = 16 mA			0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		92	130	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, f = 1 MHz	V_O = 5 V,		6.5		pF

NOTE 2: With outputs open and both ME inputs grounded, I_{CC} is measured first by selecting a word which contains the maximum number of programmed high-level outputs, then by selecting a word which contains the maximum number of programmed low-level outputs.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

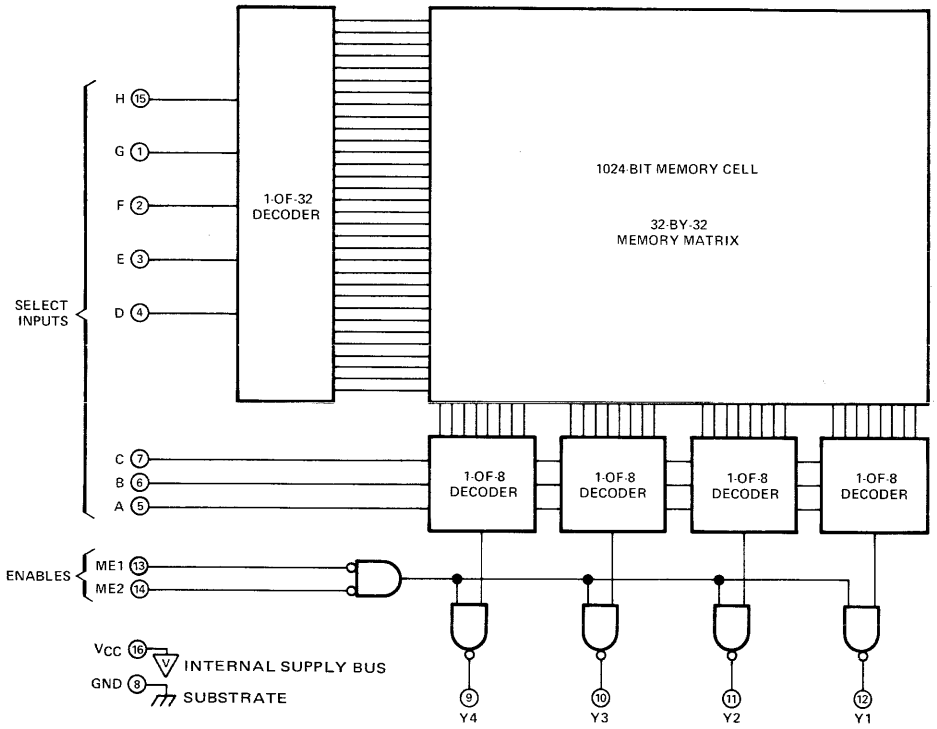
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

9

switching characteristics, V_{CC} = 5 V, T_A = 25°C

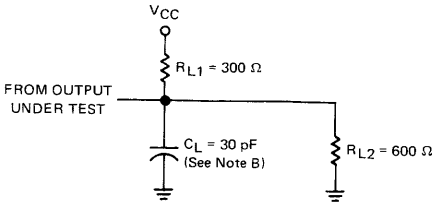
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from enable	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 1		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from enable			20	30	
t_{PLH}	Propagation delay time, low-to-high-level output from select			40	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from select			40	60	

functional block diagram

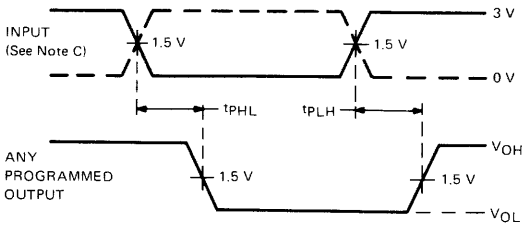


PARAMETER MEASUREMENT INFORMATION

9



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. The pulse generator is connected to the input under test. The other inputs, memory content permitting, are connected so that the input will switch the output under test.

FIGURE 1—PROPAGATION DELAY TIMES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

ORDERING INSTRUCTIONS

Programming instructions for the SN54187 or SN74187 are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under data card format, accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete truth table of the requested part. This truth table, showing output conditions for each of the 256 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the truth table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the eight words specified and describes the conditions at the four outputs for each of the eight words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

SUPPLEMENTARY ORDERING DATA

Submit the following information with the data cards:

a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number.

The following information will be furnished to the customer by Texas Instruments:

a) TI part number
b) TI sales order number
c) Date received.

DATA CARD FORMAT

Column	
1- 3	Punch a right-justified integer representing the binary input address (000-248) for the first set of outputs described on the card.
4	Punch a "–" (Minus sign)
5- 7	Punch a right-justified integer representing the binary input address (0007-255) for the last set of outputs described on the card.
8- 9	Blank
10-13	Punch "H", "L", or "X" for bits four, three, two, and one (outputs Y4, Y3, Y2, and Y1 in that order) for the first set of outputs specified on the card. H = high-level output, L = low-level output, X = output level irrelevant.
14	Blank
15-18	Punch "H", "L", or "X" for the second set of outputs.
19	Blank
20-23	Punch "H", "L", or "X" for the third set of outputs.
24	Blank
25-28	Punch "H" "L", or "X" for the fourth set of outputs.
29	Blank
30-33	Punch "H", "L", or "X" for the fifth set of outputs.
34	Blank
35-38	Punch "H", "L", or "X" for the sixth set of outputs.
39	Blank
40-43	Punch "H", "L", or "X" for the seventh set of outputs.
44	Blank
45-48	Punch "H", "L", or "X" for the eighth set of outputs.
49	Blank
50-51	Punch a right-justified integer representing the current calendar day of the month.
52	Blank
53-55	Punch an alphabetic abbreviation representing the current month.
56	Blank
57-58	Punch the last two digits of the current year.
59	Blank
60-61	Punch "SN"
62-66	Punch a left-justified integer representing the Texas Instruments part number. This is supplied by the factory through a TI sales representative.
67-68	Blank
69-80	Preferably these columns should be punched to reflect the customer's part or specification-control number. This information is not essential.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54170, SN74170
4-BY-4 REGISTER FILES

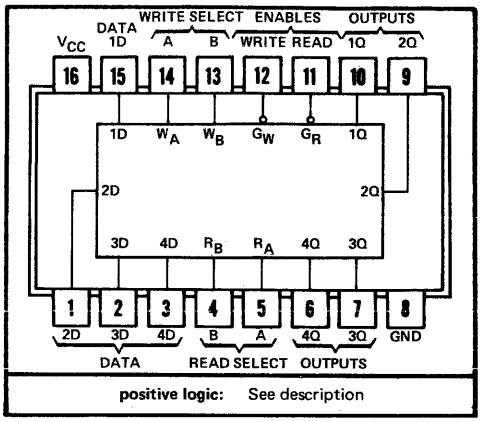
- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times . . . Typically 20 ns
- Open-Collector Outputs with 30-μA Maximum Off-State Current
- Organized as 4 Words of 4 Bits
- Expandable to 1024 Words of n-Bits
- For Use as:

  Scratch-Pad Memory

  Buffer Storage between Processors

  Fast Multiplication Schemes

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assigments for these circuits are the same for all packages.

description

The SN54170 and SN74170 MSI 16-bit TTL register files incorporate the equivalent of 98 gates on a monolithic chip measuring only 90 by 110 mils. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write enable input, G_W is high, the data inputs are inhibited and their states can cause no change in the information stored in the internal latches. When the read enable input, G_R, is high, the data outputs are inhibited and remain high.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (45 nanoseconds maximum) and the read time (35 nanoseconds maximum). The register file has a non-destructive readout in that data is not lost when addressed.

All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

Power dissipation is typically 500 mW total or 5 mW per gate. The SN54170 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74170 is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

logic

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_n	Q_n	Q_n
L	H	L	Q_n	Q = D	Q_n	Q_n
H	L	L	Q_n	Q_n	Q = D	Q_n
H	H	L	Q_n	Q_n	Q_n	Q = D
X	X	H	Q_n	Q_n	Q_n	Q_n

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	1Q	2Q	3Q	4Q
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES: A. H = high level, L = low level, X = irrelevant
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q_n = No change.
D. W0B1 = The first bit of word 0, etc.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Output voltage (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range: SN54170J Circuits . . . . . −55°C to 125°C
SN74170J, N Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

		SN54170			SN74170			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}				16			16	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data (see Note 3 and Figure 1)	data input with respect to write enable, $t_{setup(D)}$	10			10			ns
	write select with respect to write enable, $t_{setup(W)}$	15			15			ns
	read select with respect to read enable, $t_{setup(R)}$	5			5			ns
Hold times, high- or low-level data (see Note 4 and Figure 1)	data input with respect to write enable, $t_{hold(D)}$	0			0			ns
	write select with respect to write enable, $t_{hold(W)}$	5			5			ns
	read select with respect to read enable, $t_{hold(R)}$	5			5			ns
Latch time for new data, t_{latch} (see Note 5)		25			25			ns
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

NOTES: 3. Setup time is the interval immediately preceding the negative-going edge of the enable pulse during which interval the data or address to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the positive-going edge of the enable pulse during which interval the data or address to be recognized must be maintained at the input to ensure its continued recognition.
5. Latch time is the time required for the internal output of the latch to assume the state of new data. See Figure 1. This is important only when attempting to read from a location immediately after that location has received new data.

9

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN,	V_O = 5.5 V			30	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, see Note 6	SN54170		127‡	140	mA
			SN74170		127‡	150	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Typical power dissipation shown is an average for 50% duty cycle at V_{CC} = 5 V, T_A = 25°C.

NOTE 6: Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

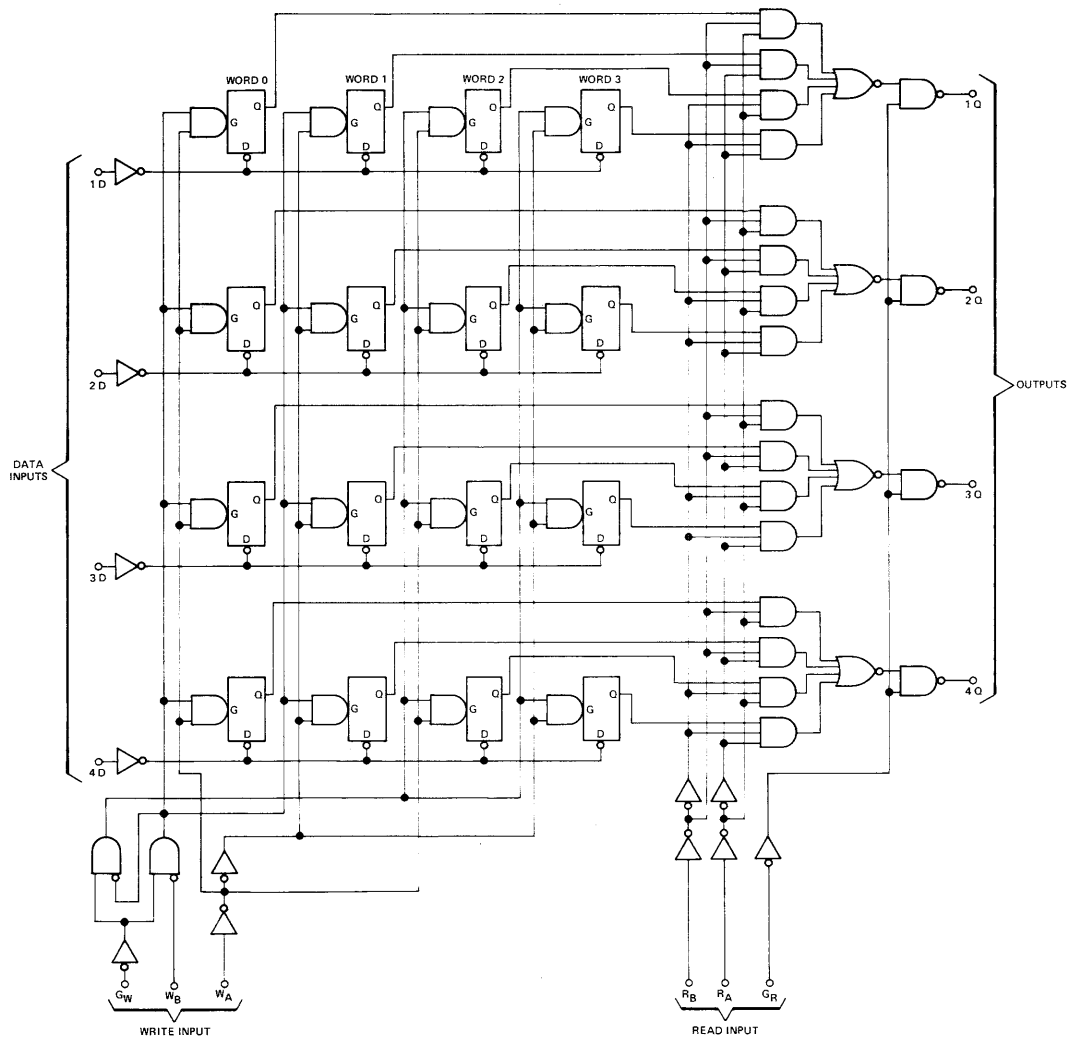
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from read enable to any Q	C_L = 15 pF,	R_L = 400 Ω		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from read enable to any Q	C_L = 15 pF,	R_L = 400 Ω		20	30	ns

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

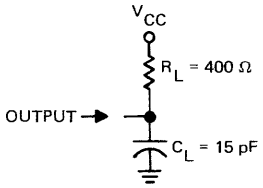
functional block diagram



9

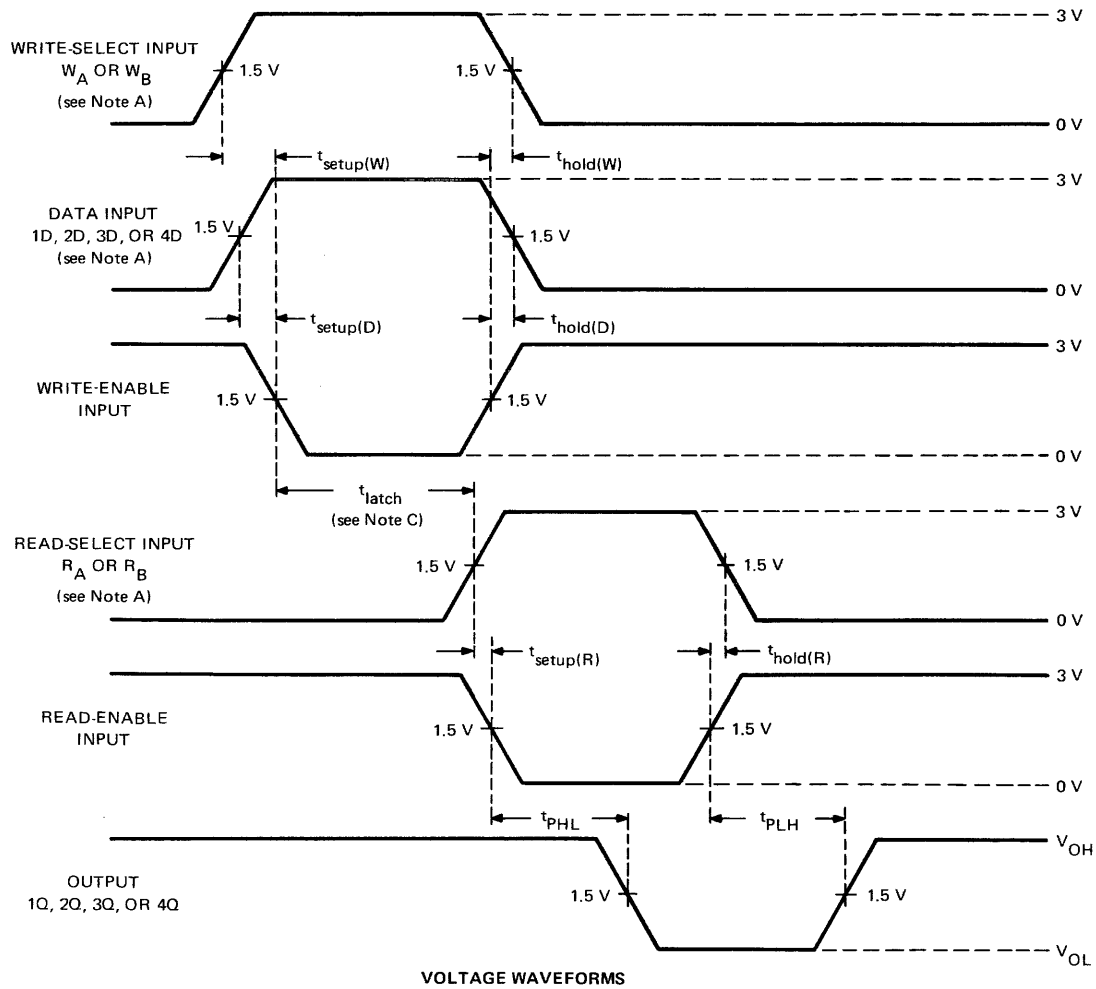
PARAMETER MEASUREMENT INFORMATION

switching characteristics



NOTE: C_L includes probe and jig capacitance.

LOAD FOR OUTPUT UNDER TEST



VOLTAGE WAVEFORMS

NOTES: A. High-level inputs are illustrated; however, low-level setup and hold times are the same.
B. Waveforms are supplied by generators with the following characteristics: PRR ⩽ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle ⩽ 50%, $t_r \leqslant 10$ ns, $t_f = 10$ ns.
C. This applies only when reading from a location immediately after that location has received new data.

FIGURE 1–SWITCHING TIMES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATION DATA

general

These register files may be cascaded to form n-bit registers with capacities of 1024 words. Word capacity is increased by wire-AND connecting the four outputs of a number of register files (up to 256). One write-select and one read-select register is required for all the paralleled files.

For increased word length (number of bits), a number of files may be selected and enabled simultaneously to provide the desired word length. This scheme is compatible for using parallel files to provide more words also. All inputs and outputs, except the write-enable and read-enable lines, are paralleled to add word capacity. The enable lines are separate for each word.

These register files can be used with improved efficiency in most applications that require a scratch-pad-type memory. Because recovery times are eliminated, the cycle time is a function of the longer of the write or read time. In the case of the SN54170/SN74170, this is the write time which is 45 nanoseconds maximum. The separate write and read address inputs permit efficient usage in applications where new data is entered throughout the memory during each cycle. A familiar example of this is a display in which the information moves across a panel of lights. The first display data is stored in the file, and as it is being read and displayed, the next display data is being written into the memory. More realistically, the SN54170/SN74170 is capable of operating at speeds that permit its use as a high-speed buffer memory between main memories or peripheral stations. In addition, the register file could be used to acquire tabular data, as a complete table or on a partial basis, recycling to present the entire bank of data.

high-speed buffer memory

These register files may also be organized differently on the read inputs than on the write outputs. As shown in Figure A, for example, the SN54170/SN74170 is utilized to acquire 256-bit words from the main memory and make 32-bit words available to the central processor unit (CPU). The 256-bit word is transferred in parallel to the buffer memory. A typical access time to the main memory is in the order of one microsecond. The buffer memory is organized so that the 256 bits of data are made available to the CPU in 32-bit words. Access time to data stored in the buffer register is 35 nanoseconds. In terms of frequency, data may be transferred from core memory to buffer memory at typically one megahertz; however, the transfer rate from buffer register to CPU is typically 20 megahertz when data setup time at the CPU is considered (30 nanoseconds propagation delay time through the SN54170/SN74170 and 10 to 20 nanoseconds data setup time in the CPU).

This buffer memory provides the following advantages:

- ability to simultaneously read and write means that the CPU is not interrupted as the buffer memory is being re-programmed
- the flexibility of organizing the write inputs and read outputs differently gives an effective main-memory access time of 125 nanoseconds:

$$\left(\frac{32\text{ bits}}{256\text{ bits}} \times 1\ \mu s\right) \text{ for one CPU word (32 bits).}$$

The concept of this organization is illustrated in Figure B which shows a 16-bit word being made available in 4-bit words. The 16-bit word is written simultaneously into word locations A, B, C, and D by a common write signal. Any 4-bit word may then be selected from these word locations by separate read-enable strobes.

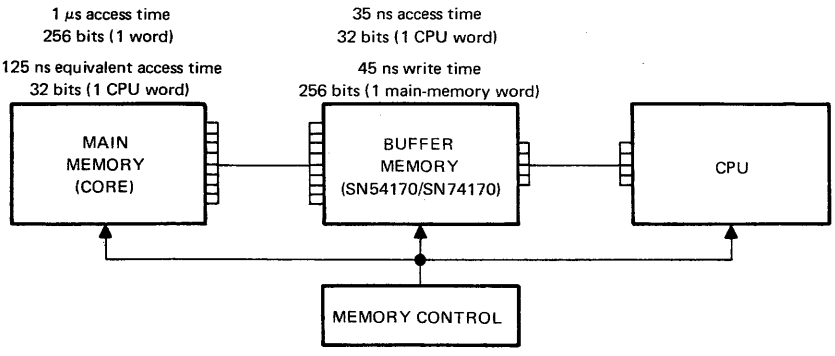


FIGURE A—HIGH-SPEED BUFFER MEMORY

TYPICAL APPLICATION DATA

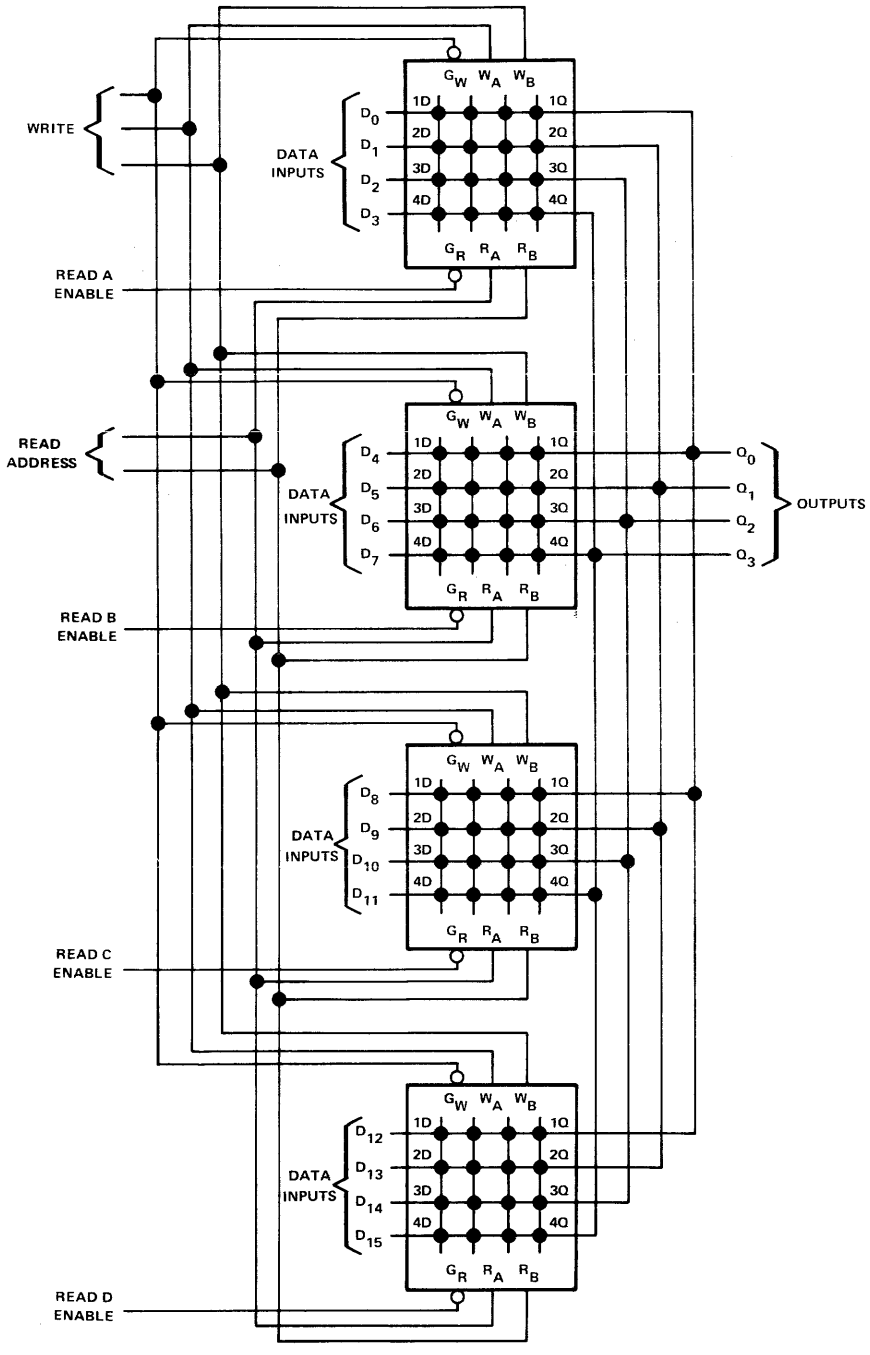


FIGURE 8—TYPICAL 16-BIT-WORD-TO-4-BIT-WORD BUFFER MEMORY

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

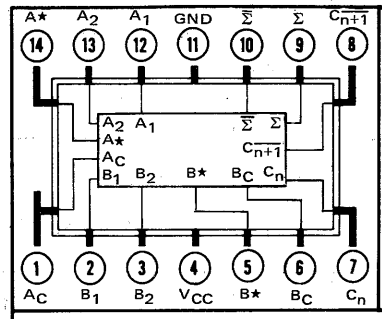
CIRCUIT TYPES SN5480, SN7480
GATED FULL ADDERS

logic

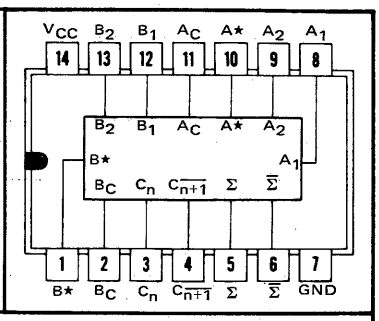
TRUTH TABLE
(See Notes 1, 2, and 3)

C_n	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	Σ
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See truth table

NOTES: 1. $A = \overline{A★ \cdot A_C}$, $B = \overline{B★ \cdot B_C}$ where $A★ = \overline{A_1 \cdot A_2}$, $B★ = \overline{B_1 \cdot B_2}$
2. When A★ or B★ are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to GND.
3. When A_1 and A_2 or B_1 and B_2 are used as inputs, A★or B★ respectively must be open or used to perform Dot-OR logic.

description

This single-bit, high-speed, binary full adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output is designed for medium- and high-speed, multiple-bit, parallel-add/serial-carry applications. The circuit (see schematic diagram) utilizes diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits.

absolute maximum ratings over operating temperature range (unless otherwise noted)

9

Supply Voltage V_{CC} (See Note 4) . . . . . 7 V
Input Voltage, V_{in} (See Notes 4 and 5) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5480 Circuits . . . . . −55°C to 125°C
SN7480 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5480 Circuits	4.5	5	5.5	V
SN7480 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs:				
$\overline{C_{n+1}}$, N			5	
Σ or $\overline{\Sigma}$, N			10	
A★ or B★, N			3	

NOTES: 4. The voltages are with respect to ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage	1 and 2			2			V
$V_{in(0)}$	Logical 0 input voltage	1 and 2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2			2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	1				0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, A_2, B_1, B_2, A_C or B_C	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at A* or B*	4	V_{CC} = MAX, V_{in} = 0.4 V				−2.6	mA
$I_{in(0)}$	Logical 0 level input current at C_n	4	V_{CC} = MAX, V_{in} = 0.4 V				−8	mA
$I_{in(1)}$	Logical 1 level input current at A_1, A_2, B_1, B_2, A_C or B_C	5	V_{CC} = MAX, V_{in} = 2.4 V				15	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at C_n	6	V_{CC} = MAX, V_{in} = 2.4 V				200	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current at Σ or $\overline{\Sigma}$§	7	V_{CC} = MAX	SN5480	−20		−57	mA
				SN7480	−18		−57	mA
I_{OS}	Short-circuit output current at $\overline{C_{n+1}}$§	7	V_{CC} = MAX	SN5480	−20		−70	mA
				SN7480	−18		−70	mA
I_{CC}	Supply current	8	V_{CC} = MAX	SN5480		21	31	mA
				SN7480		21	35	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

9

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	FIGURE 9 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_n	$\overline{C_{n+1}}$	1	C_L = 15 pF, R_L = 780 Ω		13	17	ns
t_{pd0}			2	C_L = 15 pF, R_L = 780 Ω		8	12	ns
t_{pd1}	B_C	$\overline{C_{n+1}}$	3	C_L = 15 pF, R_L = 780 Ω		18	25	ns
t_{pd0}			4	C_L = 15 pF, R_L = 780 Ω		38	55	ns
t_{pd1}	A_C	Σ	5	C_L = 15 pF, R_L = 400 Ω		52	70	ns
t_{pd0}			6	C_L = 15 pF, R_L = 400 Ω		62	80	ns
t_{pd1}	B_C	$\overline{\Sigma}$	7	C_L = 15 pF, R_L = 400 Ω		38	55	ns
t_{pd0}			8	C_L = 15 pF, R_L = 400 Ω		56	75	ns
t_{pd1}	A_1	A*	9	C_L = 15 pF		48	65	ns
t_{pd0}			10	C_L = 15 pF		17	25	ns
t_{pd1}	B_1	B*	11	C_L = 15 pF		48	65	ns
t_{pd0}			12	C_L = 15 pF		17	25	ns

¶ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

TYPICAL APPLICATIONS

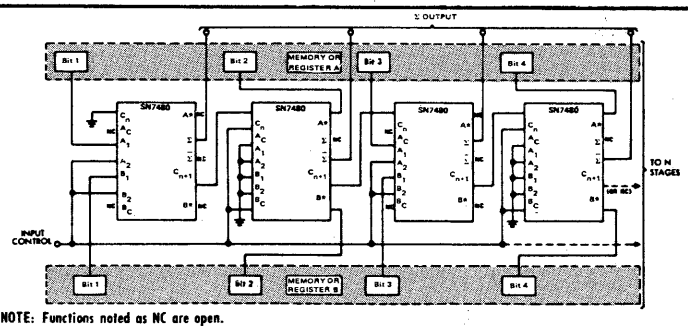
n-bit binary adder or subtractor (see figures A and B)

The SN7480 is designed specifically for N-bit adder or subtractor operations without external gates or inverters. In both applications, the sum or difference functions are generated in parallel while the carry functions are obtained serially. When the number of stages is small, the add or subtract time determines the maximum system clock rate. However, as the number of bits increases, the time required for the carry function to ripple through each bit becomes the limiting factor. Normally the ripple time of adders built with standard integrated circuits is excessive, and the resulting system speed is so slow that other more complex methods are required to perform these functions.

In the SN7480, two methods are used to reduce the carry delay. The carry circuit employs a high-speed Darlington output, and the logic gating has only one inversion between the C_n input and the $\overline{C_{n+1}}$ output. This logic configuration results in an inverted carry output, and consequently an inverted carry input to the succeeding stage. To counteract this inverted input without sacrificing propagation time through the carry, gates are provided within the circuit to invert the A and B inputs and the resulting sum or difference output. This interconnection method is illustrated by bit 2 and bit 4 of the adder (Figure A). The inverted carry output is a true carry from bit 2 and bit 4, enabling the use of noninverted A and B inputs for the odd-numbered bits.

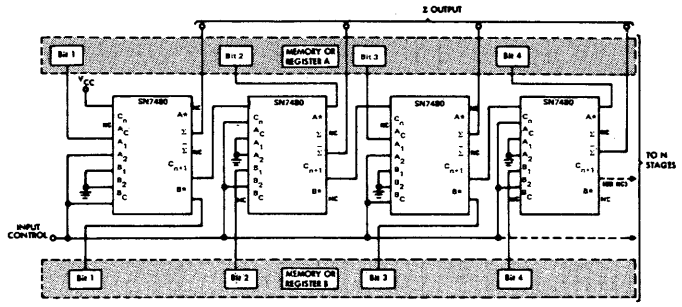
When performing subtraction (Figure B) the C_n input to bit 1 is connected to a logical 1 and input bits and input control functions for the subtrahend (memory or register B) are effectively inverted.

The input control is used to disable the A and B inputs when memory or register information is being shifted. A logical 0 applied to this line will bring each sum or difference output to a logical 0 condition and maintain this level regardless of the state of the input information into each bit. For the adder (Figure A), input control is applied to A_2 and B_2 of odd-numbered bits and to A_C and B_C of even numbered bits. For the subtractor (Figure B), input control is applied to A_2 and B_C of the odd-numbered bits and to A_C and B_2 of the even-numbered bits. These alternating patterns are necessary to complement the varying input sequence which they control.



NOTE: Functions noted as NC are open.

FIGURE A – N-BIT BINARY ADDER



NOTE: Functions noted as NC are open.

FIGURE B – N-BIT BINARY SUBTRACTOR

9

TYPICAL APPLICATIONS

n-bit binary adder with register selection (see figure C)

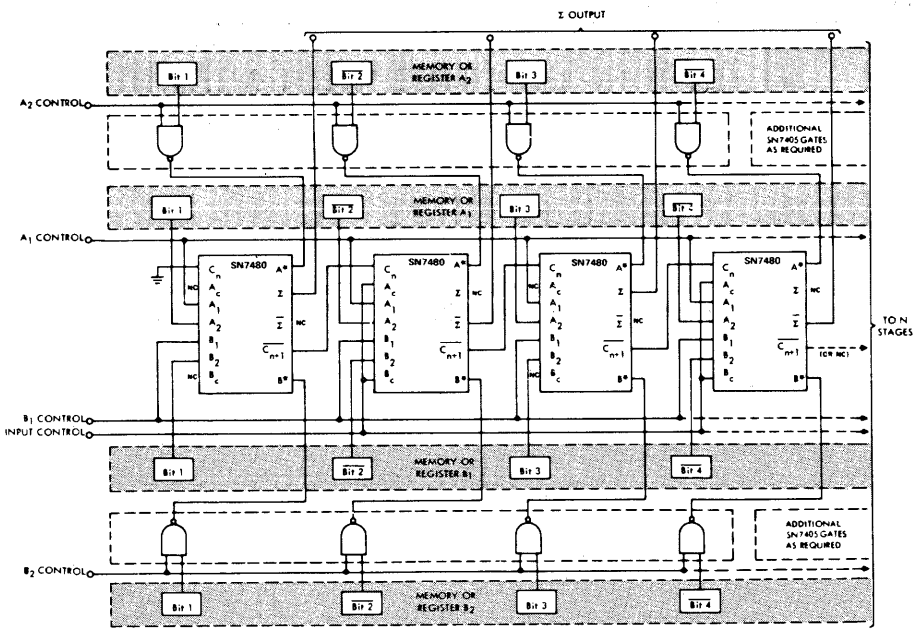
This application fully utilizes the flexibility of the input gating available within the SN7480. Two "A" registers and two "B" registers drive a single adder for each bit required. Register selection is performed internally for registers A_1 and B_1, and externally by a type SN7405 TTL gate for registers A_2 and B_2. Dot-OR logic is performed at the A★ and B★ nodes within the the adder when the register selection is made.

Operation is as follows: To add the contents of Register A_1 to Register B_1, A_2 and B_2 control lines are brought to the logical 0 state. In similar fashion, the contents of register A_1 are added to register B_2 by holding A_2 and B_1 control lines at a logical 0. Four register combinations may be used. Even-numbered input bits from each register must be inverted since the A★ and B★ inputs are being used to perform Dot-OR logic. This is not a configuration restriction for flip-flop type registers and memories, but may require additional logic elements if other storage configurations are used as inputs.

The input control function is available as in the previous application and is implemented by bringing all four register control lines and the input control line to a logical 0 level. This condition ensures a logical 0 at each Σ output regardless of "A" and "B" register logic levels.

Up to four "A" registers and four "B" registers may be implemented in a fashion analogous to that shown in Figure C. Inputs from the register-control gates (SN7405) of the additional registers would be Dot-OR connected with A_2 and B_2 registers at the A★ and B★ inputs.

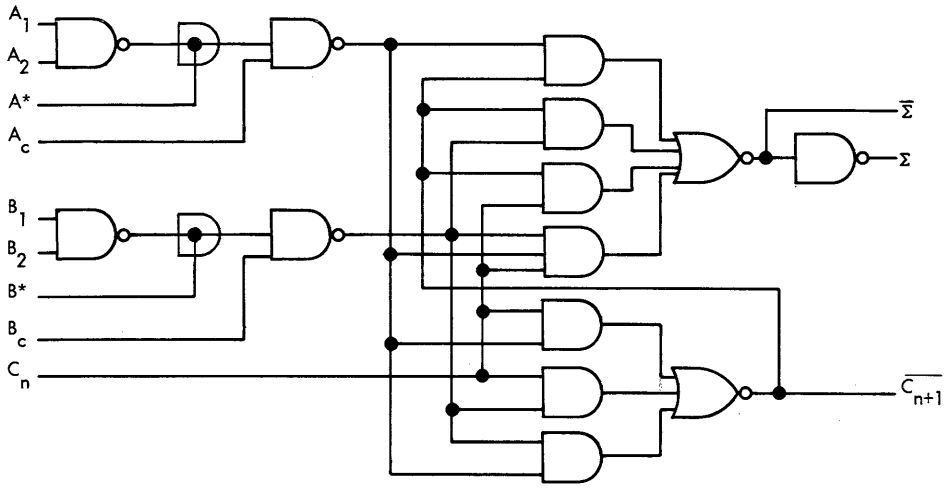
To perform N-bit subtraction, the C_n input at bit 1 is connected to a logical 1 and bit inputs from each register or memory used as a subtrahend must consist of the complement of bit inputs shown for the adder addend. Input control remains the same.



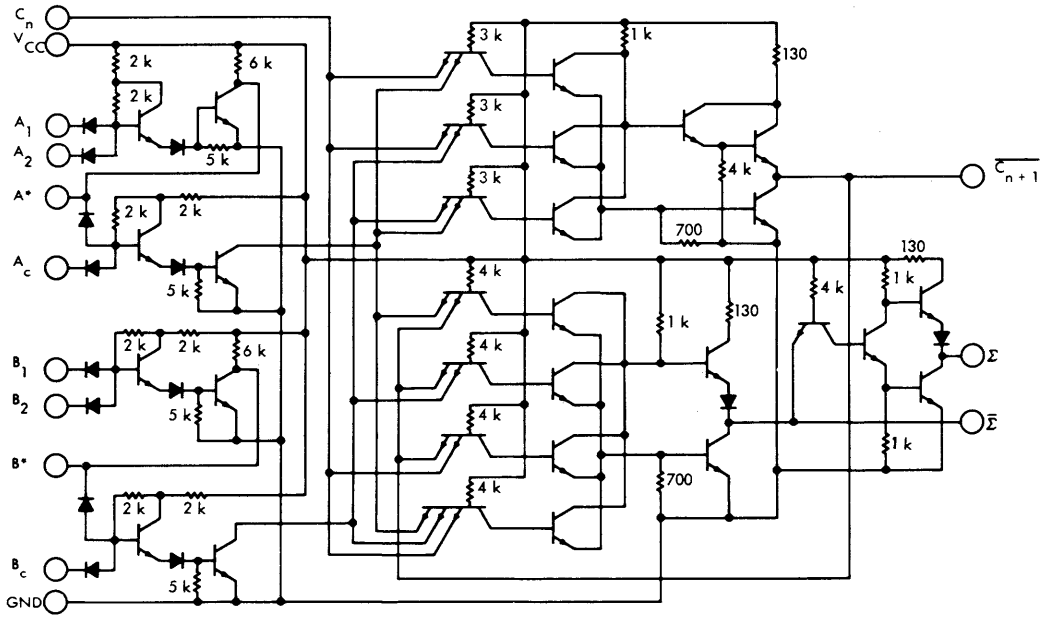
NOTE: Functions noted as NC are open.

FIGURE C—N-BIT ADDER WITH REGISTER SELECTION

functional block diagram



schematic

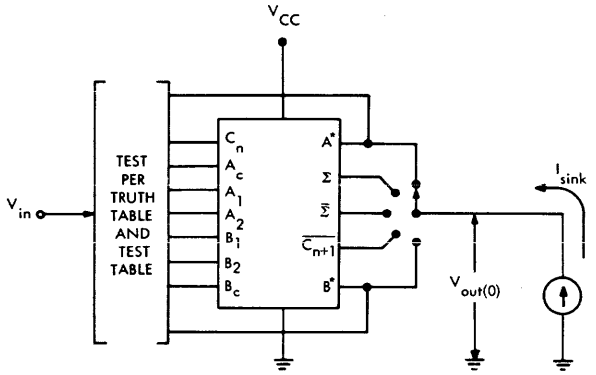


Component values shown are nominal.
Resistor values are in ohms.

9

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§

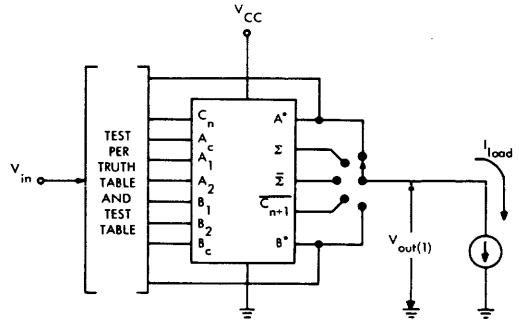


TEST TABLE

Output Under Test	I_{sink} (Min)
Σ or $\overline{\Sigma}$	16 mA
$\overline{C_{n+1}}$	8 mA
A★ or B★	4.8 mA

1. Each input or output is tested separately.
2. When A★ is tested A_1 and A_2 are at GND. When B★ is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 is tested, A★ or B★ respectively, is open.

FIGURE 1



TEST TABLE

Output Under Test	I_{load} (Min)
Σ or $\overline{\Sigma}$	-400 μA
$\overline{C_{n+1}}$	-200 μA
A★ or B★	-120 μA

1. Each input or output is tested separately.
2. When A★ is tested A_1 and A_2 are at GND. When B★ is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 are tested A★ or B★, respectively, is open.

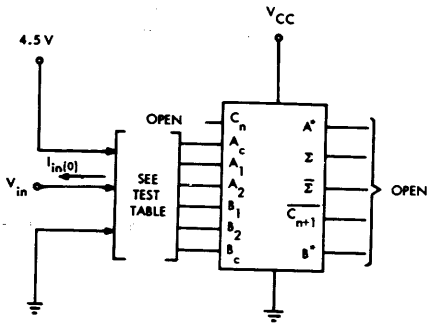
FIGURE 2

§Arrows indicate actual direction of current flow.

9

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

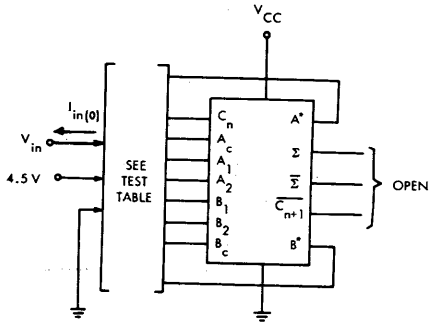


TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	GND
A_1	A_2	None
A_2	A_1	None
B_1	B_2	None
B_2	B_1	None
A_c	None	A_1 and A_2
B_c	None	B_1 and B_2

1. Each input is tested separately.

FIGURE 3



TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	GND
A★	A_c	A_1 and A_2
B★	B_c	B_1 and B_2
C_n	None	None

Unused inputs are open.

1. Each input is tested separately.

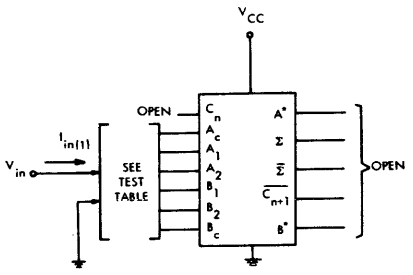
FIGURE 4

§Arrows indicate actual direction of current flow.

9

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each input is tested separately.

TEST TABLE

Apply V_{in} (Test $I_{in(1)}$)	GND
A_1	A_2
A_2	A_1
B_1	B_2
B_2	B_1
A_c	A★
B_c	B★

FIGURE 5

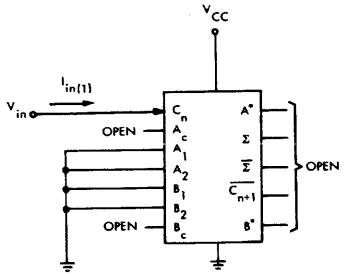
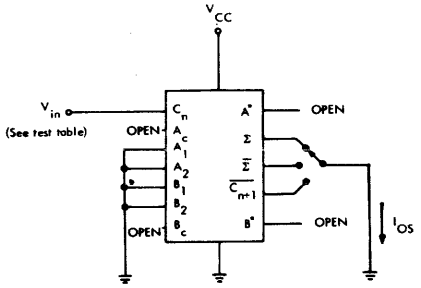


FIGURE 6



1. Each output is tested separately.

TEST TABLE

Output Under Test	V_{in} Value
Σ	V_{CC}
$\overline{\Sigma}$ or $\overline{C}_{n+1}$	GND

FIGURE 7

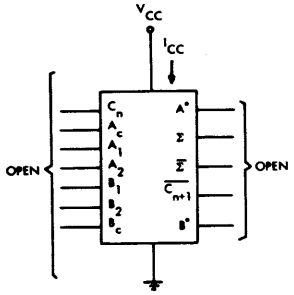
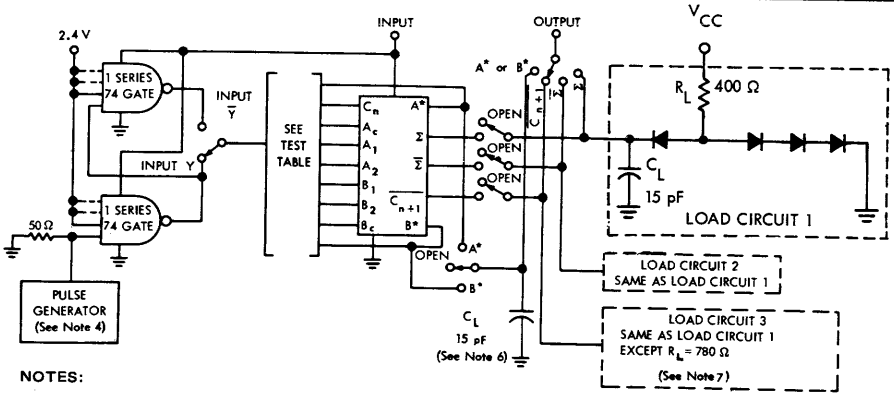


FIGURE 8

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

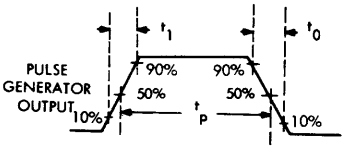
switching characteristics



NOTES:

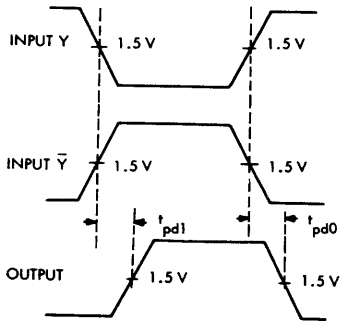
1. Perform test in accordance with test table.
2. Each output is tested separately.
3. Voltage values are with respect to network GND terminal.
4. The generator has the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leqslant 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
5. Inputs and outputs not otherwise specified are open.
6. C_L includes probe and jig capacitance.
7. Load circuit 2 simulates output load of 5.
8. All diodes are 1N3064.

TEST CIRCUIT



TEST TABLE (See Note 5)

TEST NO.	OUTPUT UNDER TEST	APPLY INPUT $\overline{Y}$ TO	APPLY INPUT Y TO	APPLY +2.4 V TO	APPLY GND TO	APPLY OUTPUT LOADING TO	
1	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$	(N = 5)
2	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$	(N = 5)
3	$\overline{C_{n+1}}$	B_c	None	C_n	A_1, B_1	$\overline{C_{n+1}}$	(N = 5)
4	$\overline{C_{n+1}}$	B_c	None	C_n	A_1, B_1	$\overline{C_{n+1}}$	(N = 5)
5	Σ	A_c	None	C_n	A_1, B_1	Σ	(N = 10)
						$\overline{\Sigma}$	(N = 10)
						$\overline{C_{n+1}}$	(N = 5)
6	Σ	A_c	None	C_n	A_1, B_1	Σ	(N = 10)
						$\overline{\Sigma}$	(N = 10)
						$\overline{C_{n+1}}$	(N = 5)
7	$\overline{\Sigma}$	B_c	None	C_n	B_1	$\overline{\Sigma}$	(N = 10)
8	$\overline{\Sigma}$	B_c	None	C_n	B_1	$\overline{\Sigma}$	(N = 10)
9	A★	None	A_1	A_2	None	A★	(C_L = 15 pF)
10	A★	None	A_1	A_2	None	A★	(C_L = 15 pF)
11	B★	None	B_1	B_2	None	B★	(C_L = 15 pF)
12	B★	None	B_1	B_2	None	B★	(C_L = 15 pF)



VOLTAGE WAVEFORMS

FIGURE 9 – SWITCHING TIMES

9

CIRCUIT TYPES SN5482, SN7482
2-BIT BINARY FULL ADDERS

A HIGH-SPEED TTL 2-BIT FULL ADDER FOR APPLICATION IN

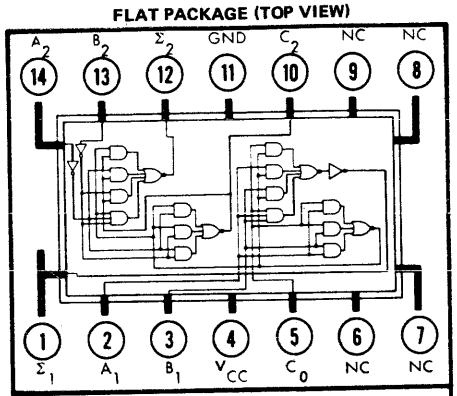
- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

TRUTH TABLE

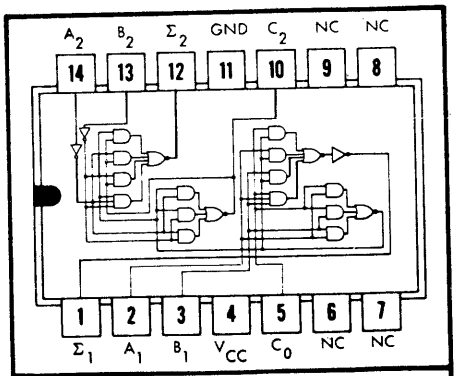
INPUT				OUTPUT					
				WHEN $C_0 = 0$			WHEN $C_0 = 1$		
A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_2	Σ_1	Σ_2	C_2
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

W
FLAT PACKAGE (TOP VIEW)



positive logic: see truth table

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

NC—No Internal Connection

9

description

This full adder performs the addition of two 2-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_2) is obtained from the second bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5482 Circuits . . . . . −55°C to 125°C
SN7482 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5482 Circuits	4.5	5	5.5	V
SN7482 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs:				
C_2			5	
Σ_1 or Σ_2			10	

electrical characteristics over recommended temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2			2.4			V
$V_{out(0)}$	Logical 0 output voltage	1					0.4	V
$I_{in(0)}$	*Logical 0 level input current at A_1, B_1, or C_0	3	V_{CC} = MAX, V_{in} = 0.4 V				−6.4	mA
$I_{in(0)}$	Logical 0 level input current at A_2 or B_2	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current at A_1, B_1, or C_0	3	V_{CC} = MAX, V_{in} = 2.4 V				160	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at A_2 or B_2	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current at Σ_1 or Σ_2§	4	V_{CC} = MAX	SN5482	−20		−55	mA
				SN7482	−18		−55	mA
I_{OS}	Short-circuit output current at C_2§	4	V_{CC} = MAX	SN5482	−20		−70	mA
				SN7482	−18		−70	mA
I_{CC}	Supply Current	3	V_{CC} = MAX	SN5482		35	50	mA
				SN7482		35	58	mA

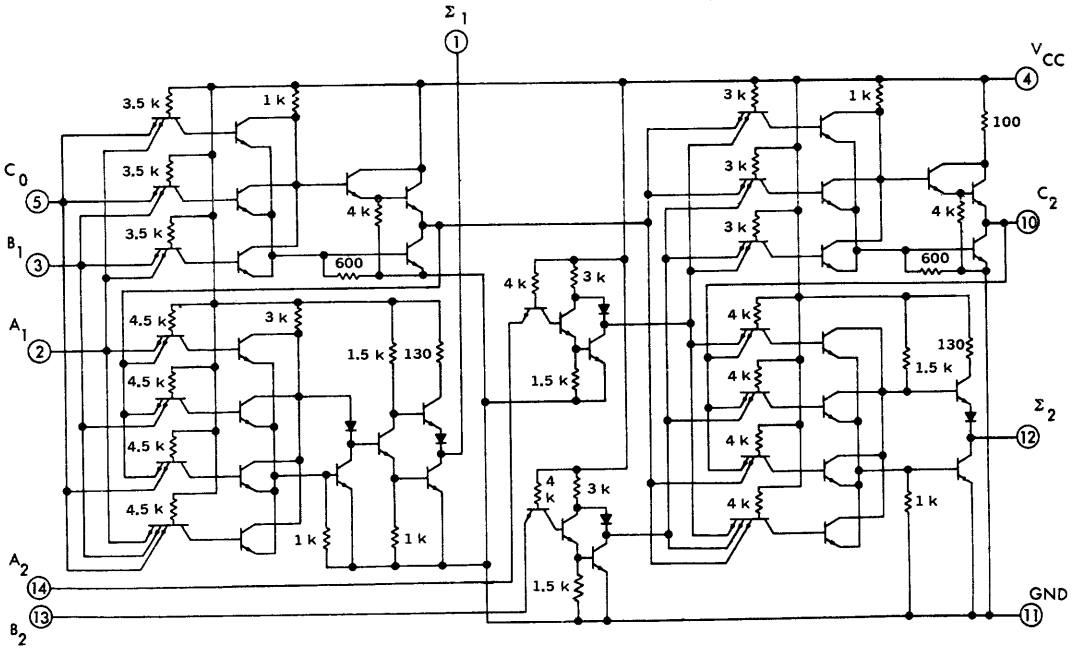
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted N = 10)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	FIGURE 5 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_0	Σ_1	1	C_L = 15 pF, R_L = 400 Ω			34	ns
t_{pd0}			2	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd1}	B_2	Σ_2	3	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd0}			4	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd1}	C_0	Σ_2	5	C_L = 15 pF, R_L = 400 Ω			38	ns
t_{pd0}			6	C_L = 15 pF, R_L = 400 Ω			42	ns
t_{pd1}	C_0	C_2	7	C_L = 15 pF, R_L = 780 Ω		12	19	ns
t_{pd0}			8	C_L = 15 pF, R_L = 780 Ω		17	27	ns

§ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

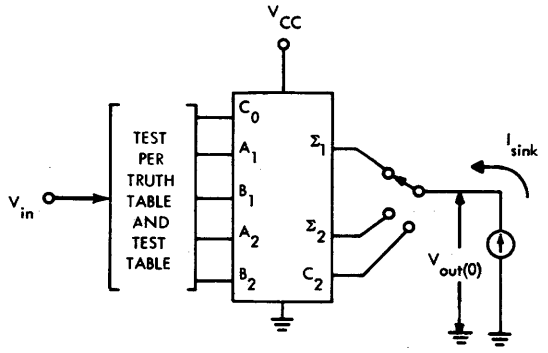
schematic



Component values shown are nominal.
Resistor values are in ohms.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

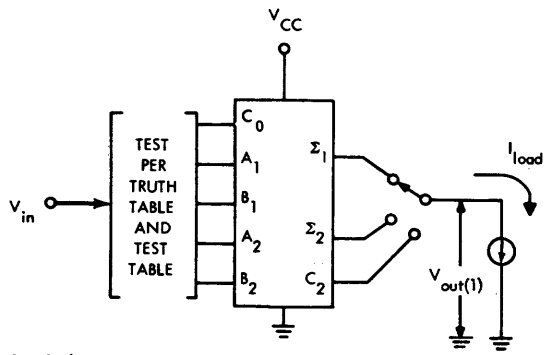


TEST TABLE

OUTPUT UNDER TEST	I_{sink}
Σ_1 or Σ_2	16 mA
C_2	8 mA

1. Each input or output is tested separately.

FIGURE 1



TEST TABLE

OUTPUT UNDER TEST	I_{load}
Σ_1 or Σ_2	−400 μA
C_2	−200 μA

1. Each input or output is tested separately.

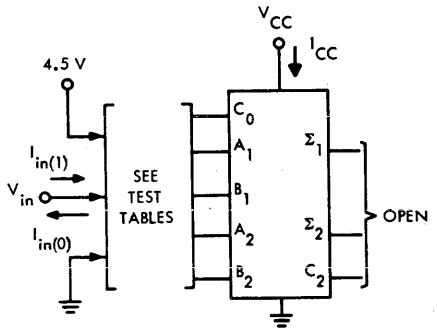
FIGURE 2

†Arrows indicate actual direction of current flow.

9

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



$I_{in(0)}$ TEST TABLE

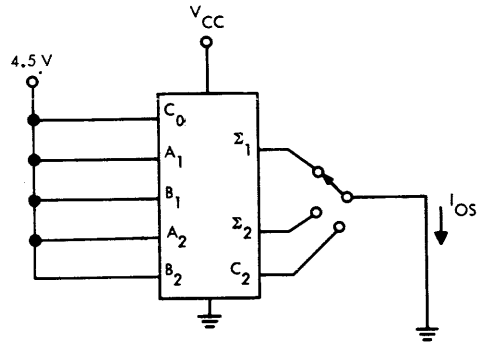
APPLY V_{in} TEST I_{in}	APPLY 4.5 V
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None

$I_{in(1)}$ TEST TABLE

APPLY V_{in} TEST I_{in}	GND
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None

1. Each input is tested separately.
2. When testing I_{CC} apply 4.5 V to A_1, A_2, and C_0; and ground B_1 and B_2.

FIGURE 3



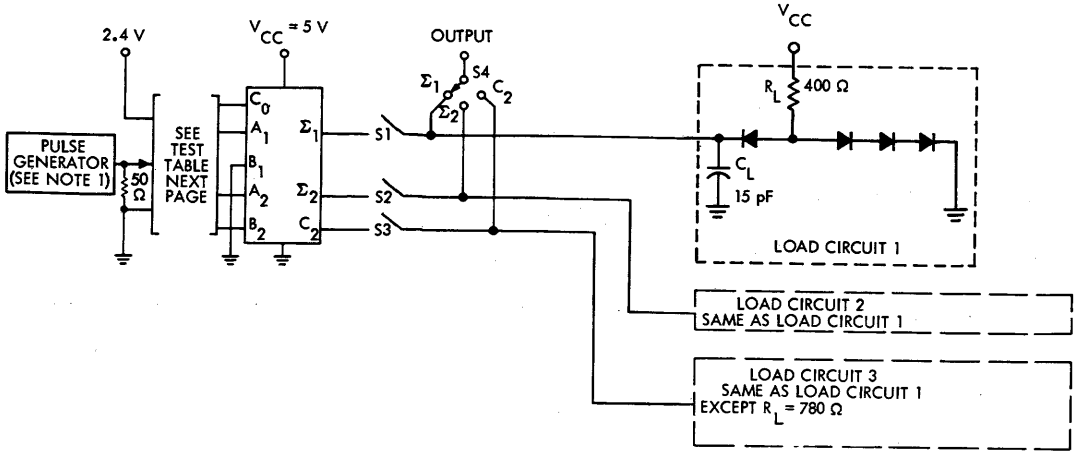
1. Each output is tested separately.

FIGURE 4

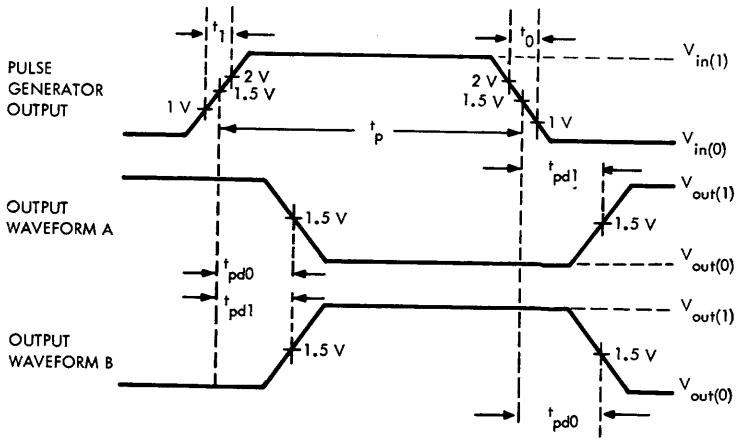
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: $V_{in(1)} \geq 2.4$ V, $V_{in(0)} \leq 0.4$ V, t_1 = 8 to 15 ns, t_0 = 3 to 5 ns, PRR = 1 MHz, t_p = 200ns, and $Z_{out} \approx 50\ \Omega$.
2. Perform test in accordance with test table.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064.

FIGURE 5–SWITCHING TIMES

9

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

SWITCHING TIMES TEST TABLE (SEE NOTE 7)

TEST NO.	PARAMETER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S4)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3
1	t_{pd1}	C_0	Σ_1 (WAVEFORM A)	A_1	A_2, B_1, B_2	CLOSED	OPEN	OPEN
2	t_{pd0}							
3	t_{pd1}	B_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, A_2 and C_0	OPEN	CLOSED	OPEN
4	t_{pd0}							
5	t_{pd1}	C_0	Σ_2 (WAVEFORM A)	A_1, A_2	B_1, B_2	OPEN	CLOSED	CLOSED
6	t_{pd0}							
7	t_{pd1}	C_0	C_2 (WAVEFORM B)	A_1, A_2	B_1, B_2	OPEN	OPEN	CLOSED
8	t_{pd0}							

NOTE 7: Inputs and outputs not otherwise specified are open.

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5483, SN7483
4-BIT BINARY FULL ADDERS

HIGH-SPEED TTL 4-BIT FULL ADDERS FOR APPLICATION IN

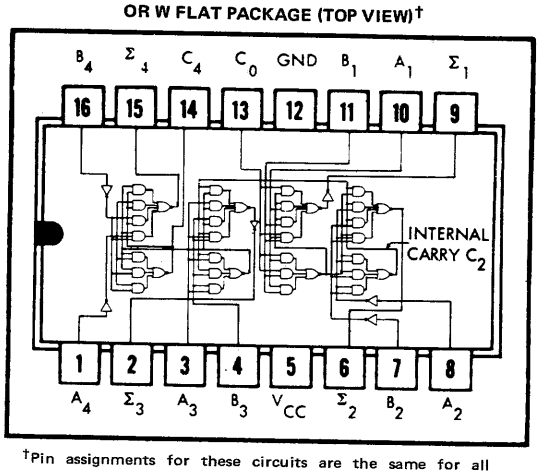
- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

INPUT							OUTPUT					
				WHEN $C_0 = 0$			WHEN $C_0 = 1$					
				WHEN $C_2 = 0$			WHEN $C_2 = 1$					
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4			
0	0	0	0	0	0	0	1	0	0			
1	0	0	0	1	0	0	0	1	0			
0	1	0	0	1	0	0	0	1	0			
1	1	0	0	0	1	0	1	1	0			
0	0	1	0	0	1	0	1	1	0			
1	0	1	0	1	1	0	0	0	1			
0	1	1	0	1	1	0	0	0	1			
1	1	1	0	0	0	1	1	0	1			
0	0	0	1	0	1	0	1	1	0			
1	0	0	1	1	1	0	0	0	1			
0	1	0	1	1	1	0	0	0	1			
1	1	0	1	0	0	1	1	0	1			
0	0	1	1	0	0	1	1	0	1			
1	0	1	1	1	0	1	0	1	1			
0	1	1	1	1	0	1	0	1	1			
1	1	1	1	0	1	1	1	1	1			

NOTE 1: Input conditions at A_1, A_2, B_1, B_2, and C_0 are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4, and C_4.

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

9

description

This full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform four-bit full-adder functions.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5483 Circuits . . . . . −55°C to 125°C
SN7483 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: (See Note 1)	SN5483 Circuits	4.5	5	5.5	V
	SN7483 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs:					
C_4				5	
Σ_1, Σ_2, Σ_3 or Σ_4				10	

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2			2.4			V
$V_{out(0)}$	Logical 0 output voltage	1					0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, A_3, B_1, B_3, or C_0	3	V_{CC} = MAX,	V_{in} = 0.4 V			−6.4	mA
$I_{in(0)}$	Logical 0 level input current at A_2, A_4, B_2, or B_4	3	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current at A_1, A_3, B_1, B_3, or C_0	3	V_{CC} = MAX,	V_{in} = 2.4 V			160	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at A_2, A_4, B_2, or B_4	3	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current at Σ_1, Σ_2, Σ_3, or Σ_4§	4	V_{CC} = MAX	SN 5483	−20		−55	mA
				SN7483	−18		−55	mA
I_{OS}	Short-circuit output current at C_4§	4	V_{CC} = MAX	SN5483	−20		−70	mA
				SN7483	−18		−70	mA
I_{CC}	Supply Current	3	V_{CC} = MAX,	SN5483		78	110	mA
				SN7483		78	128	mA

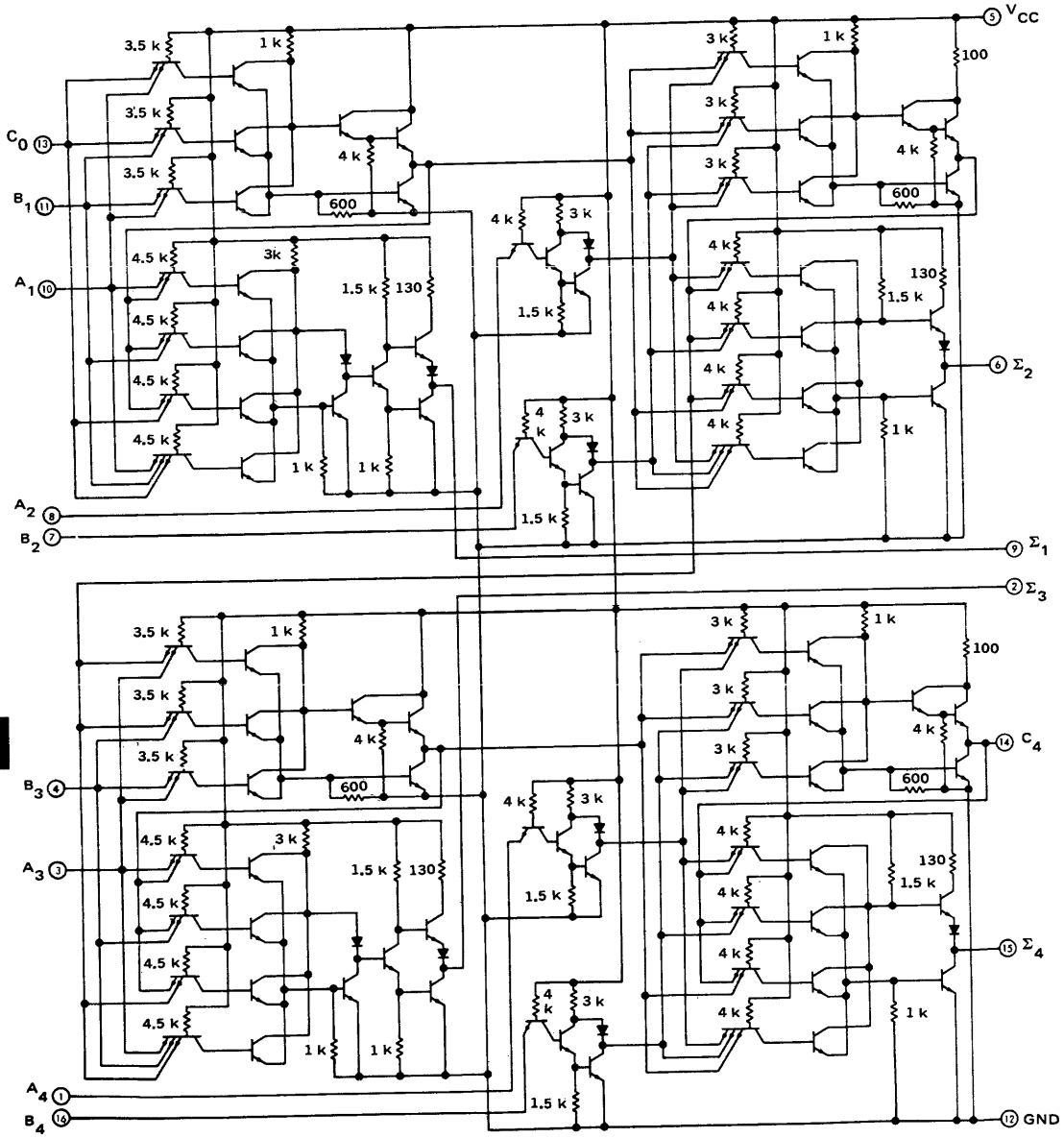
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted N = 10)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	FIGURE 5 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_0	1	1	C_L = 15 pF, R_L = 400 Ω			34	ns
t_{pd0}			2	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd1}	C_0	2	3	C_L = 15 pF, R_L = 400 Ω			38	ns
t_{pd0}			4	C_L = 15 pF, R_L = 400 Ω			42	ns
t_{pd1}	C_0	3	5	C_L = 15 pF, R_L = 400 Ω			50	ns
t_{pd0}			6	C_L = 15 pF, R_L = 400 Ω			60	ns
t_{pd1}	C_0	4	7	C_L = 15 pF, R_L = 400 Ω			55	ns
t_{pd0}			8	C_L = 15 pF, R_L = 400 Ω			55	ns
t_{pd1}	C_0	C_4	9	C_L = 15 pF, R_L = 780 Ω		35	48	ns
t_{pd0}			10	C_L = 15 pF, R_L = 780 Ω		22	32	ns
t_{pd1}	A_2 or B_2	2	11 and 13	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd0}			12 and 14	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd1}	A_4 or B_4	4	15 and 17	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd0}			16 and 18	C_L = 15 pF, R_L = 400 Ω			35	ns

§ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

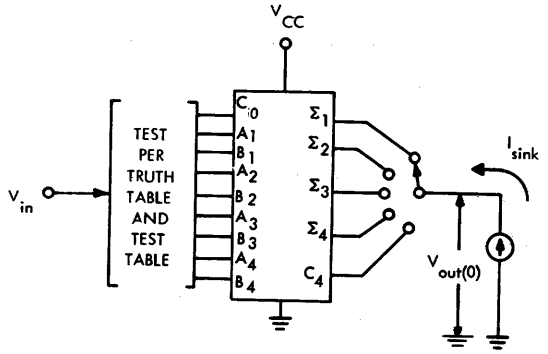
schematic



Component values shown are nominal.
Resistor values are in ohms.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

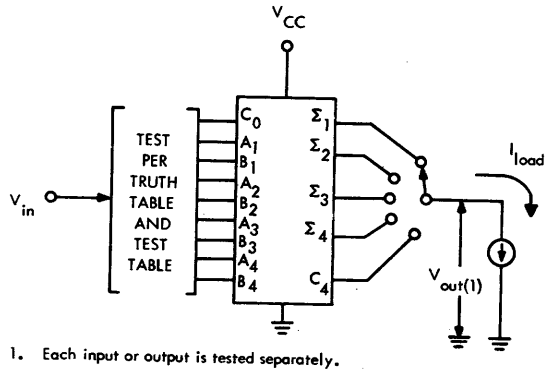


TEST TABLE

OUTPUT UNDER TEST	I_{sink}
Σ_1, Σ_2, Σ_3, or Σ_4	16 mA
C_4	8 mA

1. Each input or output is tested separately.

FIGURE 1



TEST TABLE

OUTPUT UNDER TEST	I_{load}
Σ_1, Σ_2, Σ_3, or Σ_4	− 400 μA
C_4	− 200 μA

1. Each input or output is tested separately.

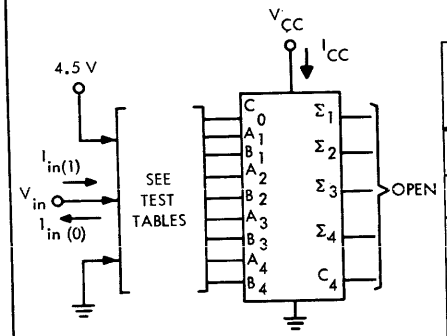
FIGURE 2

†Arrows indicate actual direction of current flow.

9

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



1. Each input is tested separately.
2. When testing I_{CC} apply 4.5 V to A_1, A_2, A_3, A_4, and C_0; and ground B_1, B_2, B_3 and B_4.

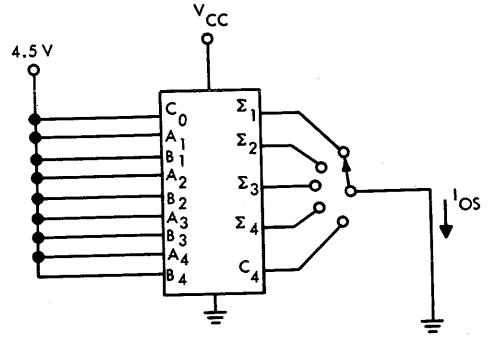
$I_{in(0)}$ TEST TABLE

APPLY V_{in} TEST I_{in}	APPLY 4.5 V
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None
A_3	A_2, B_2, and B_3
B_3	A_2, B_2, and A_3
A_4	None
B_4	None

$I_{in(1)}$ TEST TABLE

APPLY V_{in} TEST I_{in}	GND
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None
A_3	A_2, B_2, and B_3
B_3	A_2, B_2, and A_3
A_4	None
B_4	None

FIGURE 3



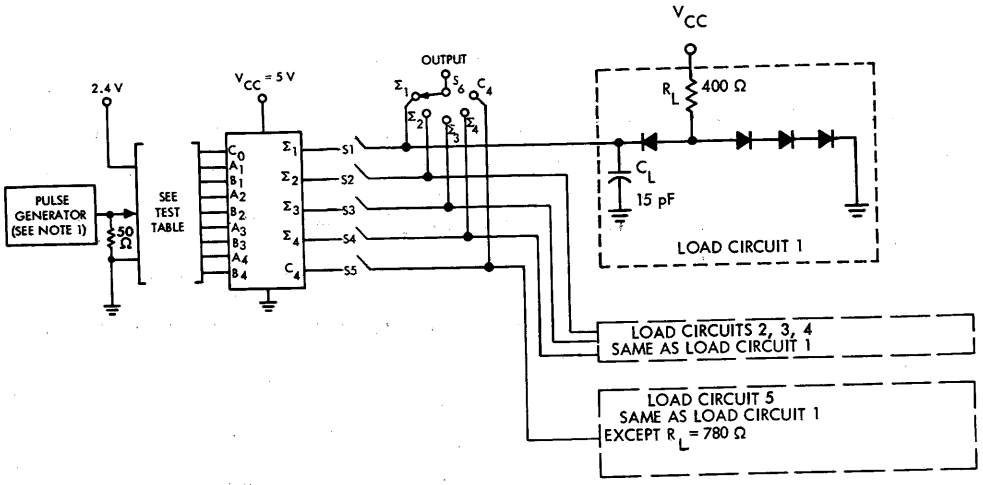
1. Each output is tested separately.

FIGURE 4

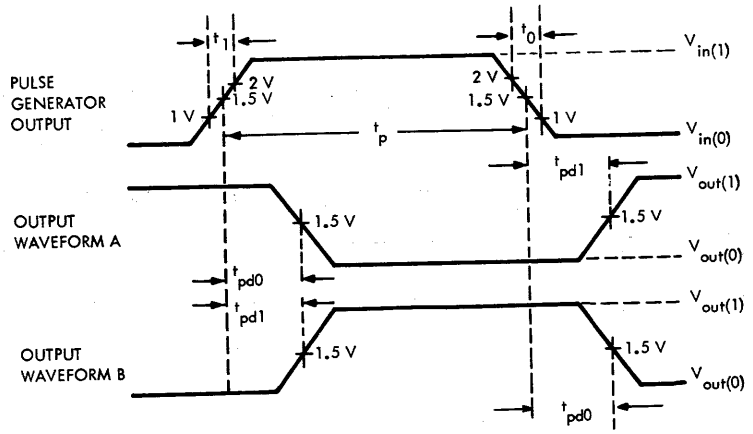
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. Pulse generator output pulse characteristics: $V_{in(1)} \geq$ 2.4 V, $V_{in(0)} \leq$ 0.4 V, t_1 = 8 to 15 ns, t_0 = 3 to 5 ns, PRR = 1 MHz, t_p = 200 ns, and $Z_{out} \approx$ 50 Ω.

2. Perform test in accordance with test table. (See sheet 2 of this figure.)
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064

FIGURE 5–SWITCHING TIMES (SHEET 1 OF 2)

9

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

TEST TABLE (SEE NOTE 7)

TEST NO.	PARAMETER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S6)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3	S4	S5
1	t_{pd1}	C_0	Σ_1 (WAVEFORM A)	A_1	B_1, A_2, and B_2	CLOSED	OPEN	OPEN	OPEN	OPEN
2	t_{pd0}									
3	t_{pd1}	C_0	Σ_2 (WAVEFORM A)	A_1 and A_2	B_1 and B_2	OPEN	CLOSED	OPEN	OPEN	OPEN
4	t_{pd0}									
5	t_{pd1}	C_0	Σ_3 (WAVEFORM A)	A_1, A_2, and A_3	B_1, B_2, and B_3	OPEN	OPEN	CLOSED	OPEN	OPEN
6	t_{pd0}									
7	t_{pd1}	C_0	Σ_4 (WAVEFORM A)	A_1, A_2, A_3, and A_4	B_1, B_2, B_3, and B_4	OPEN	OPEN	OPEN	CLOSED	CLOSED
8	t_{pd0}									
9	t_{pd1}	C_0	C_4 (WAVEFORM B)	A_1, A_2, A3, and A_4	B_1, B_2, B_3, and B_4	OPEN	OPEN	OPEN	OPEN	CLOSED
10	t_{pd0}									
11	t_{pd1}	A_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, B_2, and C_0	OPEN	CLOSED	OPEN	OPEN	OPEN
12	t_{pd0}									
13	t_{pd1}	B_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, A_2, and C_0	OPEN	CLOSED	OPEN	OPEN	OPEN
14	t_{pd0}									
15	t_{pd1}	A_4	Σ_4 (WAVEFORM B)	None	A_3, B_3, and B_4	OPEN	OPEN	OPEN	CLOSED	OPEN
16	t_{pd0}									
17	t_{pd1}	B_4	Σ_4 (WAVEFORM B)	None	A_3, B_3, and A_4	OPEN	OPEN	OPEN	CLOSED	OPEN
18	t_{pd0}									

NOTE 7: Inputs and outputs not otherwise specified are open.

FIGURE 5 – SWITCHING TIMES (SHEET 2 of 2)

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54LS83, SN74LS8
4-BIT BINARY FULL ADDER

BULLETIN NO. DL-S 7111458, MARCH 1971

HIGH-SPEED TTL 4-BIT FULL ADDERS

- Schottky-Diode-Clamped Transistors †
- Low Power Dissipation 75 mW Typical

FOR APPLICATION IN

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

description

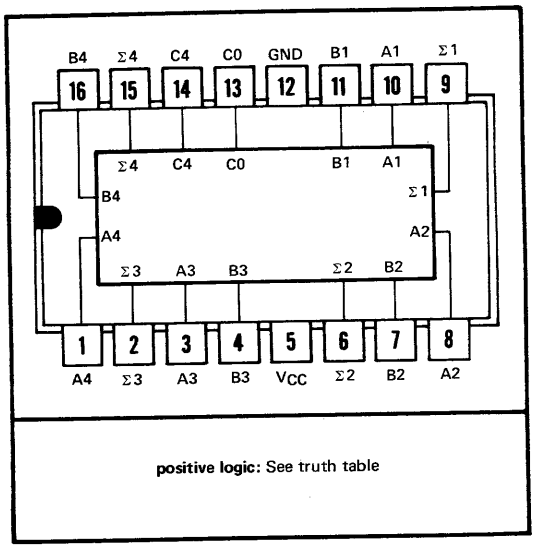
The SN54LS83 and SN74LS83 low-power Schottky TTL circuits are implemented with full Schottky-barrier-diode clamping to achieve speeds comparable to Standard Series 54/74 at one-fifth of the power. They retain the desirable features of, and are completely compatible with, most of the popular saturated logic circuits. Schottky TTL circuits currently offer the best speed-power products of any high-speed logic family.

Schottky-barrier-diode clamping prevents transistors from achieving classic saturation and thereby effectively eliminates excess charge storage and subsequent recovery times. These recovery times contribute significantly to overall propagation delays experienced with saturated digital-logic circuits.

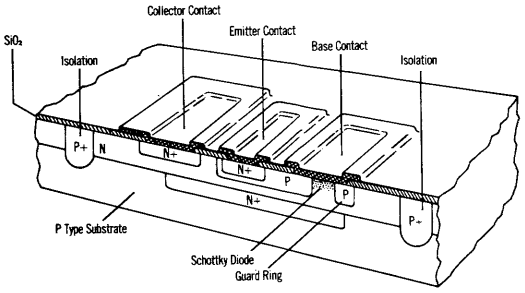
These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. Designed for medium-to-high-speed, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level is an order of magnitude below that attainable with standard integrated circuits connected to perform four-bit full-adder functions.

The SN54LS83 and SN74LS83 are completely compatible with the Series 54/74, Series 54H/74H, Series 54L/74L, and Series 54S/74S logic families. The SN54LS83 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS83 is characterized for operation from 0°C to 70°C.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See truth table



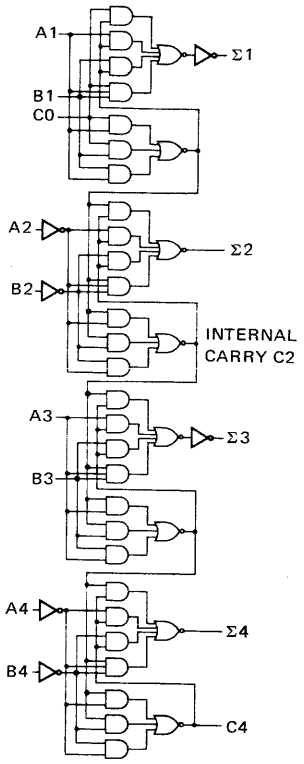
9

271

†The integrated Schottky-barrier-diode-clamped transistor is patented by Texas Instruments. U.S. patent number 3,463,975.

CIRCUIT TYPES SN54LS83, SN74LS83
4-BIT BINARY FULL ADDERS

functional block diagram



TRUTH TABLE

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
						WHEN C2 = L			WHEN C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

NOTE 1: Input conditions at A1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4, are then used to determine outputs Σ3, Σ4, and C4.

9 absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54LS83 Circuits . . . . . −55°C to 125°C
SN74LS83 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor.

recommended operating conditions

	SN54LS83			SN74LS83			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−200			−200	μA
Low-level output current, I_{OL}			4			4	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		1 and 2			2			V
V_{IL}	Low-level input voltage		1 and 2					0.9	V
V_I	Input clamp voltage		3	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage		2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.9 V, I_{OH} = −200 μA		2.4			V
V_{OL}	Low-level output voltage		1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.9 V, I_{OL} = 4 mA				0.5	V
I_I	Input current at maximum input voltage		3	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	A1, A3, B1, B3, or C0	3	V_{CC} = MAX, V_I = 2.4 V				160	μA
		A2, A4, B2, or B4						40	
I_{IL}	Low-level input current	A1, A3, B1, B3, or C0	3	V_{CC} = MAX, V_I = 0.5 V				−1.44	mA
		A2, A4, B2, or B4						−0.36	
I_{OS}	Short-circuit output current§		4	V_{CC} = MAX		−6		−40	mA
I_{CC}	Supply current		5	V_{CC} = MAX	SN54LS83		15	22	mA
					SN74LS83		15	26	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted N = 10)

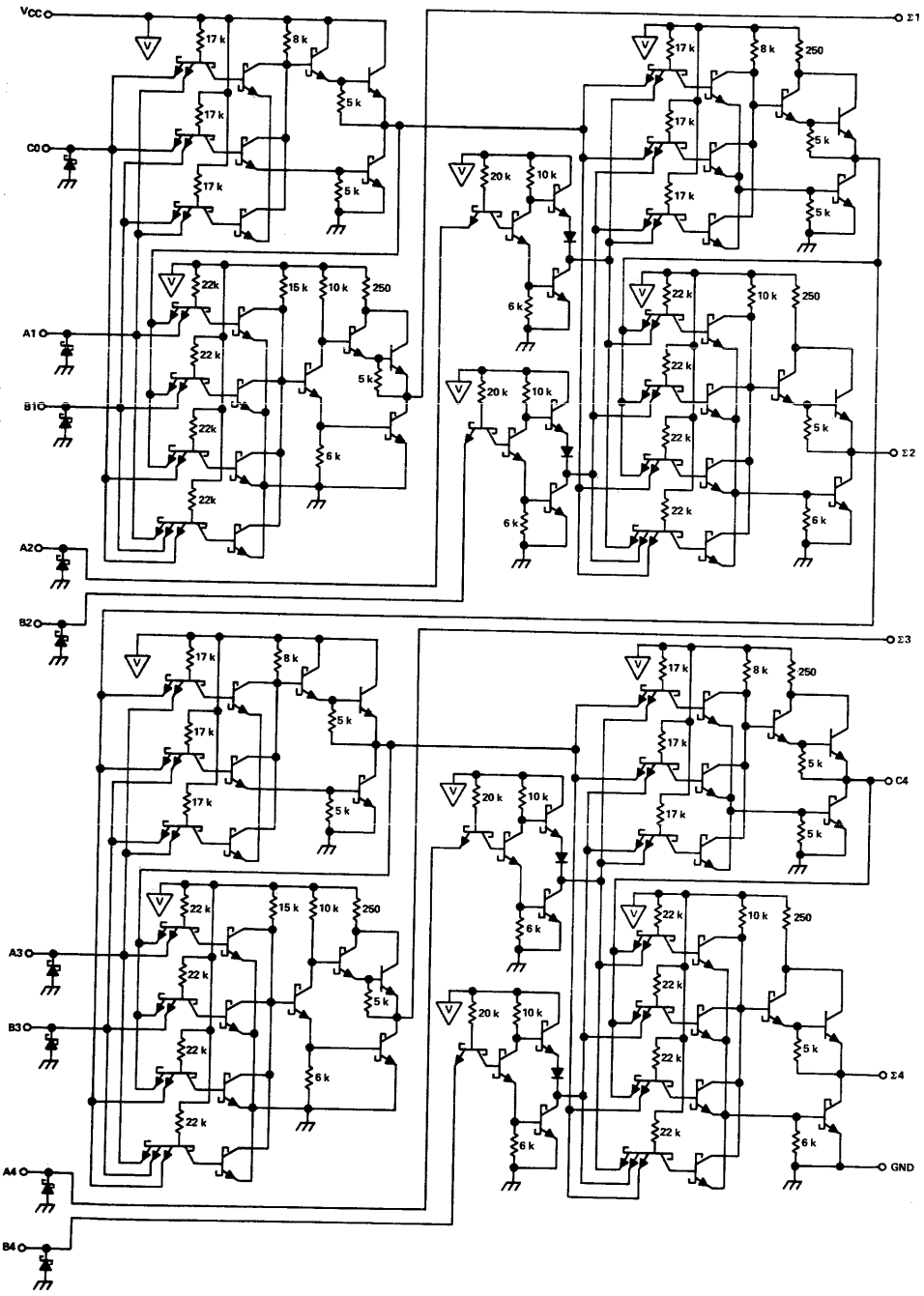
PARAMETER¶	FROM INPUT	TO OUTPUT	FIGURE 6 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Σ1	1	C_L = 50 pF, R_L = 2 kΩ		31		ns
t_{PHL}			2			38		ns
t_{PLH}	C0	Σ2	3			49		ns
t_{PHL}			4			45		ns
t_{PLH}	C0	Σ3	5			53		ns
t_{PHL}			6			66		ns
t_{PLH}	C0	Σ4	7			70		ns
t_{PHL}			8			69		ns
t_{PLH}	C0	C4	9			50		ns
t_{PHL}			10			50		ns
t_{PLH}	A2 or B2	Σ2	11 and 13			35		ns
t_{PHL}			12 and 14			30		ns
t_{PLH}	A4 or B4	Σ4	15 and 17			35		ns
t_{PHL}			16 and 18			30		ns

¶t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output.

9

CIRCUIT TYPES SN54LS83, SN74LS83
4-BIT BINARY FULL ADDERS

schematic



▽ . . . V_{CC} bus

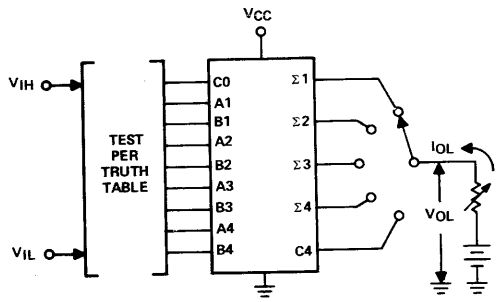
Resistor values are nominal in ohms.

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

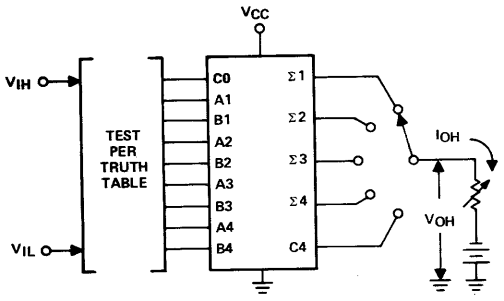
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



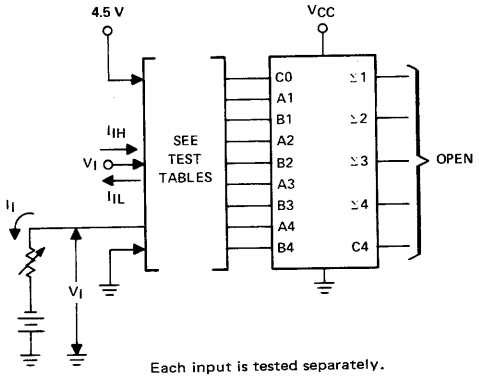
Each input or output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OL}



Each input or output is tested separately.

FIGURE 2–V_{IH}, V_{IL}, V_{OH}



Each input is tested separately.

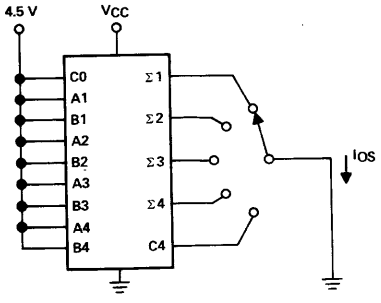
V_I, I_{IL} TEST TABLE

APPLY I_I, TEST V_I OR APPLY V_I, TEST I_{IL}	APPLY 4.5 V
C0	A1 and B1
A1	C0 and B1
B1	C0 and A1
A2	None
B2	None
A3	A2, B2, and B3
B3	A2, B2, and A3
A4	None
B4	None

I_{IH} TEST TABLE

APPLY V_I TEST I_{IH}	GND
C0	A1 and B1
A1	C0 and B1
B1	C0 and A1
A2	None
B2	None
A3	A2, B2, and B3
B3	A2, B2, and A3
A4	None
B4	None

FIGURE 3–V_I, I_{IL}, I_{IH}



Each output is tested separately.

FIGURE 4–I_{OS}

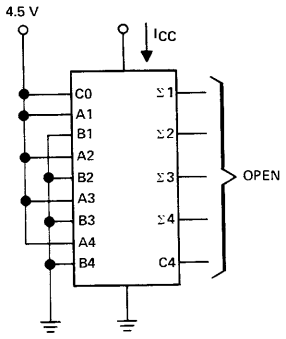
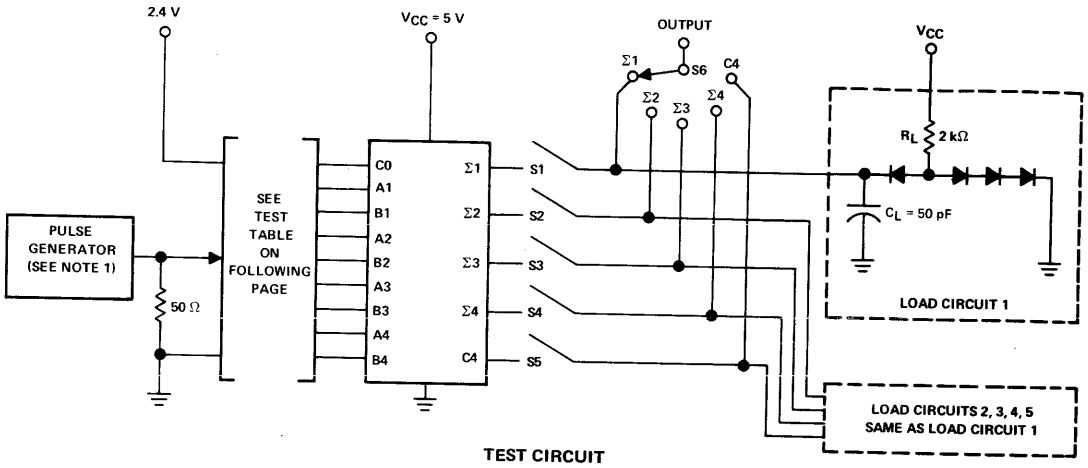


FIGURE 5–I_{CC}

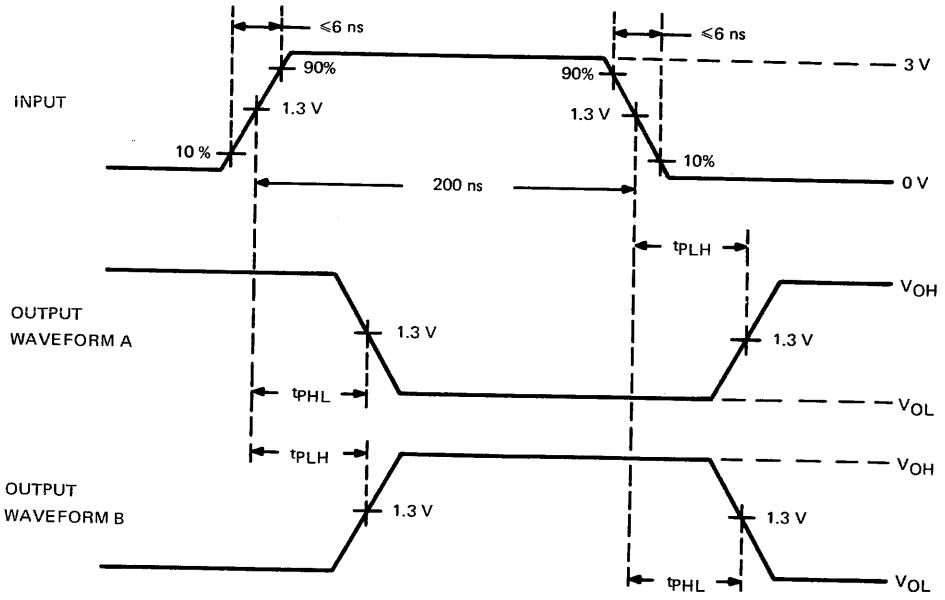
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES
1. The pulse generator has the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. Perform test in accordance with test table. (See sheet 2 of this figure.)
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064.

FIGURE 6–SWITCHING TIMES (SHEET 1 OF 2)

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

TEST TABLE (SEE NOTE 7)

TEST NO.	PARAMETER	INPUT UNDER TEST	OUTPUT UNDER TEST (S6)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3	S4	S5
1	t_{PLH}	C0	Σ1 (Waveform A)	A1	B1, A2, and B2	Closed	Open	Open	Open	Open
2	t_{PHL}									
3	t_{PLH}	C0	Σ2 (Waveform A)	A1 and A2	B1 and B2	Open	Closed	Open	Open	Open
4	t_{PHL}									
5	t_{PLH}	C0	Σ3 (Waveform A)	A1, A2, and A3	B1, B2, and B3	Open	Open	Closed	Open	Open
6	t_{PHL}									
7	t_{PLH}	C0	Σ4 (Waveform A)	A1, A2, A3, and A4	B1, B2, B3, and B4	Open	Open	Open	Closed	Closed
8	t_{PHL}									
9	t_{PLH}	C0	C4 (Waveform B)	A1, A2, A3, and A4	B1, B2, B3, and B4	Open	Open	Open	Open	Closed
10	t_{PHL}									
11	t_{PLH}	A2	Σ2 (Waveform B)	None	A1, B1, B2, and C0	Open	Closed	Open	Open	Open
12	t_{PHL}									
13	t_{PLH}	B2	Σ2 (Waveform B)	None	A1, B1, A2, and C0	Open	Closed	Open	Open	Open
14	t_{PHL}									
15	t_{PLH}	A4	Σ4 (Waveform B)	None	A3, B3, and B4	Open	Open	Open	Closed	Open
16	t_{PHL}									
17	t_{PLH}	B4	Σ4 (Waveform B)	None	A3, B3, and A4	Open	Open	Open	Closed	Open
18	t_{PHL}									

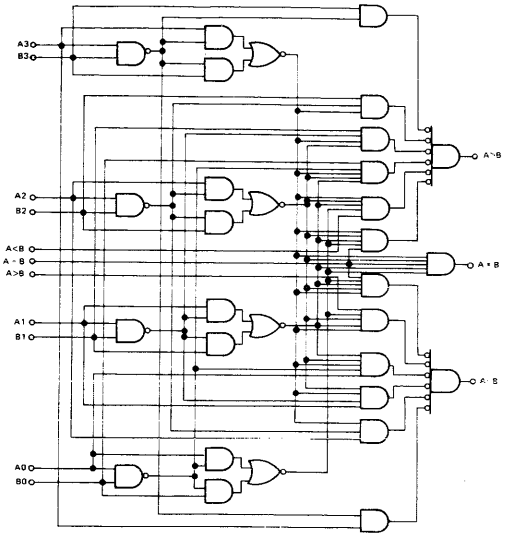
NOTE 7: Inputs and outputs are open unless otherwise specified.

FIGURE 5–SWITCHING TIMES (SHEET 2 OF 2)

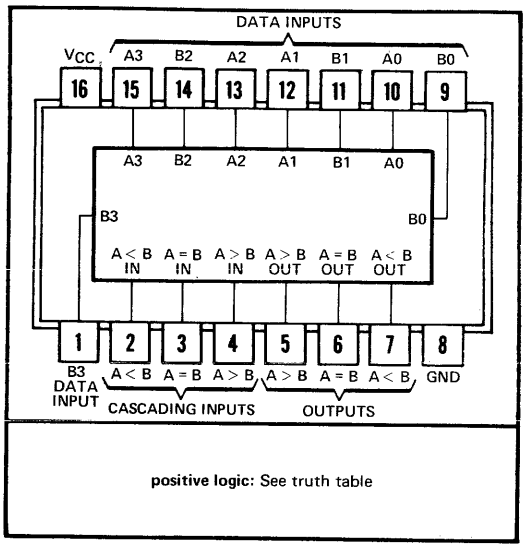
9

CIRCUIT TYPES SN5485, SN7485
4-BIT MAGNITUDE COMPARTORS

functional block diagram



J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

The SN5485 and SN7485 perform magnitude comparison of straight binary and straight BCD (8421) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. When cascaded, the total time for comparison is the function of the word length; however, only a two-gate-level delay (12 ns) is added for each four-bit expansion.

These circuits are completely compatible with most TTL and DTL families. Typical average power dissipation is 275 milliwatts. The SN5485 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN7485 is characterized for operation from 0°C to 70°C.

9

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

NOTE: H = high level, L = low level, X = irrelevant

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5485 Circuits . . . . . −55°C to 125°C
SN7485 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor.

recommended operating conditions

	SN5485			SN7485			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage							0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA		2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA				0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	A < B, A > B inputs	V_{CC} = MAX,	V_I = 2.4 V				40	μA
		all other inputs						120	
I_{IL}	Low-level input current	A < B, A > B inputs	V_{CC} = MAX,	V_I = 0.4 V				−1.6	mA
		all other inputs						−4.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX,	V_O = 0	SN5485	−20		−55	mA
					SN7485	−18		−55	
I_{CC}	Supply current		V_{CC} = MAX,	See Note 3			55	88	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

9

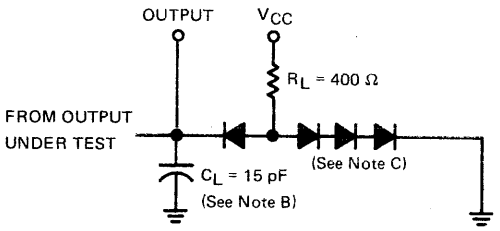
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

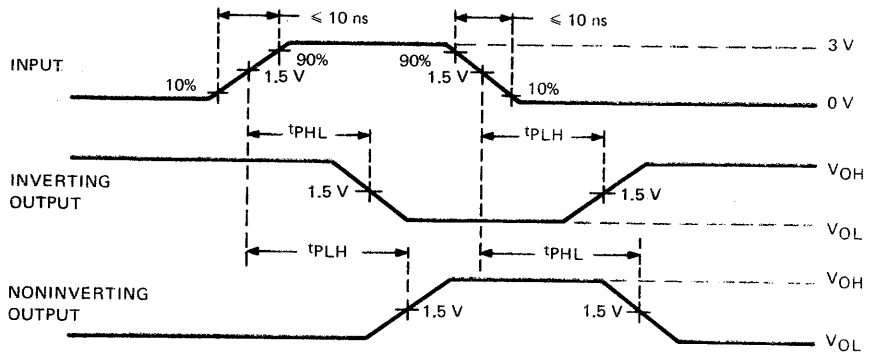
PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A < B, A > B	1	C_L = 15 pF, R_L = 400 Ω, See Figure 1		7		ns
			2			12		
			3			17	26	
		A = B	4			23	35	
t_{PHL}	Any A or B data input	A < B, A > B	1			11		ns
			2			15		
			3			20	30	
		A = B	4			20	30	
t_{PLH}	A < B or A = B	A > B	1			7	11	ns
t_{PHL}	A < B or A = B	A > B	1			11	17	ns
t_{PLH}	A = B	A = B	2			13	20	ns
t_{PHL}	A = B	A = B	2			11	17	ns
t_{PLH}	A > B or A = B	A < B	1			7	11	ns
t_{PHL}	A > B or A = B	A < B	1			11	17	ns

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, Z_{out} ≈ 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 1–PROPAGATION DELAY TIMES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

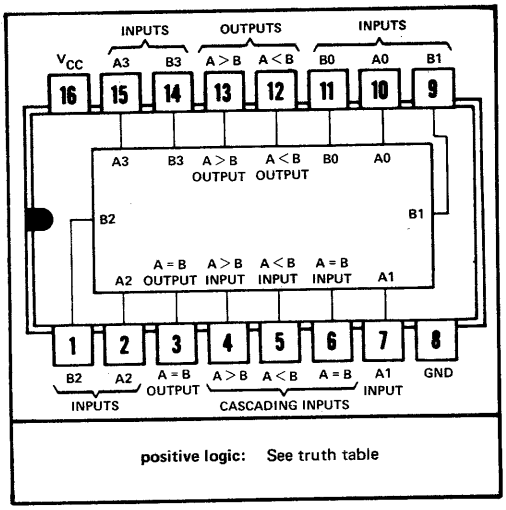
CIRCUIT TYPES SN54L85, SN74L85
4-BIT MAGNITUDE COMPARATORS

description

These 4-bit magnitude comparators compare two 4-bit words and determine their relative magnitude with the result being indicated by a high-level voltage at the A > B, A < B, or A = B output. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more significant bits. The stage handling the least significant bits must have a low-level voltage applied to the A > B and A < B inputs and a high-level voltage applied to the A = B input.

These circuits utilize low-power transistor-transistor-logic (TTL), but are fully compatible with most TTL and DTL families. Power dissipation is typically 20 mW per package. The SN54L85 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L85 is characterized for operation from 0°C to 70°C.

J OR N
DUAL-IN-LINE PACKAGE



positive logic: See truth table

logic

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

NOTE: H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 8 V
Input voltage (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range: SN54L85 Circuits . . . . . −55°C to 125°C
SN74L85 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN54L85			SN74L85			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage	1		2		V
V_{IL}	Low-level input voltage	2			0.7	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, I_{OL} = 2 mA		0.3	V
I_{IH}	High-level input current into any A or B input	3	V_{CC} = MAX, V_I = 2.4 V		30	μA
			V_{CC} = MAX, V_I = 5.5 V		300	
I_{IH}	High-level input current into A > B, A < B, or A = B input	3	V_{CC} = MAX, V_I = 2.4 V		10	μA
			V_{CC} = MAX, V_I = 5.5 V		100	
I_{IL}	Low-level input current into any A or B input	3	V_{CC} = MAX, V_I = 0.3 V		−0.54	mA
I_{IL}	Low-level input current into A > B, A < B, or A = B input	3	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX	−3	−15	mA
I_{CC}	Supply current	5	V_{CC} = MAX, V_I = 4.5 V		7.7	mA
			V_{CC} = MAX, V_I = 0		7.2	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

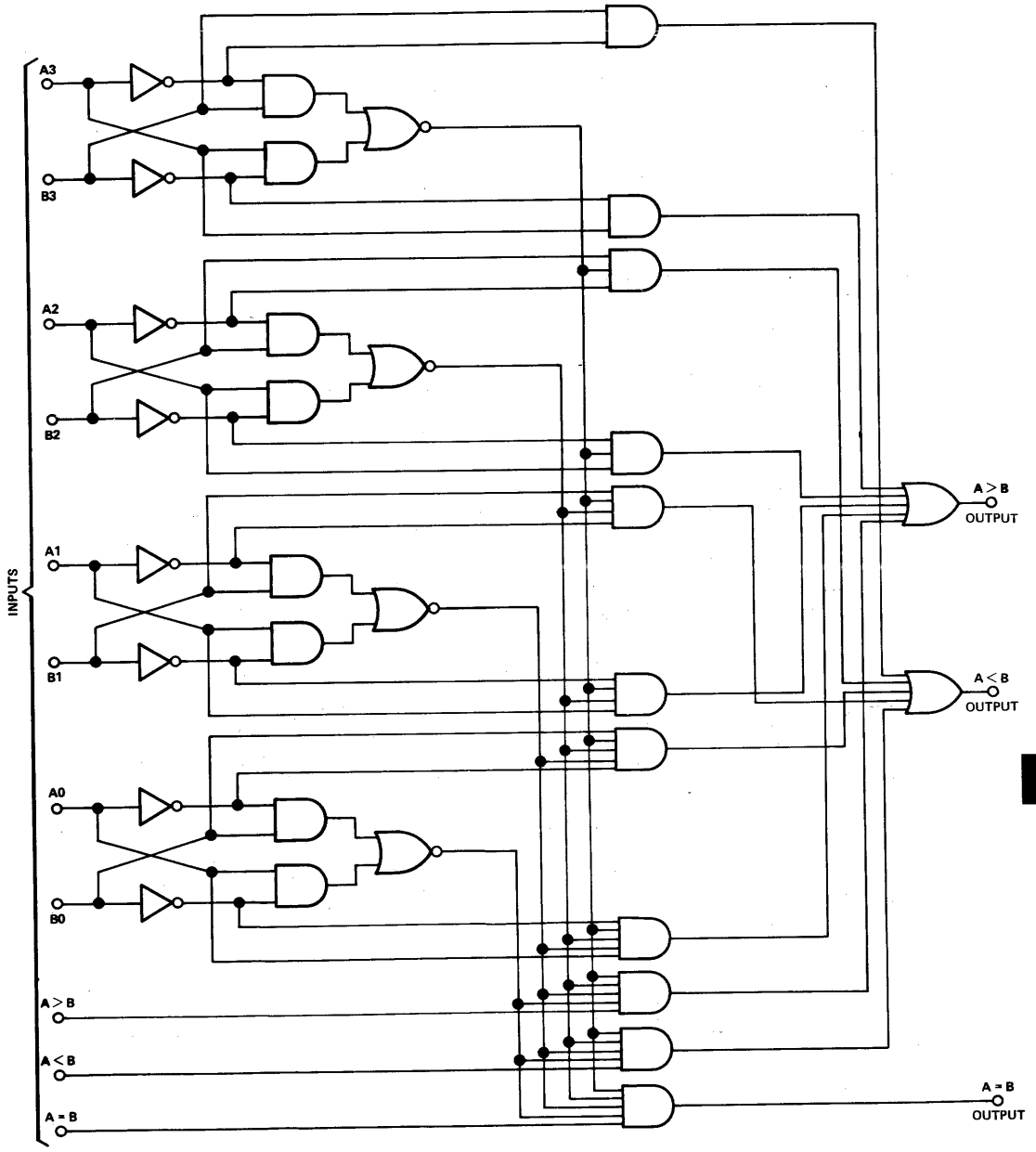
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from any A or B input	6	C_L = 50 pF, R_L = 4 kΩ		90	150	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from any A or B input	6			75	150	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from A > B, A < B, or A = B inputs	7			75	150	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from A > B, A < B, or A = B inputs	7			55	100	ns

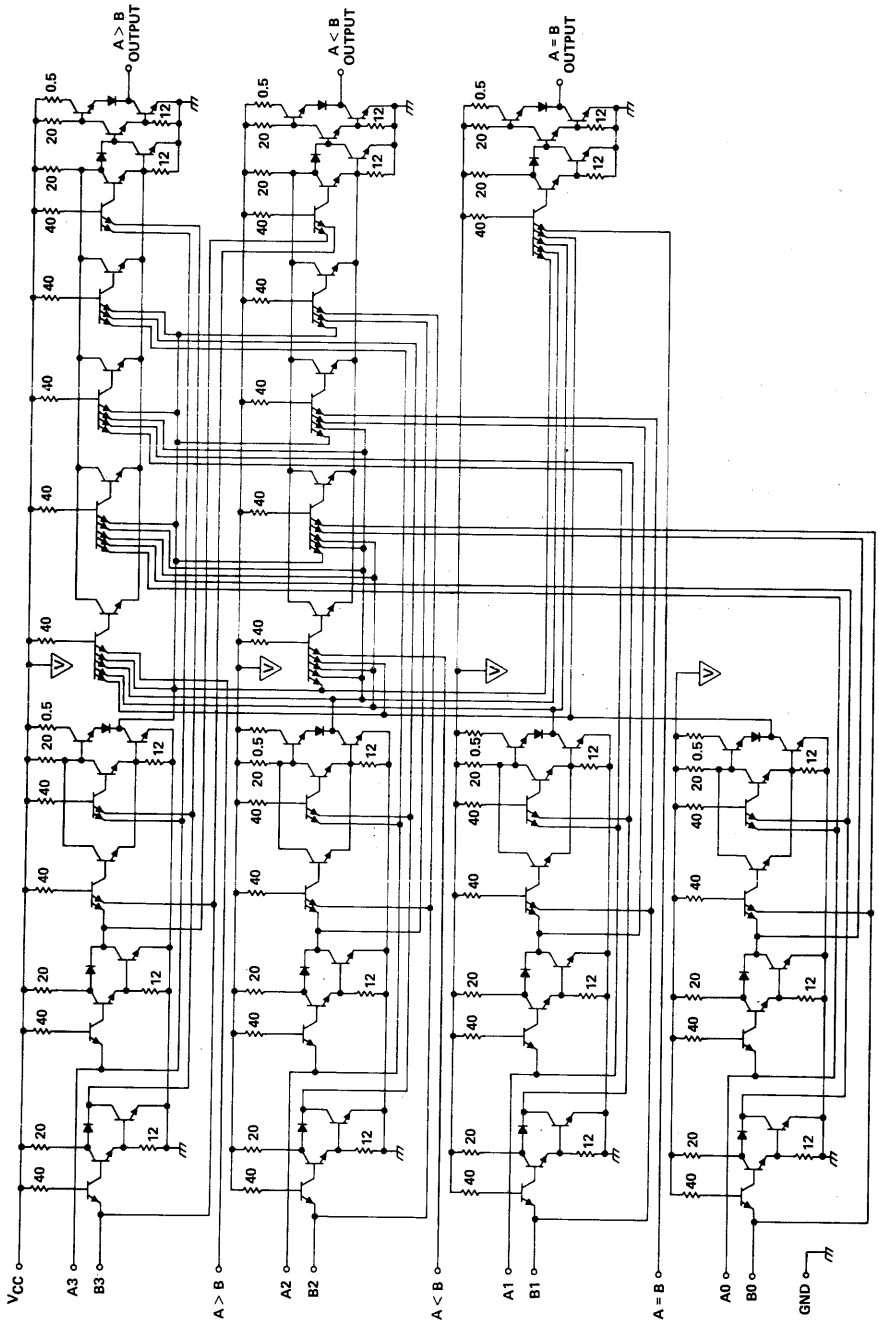
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

schematic



All resistor values shown are nominal and in kilohms.

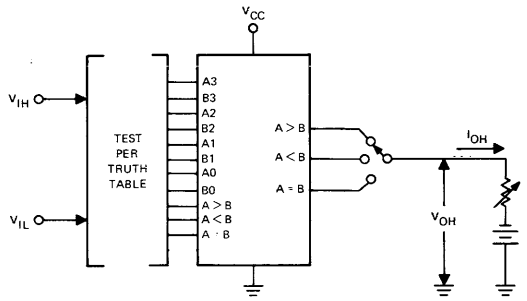
▽ ... V_{CC} bus

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

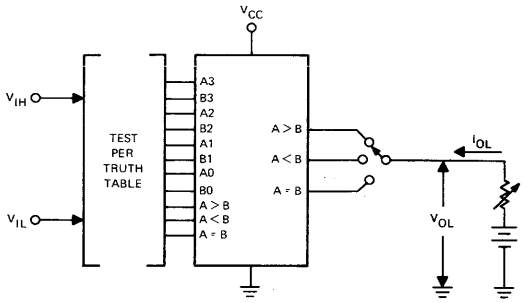
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



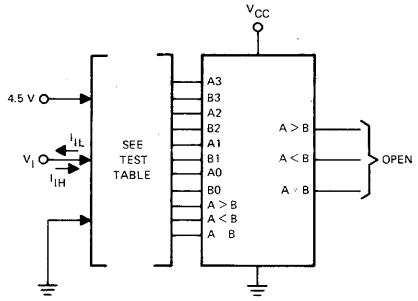
Each input is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



Each input is tested separately.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}



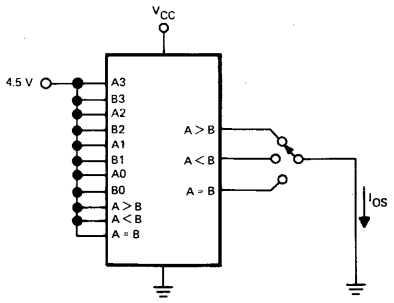
Each input is tested separately.

TEST TABLE

APPLY V_I	TEST I_{IH}		TEST I_{IL}	
	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND
A3, A2, A1, A0	ALL OTHER INPUTS	NONE	NONE	ALL OTHER INPUTS
B3, B2, B1, B0	ALL OTHER INPUTS	NONE	NONE	ALL OTHER INPUTS
A > B	A3, A2, A1, AND A0	B3, B2, B1, AND B0	ALL OTHER INPUTS	NONE
A < B			ALL OTHER INPUTS	NONE
A = B			ALL OTHER INPUTS	NONE

FIGURE 3–I_{IH}, I_{IL}

9



Each output is tested separately.

FIGURE 4–I_{OS}

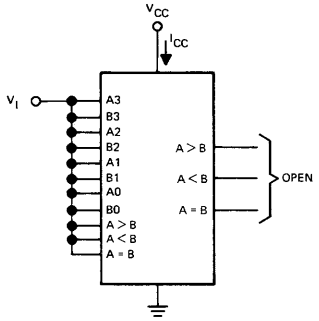
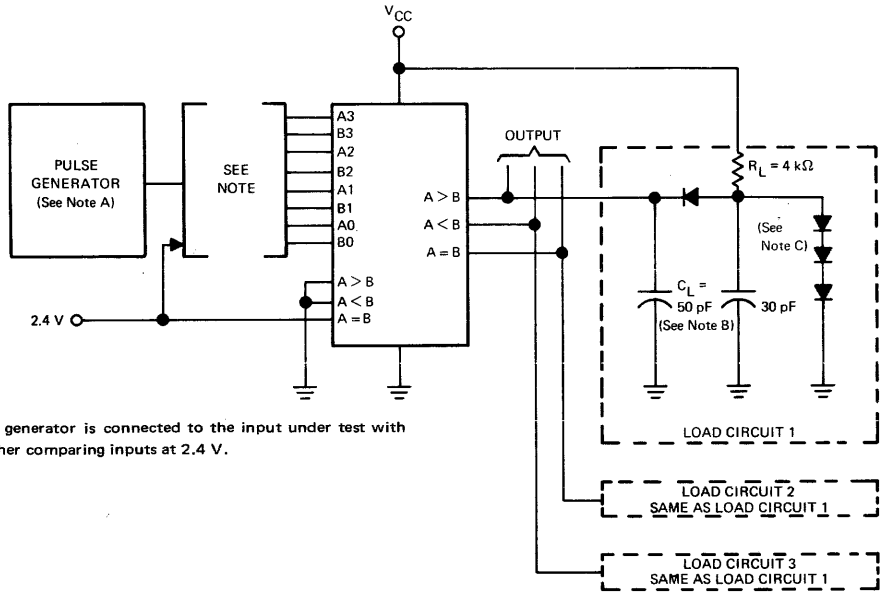


FIGURE 5–I_{CC}

§ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

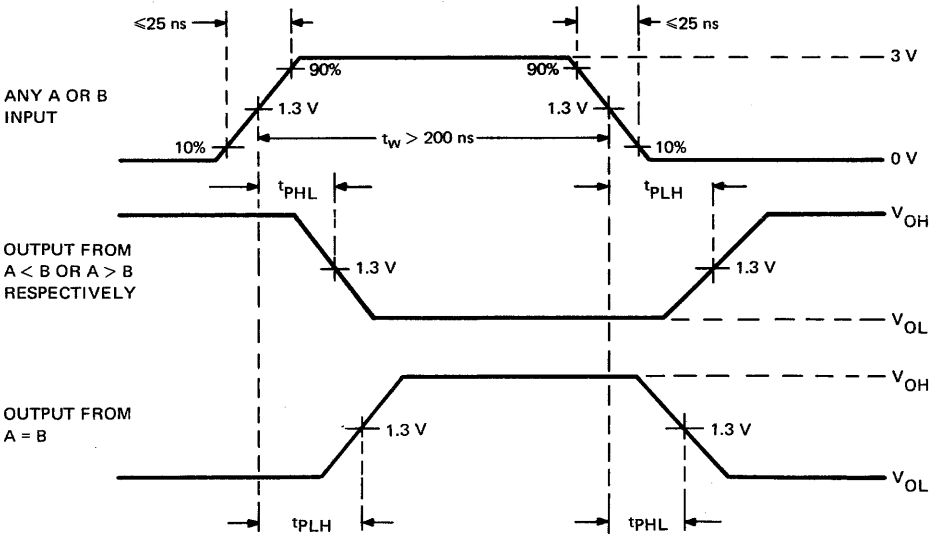
PARAMETER MEASUREMENT INFORMATION

switching characteristics



NOTE: Pulse generator is connected to the input under test with all other comparing inputs at 2.4 V.

TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 500 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916.
D. Each output is tested separately.

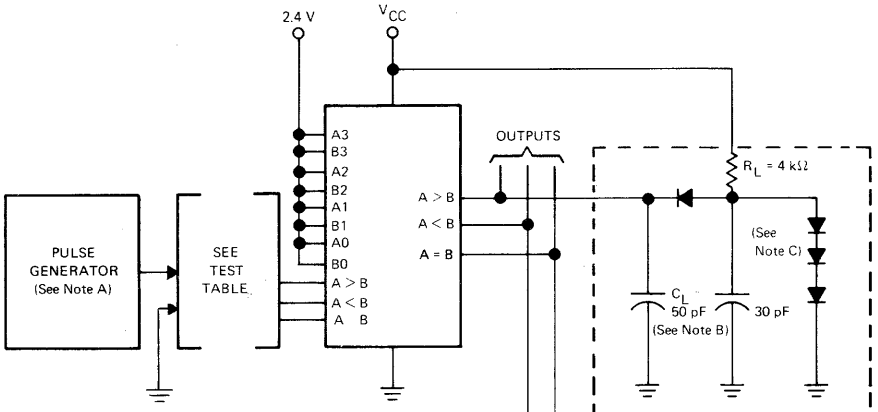
FIGURE 6—PROPAGATION TIMES FROM COMPARING INPUTS

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

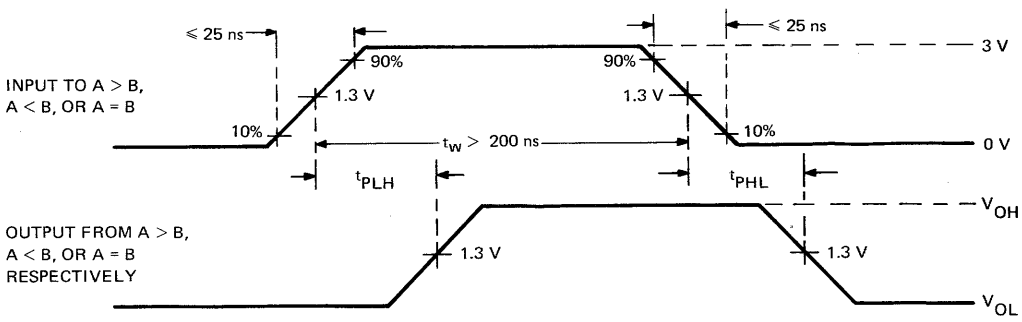
switching characteristics (continued)



TEST TABLE

APPLY PULSE GENERATOR TO	GROUND	TEST
A > B INPUT	UNUSED INPUTS	A > B OUTPUT
A < B INPUT	UNUSED INPUTS	A < B OUTPUT
A = B INPUT	UNUSED INPUTS	A = B OUTPUT

TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 500 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916.
D. Each output is tested separately.

FIGURE 7–PROPAGATION TIMES FROM CASCADING INPUTS

9

CIRCUIT TYPES SN5486, SN7486
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

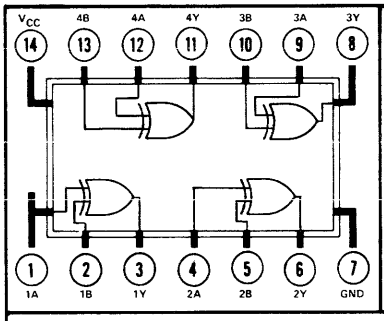
- Input-Clamping Diodes Simplify System Design
- Fully Compatible with TTL, DTL, and Other MSI Circuits
- Typical Propagation Delay Times: 12 ns

logic

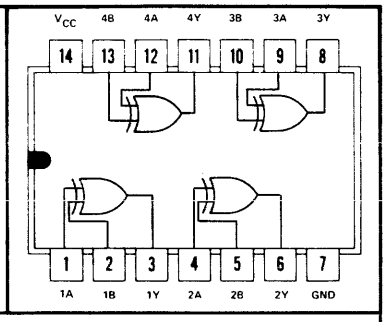
TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = A \oplus B$

description

Each of these monolithic, quadruple 2-input exclusive-OR gates utilize TTL circuitry to perform the function: $Y = A\overline{B} + \overline{A}B$. When the input states are complementary, the output goes to a logical 1.

9

These circuits are fully compatible for use with other TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out of 20 is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Propagation delay is 12 nanoseconds and power dissipation is 37.5 miliwatts typically for each exclusive-OR function.

The SN5486 is characterized for operation over the full military temperature range of −55°C to 125°C and the SN7486 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)		7 V
Input Voltage, V_{in} (See Note 1)		5.5 V
Operating Free-Air Temperature Range:	SN5486 Circuits	−55°C to 125°C
	SN7486 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5486 Circuits	4.5	5	5.5	V
SN7486 Circuits	4.75	5	5.25	V
Normalized Fan-out from each output,N: Logical 0			10	
Logical 1			20	

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS †		MIN	TYP ‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1					0.8	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −800 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
I_{OS}	Short circuit output current §	5	V_{CC} = MAX, $V_{in(1)}$ = 4.5 V, $V_{in(0)}$ = 0	SN5486	−20		−55	mA
				SN7486	−18		−55	mA
I_{CC}	Supply current	6	V_{CC} = MAX, V_{in} = 4.5 V	SN5486		30	43	mA
				SN7486		30	50	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

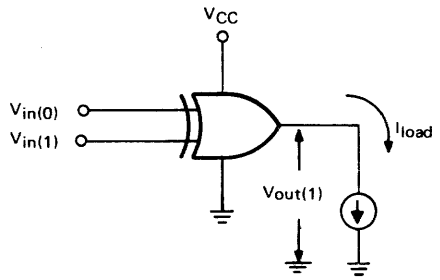
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (other input low)	7	C_L = 15 pF, R_L = 400 Ω		11	17	ns
t_{pd1}	Propagation delay time to logical 1 level (other input low)	7	C_L = 15 pF, R_L = 400 Ω		15	23	ns
t_{pd0}	Propagation delay time to logical 0 level (other input high)	7	C_L = 15 pF, R_L = 400 Ω		13	22	ns
t_{pd1}	Propagation delay time to logical 1 level (other input high)	7	C_L = 15 pF, R_L = 400 Ω		18	30	ns

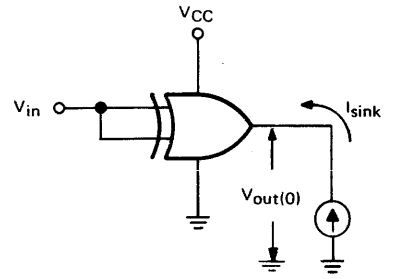
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



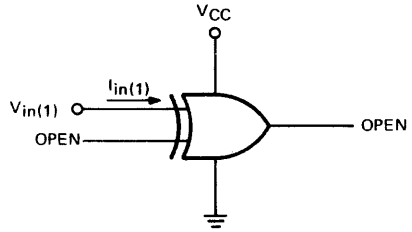
1. Each input is tested separately.

FIGURE 1



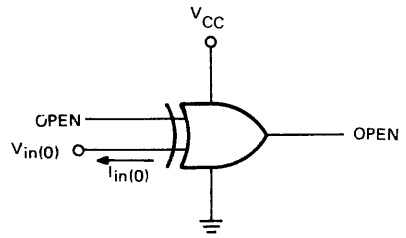
1. Logical 0 and logical 1 input conditions are tested.

FIGURE 2



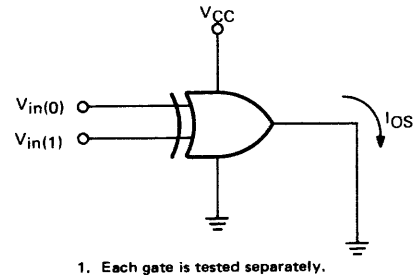
1. Each input is tested separately.

FIGURE 3



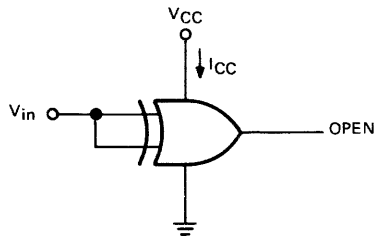
1. Each input is tested separately.

FIGURE 4



1. Each gate is tested separately.

FIGURE 5



1. Logical 0 and logical 1 input conditions are tested.

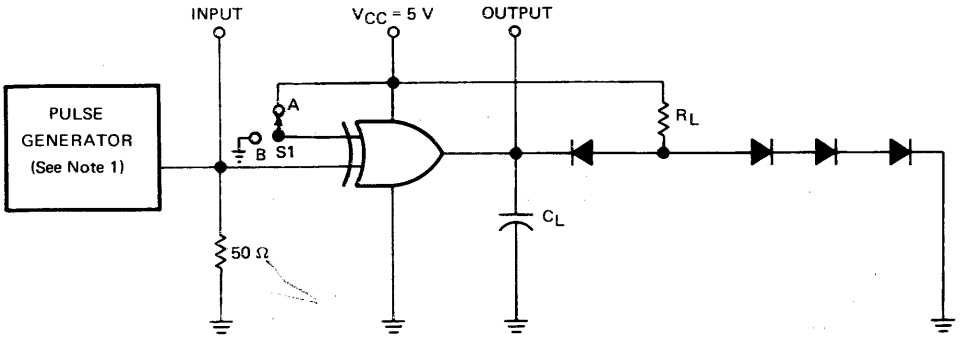
FIGURE 6

† Arrows indicate actual direction of current flow.

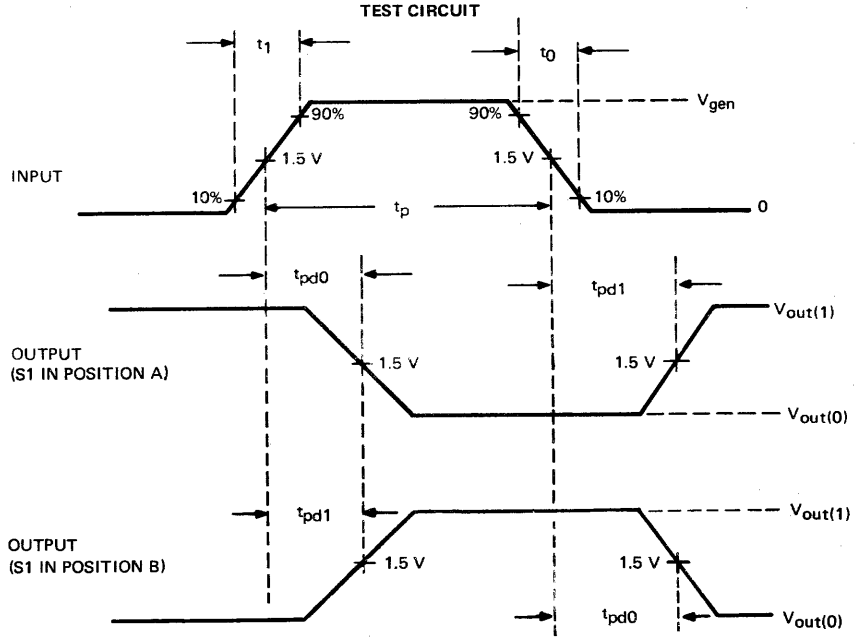
9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leqslant 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064
3. $t_{pd} = \dfrac{t_{pd0} + t_{pd1}}{2}$
4. C_L includes probe and jig capacitance.
5. Each gate tested separately.

FIGURE 7

9

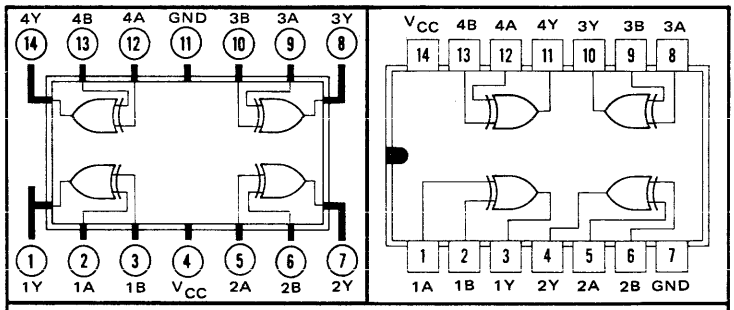
CIRCUIT TYPES SN54L86, SN74L86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

- Fully Compatible with TTL, DTL, and Other MSI Circuits
- Typical Propagation Delay Time: 43 ns

logic

T
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW



positive logic: $Y = A \oplus B$

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

description

Each of these low-power, monolithic, quadruple 2-input exclusive–OR gates utilize TTL circuitry to perform the function: $Y = A\overline{B} + \overline{A}B$. When the input states are complementary the output goes to a logical 1.

These circuits are fully compatible for use with other TTL or DTL circuits. A full fan-out to 10 series 54L/74L loads is available from each of the outputs. Typical power dissipation is 3.75 milliwatts for each exclusive-OR function.

The SN54L86 is characterized for operation over the full military temperature range of –55°C to 125°C and the SN74L86 is characterized for operation from 0°C to 70°C.

9

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 8 V
Input Voltage, V_{in} (See Note 1) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN54L86 Circuits . . . . . –55°C to 125°C
SN74L86 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . –65°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN54L86	4.5	5	5.5	V
SN74L86	4.75	5	5.25	V
Normalized Fan-out from each output, N			10	

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1				0.7	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.7 V, I_{load} = −100 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.7 V, I_{sink} = 2 mA			0.3	V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V			20	μA
			V_{CC} = MAX, V_{in} = 5.5 V			200	μA
$I_{in(0)}$	Logical 0 level input current (each input)	4	V_{CC} = MAX, V_{in} = 0.3 V			−0.36	mA
I_{OS}	Short circuit output current	5	V_{CC} = MAX, $V_{in(1)}$ = 4.5 V, $V_{in(0)}$ = 0	−3		−15	mA
$I_{CC(0)}$	Supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 4.5 V			1.67	mA
$I_{CC(1)}$	Supply current (average per gate)	5	V_{CC} = MAX $V_{in(1)}$ = 4.5 V, $V_{in(0)}$ = 0			1.1	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

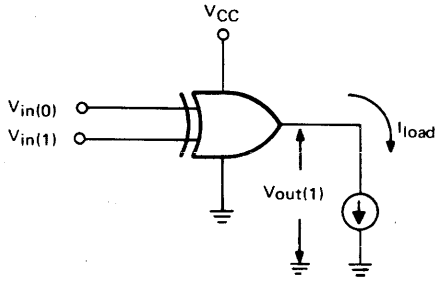
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

9

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (other input low)	7	C_L = 50 pF, R_L = 4 kΩ		60	150	ns
t_{pd1}	Propagation delay time to logical 1 level (other input low)	7	C_L = 50 pF, R_L = 4 kΩ		75	150	ns
t_{pd0}	Propagation delay time to logical 0 level (other input high)	7	C_L = 50 pF, R_L = 4 kΩ		35	60	ns
t_{pd1}	Propagation delay time to logical 1 level (other input high)	7	C_L = 50 pF, R_L = 4 kΩ		50	90	ns

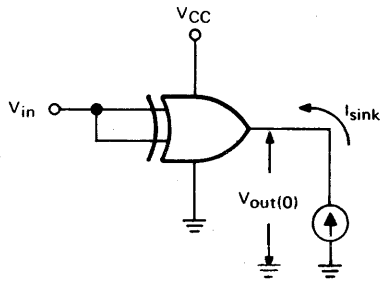
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



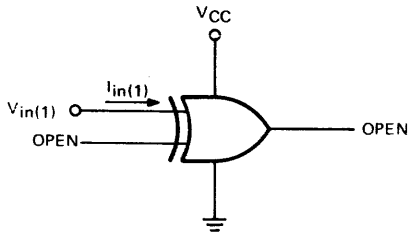
1. Each input is tested separately.

FIGURE 1



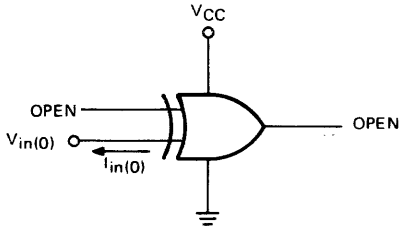
1. Logical 0 and logical 1 input conditions are tested.

FIGURE 2



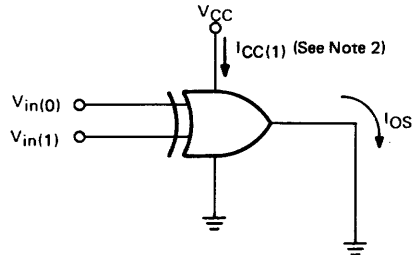
1. Each input is tested separately.

FIGURE 3



1. Each input is tested separately.

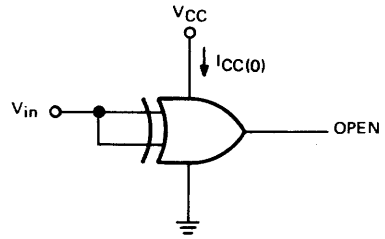
FIGURE 4



NOTES: 1. Each gate is tested separately for I_{OS}.
2. When testing $I_{CC(1)}$, the output is open,

$$\text{the average-per-gate value} = \frac{I_{CC\ \text{total}}}{\text{number of gates in package}}$$

FIGURE 5



NOTES: 1. Logical 0 and logical 1 input conditions are tested.

2. The average-per gate value $= \dfrac{I_{CC\ \text{total}}}{\text{number of gates in package}}$

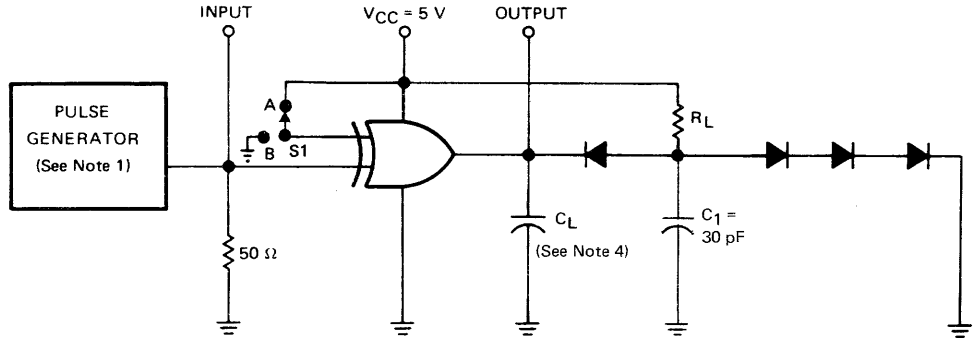
FIGURE 6

†Arrows indicate actual direction of current flow.

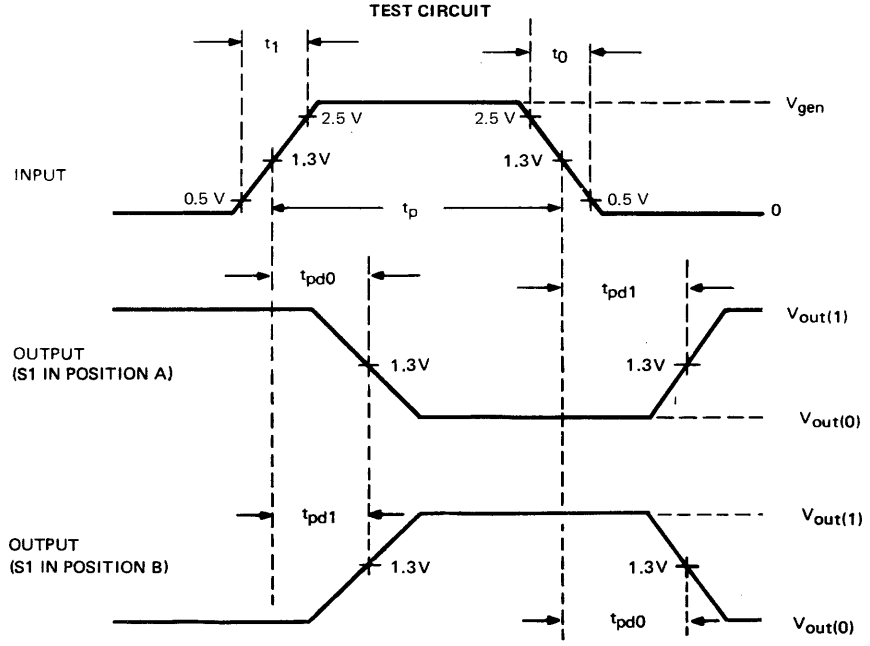
9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 60$ ns, t_p = 1 μs, PRR ≤ 500 kHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N916.
3. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
4. C_L includes probe and jig capacitance.
5. Each gate tested separately.

FIGURE 7

9

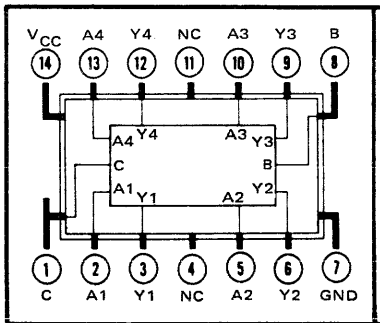
CIRCUIT TYPES SN54H87, SN74H87
4-BIT TRUE/COMPLEMENT, ZERO/ONE ELEMENT

logic

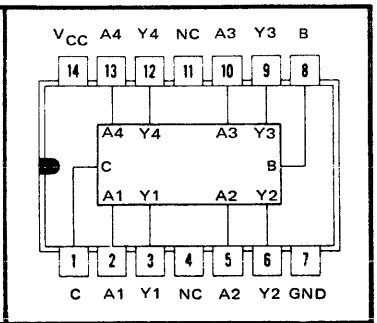
TRUTH TABLE

CONTROL INPUTS		OUTPUTS			
B	C	Y1	Y2	Y3	Y4
0	0	$\overline{A1}$	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$
0	1	A1	A2	A3	A4
1	0	1	1	1	1
1	1	0	0	0	0

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See truth table

description

These monolithic 4-bit true/complement elements, with the use of the two control lines (B, C), will transfer a 4-bit binary input (A) to the output (Y) in either true or complementary form. Furthermore, the control lines will also set all outputs to either a logical 0 or logical 1 independent of the state of the data inputs.

These circuits are fully compatible for use with other TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify system design. Each input represents only one normalized series 54H/74H load, and full fan-out to 10 series 54H/74H loads is available from each of the outputs in the logical 0 condition. In the logical 1 state, a fan-out of 20 is available to facilitate tying unused inputs to used inputs.

9

Power dissipation is 270 mW typically with an average propagation delay of 14 ns from data inputs to output.

The SN54H87 is characterized for operation over the full military temperature range of −55°C to 125°C, and the SN74H87 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)		7 V
Input Voltage, V_{in} (See Note 1)		5.5 V
Operating Free-Air Temperature Range:	SN54H87 Circuits	−55°C to 125°C
	SN74H87 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

Note 1: These voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	SN54H87 Circuits	4.5	5	5.5	V
	SN74H87 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Each Output (N):	Logical 0			10	
	Logical 1			20	

NOTE 1: These voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1				0.8	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −1 mA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 20 mA			0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	2	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
I_{OS}	Short circuit output current§	4	V_{CC} = MAX, V_{out} = 0	−40		−100	mA
I_{CC}	Supply current (SN54H87)	5	V_{CC} = MAX		54	78	mA
I_{CC}	Supply current (SN74H87)	5	V_{CC} = MAX		54	89	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level from data inputs to outputs	6	C_L = 25 pF, R_L = 280 Ω		13	19	ns
t_{pd1}	Propagation delay time to logical 1 level from data inputs to outputs	6	C_L = 25 pF, R_L = 280 Ω		14	20	ns
t_{pd0}	Propagation delay time to logical 0 level from control inputs to outputs	6	C_L = 25 pF, R_L = 280 Ω		17	25	ns
t_{pd1}	Propagation delay time to logical 1 level from control inputs to outputs	6	C_L = 25 pF, R_L = 280 Ω		17	25	ns

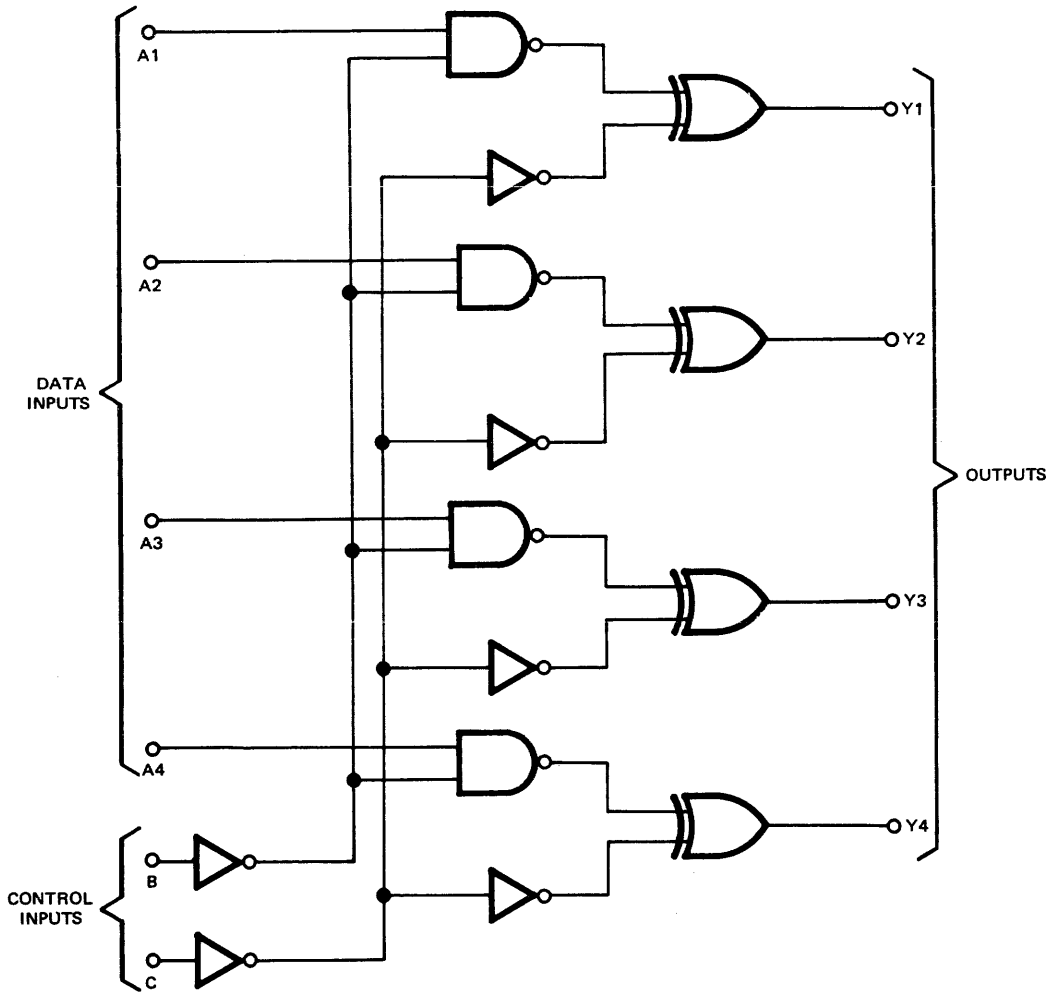
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C

§ Not more than one output should be shorted at a time.

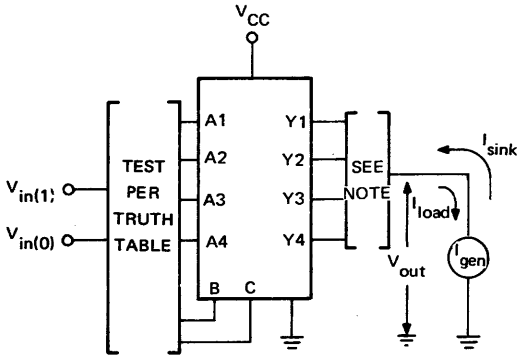
9

functional block diagram



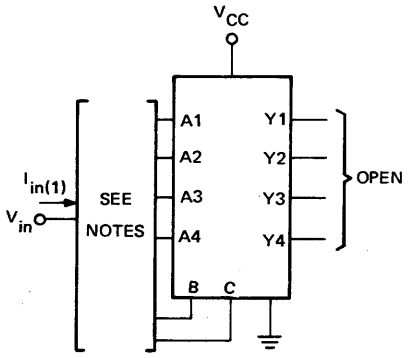
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



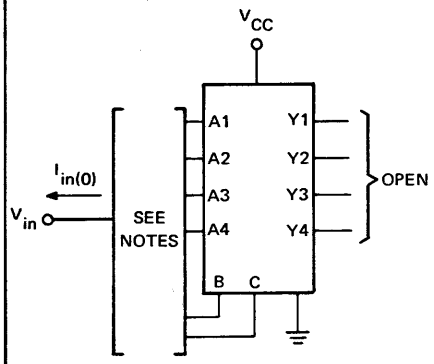
1. Each output is tested separately.

FIGURE 1



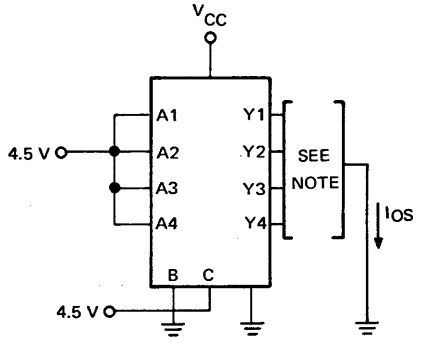
1. Each input is tested separately.
2. When testing A1, A2, A3, or A4 input B is at 4.5 V.

FIGURE 2



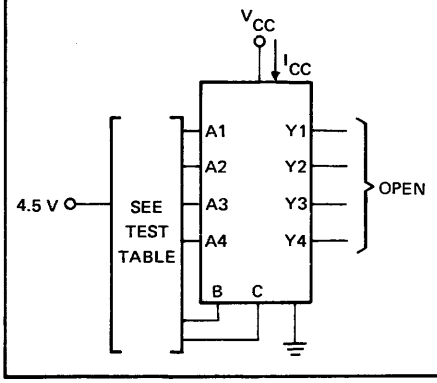
1. Each input is tested separately
2. When testing A1, A2, A3, or A4 input B is grounded.

FIGURE 3



1. Each output is tested separately.

FIGURE 4



TEST TABLE

TEST NO.	APPLY 4.5 V	GROUND
1	A1, A2, A3, A4	B, C
2	B, C	A1, A2, A3, A4

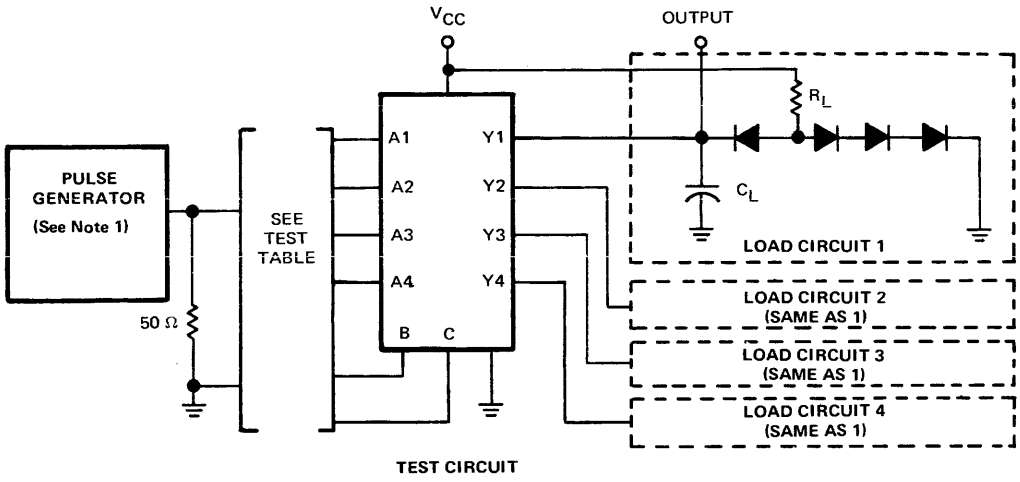
FIGURE 5

† Arrows indicate actual direction of current flow.

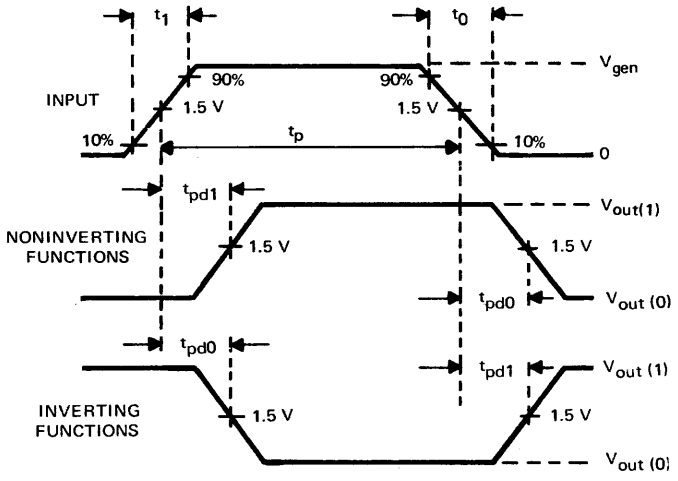
9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

TEST TABLE (See Note 2)

GND	INPUT	OUTPUT
B, C	A1	Y1
B, C	A2	Y2
B, C	A3	Y3
B, C	A4	Y4
C	B	Y1
C	B	Y2
C	B	Y3
C	B	Y4
B	C	Y1
B	C	Y2
B	C	Y3
B	C	Y4

NOTES: 1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_1 = t_0$ = 7 ns, t_p = 500 ns, PRR = 1 MHz, and $Z_{out} \approx 50\Omega$.
2. Inputs not specified are open.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N3064.

FIGURE 6 – SWITCHING TIMES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54180, SN74180
8-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

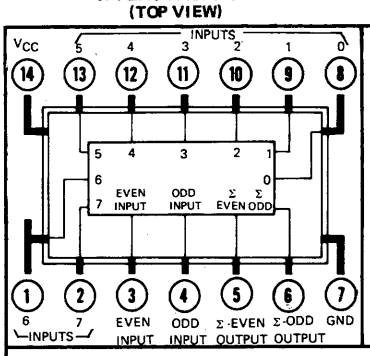
logic

TRUTH TABLE

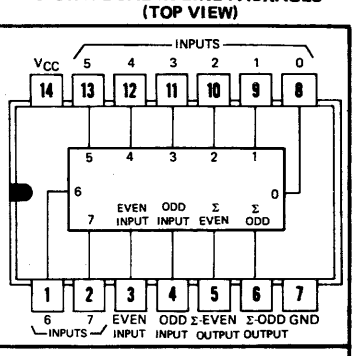
INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X= irrelevant

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGES
(TOP VIEW)



positive logic: see truth table

description

These universal, monolithic, 8-bit parity generators/checkers, utilizing familiar Series 54/74 TTL circuitry, feature odd/even outputs and control inputs to facilitate operation in either odd- or even-parity applications. The word-length capability is easily expanded by cascading. Typical applications are shown for these parity circuits being used to generate and check parity.

The SN54180/74180 are fully compatible with other TTL or DTL circuits. Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized loads is provided in the logical 1 state to facilitate the connection of unused inputs to used inputs. Typical power dissipation is 170 mW.

The SN54180 is characterized for operation over the full military temperature range of −55°C to 125°C; and the SN74180 is characterized for operation from 0°C to 70°C.

9

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)		7 V
Input Voltage, V_{in} (See Note 1)		5.5 V
Operating Free-Air Temperature Range:	SN54180 Circuits	−55°C to 125°C
	SN74180 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	SN54180	4.5	5	5.5	V
	SN74180	4.75	5	5.25	V
Normalized Fan-Out from Each Output (N):	Logical 0			10	V
	Logical 1			20	V

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1					0.8	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −800 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at each data input	2	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at each data input	2	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current at even or odd input	2	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at even or odd input	2	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
I_{OS}	Short circuit output current§	3	V_{CC} = MAX	SN54180	−20		−55	mA
				SN74180	−18		−55	mA
I_{CC}	Supply current	3 and 4	V_{CC} = MAX	SN54180		34	49	mA
				SN74180		34	56	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

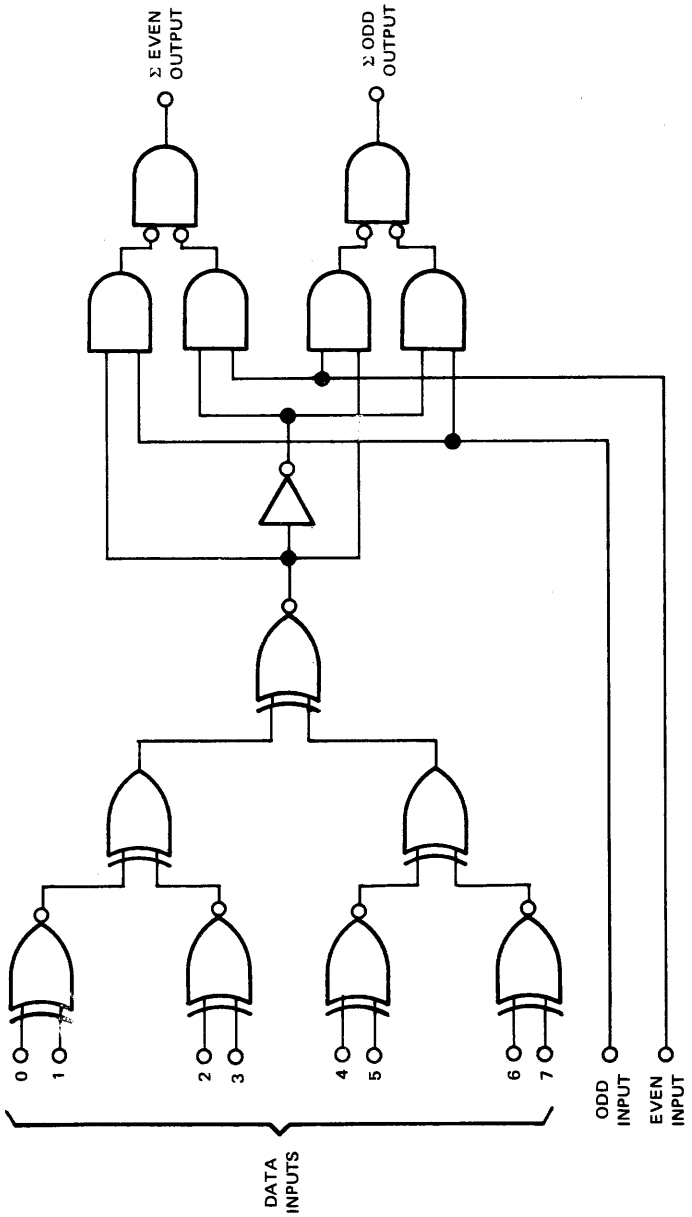
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	FROM INPUT	TO OUTPUT	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Data	Σ Even	5	C_L = 15 pF, R_L = 400 Ω, Odd input grounded		40	60	ns
t_{pd0}						45	68	
t_{pd1}	Data	Σ Odd				32	48	ns
t_{pd0}						25	38	
t_{pd1}	Data	Σ Even	5	C_L = 15 pF, R_L = 400 Ω, Even input grounded		32	48	ns
t_{pd0}						25	38	
t_{pd1}	Data	Σ Odd				40	60	ns
t_{pd0}						45	68	
t_{pd1}	Even or Odd	Σ Even or Σ Odd	5	C_L = 15 pF, R_L = 400 Ω		13	20	ns
t_{pd0}	Even or Odd	Σ Even or Σ Odd				7	10	ns

9

functional block diagram



PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

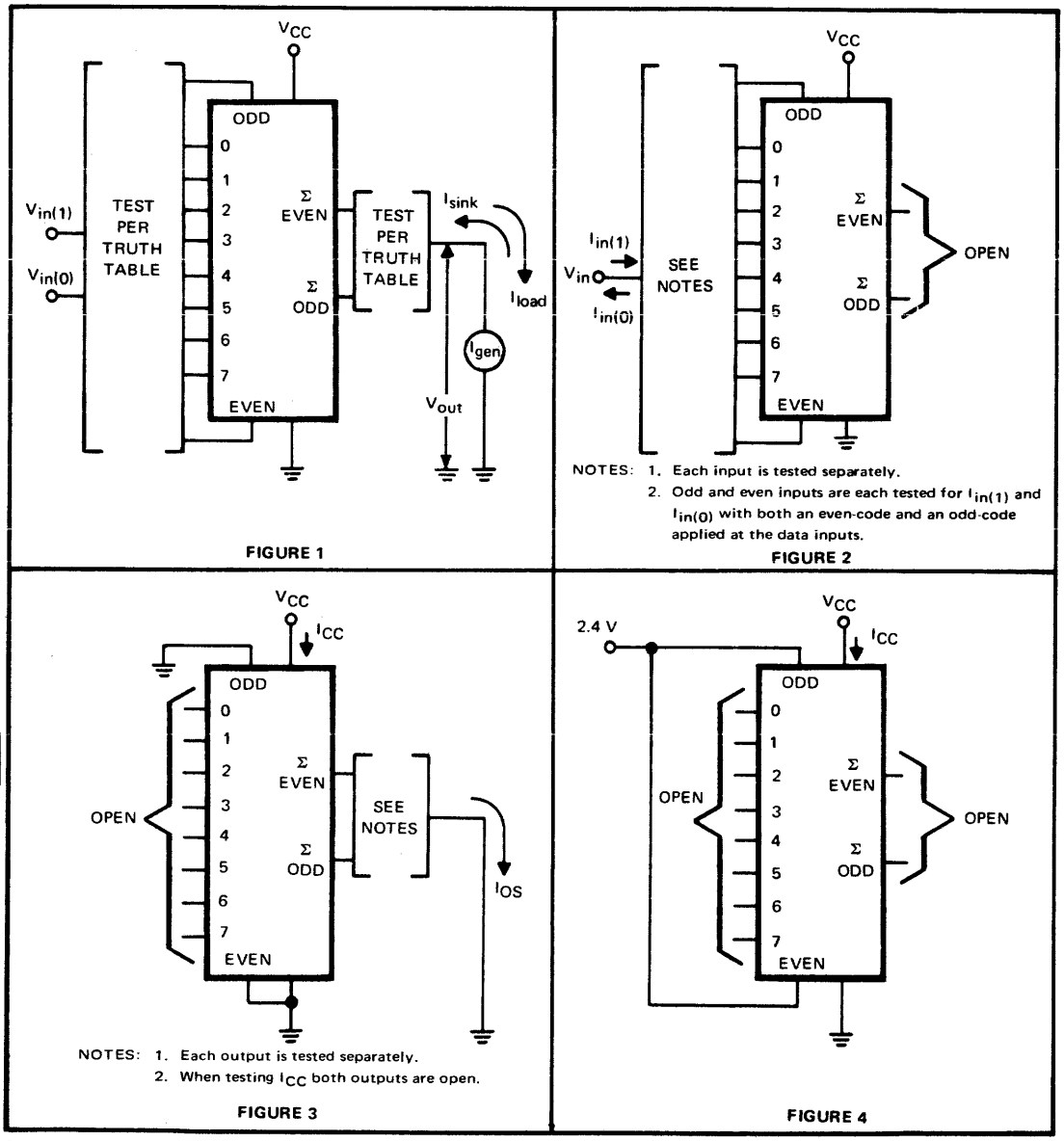


FIGURE 1

NOTES: 1. Each input is tested separately.
2. Odd and even inputs are each tested for $I_{in(1)}$ and $I_{in(0)}$ with both an even-code and an odd-code applied at the data inputs.

FIGURE 2

NOTES: 1. Each output is tested separately.
2. When testing I_{CC} both outputs are open.

FIGURE 3

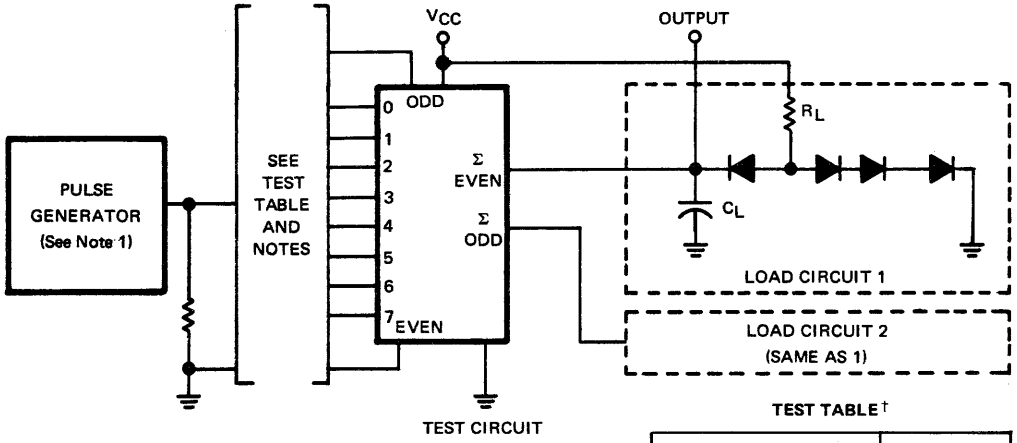
FIGURE 4

†Arrows indicate actual direction of current flow.

9

PARAMETER MEASUREMENT INFORMATION

switching characteristics

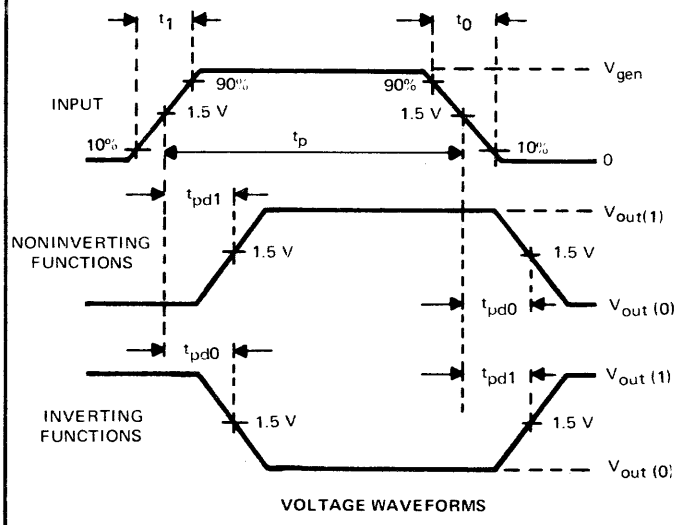


TEST CIRCUIT

TEST TABLE†

INPUT CONDITIONS		OUTPUT
APPLY PULSE	GND	TESTED
0	ODD	Σ EVEN
1	ODD	Σ EVEN
2	ODD	Σ EVEN
3	ODD	Σ EVEN
4	ODD	Σ EVEN
5	ODD	Σ EVEN
6	ODD	Σ EVEN
7	ODD	Σ EVEN
0	ODD	Σ ODD
1	ODD	Σ ODD
2	ODD	Σ ODD
3	ODD	Σ ODD
4	ODD	Σ ODD
5	ODD	Σ ODD
6	ODD	Σ ODD
7	ODD	Σ ODD
EVEN	0	Σ EVEN
ODD	NONE	Σ EVEN
EVEN	NONE	Σ ODD
ODD	0	Σ ODD

† Repeat all but the last 4 tests with the even input grounded.



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_1 = t_0$ = 10 ns, t_p = 500 ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. Inputs not specified are open.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N3064.

FIGURE 5 – SWITCHING TIMES

9

TYPICAL APPLICATIONS

verifying transmitted data

In this example (Figure A), data is being transmitted from data register A to data register B. Parity generators A1 and A2 are connected to generate an even-parity bit Q_{16} which is transmitted to register B. Parity checkers B1 and B2 verify the accuracy of the transmitted data and generate an even true (logical 1) or false (logical 0) parity output signal.

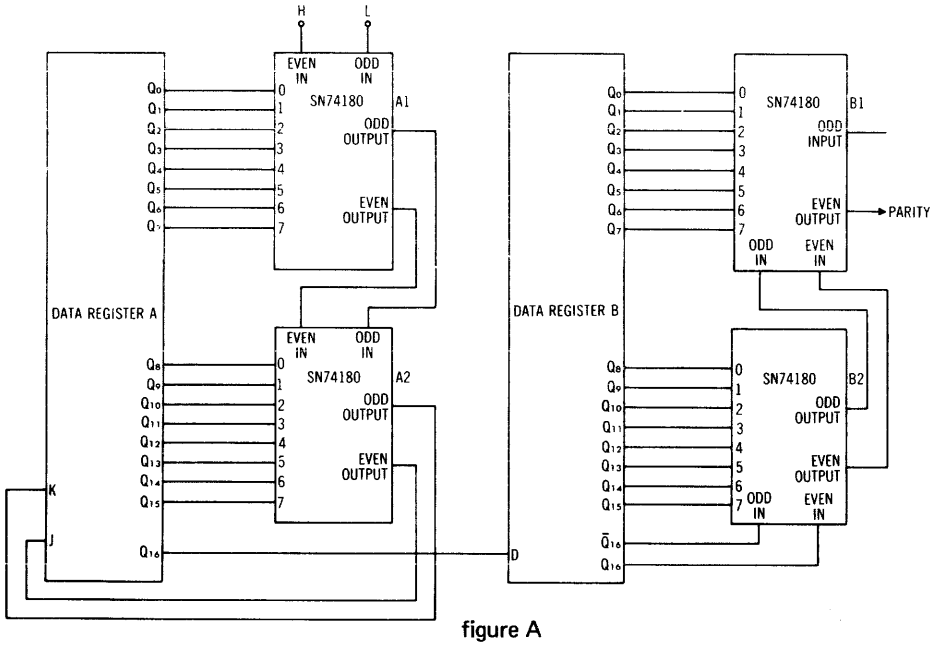


figure A

cascading for longer word lengths

The parity generator/checker may be cascaded for applications requiring longer word lengths. See Figure B. The ODD IN control is grounded for even parity generation and the EVEN IN control is grounded for odd parity generation. Two control inputs and two outputs ensure faster operation when cascading for word lengths over 8 bits, as only one gate delay is added for each additional 8-bit group. For a 32-bit word, parity can be generated in approximately 65 ns.

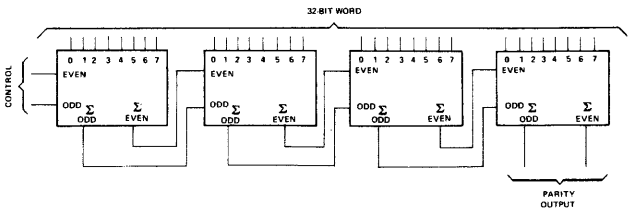


figure B

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

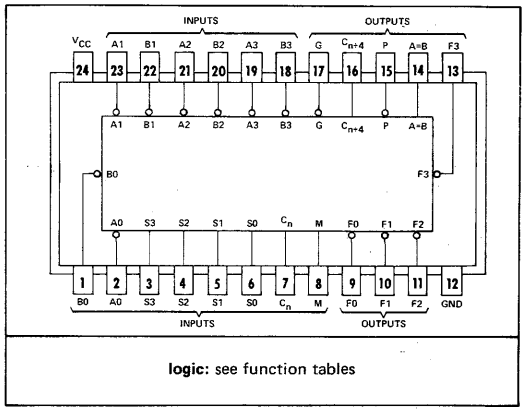
CIRCUIT TYPES SN54181, SN74181
ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS

CIRCUIT TYPES SN54181, SN74181
BULLETIN NO. DL-S 7111314, FEBRUARY 1970
REVISED JANUARY 1971

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	19, 21, 23, 2	WORD A INPUTS
B3, B2, B1, B0	18, 20, 22, 1	WORD B INPUTS
S3, S2, S1, S0	3, 4, 5, 6	FUNCTION-SELECT INPUTS
C_n	7	INV. CARRY INPUT
M	8	MODE CONTROL INPUT
F3, F2, F1, F0	13, 11, 10, 9	FUNCTION OUTPUTS
A = B	14	COMPARATOR OUTPUT
P	15	CARRY PROPAGATE OUTPUT
C_{n+4}	16	INV. CARRY OUTPUT
G	17	CARRY GENERATE OUTPUT
V_{CC}	24	SUPPLY VOLTAGE
GND	12	GROUND

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



logic: see function tables

†Pin assignments for these circuits are the same for all packages.

- Full Look-Ahead for High-Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission-Line Effects
- Darlington Outputs Reduce Turn-Off Time
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus Ten Other Logical Operations
- Typical Add Time for Four Bits . . . . 24 ns
- Typical Carry Time for Four Bits . . . . 12 ns

9

description

The SN54181 and SN74181 are high-speed arithmetic logic units (ALU)/function generators which have a complexity of 75 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in the function table. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in the SN54/SN74181 for fast, simultaneous carry generation by means of two cascade-outputs (pin 15 and 17) for the four bits in the package. When used in conjunction with the SN54182 or SN74182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. For example, the typical addition time for the SN54181/SN74181 is 24 nanoseconds for four bits. When expanding to 16-bit addition with the SN54182/SN74182, only 13 nanoseconds further delay is added so that the total addition time is 37 nanoseconds, or 2.2 nanoseconds per bit. One SN54182/SN74182 is needed for every 16 bit (four SN54181/SN74181 circuits).

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be

description (continued)

performed without external circuitry. The typical delay for the ripple carry is 12 nanoseconds for four bits. With a typical addition time of 24 nanoseconds for four bits, addition of two 8-bit words is accomplished typically in 36 nanoseconds when employing the ripple carry.

The SN54181 and SN74181 will accommodate active-high or active-low data if the pin-designations are reinterpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-high data (Figure I)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C_n}$	$\overline{C_{n+4}}$	X	Y
Active-low data (Figure II)	$\overline{A_0}$	$\overline{B_0}$	$\overline{A_1}$	$\overline{B_1}$	$\overline{A_2}$	$\overline{B_2}$	$\overline{A_3}$	$\overline{B_3}$	$\overline{F_0}$	$\overline{F_1}$	$\overline{F_2}$	$\overline{F_3}$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A–B–1 which requires an end-around or forced carry to provide A–B.

The SN54181 or SN74181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high-level state to indicate equality (A = B). The SN54181/SN74181 should be in the subtract mode when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the control lines at LHHL.

	Input C_n	Output C_{n+4}	Indicates
Active-High Data (Figure I)	H	H	A ≤ B
	L	H	A < B
	H	L	A > B
	L	L	A ≥ B
Active-Low Data (Figure II)	L	L	A ≤ B
	H	L	A < B
	L	H	A > B
	H	H	A ≥ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in the function table and include exclusive-OR, NAND, AND, NOR, and OR functions.

The SN54181/SN74181 is designed with a Darlington output configuration (54H/74H type) to reduce the high-logic-level output impedance and thereby improve the turn-off propagation delay time. All outputs are rated at a normalized fan-out of ten at the low logic level and increased to a fan-out of 20 at the high logic level. The increased high-logic-level fan-out allows the system designer more freedom in tying unused inputs to driven inputs.

The SN54181 is characterized for operation over the full military temperature range of –55°C to 125°C; the SN74181 is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

description (continued)

ALU Signal Designations

The SN54181 and SN74181 can be used with either the signal designations as shown in Figures I or II.

The logic functions and arithmetic operations obtained with signal designations as in Figure I are given in Table I; those obtained with the signal designations of Figure II are given in Table II.

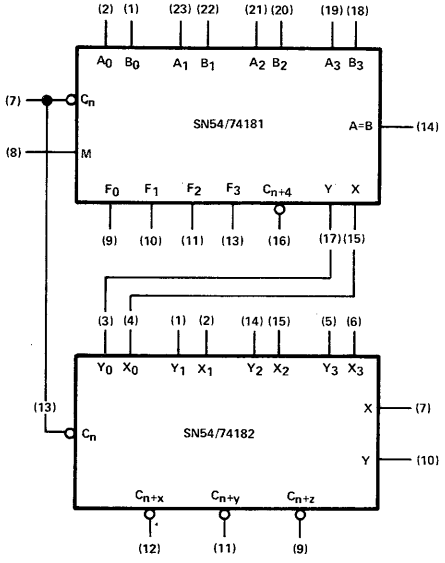


FIGURE I
(FOR TABLE I)

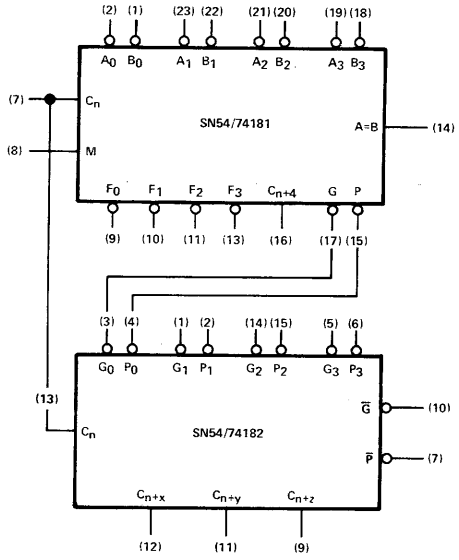


FIGURE II
(FOR TABLE II)

TABLE I

SELECTION S3 S2 S1 S0	ACTIVE-HIGH DATA: M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS: Cn = 0, $\overline{C_n}$ = 1 = H	M = L; ARITHMETIC OPERATIONS: Cn = 1, $\overline{C_n}$ = 0 = L
L L L L	F = $\overline{A}$	F = A	F = A PLUS 1
L L L H	F = $\overline{A+B}$	F = A + B	F = (A + B) PLUS 1
L L H L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L H L H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L H H L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H L L L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H L L H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H L H H	F = AB	F = AB MINUS 1	F = AB
H H L L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H H H L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H H H H	F = A	F = A MINUS 1	F = A

* Each bit is shifted to the next more significant position.

TABLE II

SELECTION S3 S2 S1 S0	ACTIVE-LOW DATA: M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS: Cn = 0, Cn = 0 = L	M = L; ARITHMETIC OPERATIONS: Cn = 1, Cn = 1 = H
L L L L	F = $\overline{A}$	F = A MINUS 1	F = A
L L L H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L L H L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L L H H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L H L L	F = $\overline{A+B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L H L H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L H H L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H L L L	F = $\overline{AB}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H L L H	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H L H H	F = A + B	F = A + B	F = (A + B) PLUS 1
H H L L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H H H L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H H H H	F = A	F = A	F = A PLUS 1

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54181 Circuits . . . . . −55°C to 125°C
SN74181 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each A input in conjunction with inputs S2 or S3, and to each B input in conjunction with inputs S0 or S3.

recommended operating conditions

		SN54181			SN74181			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_{OH}	High-level output voltage, any output except A = B	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4			V
I_{OH}	High-level output current, A = B output only	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V				250	μA
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_{IH}	High-level input current (mode input)	3	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IH}	High-level input current (any A or B input)						120	μA
I_{IH}	High-level input current (any S input)						160	μA
I_{IH}	High-level input current (carry input)						200	μA
I_{IH}	High-level input current (any input)	3	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (mode input)	3	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{IL}	Low-level input current (any A or B input)						−4.8	mA
I_{IL}	Low-level input current (any S input)						−6.4	mA
I_{IL}	Low-level input current (carry input)						−8	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX	SN54181	−20		−55	mA
				SN74181	−18		−57	
I_{CC}	Supply current	5	V_{CC} = MAX	SN54181		88	127	mA
				SN74181		88	140	
I_{CC}	Supply current	6	V_{CC} = MAX	SN54181		94	135	mA
				SN74181		94	150	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

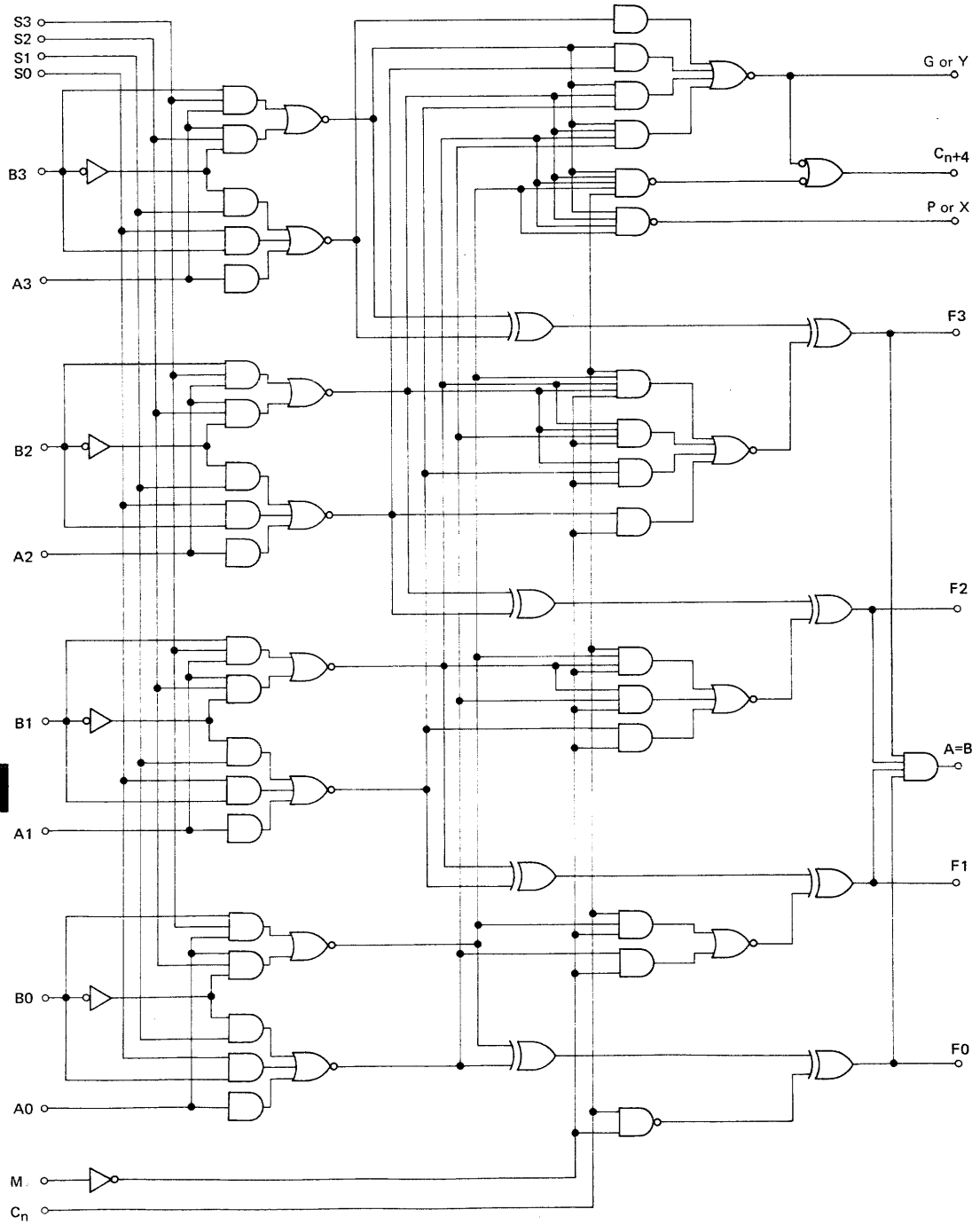
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10 (C_L = 15 pF, R_L = 400 Ω)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}	7			12	18	ns
t_{PHL}						13	19	
t_{PLH}	C_n	Any F		M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode)		13	19	ns
t_{PHL}						12	18	
t_{PLH}	Any A or B	G		M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		13	19	ns
t_{PHL}						13	19	
t_{PLH}	Any A or B	G		M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		17	25	ns
t_{PHL}						17	25	
t_{PLH}	Any A or B	P		M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		13	19	ns
t_{PHL}						17	25	
t_{PLH}	Any A or B	P		M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		17	25	ns
t_{PHL}						17	25	
t_{PLH}	Any A or B	Any F		M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		28	42	ns
t_{PHL}						21	32	
t_{PLH}	Any A or B	Any F		M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		32	48	ns
t_{PHL}						23	34	
t_{PLH}	Any A or B	Any F		M = 4.5 V (logic mode)		32	48	ns
t_{PHL}						23	34	
t_{PLH}	Any A or B	A = B		M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		35	50	ns
t_{PHL}						32	48	

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

9

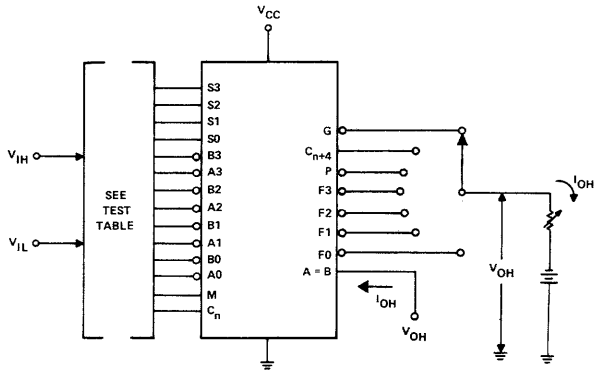
functional block diagram



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

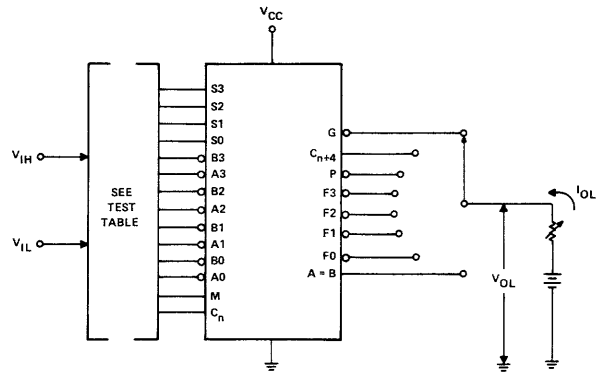


TEST TABLE

OUTPUT UNDER TEST	APPLY V_{IH}	APPLY V_{IL}
G	S3, B3, A3	S2, S1, S0, B2, A2, B1, A1, B0, A0
C_{n+4}	S3, S2, B3, B2, A2, B1, A1, B0, A0	S1, S0, A3, C_n
P	S3, S2, B3, A3, B2, A2, B1, A1, B0, A0	NONE
any F or A = B	S3, S2, S1, S0, A3, A2, A1, A0, M	NONE

Inputs not otherwise specified are connected to ground.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



TEST TABLE

OUTPUT UNDER TEST	APPLY V_{IH}	APPLY V_{IL}
G	S3, S2, S0, B2, A2, B1, A1, B0, A0	S1, B3, A3
C_{n+4}	S3, A3, A2, A1, B0, A0	S2, S1, S0, B3, B2, B1
P	S2, B3, A3, B2, A2, B1, A1, B0, A0	S3
any F	S3, S2, S1, S0, M, C_n	A3, A2, A1, A0
A = B	S3, S2, S1, S0, A3, A2, A1, M, C_n	A0

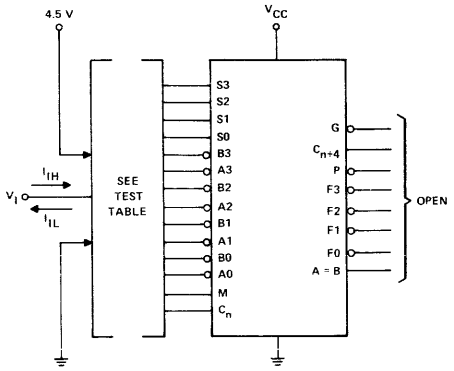
Inputs not otherwise specified are connected to ground.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

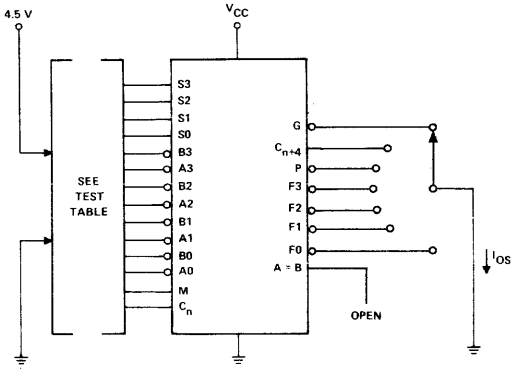


TEST TABLE

APPLY V_I MEASURE I_{IH} OR I_{IL}	CONDITIONS ON OTHER INPUTS FOR I_{IH}		CONDITIONS ON OTHER INPUTS FOR I_{IL}	
	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND
S0, S3, any A, any B, or M	NONE	ALL OTHER INPUTS	ALL OTHER INPUTS	NONE
S1, S2	B0, B1, B2, B3	ALL OTHER INPUTS	A0, A1, A2, A3	ALL OTHER INPUTS
C_n	ALL OTHER INPUTS	NONE	NONE	ALL OTHER INPUTS

Each input is tested separately.

FIGURE 3–I_{IH}, I_{IL}



TEST TABLE

OUTPUT UNDER TEST	APPLY 4.5 V	APPLY GND
G	S3, A3, B3	ALL OTHER INPUTS
C_{n+4}	NONE	ALL OTHER INPUTS
P, F0, F1, F2, or F3	ALL OTHER INPUTS	NONE

FIGURE 4–I_{OS}

9

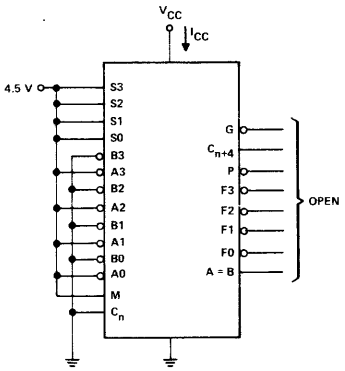


FIGURE 5–I_{CC}

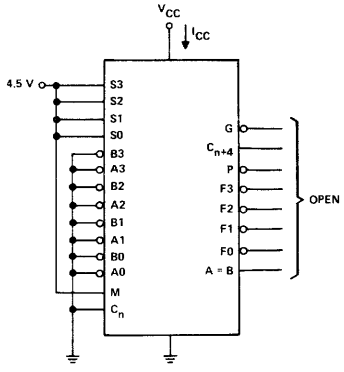


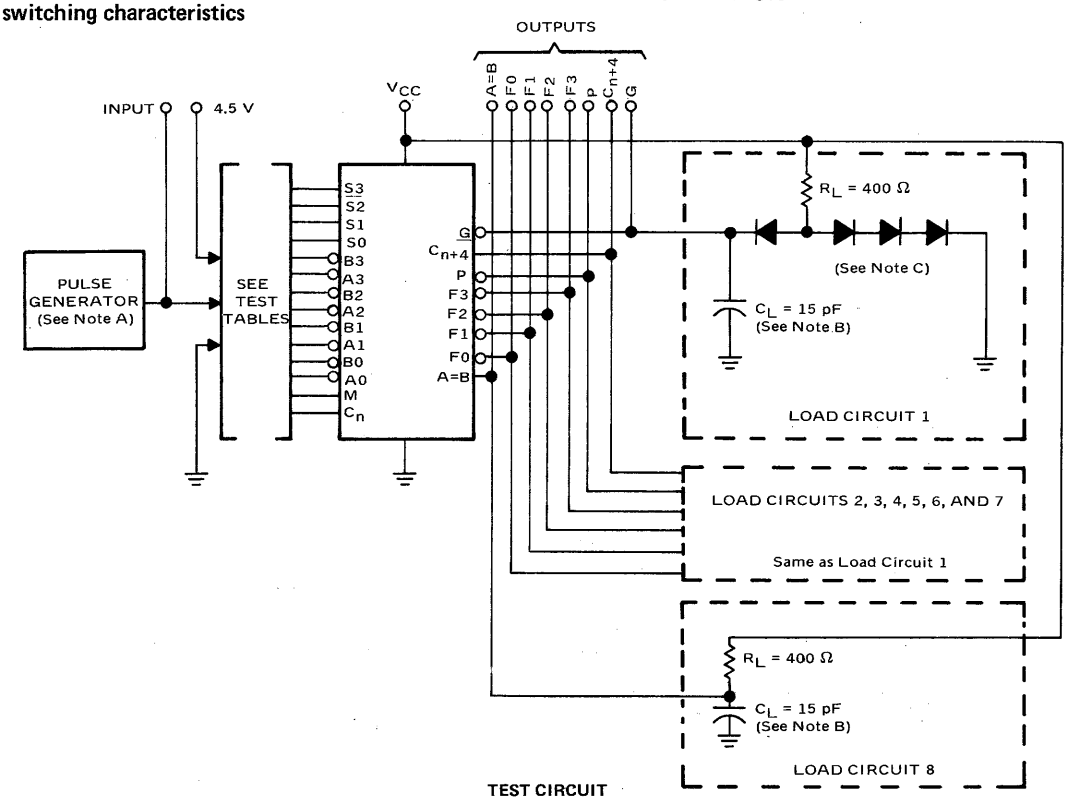
FIGURE 6–I_{CC}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

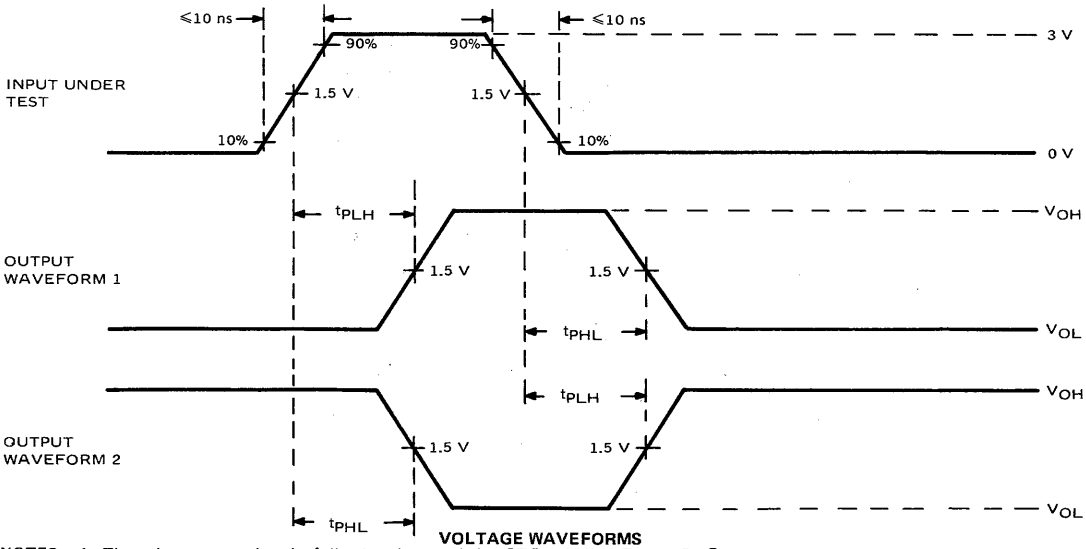
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 7–PROPAGATION DELAY TIMES

9

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

$\overline{\text{SUM}}$ MODE TEST TABLE

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	A	B	None	Remaining A and B	C_n	Any F	1
t_{PLH} / t_{PHL}	B	A	None	Remaining A and B	C_n	Any F	1
t_{PLH} / t_{PHL}	A	B	None	None	Remaining A and B, C_n	P	1
t_{PLH} / t_{PHL}	B	A	None	None	Remaining A and B, C_n	P	1
t_{PLH} / t_{PHL}	A	None	B	Remaining B	Remaining A, C_n	G	1
t_{PLH} / t_{PHL}	B	None	A	Remaining B	Remaining A, C_n	G	1
t_{PLH} / t_{PHL}	C_n	None	None	All A	All B	Any F or C_{n+4}	1

$\overline{\text{DIFF}}$ MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	A	None	B	Remaining A	Remaining B, C_n	Any F	1
t_{PLH} / t_{PHL}	B	A	None	Remaining A	Remaining B, C_n	Any F	2
t_{PLH} / t_{PHL}	A	None	B	None	Remaining A and B, C_n	P	1
t_{PLH} / t_{PHL}	B	A	None	None	Remaining A and B, C_n	P	2
t_{PLH} / t_{PHL}	A	B	None	None	Remaining A and B, C_n	G	1
t_{PLH} / t_{PHL}	B	None	A	None	Remaining A and B, C_n	G	2
t_{PLH} / t_{PHL}	A	B	None	Remaining A	Remaining B, C_n	A = B	2
t_{PLH} / t_{PHL}	B	A	None	Remaining A	Remaining B, C_n	A = B	2
t_{PLH} / t_{PHL}	C_n	None	None	All A and B	None	C_{n+4}	2

LOGIC MODE TEST TABLE

FUNCTION INPUTS: S1 = S3 = M = 4.5 V, S0 = S2 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	A	None	B	None	Remaining A and B, C_n	Any F	2
t_{PLH} / t_{PHL}	B	None	A	None	Remaining A and B, C_n	Any F	2

9

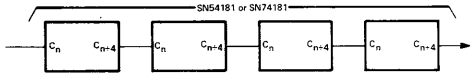
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL APPLICATION DATA

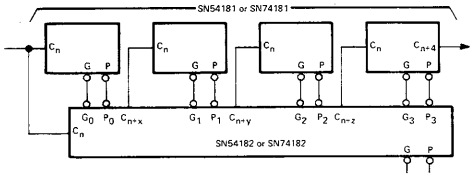
Typical addition times for various configurations are given in the table below. Subtraction times are in the same range as summation times.

TYPICAL ADDITION TIMES

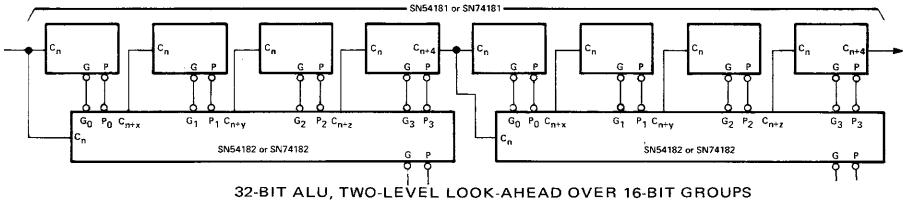
NO. OF BITS	TOTAL ADDITION TIME (ns)	ADD TIME PER BIT (ns)	PACKAGE COUNT		CARRY BETWEEN ALU's
			SN54181/ SN74181	SN54182/ SN74182	
4	24	6.0	1		NONE
8	36	4.5	2		RIPPLE
12	48	4.0	3		RIPPLE
12	36	3.0	3	1	FULL LOOK-AHEAD
16	60	3.8	4		RIPPLE
16	36	2.2	4	1	FULL LOOK-AHEAD
32	120	3.8	8		RIPPLE
32	96	3.0	8	1	PARTIAL LOOK-AHEAD
32	72	2.2	8	2	PARTIAL LOOK-AHEAD
32	60	1.9	8	3	FULL LOOK-AHEAD



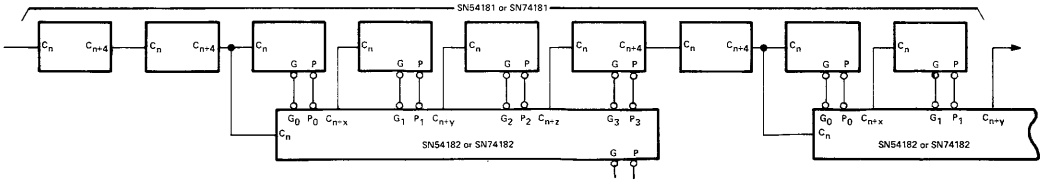
16-BIT ALU, RIPPLE CARRY



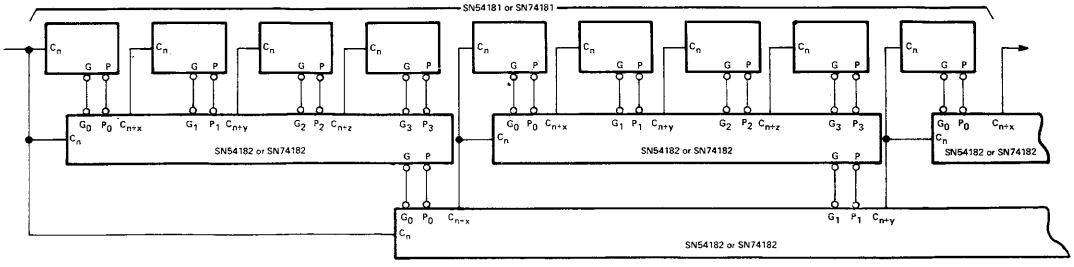
16-BIT ALU, TWO-LEVEL LOOK-AHEAD



32-BIT ALU, TWO-LEVEL LOOK-AHEAD OVER 16-BIT GROUPS



COMBINED TWO-LEVEL LOOK-AHEAD AND RIPPLE-CARRY ALU



64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS

A and B inputs and F outputs are not shown.

9

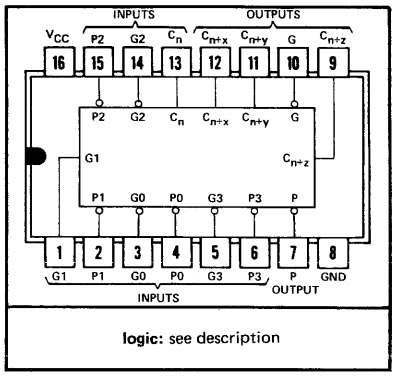
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54182, SN74182
LOOK-AHEAD CARRY GENERATORS

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
G0, G1, G2, G3	3, 1, 14, 5	ACTIVE-LOW CARRY GENERATE INPUTS
P0, P1, P2, P3	4, 2, 15, 6	ACTIVE-LOW CARRY PROPAGATE INPUTS
C_n	13	CARRY INPUT
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	CARRY OUTPUTS
G	10	ACTIVE-LOW CARRY GENERATE OUTPUT
P	7	ACTIVE-LOW CARRY PROPAGATE OUTPUT
V_{CC}	16	SUPPLY VOLTAGE
GND	8	GROUND

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



logic: see description

†Pin assignments for these circuits are the same for all packages.

description

The SN54182, SN74182 is a high-speed, look-ahead carry generator capable of anticipating a carry across four binary adders or group of adders. It is cascadable to perform full look-ahead across n-bit adders, with only 13 nanoseconds delay for each level of look-ahead. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table above.

The SN54182 or SN74182, when used in conjunction with the SN54181 or SN74181 arithmetic logic unit (ALU), provides full high-speed carry look-ahead capability for up to n-bit words. Each SN54182/SN74182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. Applications data for the SN54181/SN74181 illustrates cascading of SN54182/SN74182 circuits to perform multi-level look-ahead.

Carry inputs and outputs of the SN54181/SN74181 are in their true form and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry (input, outputs, generate, and propagate) functions of the look-ahead circuit are implemented in the compatible forms. Reinterpretations of carry functions at the SN54181/SN74181 are also applicable and compatible with the look-ahead package. Logic equations are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$\overline{P} = \overline{P_3P_2P_1P_0}$$

Inputs of the SN54182/SN74182 are diode-clamped to minimize transmission-line effects, and Darlington outputs are employed to improve turn-off times and reduce propagation delay times. Typically, the average carry time is 13 nanoseconds, and power dissipation is typically 180 milliwatts or 11 milliwatts per gate. The SN54182 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74182 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54182 Circuits . . . . . −55°C to 125°C
SN74182 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each G input in conjunction with any other G input or in conjunction with any P input.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

		SN54182			SN74182			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_{IH}	High-level input current (C_n input)	3	V_{CC} = MAX, V_I = 2.4 V				80	μA
I_{IH}	High-level input current (P3 input)						120	μA
I_{IH}	High-level input current (P2 input)						160	μA
I_{IH}	High-level input current (P0, P1, or G3 input)						200	μA
I_{IH}	High-level input current (G0 or G2 input)						360	μA
I_{IH}	High-level input current (G1 input)						400	μA
I_{IH}	High-level input current (any input)	3	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (C_n input)	3	V_{CC} = MAX, V_I = 0.4 V				−3.2	mA
I_{IL}	Low-level input current (P3 input)						−4.8	mA
I_{IL}	Low-level input current (P2 input)						−6.4	mA
I_{IL}	Low-level input current (P0, P1, or G3 input)						−8	mA
I_{IL}	Low-level input current (G0 or G2 input)						−14.4	mA
I_{IL}	Low-level input current (G1 input)						−16	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX		−40		−100	mA
I_{CCH}	Supply current, all outputs high	5	V_{CC} = MAX	SN54182		27		mA
				SN74182		27		
I_{CCL}	Supply current, all outputs low	6	V_{CC} = MAX	SN54182		45	65	mA
				SN74182		45	72	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed 1 second.

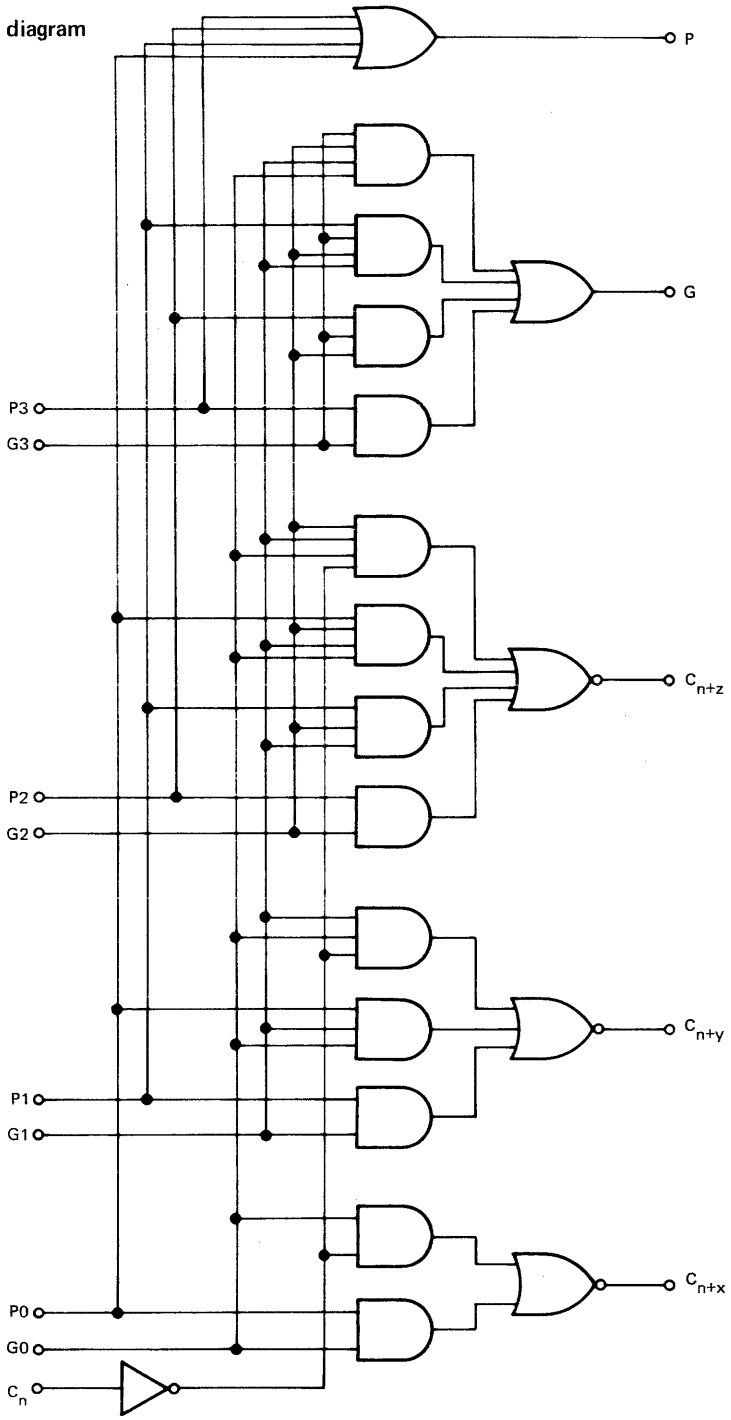
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	7	C_L = 15 pF, R_L = 400 Ω		11	17	ns
t_{PHL}	Propagation delay time, high-to-low-level output				15	22	ns

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

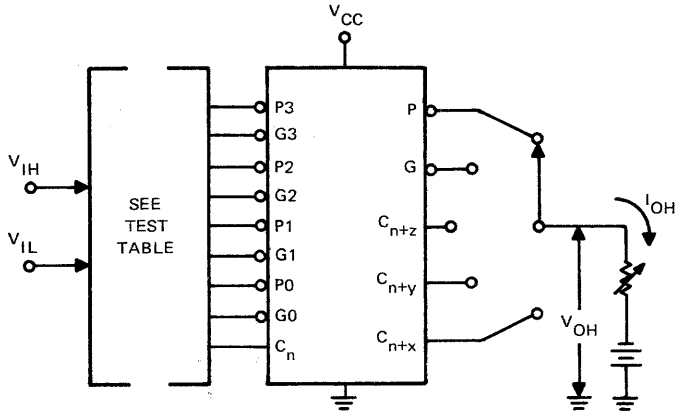
functional block diagram



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶

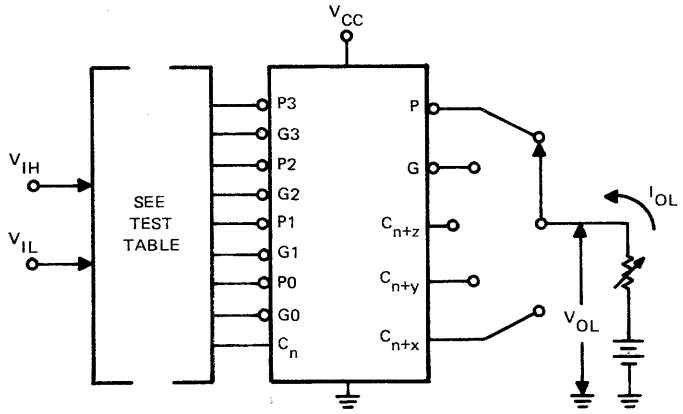


TEST TABLE

OUTPUT UNDER TEST	APPLY V_{IH}	APPLY V_{IL}
P	P0	P3, P2, P1
G	P3, G3	P2, P1, G2, G1, G0
C_{n+z}	P2, P1, P0, G1, G0	G2, C_n
C_{n+y}	P1, P0, G0	G1, C_n
C_{n+x}	P0	G0, C_n

Inputs not otherwise specified are connected to ground.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



TEST TABLE

OUTPUT UNDER TEST	APPLY V_{IH}	APPLY V_{IL}
P	NONE	P3, P2, P1, P0
G	P3, P2, P1, G2, G1, P0, G0	G3
C_{n+z}	P2, G2, C_n	P1, G1, P0, G0
C_{n+y}	P1, G1, C_n	P0, G0
C_{n+x}	P0, G0, C_n	NONE

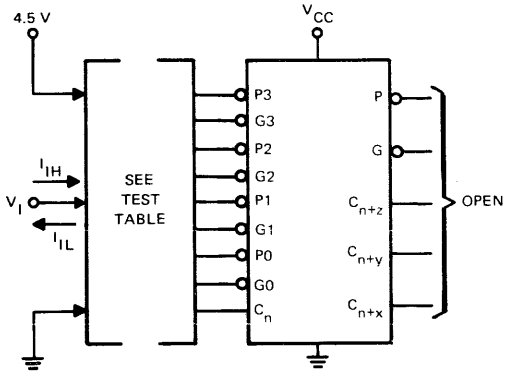
Inputs not otherwise specified are connected to ground.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}

¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

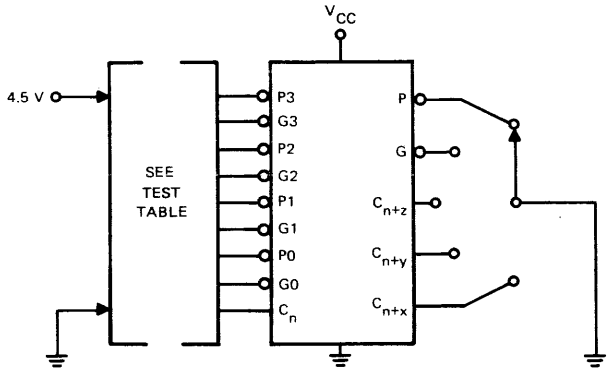


TEST TABLE

APPLY V_I, MEASURE	CONDITIONS ON OTHER INPUTS FOR I_{IH}		CONDITIONS ON OTHER INPUTS FOR I_{IL}	
I_{IH}, I_{IL}	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND
any P, or C_n	NONE	ALL OTHER INPUTS	ALL OTHER INPUTS	NONE
any G	C_n	ALL OTHER INPUTS	ALL OTHER INPUTS	C_n

Each input is tested separately.

FIGURE 3–I_{IH}, I_{IL}



TEST TABLE

OUTPUT UNDER TEST	APPLY 4.5 V	APPLY GND
P	P3, P2, P1, P0	ALL OTHER INPUTS
G	ALL OTHER INPUTS	C_n
C_{n+z}	C_n	ALL OTHER INPUTS
C_{n+y}	C_n	ALL OTHER INPUTS
C_{n+x}	C_n	ALL OTHER INPUTS

FIGURE 4–I_{OS}

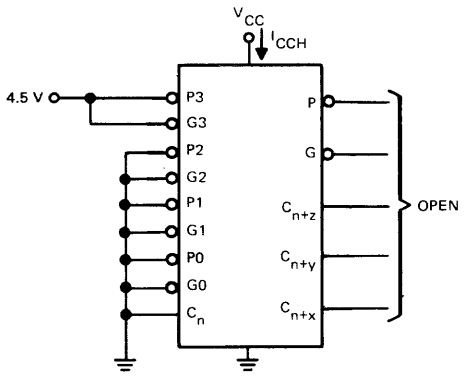


FIGURE 5–I_{CCH}

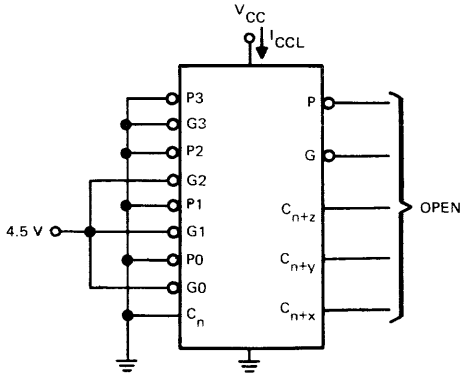


FIGURE 6–I_{CCL}

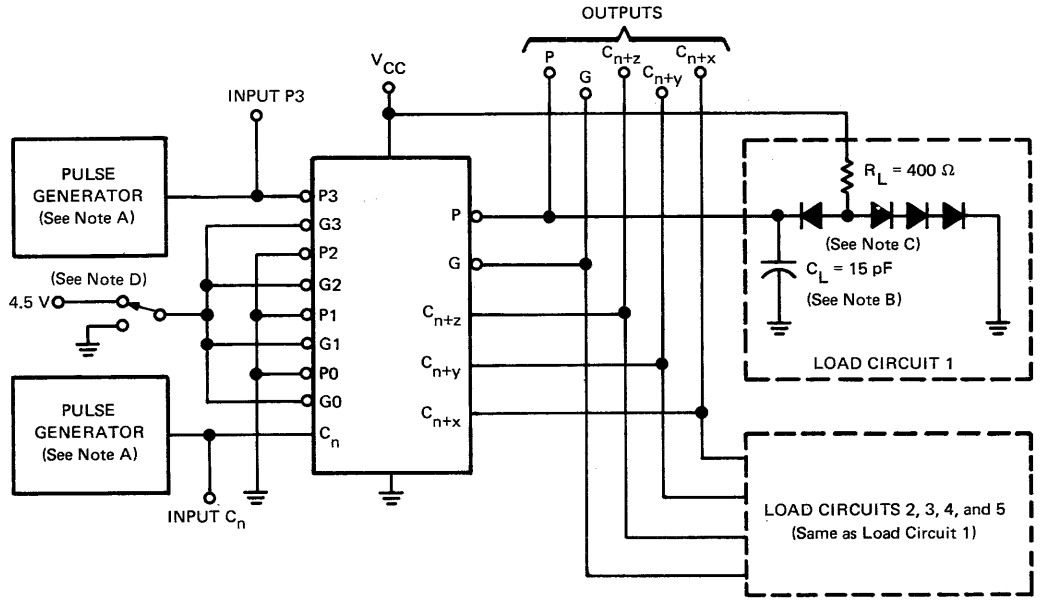
§ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

9

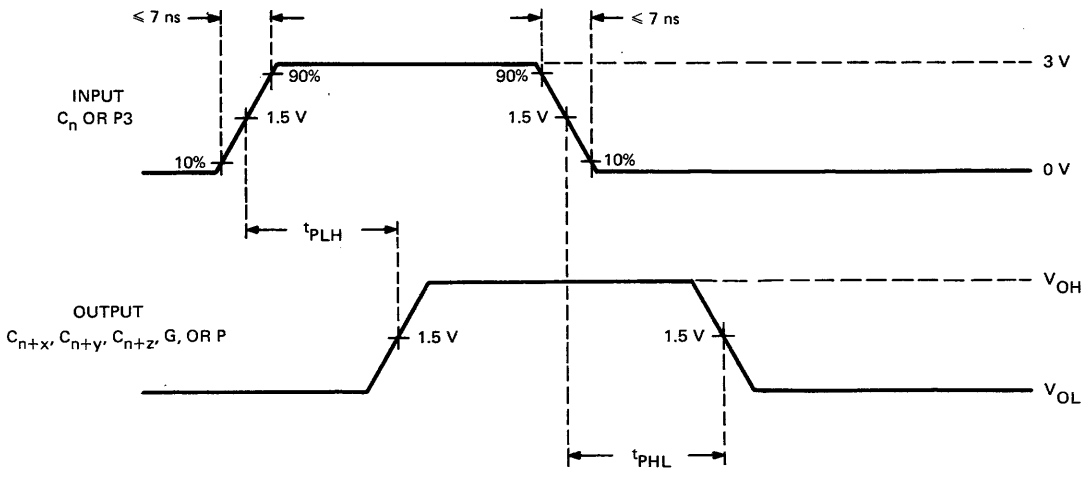
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. Apply 4.5 V for all tests except G output. When testing G output, apply ground.

FIGURE 7–PROPAGATION DELAY TIMES

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54H183, SN74H183
DUAL CARRY-SAVE FULL ADDERS

- For Use in Multiple-Input Carry-Save Adders
- High-Speed, High-Fan-Out Darlington Outputs
- Input Clamping Diodes Simplify System Design
- Compatible with Most TTL and DTL Circuits
- Typical Average Sum and Carry Propagation Delays: 11 ns
- Typical Power Dissipation: 110 mW per Bit

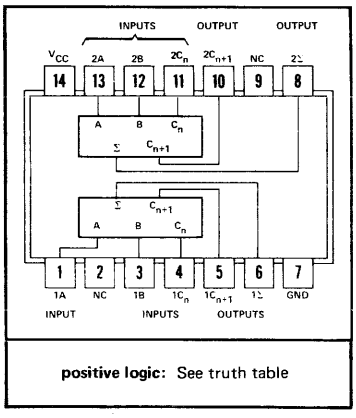
logic

TRUTH TABLE

INPUTS			OUTPUTS	
C_n	B	A	Σ	C_{n+1}
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

H = high level, L = low level

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See truth table

NC—No internal connection

†Pin assignments for these circuits are the same for all packages.

description

This dual full adder features an individual carry output from each bit for use in multiple-input, carry-save techniques to produce the true sum and true carry outputs with no more than two levels of logic. The circuit utilizes high-speed, high-fan-out, transistor-transistor logic (TTL), but is compatible with both DTL and TTL families. Typical average sum and carry propagation delay times are 11 nanoseconds each. Typical power dissipation is 110 milliwatts per bit. The SN54H183 is characterized for operation over the full military temperature range of −55°C to 125°C, and the SN74H183 is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54H183 Circuits . . . . . −55°C to 125°C
SN74H183 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

		SN54H183			SN74H183			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1			2			V
V_{IL}	Low-level input voltage	2					0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −1 mA		2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.4	V
I_{IH}	High-level input current at any input	3	V_{CC} = MAX, V_I = 2.4 V				150	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current at any input	3	V_{CC} = MAX, V_I = 0.4 V				−6	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX		−40		−100	mA
I_{CCL}	Supply current, all outputs low	5	V_{CC} = MAX, V_I = 0	SN54H183		48	69	mA
				SN74H183		48	75	
I_{CCH}	Supply current, all outputs high	5	V_{CC} = MAX, V_I = 4.5 V			40		mA

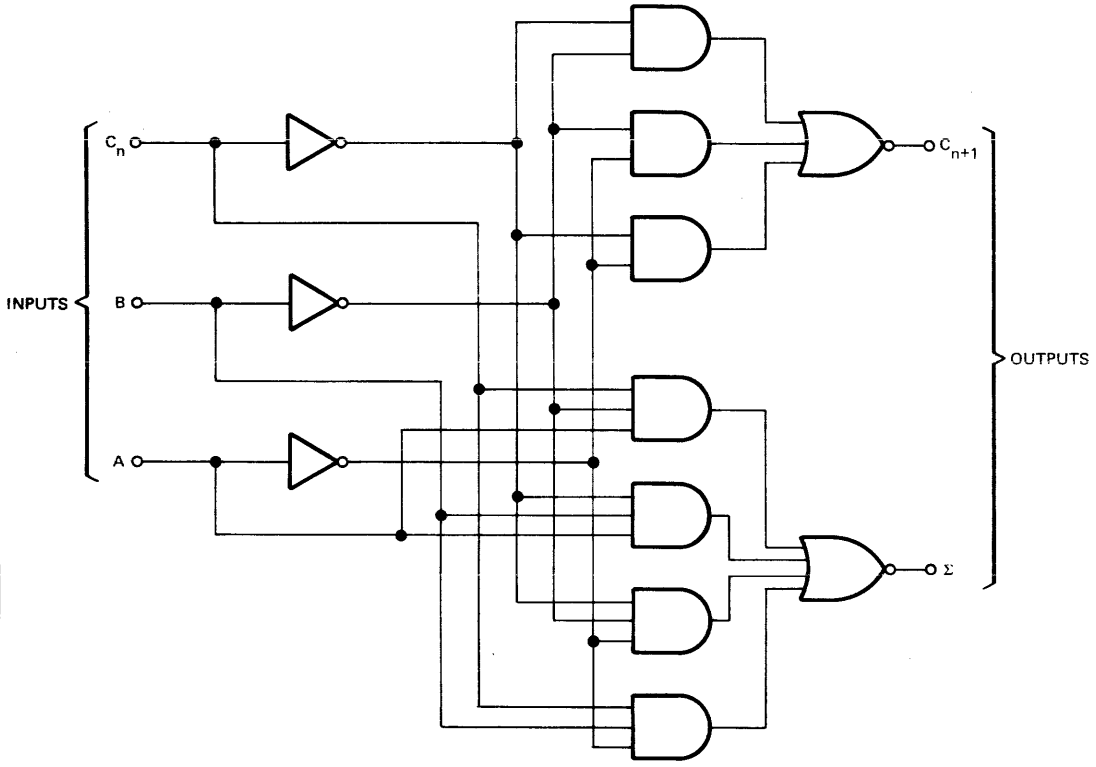
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit test should not exceed 1 second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	6	C_L = 25 pF, R_L = 280 Ω		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output				12	18	ns

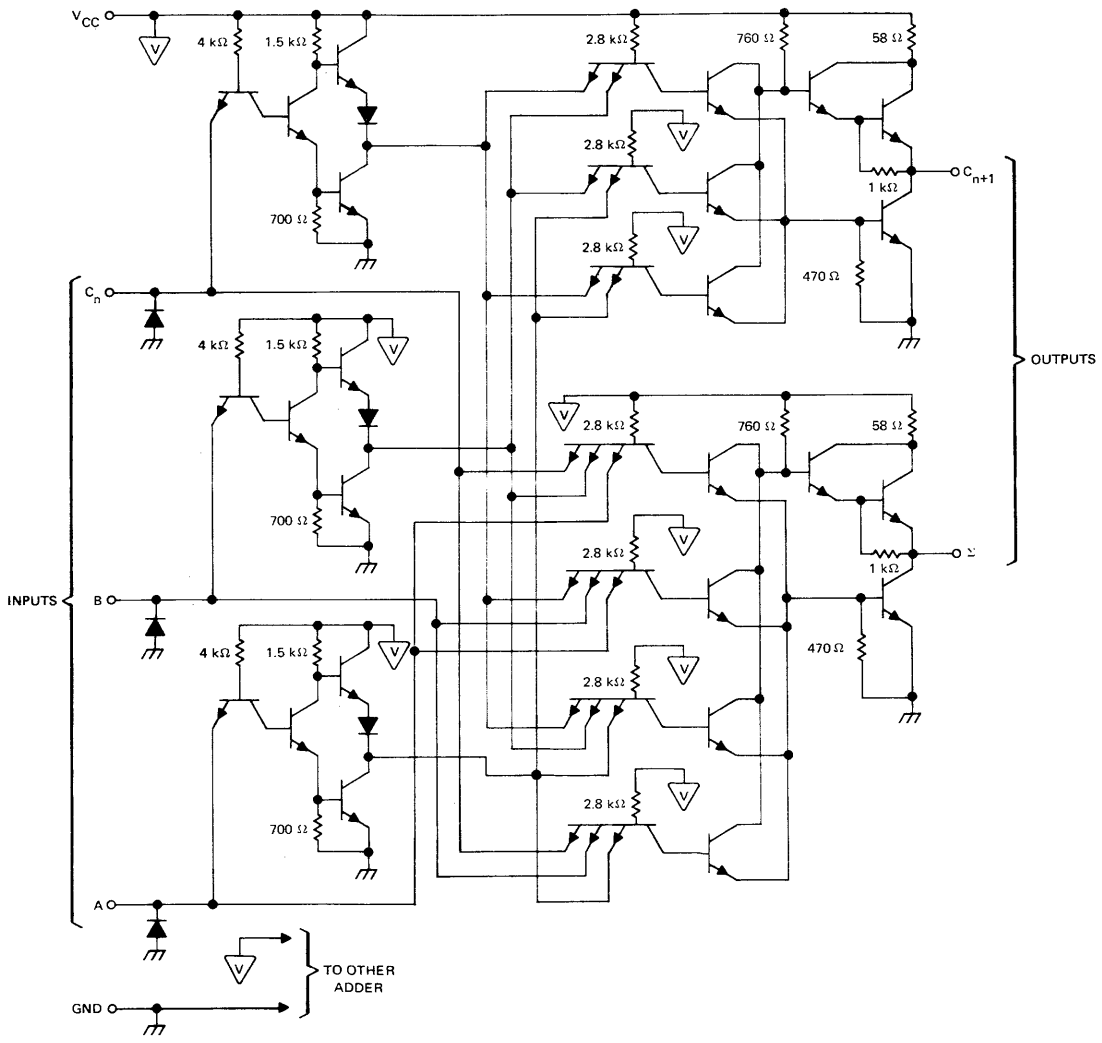
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram (each adder)



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

schematic (each adder)

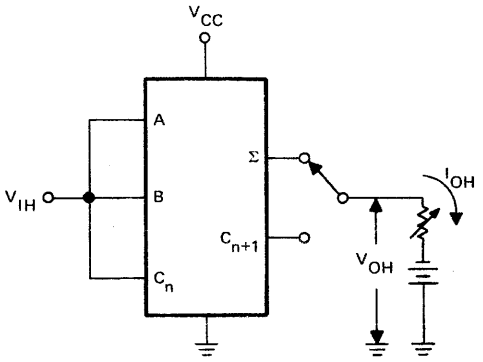


Component values shown are nominal.

▽... V_{CC} bus

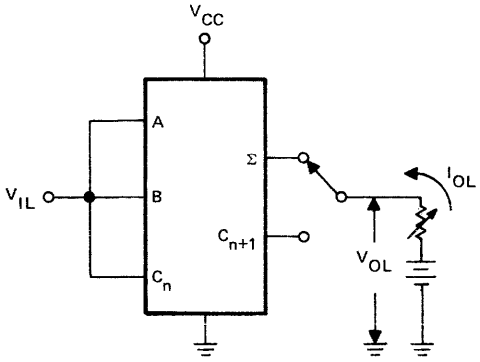
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶



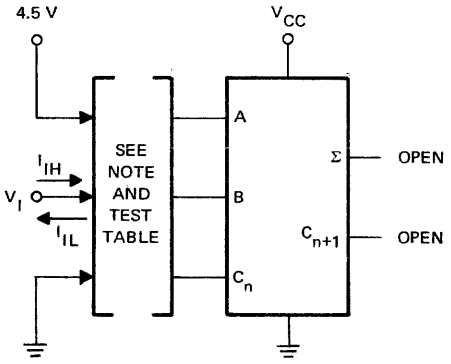
Each output is tested separately.

FIGURE 1–V_{IH}, V_{OH}



Each output is tested separately.

FIGURE 2–V_{IL}, V_{OL}

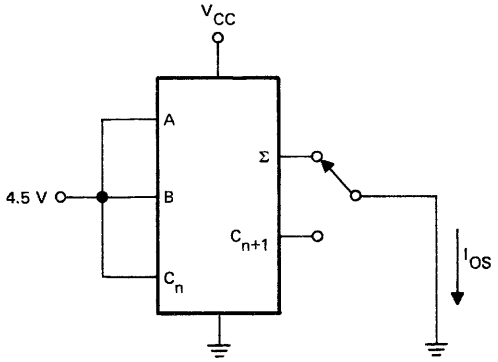


Each input is tested for both combinations of states of the other inputs.

TEST TABLE

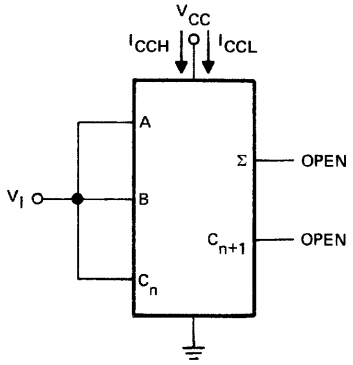
APPLY V_I, MEASURE I_{IH}/I_{IL}	CONDITIONS ON OTHER INPUTS	
	4.5 V	GND
A	B, C_n	NONE
	B	C_n
	C_n	B
	NONE	B, C_n
B	A, C_n	NONE
	A	C_n
	C_n	A
	NONE	A, C_n
C_n	A, B	NONE
	A	B
	B	A
	NONE	A, B

FIGURE 3–I_{IH}, I_{IL}



Each output is tested separately.

FIGURE 4–I_{OS}



Both adders are tested simultaneously.

FIGURE 5–I_{CCH}, I_{CCL}

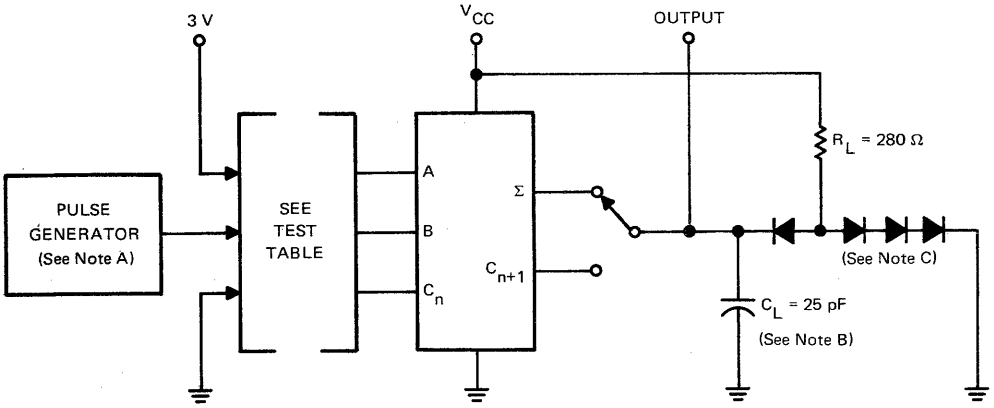
¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

9

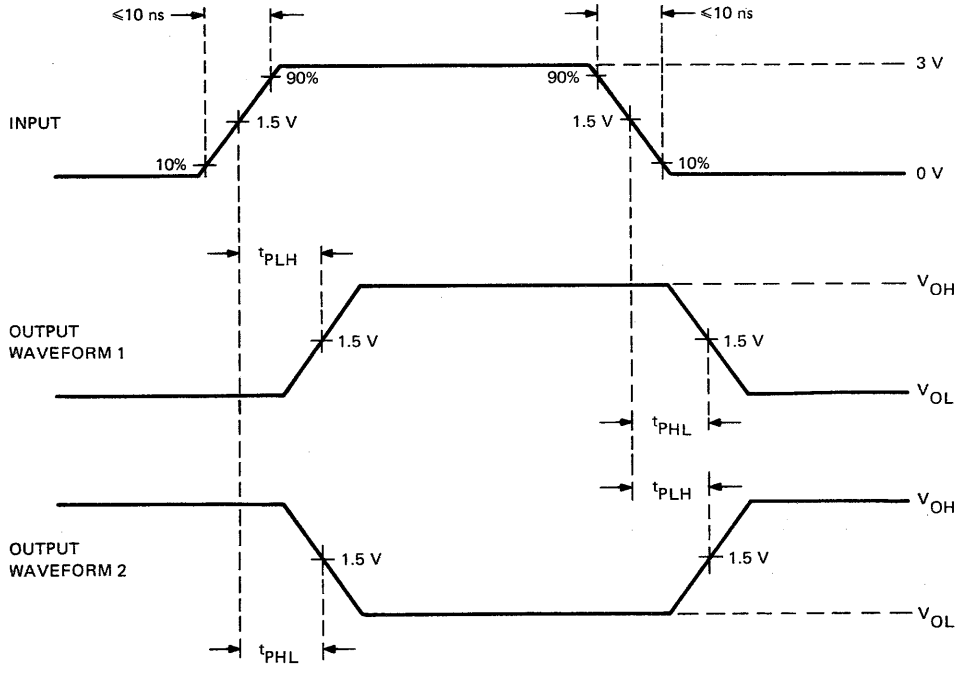
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 6–PROPAGATION DELAY TIMES

9

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

TEST TABLE FOR FIGURE 6 (EACH ADDER)

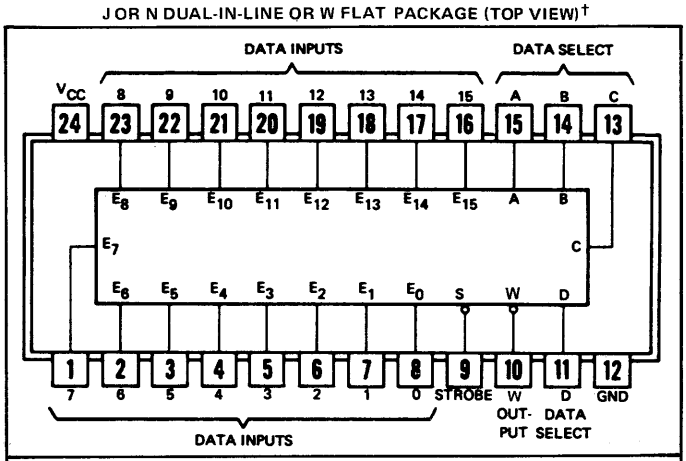
TEST NO.	PARAMETER	APPLY PULSE GENERATOR	APPLY 3 V	APPLY GND	OUTPUT UNDER TEST	OUTPUT WAVEFORM
1	t_{PLH}	A	B, C_n		Σ	1
2	t_{PHL}					
3	t_{PLH}	A	B	C_n	Σ	2
4	t_{PHL}					
5	t_{PLH}	A	C_n	B	Σ	2
6	t_{PHL}					
7	t_{PLH}	A		B, C_n	Σ	1
8	t_{PHL}					
9	t_{PLH}	A	B	C_n	C_{n+1}	1
10	t_{PHL}					
11	t_{PLH}	A	C_n	B	C_{n+1}	1
12	t_{PHL}					
13	t_{PLH}	B	A, C_n		Σ	1
14	t_{PHL}					
15	t_{PLH}	B	A	C_n	Σ	2
16	t_{PHL}					
17	t_{PLH}	B	C_n	A	Σ	2
18	t_{PHL}					
19	t_{PLH}	B		A, C_n	Σ	1
20	t_{PHL}					
21	t_{PLH}	B	A	C_n	C_{n+1}	1
22	t_{PHL}					
23	t_{PLH}	B	C_n	A	C_{n+1}	1
24	t_{PHL}					
25	t_{PLH}	C_n	A, B		Σ	1
26	t_{PHL}					
27	t_{PLH}	C_n	A	B	Σ	2
28	t_{PHL}					
29	t_{PLH}	C_n	B	A	Σ	2
30	t_{PHL}					
31	t_{PLH}	C_n		A, B	Σ	1
32	t_{PHL}					
33	t_{PLH}	C_n	A	B	C_{n+1}	1
34	t_{PHL}					
35	t_{PLH}	C_n	B	A	C_{n+1}	1
36	t_{PHL}					

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54150, SN54151, SN54152, SN74150, SN74151, SN74152
DATA SELECTORS/MULTIPLEXERS

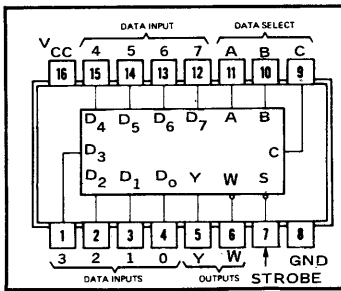
SN54150, SN74150
J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic

$$W = \bar{S}(\bar{A}\bar{B}\bar{C}\bar{D}E_0 + A\bar{B}\bar{C}\bar{D}E_1 + \bar{A}B\bar{C}\bar{D}E_2 + AB\bar{C}\bar{D}E_3 + \bar{A}\bar{B}C\bar{D}E_4 + A\bar{B}C\bar{D}E_5 + \bar{A}BC\bar{D}E_6 + ABC\bar{D}E_7$$
$$\bar{A}\bar{B}\bar{C}DE_8 + A\bar{B}\bar{C}DE_9 + \bar{A}B\bar{C}DE_{10} + AB\bar{C}DE_{11} + \bar{A}\bar{B}CDE_{12} + A\bar{B}CDE_{13} + \bar{A}BCDE_{14} + ABCDE_{15})$$

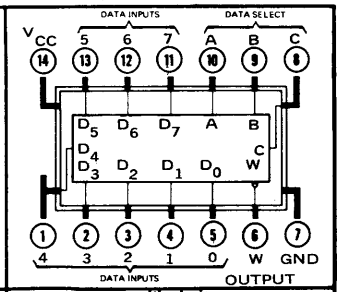
SN54151, SN74151
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



positive logic

$$Y = \bar{S}(\bar{A}\bar{B}\bar{C}D_0 + A\bar{B}\bar{C}D_1 + \bar{A}B\bar{C}D_2 + AB\bar{C}D_3 + \bar{A}\bar{B}CD_4 + A\bar{B}CD_5 + \bar{A}BCD_6 + ABCD_7) \quad W = \bar{Y}$$

SN54152, SN74152
W FLAT PACKAGE
(TOP VIEW)



positive logic

$$W = (\bar{A}\bar{B}\bar{C}D_0 + A\bar{B}\bar{C}D_1 + AB\bar{C}D_3 + \bar{A}BCD_4 + A\bar{B}CD_5 + \bar{A}BCD_6 + ABCD_7)$$

†Pin assigments for these circuits are the same for all packages.

features

- selects one-of-sixteen (or one-of-eight) data sources
- serves as a five-variable-function generator (SN54150, SN74150)
- performs parallel-to-serial conversion
- permits multiplexing from N lines to 1 line
- input-clamping diodes simplify system design
- typical propagation delay times:
  - through 4 select levels – 28 ns
  - through 3 select levels – 20 ns
  - data input to output – 10 ns
- high fan-out, low impedance, totem-pole outputs
- fully compatible with TTL, DTL and other MSI circuits

description

Each of these monolithic, data selectors/multiplexers contain inverter/drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-INVERT gate. The SN54151/74151 features complementary outputs whereas the SN54150/SN74150 and SN54152/SN74152 have inverted outputs only. The SN54150/SN74150 and SN54151/SN74151 circuits are provided with a strobe-input which, when taken to a logical 0, enables the function of these multiplexers.

These data selectors/multiplexers are fully compatible for use with other TTL or DTL circuits. Each input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized Series 54/74 loads is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Typical power dissipations are:

SN54150/SN74150 – 200 milliwatts
SN54151/SN74151 – 145 milliwatts
SN54152/SN74152 – 130 milliwatts

These data selectors feature Series 54H/74H circuitry for the OR function. This is done to minimize the capacitive effects of paralleling the phase-splitter transistors and thus reduce the propagation delay time. The SN54150, SN54151, and SN54152 are characterized for operation over the full military temperature range of −55°C to 125°C; and the SN74150, SN74151 and SN74152 are characterized for operation from 0°C to 70°C.

9

logic

TRUTH TABLE (SN54150/SN74150 ONLY)

INPUTS																		OUTPUT
D	C	B	A	STROBE	E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

When used to indicate an input condition, X = LOGICAL 1 OR LOGICAL 0

logic (continued)

TRUTH TABLE (SN54151/SN74151 AND SN54152/SN74152 ONLY)

INPUTS												OUTPUTS	
C	B	A	STROBE(1)	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y(1)	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

NOTES: 1. SN54151/SN74151 only.
2. When used to indicate an input, X = irrelevant.

9

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Note 1) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN54150, SN54151, SN54152 Circuits . . . . . −55°C to 125°C
SN74150, SN74151, SN74152 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	SN54150, SN54151, SN54152 Circuits	4.5	5	5.5	V
	SN74150, SN74151, SN74152 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Each Output (N):	Logical 0			10	
	Logical 1			20	

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	1 AND 2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −800 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1 AND 2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
I_{OS}	Short circuit output current §	4	V_{CC} = MAX, V_{out} = 0	SN54150, SN54151, SN54152	−20		−55	mA
				SN74150, SN74151, SN74152	−18		−55	mA
I_{CC}	Supply current (SN54150/SN74150)	5	V_{CC} = MAX, V_{in} = 4.5 V			40	68	mA
I_{CC}	Supply current (SN54151/SN74151)	5	V_{CC} = MAX, V_{in} = 4.5 V			29	48	mA
I_{CC}	Supply current (SN54152/SN74152)	5	V_{CC} = MAX, V_{in} = 4.5 V			26	43	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

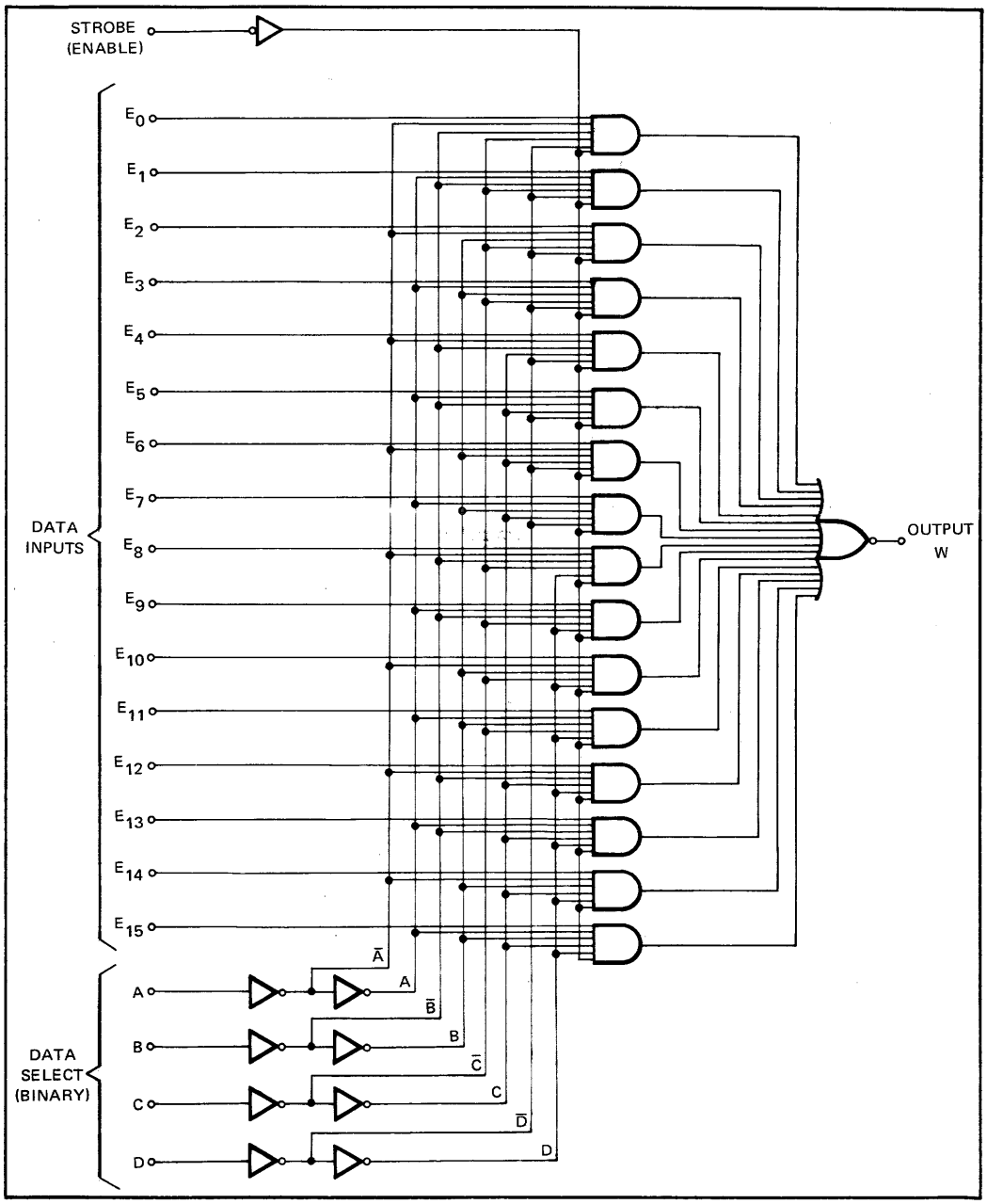
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	A, B, or C (4 levels)	Y	6	C_L = 15 pF, R_L = 400 Ω		20	30	ns
t_{pd1}	A, B, or C (4 levels)	Y				35	52	ns
t_{pd0}	A, B, C, or D (3 levels)	W				22	33	ns
t_{pd1}	A, B, C, or D (3 levels)	W				23	35	ns
t_{pd0}	STROBE	Y				19	30	ns
t_{pd1}	STROBE	Y				35	52	ns
t_{pd0}	STROBE	W				21	30	ns
t_{pd1}	STROBE	W				15.5	24	ns
t_{pd0}	D_0 thru D_7	Y				16	24	ns
t_{pd1}	D_0 thru D_7	Y				19	29	ns
t_{pd0}	E_0 thru E_{15}, D_0 thru D_7	W				8.5	14	ns
t_{pd1}	E_0 thru E_{15}, D_0 thru D_7	W				13	20	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

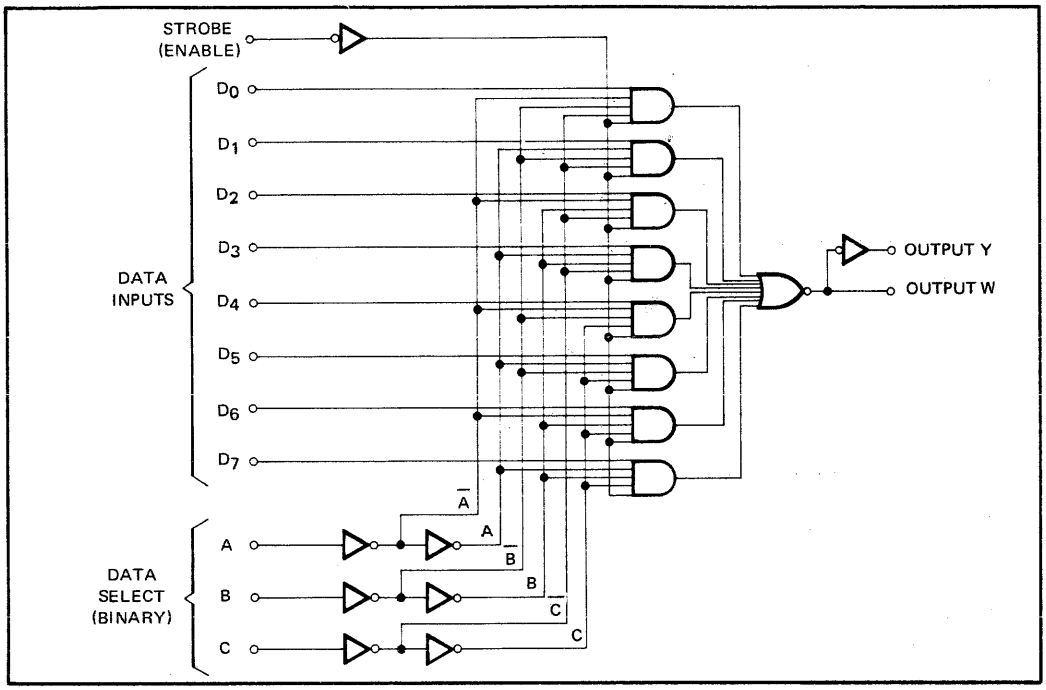
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output of the SN54151/SN74151 should be shorted at a time.

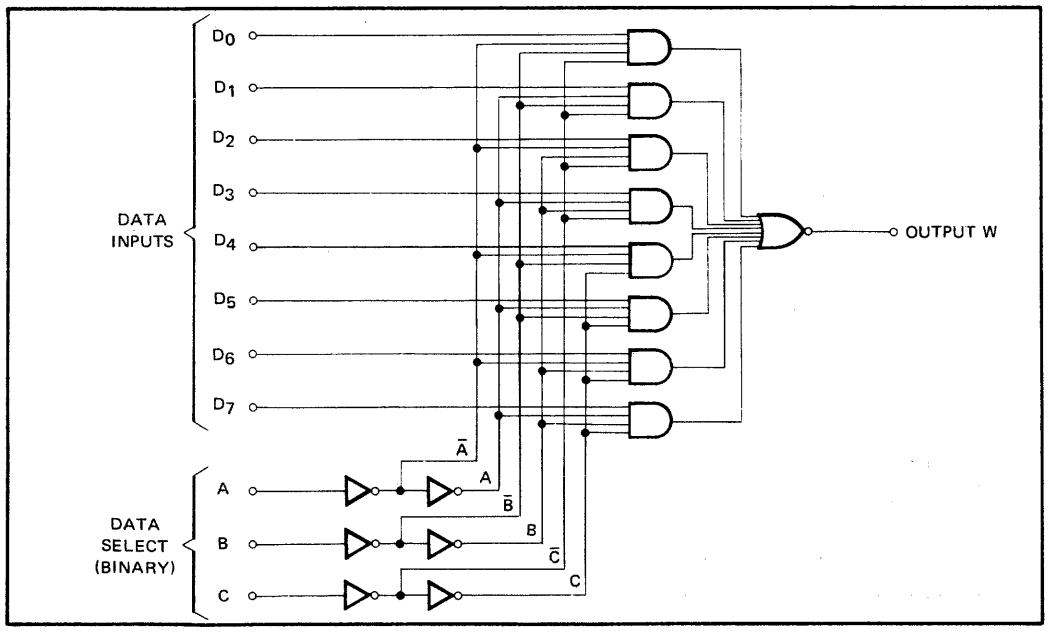
functional block diagram



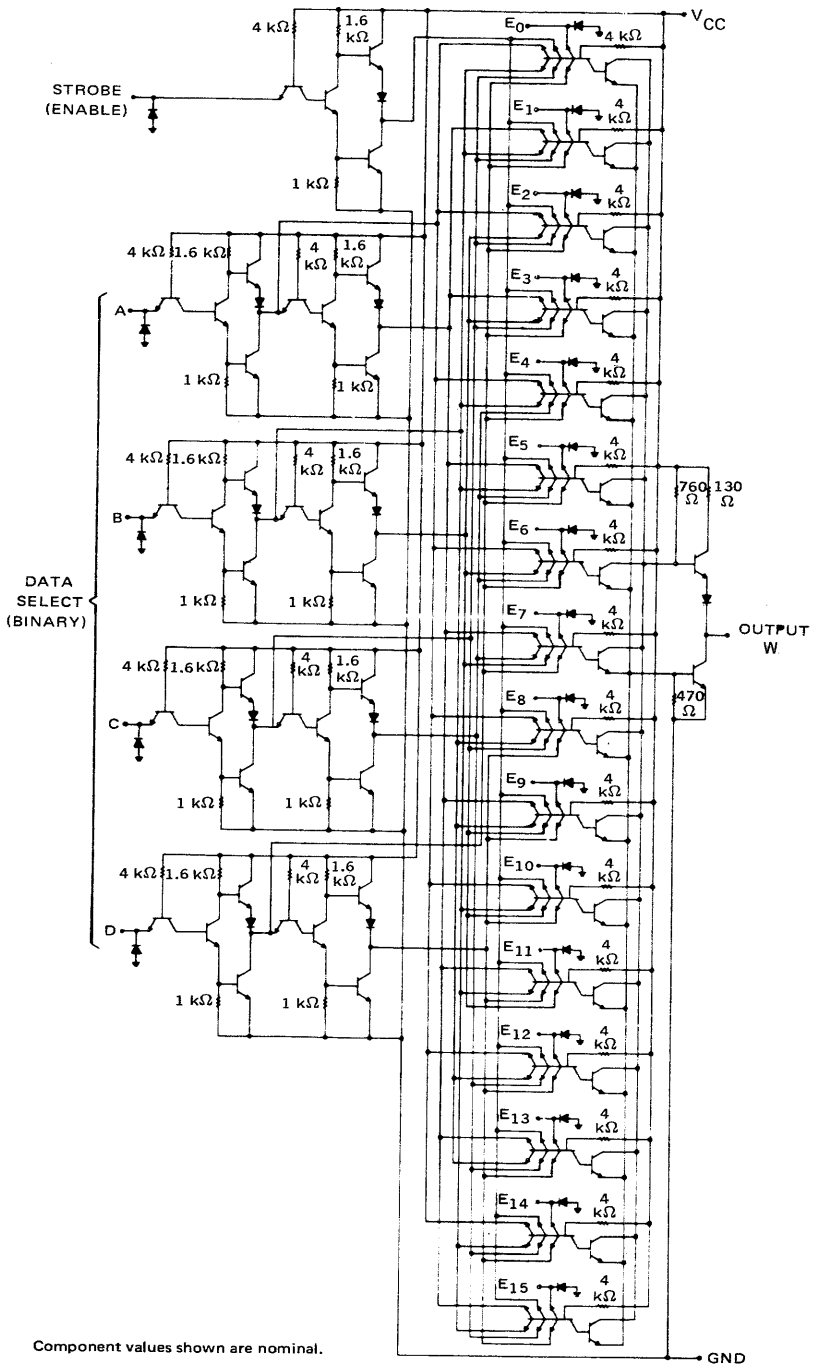
functional block diagram (SN54151, SN74151)



functional block diagram (SN54152, SN74152)



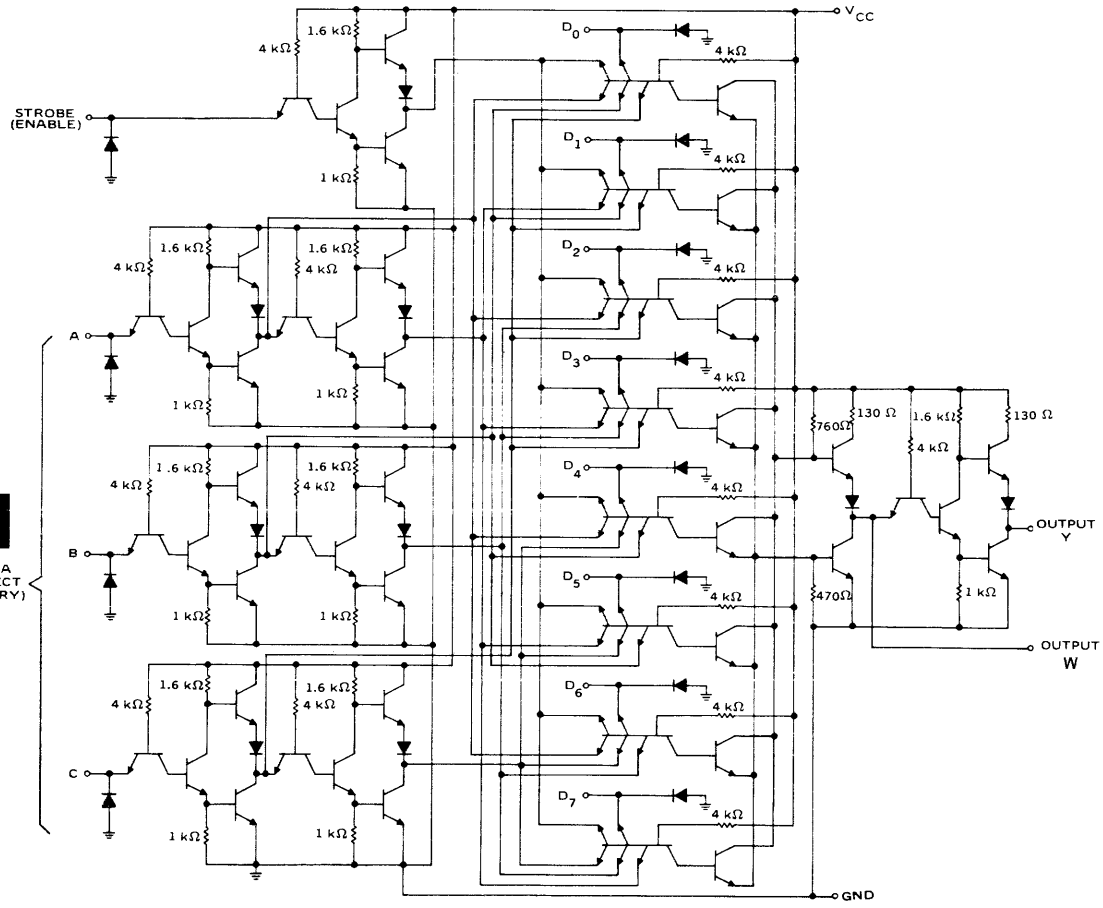
schematic



Component values shown are nominal.

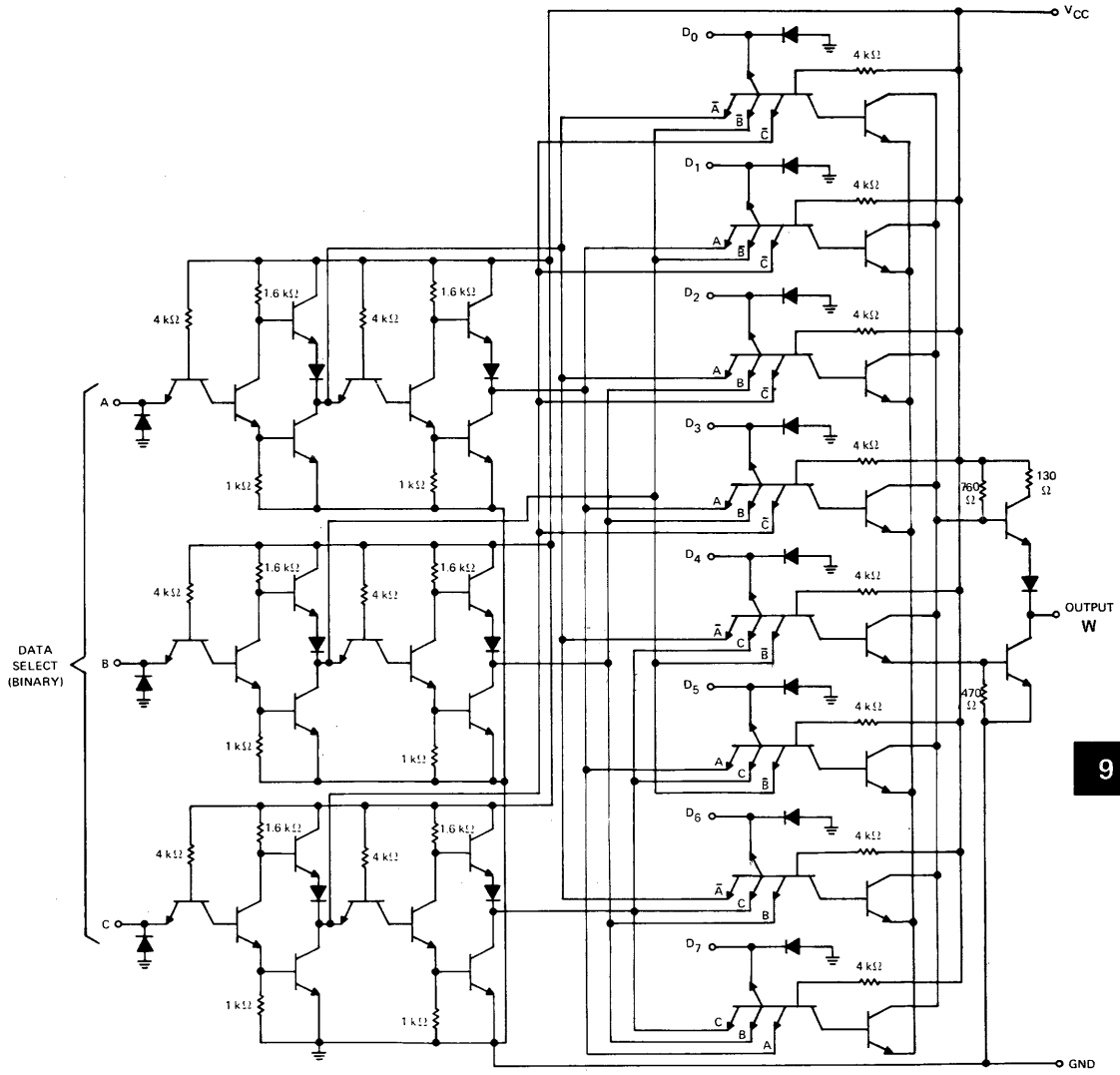
9

schematic



Component values shown are nominal.

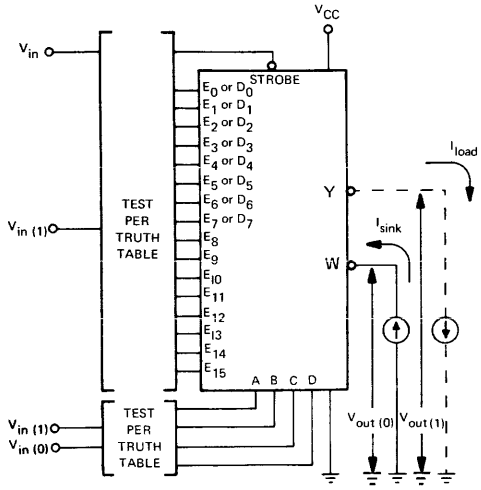
schematic



Component values shown are nominal.

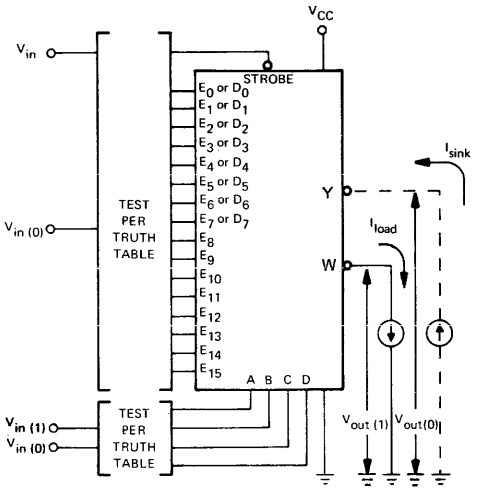
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



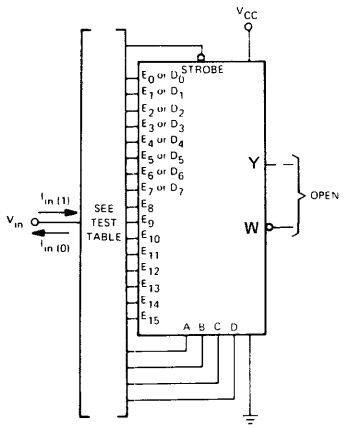
1. $V_{in(0)}$ is applied to STROBE; 8-4-2-1 code is applied to A, B, C, D; and input/output condition is tested for each step of the code.
2. $V_{in(1)}$ is applied to STROBE at which time $V_{out(0)}$ is measured at Y and $V_{out(1)}$ is measured at W.

FIGURE 1



1. $V_{in(0)}$ is applied to STROBE; 8-4-2-1 is applied to A, B, C, D; and input/output condition is tested for each step of the code.

FIGURE 2



TEST TABLE

INPUT CONDITIONS				TEST	
A	B	C	D	$I_{in(0)}$	$I_{in(1)}$
0	0	0	0	E_0 or D_0	E_{15} or D_7
1	0	0	0	E_1 or D_1	E_{14} or D_6
0	1	0	0	E_2 or D_2	E_{13} or D_5
1	1	0	0	E_3 or D_3	E_{12} or D_4
0	0	1	0	E_4 or D_4	E_{11} or D_3
1	0	1	0	E_5 or D_5	E_{10} or D_2
0	1	1	0	E_6 or D_6	E_9 or D_1
1	1	1	0	E_7 or D_7	E_8 or D_0
0	0	0	1	E_8	E_7
1	0	0	1	E_9	E_6
0	1	0	1	E_{10}	E_5
1	1	0	1	E_{11}	E_4

INPUT CONDITIONS				TEST	
A	B	C	D	$I_{in(0)}$	$I_{in(1)}$
0	0	1	1	E_{12}	E_3
1	0	1	1	E_{13}	E_2
0	1	1	1	E_{14}	E_1
1	1	1	1	E_{15}	E_0
0				A	
	0			B	
		0		C	
			0	D	
1					A
	1				B
		1			C
			1		D

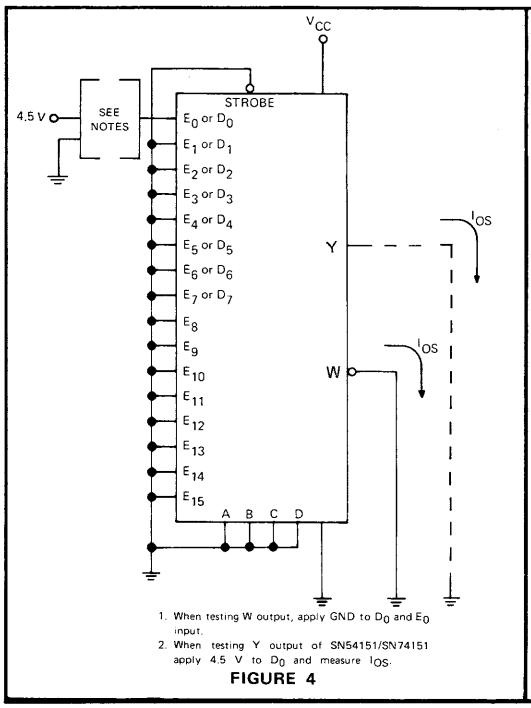
1. When testing strobe input, all other inputs are open.

FIGURE 3

† Arrows indicate actual direction of current flow. Tests as shown, are for the SN54150/SN74150. Identical tests as applicable are performed for the SN54151/SN74151 and SN54152/SN74152.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



1. When testing W output, apply GND to D_0 and E_0 input.
2. When testing Y output of SN54151/SN74151 apply 4.5 V to D_0 and measure I_{OS}.

FIGURE 4

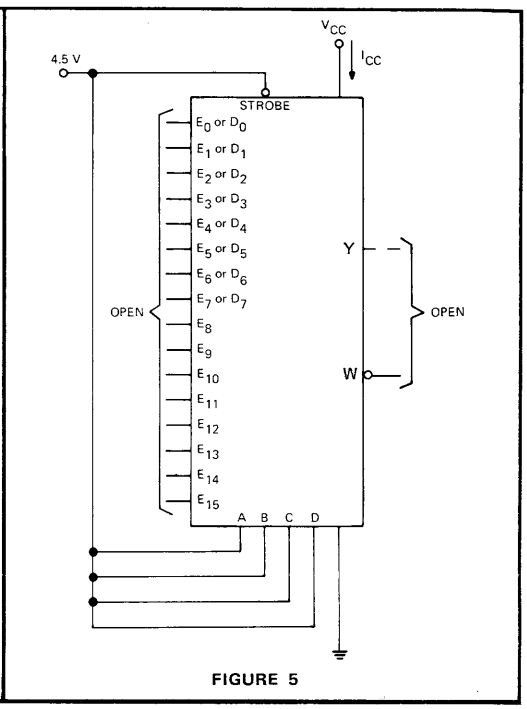


FIGURE 5

† Arrows indicate actual direction of current flow. Tests, as shown are for the SN54150/SN74150. Identical tests as applicable are performed for the SN54151/SN74151 and SN54152/SN74152.

switching characteristics†

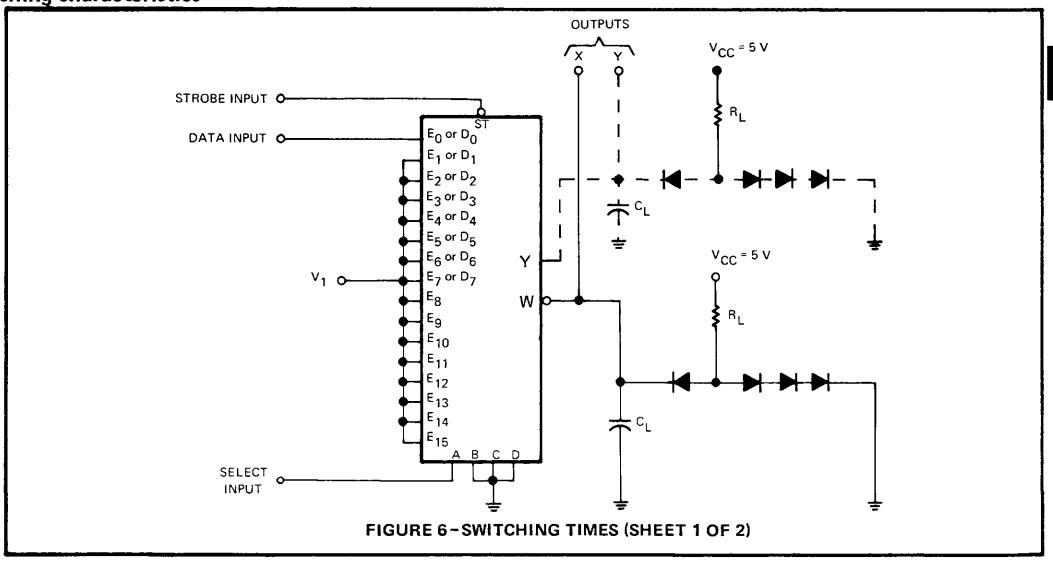
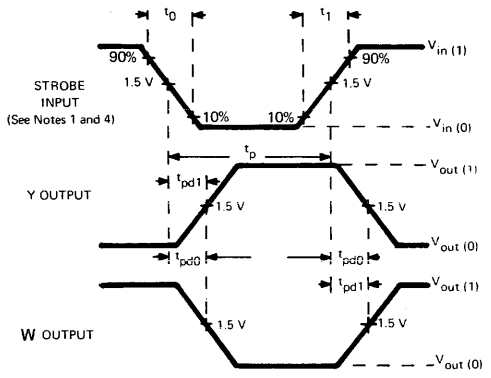


FIGURE 6–SWITCHING TIMES (SHEET 1 OF 2)

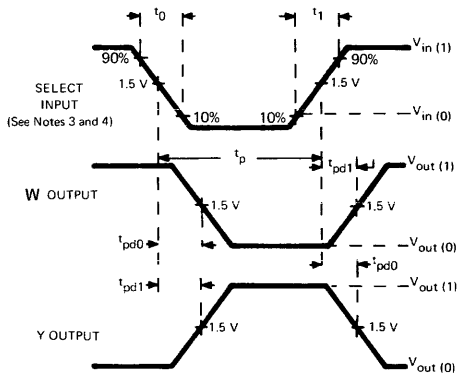
9

PARAMETER MEASUREMENT INFORMATION

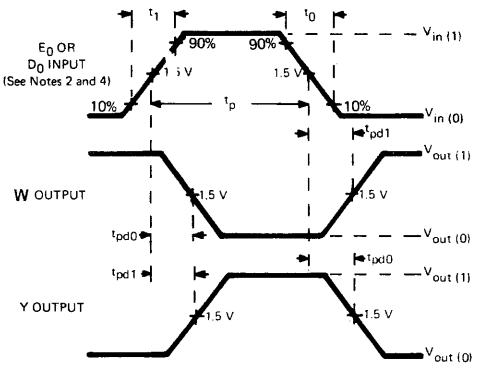
switching characteristics (continued)



STROBE-TO-OUTPUT VOLTAGE WAVEFORMS



SELECT INPUT-TO-OUTPUT VOLTAGE WAVEFORMS



DATA INPUT-TO-OUTPUT VOLTAGE WAVEFORMS

NOTES:
1. When measuring strobe-to-output times select input is at a logical 0, E_0 or D_0 is at a logical 1, V_1 = 4.5 V.
2. When measuring data input-to-output times strobe and select inputs are at a logical 0, and V_1 = 4.5 V.
3. When measuring select input-to-output times strobe input is at a logical 0, data input is at a logical 1, and V_1 = 0.
4. The input pulse has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 10 ns, PRR = 1 MHz, duty cycle = 50%, and generator $Z_{out} \approx 50\ \Omega$.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064.

FIGURE 6–SWITCHING TIMES (SHEET 2 OF 2)

† Tests, as shown, are for the SN54150/SN74150, Identical tests as applicable are performed for the SN54151/SN74151 and SN54152/SN74152.

CIRCUIT TYPES SN54153, SN74153
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

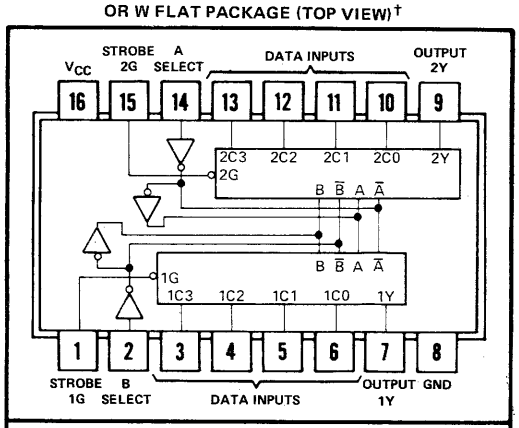
CIRCUIT TYPES SN54153, SN74153
BULLETIN NO. DL-S 7011282, FEBRUARY 1970
REVISED JANUARY 1971

- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- Typical Average Propagation Delay Times:

  Data Input to Output . . . . . 14 ns
  Strobe Input to Output . . . . 17 ns
  Select Input to Output . . . . . 22 ns

- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with most TTL and DTL Circuits

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See truth table

†Pin assigments for these circuits are the same for all packages.

TRUTH TABLE

ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

description

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

These data selectors/multiplexers are fully compatible for use with most TTL and DTL circuits. Each diode-clamped input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs to used inputs. Typical power dissipation is 180 milliwatts.

Resistor values in the OR function have been reduced to values used with Series 54H. This minimizes the capacitive effects of paralleling the phase-splitter transistors and reduces the propagation delay times. The SN54153 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74153 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54153 Circuits . . . . . −55°C to 125°C
SN74153 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54153			SN74153			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.1		V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_{IH}	High-level input current (each input)	3	V_{CC} = MAX, V_I = 2.4 V				40	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (each input)	3	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX	SN54153	−20		−55	mA
				SN74153	−18		−57	
I_{CCL}	Supply current, low-level output	5	V_{CC} = MAX	SN54153		36	52	mA
				SN74153		36	60	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

9

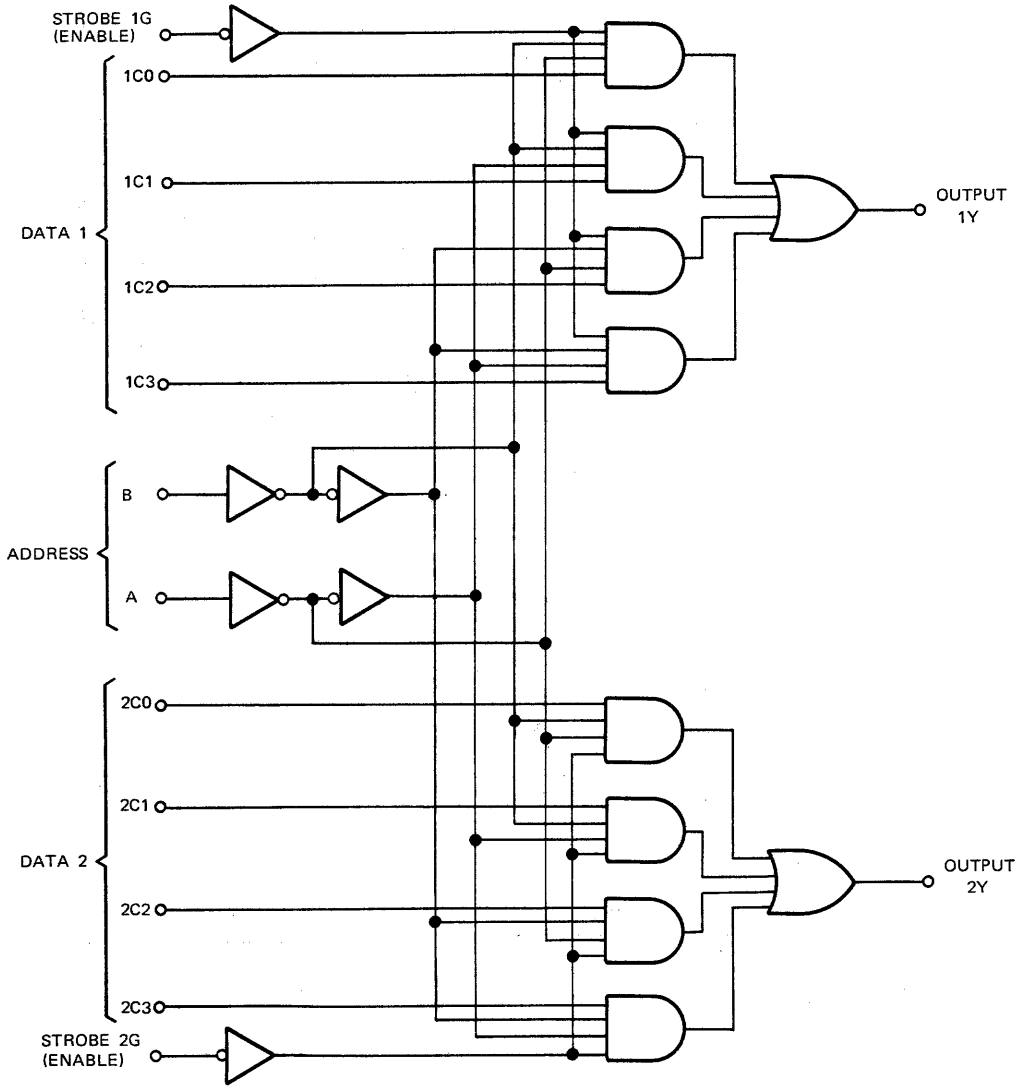
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	6	C_L = 30 pF, R_L = 400 Ω		12	18	ns
t_{PHL}	Data	Y				15	23	ns
t_{PLH}	Address	Y				22	34	ns
t_{PHL}	Address	Y				22	34	ns
t_{PLH}	Strobe	Y				19	30	ns
t_{PHL}	Strobe	Y				15	23	ns

¶t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output.

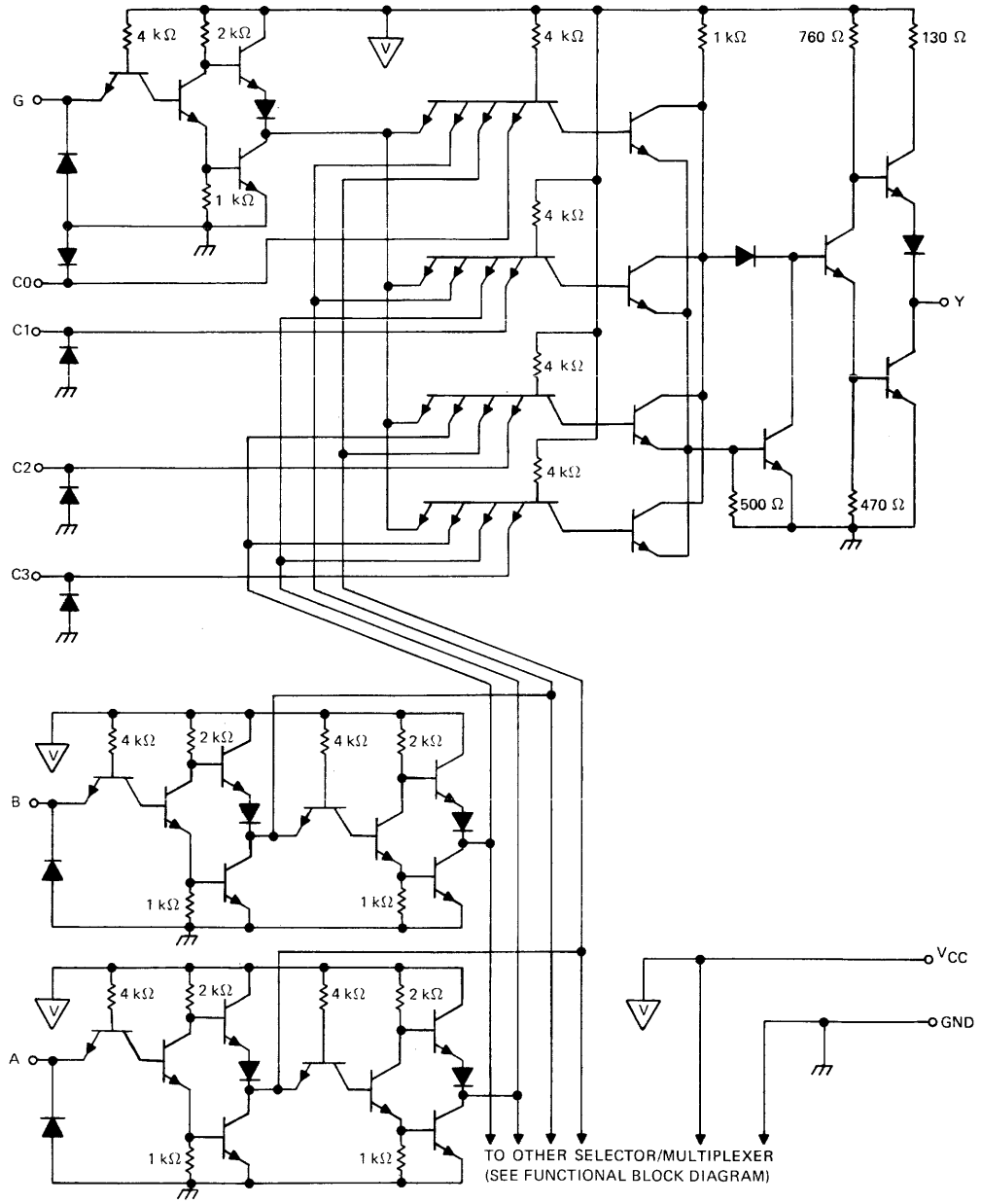
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram



9

schematic (each selector/multiplexer, and the common address section)



NOTE: Component values shown are nominal.

V — $-V_{CC}$ bus

9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

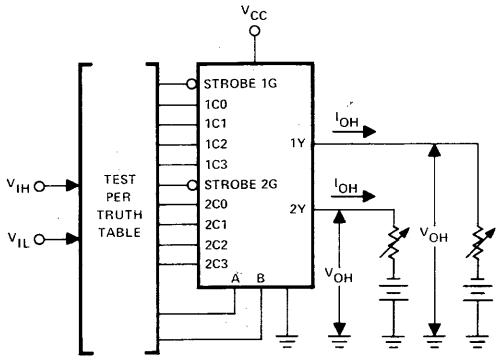


FIGURE 1–V_{IH}, V_{IL}, V_{OH}

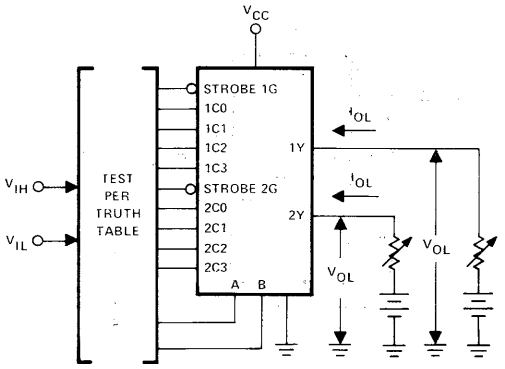
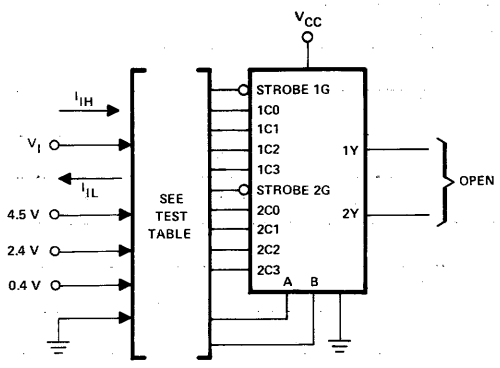


FIGURE 2–V_{IH}, V_{IL}, V_{OL}



TEST TABLE

INPUT CONDITIONS				APPLY V_I	
B	A	1G	2G	TEST I_{IL}	TEST I_{IH}
L	L	H	H		1C3, 2C3
L	H	H	H		1C2, 2C2
H	L	H	H		1C1, 2C1
H	H	H	H		A, B, 1G, 2G, 1C0, 2C0
L	L	L	L	A, B, 1G, 2G, 1C0, 2C0	
L	H	L	L	1C1, 2C1	
H	L	L	L	1C2, 2C2	
H	H	L	L	1C3, 2C3	

H = 2.4 V, L = 0.4 V

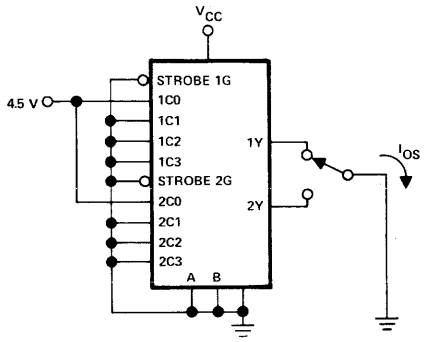
NOTE: Each input is tested separately. When I_{IH} is tested, all C inputs not under test are grounded. When I_{IL} is tested, all C inputs not under test are at 4.5 V.

FIGURE 3 –I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



NOTE: Each output is tested separately.

FIGURE 4 – I_{OS}

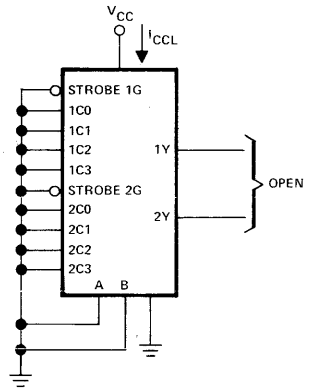


FIGURE 5 – I_{CCL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEST TABLE FOR FIGURE 6

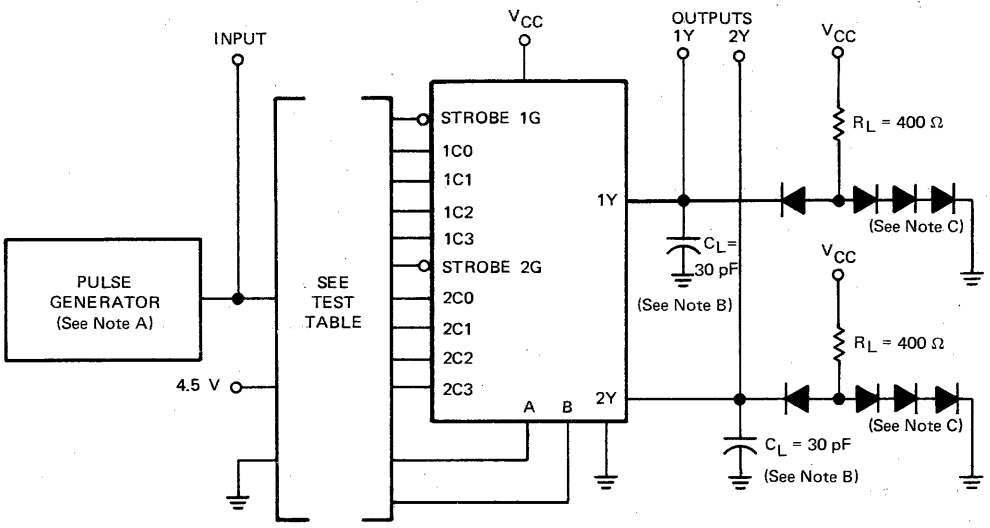
INPUTS							OUTPUT Y WAVEFORM
B	A	C0	C1	C2	C3	G	
GND	GND	INPUT	X	X	X	GND	A
GND	4.5 V	X	INPUT	X	X	GND	A
4.5 V	GND	X	X	INPUT	X	GND	A
4.5 V	4.5 V	X	X	X	INPUT	GND	A
GND	INPUT	GND	4.5 V	X	X	GND	A
INPUT	GND	GND	X	4.5 V	X	GND	A
GND	GND	4.5 V	X	X	X	INPUT	B

X = irrelevant

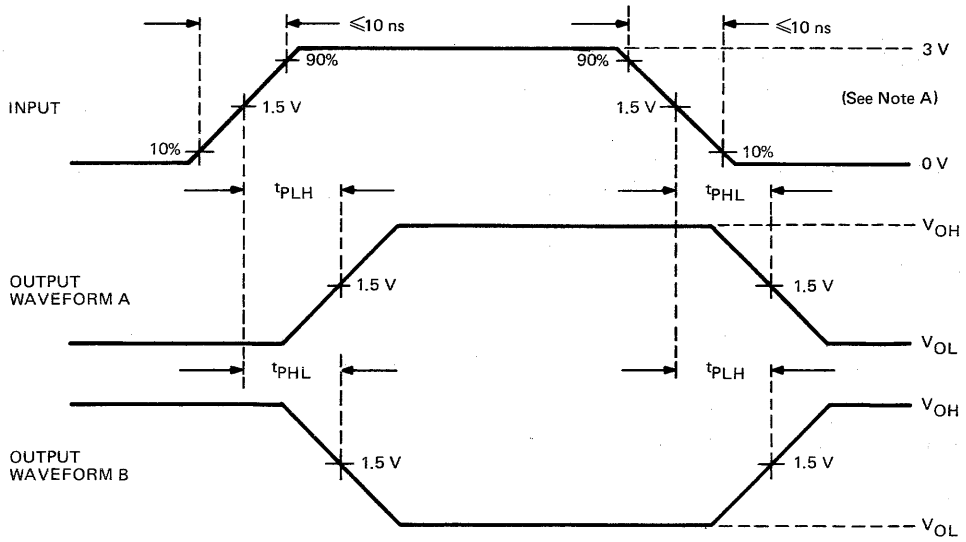
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 6–SWITCHING TIMES

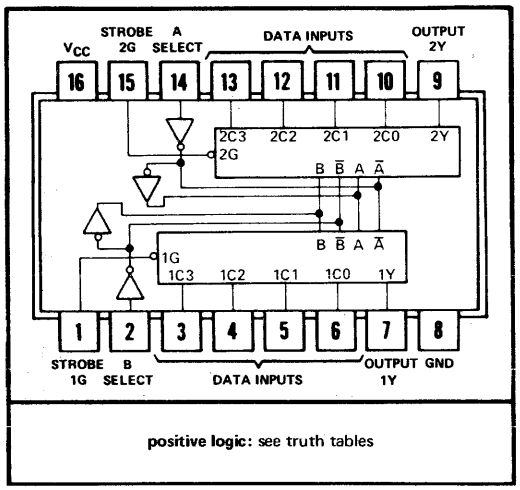
9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54L153, SN74L153
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- Typical Average Propagation Delay Times:
  - Data Input to Output . . . 27 ns
  - Strobe Input to Output . . . 34 ns
  - Select Input to Output . . . 44 ns
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with most TTL and DTL Circuits
- Low Power Dissipation . . . 90 mW Typical

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth tables

description

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate strobe inputs are provided for each of the two four-line sections.

These data selectors/multiplexers are fully compatible for use with most TTL and DTL circuits. Each diode-clamped input represents only one-half of one normalized Series 54/74 load, or approximately five Series 54L/74L gate loads at a low logic level, or two Series 54L/74L gate loads at a high logic level. A fan-out to 5 normalized Series 54/74 loads in the low-level state and 10 in the high-level state is available from each output. Typical power dissipation is 90 milliwatts.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

Resistor values in the OR function have been reduced to minimize the capactive effects of paralleling the phase-splitter transistors and to reduce the propagation delay times. The SN54L153 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L153 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54L153 Circuits . . . . . −55°C to 125°C
SN74L153 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

			SN54L153			SN74L153			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	Series 54L74L gates				40			40	
	Series 54L/74L inputs with 8-kΩ base resistors¶	High logic level			20			20	
		Low logic level			10			10	
Operating free-air temperature T_A			−55		125	0		70	°C

¶This applies for all inputs of circuit types SN54L153 and SN74L153.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_I	Input clamp voltage	3	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA				0.4	V
I_I	Input current at maximum input voltage	3	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current (each input)	3	V_{CC} = MAX, V_I = 2.4 V				20	μA
I_{IL}	Low-level input current (each input)	3	V_{CC} = MAX, V_I = 0.4 V				−0.8	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX	SN54L153	−10		−28	mA
				SN74L153	−9		−30	
I_{CCL}	Supply current, low-level output	5	V_{CC} = MAX	SN54L153			26	mA
				SN74L153		18	30	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

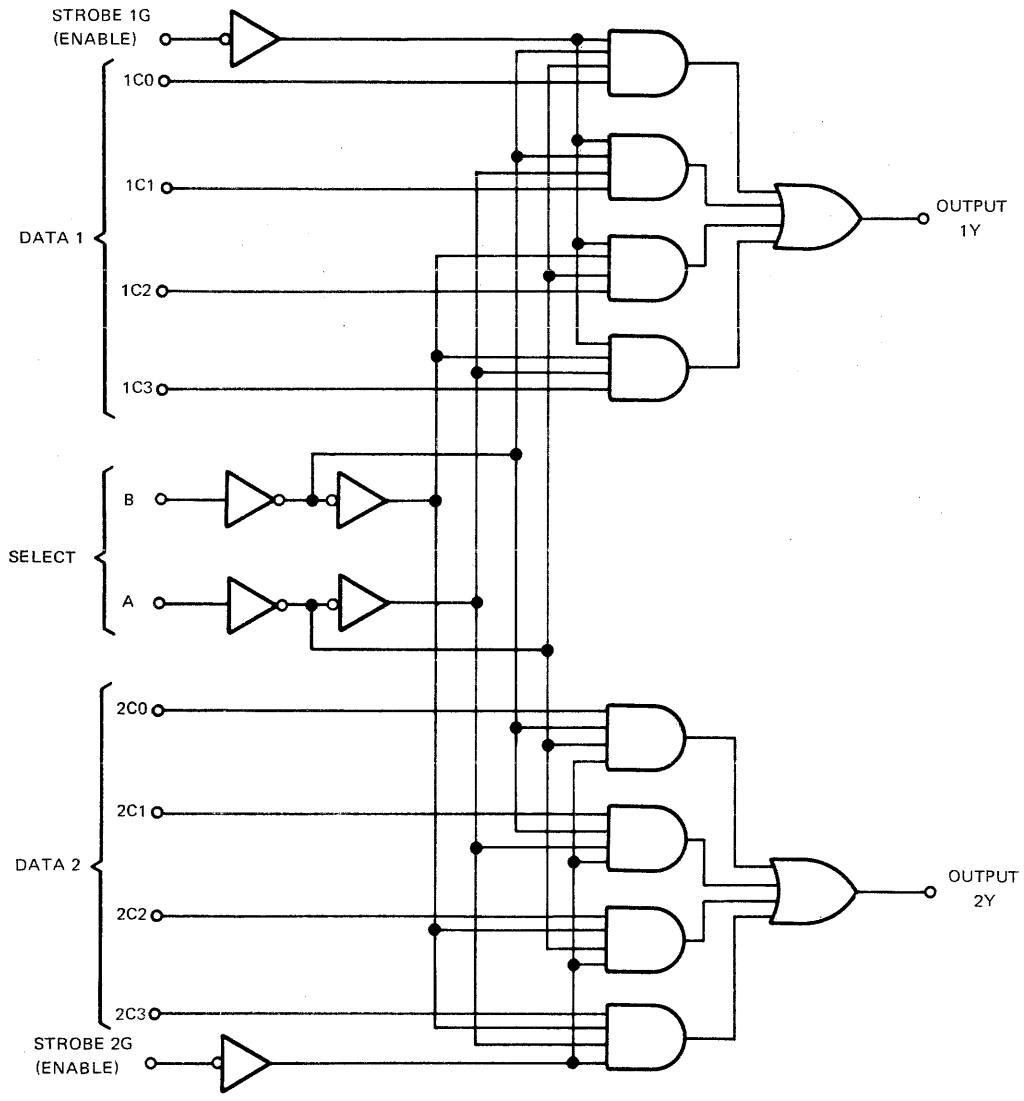
9

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER¶	FROM INPUT	TO OUTPUT	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	6	C_L = 30 pF, R_L = 400 Ω		24	36	ns
t_{PHL}	Data	Y				30	46	ns
t_{PLH}	Select	Y				44	68	ns
t_{PHL}	Select	Y				44	68	ns
t_{PLH}	Strobe	Y				38	60	ns
t_{PHL}	Strobe	Y				30	46	ns

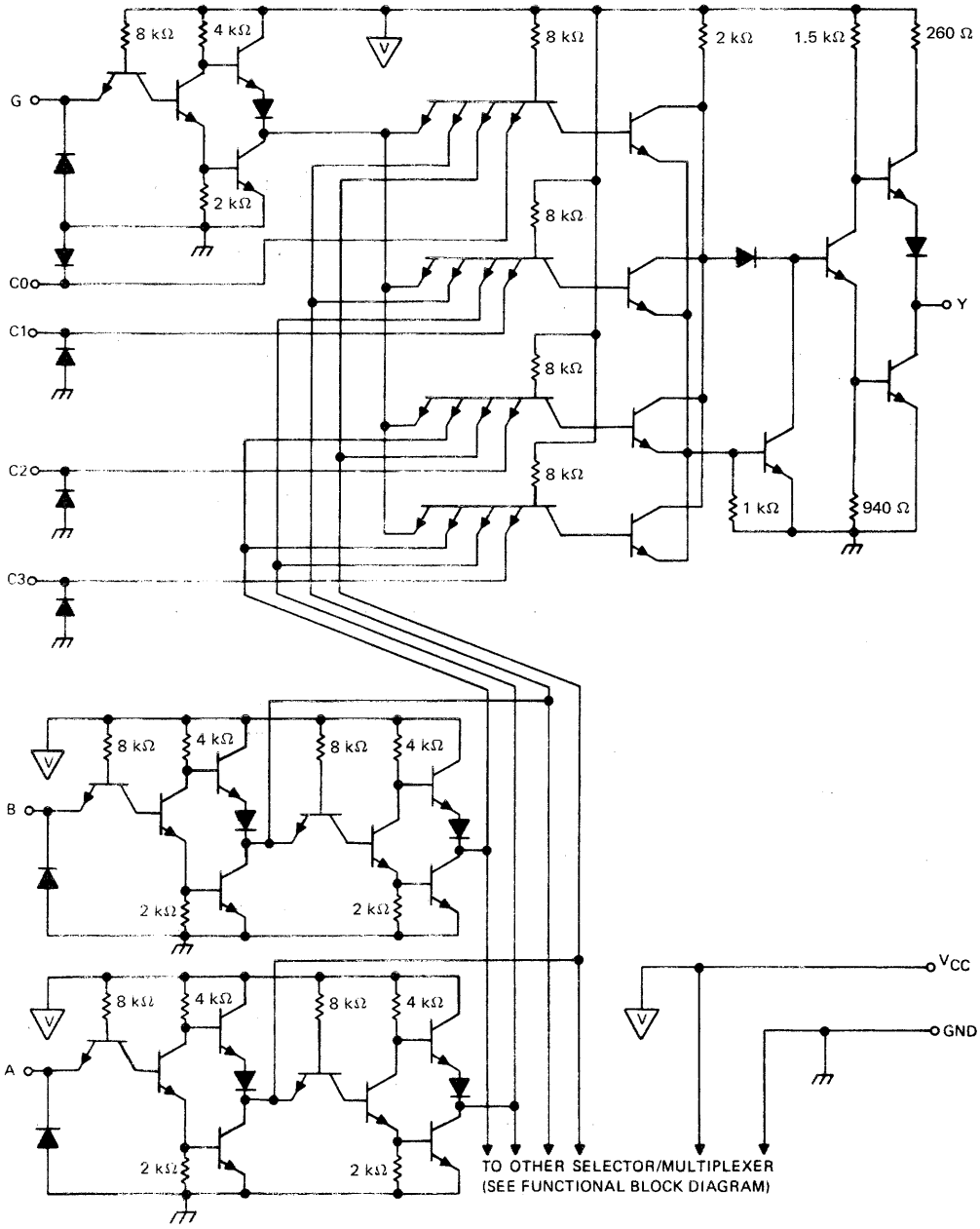
¶t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output.

functional block diagram



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

schematic (each selector/multiplexer, and the common select section)



NOTE: Component values shown are nominal.

▽ . . . V_{CC} bus

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

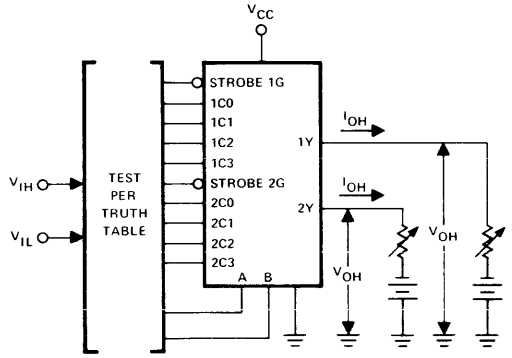


FIGURE 1–V_{IH}, V_{IL}, V_{OH}

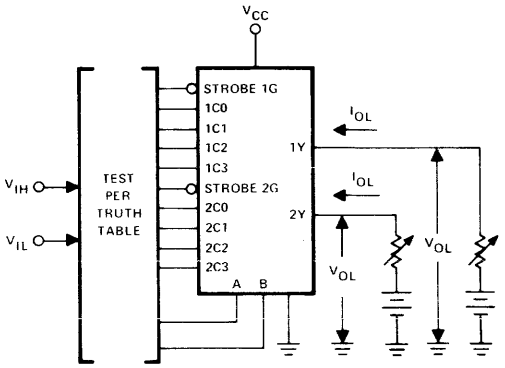
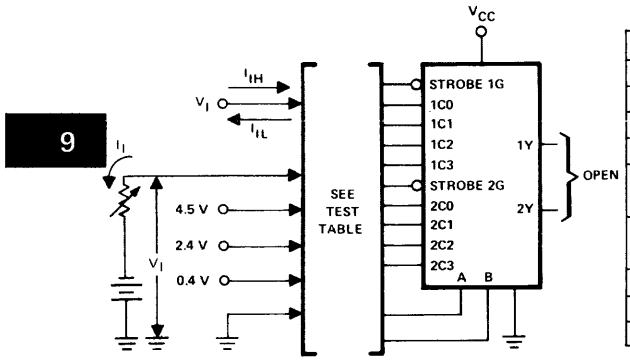


FIGURE 2–V_{IH}, V_{IL}, V_{OL}



TEST TABLE

INPUT CONDITIONS				APPLY I_I	APPLY V_I	
B	A	1G	2G	TEST V_I	TEST I_I, I_{IH}	TEST I_{IL}
L	L	H	H		1C3, 2C3	
L	H	H	H		1C2, 2C2	
H	L	H	H		1C1, 2C1	
H	H	H	H		A, B, 1G, 2G, 1C0, 2C0	
L	L	L	L	A, B, 1G, 2G, 1C0, 2C0		A, B, 1G, 2G, 1C0, 2C0
L	H	L	L	1C1, 2C1		1C1, 2C1
H	L	L	L	1C2, 2C2		1C2, 2C2
H	H	L	L	1C3, 2C3		1C3, 2C3

H = 2.4 V, L = 0.4 V

NOTE: Each input is tested separately. When I_{IH} is tested, all C inputs not under test are grounded. When I_{IL} is tested, all C inputs not under test are at 4.5 V.

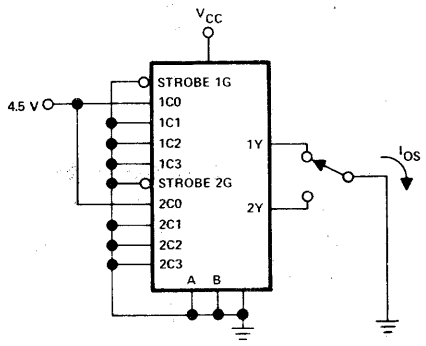
FIGURE 3–V_I, I_I, I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



NOTE: Each output is tested separately.

FIGURE 4 – I_{OS}

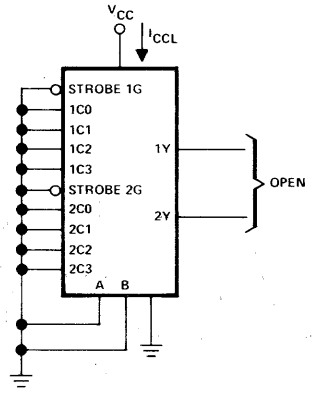


FIGURE 5 – I_{CCL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEST TABLE FOR FIGURE 6

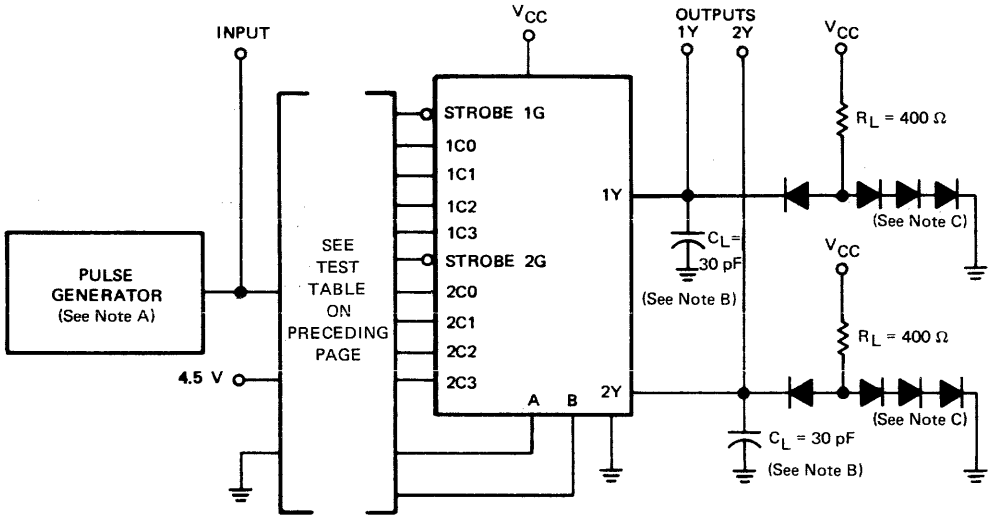
INPUTS							OUTPUT Y WAVEFORM
B	A	C0	C1	C2	C3	G	
GND	GND	INPUT	X	X	X	GND	A
GND	4.5 V	X	INPUT	X	X	GND	A
4.5 V	GND	X	X	INPUT	X	GND	A
4.5 V	4.5 V	X	X	X	INPUT	GND	A
GND	INPUT	GND	4.5 V	X	X	GND	A
INPUT	GND	GND	X	4.5 V	X	GND	A
GND	GND	4.5 V	X	X	X	INPUT	B

X = irrelevant

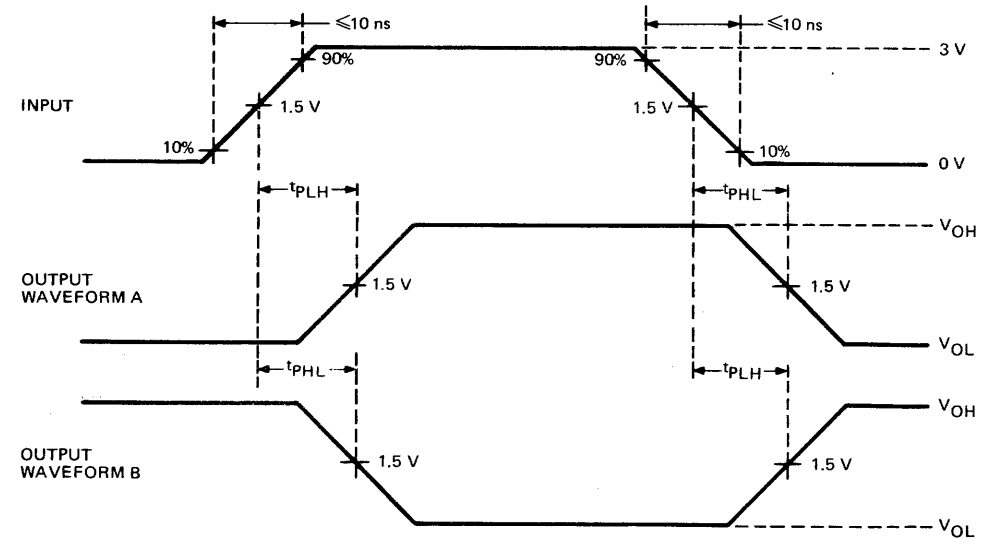
9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR≤ 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N914.

FIGURE 6–SWITCHING TIMES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES TIDM1, TIDM2
BULLETIN NO. DL-S 7111434, JANUARY 1971

MONOLITHIC DIODE MATRICES

For Application As

- Programmable Read-Only Memories
- Alphanumeric Character Generators
- Frequency Generators
- Logic Interface Circuits

For Use In

- CRT Displays
- Minicomputers
- Peripheral Equipment
- Solid-State Memories

description

These monolithic dielectrically isolated diode matrices are fabricated using epitaxial techniques. The desired matrix patterns are programmed by selectively opening the fusible link in series with each diode. This may be done by the user by following the fusing procedure described herein, or custom-programmed matrices may be ordered by sending in a schematic diagram with circles around the diodes to be deleted. Automatic equipment at Texas Instruments can provide instantaneous code-pattern customizing of devices. Only unprogrammed matrices will be symbolized with the type numbers shown in the table below. Circuits custom-programmed to a particular pattern will be assigned a special device number by Texas Instruments, and this number will appear on the device.

Both the high-speed Series TIDM1 and medium-speed Series TIDM2 matrices are available in hermetically sealed metal flat packages (F), ceramic dual-in-line packages (J), or ceramic flat packages (W). See Section 1 for ordering instructions and outline drawings of all packages.

9

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

5 X 5 MATRICES 6 X 6 MATRICES 6 X 8 MATRICES 8 X 5 MATRICES 8 X 6 MATRICES	TIDM155 TIDM166 TIDM168 TIDM185 TIDM186	TIDM255 TIDM266 TIDM268 TIDM285 TIDM286	UNIT
Peak Reverse Voltage (See Note 1)	45	35	V
Steady-State Reverse Voltage, V_R	25		V
Peak Forward Current per Diode at (or below) 25°C Free-Air Temperature (See Note 1)	100		mA
Continuous Power Dissipation at (or below) 25°C Free-Air Temperature (See Notes 2 and 3)	400		mW
Operating Free-Air Temperature Range	−65 to 150		°C
Storage Temperature Range	−65 to 200		°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	300		°C

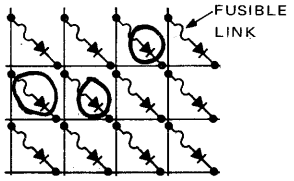
NOTES: 1. These values apply for 100-μs pulses, duty cycle ⩽ 20%.
2. The values shown for total device apply for any combination provided the ratings of individual diodes are not exceeded.
3. Derate linearly to 150°C free-air temperature at the rate of 3.2 mW/°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

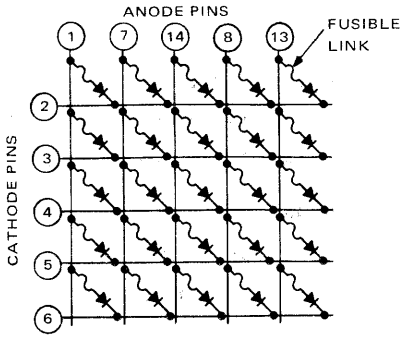
SERIES TIDM1, TIDM2
DIODE MATRICES

CUSTOMIZED CIRCUITS

To order custom programmed circuits, circle the diodes to be elimated in the appropriate schematic as shown in the example below.

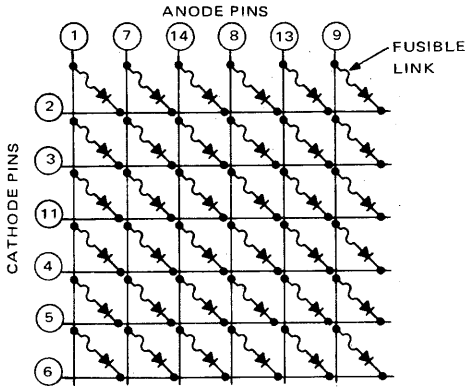


TIDM155, TIDM255 5 X 5 MATRICES



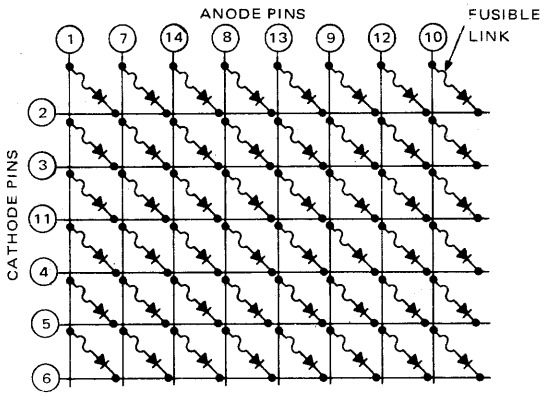
9 10 11 12 Make no external connection

TIDM166, TIDM266 6 X 6 MATRICES

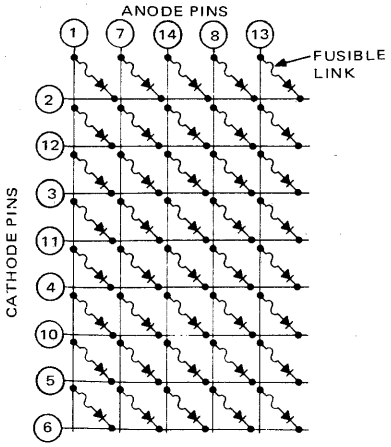


9 10 12 Make no external connection

TIDM168, TIDM268 6 X 8 MATRICES

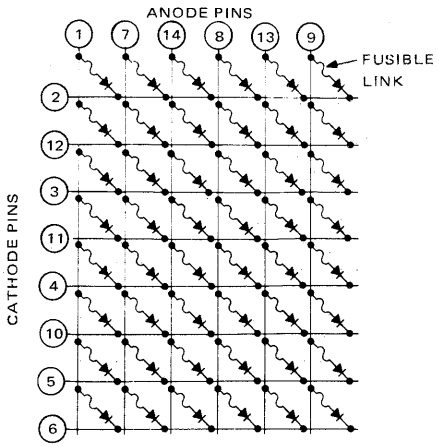


TIDM185, TIDM285 8 X 5 MATRICES



9 Make no external connection

TIDM186, TIDM286 8 X 6 MATRICES



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

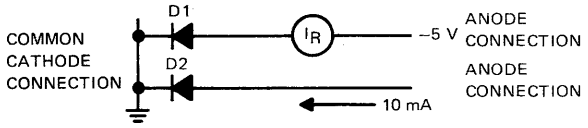
electrical characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	SERIES TIDM1			SERIES TIDM2			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)}$	Reverse Breakdown Voltage	I_R = 100 μA	45			35			V
I_R	Static Reverse Current	V_R = 25 V			20			50	nA
I_R	Static Reverse Current (with Adjacent Diode Conducting)	See Figure 1		20			50		nA
V_F	Static Forward Voltage	I_F = 1 mA			0.8			0.9	V
		I_F = 20 mA			1.5			1.7	
C_T	Total Capacitance between Any Anode Terminal and Any Cathode Terminal	V_R = 5 V, f = 1 MHz			4			4	pF

switching characteristics at 25°C free-air temperature

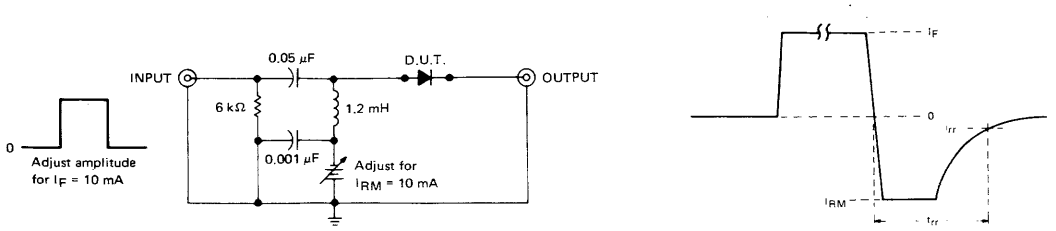
PARAMETER		TEST CONDITIONS	SERIES TIDM1			SERIES TIDM2			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{rr}	Reverse Recovery Time	I_F = 10 mA, I_{RM} = 10 mA, R_L = 100 Ω, i_{rr} = 1 mA, See Figure 2			10			25	ns

PARAMETER MEASUREMENT INFORMATION



NOTE: D1 and D2 are any two adjacent diodes with a common cathode connection.

FIGURE 1



INPUT VOLTAGE WAVEFORM | TEST CIRCUIT | OUTPUT CURRENT WAVEFORM

FIGURE 2–REVERSE RECOVERY TIME

NOTES: a. The input pulse is supplied by a generator with the following characteristics: $t_f \leq 1$ ns, Z_{out} = 50 Ω, t_w = 200 ns, duty cycle ≤ 1%.

b. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq 0.4$ ns, R_{in} = 50 Ω.

FUSING PROCEDURE

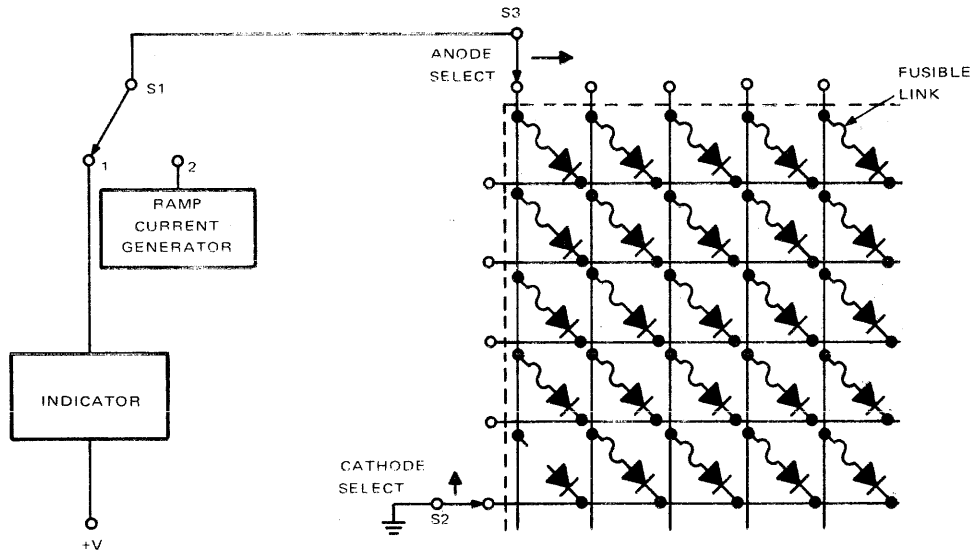


FIGURE 3

A ramp current generator provides the fusing current. The diode to be eliminated is selected by setting switches S2 and S3. When S1 is activated to position 2, current through the fusible link opens the link in series with the selected diode. The peak fusing current required to open a fusible link is approximately 750 milliamperes. Switch S1 in position 1 gives a visual indication of the condition of the selected diode before and after fusing.

TYPICAL CHARACTERISTICS

9

REVERSE CURRENT
vs
FREE-AIR TEMPERATURE

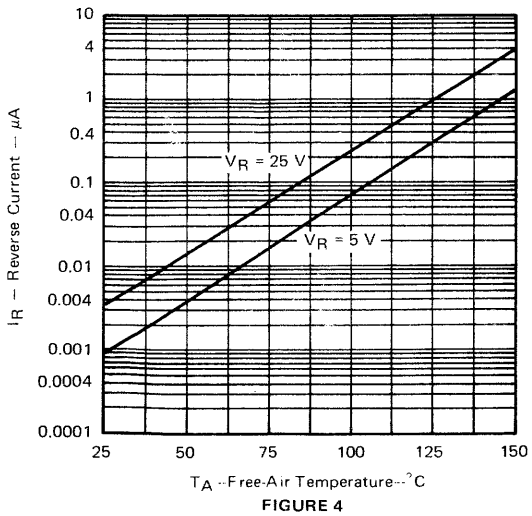


FIGURE 4

FORWARD CONDUCTION CHARACTERISTICS

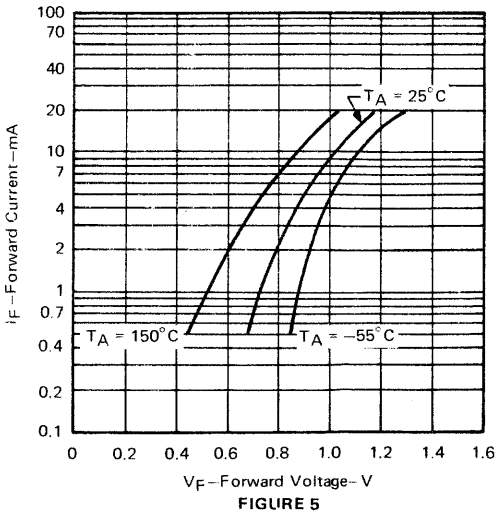


FIGURE 5

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Radiation Hardened Circuits

10

Series RSN 54L Radiation Hardened Low Power TTL Now Available

RSN54L00 – Quadruple 2-Input Positive-NAND Gate
RSN54L10 – Triple 3-Input Positive-NAND Gate
RSN54L20 – Dual 4-Input Positive-NAND Gate
RSN54L57 – 3-3-3-2 AND-OR-INVERT Gate
RSN54L71 – R-S Master-Slave Flip-Flop
RSN54L72 – J-K Master-Slave Flip-Flop
RSN54L74 – Dual D-Type Edge-Triggered Flip-Flop
RSN54L122 – Retriggerable Monostable Multivibrator with Clear
RSN54L130 – Dual 3-Input Positive-NAND Gate
RSN54L131 – Dual Expandable 3-Input Positive-NAND Gate

Also Available From Texas Instruments:

Radiation Hardened Series 54, Series 54H, Linear Circuits And Diode Arrays.

INDEX

RSN SERIES
RADIATION-HARDENED INTEGRATED CIRCUITS

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES RSN54 AND SERIES RSN54H
RADIATION-HARDENED TTL INTEGRATED CIRCUITS

TTL INTEGRATED CIRCUITS WITH HIGH TOLERANCE TO GAMMA AND NEUTRON IRRADIATION

- High Speed: Typical Gate Propagation Delay Times (C_L = 50 pF):
  Series RSN54 . . . 10 ns
  Series RSN54H . . . 7.5 ns
- High D-C Noise Margin . . . 1 Volt Typical
- Low Output Impedance Provides Low A-C Noise Susceptibility
- Waveform Integrity Maintained over Full Range of Loading and Temperature Conditions
- Normalized Fan-Out to Ten Loads
- Typical NAND Gate Power Dissipation at 50% Duty Cycle:
  Series RSN54 . . . 10 mW
  Series RSN54H . . . 23 mW

description

Series RSN54 and Series RSN54H TTL integrated circuits are specifically designed and fabricated for operation and survivability in nuclear-radiation environments. The basic Series 54/74 configuration, desirable for its "natural" hardness, has been coupled with a state-of-the-art circuit-hardening process. This technology, compatible for use in high-volume production, employs:

- dielectric isolation
- thin-film resistors
- small transistor geometries
- shallow base diffusions
- heavy gold doping
- minimum collector thickness and resistivity
- aluminum interconnection system

Series RSN54, RSN54H, and RSN54L logic families are completely compatible with one another and with most other TTL and DTL circuits. These circuits are designed to operate at the same supply voltages and logic levels with the high d-c noise margins which are characteristic of Texas Instruments Series 54/74 circuits. These families of radiation-hardened circuits include the gates and flip-flops needed to perform functions within present-day digital electronic systems. And, since these three families are compatible with one another, Series RSN54H high-speed circuits may be selectively used in system locations requiring minimal propagation delay times. In other locations where speed is not the limiting parameter, Series RSN54 or RSN54L circuits may be used.

Both Series RSN54 and Series RSN54H are designed for operation over the full military temperature range of −55°C to 125°C.

10

CONTENTS

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)	7 V
Input voltage (See Note 1)	5.5 V
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

input-current requirements

Input-current requirements reflect worst-case conditions for T_A = −55°C to 125°C and V_{CC} = 4.5 V to 5.5 V. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

a. Each input of the Series RSN54 multiple-emitter input transistors requires no more than a 1.6-mA flow out of the input at a low voltage level; therefore one normalized load (N = 1) is −1.6 mA maximum. Each input requires current into the input at a high voltage level. This current is 40 μA maximum (one normalized load) for each emitter input.

b. Each input of the Series RSN54H multiple-emitter input transistors requires no more than a 2-mA flow out of the input at a low voltage level; therefore, one normalized load (N = 1) is −2 mA maximum. Each input requires current into the input at a high voltage level. This current is 50 μA maximum (one normalized load) for each emitter input.

fan-out capability

Fan-out (N) reflects the ability of an output to sink current from a number of Series RSN54 or RSN54H loads at a low voltage level and to supply current at a high voltage level. Each output is capable of sinking current or supplying current to 10 normalized loads (N = 10) within the same series. In addition, Series RSN54H outputs will drive twelve Series RSN54 loads, or Series RSN54 outputs will drive eight Series RSN54H loads. Currents out of the output terminal are specified as negative values.

unused inputs

10

For optimum switching times and minimum noise susceptibility, unused inputs should be maintained at a positive voltage greater than 2.4 V but not to exceed the absolute maximum rating of 5.5 V. This eliminates the distributed capacitance associated with the floating-input-transistor emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between 2.4 V and 3.5 V.

b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each input presents a full load to the driving output at a high-level voltage but adds no loading at a low-level voltage.

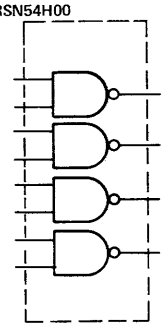
c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One-to-25 unused inputs may be connected to each 1-kΩ resistor.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

standard line summary

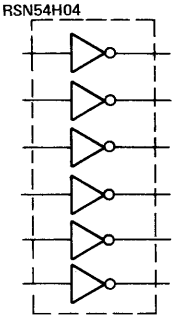
GATE CIRCUITS

RSN5400
RSN54H00



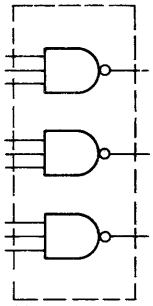
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

RSN5404
RSN54H04



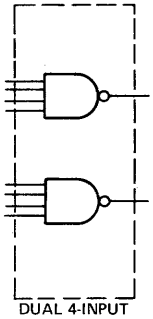
HEX INVERTERS

RSN5410
RSN54H10



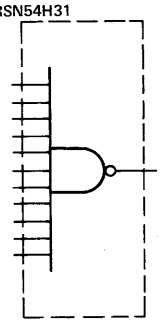
TRIPLE 3-INPUT
POSITIVE-NAND GATES

RSN5420
RSN54H20



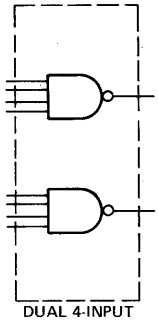
DUAL 4-INPUT
POSITIVE-NAND GATES

RSN5431
RSN54H31



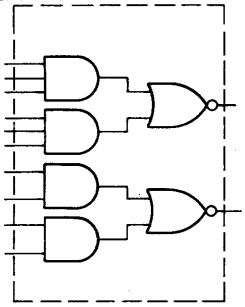
11-INPUT
POSITIVE-NAND GATES

RSN5440
RSN54H40



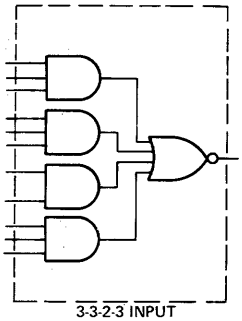
DUAL 4-INPUT
POSITIVE-NAND BUFFERS

RSN5456
RSN54H56



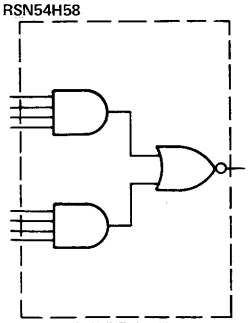
2-WIDE 3-INPUT,
2-WIDE 2-INPUT, DUAL
AND-OR-INVERT GATES

RSN5457
RSN54H57



3-3-2-3 INPUT
AND-OR-INVERT GATES

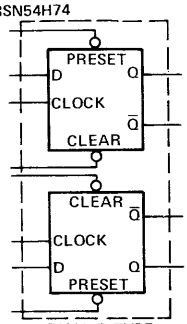
RSN5458
RSN54H58



2-WIDE 4 INPUT
AND-OR-INVERT GATES

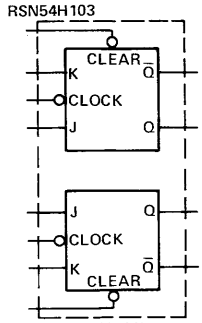
FLIP-FLOP CIRCUITS

RSN5474
RSN54H74



DUAL D-TYPE
EDGE-TRIGGERED FLIP-FLOPS

RSN54H103

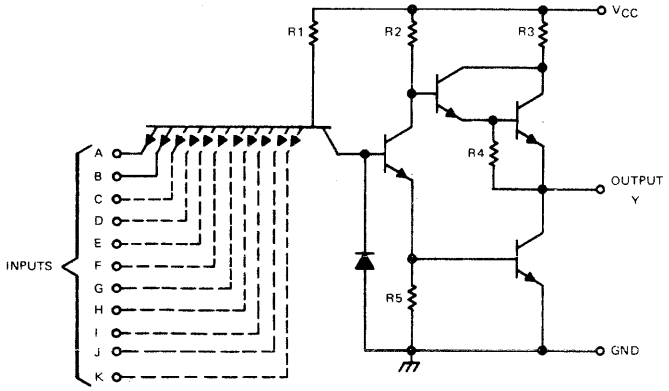


DUAL J-K
EDGE-TRIGGERED FLIP-FLOP

10

CIRCUIT TYPES RSN5400, RSN5410, RSN5420, RSN5431, RSN54H00, RSN54H10, RSN54H20, RSN54H31
POSITIVE-NAND GATES

schematic (each NAND gate)



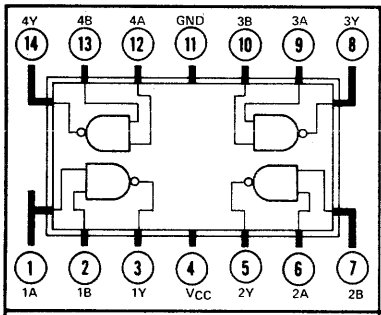
NOMINAL RESISTOR VALUES

RESISTOR	RSN5400 RSN5410 RSN5420 RSN5431	RSN54H00 RSN54H10 RSN54H20 RSN54H31
R1	4 kΩ	2.8 kΩ
R2	1.6 kΩ	760 Ω
R3	58 Ω	58 Ω
R4	1 kΩ	1 kΩ
R5	1 kΩ	470 Ω

logic

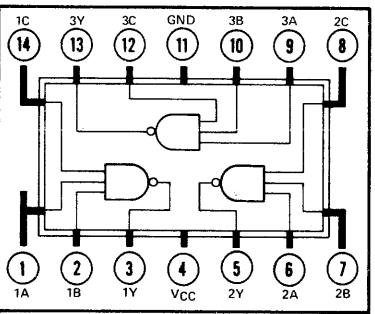
H FLAT PACKAGE (TOP VIEWS)

RSN5400, RSN54H00



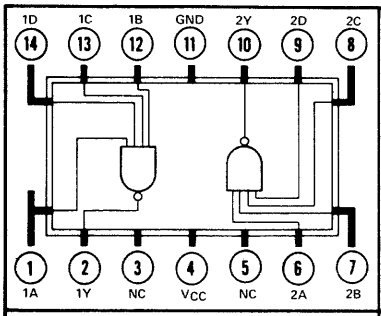
positive logic: $Y = \overline{AB}$

RSN5410, RSN54H10



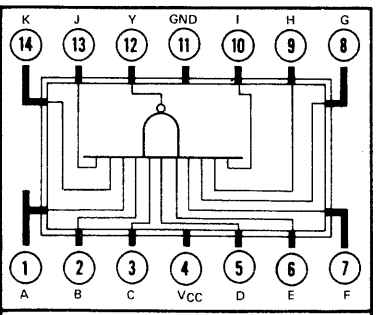
positive logic: $Y = \overline{ABC}$

RSN5420, RSN54H20



positive logic: $Y = \overline{ABCD}$

RSN5431, RSN54H31



positive logic: $Y = \overline{ABCDEFGHIJK}$

NC—No internal connection

10

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

	RSN5400 RSN5410 RSN5420 RSN5431			RSN54H00 RSN54H10 RSN54H20 RSN54H31			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Normalized fan-out from each gate, N			10			10	
High-level output current, I_{OH}			−400			−500	μA
Low-level output current, I_{OL}			16			20	mA
Operating free-air temperature, T_A	−55		125	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	RSN5400 RSN5410 RSN5420 RSN5431		RSN54H00 RSN54H10 RSN54H20 RSN54H31		UNIT
				MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage	1		2		2		V
V_{IL}	Low-level input voltage	2			0.8		0.8	V
V_{OH}	High-level output voltage	2	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = MAX	2.4		2.4		V
V_{OL}	Low-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX		0.4		0.4	V
I_I	Input current at maximum input voltage	3	V_{CC} = MAX, V_I = 5.5 V		1		1	mA
I_{IH}	High-level input current	3	V_{CC} = MAX, V_I = 2.4 V		40		50	μA
I_{IL}	Low-level input current	4	V_{CC} = MAX, V_I = 0.4 V		−1.6		−2	mA
I_{OS}	Short-circuit output current‡	5	V_{CC} = MAX	−40	−120	−40	−120	mA
I_{CCH}	Supply current, high-level output (average per gate)	6	V_{CC} = MAX, V_I = 0		1.75		2.5	mA
I_{CCL}	Supply current, low-level output (average per gate)	6	V_{CC} = MAX, V_I = 4.5 V		5.7		10.8	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Not more than one output should be shorted at a time, and the duration of the short circuit test should not exceed one second.

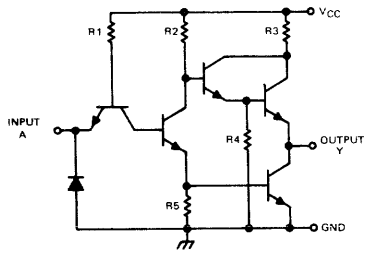
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	RSN5400 RSN5410 RSN5420		RSN5431		RSN54H00 RSN54H10 RSN54H20		RSN54H31		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	29	C_L = 50 pF		18		18		12		12	ns
t_{PHL}	Propagation delay time, high-to-low-level output	29	C_L = 50 pF		15		25		12		20	ns

10

CIRCUIT TYPES RSN5404, RSN54H04
HEX INVERTERS

schematic (each inverter)

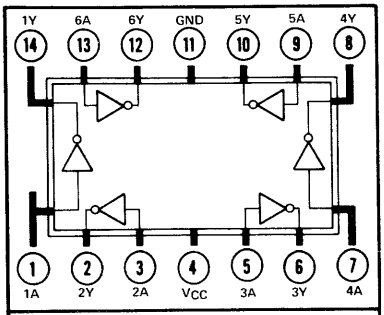


NOMINAL RESISTOR VALUES

RESISTOR	RSN5404	RSN54H04
R1	4 kΩ	2.8 kΩ
R2	1.6 kΩ	850 Ω
R3	58 Ω	58 Ω
R4	4 kΩ	4 kΩ
R5	1 kΩ	500 Ω

logic

H FLAT PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A}$

recommended operating conditions

	RSN5404			RSN54H04			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Normalized fan-out from each output, N			10			10	
High-level output current, I_{OH}			−400			−500	μA
Low-level output current, I_{OL}			16			20	mA
Operating free-air temperature, T_A	−55		125	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	RSN5404		RSN54H04		UNIT
				MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage	7		2		2		V
V_{IL}	Low-level input voltage	8			0.8		0.8	V
V_{OH}	High-level output voltage	8	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = MAX	2.4		2.4		V
V_{OL}	Low-level output voltage	7	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX		0.4		0.4	V
I_I	Input current at maximum input voltage	9	V_{CC} = MAX, V_I = 5.5 V		1		1	mA
I_{IH}	High-level input current	9	V_{CC} = MAX, V_I = 2.4 V		40		50	μA
I_{IL}	Low-level input current	10	V_{CC} = MAX, V_I = 0.4 V		−1.6		−2	mA
I_{OS}	Short-circuit output current‡	11	V_{CC} = MAX	−40	−120	−40	−120	mA
I_{CCH}	Supply current, high-level output (average per inverter)	12	V_{CC} = MAX, V_I = 0		3.2		3.8	mA
I_{CCL}	Supply current, low-level output (average per inverter)	12	V_{CC} = MAX, V_I = 4.5 V		5.6		9.7	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time, and the duration of the short-circuit test should not exceed one second.

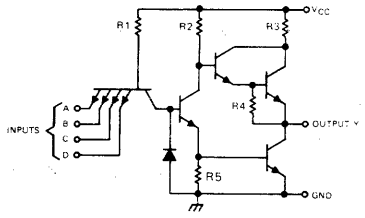
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	RSN5404		RSN54H04		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	29	C_L = 50 pF		18		12	ns
t_{PHL}	Propagation delay time, high-to-low-level output	29	C_L = 50 pF		15		12	ns

10

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

schematic (each NAND buffer)

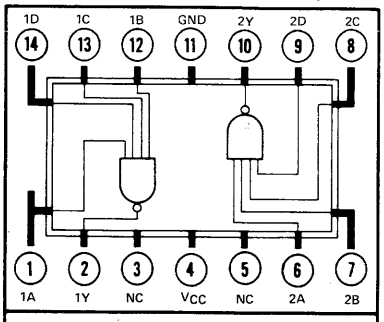


NOMINAL RESISTOR VALUES

RESISTOR	RSN5440	RSN54H40
R1	4 kΩ	1.4 kΩ
R2	600 Ω	390 Ω
R3	45 Ω	45 Ω
R4	1 kΩ	1 kΩ
R5	400 Ω	250 Ω

logic

H FLAT PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCD}$

NC—No internal connection

recommended operating conditions

	RSN5440			RSN54H40			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Normalized fan-out from each gate, N			30			30	
High-level output current, I_{OH}			−1.5			−3	mA
Low-level output current, I_{OL}			48			60	mA
Operating free-air temperature, T_A	−55		125	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	RSN5440		RSN54H40		UNIT
				MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage	1		2		2		V
V_{IL}	Low-level input voltage	2			0.8		0.8	V
V_{OH}	High-level output voltage	2	V_{CC} = MIN, V_{OL} = 0.8 V, I_{OH} = MAX	2.4		2.4		V
V_{OL}	Low-level output voltage	1	V_{CC} = MIN, V_{OH} = 2 V, I_{OL} = MAX		0.4		0.4	V
I_I	Input current at maximum input voltage	3	V_{CC} = MAX, V_I = 5.5 V		1		1	mA
I_{IH}	High-level input current	3	V_{CC} = MAX, V_I = 2.4 V		50		100	μA
I_{IL}	Low-level input current	4	V_{CC} = MAX, V_I = 0.4 V		−1.6		−4	mA
I_{OS}	Short-circuit output current‡	5	V_{CC} = MAX	−40	−125	−40	−125	mA
I_{CCH}	Supply current, high-level output (average per gate)	6	V_{CC} = MAX, V_I = 0		1.75		5	mA
I_{CCL}	Supply current, low-level output (average per gate)	6	V_{CC} = MAX, V_I = 4.5 V		12.6		21	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time, and the duration of the short-circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

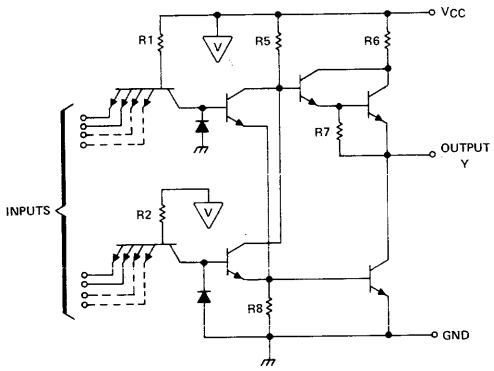
PARAMETER		TEST FIGURE	TEST CONDITIONS	RSN5440		RSN54H40		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	29	C_L = 50 pF		18		12	ns
t_{PHL}	Propagation delay time, high-to-low-level output	29	C_L = 50 pF		15		12	ns

10

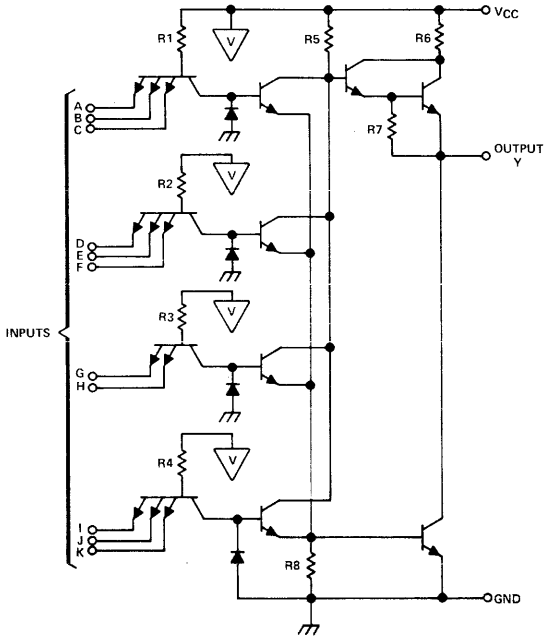
CIRCUIT TYPES RSN5456, RSN5457, RSN5458, RSN54H56, RSN54H57, RSN54H58 POSITIVE AND-OR-INVERT GATES

schematics

RSN5456, RSN5458,
RSN54H56, RSN54H58



RSN5457, RSN54H57



NOMINAL RESISTOR VALUES

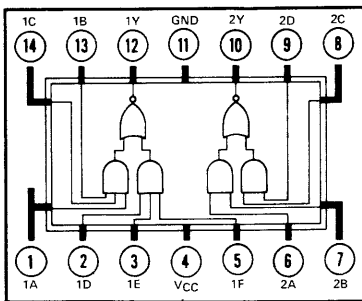
RESISTOR	RSN5456 RSN5457 RSN5458	RSN54H56 RSN54H57 RSN54H58
R1, R2, R3, R4,	4 kΩ	2.8 kΩ
R5	1.6 kΩ	760 Ω
R6	58 Ω	58 Ω
R7	1 kΩ	1 kΩ
R8	1 kΩ	470 Ω

V ... V_{CC} bus

logic

H FLAT PACKAGE (TOP VIEWS)

RSN5456, RSN54H56

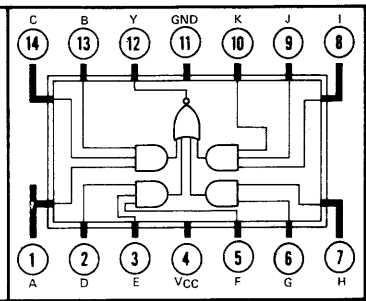


positive logic:

$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$

$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$

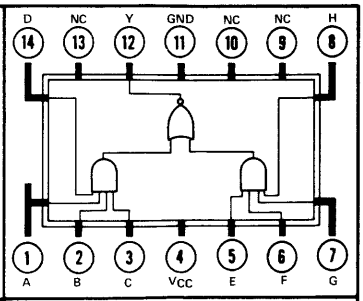
RSN5457, RSN54H57



positive logic:

$Y = \overline{(ABC) + (DEF) + (GH) + (IJK)}$

RSN5458, RSN54H58



positive logic:

$Y = \overline{(ABCD) + (EFGH)}$

NC—No internal connection

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

	SERIES RSN54			SERIES RSN54H			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Normalized fan-out from each output, N			10			10	
High-level output current, I_{OH}			−400			−500	μA
Low-level output current, I_{OL}			16			20	mA
Operating free-air temperature, T_A	−55		125	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES RSN54		SERIES RSN54H		UNIT
					MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage	13			2		2		V
V_{IL}	Low-level input voltage	14				0.8		0.8	V
V_{OH}	High-level output voltage	14	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = MAX		2.4		2.4		V
V_{OL}	Low-level output voltage	13	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX			0.4		0.4	V
I_I	Input current at maximum input voltage	15	V_{CC} = MAX, V_I = 5.5 V			1		1	mA
I_{IH}	High-level input current	15	V_{CC} = MAX, V_I = 2.4 V			40		50	μA
I_{IL}	Low-level input current	16	V_{CC} = MAX, V_I = 0.4 V			−1.6		−2	mA
I_{OS}	Short-circuit output current‡	17	V_{CC} = MAX		−40	−120	−40	−120	mA
I_{CCH}	Supply current, high-level output	18	V_{CC} = MAX, V_I = 0	RSN5456		7			mA
				RSN5457		7			
				RSN5458		3.5			
				RSN54H56				10	
				RSN54H57				10	
				RSN54H58				5	
I_{CCL}	Supply current, low-level output	18	V_{CC} = MAX, V_I = 4.5 V	RSN5456		14			mA
				RSN5457		10			
				RSN5458		7			
				RSN54H56				25	
				RSN54H57				16	
				RSN54H58				13	

10

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

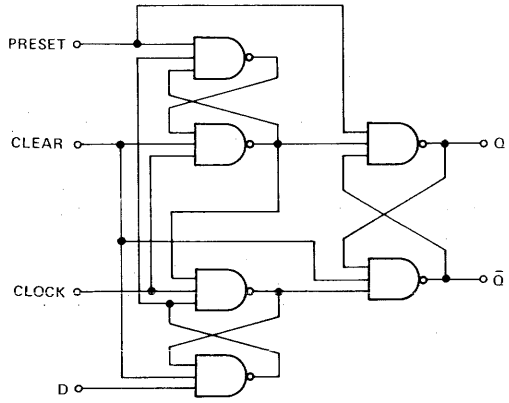
‡Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	SERIES RSN54		SERIES RSN54H		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	29	C_L = 50 pF		20		15	ns
t_{PHL}	Propagation delay time high-to-low-level output	29	C_L = 50 pF		15		12	ns

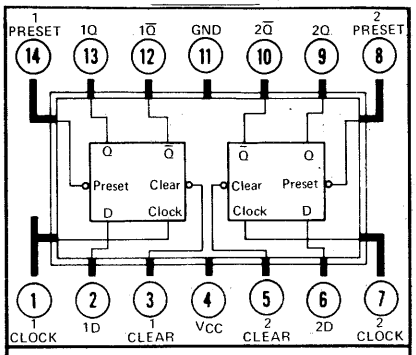
CIRCUIT TYPES RSN5474, RSN54H74
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

functional block diagram (each flip-flop)



logic

H FLAT PACKAGE (TOP VIEW)



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

TRUTH TABLE
(Each Flip-Flop)

t_n	t_{n+1}	
INPUT	OUTPUT	
D	Q	Q̄
L	L	H
H	H	L

H = high level, L = low level
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

description

These monolithic, high-speed, dual, edge-triggered flip-flops utilize TTL circuitry to perform D-type flip-flop logic. Each flip-flop has inc vidual clear and preset inputs, and also complementary Q and Q̄ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

recommended operating conditions

	RSN5474			RSN54H74			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Normalized fan-out from each output, N			10			10	
High-level output current, I_{OH}			−400			−500	μA
Low-level output current, I_{OL}	0		16	0		20	mA
Clock frequency, f_{clock}			20			30	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 30 or 31)	30			20			ns
Width of preset pulse, $t_{w(preset)}$ (see Figure 32)	30			20			ns
Width of clear pulse, $t_{w(clear)}$ (see Figure 32)	30			20			ns
Input setup time, t_{setup} (see Note 1 and Figures 30 and 31)	20			15			ns
Input hold time, t_{hold} (see Note 2 and Figures 30 and 31)	5			0			ns
Operating free-air temperature, T_A	−55		125	−55		125	°C

NOTES: 1. Setup time is the interval immediately preceding the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†	RSN5474 MIN	RSN5474 MAX	RSN54H74 MIN	RSN54H74 MAX	UNIT
V_{IH}	High-level input voltage		19 and 20		2		2		V
V_{IL}	Low-level input voltage		19 and 20			0.8		0.8	V
V_{OH}	High-level output voltage		19	V_{CC} = MIN, I_{OH} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	2.4		2.4		V
V_{OL}	Low-level output voltage		20	V_{CC} = MIN I_{OL} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V		0.4		0.4	V
I_I	Input current at maximum input voltage		21	V_{CC} = MAX, V_I = 5.5 V		1		1	mA
I_{IH}	High-level input current	D input	21	V_{CC} = MAX, V_I = 2.4 V		40		50	μA
		preset or clock				80		100	
		clear				120		150	
I_{IL}	Low-level input current	preset or D	21	V_{CC} = MAX, V_I = 0.4 V		−1.6		−2	mA
		clock or clear				−3.2		−4	
I_{OS}	Short-circuit output current‡		22	V_{CC} = MAX	−40	−120	−40	−120	mA
I_{CC}	Supply current		23	V_{CC} = 5 V,		28		45	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

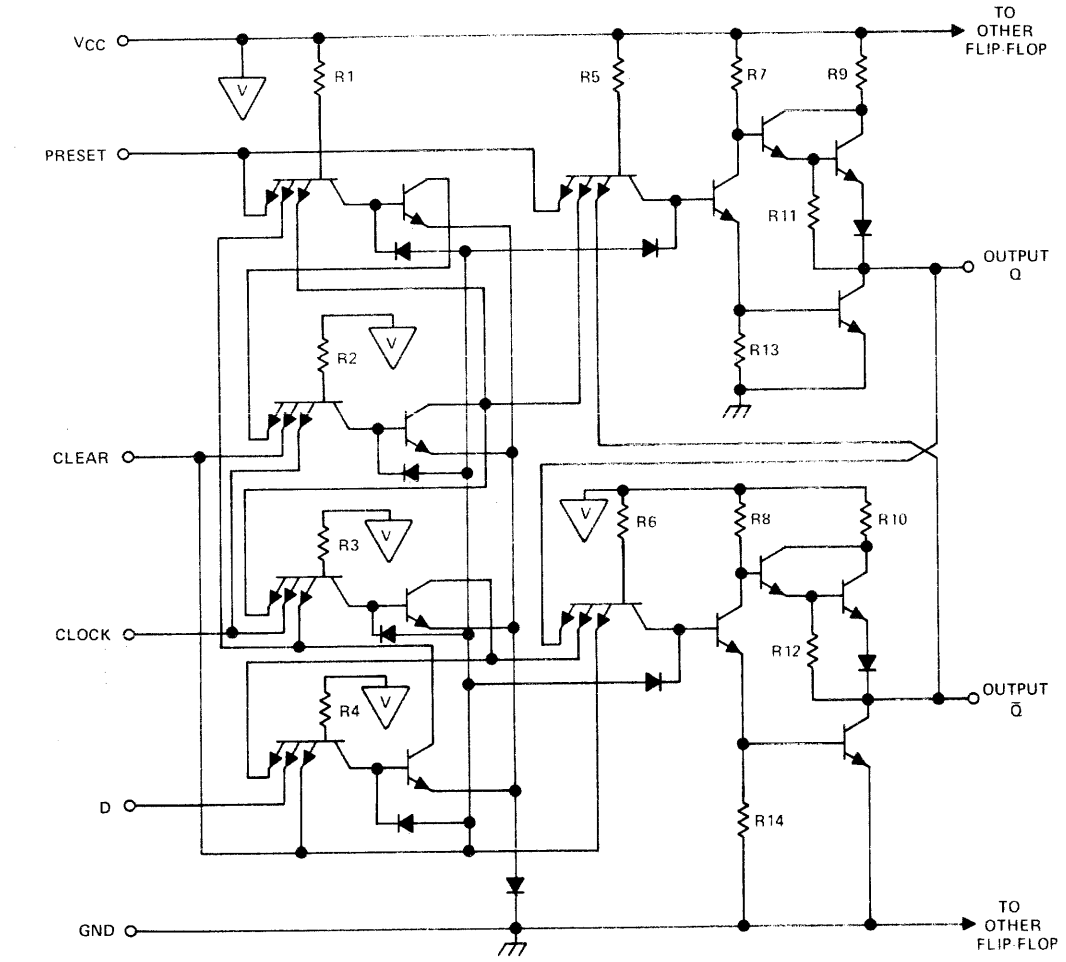
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	RSN5474 MIN	RSN5474 MAX	RSN54H74 MIN	RSN54H74 MAX	UNIT
f_{max}	Maximum clock frequency	30 and 31	C_L = 50 pF	20		30		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear or preset	32	C_L = 50 pF		25		20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear or preset	32	C_L = 50 pF		35		30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock	30 and 31	C_L = 50 pF		25		20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock	30 and 31	C_L = 50 pF		30		25	ns

10

CIRCUIT TYPES RSN5474, RSN54H74
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

schematic (each flip-flop)



▽ . . . V_{CC} bus

NOMINAL RESISTOR VALUES

RESISTOR	RSN5474	RSN54H74
R1,R2,R3,R4,R5,R6	4 kΩ	2.8 kΩ
R7,R8,	1.6 kΩ	760 Ω
R9,R10	58 Ω	58 Ω
R11,R12	1 kΩ	1 kΩ
R13,R14	1 kΩ	470 Ω

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

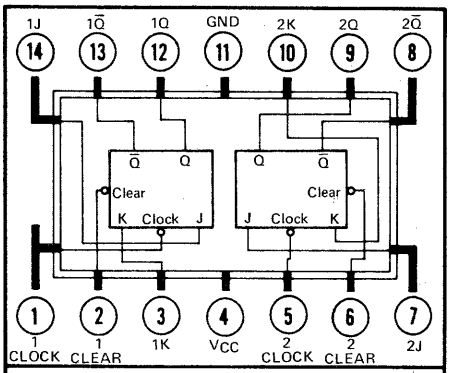
logic

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

H = high level, L = low level
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

H FLAT PACKAGE (TOP VIEW)



asynchronous input:
Low input to clear resets Q to low level.
Clear is independent of clock.

description

These monolithic J-K flip-flops are negative-edge triggered. The inputs are inhibited while the clock input is low; when the clock goes high the inputs are enabled and data will be accepted. The logic levels of the J and K inputs may be allowed to change when the clock input is high and the truth table will be observed as long as the minimum set-up times are maintained. Input data is transferred to the outputs on the negative edge of the clock pulse. A low input to clear resets Q to the low logic level independently of the clock.

recommended operating conditions

		RSN54H103			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	V
Normalized fan-out from each output, N				10	
High-level output current, I_{OH}				−500	μA
Low-level output current, I_{OL}				20	mA
Clock frequency, f_{clock}		0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 33)		15			ns
Width of clear pulse, $t_{w(clear)}$ (see Figure 34)		15			ns
Input setup time, t_{setup} (see Note 1 and Figure 33)	High-level data	10			ns
	Low-level data	15			
Input hold time, t_{hold} (see Note 2 and Figure 33)		0			ns
High-to-low-level transition time of clock pulse, $t_{THL(clock)}$				150	ns
Operating free-air-temperature, T_A		−55		125	°C

NOTES: 1. Setup time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

10

CIRCUIT TYPE RSN54H103
DUAL J-K EDGE-TRIGGERED FLIP-FLOP

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†	RSN54H103 MIN	RSN54H103 MAX	UNIT
V_{IH}	High-level input voltage		24 and 25		2		V
V_{IL}	Low-level input voltage		24 and 25			0.8	V
V_{OH}	High-level output voltage		24	V_{CC} = MIN, I_{OH} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	2.4		V
V_{OL}	Low-level output voltage		25	V_{CC} = MIN, I_{OL} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V		0.4	V
I_I	Input current at maximum input voltage		26	V_{CC} = MAX, V_I = 5.5 V		1	mA
I_{IH}	High-level input current	J or K input	26	V_{CC} = MAX, V_I = 2.4 V		50	μA
		clock or clear				100	
I_{IL}	Low-level input current	J or K input	26	V_{CC} = MAX, V_I = 0.4 V		−2	mA
		clock or clear				−4	
I_{OS}	Short-circuit output current‡		27	V_{CC} = MAX	−40	−100	mA
I_{CC}	Supply current		28	V_{CC} = MAX		52	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡No more than one output should be shorted at a time, and duration of the short-circuit test should not exceedone second. Only the $\overline{Q}$ outputs are tested.

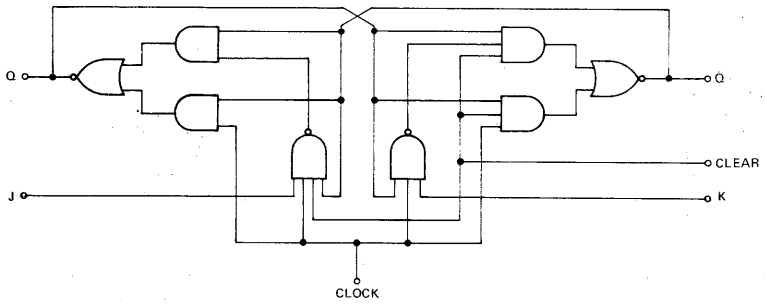
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	RSN54H103 MIN	RSN54H103 MAX	UNIT
f_{max}	Maximum clock frequency	33	C_L = 50 pF, R_L = 280 Ω	25		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear to $\overline{Q}$	34	C_L = 50 pF, R_L = 280 Ω		15	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear to Q	34	C_L = 50 pF, R_L = 280 Ω		15	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock	33	C_L = 50 pF, R_L = 280 Ω		15	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock	33	C_L = 50 pF, R_L = 280 Ω		15	ns

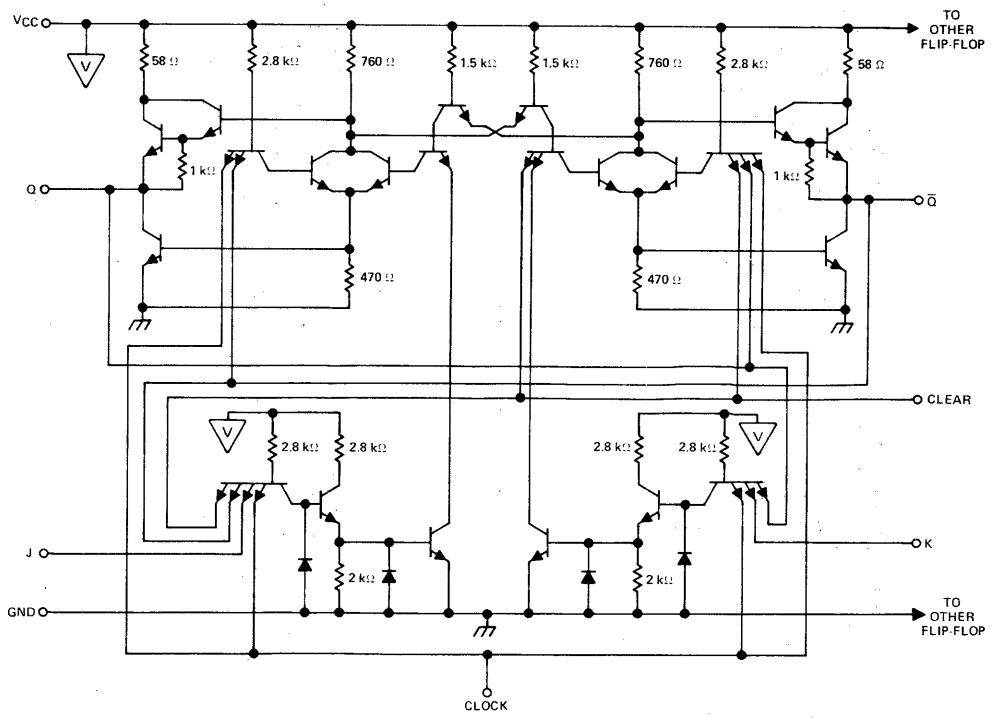
10

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram (each flip-flop)



schematic (each flip-flop)

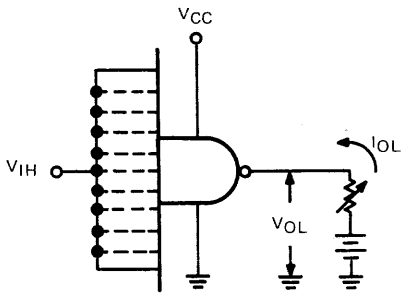


▽ . . . V_{CC} bus
Resistor values shown are nominal.

10

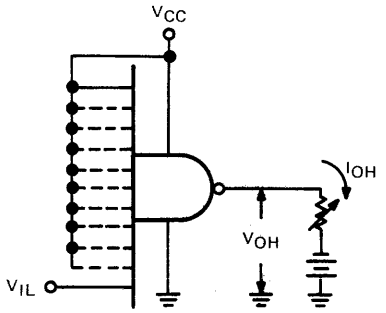
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶



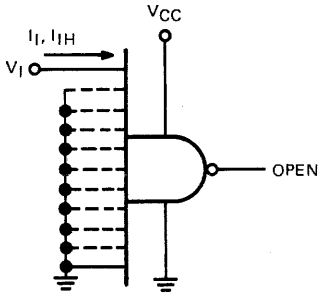
All inputs are tested simultaneously.

FIGURE 1–V_{IH}, V_{OL}



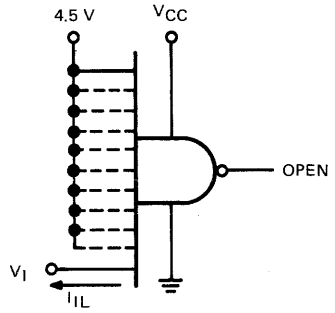
Each input is tested separately.

FIGURE 2–V_{IL}, V_{OH}



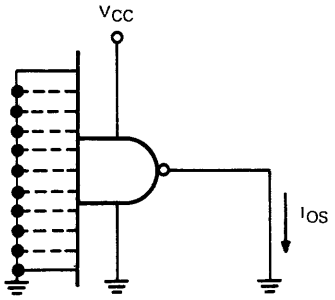
Each input is tested separately.

FIGURE 3–I_I, I_{IH}



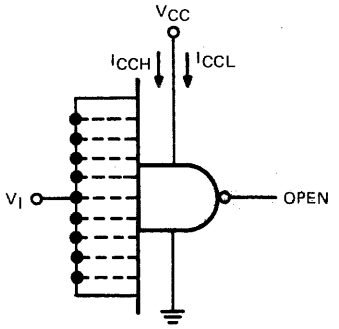
Each input is tested separately.

FIGURE 4–I_{IL}



Each gate is tested separately.

FIGURE 5–I_{OS}



All gates are tested simultaneously. Average-per-gate value = $\frac{I_{CC}\ \text{total}}{\text{number of gates in package}}$.

FIGURE 6–I_{CCH}, I_{CCL}

¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

10

PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶ (continued)

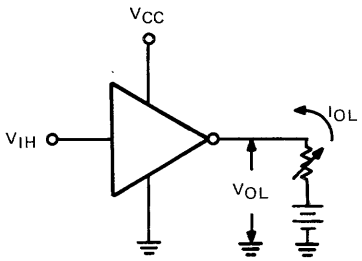


FIGURE 7–V_{IH}, V_{OL}

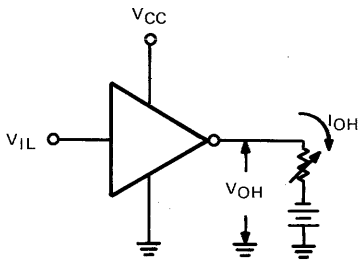


FIGURE 8–V_{IL}, V_{OH}

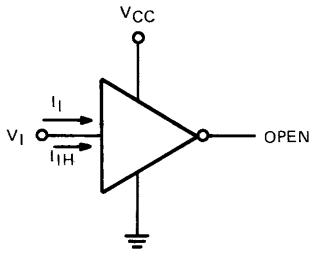


FIGURE 9–I_I, I_{IH}

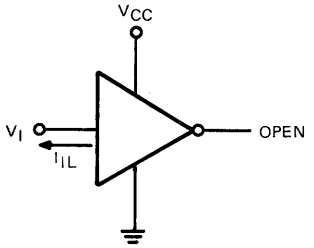
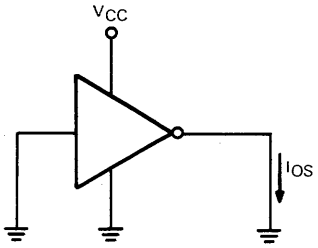
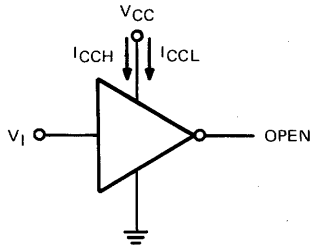


FIGURE 10–I_{IL}



Each inverter is tested separately.

FIGURE 11–I_{OS}



All inverters are tested simultaneously. Average-per-inverter value = $\frac{I_{CC\ total}}{\text{number of inverters in package}}$

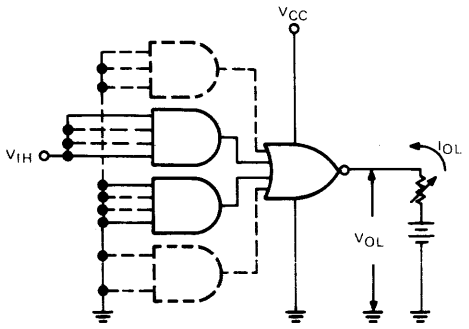
FIGURE 12–I_{CCH}, I_{CCL}

¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

10

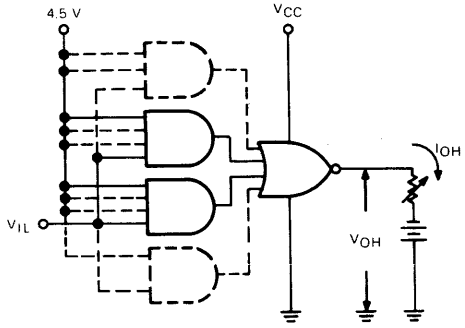
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶ (continued)



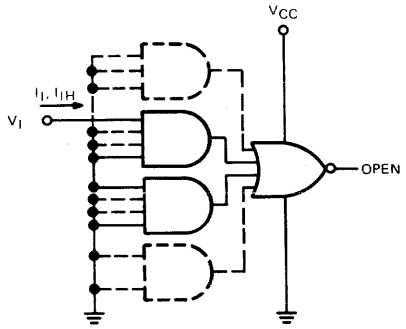
Each AND section is tested separately.

FIGURE 13–V_{IH}, V_{OL}



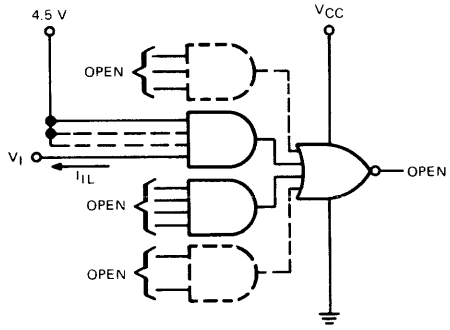
Each set of inputs is tested separately. A set comprises one input from each AND section.

FIGURE 14–V_{IL}, V_{OH}



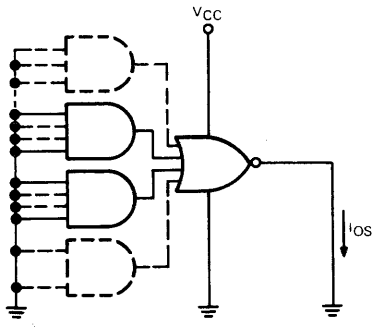
Each input is tested separately.

FIGURE 15–I_I, I_{IH}



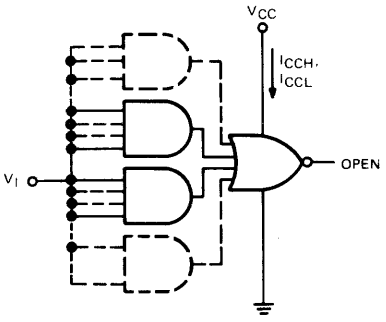
Each input is tested separately.

FIGURE 16–I_{IL}



Each output is tested separately.

FIGURE 17–I_{OS}



All gates are tested simultaneously. Average per-gate value = $\frac{I_{CC}\ \text{total}}{\text{number of AOI gates in package}}$.

FIGURE 18–I_{CCH}, I_{CCL}

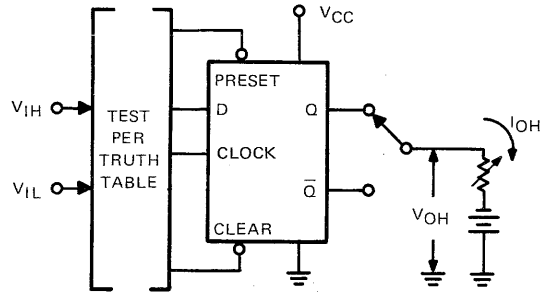
¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.
Dashed lines represent gates and/or inputs and outputs which are applicable to only some of the circuit types which reference these test circuits.

10

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

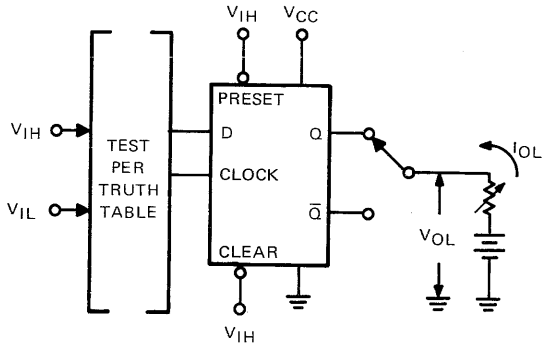
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶ (continued)



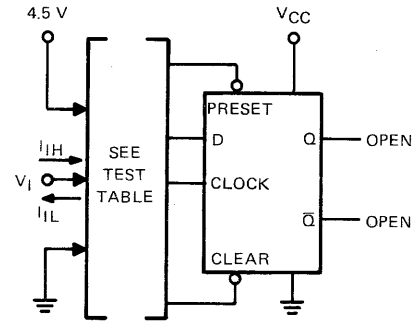
A. Each flip-flop is tested separately.
B. Each output is tested separately.
C. V_{OH} is also tested using clear and preset inputs.

FIGURE 19–V_{IH}, V_{IL}, V_{OH}



A. Each flip-flop is tested separately.
B. Each output is tested separately.

FIGURE 20–V_{IH}, V_{IL}, V_{OL}

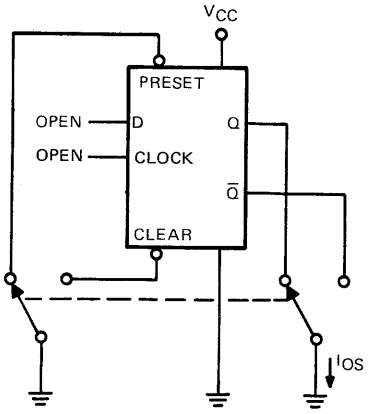


TEST TABLE

APPLY V_I MEASURE	CONDITIONS ON OTHER INPUTS FOR I_I, I_{IH}		CONDITIONS ON OTHER INPUTS FOR I_{IL}	
I_I, I_{IH}, I_{IL}	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND
Clock	Clear and D	Preset	Clear	Preset and D
Clock	Preset and D	Clear		
Preset	Clear and D	Clock (See Note B)	Clear	Clock and D
Clear	Preset	D and Clock (See Note B)	Clock, D, and Preset	None
Clear			D	Preset and Clock
D	Clock and Preset	Clear	Clock and Clear	Preset

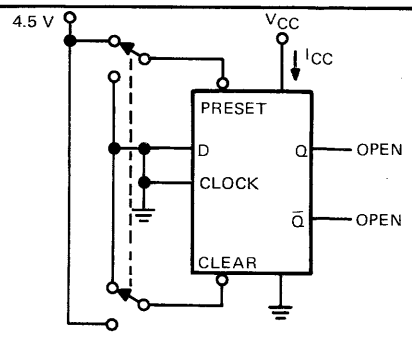
NOTES: A. Each input of each flip-flop is tested separately.
B. GND is momentarily applied to clock, then 4.5 V.

FIGURE 21–I_{IH}, I_{IL}



Each output is tested separately.

FIGURE 22–I_{OS}



I_{CC} is measured simultaneously for both flip-flops with D, clock, and preset at ground; then with D, clock, and clear at ground.

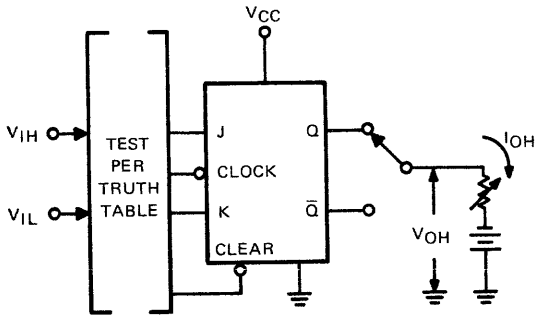
FIGURE 23–I_{CC}

¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

10

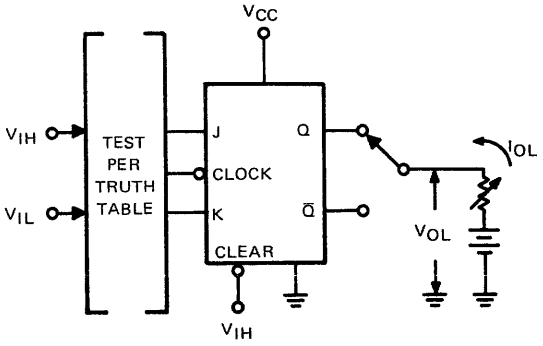
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶ (continued)



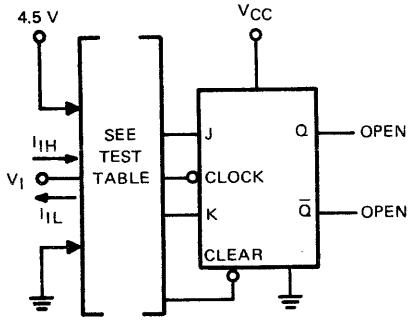
NOTES: A. Each flip-flop is tested separately.
B. Each output is tested separately.
C. V_{OH} at the $\overline{Q}$ output is also tested using the clear input.

FIGURE 24–V_{IH}, V_{IL}, V_{OH}



NOTES: A. Each flip-flop is tested separately.
B. Each output is tested separately.

FIGURE 25–V_{IH}, V_{IL}, V_{OL}



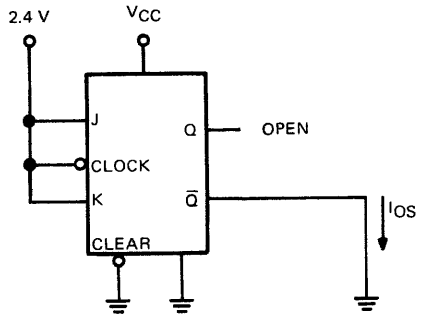
TEST TABLE

APPLY V_I, MEASURE I_{IH} OR I_{IL}	CONDITIONS ON OTHER INPUTS FOR I_{IH}			CONDITIONS ON OTHER INPUTS FOR I_{IL}	
	APPLY 4.5 V	APPLY MOMENTARY GND	APPLY GND	APPLY 4.5 V	APPLY MOMENTARY GND
Clock			Clear, J, and K	Clear, J, and K (See Note B)	
	Clear	$\overline{Q}$ (See Note C)	J and K		
Clear		Clear (See Note D)	Clock and J	Clock and J	
		$\overline{Q}$ (See Note C)	Clock and J		
J			Clock and Clear	Clock and Clear	Q (See Note C)
K		Clear (See Note E)	Clock	Clock and Clear	$\overline{Q}$ (See Note C)

NOTES: A. Each input of each flip-flop is tested separately.
B. While maintaining all other conditions, the clock input is momentarily raised to 4.5 V, the V_I is reapplied, and a second measurement of I_{IL} is made.
C. After the application of momentary ground to the specified output, both Q and $\overline{Q}$ are left floating.
D. Apply momentary ground before V_I.
E. Apply momentary ground, then 4.5 V.

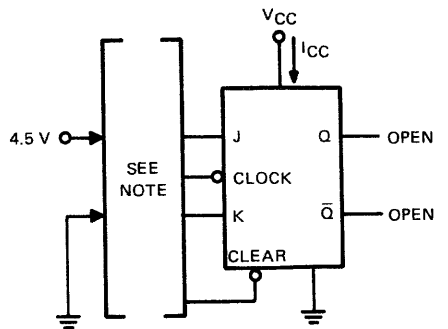
FIGURE 26–I_{IH}, I_{IL}

10



Each $\overline{Q}$ output is tested separately.

FIGURE 27–I_{OS}



I_{CC} is measured with J, K, clear, and clock grounded. A second measurement is made with K grounded, 4.5 V applied to J and clear, and momentary 4.5 V, then ground, applied to clock.

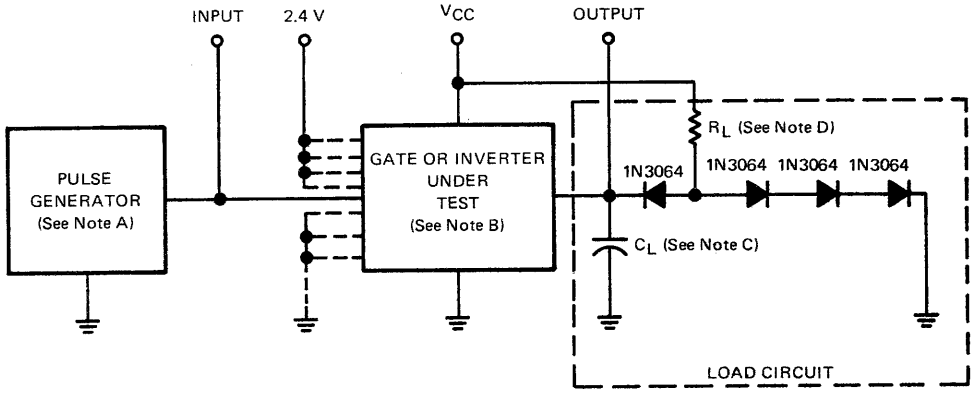
FIGURE 28–I_{CC}

¶Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

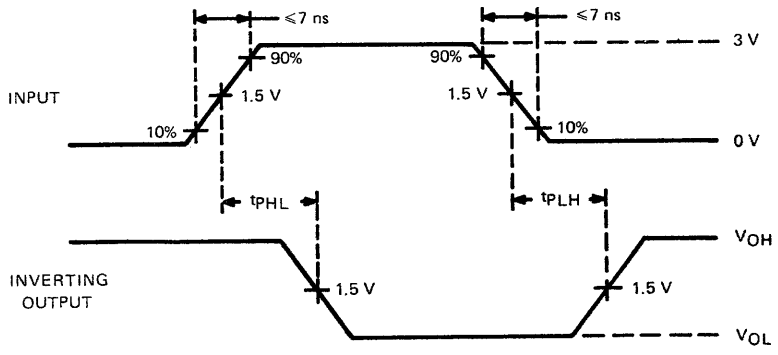
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

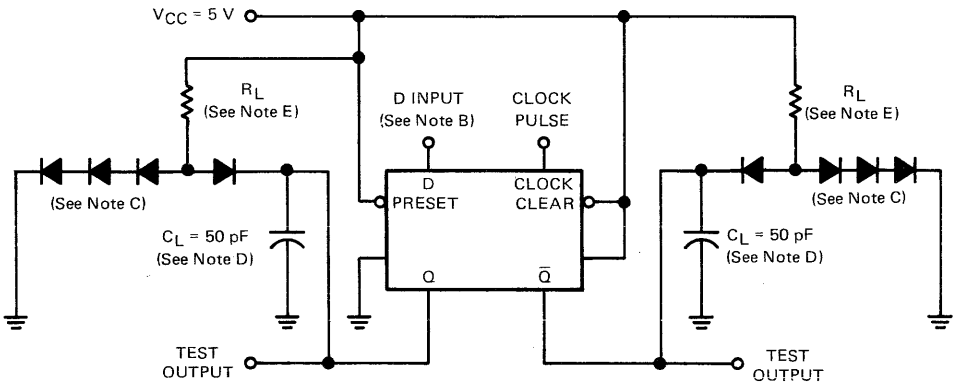
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.
B. Input conditions are established for each gate as follows:
1. Input pulse is applied to one input and 2.4 V is applied to all unused inputs of the NAND gates.
2. Input pulse is applied to one AND section, and 2.4 V is applied to all unused inputs of that AND section, and all inputs of all unused AND sections of the AND-OR-INVERT gates are grounded.
C. C_L includes probe and jig capacitance.
D. For Series RSN54 circuits, $R_L = 400\ \Omega$. For Series RSN54H circuits, $R_L = 280\ \Omega$.

FIGURE 29–GATE PROPAGATION DELAY TIMES

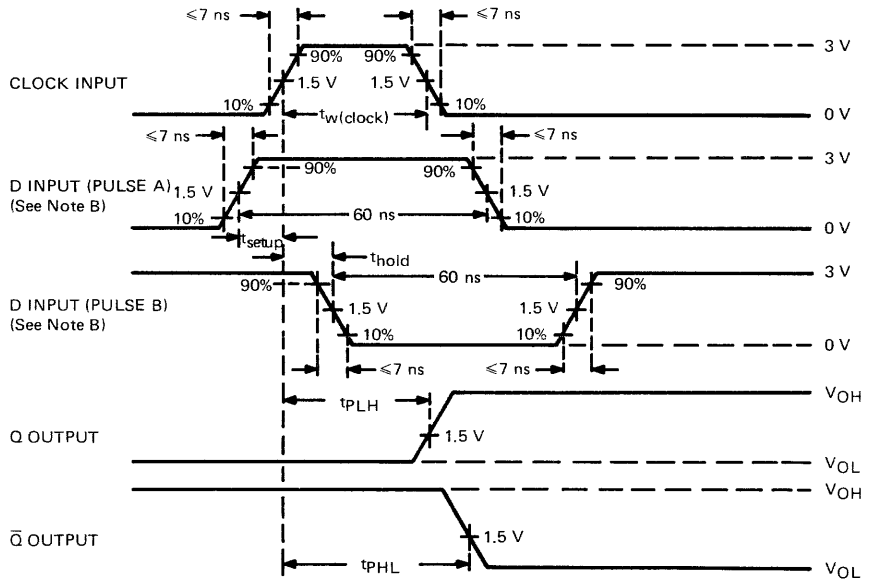
10

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Clock input pulse has the following characteristics: $t_{w(clock)}$ = 30 ns for RSN5474 circuits, 20 ns for RSN54H74 circuits, and PRR = 1 MHz. When testing f_{clock}, vary PRR.

B. D input (pulse A) has the following characteristics: t_{setup} = 20 ns for RSN5474 circuits, 15 ns for RSN54H74 circuits, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 5 ns for RSN5474 circuits, 0 ns for RSN54H74 circuits, and PRR is 50% of the clock PRR.

C. All diodes are 1N3064.

D. C_L includes probe and jig capacitance.

E. For RSN5474 circuits, R_L = 400 Ω. For RSN54H74 circuits, R_L = 280 Ω.

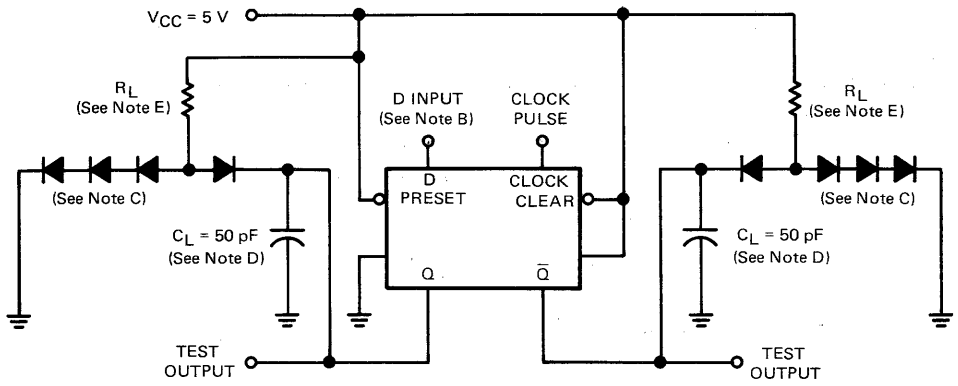
FIGURE 30–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUT OF D-TYPE FLIP-FLOPS (HIGH-LEVEL DATA)

10

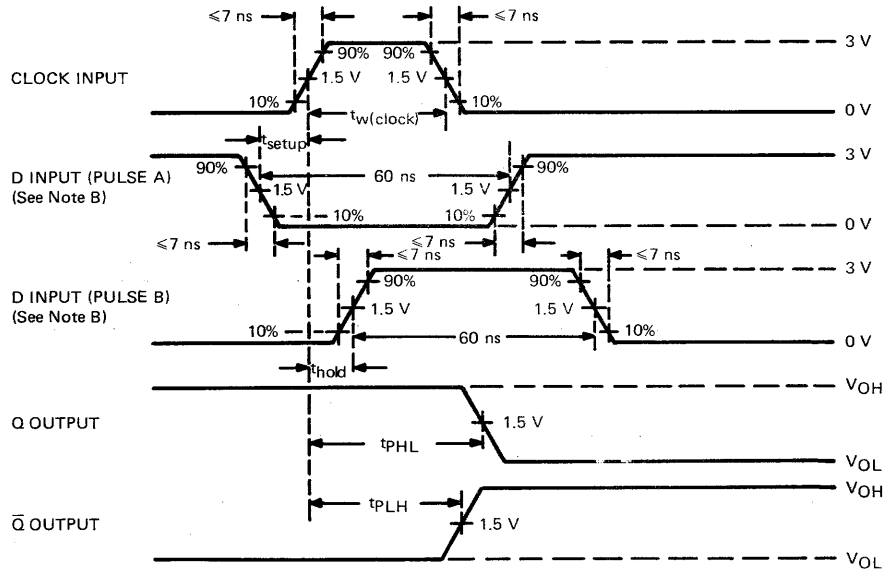
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Clock input pulse has the following characteristics: t_w = 30 ns for RSN5474 circuits, 20 ns for RSN54H74 circuits, and PRR = 1 MHz. When testing f_{clock}, vary PRR.

B. D input (pulse A) has the following characteristics: t_{setup} = 20 ns for RSN5474 circuits, 15 ns for RSN54H74 circuits, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 5 ns for RSN5474 circuits, 0 ns for RSN54H74 circuits, t_w = 60 ns, and PRR is 50% of the clock PRR.

C. All diodes are 1N3064.

D. C_L includes probe and jig capacitance.

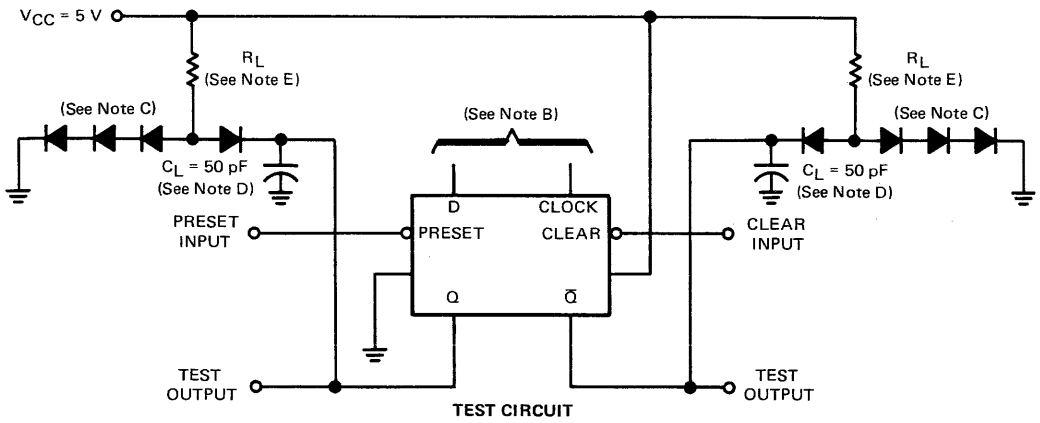
E. For RSN5474 circuits, R_L = 400 Ω. For RSN54H74 circuits, R_L = 280 Ω.

FIGURE 31–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS OF D-TYPE FLIP-FLOPS (LOW-LEVEL DATA)

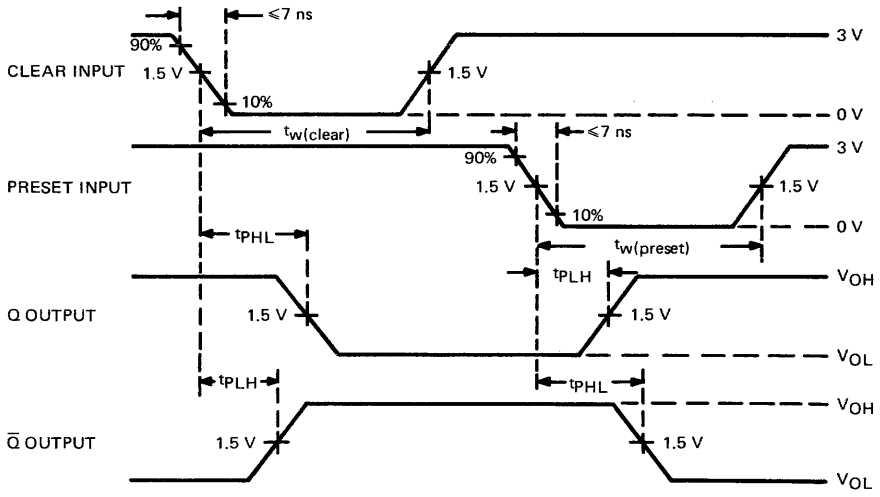
10

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Clear or preset input pulse characteristics: $t_{w(clear)} = t_{(preset)}$ = 30 ns for RSN5474 circuits, 20 ns for RSN54H74 circuits, and PRR = 1 MHz.
B. Clear and preset inputs dominate regardless of the state of clock or D inputs.
C. All diodes are 1N3064.
D. C_L includes probe and jig capacitance.
E. For RSN5474 circuits, R_L = 400 Ω. For RSN54H74 circuits, R_L = 280 Ω.

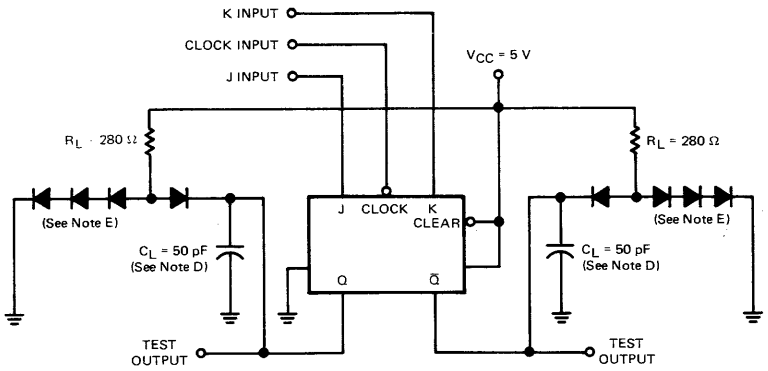
FIGURE 32–SWITCHING CHARACTERISTICS, ASYNCHRONOUS INPUTS OF D-TYPE FLIP-FLOPS

10

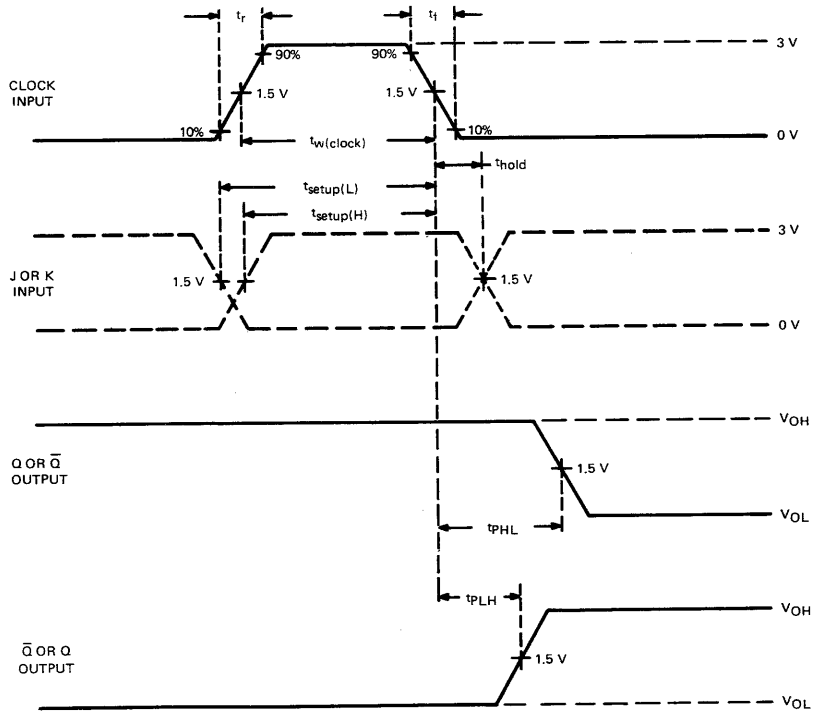
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. When testing propagation delay times from clock input, the clock input pulse characteristics are: $t_r \leq 7$ ns, $t_f \leq 7$ ns, $t_{w(clock)} = 20$ ns, PRR = 1 MHz.

B. When testing f_{max}, the clock input characteristics are: $t_r \leq 3$ ns, $t_f = \leq 3$ ns, $t_{w(clock)} = 12$ ns, PRR = 25 MHz.

C. Both J and K inputs are tested with the input not under test grounded. For the J or K input pulse, t_r or $t_f \leq 7$ ns, and t_{setup} is the minimum specified under recommended operating conditions.

D. C_L includes probe and jig capacitance.

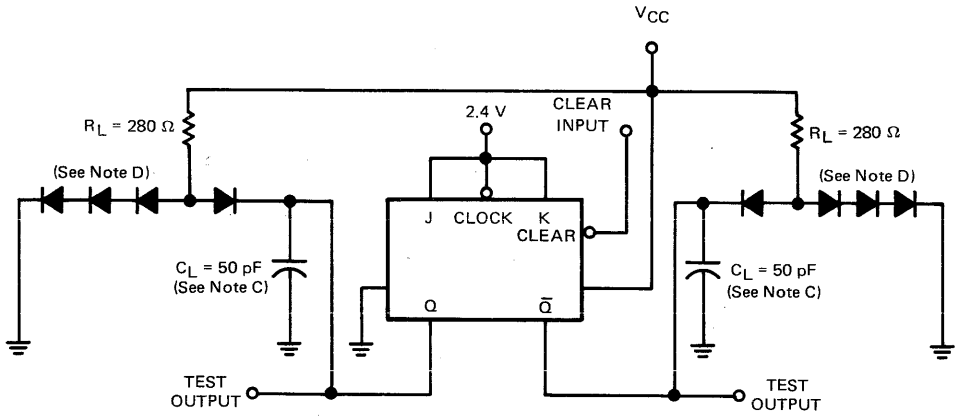
E. All diodes are 1N3064.

FIGURE 33–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS OF J-K FLIP-FLOPS

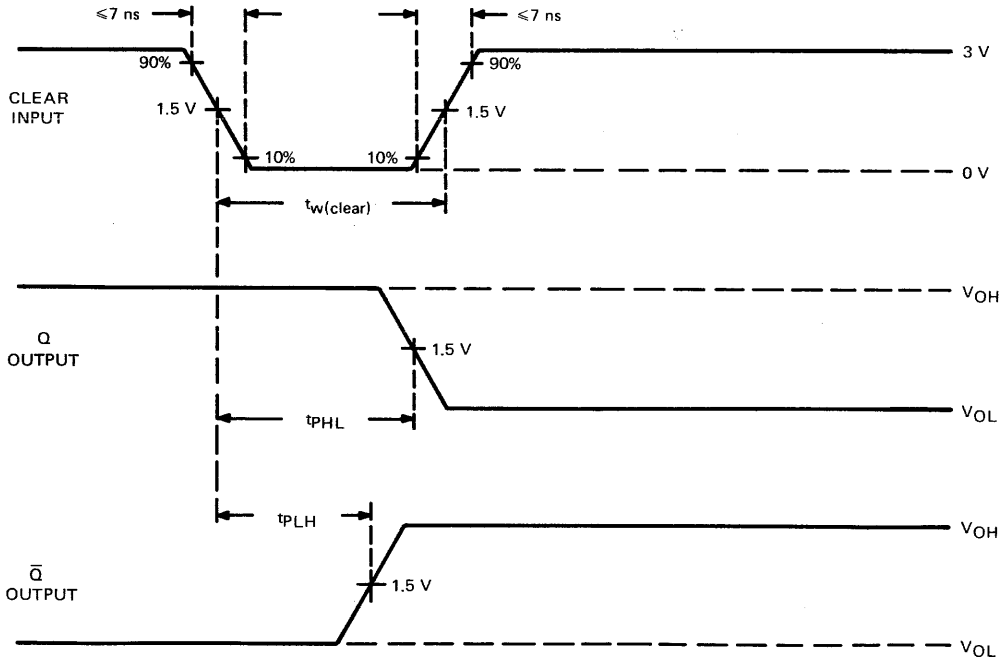
10

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The clear input pulse characteristics are: $t_{w(clear)}$ = 16 ns, PRR = 1 MHz.
B. Q output may be set to the high level with a clock pulse.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N3064.

FIGURE 34–SWITCHING CHARACTERISTICS, ASYNCHRONOUS INPUTS OF J-K FLIP-FLOPS

10

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES RSN54L
RADIATION-HARDENED TTL INTEGRATED CIRCUITS

TTL INTEGRATED CIRCUITS WITH HIGH TOLERANCE TO GAMMA AND NEUTRON IRRADIATION

- Very Low Power Dissipation . . . 1 mW Per Gate Typical at 50% Duty Cycle
- High D-C Noise Margin . . . 1 Volt Typical
- Low Output Impedance Provides Low A-C Noise Susceptibility
- Waveform Integrity over Full Range of Loading and Temperature Conditions
- Normalized Fan-Out to Ten Loads
- Typical NAND Gate Propagation Delay Time (C_L = 50 pF) . . . 45 ns

description

Series RSN54L TTL integrated circuits are specifically designed and fabricated for operation and survivability in nuclear-radiation environments. The basic Series 54/74 configuration, desirable for its "natural" hardness, has been coupled with a state-of-the-art circuit-hardening process. This technology, compatible for use in high volume production, employs:

- dielectric isolation
- thin-film resistors
- small transistor geometries
- shallow base diffusions
- heavy gold doping
- minimum collector thickness and resistivity
- aluminum interconnection system

Series RSN54, RSN54H, and RSN54L logic families are completely compatible with one another and with most other TTL and DTL circuits. These circuits are designed to operate at the same supply voltages and logic levels with the high d-c noise margins which are characteristic of Texas Instruments Series 54/74 circuits. These families of radiation-hardened circuits include the gates and flip-flops needed to perform functions within present-day digital electronic systems. And since these three families are compatible with one another, Series RSN54L circuits may be selectively used to minimize power dissipation in system locations where speed is not the limiting parameter.

Series RSN54L circuits are designed for operation over the full military temperature range of −55°C to 125°C.

10

CONTENTS

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)	7 V
Input voltage (See Notes 1 and 2)	5.5 V
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

input-current requirements

Input-current requirements reflect worst-case conditions for T_A = −55°C to 125°C and V_{CC} = 4.5 V to 5.5 V. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

Each input of the Series RSN54L multiple-emitter input transistors requires no more than a 0.18-mA flow out of the input at a low voltage level; therefore one normalized load (N = 1) is −0.18 mA maximum. Each input requires current into the input at a high voltage level. This current is 10 μA maximum (one normalized load) for each emitter input.

fan-out capability

Fan-out (N) reflects the ability of an output to sink current from a number of Series RSN54L loads at a low voltage level and to supply current at a high voltage level. Each output is capable of sinking current or supplying current to 10 normalized loads (N = 10) within the same series. In addition, Series RSN54L outputs will drive one Series RSN54 load, plus two Series RSN54L loads or one Series RSN54H load. Currents out of the output terminal are specified as negative values.

unused inputs

For optimum switching times and minimum noise susceptibility, unused inputs should be maintained at a positive voltage greater than 2.4 V but not to exceed the absolute maximum rating of 5.5 V. This eliminates the distributed capacitance associated with the floating-input-transistor emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferably this voltage should be between 2.4 V and 3.5 V.

10

b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each input presents a full load to the driving output at a high-level voltage but adds no loading at a low-level voltage.

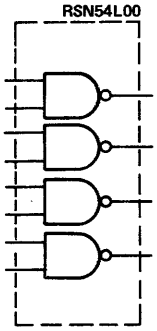
c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One-to-25 unused inputs may be connected to each 1-kΩ resistor.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

standard line summary

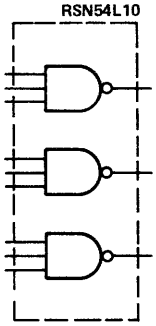
GATE CIRCUITS

RSN54L00



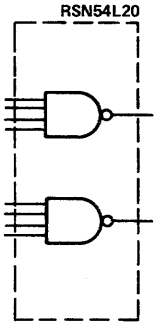
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

RSN54L10



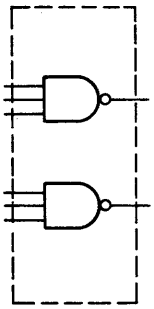
TRIPLE 3-INPUT
POSITIVE-NAND GATES

RSN54L20



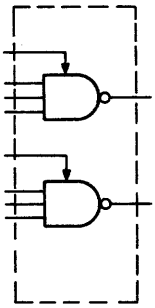
DUAL 4-INPUT
POSITIVE-NAND GATES

RSN54L130



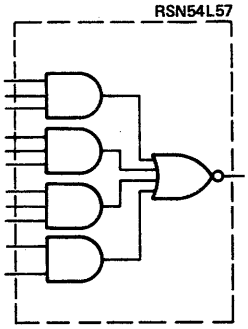
DUAL 3-INPUT
POSITIVE-NAND GATE

RSN54L131



DUAL EXPANDABLE 3-INPUT
POSITIVE-NAND GATE

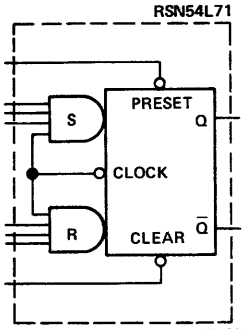
RSN54L57



3-3-3-2 INPUT
AND-OR-INVERT GATE

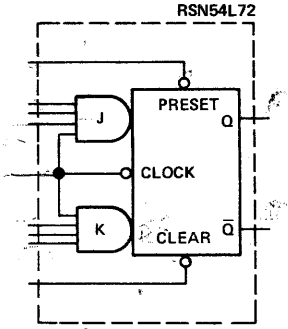
FLIP-FLOP CIRCUITS

RSN54L71



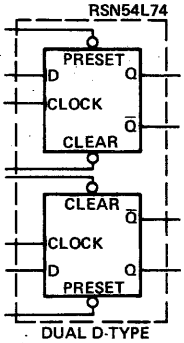
S-R MASTER SLAVE FLIP-FLOP

RSN54L72



J-K MASTER SLAVE FLIP-FLOP

RSN54L74



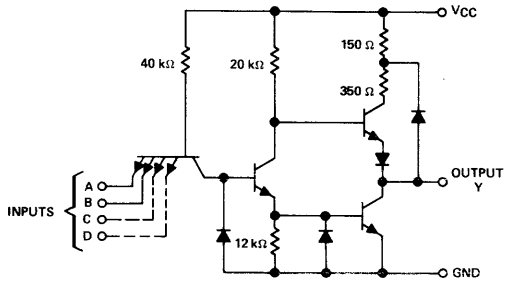
DUAL D-TYPE
EDGE-TRIGGERED FLIP-FLOPS

10

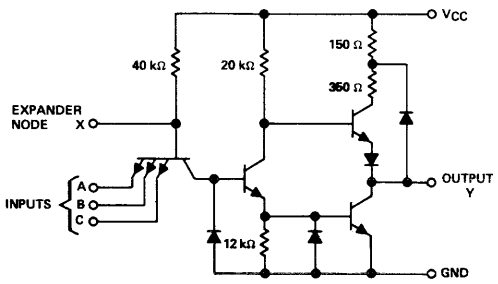
CIRCUIT TYPES RSN54L00, RSN54L10, RSN54L20, RSN54L130, RSN54L131
POSITIVE-NAND GATES

schematics (each gate)

RSN54L00, RSN54L10, RSN54L20, RSN54L130



RSN54L131

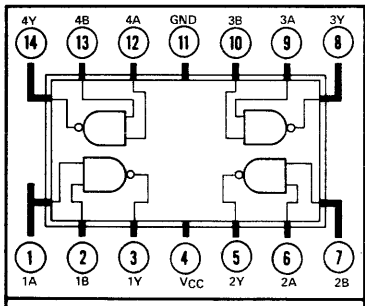


Component values shown are nominal.

logic

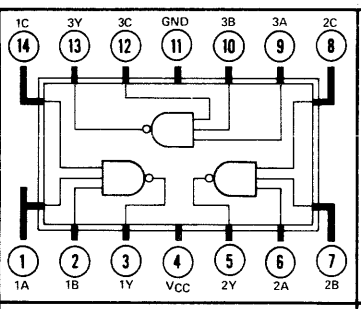
H FLAT PACKAGE (TOP VIEWS)

RSN54L00



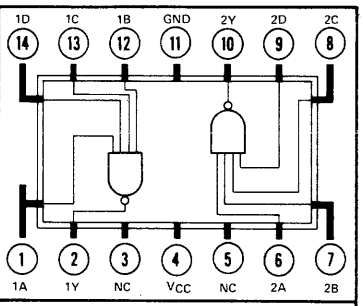
positive logic: $Y = \overline{AB}$

RSN54L10



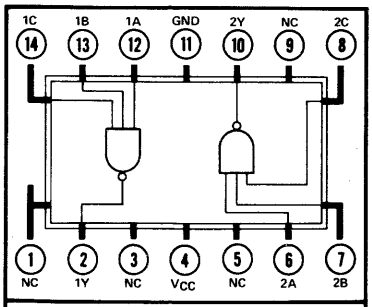
positive logic: $Y = \overline{ABC}$

RSN54L20



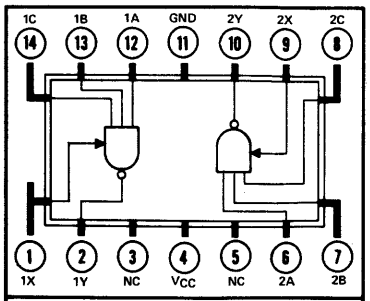
positive logic: $Y = \overline{ABCD}$

RSN54L130



positive logic: $Y = \overline{ABC}$

RSN54L131



positive logic: $Y = \overline{ABCX}$

NC—No internal connection

10

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Normalized fan-out from each gate, N			10	
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage	1		1.9		V
V_{IL}	Low-level input voltage	2			0.8	
V_{OH}	High-level output voltage	2	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	1	V_{CC} = MIN, V_{IH} = 1.9 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	3	V_{CC} = MAX, V_I = 5.5 V		100	μA
I_{IH}	High-level input current	3	V_{CC} = MAX, V_I = 2.4 V		10	μA
I_{IL}	Low-level input current	4	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{OS}	Short-circuit output current	5	V_{CC} = MAX	−1	−15	mA
I_{CCH}	Supply current, high-level output (average per gate)	6	V_{CC} = MAX, V_I = 0		0.2	mA
I_{CCL}	Supply current, low-level output (average per gate)	6	V_{CC} = MAX, V_I = 4.5 V		0.51	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

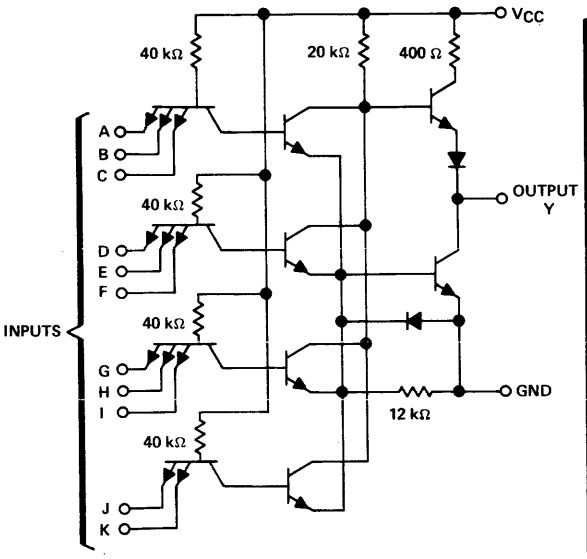
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	28	C_L = 50 pF, R_L = 4 kΩ		60	ns
t_{PLH}	Propagation delay time, high-to-low-level output				60	ns

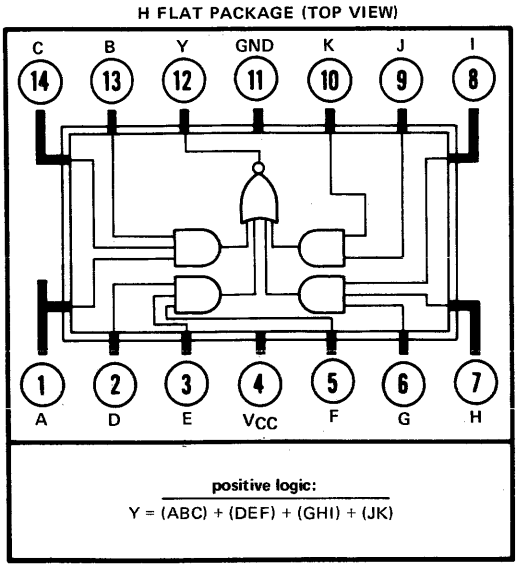
10

CIRCUIT TYPE RSN54L57
3-3-3-2-INPUT AND-OR-INVERT GATE

schematic



logic



recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Normalized fan-out from output, N			10	
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage	7		1.9		V
V_{IL}	Low-level input voltage	8			0.8	V
V_{OH}	High-level output voltage	8	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	7	V_{CC} = MIN, I_{IH} = 1.9 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	9	V_{CC} = MAX, V_I = 5.5 V		100	μA
I_{IH}	High-level input current	9	V_{CC} = MAX, V_I = 2.4 V		10	μA
I_{IL}	Low-level input current	10	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{OS}	Short-circuit output current	11	V_{CC} = MAX	−1	−15	mA
I_{CCH}	Supply current, high-level output	12	V_{CC} = MAX, V_I = 0		0.8	mA
I_{CCL}	Supply current, low-level output	12	V_{CC} = MAX, V_I = 4.5 V		0.99	mA

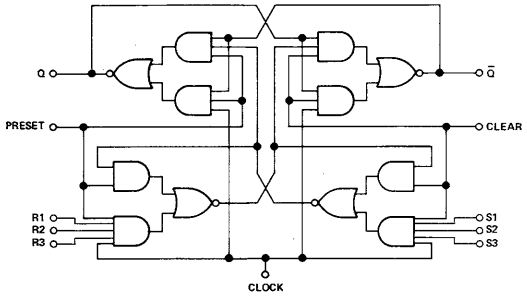
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	28	C_L = 50 pF, R_L = 4 kΩ		90	ns
t_{PHL}	Propagation delay time, high-to-low-level output				60	ns

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

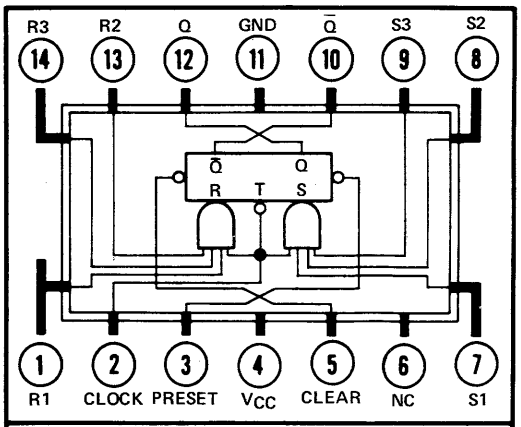
CIRCUIT TYPE RSN54L71
S-R MASTER-SLAVE FLIP-FLOP

functional block diagram



logic

H FLAT PACKAGE (TOP VIEW)



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

NC—No internal connection

description

These S-R flip-flops are based on the master-slave principle. The AND-OR gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

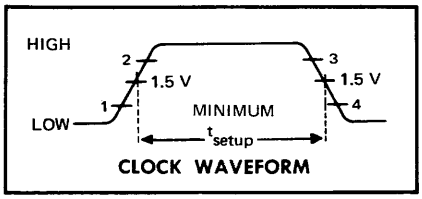
1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND-OR gate inputs
4. Transfer information from master to slave

Logic levels of S and R inputs must not be allowed to change when the clock pulse is in a high state.

TRUTH TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
S	R	Q	$\bar{Q}$
L	L	Q_n	$\bar{Q}_n$
L	H	L	H
H	L	H	L
H	H	Indeterminate	

S = S1·S2·S3
R = R1·R2·R3
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
Q_n = level of output Q at t_n
$\bar{Q}_n$ = level of output $\bar{Q}$ at t_n



CLOCK WAVEFORM

10

CIRCUIT TYPE RSN54L71
S-R MASTER-SLAVE FLIP-FLOP

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Normalized fan-out from each output, N			10	
Width of clock pulse, $t_{w(clock)}$	200			ns
Width of preset pulse, $t_{w(preset)}$	100			ns
Width of clear pulse, $t_{w(clear)}$	100			ns
Input setup time, t_{setup} (see Note 1)	100			ns
Input hold time, t_{hold} (see Note 2)	0			ns
Operating free-air temperature, T_A	−55		125	°C

NOTES: 1. Setup time is the interval immediately preceeding the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†		MIN	MAX	UNIT
V_{IH}	High-level input voltage		13 and 14			1.9		V
V_{IL}	Low-level input voltage		13 and 14				0.8	V
V_{OH}	High-level output voltage		13	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 1.9 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage		14	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 1.9 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	Any S or R	15	V_{CC} = MAX,	V_I = 5.5 V		100	μA
		Preset, clear or clock					200	
I_{IH}	High-level input current	Any S or R	15	V_{CC} = MAX,	V_I = 2.4 V		10	μA
		Preset, clear, or clock					20	
I_{IL}	Low-level input current	Any S or R	16	V_{CC} = MAX,	V_I = 0.3 V		−0.18	mA
		Preset, clear, or clock					−0.4	
I_{OS}	Short-circuit output current		17	V_{CC} = MAX		−1	−15	mA
I_{CC}	Supply current		15	V_{CC} = MAX			1.44	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

10

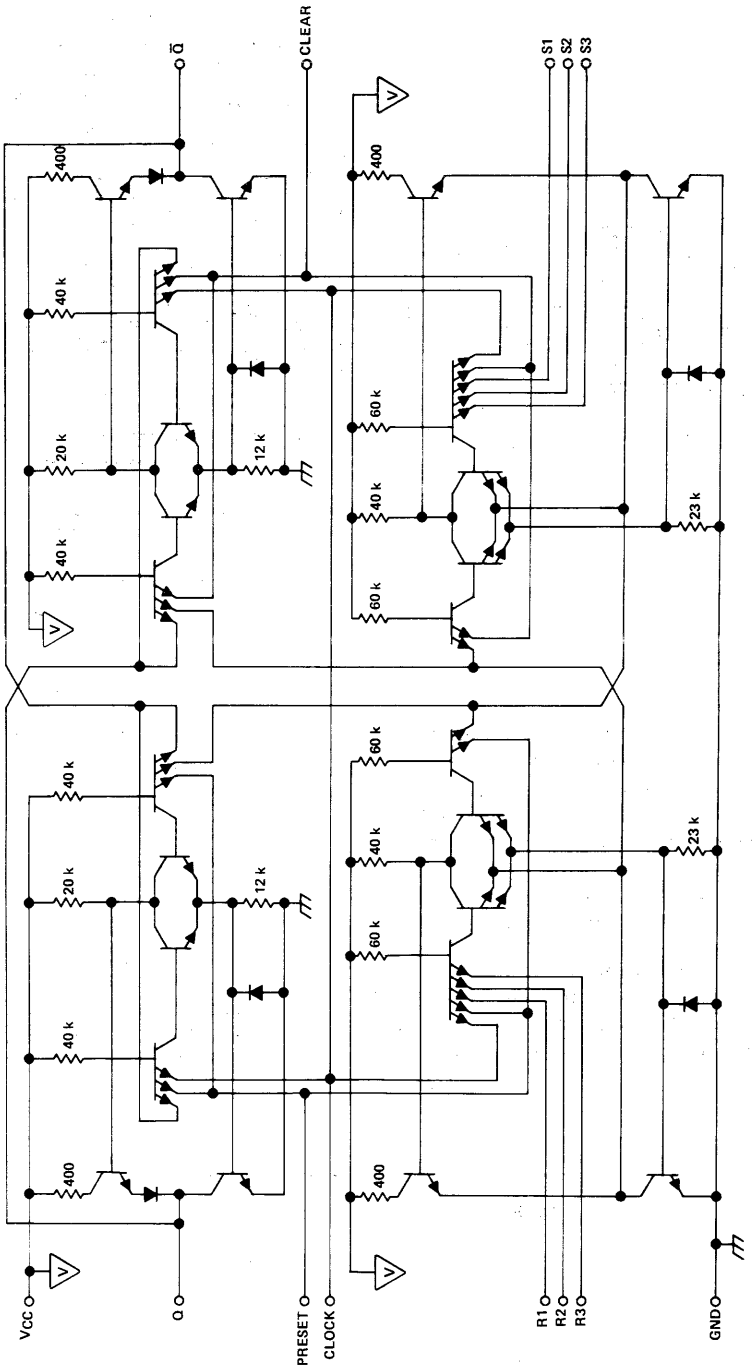
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	29	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from preset or clear	30				75	ns
t_{PHL}	Propagation delay time, high-to-low-level output from preset or clear					150	
t_{PLH}	Propagation delay time, low-to-high-level output from clock	29		10		75	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			10		150	

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE RSN54L71
S-R MASTER-SLAVE FLIP-FLOP

schematic

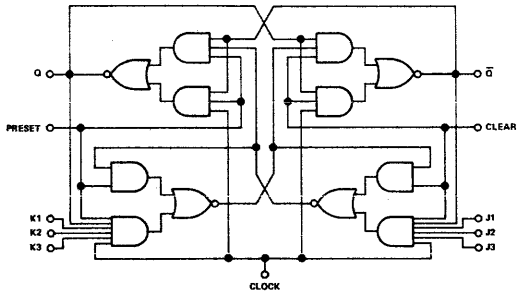


▽ . . . V_{CC} bus
Resistor values are nominal in ohms.

10

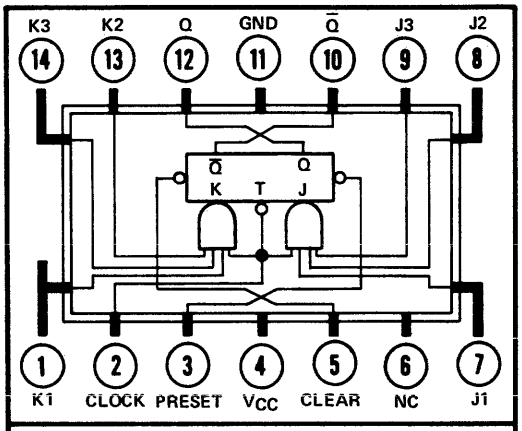
CIRCUIT TYPE RSN54L72
J-K MASTER-SLAVE FLIP-FLOP

functional block diagram



logic

H FLAT PACKAGE (TOP VIEW)



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

NC—No internal connection

description

These J-K flip-flops are based on the master-slave principle. The AND-OR gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

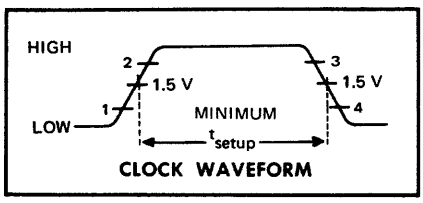
1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND-OR gate inputs
4. Transfer information from master to slave

Logic levels of J and K inputs must not be allowed to change when the clock pulse is in a high state.

TRUTH TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	K	Q	$\bar{Q}$
L	L	Q_n	$\bar{Q}_n$
L	H	L	H
H	L	H	L
H	H	$\bar{Q}_n$	Q_n

J = J1•J2•J3
K = K1•K2•K3
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
Q_n = level of output Q at t_n
$\bar{Q}_n$ = complement of Q_n or level of output $\bar{Q}$ at t_n



CLOCK WAVEFORM

10

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Normalized fan-out from each output, N			10	
Width of clock pulse, $t_{w(clock)}$	200			ns
Width of preset pulse, $t_{w(preset)}$	100			ns
Width of clear pulse, $t_{w(clear)}$	100			ns
Input setup time, t_{setup} (see Note 1)	$t_{w(clock)}$			ns
Input hold time, t_{hold} (see Note 2)	0			ns
Operating free-air temperature, T_A	−55		125	°C

NOTES: 1. Setup time is the interval immediately preceeding the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†		MIN	MAX	UNIT
V_{IH}	High-level input voltage		18 and 19			1.9		V
V_{IL}	Low-level input voltage		18 and 19				0.8	V
V_{OH}	High-level output voltage		18	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 1.9 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage		19	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 1.9 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	Any J or K	20	V_{CC} = MAX,	V_I = 5.5 V		100	μA
		Preset, clear or clock					200	
I_{IH}	High-level input current	Any J or K	20	V_{CC} = MAX,	V_I = 2.4 V		10	μA
		Preset, clear, or clock					20	
I_{IL}	Low-level input current	Any J or K	21	V_{CC} = MAX,	V_I = 0.3 V		−0.18	mA
		Preset, clear, or clock					−0.4	
I_{OS}	Short-circuit output current		22	V_{CC} = MAX		−1	−15	mA
I_{CC}	Supply current		20	V_{CC} = MAX			1.44	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

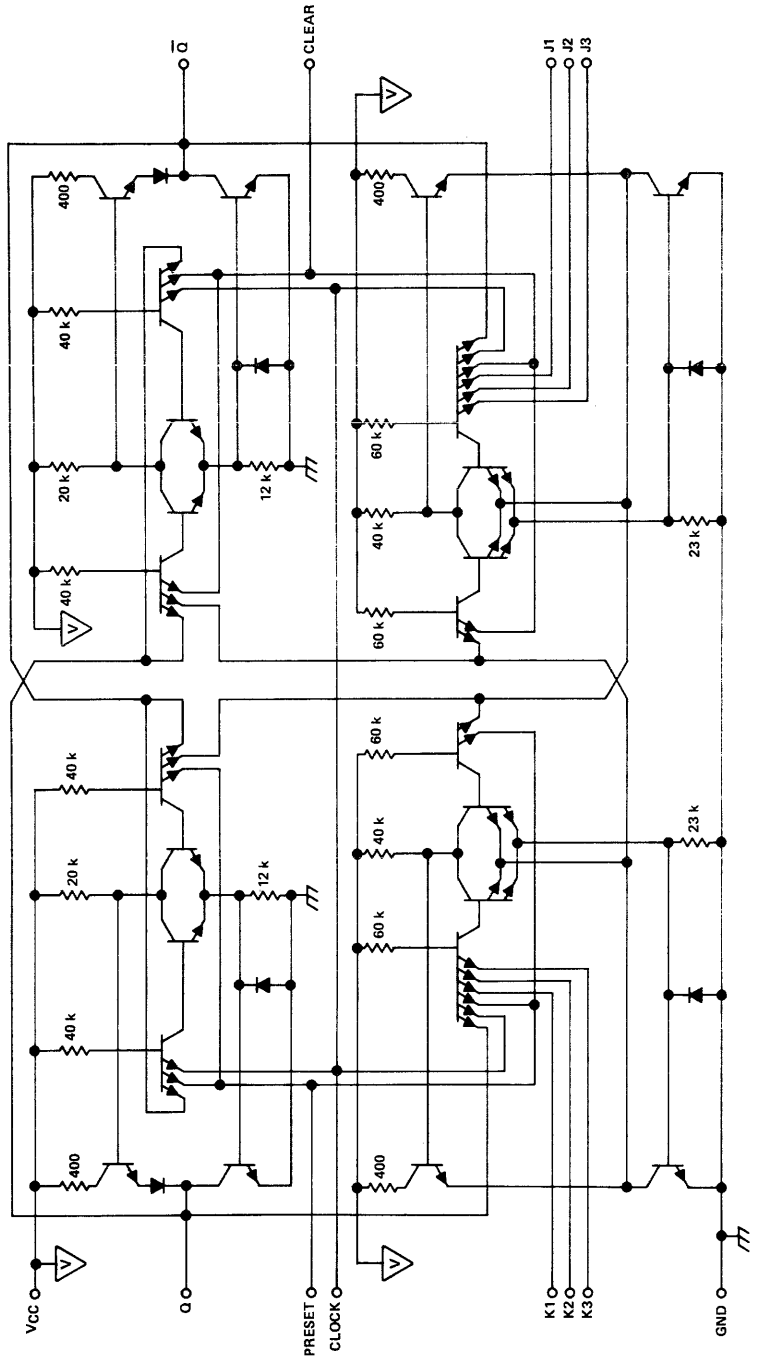
10

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	29	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from preset or clear	30				75	ns
t_{PHL}	Propagation delay time, high-to-low-level output from preset or clear					150	
t_{PLH}	Propagation delay time, low-to-high-level output from clock	29		10		75	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			10		150	

CIRCUIT TYPE RSN54L72
J-K MASTER-SLAVE FLIP-FLOP

schematic



10

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE RSN54L74
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

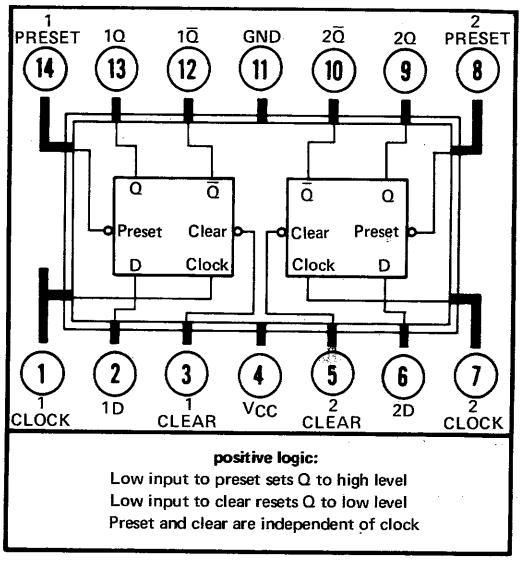
TRUTH TABLE

INPUT AT t_n	OUTPUTS AT t_{n+1}	
D	Q	$\bar{Q}$
L	L	H
H	H	L

H = high level, L = low level
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

logic

H FLAT PACKAGE (TOP VIEW)



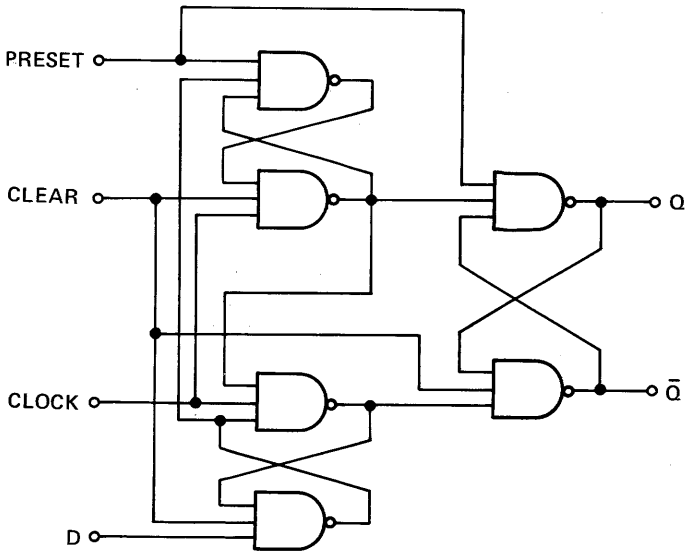
positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

description

This monolithic, dual, low-power edge-triggered flip-flop utilizes TTL circuitry to perform D-type flip-flop logic. Each flip-flop has individual clear and preset inputs, and also complementary Q and $\bar{Q}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

functional block diagram (each flip-flop)



10

CIRCUIT TYPE RSN54L74
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Normalized fan-out from each output, N			10	
Width of clock pulse, $t_{w(clock)}$	200			ns
Width of preset pulse, $t_{w(preset)}$	100			ns
Width of clear pulse, $t_{w(clear)}$	100			ns
Input setup time, t_{setup} (see Note 1)	30			ns
Input hold time, t_{hold} (see Note 2)	0			ns
Operating free-air temperature, T_A	−55		125	°C

NOTES: 1. Setup time is the interval immediately preceeding the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage		23 and 24		1.9		V
V_{IL}	Low-level input voltage		23 and 24			0.8	V
V_{OH}	High-level output voltage		23	V_{CC} = MIN, V_{IH} = 1.9 V, V_{IL} = 0.8 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage		24	V_{CC} = MIN, V_{IH} = 1.9 V, V_{IL} = 0.8 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	D input	25	V_{CC} = MAX, V_I = 5.5 V		0.1	mA
		Preset or clock				0.2	
		Clear				0.3	
I_{IH}	High-level input current	D input	25	V_{CC} = MAX, V_I = 2.4 V		10	μA
		Preset or clock				20	
		Clear				30	
I_{IL}	Low-level input current	D or preset	25	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
		Clear or clock				−0.36	
I_{OS}	Short-circuit output current		26	V_{CC} = MAX	−1	−15	mA
I_{CC}	Supply current (each flip-flop)		27	V_{CC} = MAX		1.5	mA

10

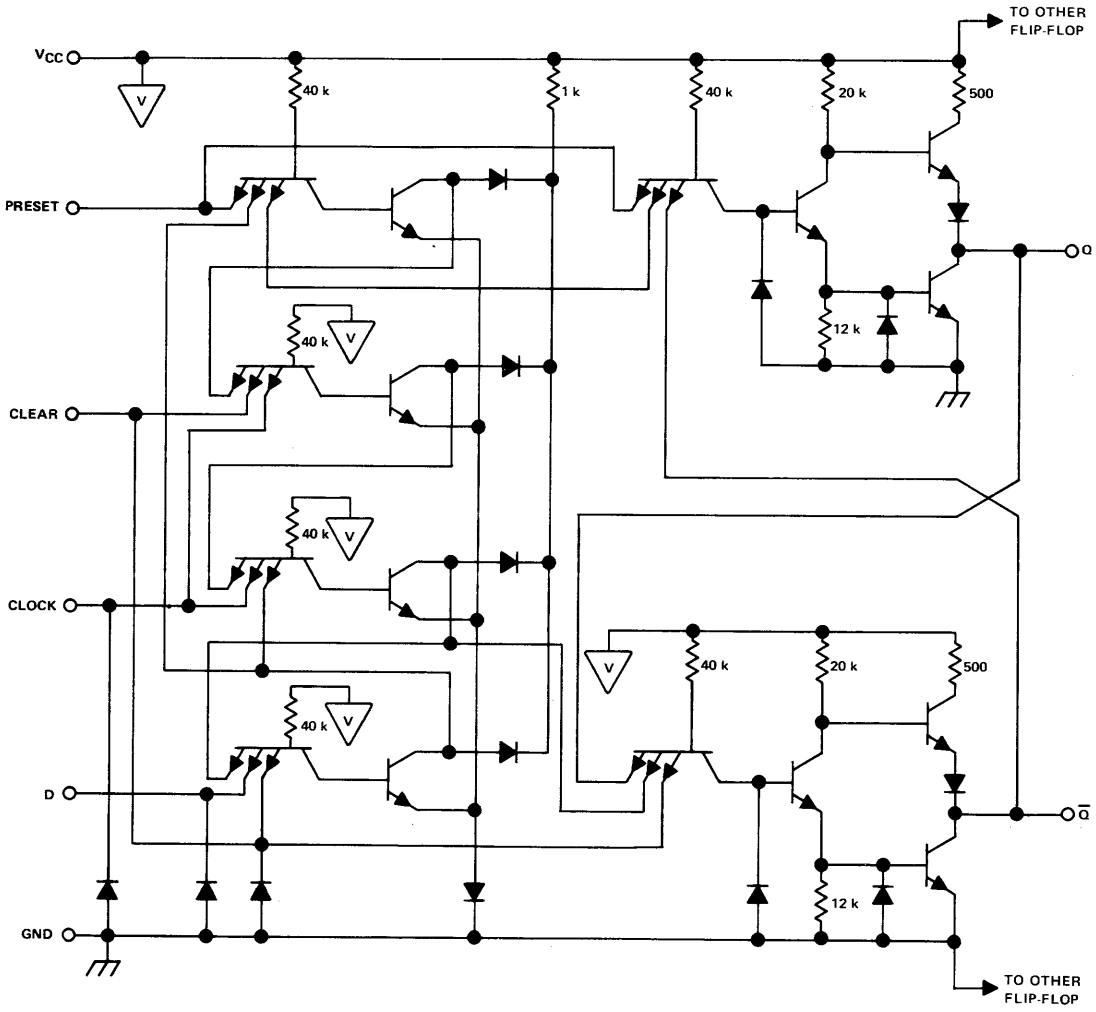
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	31 and 32	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from preset or clear	33			50	75	ns
t_{PHL}	Propagation delay time, high-to-low-level output from preset or clear				80	150	
t_{PLH}	Propagation delay time, low-to-high-level output from clock	31 and 32			60	100	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock				90	150	

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

schematic

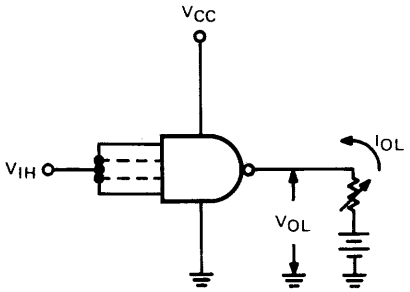


▽ . . . V_{CC} bus
Resistor values are nominal in ohms.

10

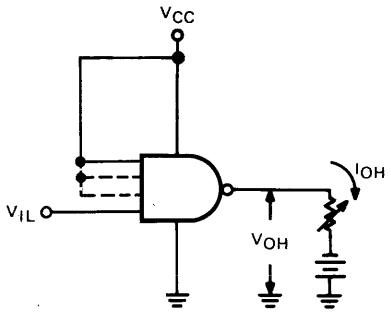
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶



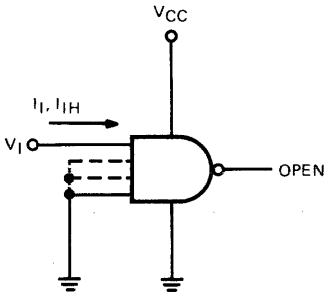
All inputs are tested simultaneously.

FIGURE 1–V_{IH}, V_{OL}



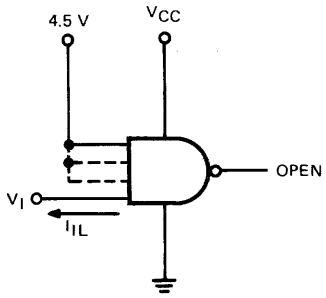
Each input is tested separately.

FIGURE 2–V_{IL}, V_{OH}



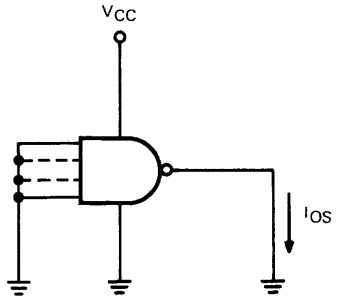
Each input is tested separately.

FIGURE 3–I_I, I_{IH}



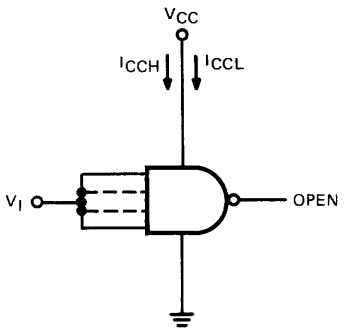
Each input is tested separately.

FIGURE 4–I_{IL}



Each gate is tested separately.

FIGURE 5–I_{OS}



All gates are tested simultaneously. Average-per-gate value = $\frac{I_{CC\ total}}{\text{number of gates in package}}$.

FIGURE 6–I_{CCH}, I_{CCL}

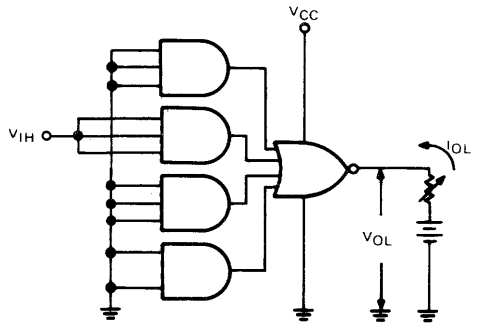
¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

10

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

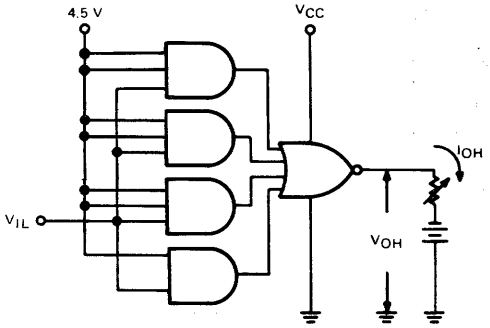
PARAMETER MEASUREMENT INFORMATION

d-c test circuits[¶] (continued)



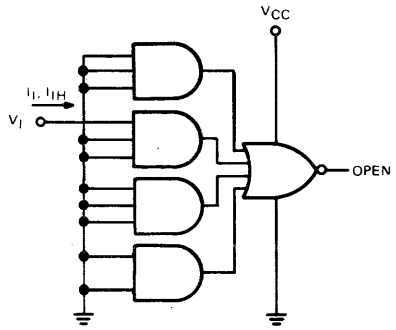
Each AND section is tested separately.

FIGURE 7–V_{IH}, V_{OL}



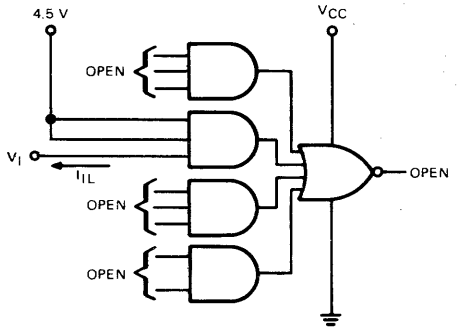
Each set of inputs is tested separately. A set comprises one input from each AND section.

FIGURE 8–V_{IL}, V_{OH}



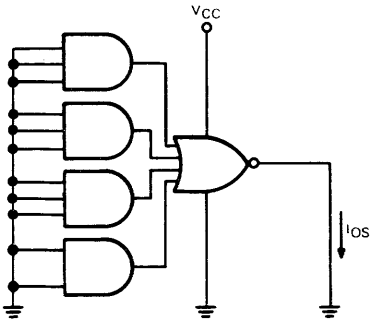
Each input is tested separately.

FIGURE 9–I_I, I_{IH}



Each input is tested separately.

FIGURE 10–I_{IL}



Each output is tested separately.

FIGURE 11–I_{OS}

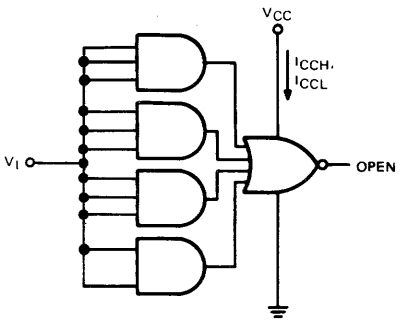


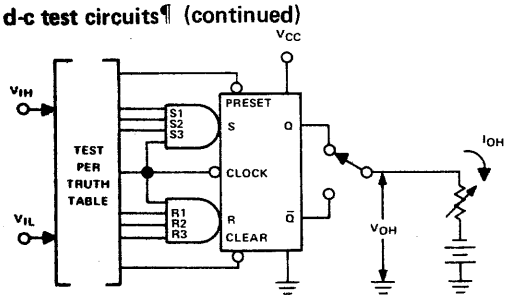
FIGURE 12–I_{CCH}, I_{CCL}

[¶] Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

10

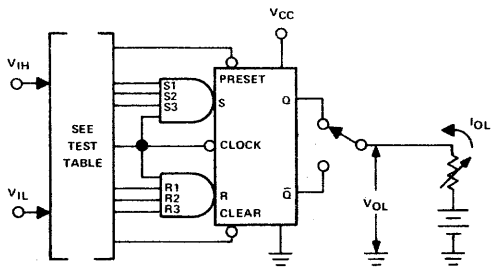
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶ (continued)



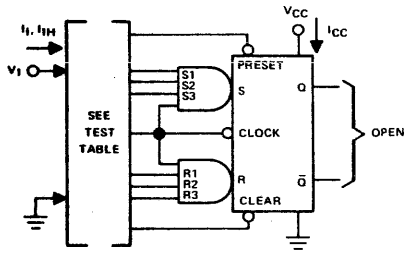
Each output is tested separately.

FIGURE 13–V_{IH}, V_{IL}, V_{OH}



Each input is tested separately.

FIGURE 14–V_{IH}, V_{IL}, V_{OL}

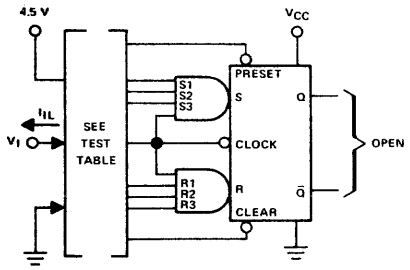


1. Each input is tested separately.
2. With all other inputs grounded, I_{CC} is measured first with clear, then preset, at 4.5 V.

TEST TABLE

APPLY V_I (TEST I_I, I_{IH})	GROUND
Clock	Preset, Clear, R1, R2, R3, S1, S2, and S3
Preset	Clock, R1, R2, and R3
Clear	Clock, S1, S2, and S3
R1	Clock, Preset, R2, and R3
R2	Clock, Preset, R1, and R3
R3	Clock, Preset, R1, and R2
S1	Clock, Clear, S2, and S3
S2	Clock, Clear, S1, and S3
S3	Clock, Clear, S1, and S2

FIGURE 15–I_I, I_{IH}, I_{CC}

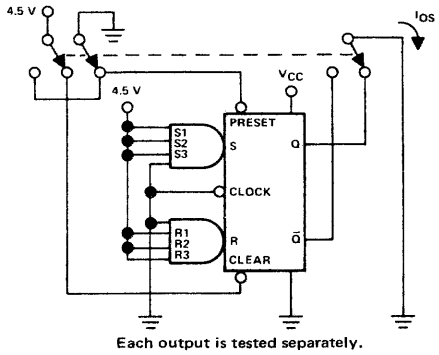


Each input is tested separately.

TEST TABLE

APPLY V_I (TEST I_{IL})	APPLY 4.5 V
Clock	Preset, R1, R2, R3, S1, S2, and S3
Clock	Clear, R1, R2, R3, S1, S2, and S3
Preset	R1, R2, R3, S1, S2, and S3
Clear	R1, R2, R3, S1, S2, and S3
R1	Preset, Clock, R2, and R3
R2	Preset, Clock, R1, and R3
R3	Preset, Clock, R1, and R2
S1	Clear, Clock, S2, and S3
S2	Clear, Clock, S1, and S3
S3	Clear, Clock, S1, and S2

FIGURE 16–I_{IL}



Each output is tested separately.

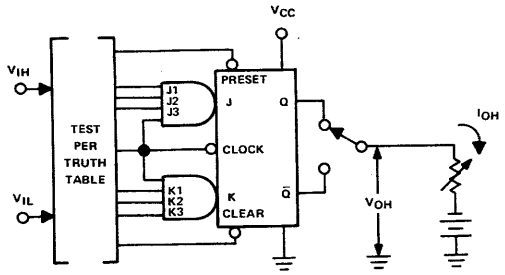
FIGURE 17–I_{OS}

¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

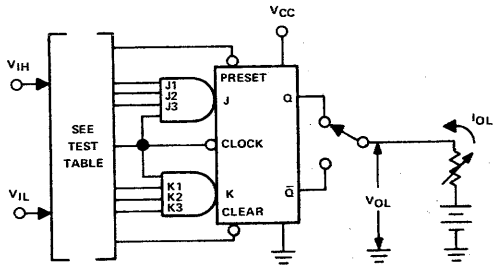
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶ (continued)



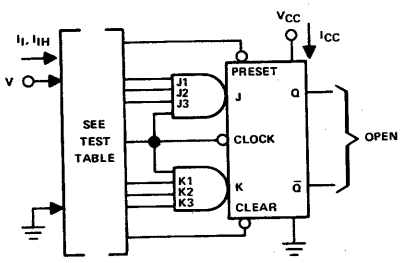
Each output is tested separately.

FIGURE 18–V_{IL}, V_{IH}, V_{OH}



Each output is tested separately.

FIGURE 19–V_{IL}, V_{IH}, V_{OL}

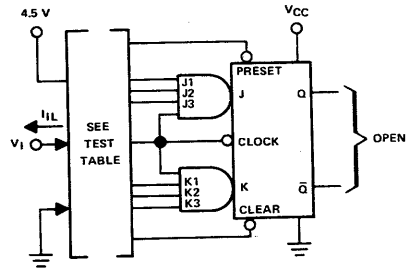


1. Each input is tested separately.
2. With all other inputs grounded, I_{CC} is measured first with clear, then preset, at 4.5 V.

TEST TABLE

APPLY V_I (TEST I_I, I_{IH})	GROUND
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2, and K3
Clear	Clock, J1, J2, and J3
J1	Clock, Clear, J2 and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

FIGURE 20–I_I, I_{IH}, I_{CC}

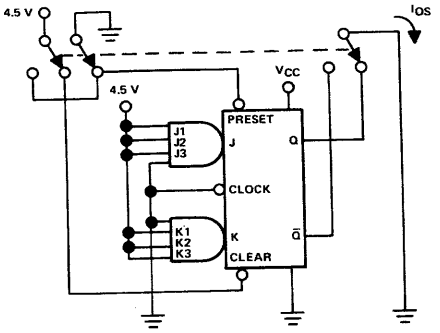


Each input is tested separately.

TEST TABLE

APPLY V_I (TEST I_{IL})	APPLY MOMENTARY GND, THEN 4.5 V	APPLY 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

FIGURE 21–I_{IL}



Each output is tested separately.

FIGURE 22–I_{OS}

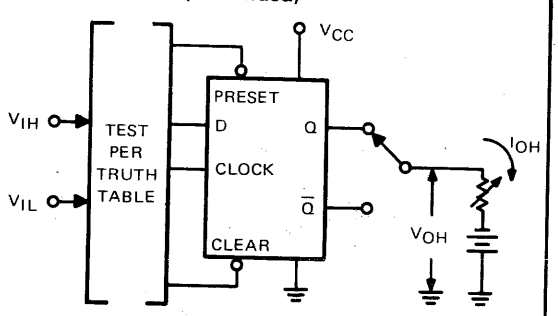
¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

10

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

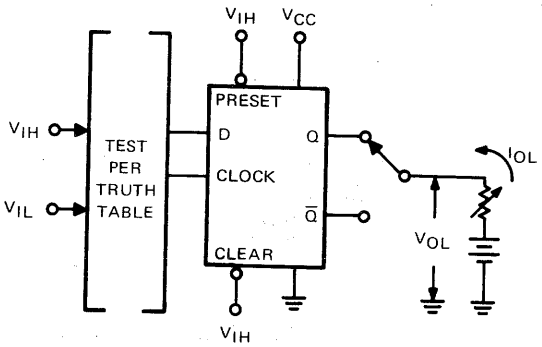
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶ (continued)



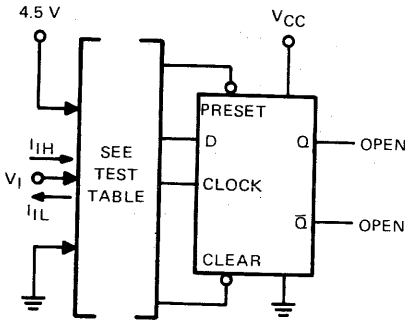
A. Each flip-flop is tested separately.
B. Each output is tested separately.
C. V_{OH} is also tested using clear and preset inputs.

FIGURE 23–V_{IH}, V_{IL}, V_{OH}



A. Each flip-flop is tested separately.
B. Each output is tested separately.

FIGURE 24–V_{IH}, V_{IL}, V_{OL}

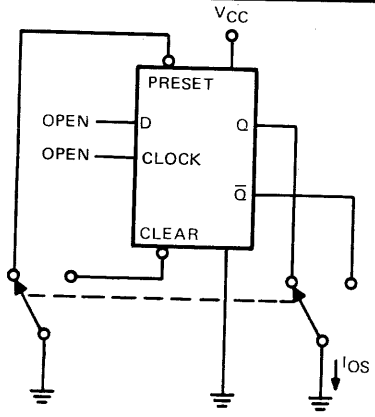


TEST TABLE

APPLY V_I MEASURE I_I, I_{IH}, I_{IL}	CONDITIONS ON OTHER INPUTS FOR I_I, I_{IH}		CONDITIONS ON OTHER INPUTS FOR I_{IL}	
	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND
Clock	Clear and D	Preset	Clear	Preset and D
Clock	Preset and D	Clear		
Preset	Clear and D	Clock (See Note B)	Clear	Clock and D
Clear	Preset	D and Clock (See Note B)	Clock, D, and Preset	None
Clear			D	Preset and Clock
D	Clock and Preset	Clear	Clock and Clear	Preset

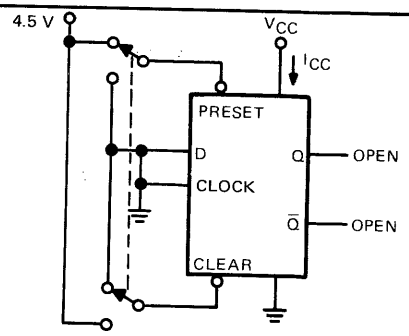
NOTES: A. Each input of each flip-flop is tested separately.
B. GND is momentarily applied to clock, then 4.5 V.

FIGURE 25–I_I, I_{IH}, I_{IL}



Each output is tested separately.

FIGURE 26–I_{OS}



I_{CC} is measured simultaneously for both flip-flops with D, clock, and preset at ground; then with D, clock, and clear at ground.

FIGURE 27–I_{CC}

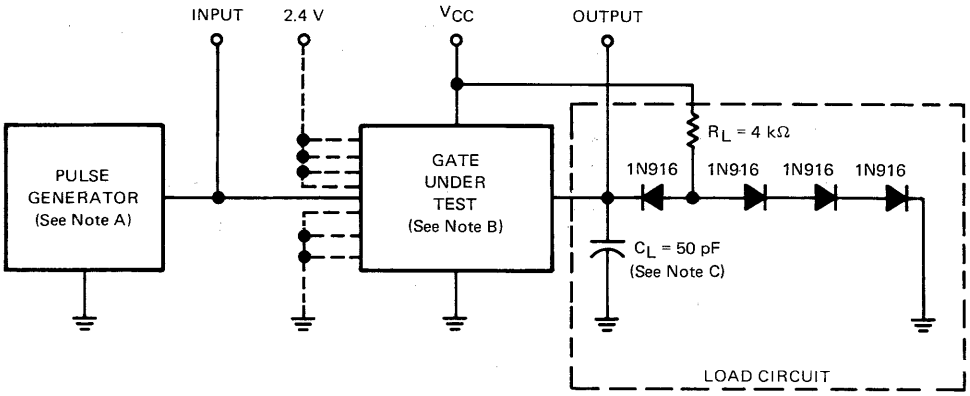
¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

10

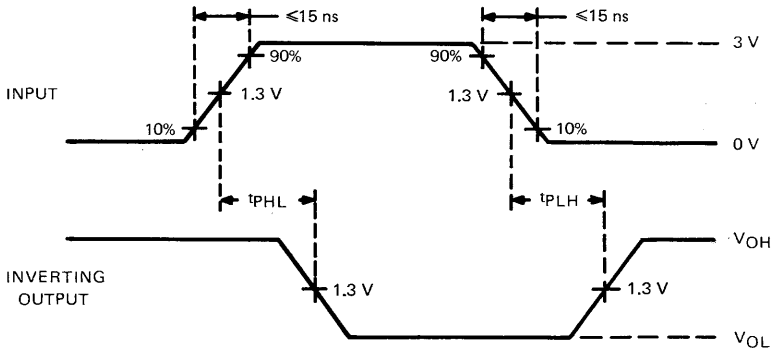
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

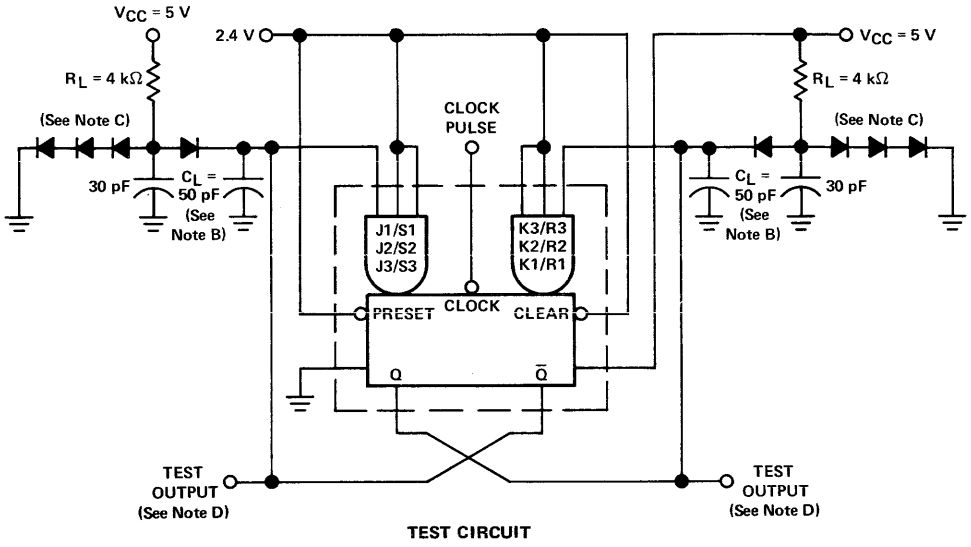
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.
B. Input conditions are established for each gate as follows:
1. Input pulse is applied to one input and 2.4 V is applied to all unused inputs of the NAND gates.
2. Input pulse is applied to one AND section, and 2.4 V is applied to all unused inputs of the AND section, and all inputs of all unused AND sections of the AND-OR-INVERT gate are grounded.
C. C_L includes probe and jig capacitance.

FIGURE 28–GATE PROPAGATION DELAY TIMES

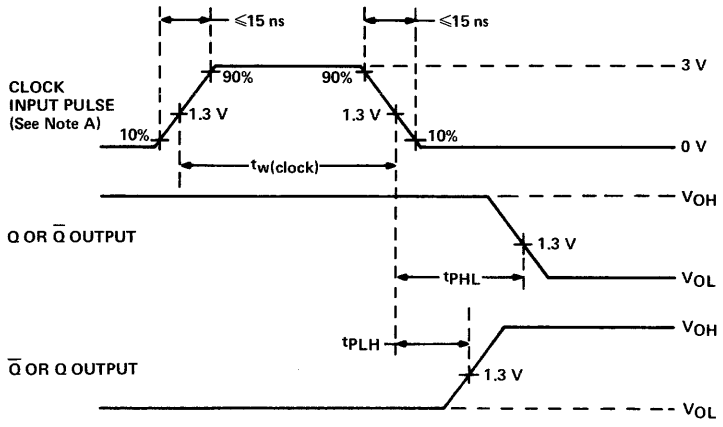
10

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

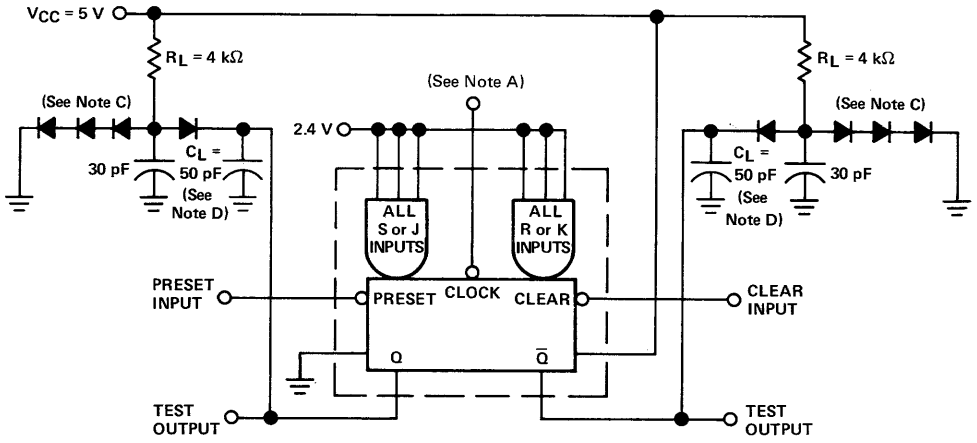
NOTES: A. Clock input characteristics: t_w = 200 ns, and PRR = 500 kHz. When testing f_{max}, vary PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916.
D. Load is applied only to output under test.

FIGURE 29–S-R AND J-K FLIP-FLOP SWITCHING TIMES FROM SYNCHRONOUS INPUTS

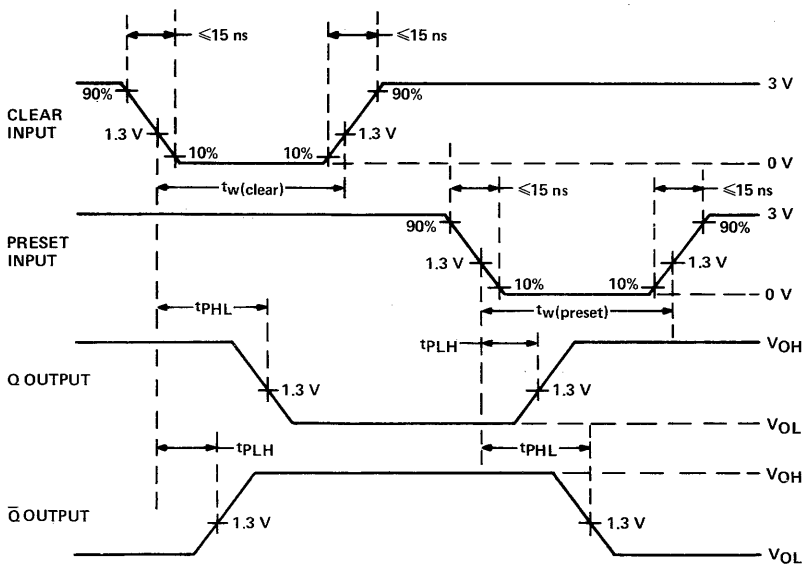
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

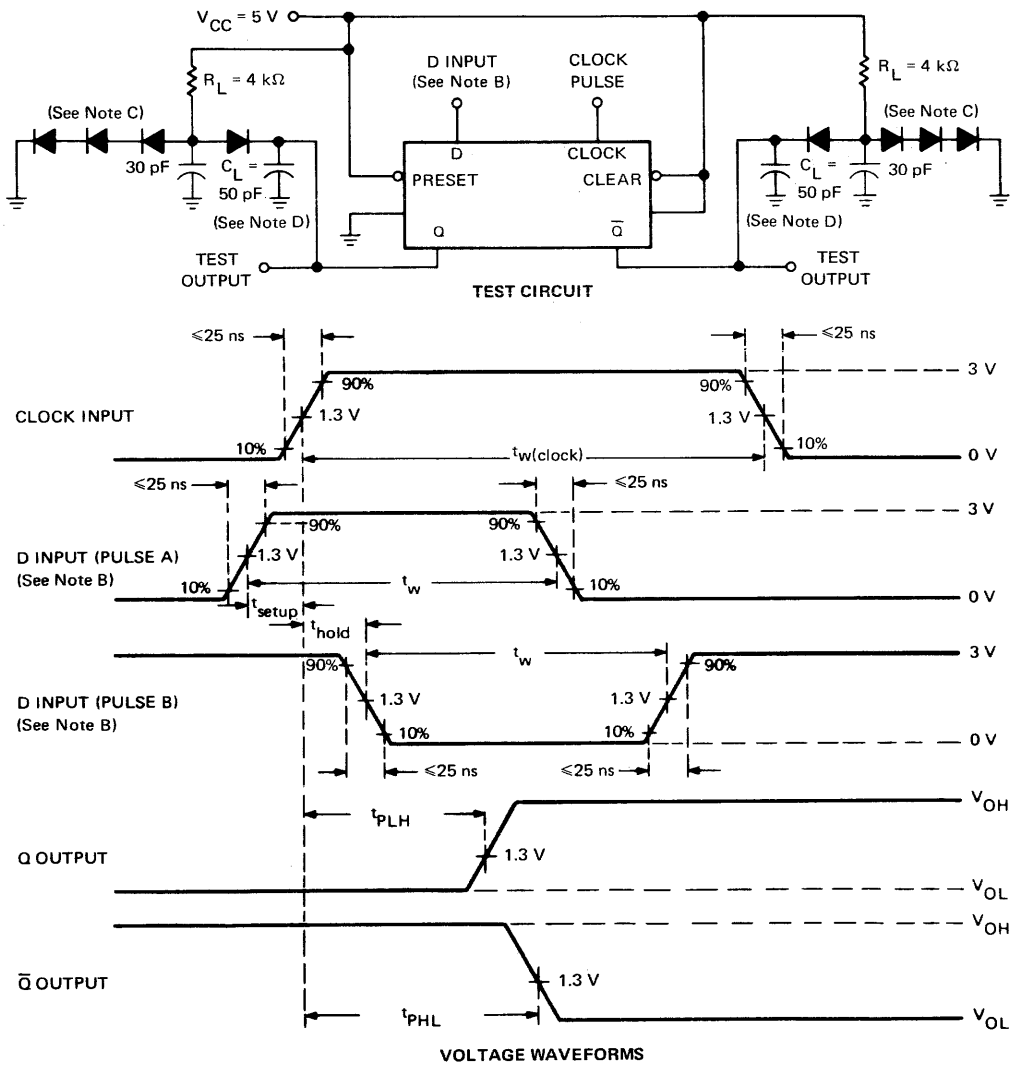
NOTES: A. Clear or preset inputs dominate regardless of the state of clock or logic inputs.
B. Clear or preset input pulse characteristics: $t_{w(clear)}$ = 100 ns, $t_{w(preset)}$ = 100 ns, and PRR = 500 kHz.
C. All diodes are 1N916.
D. C_L includes probe and jig capacitance.

FIGURE 30—S-R AND J-K FLIP-FLOP SWITCHING TIMES FROM ASYNCHRONOUS INPUTS

10

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



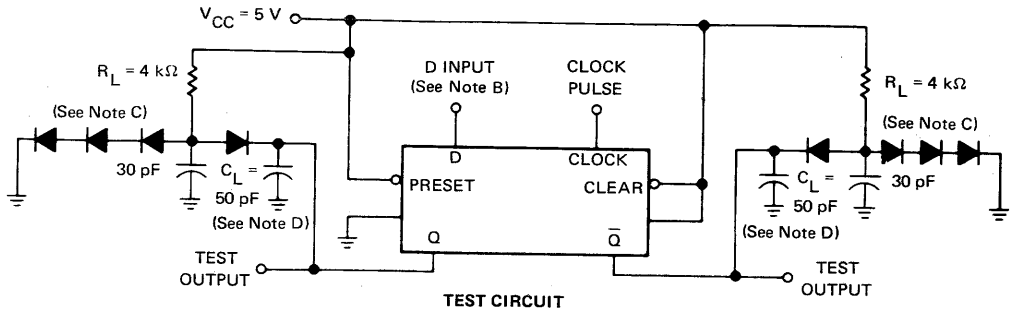
NOTES: A. Clock input pulse has the following characteristics: $t_{w(clock)}$ = 200 ns and PRR = 500 kHz. When testing f_{max}, vary PRR.
B. D input (pulse A) has the following characteristics: t_{setup} = 30 ns, t_w = 100 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 0 ns, t_w = 80 ns, and PRR is 50% of the clock PRR.
C. All diodes are 1N916.
D. C_L includes probe and jig capacitance.

FIGURE 31–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS (HIGH-LEVEL DATA)

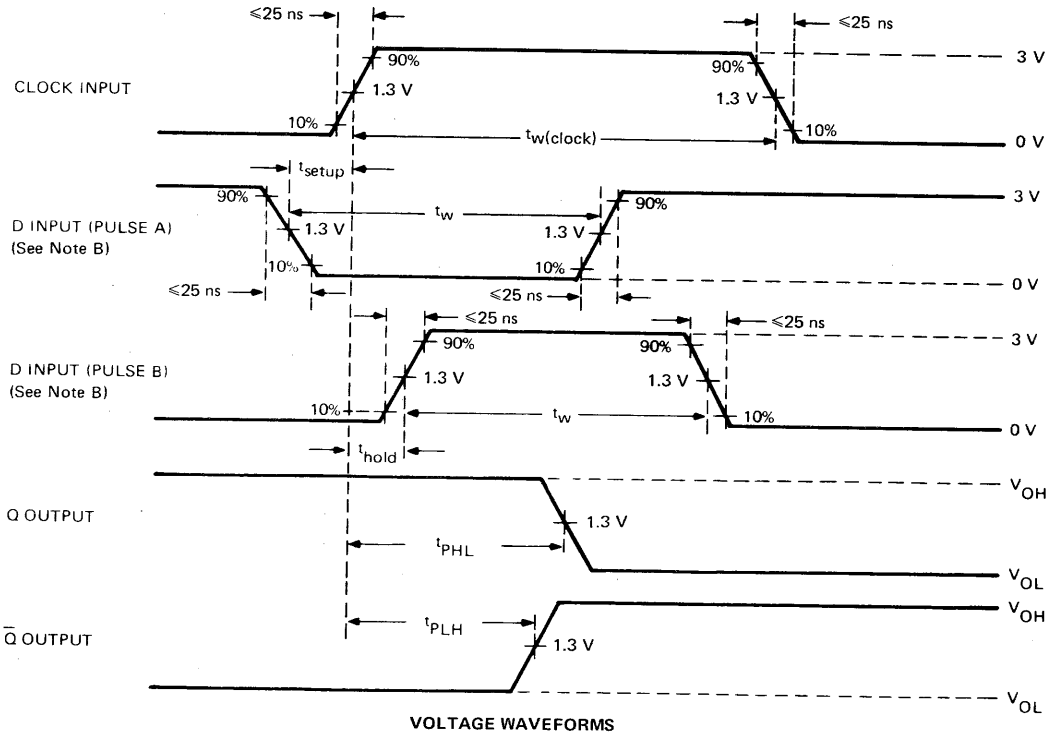
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

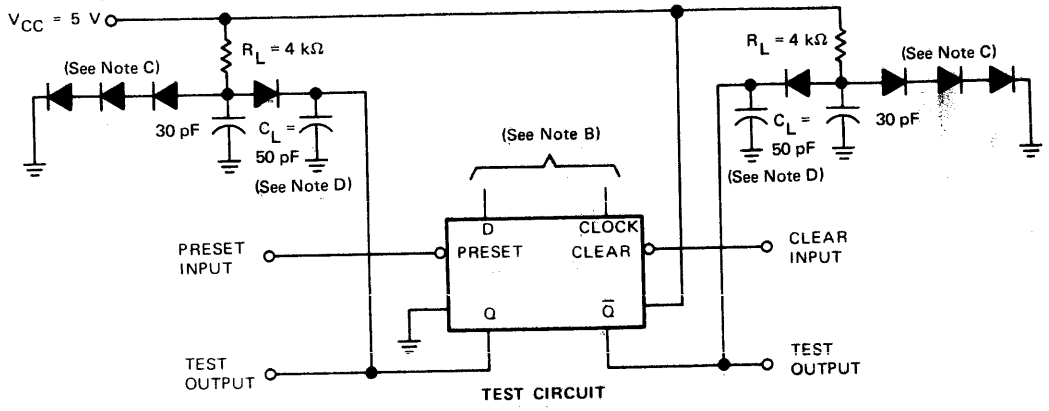
NOTES: A. Clock input pulse has the following characteristics: t_w = 200 ns and PRR = 500 kHz. When testing f_{max}, vary PRR.
B. D input (pulse A) has the following characteristics: t_{setup} = 30 ns, t_w = 100 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 0 ns, t_w = 80 ns, and PRR is 50% of the clock PRR.
C. All diodes are 1N916.
D. C_L includes probe and jig capacitance.

FIGURE 32–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS (LOW-LEVEL DATA)

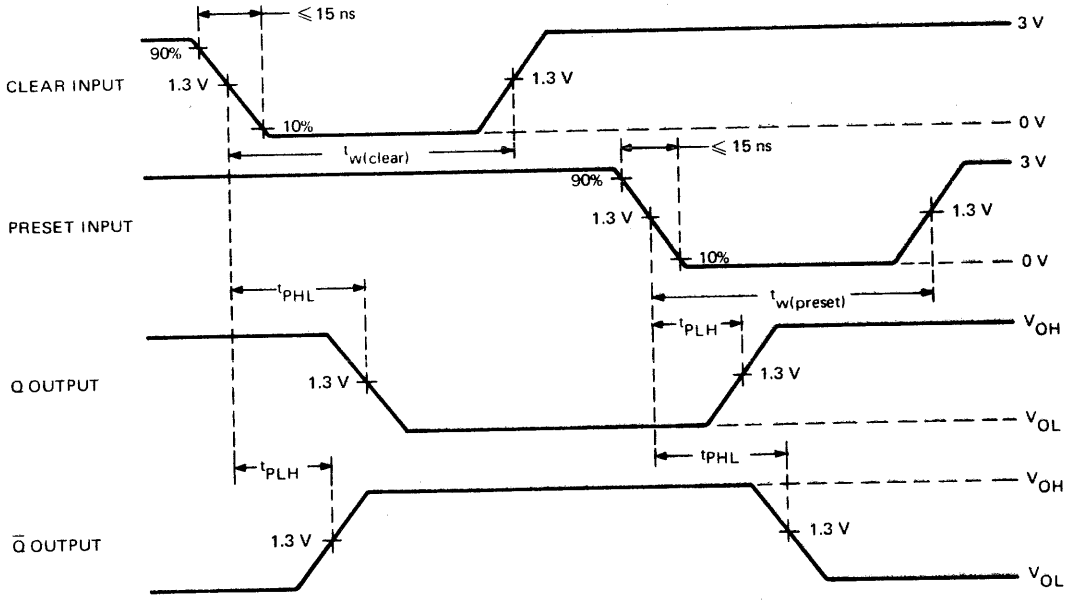
10

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Clear or Preset input pulse characteristics: $t_{w(clear)} = t_{w(preset)}$ = 100 ns, PRR = 500 kHz.
B. Clear and Preset inputs dominate regardless of the state of Clock or D inputs.
C. All diodes are 1N916.
D. C_L includes probe and jig capacitance.

FIGURE 33–ASYNCHRONOUS INPUTS SWITCHING CHARACTERISTICS

10

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

RSN55900—DUAL-CHANNEL PREAMPLIFIER
RSN55910—SWITCHED BUFFER
RSN55920—D-C COUPLED 4-CHANNEL SENSE AMPLIFIER

RSN55900 electrical characteristics at 25°C free-air temperature

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
I_{IB}	Input bias current				25	μA
I_{SL}	Low-level strobe current	V_S = 0 V			4	mA
A_{VD}	Large-signal differential voltage amplification	V_{ID} = 10 mV	100		200	
V_{OPP}	Maximum peak-to-peak output voltage swing		7			V
V_{OC}	Common-mode output voltage	V_I = 0 V	5		7	V
I_{CC1}	Supply current from V_{CC1}	V_{CC1} = 12 V			12	mA
I_{CC2}	Supply current from V_{CC2}	V_{CC2} = 5 V			15	mA
I_{EE}	Supply current from V_{EE}	V_{EE} = −10 V			−17	mA
t_{PLH}	Propagation time, low-to-high-level output			15		ns

RSN55910 electrical characteristics at 25°C free-air temperature

PARAMETER		SUPPLY MODE	CONDITIONS	MIN	MAX	UNIT
$V_{OH(\overline{Y})}$	High-level $\overline{Y}$ output voltage	1	V_{ID} = 40 mV	4.5		V
		2	V_{ID} = 85 mV	4.5		
$V_{OL(\overline{Y})}$	Low-level $\overline{Y}$ output voltage	1	V_{ID} = 300 mV		0.5	V
		2	V_{ID} = 400 mV		0.5	
I_{CC1}	Supply current from V_{CC1}	1	V_{CC1} = 12 V		5	mA
I_{CC2}	Supply current from V_{CC2}	1	V_{CC2} = 5 V		20	mA
I_{EE}	Supply current from V_{EE}	1	V_{EE} = −10 V		−17	mA
$t_{PHL(\overline{Y})}$	Propagation time, high-to-low-level $\overline{Y}$ output	1		8	28	ns
		2		8	35	
$t_{PLH(\overline{Y})}$	Propagation time, low-to-high-level $\overline{Y}$ output	1		10	45	ns
		2		10	46	

SUPPLY MODE	V_{CC1}	V_{CC2}	V_{CC3}	V_{EE}
1	12 V	5 V	OPEN	−10 V
2	GND	5 V	5 V	−10 V

All voltage values, except differential voltages, are with respect to the network ground terminal.

10

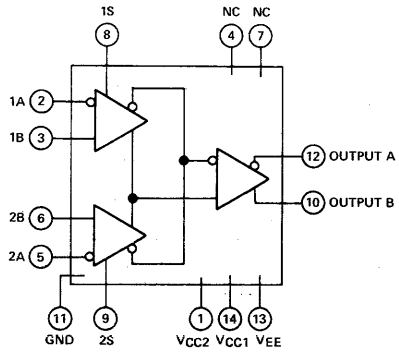
RSN55920 electrical characteristics at 25°C free-air temperature

PARAMETER		CONDITIONS	MIN	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V		2.5	mV
I_{IB}	Input bias current			100	μA
I_{SL}	Low-level strobe current	V_S = 0 V		1.38	mA
V_{OH}	High-level output voltage	V_{ID} = 50 mV	2.4		V
V_{OL}	Low-level output voltage	V_{ID} = −50 mV		0.45	V
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.5 V		30	mA
I_{EE}	Supply current from V_{EE}	V_{EE} = −6.6 V		−19	mA

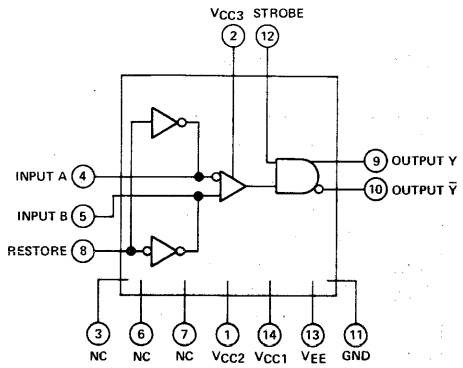
†All radiation tolerant integrated circuits are supplied in H flat packages. See Section 1 for dimensional drawings.

PRELIMINARY DATA: Supplementary data will be published at a later date.

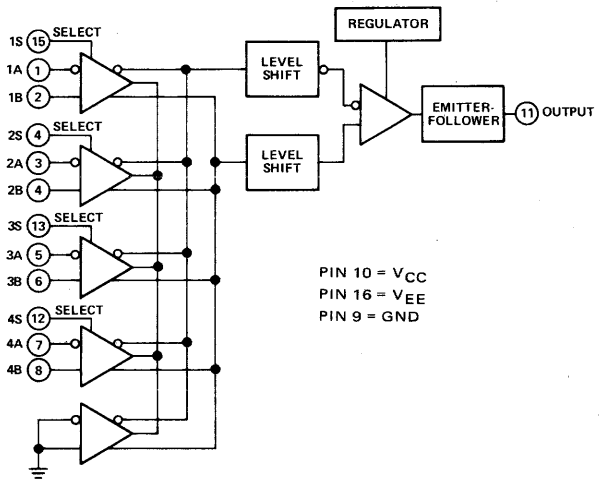
functional logic diagrams



RSN55900



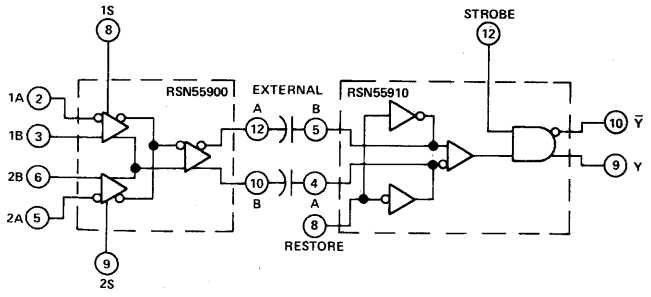
RSN55910



RSN55920

10

TYPICAL APPLICATION DATA



PIN	MIN	NOM	MAX
1	4.5 V	5 V	5.5 V
14	10.8 V	12 V	13.2 V
13	−11 V	−10 V	−9 V

PRINTED IN U.S.A.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

RADIATION TOLERANT DTL

These radiation-tolerant circuits are electrically similar to and functionally interchangeable with their Series 15930‡ counterparts. The terminal assignments are the same. They are mounted in the 14-pin H ceramic package and are intended for operation over the full military range of −55°C to 125°C.

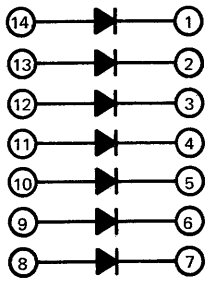
TYPE	FUNCTION
RSN15930	Expandable Dual 4-Input NAND Gate
RSN15932	Expandable Dual 4-Input NAND Buffer Gate
RSN15944	Expandable Dual 4-Input NAND Power Gate
RSN15945	J-K/R-S Flip-Flop
RSN15962	Triple 3-Input NAND Gate

typical characteristics at 25°C free-air temperature

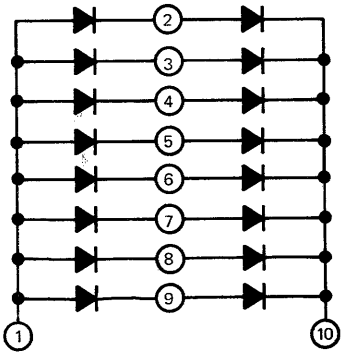
Propagation delay time	25 ns
Power dissipation	12 mW
D-c noise immunity	750 mV

RADIATION TOLERANT DIODE ARRAYS

RSN14925
7-DIODE ARRAY
14-PIN PACKAGE



RSN14097
16-DIODE ARRAY
10-PIN PACKAGE



10

electrical characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)}$	Reverse Breakdown Voltage	I_R = 10 μA	40			V
I_R	Static Reverse Current	V_R = 40 V			500	nA
V_F	Static Forward Voltage	I_F = 500 mA			1.5	V
		I_F = 100 mA	0.7		1	
C_T	Total Capacitance	V_R = 0, f = 1 MHz		12		pF

†All radiation tolerant devices are supplied in H flat packages. See Section 1 for dimensional drawings.
‡Refer to Section 11 for more complete data on Series 15930.

PRELIMINARY DATA:
Supplementary data will be published at a later date.

LINEAR INTEGRATED CIRCUIT

CIRCUIT TYPE RSN52709 RADIATION-HARDENED HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

featuring

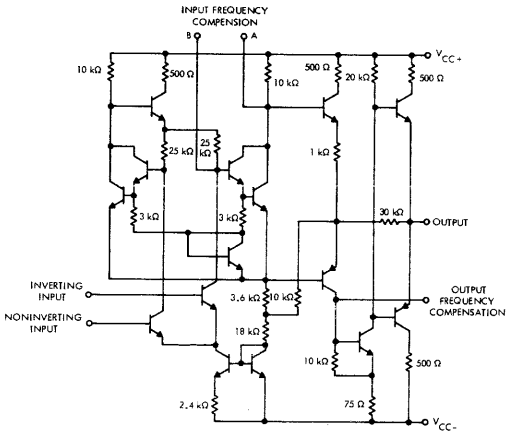
HIGH TOLERANCE TO GAMMA AND NEUTRON IRRADIATION

- **Input Voltage Range . . . ±8 V Min**
- **Maximum Peak-to-Peak Output Voltage Swing . . . 20 V Min**

description

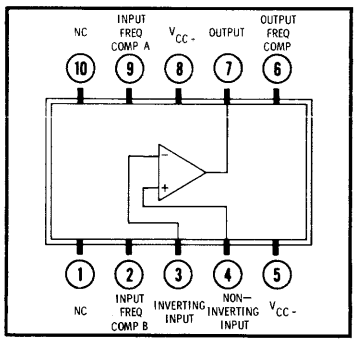
The RSN52 709 circuit is a radiation-hardened, high-performance operational amplifier specifically designed and fabricated for operation and survivability in a nuclear environment. Small-geometry transistors, shallow base diffusions, component matching, dielectric isolation, and thin-film resistors are utilized to improve performance and minimize sensitivity to gamma and neutron irradiation. Provisions are incorporated within the circuit whereby external components may be used to compensate the amplifier for stable operation under various feedback or load conditions. Definitive specifications are provided for electrical characteristics over the full military temperature range of -55°C to 125°C. Data on changes in device performance characteristics resulting from exposure to gamma or neutron irradiation is available at Texas Instruments upon demonstration of need-to-know and applicable security credentials.

schematic and terminal assignments



Component values shown are nominal.

H FLAT PACKAGE (TOP VIEW)



NC—No internal connection

10

For ordering instructions and mechanical data, refer to Section 1.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (See Note 1): V_{CC+} . . . . . 18 V
V_{CC-} . . . . . -18 V
Differential input voltage . . . . . ±5 V
Input voltage (either input, See Note 1) . . . . . ±10 V
Duration of short-circuit output current (T_A = 25°C) . . . . . 5 s
Continuous total power dissipation at (or below) 100°C free-air temperature (See Note 2) . . . . . 250 mW
Operating free-air temperature range (See Note 2) . . . . . -55°C to 125°C
Storage temperature range . . . . . -65°C to 150°C

NOTES: 1. These voltage values are with respect to the zero reference level of the supply voltage.
2. Derate linearly to 125°C free-air temperature at the rate of 5 mW/°C.

voltages specified

Unless otherwise noted, supply voltages specified in the following tables are V_{CC} = 9 V to 15 V, where a positive voltage within the specified range or of the specified value is applied to V_{CC+} and an equal negative voltage is applied to V_{CC-}. Unless otherwise noted, all voltages except V_{IO} are with respect to the zero reference level (ground) of the supply voltages.

electrical characteristics (unless otherwise noted, V_{CC} = 9 V to 15 V, T_A = 25°C)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IO}	Differential-input offset voltage	$R_s \leq 10$ kΩ,	T_A = -55°C to 125°C			6	mV
		$R_s \leq 10$ kΩ			1	5	mV
α_{VIO}	Differential-input offset voltage temperature coefficient	R_s = 50 Ω,	T_A = -55°C to 125°C		3		μV/°C
		$R_s \leq 10$ kΩ,	T_A = -55°C to 125°C		6		μV/°C
I_{IB}	Input bias current	V_{CC} = 15 V			100	500	nA
		V_{CC} = 15 V,	T_A = -55°C		120	1500	nA
I_{IO}	Differential-input offset current		T_A = 125°C		20	200	nA
					25	200	nA
			T_A = -55°C		30	500	nA
I_{IR}	Input reverse current	V_{ID} = 5 V				5	μA
V_{OPP}	Maximum peak-to-peak output voltage swing	V_{CC} = 15 V,	$R_L \geq 10$ kΩ, T_A = -55°C to 125°C	24			V
		V_{CC} = 15 V,	$R_L \geq 2$ kΩ, T_A = -55°C to 125°C	20			V
V_I	Input voltage range	V_{CC} = 15 V,	T_A = -55°C to 125°C	±8			V
A_{VD}	Large-signal open-loop differential voltage gain	V_{CC} = 15 V, V_O = ±10 V,	$R_L \geq 2$ kΩ, T_A = -55°C to 125°C	20,000	40,000‡	70,000	
CMRR	Common-mode rejection ratio	$R_s \leq 10$ kΩ,	T_A = -55°C to 125°C	70	90‡		dB
r_i	Input resistance		T_A = -55°C	40	100		kΩ
				150	400		kΩ
r_o	Output resistance				150		Ω
$\Delta V_{IO}/\Delta V_{CC}$	Supply voltage sensitivity	$R_s \leq 10$ kΩ,	T_A = -55°C to 125°C		25‡	150	μV/V
P_D	Total power dissipation	V_{CC} = 15 V,	V_O = 0		80	165	mW

† All typical values are at V_{CC} = 15 V.
‡ These typical values are at T_A = 25°C.

transient response, V_{CC} = 9 V to 15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Rise time	V_{in} = 20 mV,	C_L = open			1.5	μs
	Overshoot	V_{in} = 20 mV,	$C_L \leq$ 100 pF			30%	

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DTL Circuits Summary

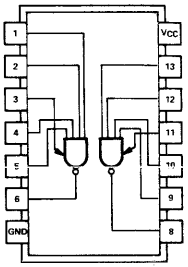
DTL
SMALL-SCALE INTEGRATION (SSI)

Function	Operating Temperature Ranges		Packages*		
	−55°C to 125°C	0°C to 75°C	Dual-In-Line		Flat
GATES WITH 6-kΩ PULL-UP RESISTORS					
Expandable Dual 4-Input NAND Gates	SN15930	SN15830	J	N	U
Quadruple 2-Input NAND Gates	SN15946	SN15846	J	N	U
Triple 3-Input NAND Gates	SN15962	SN15862	J	N	U
Dual 5-Input NAND Gates	SN151900	SN151800	J	N	U
Expandable 8-Input NAND Gates	SN151902	SN151802	J	N	U
10-Input NAND Gates	SN151904	SN151804	J	N	U
Quadruple 2-Input AND Gates	SN151906	SN151806	J	N	U
Quadruple 2-Input OR Gates	SN151908	SN151808	J	N	U
Quadruple 2-Input NOR Gates	SN151910	SN151810	J	N	U
Quadruple 2-Input Exclusive-OR Gates	SN151912	SN151812	J	N	U
GATES WITH 2-kΩ PULL-UP RESISTORS					
Quadruple 2-Input NAND Gates	SN15949	SN15849	J	N	U
Expandable Dual 4-Input NAND Gates	SN15961	SN15861	J	N	U
Triple 3-Input NAND Gates	SN15963	SN15863	J	N	U
Dual 5-Input NAND Gates	SN151901	SN151801	J	N	U
Expandable 8-Input NAND Gates	SN151903	SN151803	J	N	U
10-Input NAND Gates	SN151905	SN151805	J	N	U
Quadruple 2-Input AND Gates	SN151907	SN151807	J	N	U
Quadruple 2-Input OR Gates	SN151909	SN151809	J	N	U
Quadruple 2-Input NOR Gates	SN151911	SN151811	J	N	U
POWER/BUFFER GATES					
Expandable Dual 4-Input NAND Buffer Gates	SN15932	SN15832	J	N	U
Expandable Dual 4-Input NAND Power Gates	SN15944	SN15844	J	N	U
Quadruple 2-Input NAND Buffer Gates	SN15957	SN15857	J	N	U
Quadruple 2-Input NAND Power Gates	SN15958	SN15858	J	N	U
HEX INVERTERS					
6-kΩ Pull-Up Resistors	SN15934	SN15834	J	N	U
Expandable (Open-Base) or Translator Inputs	SN15935	SN15835	J	N	U
6-kΩ Pull-Up Resistors	SN15936	SN15836	J	N	U
2-kΩ Pull-Up Resistors	SN15937	SN15837	J	N	U
Open-Collector Outputs	SN15938	SN15838	J	N	U
EXPANDERS					
Dual 4-Input Expanders	SN15933	SN15833	J	N	U
FLIP-FLOPS					
Gated J-K/R-S (6-kΩ Pull-Up Resistors)	SN15931	SN15831	J	N	U
Gated J-K/R-S (6-kΩ Pull-Up Resistors)	SN15945	SN15845	J	N	U
Gated J-K/R-S (2-kΩ Pull-Up Resistors)	SN15948	SN15848	J	N	U
Pulse-Triggered Binary (Active Pull-Up)	SN15950	SN15850	J	N	U
Dual J-K, Individual Clocks and Presets (6-kΩ Pull-Up Resistors)	SN159093	SN158093	J	N	U
Dual J-K, Individual Clocks and Presets (2-kΩ Pull-Up Resistors)	SN159094	SN158094	J	N	U
Dual J-K, Common Clocks and Clears (2-kΩ Pull-Up Resistors)	SN159097	SN158097	J	N	U
Dual J-K, Common Clocks and Clears (6-kΩ Pull-Up Resistors)	SN159099	SN158099	J	N	U
MONOSTABLE MULTIVIBRATORS					
Gated, Negative-Edge-Triggered	SN15951	SN15851	J	N	U

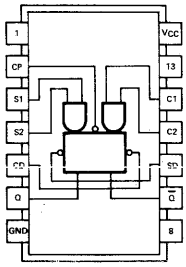
*For outline drawings of all packages, see Section 1.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

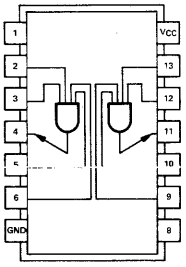
SN15830, SN15832, SN15844, SN15861, SN15930, SN15932, SN15944, SN15961



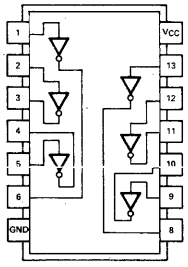
SN15831, SN15845, SN15848, SN15931, SN15945, SN15948, (See Truth Tables 1 and 2)



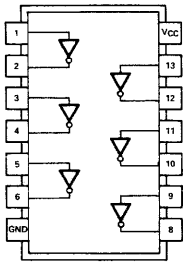
SN15833, SN15933



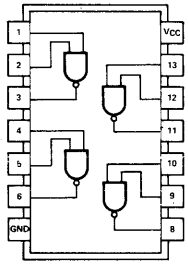
SN15834, SN15934



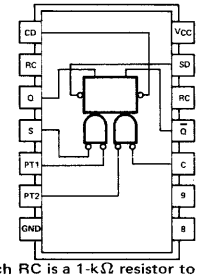
SN15835, SN15836, SN15837, SN15838, SN15935, SN15936, SN15937, SN15938



SN15846, SN15849, SN15946, SN15949

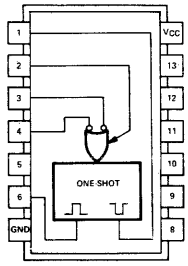


SN15850, SN15950 (See Truth Tables 3 and 4)



Each RC is a 1-kΩ resistor to V_{CC}.

SN15851, SN15951 (See Notes A, B, and C)



TRUTH TABLE 1
R-S MODE

t_n				t_{n+1}
S1	S2	C1	C2	Q
L	X	L	X	Qn
L	X	X	L	Qn
X	L	L	X	Qn
X	L	X	L	Qn
L	X	H	H	L
X	L	H	H	L
H	H	L	X	H
H	H	X	L	H
H	H	H	H	Indeterminate

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. H = high, L = low, X = irrelevant.
4. For operation in the J-K mode connect S2 to Q and C2 to $\overline{Q}$.

TRUTH TABLE 2
J-K MODE

t_n		t_{n+1}
S1	C1	Q
L	L	Qn
L	H	L
H	L	H
H	H	$\overline{Q}$n

TRUTH TABLE 3
SYNCHRONOUS

t_n PULSE INPUT				t_{n+1} OUTPUT	
S	C	PT1	PT2	Q	$\overline{Q}$
H	X	X	H	Qn	$\overline{Q}$n
X	H	H	X	Qn	$\overline{Q}$n
L	H	L	X	H	L
L	X	L	H	H	L
H	L	X	L	L	H
X	L	H	L	L	H
L	L	L	L	Indeterminate	

NOTES: 5. Logical levels shown for pulse inputs PT1 and PT2 indicate that a transition to that level has just occured.
6. Truth tables reflect individual conditions at the input. Either direct input may be used to inhibit its corresponding pulse input.

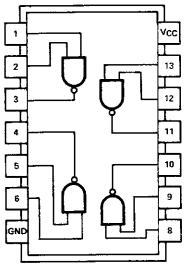
TRUTH TABLE 4
ASYNCHRONOUS

DIRECT INPUT		OUTPUT	
SD	CD	Q	$\overline{Q}$
H	H	Qn	$\overline{Q}$n
L	H	L	H
H	L	H	L
L	L	H	H

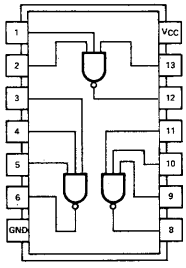
NOTES: A. External timing resistor may be connected between pins 14 and 10 to control pulse width.
B. External timing capacitor may be connected between pins 10 and 11 to control pulse width.
C. Input sensitivity can be decreased by adding a capacitor from pin 5 to ground.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

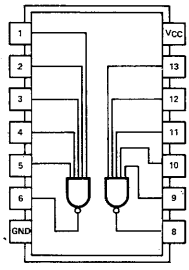
SN15857, SN15858,
SN15957, SN15958



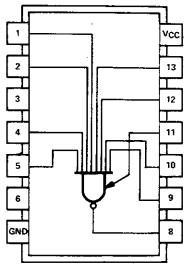
SN15862, SN15863,
SN15962, SN15963



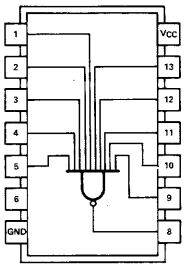
SN151800, SN151801,
SN151900, SN151901



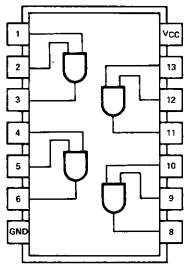
SN151802, SN151803,
SN151902, SN151903



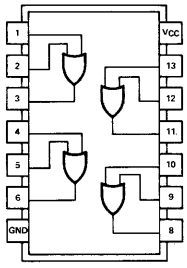
SN151804, SN151805,
SN151904, SN151905



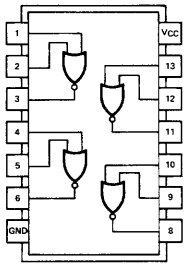
SN151806, SN151807,
SN151906, SN151907



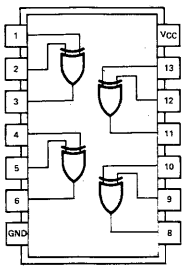
SN151808, SN151809,
SN151908, SN151909



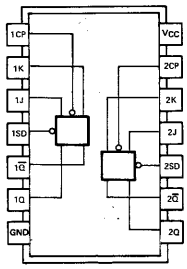
SN151810, SN151811,
SN151910, SN151911



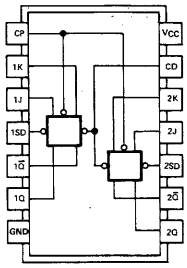
SN151812,
SN151912



SN158093, SN158094,
SN159093, SN159094
(See Truth Table 5)



SN158097, SN158099,
SN159097, SN159099
(See Truth Table 5)



TRUTH TABLE 5

t_n		t_{n+1}
J	K	Q
L	L	Qn
L	H	L
H	L	H
H	H	$\bar{Q}n$

11

SERIES 15830 GATES, EXPANDER, AND ONE-SHOT

electrical and switching characteristics (unless otherwise noted, V_{CC} = 5 V)

PARAMETER	CONDITIONS	T_A(°C)	SN15830 SN15834 SN15836 SN15846 SN15862 SN151800 SN151802 SN151804		SN15832 SN15857		SN15833		SN15835		SN15837 SN15849 SN15861 SN15863 SN151801 SN151803 SN151805		SN15838		SN15844 SN15858		SN15851		SN151806		SN151807		SN151808		SN151809		SN151810		SN151811		SN151812		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL}	I_O = I_{OL} MIN	0 and 25		0.45		0.45				0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45	V
		75		0.5		0.5				0.5		0.5		0.5		0.5		0.5		0.5		0.5		0.5		0.5		0.5		0.5		0.5	
V_{OH}	I_O = I_{OH} MIN	0 and 25	2.6		2.6				2.6		3.8		6[1,2]		6[1,2]		2.6		2.6		2.6		2.6		2.6		2.6		2.6		2.6		2.6	V
		75	2.5		2.5				2.5		3.7						2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		
V_{IL}		0		1.2		1.2				2.1		1.2		1.2		1.2				1.2		1.2		1.2		1.2		1.2		1.2		1.2	V
		25		1.1		1.1				1.92		1.1		1.1		1.1	See Note A			1.1		1.1		1.1		1.1		1.1		1.1		1.1	
		75		0.95		0.95				1.7		0.95		0.95		0.95				0.95		0.95		0.95		0.95		0.95		0.95		0.95	
V_{IH}		0	2		2						2		2		2				2		2		2		2		2		2		2		V
		25	1.9		1.9						1.9		1.9		1.9		See Note A		1.9		1.9		1.9		1.9		1.9		1.9		1.9		
		75	1.8		1.8						1.8		1.8		1.8				1.8		1.8		1.8		1.8		1.8		1.8		1.8		
I_{OL}	V_O = V_{OL} MAX	0 and 25	12		36				12		10.6		12		40		15		12		11		12		11		12		11		12		mA
		75	11.4		34				11.4		10.2		11.4		36		14.5		11.4		10.4		11.4		10.4		11.4		10.4		11.4		
I_{OH}	V_O = V_{OH} MIN	0	−0.12		−2.0				−0.12		−0.12						−0.18		−0.12		−0.5		−0.12		−0.5		−0.12		−0.5		−0.12		mA
		25	−0.12		−2.5				−0.12		−0.12						−0.18		−0.12		−0.5		−0.12		−0.5		−0.12		−0.5		−0.12		
		75	−0.12		−3.0				−0.12		−0.12						−0.18		−0.12		−0.5		−0.12		−0.5		−0.12		−0.5		−0.12		
I_{OS}	V_O = 0 V	0		−1.3	−15					−1.3										−1.3		−3.9		−1.3		−3.9		−1.3		−3.9		−1.3	mA
		25		−1.3	−16					−1.3		−3.68								−1.3		−3.9		−1.3		−3.9		−1.3		−3.9		−1.3	
		75		−1.25	−14					−1.25										−1.25		−3.75		−1.25		−3.75		−1.25		−3.75		−1.25	
I_{IL}	V_I = V_{OL} MAX	0 and 25		−1.4		−1.4				−1.4[3]		−1.4		−1.4		−1.4	−1.35	−2.8		−1.4		−1.4		−1.4		−1.4		−1.4		−1.4		−2.8	mA
		75		−1.33		−1.33				−1.33[3]		−1.33		−1.33		−1.33	−1.25	−2.63		−1.33		−1.33		−1.33		−1.33		−1.33		−1.33		−2.67	
I_{IH}	V_I = 4 V	0 and 25		5		5		5				5		5		5		5		5		5		5		5		5		5		10	μA
		75		10		10		10				10		10		10		10		10		10		10		10		10		10		20	
V_F	I_F = 2 mA	0					0.75	0.9																									V
		25					0.68	0.82																									
		75					0.6	0.75																									
I_{CCL}	AVG. PER GATE	25		4		15				4		4		4		12		12	5.75		7.75		7.25		9.38		5.5		7.65		9.75	mA
I_{CCH}	AVG. PER GATE, V_{CC} = 8 V	25		4		4				4		4		4		4		26.7[4]	9.75		9.75		14.25		14.25		5.62		4.87		13.25	mA
t_{PHL}		25	10	30	15	40			10	30	10	30	10	30	10	35	5	50	15	65	15	65	15	65	15	65	10	30	10	30	25	80	ns
t_{PLH}		25	25	80	25	80			25	80	15	60	25	80	15	50	5	50	25	80	15	65	25	90	15	75	25	90	15	75	25	80	ns

(1) 25°C only.
(2) For the SN15838, SN15844, and SN15858, V_{OH} is measured at 5 mA.
(3) V_I = 1.35 V at T_A at 0°C, 1.27 V at T_A = 25°C, and 1.25 V at T_A = 70°C.
(4) For the SN15851, total quiescent values of I_{CC} are given for V_{CC} = 5 V and V_{CC} = 8 V.

NOTE A: This monostable multivibrator is triggered with a negative-going transition ≥ 1 volt having a fall time ≤ 25 ns/volt.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES 15930 GATES, EXPANDER, AND ONE-SHOT

electrical and switching characteristics (unless otherwise noted, V_{CC} = 5 V)

PARAMETER	CONDITIONS	T_A(°C)	SN15930, SN15934, SN15936, SN15946, SN15962, SN151900, SN151902, SN151904		SN15932, SN15957		SN15933		SN15935		SN15937, SN15949, SN15961, SN15963, SN151901, SN151903, SN151905		SN15938		SN15944, SN15958		SN15951		SN151906		SN151907		SN151908		SN151909		SN151910		SN151911		SN151912		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL}	$I_O = I_{OL}$ MIN	−55 and 25		0.4		0.4				0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4	V
		125		0.45		0.45				0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45	
V_{OH}	$I_O = I_{OH}$ MIN	−55	2.5		2.5				2.5		3.8						2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		V
		25	2.6		2.6				2.6		3.8		6(1,2)		6(1,2)		2.6		2.6		2.6		2.6		2.6		2.6		2.6		2.6		
		125	2.5		2.5				2.5		3.7						2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		
V_{IL}		−55		1.4		1.4				2.38		1.4		1.4		1.4				1.4		1.4		1.4		1.4		1.4		1.4		1.4	V
		25		1.1		1.1				1.92		1.1		1.1		1.1	See Note A			1.1		1.1		1.1		1.1		1.1		1.1		1.1	
		125		0.8		0.8				1.45		0.8		0.8		0.8				0.8		0.8		0.8		0.8		0.8		0.8		0.8	
V_{IH}		−55	2.1		2.1						2.1		2.1		2.1				2.1		2.1		2.1		2.1		2.1		2.1		2.1		V
		25	1.9		1.9						1.9		1.9		1.9		See Note A		2		2		2		2		2		2		2		
		125	1.7		1.7						1.7		1.7		1.7				2		2		2		2		2		2		2		
I_{OL}	$V_O = V_{OL}$ MAX	−55	11.4		34				11.4		10		11.4		36		15		11.4		10.4		11.4		10.4		11.4		10.4		11.4		mA
		25	12		36				12		10.6		12		40		15		12		11		12		11		12		11		12		
		125	10.8		32				10.8		9.5		10.8		36		14		10.8		9.8		10.8		9.8		10.8		9.8		10.8		
I_{OH}	$V_O = V_{OH}$ MIN	−55	−0.12		−2				−0.12		−0.12						−0.18		−0.12		−0.5		−0.12		−0.5		−0.12		−0.5		−0.12		mA
		25	−0.12		−2.5				−0.12		−0.12						−0.18		−0.12		−0.5		−0.12		−0.5		−0.12		−0.5		−0.12		
		125	−0.12		−3				−0.12		−0.12						−0.18		−0.12		−0.5		−0.12		−0.5		−0.12		−0.5		−0.12		
I_{OS}	V_O = 0 V	−55 and 25		−1.34	−18					−1.34		−2.1(1) −3.7								−1.34		−4		−1.34		−4		−1.34		−4		−1.34	mA
		125		−1.3	−16					−1.3		−3.28								−1.3		−3.9		−1.3		−3.9		−1.3		−3		−1.3	
I_{IL}	V_I = 0 V	−55 and 25		−1.6		−1.6				−1.6(3)		−1.6		−1.6		−1.6	−1.6	−3.1		−1.6		−1.6		−1.6		−1.6		−1.6		−1.6		−3.2	mA
		125		−1.5		−1.5				−1.5(3)		−1.5		−1.5		−1.5	−1.4	−3		−1.5		−1.5		−1.5		−1.5		−1.5		−1.5		−3	
I_{IH}	V_I = 4 V	−55 and 25		2		2		2				2		2		2		2		2		2		2		2		2		2		4	μA
		125		5		5		5				5		5		5		5		5		5		5		5		5		5		10	
V_F	I_F = 2 mA	−55					0.85	0.98																									V
		25					0.7	0.82																									
		125					0.5	0.65																									
I_{CCL}	AVG. PER GATE	25		3.25		13.3				3.25		3.25		3.25		10		9 (4)		4.88		7.25		6.25		8.38		5		6.9		8.5	mA
I_{CCH}	AVG. PER GATE, V_{CC} = 8 V	25		2.75		3				2.75		2.75		2.75		3		20		8.5		8.5		12.5		12.5		4.87		4.87		11.25	mA
t_{PHL}		25	10	30	15	40			10	30	10	30	10	30	10	35	5	50	15	65	15	65	15	65	15	65	10	30	10	30	25	80	ns
t_{PLH}		25	25	80	25	80			25	80	15	60	25	80	15	50	5	50	25	80	15	65	25	90	15	75	25	90	15	75	25	80	ns

(1) 25°C only.
(2) For the SN15938, SN15944, and SN15958, V_{OH} is measured at 5 mA.
(3) V_I = 0.98 V at T_A = −55°C, 0.82 V at T_A = 25°C, and 0.65 V at T_A = 125°C.
(4) For the SN15951, total quiescent values of I_{CC} are given for V_{CC} = 5 V and V_{CC} = 8 V.

NOTE A: This monostable multivibrator is triggered with a negative-going transition ≥ 1 volt having a fall time ≤ 25 ns/volt.

SERIES 15830 DTL FLIP-FLOPS

electrical and switching characteristics (unless otherwise noted, V_{CC} = 5)

PARAMETER	CONDITIONS		T_A(°C)	SN15831 MIN	SN15831 MAX	SN15845 MIN	SN15845 MAX	SN15848 MIN	SN15848 MAX	SN15850 MIN	SN15850 MAX	SN158093 MIN	SN158093 MAX	SN158094 MIN	SN158094 MAX	SN158097 MIN	SN158097 MAX	SN158099 MIN	SN158099 MAX	UNIT
V_{OL}	$I_O = I_{OL}$ MIN		0 and 25		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45	V
			75		0.5		0.5		0.5		0.5		0.5		0.5		0.5		0.5	
V_{OH}	$I_O = I_{OH}$ MIN		0 and 25	2.6		2.6		3.8		2.6		2.6		3.8		3.8		2.6		V
			75	2.5		2.5		3.7		2.5		2.5		3.7		3.7		2.5		
V_{IL}			0		1.2		1.2		1.2		1.2		1.2		1.2		1.2		1.2	V
			25		1.1		1.1		1.1		1.1		1.1		1.1		1.1		1.1	
			75		0.95		0.95		0.95		0.95		0.95		0.95		0.95		0.95	
V_{IH}			0	2		2		2		2		2		2		2		2		V
			25	1.9		1.9		1.9		1.9		1.9		1.9		1.9		1.9		
			75	1.8		1.8		1.8		1.8		1.8		1.8		1.8		1.8		
I_{OL}	$V_O = V_{OL}$ MAX		0 and 25	10.5		16.8		15.4		12		16.8		15.4		15.4		16.8		mA
			75	10.2		16		14.6		11.4		16		14.6		14.6		16		
I_{OH}	$V_O = V_{OH}$ MIN		0, 25, and 75	−0.12		−0.12		−0.12		−1.5		−0.12		−0.12		−0.12		−0.12		mA
I_{OS}	V_O = 0 V		0			−0.59	−1.41	−1.77	−4.2	−13.7	−29									mA
			25			−0.59	−1.41	−1.77	−4.2	−13.7	−29		−2.36		−5.15		−5.15		−2.36	
			75			−0.55	−1.38	−1.6	−4	−12.6	−28									
I_{IL}	$V_I = V_{OL}$ MAX	DATA INPUTS	0 and 25		−1.05		−0.95		−0.95		−2.1		−0.95		−0.95		−0.95		−0.95	mA
			75		−1		−0.9		−0.9		−2		−0.9		−0.9		−0.9		−0.9	
		CLOCK INPUT	0 and 25		−2.8		−2.8		−2.24				−2.8		−2.8		−5.6		−5.6	mA
			75		−2.67		−2.67		−2.13				−2.67		−2.67		−5.34		−5.34	
		PRESET or CLEAR INPUT	0 and 25		−0.95		−2.1		−2.1		−1.6		−2.8		−2.8	(1)	−2.8	(1)	−2.8	mA
			75		−0.9		−2		−2		−1.52		−2.67		−2.67		−2.67		−2.67	
I_{IH}	V_I = 4 V	DATA INPUTS	0 and 25		5		5		5		5		5		5		5		5	μA
			75		10		10		10		10		10		10		10		10	
		CLOCK INPUT	0 and 25		30		20		20				20		20		40		40	μA
			75		40		30		30				30		30		60		60	
		PRESET or CLEAR INPUT	0 and 25		5		5		5		5		5		5	(1)	5	(1)	5	μA
			75		10		10		10		10		10		10		10		10	
I_{CC}			25		14		16		17.5		9.3		32		35		35		32	mA
	V_{CC} = 8 V		25		18		18.5		22.5		19.6		37		45		45		37	mA
t_{PHL}	FROM CLOCK TO OUTPUT		25	35	75	15	75	15	65	5	32	15	75	15	65	15	65	15	75	ns
t_{PLH}	FROM CLOCK TO OUTPUT		25	35	75	25	75	25	75	5	25	25	75	25	75	25	75	25	75	ns

(1) Double the limit for the common clear input.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES 15930 DTL FLIP-FLOPS

electrical and switching characteristics (unless otherwise noted, V_{CC} = 5)

PARAMETER	CONDITIONS		T_A(°C)	SN15931 MIN	SN15931 MAX	SN15945 MIN	SN15945 MAX	SN15948 MIN	SN15948 MAX	SN15950 MIN	SN15950 MAX	SN159093 MIN	SN159093 MAX	SN159094 MIN	SN159094 MAX	SN159097 MIN	SN159097 MAX	SN159099 MIN	SN159099 MAX	UNIT
V_{OL}	$I_O = I_{OL}$ MIN		−55 and 25		0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4	V
			125		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45	
V_{OH}	$I_O = I_{OH}$ MIN		−55	2.5		2.5		3.8		3.8		2.5		3.8		3.8		2.5		V
			25	2.6		2.6		3.8		3.8		2.6		3.8		3.8		2.6		
			125	2.5		2.5		3.7		3.7		2.5		3.7		3.7		2.5		
V_{IL}			−55		1.1		1.4		1.4		1.4		1.4		1.4		1.4		1.4	V
			25		0.95		1.1		1.1		1.1		1.1		1.1		1.1		1.1	
			125		0.75		0.8		0.8		0.8		0.8		0.8		0.8		0.8	
V_{IH}			−55	2.1		2.1		2.1		2.1		2.1		2.1		2.1		2.1		V
			25	1.9		1.9		1.9		1.9		1.9		1.9		1.9		1.9		
			125	1.7		1.7		1.7		1.7		1.7		1.7		1.7		1.7		
I_{OL}	$V_O = V_{OL}$ MAX		−55	10		14.6		13		11.4		14.6		13		13		14.6		mA
			25	10.6		15.2		13.6		12		15.2		13.6		13.6		15.2		
			125	9.5		13.8		12.3		10.8		13.8		12.3		12.3		13.8		
I_{OH}	$V_O = V_{OH}$ MIN		−55	−0.12		−0.12		−0.12		−1.5		−0.12		−0.12		−0.12		−0.12		mA
			25	−0.12		−0.12		−0.12		−1.5		−0.12		−0.12		−0.12		−0.12		
			125	−0.12		−0.12		−0.12		−1.5		−0.12		−0.12		−0.12		−0.12		
I_{OS}	V_O = 0 V		−55 and 25			−0.7	−1.33	−2.1	−3.96	−15.7	−27	−0.7(1)	−2.4(1)	−2.1(1)	−5(1)	−2.1(1)	5(1)	−0.7(1)	−2.4(1)	mA
			125			−0.62	−1.3	−1.86	−3.54	−14.6	−26									
I_{IL}	V_I = 0 V	DATA INPUTS	−55 and 25		−1.07		−1.07		−1.07		−2.4		−1.07		−1.07		−1.07		−1.07	mA
			125		−1		−1		−1		−2.25		−1		−1		−1		−1	
		CLOCK INPUT	−55 and 25		−3.4		−3.2		−2.56				−3.2		−3.2		−6.4		−6.4	mA
			125		−3		−2.8		−2.2				−3		−3		−6.0		−6.0	
		PRESET or CLEAR INPUT	−55		−1.2		−2.4		−2.4		−1.82		−3.2		−3.2	(2)	−3.2	(2)	−3.2	mA
			25		−1.2		−2.4		−2.4		−1.82		−3.2		−3.2		−3.2		−3.2	
			125		−1.1		−2.1		−2.1		−1.62		−3.0		−3.0		−3.0		−3.0	
I_{IH}	V_I = 4 V	DATA INPUTS	−55 and 25		2		2		2		2		2		2		2		2	μA
			125		5		5		5		5		5		5		5		5	
		CLOCK INPUT	−55 and 25		20		10		10				10		10		20		20	μA
			125		30		20		20				20		20		40		40	
		PRESET or CLEAR INPUT	−55 and 25		2		2		2		2		2		2	(2)	2	(2)	2	μA
			125		5		5		5		5		5		5		5		5	
I_{CC}			25		11		14		16.2		8.7		28		32		32		28	mA
	V_{CC} = 8 V		25		14.5		17		21.6		18.4		34		42		42		34	mA
t_{PHL}	FROM CLOCK TO OUTPUT		25	35	75	15	75	15	65	5	32	15	75	15	65	15	65	15	75	ns
t_{PLH}	FROM CLOCK TO OUTPUT		25	35	75	25	75	25	75	5	25	25	75	25	75	25	75	25	75	ns

(1) 25°C only.
(2) Double the limit shown for common clear inputs.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Series SNF/SNG Circuits Summary

SERIES SNG GATES*

FUNCTIONS	OPERATING TEMPERATURE RANGE −55°C to 125°C	FAN-OUT	OPERATING TEMPERATURE RANGE 0°C to 75°C	FAN-OUT	PACKAGES‡		
					Dual-In-Line		Flat
Dual 4-Input NAND Gates	SNG40 SNG41	15 7	SNG42 SNG43	12 6	J	N	U
Expandable 2-2-2-3-Input AND-OR-INVERT Gates	SNG50 SNG51	15 7	SNG52 SNG53	12 6	J	N	U
8-Input NAND Gates	SNG60 SNG61	15 7	SNG62 SNG63	12 6	J	N	U
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gates	SNG70 SNG71	15 7	SNG72 SNG73	12 6	J	N	U
Dual Pulse Shaper/Delay AND Gates	SNG80 SNG81	15 7	SNG82 SNG83	12 6	J	N	U
2-Wide 3-Input AND-OR-INVERT Gates with 2-Input Gated Complement	SNG90 SNG91	15 7	SNG92 SNG93	12 6	J	N	U
Expandable 3-Wide 3-Input AND-OR-INVERT Gates	SNG100 SNG101	15 7	SNG102 SNG103	12 6	J	N	U
Expandable 2-Wide 4-Input AND-OR-INVERT Gates	SNG110 SNG111	15 7	SNG112 SNG113	12 6	J	N	U
Expandable 8-Input NAND Gates	SNG120 SNG121	15 7	SNG122 SNG123	12 6	J	N	U
Dual 4-Input Line Drivers	SNG130 SNG131	30 15	SNG132 SNG133	24 12	J	N	U
Quadruple 2-Input NAND Gates	SNG140 SNG141	15 7	SNG142 SNG143	12 6	J	N	U
3-2-2-3-Input Expanders for AND-OR-INVERT Gates	SNG150 SNG151		SNG152 SNG153		J	N	U
Triple 2-Input NAND Drivers	SNG160 SNG161	15 7	SNG162 SNG163	12 6	J	N	U
Dual 4-Input Expanders for AND-OR-INVERT Gates	SNG170 SNG171		SNG172 SNG173		J	N	U
Dual 4-Input Expanders for NAND Gates	SNG180 SNG181		SNG182 SNG183		J	N	U
Triple 3-Input NAND Gates	SNG190 SNG191	15 7	SNG192 SNG193	12 6	J	N	U
Expandable 8-Input NAND Gates	SNG200 SNG201	11 6	SNG202 SNG203	9 5	J	N	U
Expandable 2-Wide 4-Input AND-OR-INVERT Gates	SNG210 SNG211	11 6	SNG212 SNG213	9 5	J	N	U
Quadruple 2-Input NAND Gates	SNG220 SNG221	11 6	SNG222 SNG223	9 5	J	N	U
3-2-2-3-Input Expanders for AND-OR-INVERT Gates	SNG230 SNG231		SNG232 SNG233		J	N	U
Dual 4-Input NAND Gates	SNG240 SNG241	11 6	SNG242 SNG243	9 5	J	N	U
Expandable 2-2-2-3-Input AND-OR-INVERT Gates	SNG250 SNG251	11 6	SNG252 SNG253	9 5	J	N	U
8-Input NAND Gates	SNG260 SNG261	11 6	SNG262 SNG263	9 5	J	N	U
Dual 4-Input Expanders for AND-OR-INVERT Gates	SNG270 SNG271		SNG272 SNG273		J	N	U
OR-Expandable Dual 4-Input AND Gates	SNG280 SNG281	15 7	SNG282 SNG283	12 6	J	N	U
Dual 2-3-Input Expanders for OR Expandable AND Gates	SNG290 SNG291		SNG292 SNG293		J	N	U
Expandable 3-Wide 3-Input AND-OR-INVERT Gates	SNG300 SNG301	11 6	SNG302 SNG303	9 5	J	N	U
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gates	SNG310 SNG311	11 6	SNG312 SNG313	9 5	J	N	U
Triple 3-Input NAND Gates	SNG320 SNG321	11 6	SNG322 SNG323	9 5	J	N	U
Quadruple 2-Input NAND Lamp/Line Drivers	SNG351	30	SNG353	24	J	N	U

*Interchangeable with SUHL 1† and SUHL 2† TTL circuits
†Trademark of Sylvania Electric Products, Inc.
‡For outline drawings of all packages, see Section 1.

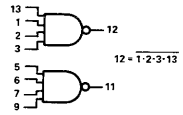
12

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

GATES

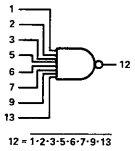
Pin 4 is V_{CC}, pin 10 is GND

SNG40, 41, 42, 43
SNG240, 241, 242, 243



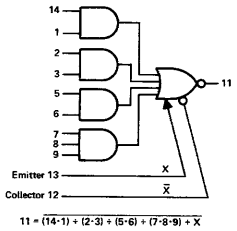
Dual 4-Input NAND Gates

SNG60, 61, 62, 63
SNG260, 261, 262, 263



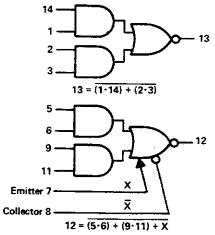
8-Input NAND Gates

SNG50, 51, 52, 53
SNG250, 251, 252, 253



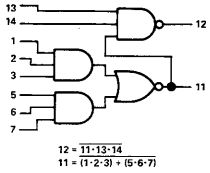
Expandable 2-2-2-3-Input
AND-OR-INVERT Gates

SNG70, 71, 72, 73
SNG310, 311, 312, 313



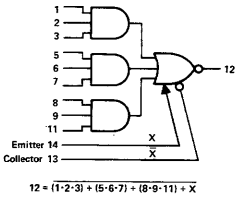
Expandable 2-Wide 2-Input
AND-OR-INVERT Gates

SNG90, 91, 92, 93



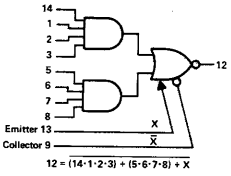
2-Wide 3-Input AND-OR-INVERT Gates
with 2-Input Gated Compliment

SNG100, 101, 102, 103
SNG300, 301, 301, 303



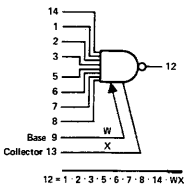
Expandable 3-Wide 3-Input
AND-OR-INVERT Gates

SNG110, 111, 112, 113
SNG210, 211, 212, 213



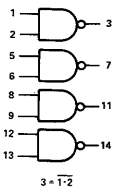
Expandable 2-Wide 4-Input
AND-OR-INVERT Gates

SNG120, 121, 122, 123
SNG200, 201, 202, 203



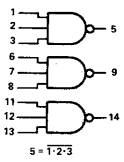
Expandable 8-Input NAND Gates

SNG140, 141, 142, 143
SNG220, 221, 222, 223



Quadruple 2-Input NAND Gates

SNG190, 191, 192, 193
SNG320, 321, 322, 323



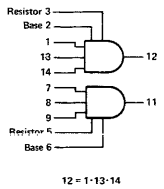
Triple 3-Input NAND Gates

12

SERIES SNF/SNG
TTL INTEGRATED CIRCUITS

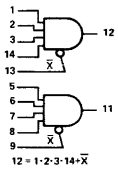
GATES (continued)

SNG80, 81, 82, 83



Dual Pulse Shaper/Delay AND Gates

SNG280, 281, 282, 283

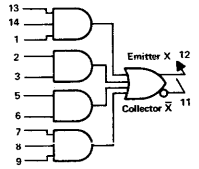


OR-Expandable Dual 4-Input AND Gates

EXPANDERS

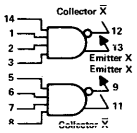
Pin 4 is V_{CC}, pin 10 is GND

SNG150, 151, 152, 153
SNG230, 231, 232, 233



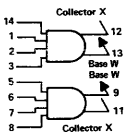
3-2-2-3 Input Expanders for A-O-I Gates

SNG170, 171, 172, 173
SNG270, 271, 272, 273



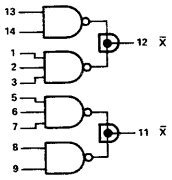
Dual 4-Input Expanders for A-O-I Gates

SNG180, 181, 182, 183



Dual 4-Input Expanders for NAND Gates

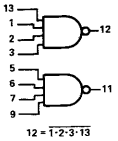
SNG290, 291, 292, 293



Dual 2-3 Input Expanders for OR-Expandable AND Gates

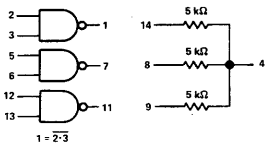
DRIVERS

SNG130, 131, 132, 133, 134



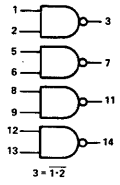
Dual 4-Input Line Drivers

SNG160, 161, 162, 163



Triple 2-Input NAND Drivers

SNG351, 353



Quadruple 2-Input NAND Lamp/Line Drivers

12

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics (unless otherwise noted, V_{CC} = 5 V)

PARAMETER	CONDITIONS	T_A†	SNG40, 41 SNG50, 51 SNG60, 61 SNG90, 91 SNG100, 101 SNG110, 111 SNG120, 121 SNG140, 141 SNG190, 191		SNG200, 201 SNG210, 211 SNG220, 221 SNG240, 241 SNG250, 251 SNG260, 261 SNG300, 301 SNG310, 311 SNG320, 321		SNG130, 131		SNG150, 151 SNG170, 171		SNG160, 161		SNG180, 181		SNG230, 231		SNG270, 271		SNG290, 291		SNG351		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{IL}	V_{IL} = 0 V	ALL		−1.33		−2		−2		−1.33		−1.33				−2		−2		−1.33		−2(6)	mA
I_{IH}	V_{IH} = 4.5 V	ALL		100		100		200		100		100	100			100		100		100		100(6)	μA
I_{Ih}	V_{IH} = 5.5 V	ALL		1		1		1		1		1	1			1		1		1		1(6)	mA
V_{IH} min	V_I (applied)	−55°C	2		2		2		2		2					2		2	1.9		2(7)		V
		25°C	1.7		1.8		1.7		1.7		1.7					1.7		1.7	1.6		2(7)		
		125°C	1.4		1.6		1.4		1.4		1.4					1.4		1.4	1.3		2(7)		
	V_{OL} (measured)	ALL		0.45		0.45		0.45		0.65(4,9)		0.45				0.65(9)		0.65(9)		1.05(5)		0.6(7)	V
	SNGXX0: I_{OL} (forced)	ALL	20		22		40				30					6(3)		6(3)					mA
	SNGXX1: I_{OL} (forced)	ALL	10		12		20				15					6(3)		6(3)				60(7)	
V_{IL} max	V_I (applied)	−55°C	1		0.9		1		1		1.4					0.9		1	1.3		0.8(7)		V
		25°C	1.2		1.1		1.2		1.2		1.1					1.1		1.2	1.2		0.8(7)		
		125°C	0.9		0.9		0.9		0.9		0.8					0.9		0.9	0.85		0.8(7)		
	V_{OH} (measured)	−55°C	2.5		2.5		2.5		4.8(4)		2.5					4.8(4)		4.8(4)	3.5(5)		5.5(7)		V
		25°C	2.4		2.4		2.4		4.8(4)		2.4					4.8(4)		4.8(4)	3.5(5)		5.5(7)		
		125°C	2.7		2.5		2.7		4.8(4)		2.7					4.8(4)		4.8(4)	3.5(5)		5.5(7)		
	SNGXX0: I_{OH} (forced)	ALL	−1.5		−2.2		−3				0												mA
	SNGXX1: I_{OH} (forced)	ALL	−0.7		−1.2		−1.5				0										1(7)		
I_{OH}	V_{OH} = 5.5 V	ALL		250		250		250		250		250				250		250		250		250(8)	μA
I_{OS}	V_O = 0 V	ALL	−10	−45	−25	−100	−50	−150			−0.8	−1.33											mA
V_{OL}	V_{IH} = 2.8 V I_{OL} = forced as above	−55°C		0.4		0.4		0.4		0.65(2,4)		0.4								1(5)			V
		25°C		0.4		0.4		0.4		0.65(2,4)		0.4								1(5)			
		125°C		0.45		0.45		0.45		0.65(2,4)		0.45								1.05(5)			
V_{OH}	V_{IL} = 0.45 V I_{OH} = forced as above	−55°C	2.8		2.7		2.8		4.8(2,4)										4.8(5)				V
		25°C	3.2		3.1		3.2		4.8(2,4)										4.8(5)				
		125°C	3.35		3.15		3.35		4.8(2,4)										4.8(5)				
V_{BE} or V_{BC}	I_B = 1.33 mA for V_{BE} I_B = 1 mA for V_{BC}	−55°C												1.3									V
		25°C												1.1									
		125°C												1									
V_{CE}	I_B = 1.33 mA	ALL												0.2									V
h_{FE}	I_B = 1.33 mA, V_{CE} = 1.5 V	ALL											3										
V_{OL}	SNG130: I_{OL} = 100 mA	25°C						0.8															V
	SNG131: I_{OL} = 60 mA	25°C						0.8															
I_{OH}	V_{OH} = 7 V	25°C						1(1)				0.1											mA

†Specifications guaranteed at "ALL" temperatures are verified by measurements at T_A = −55°C, T_A = 25°C, and T_A = 125°C.

(1) V_{OH} = 6.5 V

(2) $R_{collector}$ = 800 Ω.

(3) V_E = 1 V at −55°C, 0.85 V at 25°C, and 0.65 V at 125°C.

(4) V_E = 0.9 V at −55°C, 0.75 V at 25°C, and 0.55 V at 125°C.

(5) R_L = 750 Ω

(6) V_{CC} = 5.5 V

(7) V_{CC} = 4.5 V

(8) V_O = 8 V

(9) V_{OL} for these expanders is measured between collector and emitter.

12

electrical characteristics (unless otherwise noted, V_{CC} = 5 V)

PARAMETER	CONDITIONS	T_A†	SNG42, 43 SNG52, 53 SNG62, 63 SNG72, 73 SNG92, 93 SNG102, 103 SNG112, 113 SNG122, 123 SNG142, 143 SNG192, 193		SNG202, 203 SNG212, 213 SNG222, 223 SNG242, 243 SNG252, 253 SNG262, 263 SNG302, 303 SNG312, 313 SNG322, 323		SNG132, 133		SNG152, 153 SNG172, 173		SNG162, 163		SNG182, 183		SNG232, 233		SNG272, 273		SNG292, 293		SNG353		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{IL}	V_{IL} = 0 V	ALL		−1.66		−2.5		−2.5		−1.66		−1.66				−2.5		−2.5		−1.6		−2.5(6)	mA
I_{IH}	V_{IH} = 4.5 V	ALL		100		100		200		100		100		100		100		100		100		100(6)	μA
I_{IH}	V_{IH} = 5.5 V	ALL		1		1		2		1		1		1		1		1		1		1(6)	mA
V_{IH} min	V_I (applied)	0°C	1.9		1.9		1.9		1.9		1.9					1.9	1.9		1.8		2(7)		V
		25°C	1.8		1.8		1.8		1.8		1.8					1.8	1.8		1.7		2(7)		
		75°C	1.7		1.7		1.7		1.7		1.7					1.7	1.7		1.6		2(7)		
	V_{OL} (measured)	ALL		0.45		0.45		0.45		0.65(4,10)		0.45				0.65(10)		0.65(10)		1.05(5)		0.8(7)	V
	SNGXX2: I_{OL} (forced)	ALL	20		22.5		40				30					6(3)	6(3)						mA
	SNGXX3: I_{OL} (forced)	ALL	10		12.5		20				15					6(3)	6(3)					60(7)	
V_{IL} max	V_I (applied)	0°C	1.1		1		1.1		1.1		1.2					1	1		1.2		0.8(7)		V
		25°C	1.2		1.1		1.2		1.2		1.1					1.1	1.1		1.2		0.8(7)		
		75°C	1.1		1		1.1		1.1		0.95					1	1		1		0.8(7)		
	V_{OH} (measured)	0°C	2.5		2.5		2.5		4.8(4)		2.5				4.8(4)		4.8(4)		3.5(5)		5.5(7)		V
		25°C	2.4		2.4		2.4		4.8(4)		2.4				4.8(4)		4.8(4)		3.5(5)		5.5(7)		
		75°C	2.5		2.5		2.5		4.8(4)		2.5				4.8(4)		4.8(4)		3.5(5)		5.5(7)		
	SNGXX2: I_{OH} (forced)	ALL	−1.2		−1.8		−2.4				0											1(7)	mA
	SNGXX3: I_{OH} (forced)	ALL	−0.6		−1		−1.2				0												
I_{OH}	V_{OH} = 5.5 V	ALL		250		250		250		250		250				250		250		250		250(8)	μA
I_{OS}	V_O = 0 V	ALL	−10	−45	−25	−100	−50	−150		−0.75	−0.75	−1.55											mA
V_{OL}	V_{IH} = 3 V, I_{OL} = forced as above	0°C		0.4		0.4		0.4		0.65(2,4)		0.4								1(5)		0.6(9)	V
		25°C		0.4		0.4		0.4		0.65(2,4)		0.4								1(5)		0.6(9)	
		75°C		0.45		0.45		0.45		0.65(2,4)		0.45								1.05(5)		0.6(9)	
V_{OH}	V_{IL} = 0.45 V, I_{OH} = forced as above	0°C	3		2.9		3		4.8(2,4)										4.8(5)				V
		25°C	3.1		3		3.1		4.8(2,4)										4.8(5)				
		75°C	3.15		3		3.15		4.8(2,4)										4.8(5)				
V_{BE} or V_{BC}	I_B = 1.66 mA for V_{BE} I_B = 1 mA for V_{BC}	0°C												1.3									V
		25°C												1.2									
		75°C												1.1									
V_{CE}	I_B = 1.66 mA	ALL												0.2									V
h_{FE}	I_B = 1.66 mA, V_{CE} = 1.5 V	ALL												3									
V_{OL}	SNG132: I_{OL} = 100 mA	25°C					0.8																V
	SNG133: I_{OL} = 60 mA	25°C					0.6																
I_{OH}	V_{OH} = 7 V	25°C					1(1)					0.1											mA

†Specifications guaranteed at "ALL" temperatures are verified by measurements at T_A = 0°C, T_A = 25°C, and T_A = 75°C.

(1) V_{OH} = 6.5 V
(2) $R_{collector}$ = 800 Ω.
(3) V_E = 0.9 V at 0°C, 0.85 V at 25°C, and 0.75 V at 75°C.
(4) V_E = 0.8 V at 0°C, 0.75 V at 25°C, and 0.65 V at 75°C.
(5) R_L = 750 Ω
(6) V_{CC} = 5.25 V
(7) V_{CC} = 4.75 V
(8) V_{CC} = 8 V
(9) V_{CC} = 4.75 V, V_I = 2.2 V
(10) V_{OL} for these expanders is measured between collector and emitter.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics, V_{CC} = 5 V

PARAMETER	CONDITIONS	T_A(1)	SNG80, 81 MIN	SNG80, 81 MAX	T_A(2)	SNG82, 83 MIN	SNG82, 83 MAX	UNIT
I_{IL}	V_{IL} = 0 V	ALL		−1.33	ALL		−1.66	mA
I_{IH}	V_{IH} = 4.5 V	ALL		100	ALL		100	μA
I_{IH}	V_{IH} = 5.5 V	ALL		1	ALL		1	mA
V_{OH}	V_I (applied)	−55°C	1.85↑		0°C	1.75↑		V
		25°C	1.55↑		25°C	1.55↑		
		125°C	1.28↑		75°C	1.40↑		
	V_{OH} (measured)	ALL	3.2		ALL	3.2		V
	SNG80, 82: I_{OH}	ALL	−3		ALL	−3		mA
	SNG81, 83: I_{OH}	ALL	−1.5		ALL	−1.5		
V_{OH}	V_I (applied)	−55°C	1.2↓		0°C	1.2↓		V
		25°C	1.1↓		25°C	1.1↓		
		125°C	0.9↓		75°C	1.02↓		
	V_{OH} (measured)	ALL	3.2		ALL	3.2		V
	SNG80, 82: I_{OH}	ALL	−3		ALL	−3		mA
	SNG81, 83: I_{OH}	ALL	−1.5		ALL	−1.5		
V_{OL}	V_I (applied)	−55°C	1.4↑		0°C	1.32↑		V
		25°C	1.22↑		25°C	1.22↑		
		125°C	0.95↑		75°C	1.07↑		
	V_{OL} (measured)	ALL		0.4	ALL		0.4	V
	SNG80, 82: I_{OL}	ALL	22		ALL	22		mA
	SNG81, 83: I_{OL}	ALL	12		ALL	12		
V_{OL}	V_I (applied)	−55°C	0.77↓		0°C	0.75↓		V
		25°C	0.81↓		25°C	0.81↓		
		125°C	0.57↓		75°C	0.7↓		
	V_{OL} (measured)	ALL		0.4	ALL		0.4	V
	SNG80, 82: I_{OL}	ALL	22		ALL	22		mA
	SNG81, 83: I_{OL}	ALL	12		ALL	12		
I_{OH}	V_{OH} = 5.5 V	ALL		250	ALL		250	μA
I_{OS}	V_O = 0 V	ALL	−25	−100	ALL	−25	−100	mA

electrical characteristics, V_{CC} = 5 V

PARAMETER	CONDITIONS	T_A(1)	SNG280, 281 MIN	SNG280, 281 MAX	T_A(2)	SNG282, 283 MIN	SNG282, 283 MAX	UNIT
I_{IL}	V_{IL} = 0 V	ALL		−1.33	ALL		−1.66	mA
I_{IH}	V_{IH} = 4.5 V	ALL		100	ALL		100	μA
I_{IH}	V_{IH} = 5.5 V	ALL		1	ALL		1	mA
V_{IH} min	V_I (applied)	−55°C	1.9		0°C	1.8		V
		25°C	1.6		25°C	1.7		
		125°C	1.3		75°C	1.6		
	V_{OH} (measured)	−55°C	2.5		0°C	2.5		V
		25°C	2.4		25°C	2.6		
		125°C	2.7		75°C	2.7		
	SNG280, 282: I_{OH} (forced)	ALL	−1.5		ALL	−1.2		mA
	SNG281, 283: I_{OH} (forced)	ALL	−0.7		ALL	−0.6		
V_{IL} max	V_I (applied)	−55°C	1.3		0°C	1.2		V
		25°C	1.2		25°C	1.2		
		125°C	0.85		75°C	1		
	V_{OL} (measured)	ALL		0.45	ALL		0.45	V
	SNG280, 282: I_{OL} (forced)	ALL	20		ALL	20		mA
	SNG281, 283: I_{OL} (forced)	ALL	10		ALL	10		
I_{OH}	V_{OH} = 5.5 V	ALL		250	ALL		250	μA
I_{OS}	V_O = 0 V	ALL	−15	−60	ALL	−15	−60	mA
V_{OL}	V_{IL} = 0.45 V	−55°C		0.4	0°C		0.4	V
	I_{OL} = forced as above	25°C		0.4	25°C		0.4	
		125°C		0.45	75°C		0.45	
V_{OH}	V_{IH} = 2.8 V	−55°C	2.8		0°C	3(3)		V
	I_{OH} = forced as above	25°C	3.1		25°C	3.1(3)		
		125°C	3.3		75°C	3.1(3)		

↑ This symbol designates a voltage which rises from 0 V to the specified level.
↓ This symbol designates a voltage which falls from 4 V to the specified level.
(1) Specifications guaranteed at "ALL" temperatures in this column are verified by measurements at T_A = −55°C, T_A = 25°C, and T_A = 125°C.
(2) Specifications guaranteed at "ALL" temperatures in this column are verified by measurements at T_A = 0°C, T_A = 25°C, and T_A = 75°C.
(3) V_{IH} = 3 V.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

maximum supply current in mA at specified free-air temperature

TYPE	I_{CCH} V_{CC} = 8 V 25°C	I_{CCL} V_{CC} = 5 V −55°C to 125°C	I_{CCH} V_{CC} = 5 V −55°C to 125°C
SNG40, 41	10	12	6
SNG50, 51	12	9	7.5
SNG60, 61	5	6	3
SNG70, 71	10	14	7
SNG80, 81	50(3)	35	11
SNG90, 91	34	10(4)	7
SNG100, 101	10	8	6
SNG110, 111	10	7	4
SNG120, 121	5	6	3
SNG130, 131	15	28	9
SNG140, 141	20	24	12
SNG150, 151	20	5(1) (2)	6(1)
SNG160, 161	15	27	9
SNG170, 171	10	2.5(2)	3
SNG180, 181	NA	NA	NA
SNG190, 191	15	18	9
SNG200, 201	6.5	7.5	3.5
SNG210, 211	10	9	6
SNG220, 221	26	30	14
SNG230, 231	14	6	8.5
SNG240, 241	13	15	7.5
SNG250, 251	17	12	10
SNG260, 261	6.5	7.5	3.5
SNG270, 271	7	3(2)	4.25
SNG280, 281	32	22	20
SNG290, 291	20	5	6
SNG300, 301	13.5	10.5	7.8
SNG310, 311	20	18	12
SNG320, 321	19.5	22.5	10.5
SNG351	28(3)	48	10

TYPE	I_{CCH} V_{CC} = 7 V 25°C	I_{CCL} V_{CC} = 5 V 0°C to 75°C	I_{CCH} V_{CC} = 5 V 0°C to 75°C
SNG42, 43	10	15	6
SNG52, 53	12	11	7.5
SNG62, 63	5	7.5	3
SNG72, 73	10	18	8
SNG82, 83	50	35	11
SNG92, 93	24	12(4)	7
SNG102, 103	10	10	6
SNG112, 113	10	9	4
SNG122, 123	5	7.5	3
SNG132, 133	15	34	11
SNG142, 143	20	30	12
SNG152, 153	20	6(1)(2)	7(1)
SNG162, 163	15	28.5	9
SNG172, 173	10	3(2)	3.5
SNG182, 183	NA	NA	NA
SNG192, 193	15	22.5	9
SNG202, 203	6.75	10	5
SNG212, 213	11	12	7.5
SNG222, 223	27	40	20
SNG232, 233	15	7.2	10.5
SNG242, 243	13.5	20	10
SNG252, 253	18	16	13
SNG262, 263	6.75	10	5
SNG272, 273	7.5	3.6(2)	5.25
SNG282, 283	34	27	24
SNG292, 293	20	6	7
SNG302, 303	15	14	10
SNG312, 313	22	24	15
SNG322, 323	20.25	30	15
SNG353	35	55	12

(1) Output emitters tied together, output collectors tied together.
(2) $V_{emitter}$ = 0.8 V
(3) V_{CC} = 7 V
(4) I_{CCL} is tested with gate I "on" and gate II "off", then vice-versa.

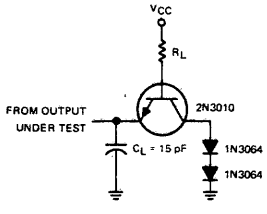
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES SNG GATES (Continued)

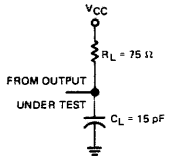
maximum switching times in ns at 25°C free-air temperature

TYPE		t_{PHL}	t_{PLH}	t_{THL}	t_{TLH}	LOAD CIRCUIT	R_L (Ω) SNGXX0	SNGXX1	SNGXX2	SNGXX3
SNG40, 41, 42, 43		20	20	5	8	1	260	570	330	600
SNG50, 51, 52, 53		23	23	6	8	1	260	570	330	600
SNG60, 61, 62, 63		24	20	5	8	1	260	570	330	600
SNG70, 71, 72, 73		22	22	6	8	1	260	570	330	600
SNG80, 81, 82, 83		20	20	4	4	1	← 2500 →			
SNG90, 91, 92, 93	Gate 1	22	22	6	8	1	260	570	330	600
	Gate 2	20	20	5	5					
SNG100, 101, 102, 103		22	22	6	8	1	260	570	330	600
SNG110, 111, 112, 113		22	22	6	8	1	260	570	330	600
SNG120, 121, 122, 123		28	20	5	8	1	260	570	330	600
SNG130, 131, 132, 133	C_L = 150 pF	25	25	12	15	4	260	570	330	600
	C_L = 1000 pF	50	40	30	30					
SNG140, 141, 142, 143		20	20	5	8	1	260	570	330	600
SNG150, 151, 152, 153		Δ4	Δ4							
SNG160, 161, 162, 163		20	30	5		3	← 350 →			
		20	70			3	← 5000 →			
SNG170, 171, 172, 173		Δ1	Δ1							
SNG180, 181, 182, 183		Δ3	Δ3							
SNG190, 191, 192, 193		20	20	5	8	1	260	570	330	600
SNG200, 201, 202, 203		15	10	3	4.5	1	← 2500 →			
SNG210, 211, 212, 213		11	11	3	4.5	1	← 2500 →			
SNG220, 221, 222, 223		10	10	2.5	4	1	← 2500 →			
SNG230, 231, 232, 233		Δ2	Δ2							
SNG240, 241, 242, 243		10	10	2.5	4	1	← 2500 →			
SNG250, 251, 252, 253		12	12	3	4.5	1	← 2500 →			
SNG260, 261, 262, 263		12	10	3	4	1	← 2500 →			
SNG270, 271, 272, 273		Δ1	Δ1							
SNG280, 281, 282, 283		15	15	5	8	1	← 4000 →			
SNG290, 291, 292, 293		15	15	5	8	1	← 4000 →			
SNG300, 301, 302, 303		12	12	3	4.5	1	← 2500 →			
SNG310, 311, 312, 313		11	11	3	4.5	1	← 2500 →			
SNG320, 321, 322, 323		10	10	2.5	4	1	← 2500 →			
SNG351, 353		25	10	10	10	2	← 75 →			

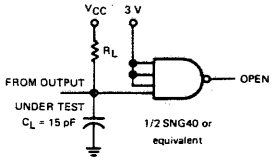
Δ—typical average delay added through expanded gate.



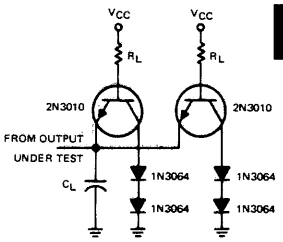
LOAD CIRCUIT 1



LOAD CIRCUIT 2



LOAD CIRCUIT 3



LOAD CIRCUIT 4

C_L includes probe and jig capacitance.

12

SERIES SNF FLIP-FLOPS*

FUNCTION	OPERATING TEMPERATURE RANGE −55°C to 125°C	FAN-OUT	OPERATING TEMPERATURE RANGE 0°C to 75°C	FAN-OUT	PACKAGES‡ Dual-in-Line J	Dual-in-Line N	Flat U
$\overline{S}$-$\overline{R}$ Flip-Flops	SNF10	15	SNF12	12	J	N	U
	SNF11	7	SNF13	6			
S-R Clocked Flip-Flops	SNF20	15	SNF22	12	J	N	U
	SNF21	7	SNF23	6			
Capacitively-Coupled $\overline{S}$-$\overline{R}$ Flip-Flops	SNF30	15	SNF32	12	J	N	U
	SNF31	7	SNF33	6			
AND-Input J-K Flip-Flops	SNF50	15	SNF52	12	J	N	U
	SNF51	7	SNF53	6			
AND-OR-Input J-K Flip-Flops	SNF60	15	SNF62	12	J	N	U
	SNF61	7	SNF63	6			
Dual J-K Flip-Flops (Separate Clocks)	SNF100	11	SNF102	9	J	N	U
	SNF101	6	SNF103	5			
Dual J-K Flip-Flops (Common Clock and Clear)	SNF110	11	SNF112	9	J	N	U
	SNF111	6	SNF113	5			
Dual J-K Flip-Flops (Separate Clocks)	SNF120	11	SNF122	9	J	N	U
	SNF121	6	SNF123	5			
Dual J-K Flip-Flops (Common Clock and Clear)	SNF130	11	SNF132	9	J	N	U
	SNF131	6	SNF133	5			
AND-Input J-K Flip-Flops	SNF200	11	SNF202	9	J	N	U
	SNF201	6	SNF203	5			
AND-OR-Input J-K Flip-Flops	SNF210	11	SNF212	9	J	N	U
	SNF211	6	SNF213	5			
AND-Input J-K Flip-Flops	SNF250	11	SNF252	9	J	N	U
	SNF251	6	SNF253	5			
AND-OR-Input J-K Flip-Flops	SNF260	11	SNF262	9	J	N	U
	SNF261	6	SNF263	5			

‡ For outline drawings of all packages, see section 1.

12

* Interchangeable with SUHL 1† and SUHL 2† TTL circuits.
† Trademark of Sylvania Electric Products, Inc.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

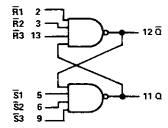
SERIES SNF FLIP-FLOPS (Continued)

line summary

Pin 4 is V_{CC}, pin 10 is GND

GATED FLIP-FLOPS

SNF10, 11, 12, 13



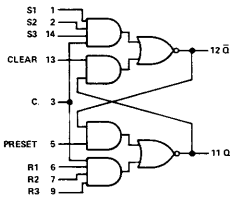
TRUTH TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
S̄	R̄	Q	Q̄
H	H	Q_n	$\bar{Q}_n$
H	L	L	H
L	H	H	L
L	L	Indeterminate	

$\bar{S} = \bar{S}1 + \bar{S}2 + \bar{S}3$
$\bar{R} = \bar{R}1 + \bar{R}2 + \bar{R}3$

S̄-R̄ FLIP-FLOPS

SNF20, 21, 22, 23



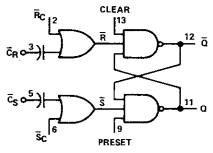
TRUTH TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
S	R	Q	Q̄
L	L	Q_n	$\bar{Q}_n$
L	H	L	H
H	L	H	L
H	H	Indeterminate	

S = S1 · S2 · S3
R = R1 · R2 · R3
Low input to preset sets Q high
Low input to clear resets Q low
Preset and clear are operable when clock is low.

S-R CLOCKED FLIP-FLOPS

SNF30, 31, 32, 33



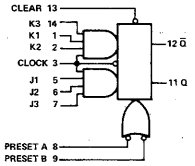
TRUTH TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
S̄	R̄	Q	Q̄
H	H	Q_n	$\bar{Q}_n$
H	L	L	H
L	H	H	L
L	L	Indeterminate	

An active-low condition at S̄ requires a low at S̄C and a high-to-low transition at C̄S.
An active-low condition at R̄ requires a low at R̄C and a high to low transition at C̄R.

CAPACITIVELY-COUPLED S̄-R̄ FLIP-FLOPS

SNF50, 51, 52, 53
SNF200, 201, 202, 203
SNF250, 251, 252, 253



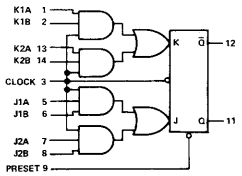
TRUTH TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	K	Q	Q̄
L	L	Q_n	$\bar{Q}_n$
L	H	L	H
H	L	H	L
H	H	$\bar{Q}_n$	Q_n

J = J1 · J2 · J3
K = K1 · K2 · K3

AND-INPUT J-K FLIP-FLOPS

SNF60, 61, 62, 63
SNF210, 211, 212, 213
SNF260, 261, 262, 263



TRUTH TABLE

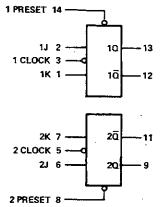
INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	K	Q	Q̄
L	L	Q_n	$\bar{Q}_n$
L	H	L	H
H	L	H	L
H	H	$\bar{Q}_n$	Q_n

J = J1A · J1B + J2A · J2B
K = K1A · K1B + K2A · K2B

AND-OR-INPUT J-K FLIP-FLOPS

DUAL FLIP-FLOPS

SNF100, 101, 102, 103
SNF120, 121, 122, 123

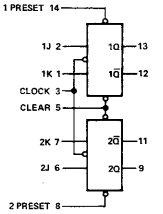


TRUTH TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	K	Q	Q̄
L	L	Q_n	$\bar{Q}_n$
L	H	L	H
H	L	H	L
H	H	$\bar{Q}_n$	Q_n

DUAL J-K FLIP-FLOPS (SEPARATE CLOCKS)

SNF110, 111, 112, 113
SNF130, 131, 132, 133



TRUTH TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	K	Q	Q̄
L	L	Q_n	$\bar{Q}_n$
L	H	L	H
H	L	H	L
H	H	$\bar{Q}_n$	Q_n

DUAL J-K FLIP-FLOPS (COMMON CLOCK AND CLEAR)

H = high level
L = low level
t_n = bit time before clock pulse
t_{n+1} = bit time after clock impulse
Q_n = level of output Q at t_n
$\bar{Q}_n$ = complement of Q_n or level of output Q̄ at t_n

12

electrical characteristics (unless otherwise noted, V_{CC} = 5 V)

PARAMETER		CONDITIONS	T_A†	SNF10, 11		SNF20, 21		SNF30, 31		SNF50, 51		SNF60, 61		SNF100, 101		SNF110, 111		SNF120, 121		SNF130, 131		SNF200, 201		SNF210, 211		SNF250, 251		SNF260, 261		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{IL}	R, S, J, or K INPUTS	V_I = 0 V	ALL		−1.33		−1.33				1.33		1.33		−1.33		−1.33		−1.33		−1.33		−1.33		−1.33		1.33		−1.33	mA
	CLOCK INPUT						−2.66				1.33[2]		2.66[2]		−1.33		−2.66		−1.33		2.66		−1.33		−2[2]		−4[2]	
	PRESET INPUT								−1.33		1.33		1.33		2.4		−2.4		−2.4		2.4		2.4		−2.4		1.33		−1.33	
	CLEAR INPUT								−1.33		1.33						−4.8				4.8		−2.4				−1.33			
	$\overline{C}_R$ or $\overline{C}_S$ INPUT							−0.4	−1.1																				
I_{IH}	R, S, J, or K INPUTS	V_I = 4.5 V	ALL		100		100				100		100		70		70		70		70		70		70		100		100	μA
	CLOCK INPUT						200		150		200		400		140		280		140		280		140		280		150		400	
	PRESET INPUT								100		100		100		70		70		70		70		70		70		100		100	
	CLEAR INPUT								100		100						140				140		70				100			
I_{IH}	R, S, J, or K INPUTS	V_I = 5.5 V	ALL		1		1				1		1		1		1		1		1		1		1		1		1	mA
	CLOCK INPUT						1		1		2		4		2		4		2		4		2		4		2		2[3]	
	PRESET INPUT								1		1		1		1		1		1		1		1		1		1		1	
	CLEAR INPUT								1		1						2				2		1				1			
V_{IH} min		V_I (applied)	−55°C	2		2		2		2		2		2		2		2		2		2		2		2		2		V
			25°C	1.7		1.7		1.7		1.7		1.7		1.8		1.8		1.8		1.8		1.8		1.7		1.7		1.7		
			125°C	1.4		1.4		1.4		1.4		1.4		1.5		1.5		1.5		1.5		1.4		1.4		1.4		1.4		
		V_O (measured)	ALL		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45	V
		SNFXX0: I_{OL} (forced)	ALL	20		20		20		20		20		22		22		22		22		22		22		22		22		mA
		SNFXX1: I_{OL} (forced)	ALL	10		10		10		10		10		12		12		12		12		12		12		12		12		
V_{IL} max		V_I (applied)	−55°C	1		1		1		1		1		0.9		0.9		0.9		0.9		1.0		0.9		1		1		V
			25°C	1.2		1.2		1.2		1.2		1.2		1.1		1.1		1.1		1.1		1.2		1.1		1.2		1.2		
			125°C	0.9		0.9		0.9		0.9		0.9		0.9		0.9		0.9		0.9		0.9		0.9		0.9		0.9		
		V_O (measured)	−55°C	2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		V
			25°C	2.4		2.4		2.4		2.4		2.4		2.4		2.4		2.4		2.4		2.4		2.4		2.4		2.4		
			125°C	2.7		2.7		2.7		2.7		2.7		2.5		2.5		2.5		2.5		2.7		2.5		2.7		2.7		
		SNFXX0: I_{OH} (forced)	ALL		−1.5		−1.5		−1.5		−1.5		−1.5		−2.2		−2.2		−2.2		−2.2		−1.5		−1.5		−1.5		mA
		SNFXX1: I_{OH} (forced)	ALL		−0.7		−0.7		−0.7		−0.7		−0.7		−1.2		−1.2		−1.2		−1.2		−0.7		−0.7		−0.7		−0.7	
I_{OH}		V_{OH} = 5.5 V	ALL		1.25		1.25		1.25		2.25		3.25		1.25		1.25		1.25		1.25		2.25		2.25		2.25		4.25	mA
		V_{OH} = 4.5 V	ALL						0.35				0.55																0.65	
I_{OS}		V_O = 0 V	ALL	−10	−45	−10	−45	−10	−45	−30	−70	−30	−70	−30	−90	−30	−90	−30	−90	−30	−90	−30	−90	−30	−90	−30[1]	−70[1]	−30[1]	−70[1]	mA
V_{OL}		V_{IH} = 2.8 V,	−55°C		0.4		0.4		0.4[4]		0.4		0.4		0.4		0.4		0.4		0.4		0.4				0.4		0.4	V
		V_{IL} = 0.45 V,	25°C		0.4		0.4		0.4[4]		0.4		0.4		0.4		0.4		0.4		0.4		0.4				0.4		0.4	
		I_{OL} = forced (as above)	−125°C		0.45		0.45		0.45[4]		0.45		0.45		0.45		0.45		0.45		0.45		0.45				0.45		0.45	
V_{OH}		V_{IH} = 2.8 V,	−55°C	2.8		2.8		3		2.8		2.8		2.8		2.8		2.8		2.8		2.8		2.8		2.8		2.8		V
		V_{IL} = 0.45 V,	25°C	3.2		3.2		3.1		3.2		3.2		3		3		3		3		3		3		3.2		3.2		
		I_{OH} = forced (as above)	125°C	3.35		3.35		3.15		3.35		3.35		3		3		3		3		3		3		3.35		3.35		
I_{CC}			ALL		9[1]		11		9		12		15		28		28		28		28		14		16		12		15	mA
t_{PHL}		LOAD CIRCUIT A	25°C		30		20		40		40		40		20		20		15		15		15		15		25		25	ns
t_{THL}		LOAD CIRCUIT A	25°C		5		5		5		5		5		2.5		2.5		2.5		2.5		2.5		2.5		4		4	ns
t_{PLH}		LOAD CIRCUIT A	25°C		20		30		20		20		20		20		20		15		15		15		15		20		20	ns
t_{TLH}		LOAD CIRCUIT A	25°C		8		8		8		8		8		4		4		4		4		4		4		6		6	ns

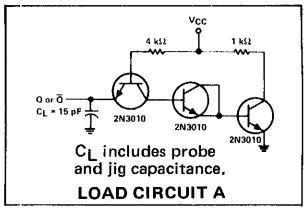
† Specifications guaranteed at "ALL" temperatures are verified by measurements at T_A = −55° C, T_A = 25° C, and T_A = 125° C.

recommended operating conditions at T_A = 25°C

f_{clock}	Clock frequency	20		20		10		20		20		35		35		50		MHz
$t_{w(clock)}$	Width of clock pulse		30		20		20		20		20		20		15		15	ns
$t_{w(preset)}$	Width of preset pulse		30				40		40		20		20		15		25	ns
$t_{w(clear)}$	Width of clear pulse		30				40		40		20		20		15		25	ns

f_{clock}	Clock frequency	50		50		50		50		30		30						MHz
$t_{w(clock)}$	Width of clock pulse	15		15		15		15		15		15						ns
$t_{w(preset)}$	Width of preset pulse	15		15		15		15		25		25						ns
$t_{w(clear)}$	Width of clear pulse	15		15		15		15		25								ns

(1) T_A = 25° C only.
(2) V_I = 0.2 V.
(3) Outputs and preset are open, all other inputs are grounded.
When Q is grounded and all other inputs are open, I_{IH} = 4 mA maximum.
(4) V_{IH} = 3 V.



C_L includes probe and jig capacitance.

LOAD CIRCUIT A

electrical characteristics (unless otherwise noted, V_{CC} = 5 V)

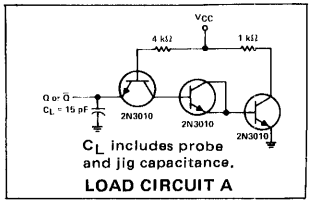
PARAMETER		CONDITIONS	T_A†	SNF12, 13		SNF22, 23		SNF32, 33		SNF52, 53		SNF62, 63		SNF102, 103		SNF112, 113		SNF122, 123		SNF132, 133		SNF202, 203		SNF212, 213		SNF252, 253		SNF262, 263		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{IL}	R, S, J, or K INPUTS	V_I = 0 V	ALL		−1.66		−1.66				−1.66		−1.66		−1.66		−1.66		−1.66		−1.66		−1.66		−1.66		1.66		
	CLOCK INPUT						−3.3				−1.66[4]		−3.33[4]		−1.66		−3.32		−1.66		−3.32		−1.66		−3.3		−2.5[4]		
	PRESET INPUT								−1.66		−1.66		−1.66		−2.8		−2.8		−2.8		−2.8		−2.8		−2.8		−1.66		−1.86	mA
	CLEAR INPUT								−1.66		−1.66						−5.6				−5.6		−2.8				−1.66			
	C_R or C_S INPUT							−0.4	−1.3																					
I_{IH}	R, S, J, or K INPUTS	V_I 4.5 V	ALL		100		100				100		100	70	70	70	70	70	70	70	70	70	70	70	70		100		100	
	CLOCK INPUT						200		150		200		400	140	280	140	280	140	280	140	280	140	280	140	280		150		400	μA
	PRESET INPUT								100		100		100	70	70	70	70	70	70	70	70	70	70	70	70		100		100	
	CLEAR INPUT								100		100				140				140		140		70				100			
I_{IH}	R, S, J, or K INPUTS	V_I 5.5 V	ALL				1				1		1	1	1	1	1	1	1	1	1	1	1	1	1		1		1	
	CLOCK INPUT						2		1		2		4	2	4	2	4	2	4	2	4	2	4	2	4		2		2[3]	mA
	PRESET INPUT								1		1		1	1	1	1	1	1	1	1	1	1	1	1	1		1		1	
	CLEAR INPUT								1		1				2				2		2		1				1			
V_{IH} min		V_I (applied)	0°C	1.9		1.9		1.9		1.9		1.9		1.9		1.9		1.9		1.9		1.9		1.9		1.9		1.9		
			25°C	1.8		1.8		1.8		1.8		1.8		1.8		1.8		1.8		1.8		1.8		1.8		1.8		1.8		V
			75°C	1.7		1.7		1.7		1.7		1.7		1.7		1.7		1.7		1.7		1.7		1.7		1.7		1.7		
		V_O (measured)	ALL		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45	V
		SNFXX2: I_{OL} (forced)	ALL		20		20		20		20		20		22.5		22.5		22.5		22.5		22.5		22.5		22.6		mA
		SNFXX3: I_{OL} (forced)	ALL		10		10		10		10		10		12.5		12.5		12.5		12.5		12.5		12.5		12.6		
V_{IL} max		V_I (applied)	0°C		1.1		1.1		1.1		1.1		1.1		1		1		1		1		1		1		1.1		
			25°C		1.2		1.2		1.2		1.2		1.2		1.1		1.1		1.1		1.1		1.1		1.1		1.2		1.2	V
			75°C		1.1		1.1		1.1		1.1		1.1		1		1		1		1		1		1		1.1		1.1	
		V_O (measured)	0°C	2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		
			25°C	2.4		2.4		2.4		2.4		2.4		2.4		2.4		2.4		2.4		2.4		2.4		2.4		2.4		V
			75°C	2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5		
		SNFXX2: I_{OH} (forced)	ALL		−1.2		−1.2		−1.2		−1.2		−1.2		−1.8		−1.8		−1.8		−1.8		−1.2		−1.2		−1.2		mA
		SNFXX3: I_{OH} (forced)	ALL		−0.6		−0.6		−0.6		−0.6		−0.6		−1		−1		−1		−1		−0.6		−0.6		−0.6		
I_{OH}		V_{OH} = 5.5 V	ALL		1.25		1.25		1.25		2.25		3.25		1.25		1.25		1.25		1.25		2.25		2.25		2.25		4.25	mA
		V_{OH} = 4.5 V	ALL						0.35				0.55																0.65	
I_{OS}			ALL	−10	−46	−10	−45	−10	−45	−30	−70	−30	−70	−30	−90	−30	−90	−30	−90	−30	−90	30	−90	−30	−90	−30[1]	−70[1]	−30[1]	−70[1]	mA
V_{OL}		V_{IH} = 3 V, V_{IL} = 0.45 V, I_{OL} = forced (as above)	0°C		0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4	
			25°C		0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4		0.4	V
			75°C		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45	
V_{OH}		V_{IH} = 3 V, V_{IL} = 0.45 V, I_{OH} = forced (as above)	0°C	3		3		3		3		3		3		3		3		3		3		3		3		3		
			25°C	3.1		3.1		3.1		3.1		3.1		3		3		3		3		3		3		3.1		3.1		V
			75°C	3.15		3.15		3.15		3.15		3.15		3		3		3		3		3		3		3.15		3.15		
I_{CC}			ALL		9[1]		13		9		14		18		34		34		34		34		17		19		14		18	mA
t_{PHL}		LOAD CIRCUIT A	25°C		30		20		40		40		40		20		20		15		15		15		15		25		25	ns
t_{THL}		LOAD CIRCUIT A	25°C		5		5		5		5		5		2.5		2.5		2.5		2.5		2.5		2.5		4		4	ns
t_{PLH}		LOAD CIRCUIT A	25°C		20		30		20		20		20		20		20		15		15		15		15		20		20	ns
t_{TLH}		LOAD CIRCUIT A	25°C		8		8		8		8		8		4		4		4		4		4		4		6		6	ns

† Specifications guaranteed at "ALL" temperatures are verified by measurement at T_A = 0° C, T_A = 25° C, T_A = 75° C.

recommended operating conditions at T_A = 25°C

f_{clock}	Clock frequency	20	20	10	20	20	35	35	50	50	50	50	30	30	MHz
$t_{w(clock)}$	Width of clock pulse		30	20	20	20	20	20	15	15	15	15	15	15	ns
$t_{w(preset)}$	Width of preset pulse		30		40	40	20	20	15	15	15	15	26	25	ns
$t_{w(clear)}$	Width of clear pulse		30		40	40	20	20	15	15	15	15	26		ns

(1) T_A = 25°C only.
(2) V_I = 0.2 V.
(3) Outputs and preset are open, all other inputs are grounded.
When Q is grounded and all other inputs are open, I_{IH} = 4 mA maximum.
(4) V_{IH} = 3 V.



C_L includes probe and jig capacitance.
LOAD CIRCUIT A

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

High-Noise-Immunity Logic (HNIL) Summary

general

The High-Noise-Immunity Logic (HNIL) family of integrated circuits is intended for applications requiring a higher degree of inherent electrical noise immunity than is available with more standard forms of integrated circuit logic families. The considerably higher input threshold exhibited by HNIL is obtained by using, in the input circuitry, a reverse-biased base-emitter junction which operates in the avalanche breakdown mode. The relatively slow propagation delays of HNIL also enhance the noise rejection capability of this type of integrated circuit. Buffered outputs on all elements and wide logic swings eliminate the necessity for interface circuitry in most applications. HNIL is ideally suited for industrial and consumer applications requiring maximum noise immunity and excellent line-driving capability. Typical applications include control circuitry in appliances, numerical-control machines, process control, materials handling, and electrostatic copying equipment. The Texas Instruments HNIL integrated circuits are designed to be pin-for-pin replacements for the Amelco series 300 devices. For information concerning availability of additional HNIL circuits and full military temperature range devices, please contact L/CC Product Marketing, Box 5012, M.S. 914, Dallas, Texas 75222, Phone 214-238-3081.

functional index

FUNCTION	OPERATING TEMPERATURE RANGE −30°C to 85°C	PACKAGES* Dual-In-Line	
NAND GATES			
Dual 5-Input NAND Gate (Active Pull-Up)	SN15301	J	N
Quadruple 2-Input NAND Gates (Open-Collector)	SN15302	J	N
	SN15323	J	N
Quadruple 2-Input NAND Gates (Resistive Pull-Up)	SN15303	J	N
	SN15324	J	N
Quadruple 2-Input NAND Gate (Active Pull-Up)	SN15321	J	N
Dual 2-Input, Dual 3-Input NAND Gate (Active Pull-Up)	SN15325	J	N
Dual 2-Input, Dual 3-Input NAND Gate (Resistive Pull-Up)	SN15326	J	N
FLIP-FLOPS			
Dual J-K Flip-Flop	SN15312	J	N
Dual Monostable Multivibrator	SN15342	J	N
Quadruple $D\overline{G}$ Flip-Flop	SN15370	J	N

* For outline drawings of all packages, see Section 1.

13

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage . . . . . 16.5 V
Input voltage (exclusive of expanders) . . . . . 16.5 V
Input voltage (expanders) . . . . . 6 V
Output voltage . . . . . 16.5 V
Output current at (or below) 25°C free-air temperature:
SN15301, SN15302 . . . . . 80 mA
All other types . . . . . 15 mA
Duration of output short-circuit to ground (See Note 1) . . . . . unlimited
Operating free-air temperature range . . . . . −30°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

electrical characteristics over rated operating free-air temperature range

PARAMETER	V_{OH} at $I_O = 0$	V_{OH} at I_O	I_{OH} at $V_O = 13.5$ V	V_{OL} at I_O	V_{OL} at I_O	I_{IL} at $V_I = 1.8$ V	I_{IH}† at $V_I = 15$ V	I_{CC}‡ at $V_{CC} = 15$ V
UNIT	V min	V min mA	μA max	V max mA	V max mA	mA max	μA max	mA max
SN15301	12	8 −15		1.6 50	1.8 75	−1.9	100	40
SN15302			100	0.7 30	1.2 60	−1.9	100	40
SN15303	12	8 −0.3		0.8 40	1.2 60	−1.9	100	43
SN15312	12	8 −5		1.8 9.5		−1.9 −3.8§	100	36
SN15321	12	8 −5		1.6 9.5		−1.9	100	18
SN15323			100	0.6 11		−1.9	100	6
SN15324	12	8 −0.3		0.8 15		−1.9	100	36
SN15325	12	8 −5		1.6 9.5		−1.9	100	18
SN15326	12	8 −0.3		0.8 15		−1.9	100	36
SN15342	12	8 −5		1.8 9.5		−1.9	100	22.5
SN15370	12	8 −0.3		0.6 8.8		−1.9 −3.8#	100	45

Test conditions (unless otherwise specified): V_{CC} . . . . . 13.5 V
V_{IH} . . . . . 6.75 V
V_{IL} . . . . . 5 V
V_I (I_{IL} test) . . . . . 1.8 V

†Typically less than 1 μA at 25°C free-air temperature.
‡Measured with all inputs open.
§Applies to preset and clear inputs only.
#Applies to data input only.

NOTE 1: All outputs may be shorted simultaneously.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics

GATES

PARAMETER	t_{PLH}	t_{PHL}
UNIT	ns max	ns max
SN15301	250	200
SN15302	300	200
SN15303	300	200
SN15326	400	150

FLIP-FLOPS

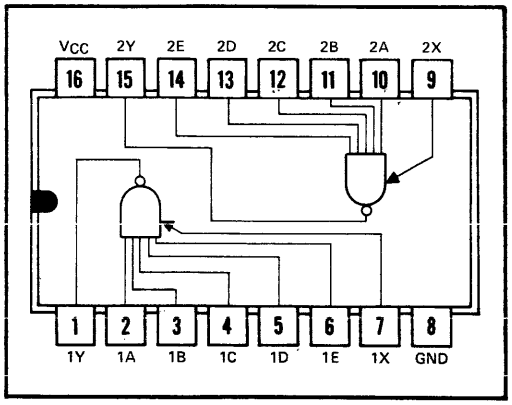
PARAMETER	t_{PLH}	t_{PHL}	TEST CONDITIONS				
UNIT	ns max	ns max	CLOCK	SET	RESET	D	$\overline{G}$
SN15312	200	200	↓				
	150	200		↓	↓		
SN15342	200	150					
SN15370	500					6.75 V	↓
		300				5 V	↓
	320					↑	5 V
		200				↓	5 V

NOTES:
1. V_{CC} = 13.5 V, high level of pulses is 10 V, low level of pulses is 0 V.
2. Measurements are made from the 5.5-V point on the input waveform to the 50% point on the output waveform.
3. Load for SN15301, SN15302, and SN15303 is 2 kΩ to V_{CC}, 50 pF to GND. Load for all other devices is 10 kΩ to V_{CC}, 10 pF to GND.
4. The output pulse width ($t_w \simeq 0.7$ RC) of the SN15342 is determined by an external capacitor, and for precision applications, an external timing resistor which should not exceed 62 kΩ or be less than 2 kΩ. For normal applications the 20 kΩ nominal internal resistor is connected by shorting pin 1 to pin 3 or pin 15 to pin 13.

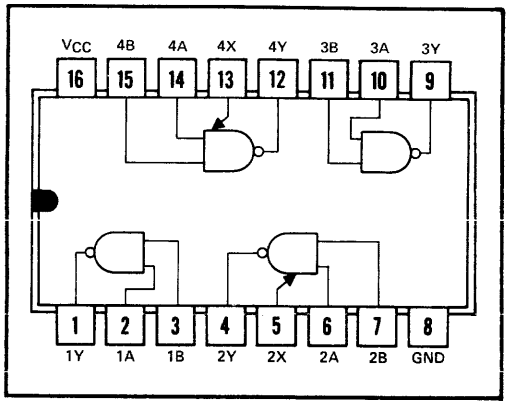
13

terminal assignments, J or N dual-in-line packages (top views)

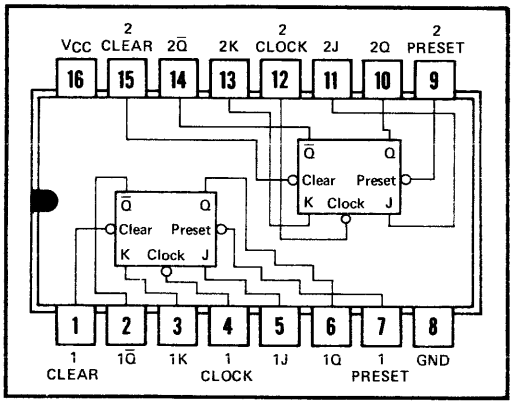
SN15301



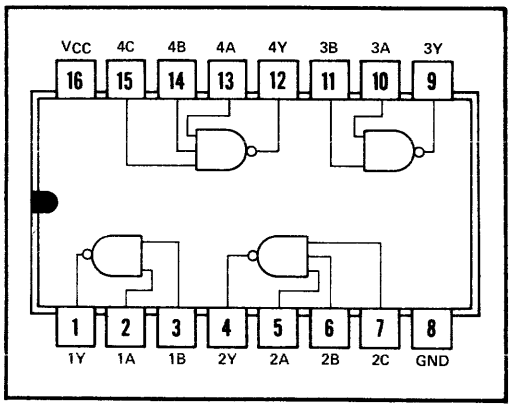
SN15302, SN15303, SN15321, SN15324



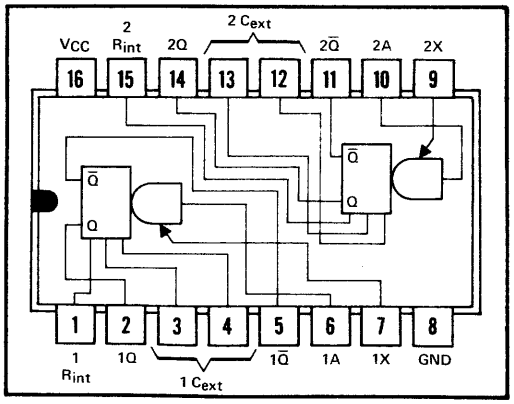
SN15312



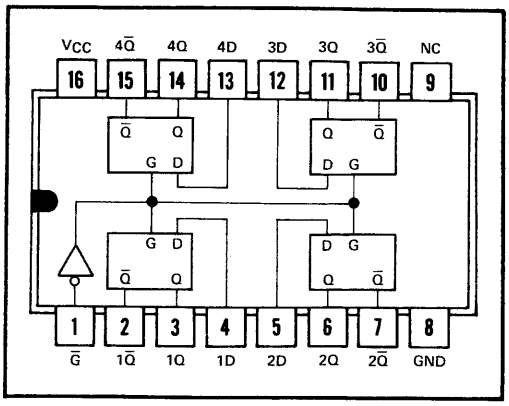
SN15325, SN15326



SN15342



SN15370



NC—No internal connection

13

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS/LSI Circuits

CONTENTS

14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

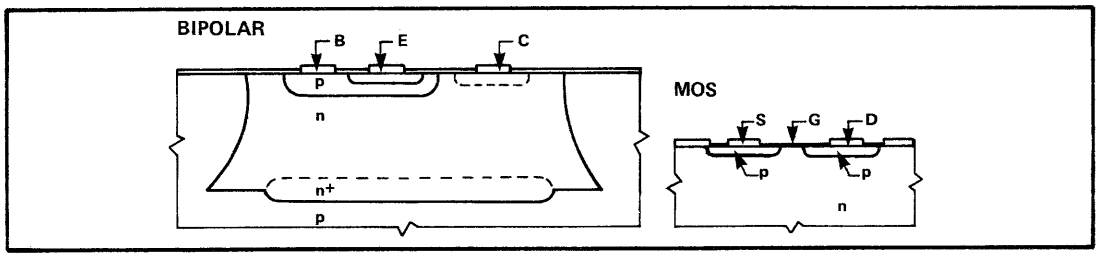
CONTENTS

MOS . . . . . an innovative technology

Many types of equipment previously not suitable for electronic control can now take full advantage of the latest electronics technology. Equipment costs can be kept low, and equipment size can be reduced easily. MOS (Metal Oxide Semiconductor) circuits are ideal for digital applications including timers and counters, data transmission and switching equipment, recorders, calculators, controls and computer equipment. MOS is also suitable for analog applications such as telemetry and test equipment.

MOS technology can be applied to hundreds of equipment types at costs usually lower than for other technologies with significant improvements in reliability.

The introduction of MOS/LSI into new classes of equipments is possible because the basic MOS device combines the best attributes of the pentode vacuum tube with all the advantages of the transistor. MOS devices have high-input impedance, they are small, simple to fabricate, and consume little power; consequently they offer the highest complexity of large-scale-integrated circuits.



COMPARISON OF TRANSISTOR CROSS SECTIONS

WHAT IS MOS?

MOS ICs require only one-third of the process steps needed for the standard double-diffused bipolar IC. But the most significant feature is the large number of semiconductor circuit elements that can be put on a small chip. This high circuit density means large-scale integration, and permits TI to put up to 5000 devices on a silicon chip only 150- x 150-mils square. Each transistor in the MOS/LSI array requires as little as 1 square mil of chip area – a great reduction over the bipolar transistors requiring 49 to 50 square mils.

Inherent advantages of MOS/LSI include:

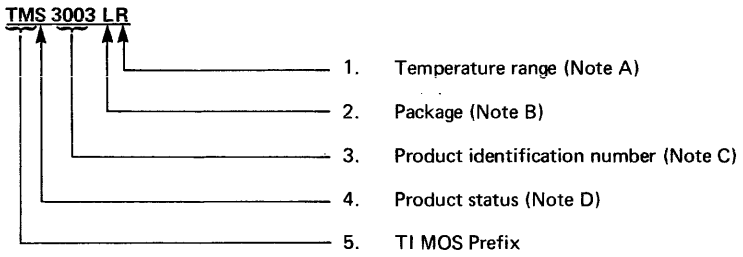
- increased circuit complexity per package
- lower cost per circuit function
- fewer subsystems to test
- fewer parts to assemble and inspect
- lower power-drain per function
- a choice of standard or custom products

From the design standpoint, MOS/LSI is a two-dimensional layout rather than three dimensional. Mathematically its operation can be predicted, and mathematical models lend themselves to Computer-Aided Design analysis. Therefore the circuit can be laid out and its operation checked before it is built.

TEXAS INSTRUMENTS MOS/LSI DEVICE NUMBERING SYSTEM

Electrical characteristics presented in this catalog, unless otherwise noted, apply for circuit type(s) listed in the page heading, regardless of package. Factory orders for circuits described should include the complete part-type numbers listed on each page.

MOS NUMBERING SYSTEM



NOTE A Temperature Range

C	−25°C to +85°C (commercial)
M	−55°C to +125°C (military)
R	−55°C to +85°C (reduced military)
S	Special range (as designated by customer)

NOTE B Package

F	Flat package
J	Ceramic dual-in-line
N	Plastic dual-in-line
L	Plug-in package
U	Unencapsulated (beam lead, etc.)

NOTE C Product Identification Number

Part number unique to each device type

NOTE D Product Status

S	Standard devices
X	Prototype or experimental
C	Custom design
T	High reliability

Because of the high complexity of MOS/LSI, TI has had to innovate in the packaging area. The packages selected by TI are standards of the industry. Accessories for these packages are readily available.

All standard MOS/LSI devices supplied in ceramic dual-in-line packages and most of those mounted in plug-in-type packages are now available in plastic.

1) Dual-in-line package

a) Pin-to-pin spacing

A pin-to-pin spacing of 100 mils has been selected for all dual-in-line packages.

b) Row-to-row spacing

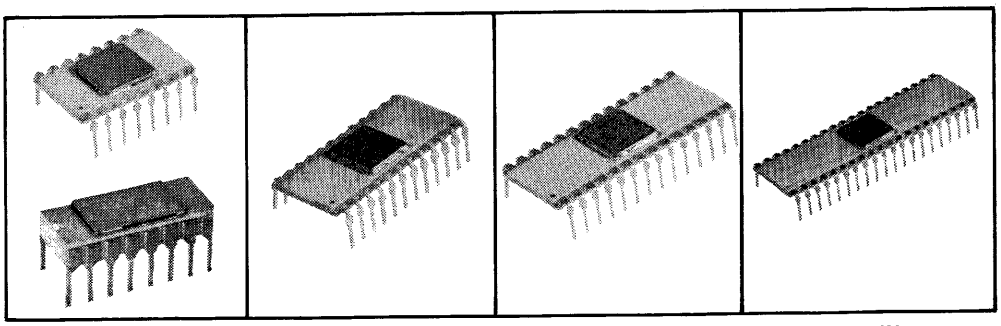
Two spacings are used for mounting-hole rows — 300 mils and 600 mils

c) Ceramic package types

TI uses several hermetically sealed ceramic dual-in-line packages, which consist of a ceramic base, gold-plated cap and gold-plated leads.

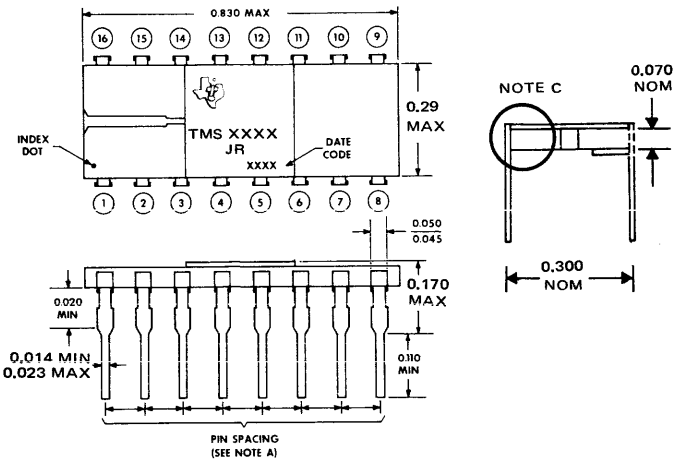
The following packages are presently in use:

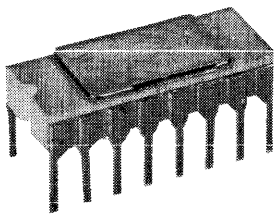
	16 PIN	24 PIN	26 PIN	40 PIN
300 MILS BETWEEN ROWS	X			
600 MILS BETWEEN ROWS	X	X	X	X



16 PIN 24 PIN 28 PIN 40 PIN

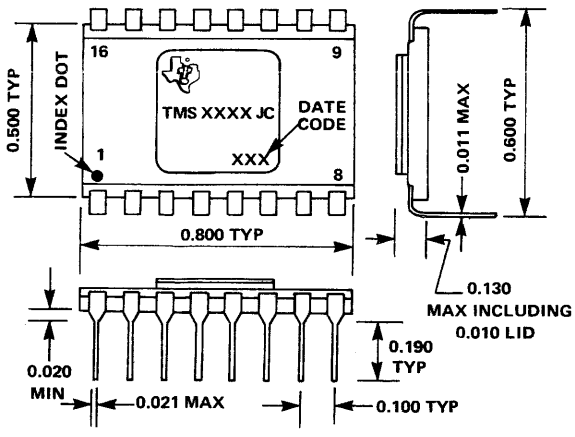
16-pin package (300-mil row spacing)

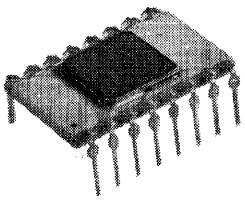




A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 16.
B. All dimensions are in inches.
C. LEADS MAY BE BRAZED TO SIDES OR BOTTOM OF PACKAGE

16-pin package (600-mil row spacing)

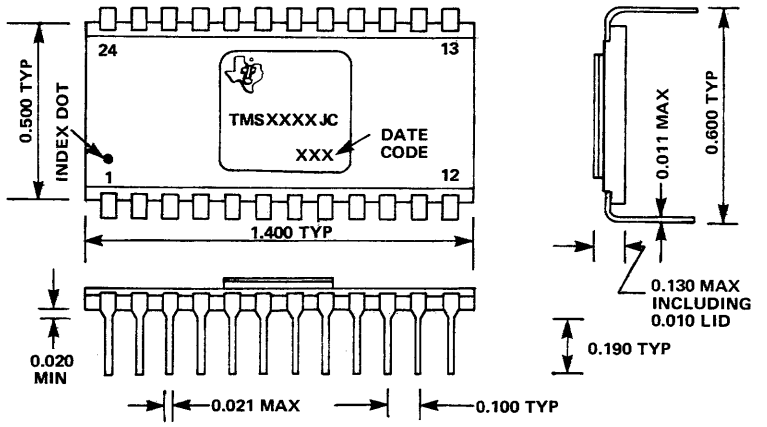


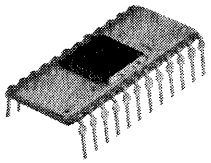


NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located with ±0.010 of its true longitudinal position relative to pins 1 and 16.
B. All dimensions are in inches.

14

24-pin package

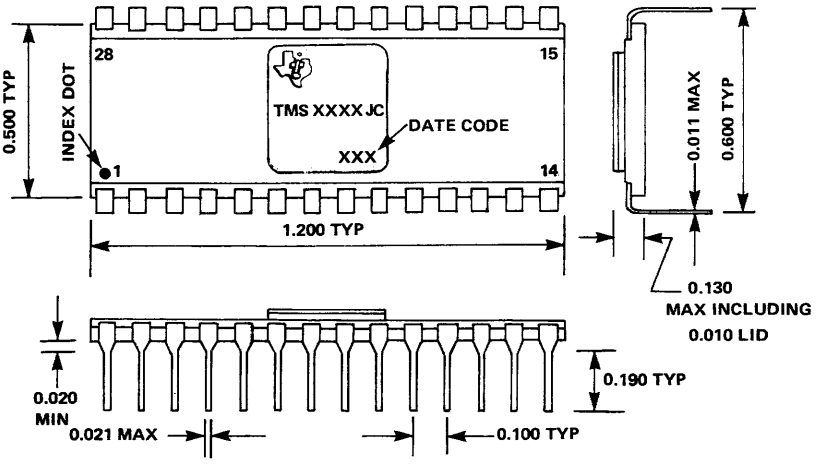


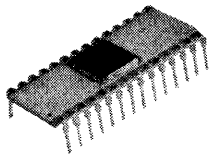


NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 24.

B. All dimensions are in inches.

28-pin package



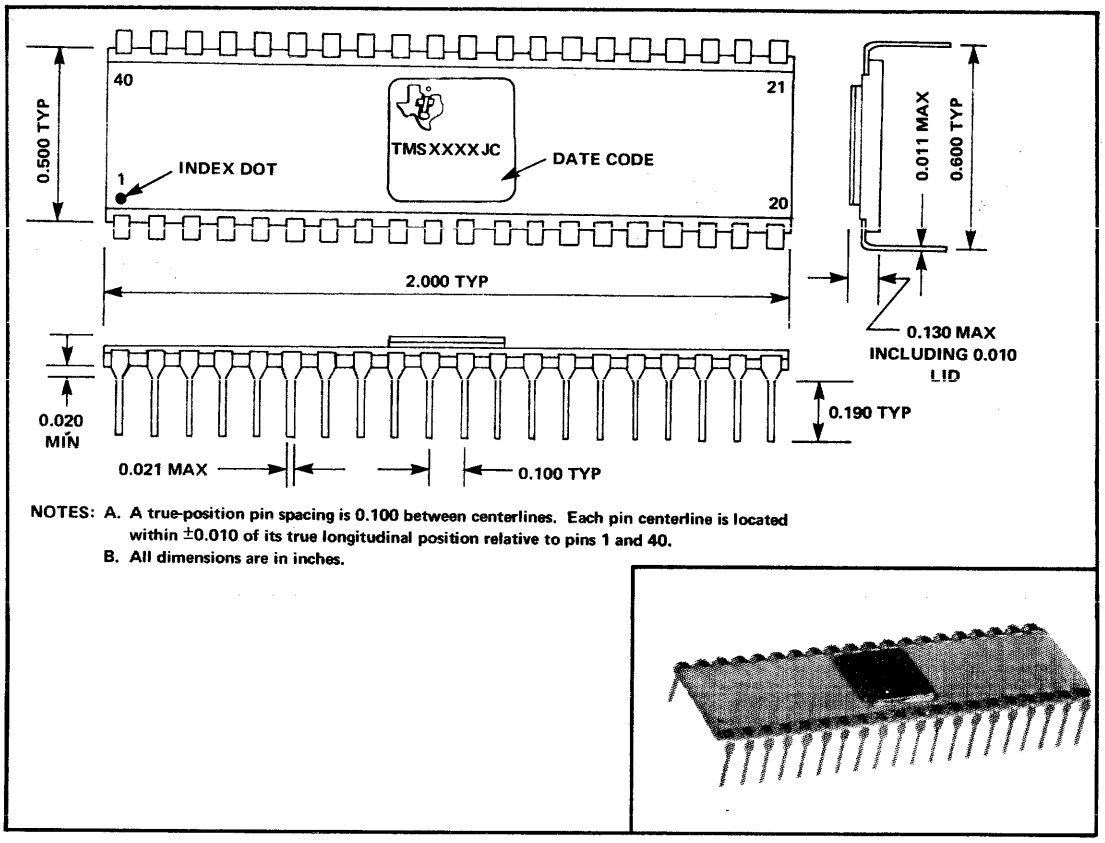


NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 28.

B. All dimensions are in inches.

14

40-pin package



NOTES: A. A true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 40.
B. All dimensions are in inches.

d) Plastic packages

Over the last two years TI has developed methods of plastic encapsulation specially adapted to MOS/LSI circuits. A proprietary plastic compound and proprietary methods are employed to ensure a level of reliability comparable to that of hermetically sealed packages and at substantial cost savings. A reliability report available from TI (Bulletin CB-132) describes the results obtained after several million plastic-packaged-device hours of life test.

The following plastic packages are presently in use:

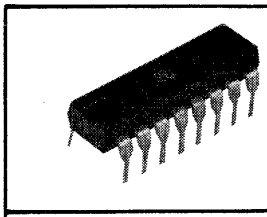
	16 PIN	18 PIN	24 PIN	28 PIN	40 PIN
300 MILS BETWEEN ROWS	X	X			
600 MILS BETWEEN ROWS	X		X	X	X

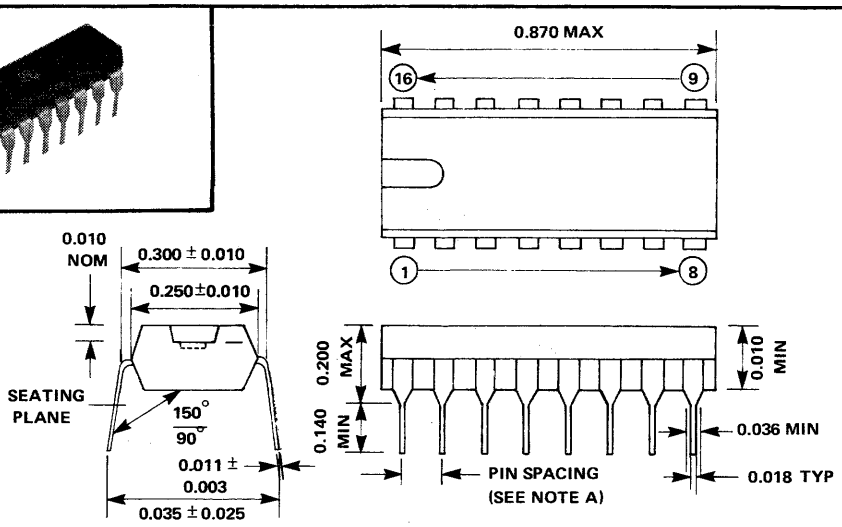
14

The spacing between leads and between rows as well as the physical dimensions of the packages are identical to those of the ceramic packages. The pin configuration in plastic and in ceramic is always the same. The users who have designed in TI's standard devices over the years can now take advantage of the considerable cost savings provided by plastic without having to modify their systems.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

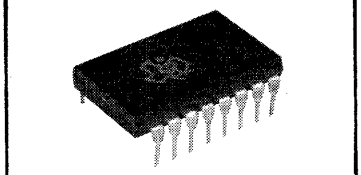
16-pin package (300-mil row spacing)





NOTES: A. The true position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 16.
B. All dimensions in inches unless otherwise noted.

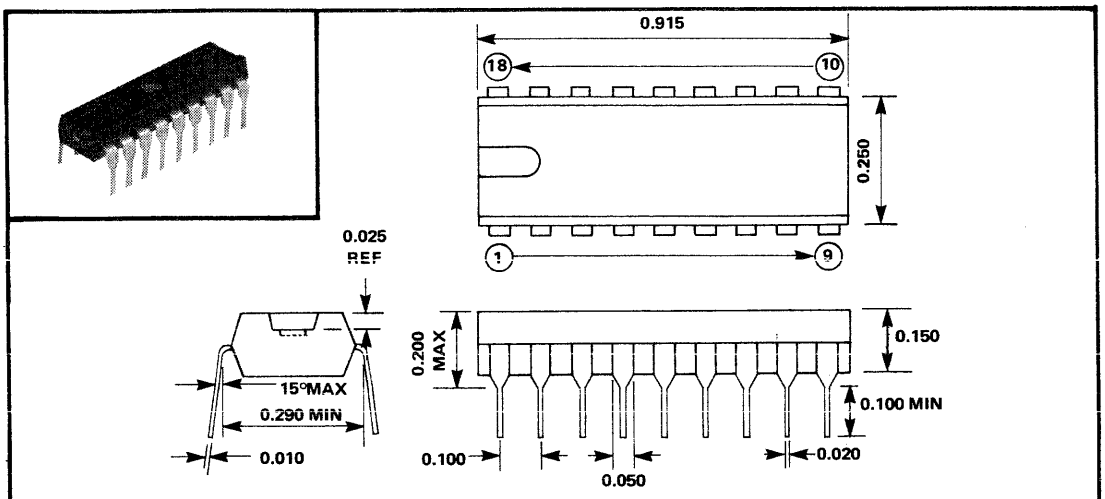
16-pin package (600-mil row spacing)



NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 24.
B. All dimensions are in inches unless otherwise noted.

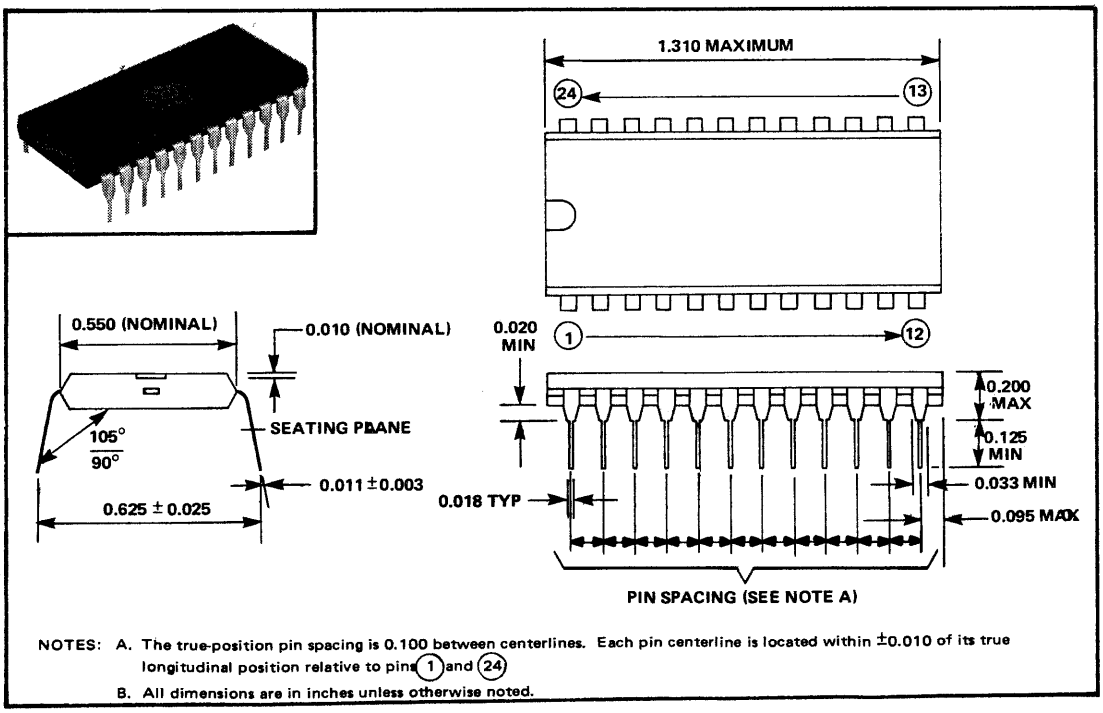
14

18-pin package



NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 18.
B. All dimensions in inches unless otherwise noted.

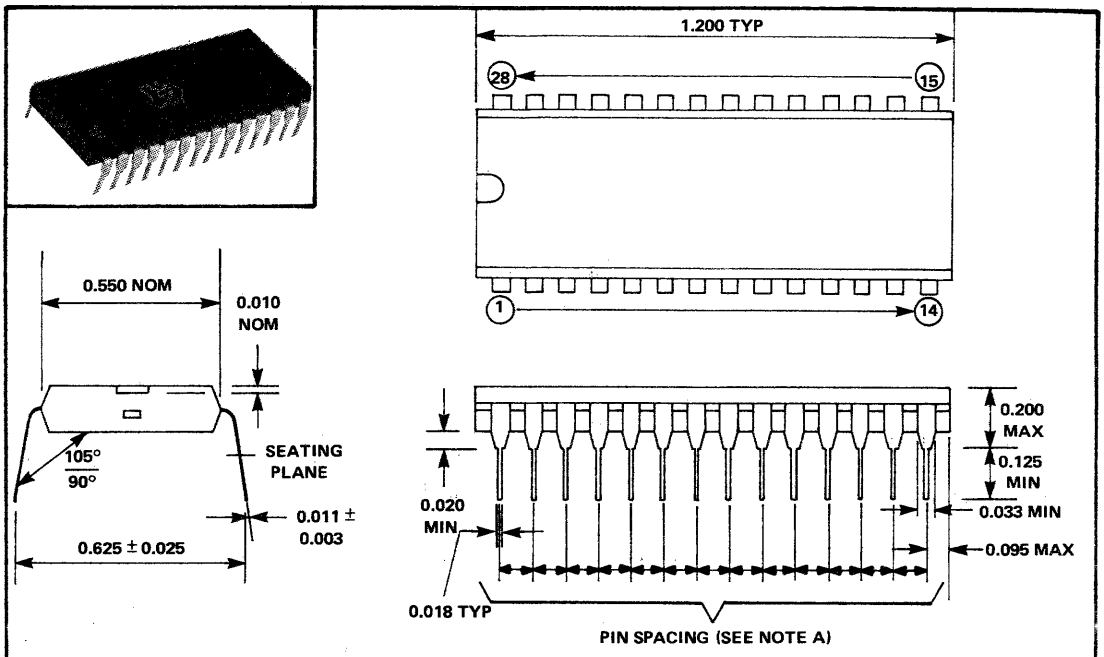
24-pin package



NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 24.
B. All dimensions are in inches unless otherwise noted.

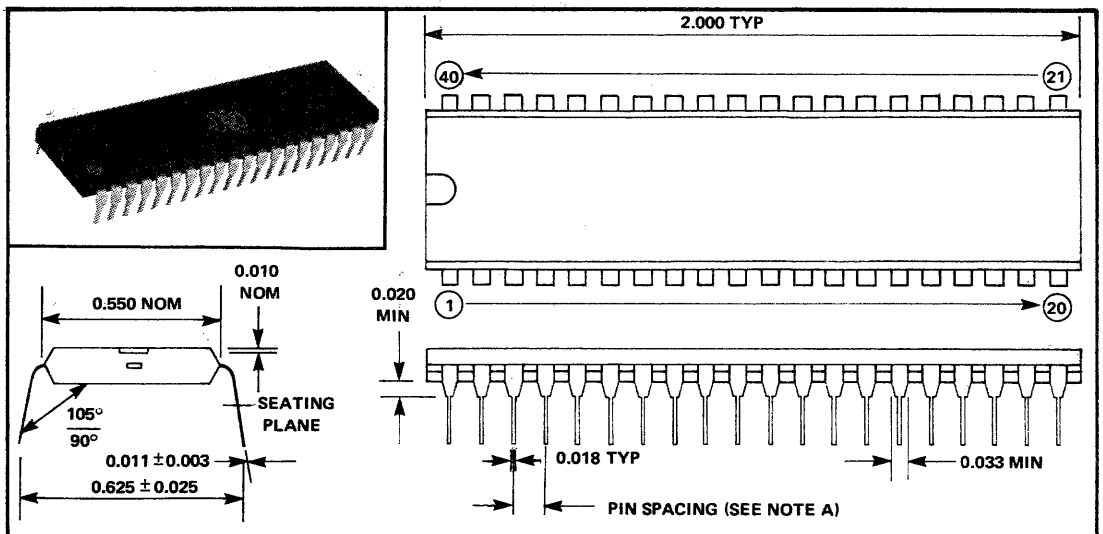
14

28-pin package



NOTES: A. The true position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 28.
B. All dimensions are in inches unless otherwise noted.

40-pin package



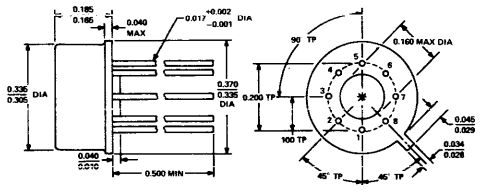
NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 40.
B. All dimensions are in inches unless otherwise noted.

14

3) Plug-in-type packages

For devices such as shift registers requiring few inputs and outputs, TI uses two plug-in type packages.

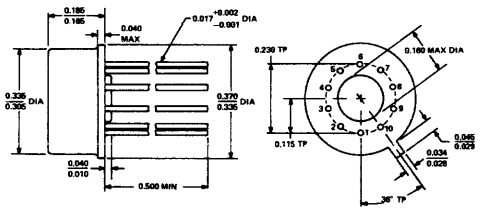
8-PIN PLUG-IN PACKAGE



Same as JEDEC TO-99 and MO-002AK except for diameter of standoff

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

10-PIN PLUG-IN PACKAGE



Same as JEDEC TO-100 and MO-006AD except for diameter of standoff

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

4) Manufacturing information

a) Alloying

Alloying is performed under inert atmosphere. A silicon gold eutectic is formed during the alloying operation.

14

b) Bonding

Thermal compression bonding is used. Typical bond strength is 5 grams. Bond strength is monitored on a lot-to-lot basis. Any bond strength of less than 2½ grams causes rejection of the entire lot of devices.

c) Sealing

TI uses a low temperature gold-tin brazing to seal ceramic packages.

Plug-in-type packages are welded.

Glass leaks are eliminated by using an etheylene glycol solution heated to +150°C.

Fine-leak elimination is performed through mass spectrometer techniques.

All MOS/LSI devices produced by TI are capable of withstanding 5×10^{-7} ppm fine-leak inspection, and may be screened to 5×10^{-8} ppm fine leak if desired by the customer for special applications.

d) Shock and Vibration

All packages are capable of withstanding a shock of 3,000 Gs.

All devices are capable of passing a 20,000-G acceleration (centrifuge) test in the Y axis.

Pin strength is measured by a pin-shearing test. All pins are able to withstand the application of a force of 6 pounds at 45° in the peel-off direction.

MOS/LSI SYSTEM COMPATIBILITY

MOS/LSI circuits have proven conclusively in the past few years their value to system designers. Most designs presently under consideration use both MOS/LSI and bipolar technologies in order to take full advantage of the low cost and high packaging density of MOS/LSI, as well as the flexibility of bipolar techniques for low complexity functions. With present MOS/LSI devices the task of the designer has been greatly simplifier. The devices do not require separate interface circuits between MOS and MOS circuits nor between bipolar and MOS circuits. MOS/MOS and MOS/bipolar compatibility is demonstrated in each of the data sheets included in this catalog. The following information is general and applicable to all TI MOS/LSI devices.

1) POWER SUPPLIES

Two manufacturing technologies are common in MOS/LSI and common throughout the industry: High-threshold MOS and Low-threshold MOS. The power supply requirements generally are:

	V_{SS}	V_{DD}	V_{GG}
High Threshold	0	−12 V	−24 V
Low Threshold	0	−5 V	−17 V

Where

V_{SS} is the substrate supply

V_{DD} is the drain supply

V_{GG} is the gate supply

The drain supply will draw most of the current. Some circuits are designed to use only one power supply (saturated logic). V_{DD} and V_{GG} are then common.

To use MOS in a system it is often convenient to translate all the power supply voltages by a certain voltage. The common arrangement is:

	V_{SS}	V_{DD}	V_{GG}
High Threshold	+12 V	0 V	−12 V
Low Threshold	+5 V	0 V	−12 V

NOTE: Some high-threshold devices are specified at V_{GG} = −28 V and V_{DD} = −14 V.

2) COMPATIBILITY

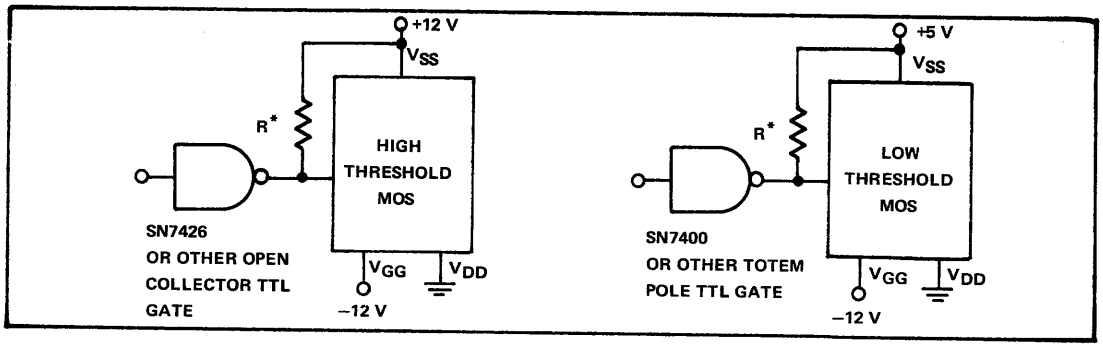
Referencing all voltages to V_{SS}, the input swing on most MOS circuits is as follows:

	High Level	Low level
High Threshold	0 to −3 V	−9 V to −24 V
Low Threshold	0 to −1.5 V	−4.2 V to −17 V

Relating to the translated power supplies as above this becomes:

	High Threshold	Low Threshold
V_{SS}	+12 V	+5 V
V_{DD}	0 V	0 V
V_{GG}	−12 V	−12 V
High level	+9 V to +12 V	+3.5 V to +5 V
Low level	+3 V to −12 V	0.8 V to −12 V

In all cases the input of the MOS circuit will look like a very high impedance. The input compatibility is easily achieved.



* The value of the R resistor varies depending on speed-power requirements. In many cases this resistor is diffused on the MOS chip. For low-threshold MOS the resistor assures that the worst-case TTL output is pulled up to at least 3.5 V for proper MOS circuit operation.

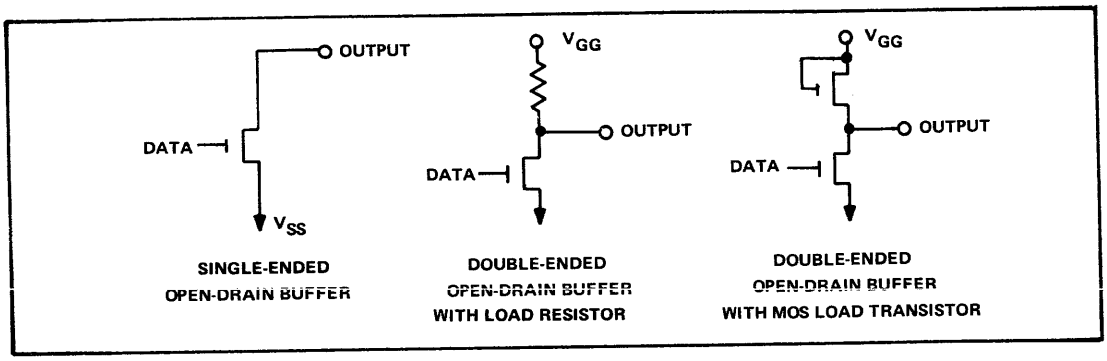
3) OUTPUT COMPATIBILITY

Three types of buffers are commonly used on MOS devices:

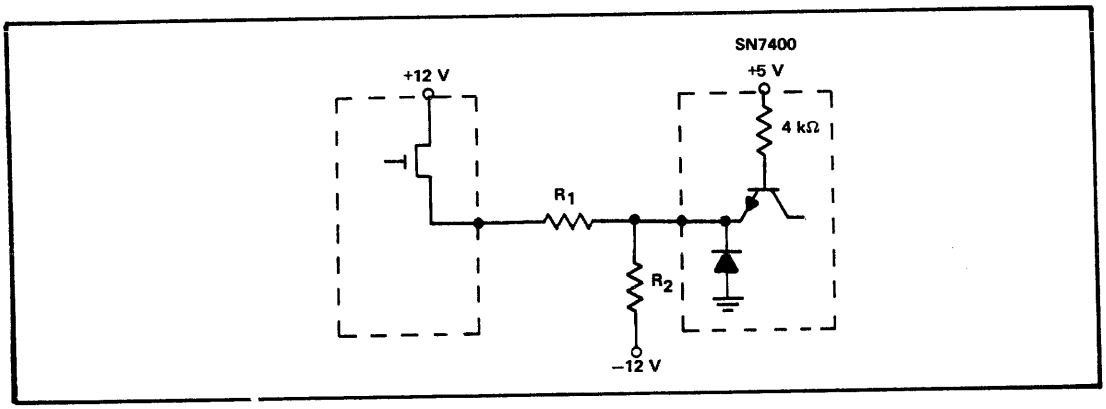
- Single-ended open-drain
- Double-ended
- Push-pull

a) Single-ended open-drain and double-ended

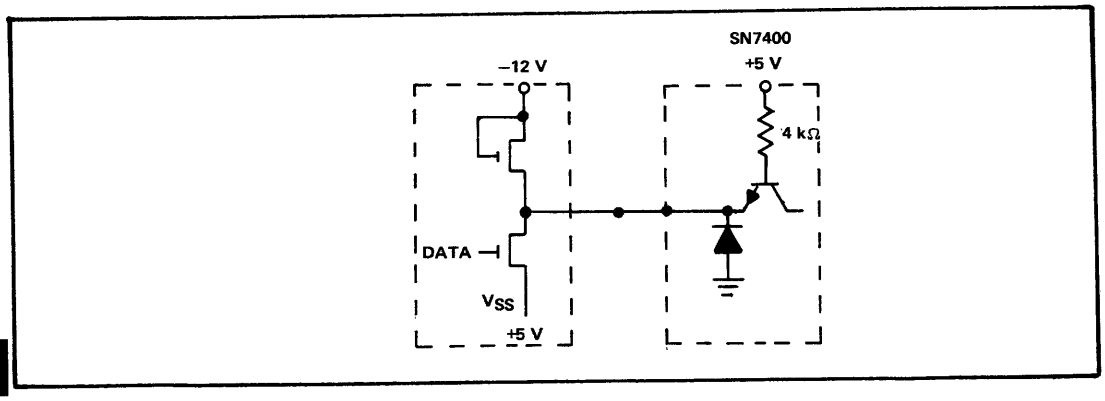
The buffer is simply a current switch. In the "off" state the impedance of the buffer is extremely large, while in the "on" state it is typically under 1 kΩ. A discrete resistor or an MOS transistor may be used as a load with a single-ended open-drain buffer. This resistor or the transistor may be internal to the MOS circuit. When the load transistor is internal to the MOS circuit, the buffer is called a double-ended buffer.



In every case compatibility with MOS is easily achieved. For instance, a single-ended buffer with high-threshold MOS:

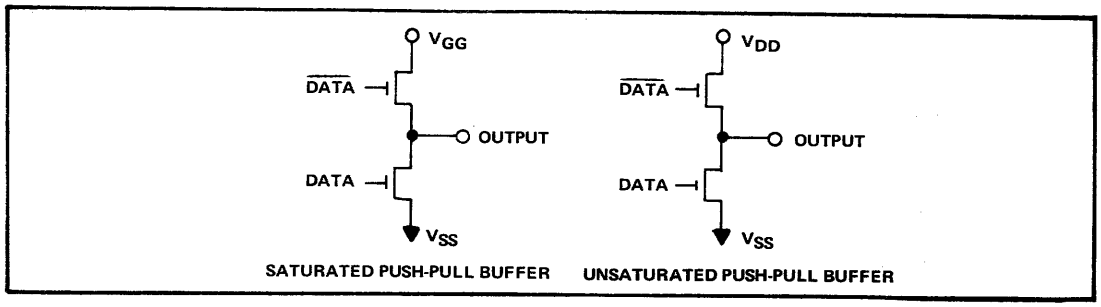


R_2 provides the necessary current sink for the TTL input; R_1 limits the positive excursion to +5 V. If used for low-threshold MOS, V_{SS} is translated up to +5 V instead of +12 V and R_1 can be eliminated. If R_2 is on the chip, no external components are necessary.



b) Push-pull buffer

Two types are common:



The unsaturated push-pull buffer is the most commonly used for low-threshold circuits. It permits direct TTL compatibility without external components. It will also drive directly other low-threshold MOS circuits. This buffer type is used on most of the new MOS/LSI circuits produced by TI.

4) CLOCKS

Depending on the circuit type, there are different clock requirements:

No clocks – Static RAMs, ROMs, etc.

1 clock – with other clocks generated internally

2 clocks – most shift registers

4 clocks – very high-speed low-power-dissipation shift registers

a) One external clock

An internal circuit generates the clocks from a single outside clock signal. The outside clock signal has the same swing as the data input signal and the compatibility is identical (see preceeding paragraph 3).

Single-clock low-threshold MOS circuits will accept a TTL clock without adding components.

b) Two or four clocks

The clock signals must swing between V_{SS} and V_{GG}. To go from a single-TTL-level clock to a multiple-MOS-level clock, two circuits are required: 1) a clock generator to generate the necessary clock pulses, and 2) a clock driver to bring the clock levels to the required values. In most cases only one clock circuit is needed for an entire MOS/LSI system.

SHIFT REGISTERS

In all digital equipment there is a need to temporarily store and transfer data. MOS shift registers are ideally suited for these applications, because they can store economically very large amounts of information.

1) Basic Configuration

MOS shift registers can be supplied in the following configurations:

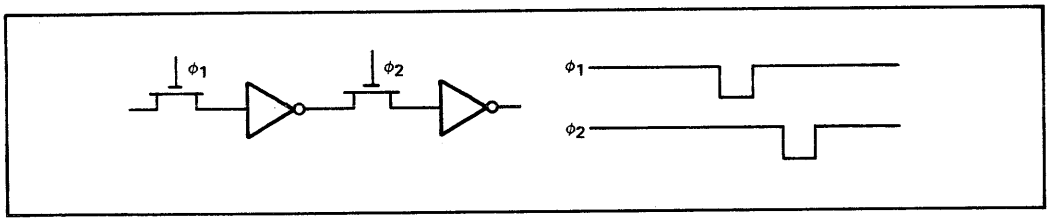
Serial-in/Serial-out

Parallel-in/Serial-out

Serial-in/Parallel-out

The serial-in/serial-out configuration is by far the most popular.

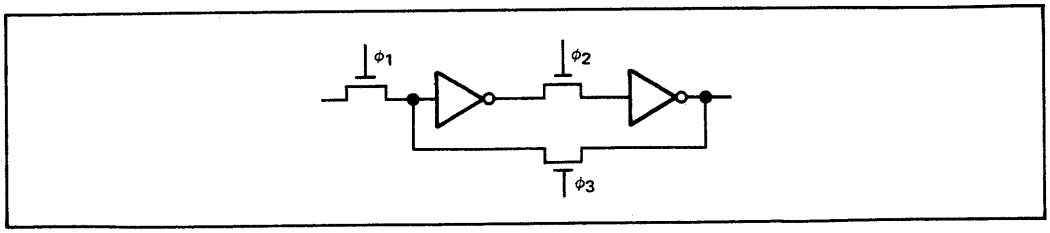
An MOS shift register will be able to store N bits. Each bit is stored on a basic cell consisting of two MOS inverters and timing devices.



2) Static or Dynamic

Dynamic shift registers use two independent inverters (not cross-coupled). The data is temporarily stored on a capacitor inherent to an MOS device. The device can not be operated below a certain clock frequency, or the data storage will be lost.

A static shift register operates the same way a dynamic shift register does, as long as the frequency is high. The two inverters used in a static shift register are the static type (unclocked loads). When the frequency falls below a certain level, a third phase is generated internally and this signal is used to close a feedback loop between the output of the second inverter and the input of the first one.

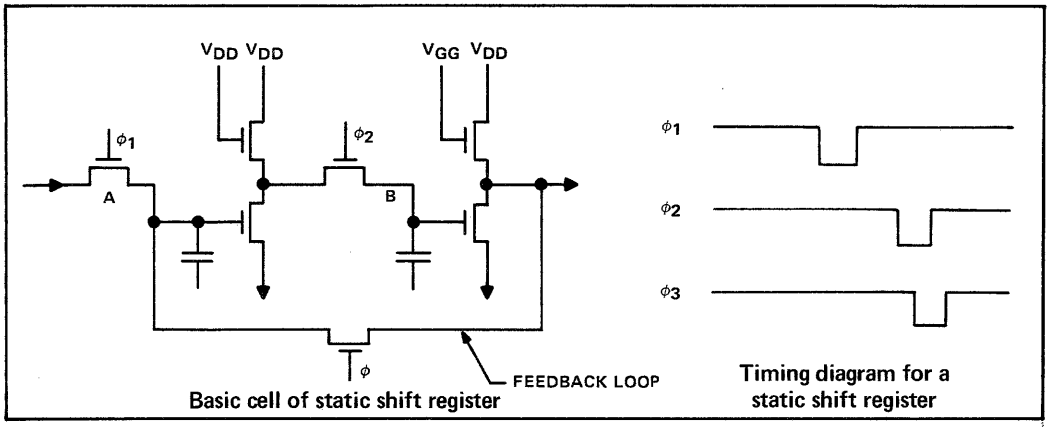


TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Dynamic shift registers are faster than static registers and dissipate less power. They are not as flexible to use in a system.

a) **Static Shift Registers**

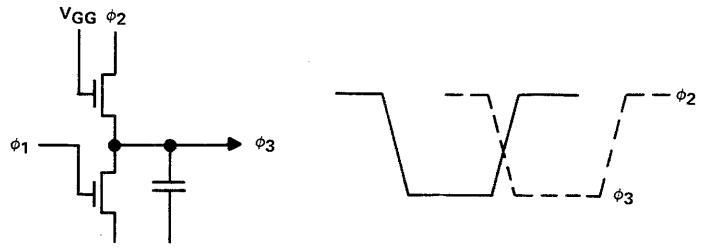
A static shift register uses two static MOS inverters. Three phases (clocks) are necessary for operation. The third-phase clock is always generated internally. The third phase times the feedback loop. The second-clock phase is often generated internally.



Basic cell of static shift register

Timing diagram for a static shift register

A and B are storage nodes. The device operates dynamically except when ϕ_3 is On. ϕ_3 is On when $\phi_1 = 0$ and $\phi_2 = 1$ for more than 10 microseconds. ϕ_3 is delayed ϕ_2 generated by an inverter. Load devices are On all the time. The third phase is generated whenever ϕ_1 stays at a logic 0 and ϕ_2 at a logic 1 for more than 10 microseconds.



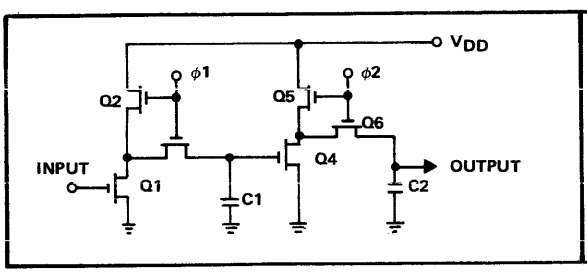
ϕ_3 Generation

Static shift registers operate in the 0- to 2.5-MHz clock range. They are extremely flexible and data can be held indefinitely, as long as power is supplied.

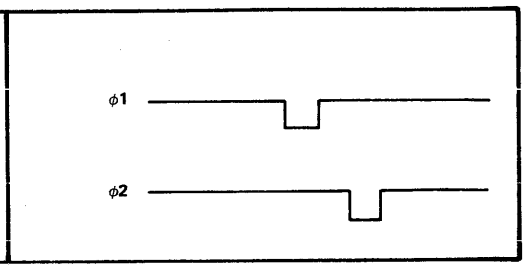
b) Dynamic Shift Registers

Dynamic shift registers use either two or four phases (clocks). These phases can be generated on the chip or be supplied externally. Two-phase shift registers can be classified as ratio and ratioless circuits.

The two-phase ratio-type shift register consists of two simple dynamic inverters and of timing devices.



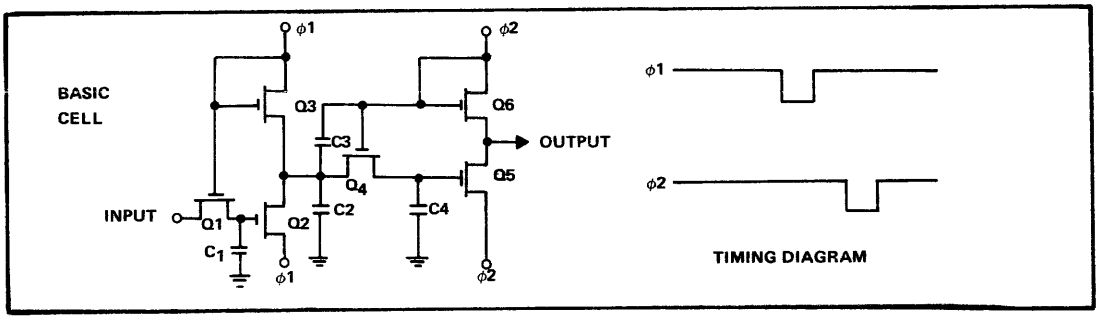
Basic cell for a dynamic shift register



Timing diagram for a 2 phase dynamic shift register

When ϕ_1 is at a logic level 1 (low) the capacitance C_1 charges at the inverse of the data input. Data is transferred out when ϕ_2 goes to 1.

The two-phase ratioless dynamic shift register has been designed to decrease the power dissipation and the chip area. In a ratio-type circuit, current flows through the inverter when the clock and data input are simultaneously at a logic 1. There must be a certain minimum ratio between the size of the two MOS transistors in the inverters (typically>5:1). This will require more chip area than in a ratioless shift register, in which the MOS devices used are usually identical in size.

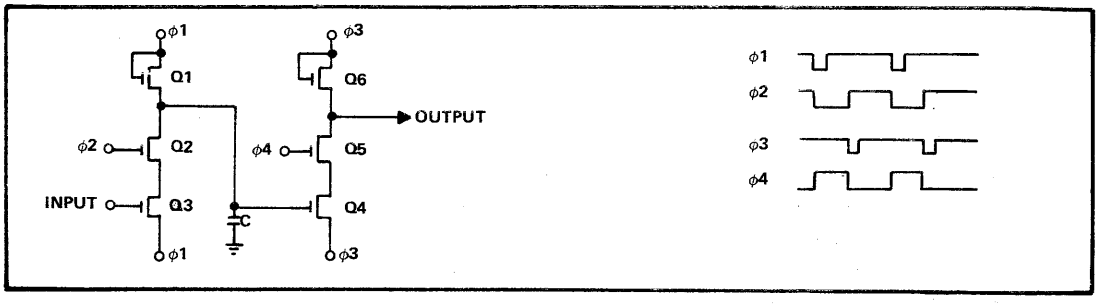


Two-phase ratioless dynamic shift register

The two-phase ratioless dynamic shift register uses identical transistors throughout and can therefore work at higher clock rates because the precharging paths are of lower impedance than those in the ratio circuit. When ϕ_1 goes to '1' C_2 charges to '1' via Q_3, and C_1 charges to the data input level via Q_1. When ϕ_1 returns to '0', transistor Q_2 turn On if the Input level was a '1' and discharges C_2. For a '0' input, Q_2 stays Off and C_2 is not discharged. Now ϕ_2 goes to a '1' and turns on Q_4 so that C_2 shares any charge it has with C_4. C_3 is used to compensate for the loss of potential across C_2 by introducing a small extra charge on the negative edge of ϕ_2. It does not introduce enough to destroy a logic '0' on C_2. When ϕ_2 returns to a '0', the charge on C_4 transfers the data-input level to the Output.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Four-phase shift registers are used for very high density circuits operated at very high speed.



Four-phase shift register basic cell and timing diagram

In the basic four-phase dynamic shift register, C is precharged via Q_1 during ϕ_1. After ϕ_1, ϕ_2 holds Q_2 On, so C takes a level which is the inverse of the input. The process is repeated by the Slave section $Q_4 - Q_6$ so that the Input level is transferred to the Output after ϕ_3 and during ϕ_4. The stage uses similar transistors throughout, giving high package density. Power dissipation is low, speed can be high, but a relatively complex clock drive circuit is required.

3) MOS Shift Registers from TI

	CLOCK	LOGIC	POWER SUPPLY	FREQUENCY	NUMBER OF BITS
TMS 3000 LR	2	Static	+14 V, −14 V	0 – 1 MHz	2 X 25
TMS 3001 LR	2	Static	+14 V, −14 V	0 – 1 MHz	2 X 32
TMS 3002 LR	2	Static	+14 V, −14 V	0 – 1 MHz	2 X 50
TMS 3003 LR	2	Static	+14 V, −14 V	0 – 1 MHz	2 X 100
TMS 3012 JR/NC	1	Static	+14 V, −14 V	0 – 1 MHz	2 X 128 (Accumulator)
TMS 3016 LR	2	Static	+14 V, −14 V	0 – 1 MHz	2 X 16
TMS 3028 LR	1	Static	+14 V, −14 V	0 – 1 MHz	2 X 128
TMS 3101 LC/NC	2	Static	+5 V, −12 V	0 – 2.5 MHz	2 X 100
TMS 3102 LC/NC	2	Static	+5 V, −12 V	0 – 2.5 MHz	2 X 80
TMS 3103 LC/NC	2	Static	+5 V, −12 V	0 – 2.5 MHz	2 X 64
TMS 3112 JC/NC	1	Static	+5 V, −12 V	0 – 1 MHz	6 X 32
TMS 3113 JC/NC		Static	+5 V, −12 V	0 – 2.0 MHz	2 X 133
TMS 3114 JC/NC		Static	+5 V, −12 V	0 – 7.0 MHz	2 X 128
TMS 3304 LR	2	Dynamic	+14 V, −14 V	10 kHz – 5 MHz	3 X 66
TMS 3305 LR	2	Dynamic	+14 V, −14 V	10 kHz – 5 MHz	3 X 64
TMS 3309 LR	4	Dynamic	+12 V, −12 V	10 kHz – 10 MHz	2 X 512
TMS 3314 JR	2	Dynamic	+14 V, −14 V	10 kHz – 2 MHz	3(60 + 4)
TMS 3401 LC	2	Dynamic	+5 V, −12 V	20 kHz – 5 MHz	1 X 512
TMS 3402 LC	2	Dynamic	+5 V, −12 V	20 kHz – 5 MHz	1 X 500
TMS 3404 LC/NC	2	Dynamic	+5 V, −12 V		2 X 512
TMS 3409 JC/NC	1	Dynamic	+5 V, −12 V	10 kHz – 25 MHz	4 X 80
TMS 3412 JC/NC	2	Dynamic	+5 V, −5 V	10 kHz – 6 MHz	4 X 256
TMS 3413 LC/NC	2	Dynamic	+5 V, −5 V	10 kHz – 6 MHz	2 X 512
TMS 3414 LC/NC	2	Dynamic	+5 V, −5 V	10 kHz – 6 MHz	1 X 1024

4) Application

MOS shift registers have met a very wide market acceptance. They have become extremely price competitive and are widely used for memories as well as to replace magneto-stricture and glass-delay lines.

Typical Applications are:

- Data handling
- Refresh memories
- Buffer memories
- Scratch-pad memories
- Delay line
- Desk-top calculators
- Display systems
- Peripherals
- Radar systems

The advantages of MOS shift registers over conventional delay lines and core storage are:

- Price
- Modularity
- Speed
- Physical size
- Physical integrity
- Temperature range

In data handling applications, MOS shift registers can be used either in digit-serial/bit-serial mode or in digit-serial/bit-parallel mode. The latter offers the highest speed of operation but increases the cost of hardware.

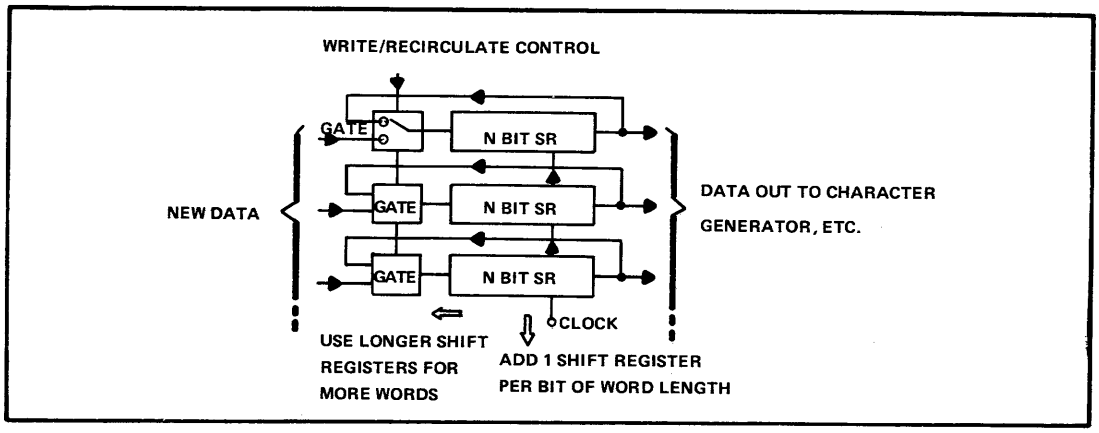
In the digit-serial/bit-parallel mode it is convenient to store one digit in a small separate register for operations such as carry correction, loop equalization, and shift. This is achieved in devices such as the TMS 3314 JR triple-60 plus triple-4 shift register.

Any N-bit shift register can be used as a refresh memory by returning outputs to inputs as shown. A particular bit of information is available at the output every

$$\frac{N}{\text{clock frequency}} \text{ seconds.}$$

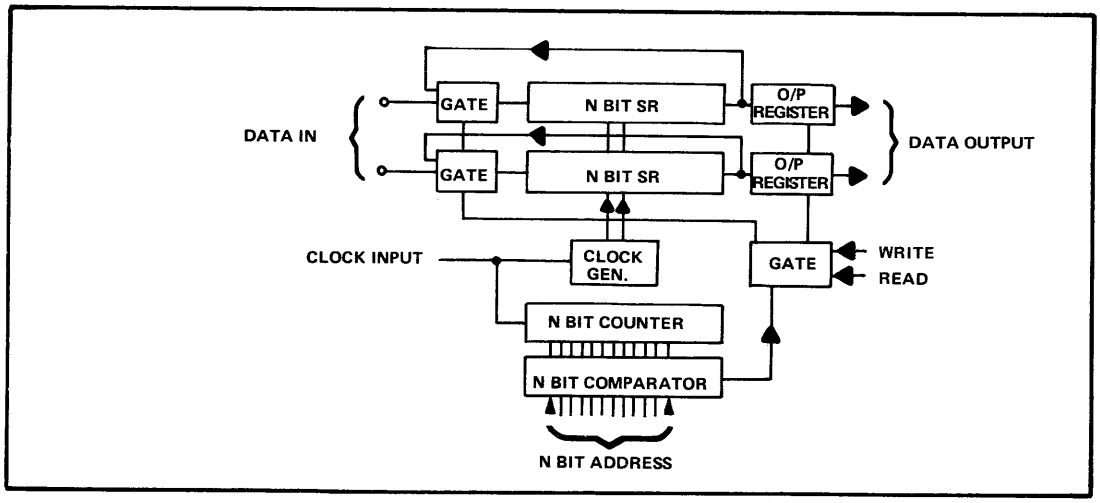
This is particularly useful for renewing fading displays such as CRT character-generator systems. New data is written in via a 2-way input gate circuit.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222



Shift registers used as refresh memory

By adding an address counter and comparator in the refresh memory, it becomes a "scratch pad" memory. Data can be written into and read out of any point specified by the input address code. An output register is necessary to store the required output data and to provide a 1-bit delay so that the Read address is the same as the Write address because there is a 1-bit delay between output and input.

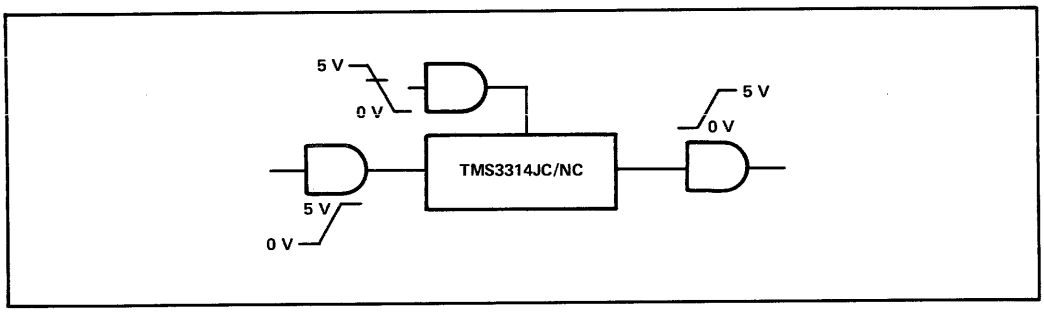


Shift registers used as scratch pad memory

14

5) Clocking the Shift Registers

Most of the new shift registers designed by Texas Instruments feature *total TTL compatibility*. A clock driver is included on the chip and the clock line is driven directly by TTL. For examples of this configuration, see the specifications for the TMS 3314 JC/NC and the TMS 3409 JC/NC.

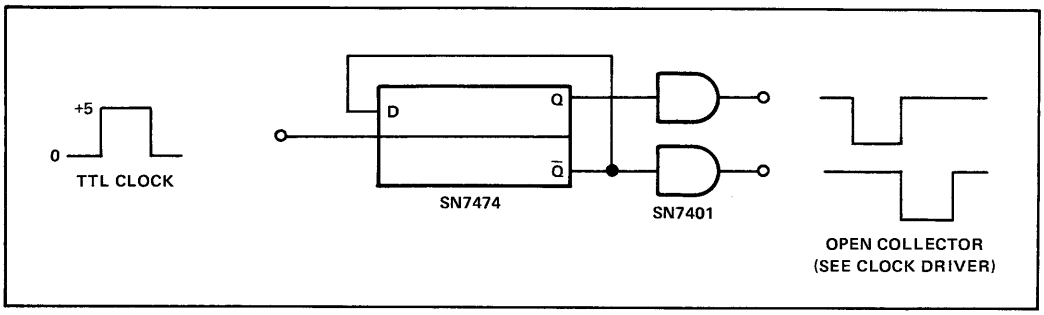


Older circuits use two clock lines with a V_{GG} swing. The user must:

- Generate the clocks
- Level shift the clocks

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Generating the two nonoverlapping clocks is a simple matter, easily accomplished through a D-type flip-flop.

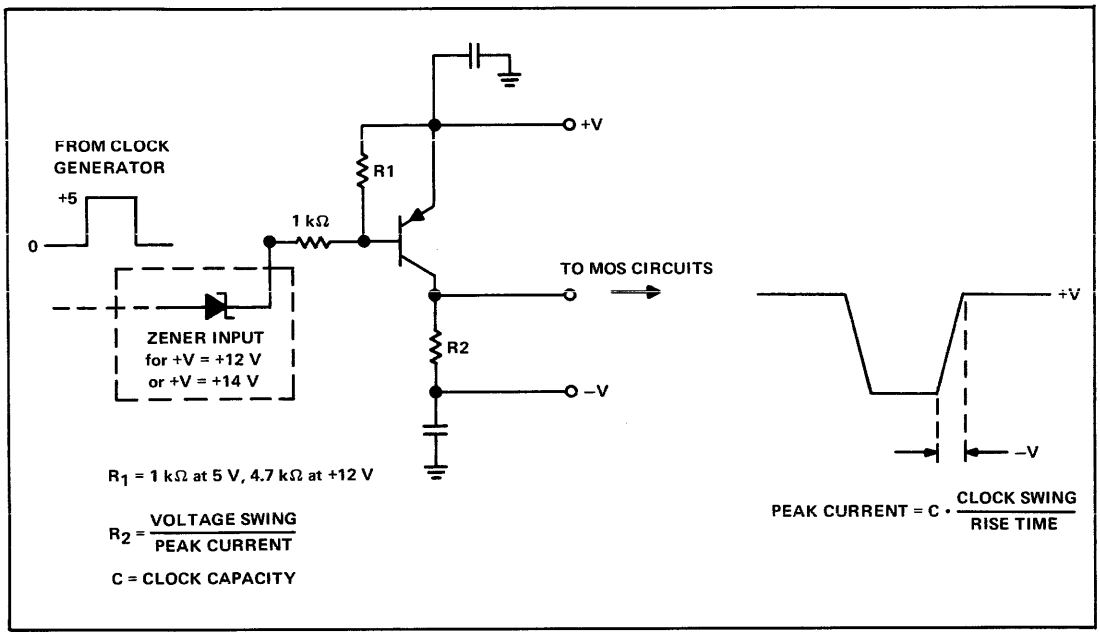


This arrangement is favorable because Q and $\overline{Q}$ will be of opposite polarities when the TTL clock is stopped and this allows static storage in static shift registers.

Should four phases be generated, the user would connect two D-type flip-flops as a Johnson counter.

Once the clocks are generated, the voltage level must be shifted to the appropriate value.

This can be achieved easily as shown in the illustration below. The clock driver circuit is used to drive a capacitive load (clock lines capacitance) between +V and −V.



Typical clock driver circuits

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS
LSI

TMS 3000 LR-DUAL 25-BIT STATIC SHIFT REGISTER
TMS 3001 LR-DUAL 32-BIT STATIC SHIFT REGISTER

FEBRUARY 1971

features

- Static logic
- DC to 1 MHz operation
- Low power dissipation
- Push-pull output buffers
- TTL compatible

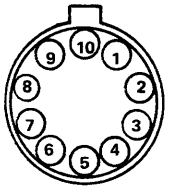
description

The TMS 3000 LR and TMS 3001 LR are dual static shift registers. Each device contains two dc-to-1-MHz shift registers with independent input and output terminals and common clocks and power. MOS thick-oxide technology is used to fabricate cross-coupled flip-flops for each register bit so that data can be stored indefinitely. Transistors in the device are P-channel enhancement-mode type. All input leads have zener network protection and all outputs contain low-output-impedance, non-inverting push-pull output buffers.

Two power supply levels and two clocks are required for operation with a third clock generated internally. Data is transferred into the register when the ϕ_1 clock is pulsed to logic 1. Data is shifted when the ϕ_1 clock is returned to logic 0 and the ϕ_2 clock is pulsed to logic 1. Output data appears on the logic 0 to logic 1 transition of the ϕ_2 clock. For long term storage, the ϕ_1 clock must be held at logic 0 and the ϕ_2 clock at logic 1.

mechanical data and pin configuration

The TMS 3000 LR and TMS 3001 LR are mounted in TO-100 packages. (See MOS/LSI packaging section.)



BOTTOM VIEW

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Input 1	6	Clock ϕ_2
2	Output 1	7	V_{GG}
3	V_{DD}	8	Output 2
4	Clock ϕ_1	9	Input 2
5	GND (V_{SS})	10	No connection

logic definition

Negative logic is assumed

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−30 V to 0.3 V
Phase one clock input voltage $V_{\phi 1}$ range (See Note 1)	−30 V to 0.3 V
Phase two clock input voltage $V_{\phi 2}$ range (See Note 1)	−30 V to 0.3 V
Data input voltage V_I range (See Note 1)	−30 V to 0.3 V
Power dissipation	450 mW
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal, V_{SS}.

14

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−12	−14	−15	V
Supply voltage V_{GG}	−24	−28	−29	V
Logic 0 data input voltage $V_{i(0)}$ (See Note 2)	0.3	0	−2	V
Logic 1 data input voltage $V_{i(1)}$ (See Note 2)	−9.5	−14	−29	V
Width of data pulse, $t_{p(data)}$ (See voltage waveforms)	0.4†			μs
Data setup time, t_{setup} (See voltage waveforms and Note 3)	100			ns
Data hold time, t_{hold} (See voltage waveforms and Note 4)	20			ns
Logic 0 clock input voltage $V_{\phi 0(clock)}$ (See Notes 2 and 5)	0.3	0	2	V
Logic 1 clock input voltage $V_{\phi 1(clock)}$ (See Notes 2 and 5)	−24	−28	−29	V
Rise time of clock pulse, $t_{r(clock)}$ (See voltage waveforms)	0		5	μs
Fall time of clock pulse, $t_{f(clock)}$ (See voltage waveforms)			5	μs
ϕ_1 clock pulse width, $t_{p(\phi 1)}$ (See voltage waveforms)	0.3†		10†	μs
ϕ_2 clock pulse width, $t_{p(\phi 2)}$ (See voltage waveforms)	0.4†		∞†	μs
Time interval from ϕ_1 clock to ϕ_2 clock input pulse, $t_{\phi 12}$ (See waveforms and Note 5)	0.01		10	μs
Time interval from ϕ_2 clock to ϕ_1 clock input pulse, $t_{\phi 21}$ (See waveforms and Note 5)	0.01		10	μs
Clock repetition rate	0		1	MHz

NOTES: 2. These voltage values are with respect to network ground terminal, V_{SS}.

3. Setup time is the interval immediately preceeding the positive-going edge of the phase 1 clock during which period the data to be recognized must be maintained at the input to ensure its recognition.

4. Hold time is the interval immediately following the positive-going edge of the phase 1 clock during which period the data to be recognized must be maintained at the input to ensure its recognition.

5. The two clock pulses must never be simultaneously more than 3 volts more negative than V_{SS}.

† These values are at $V_{DD} = -14$ V, $V_{GG} = -28$ V, and $T_A = 25°C$.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNITS
I_{IL}	Logic 1 input current into data input	$V_I = -20$ V, $T° = 25°C$			0.5	μA
$I_{IL(\phi)}$	Logic 1 input current into either clock input	$V_I = -28$ V, $V_{GG} = 0$ V, $T° = 25°C$			50	μA
V_{OH}	Logic 0 output voltage	$I_O = 0$ mA, $C_L = 20$ pF		0.3	−1	V
		$I_O = 2$ mA, $C_L = 20$ pF		−2.6	−5	V
		$I_O = 0$ mA, $V_{dd} = -12$ V, $V_{gg} = -24$ V		−0.5	−1	V
V_{OL}	Logic 1 output voltage	$I_O = 0$, $C_L = 20$ pF	−12	−13.5	−14	V
		$I_O = 0.5$ mA	−10.5	−12.5	−14	V
		$I_O = 0$ mA, $V_{dd} = -12$ V, $V_{gg} = -24$ V, $V_\phi, V_{\phi L} = -24$ V, $C_L = 20$ pF, $V_{in(1)} = -8.5$ V, $V_{in(0)} = -2$ V	−8.8	−10.5	−12	V
R_{OH}	Output resistance, logic 0	$I_O = -2.0$ mA		1.5	2.5	kΩ
R_{OL}	Output resistance, logic 1	$I_O = 0.5$ mA		1.5	7	kΩ
I_{DD}	Supply current from V_{DD} terminal*	TMS 3000 LR, $T° = 25°C$		−14	−20	mA
		TMS 3001 LR, $T° = 25°C$		−16	−24	mA
I_{GG}	Supply current from V_{GG} terminal*	TMS 3000 LR, $T° = 25°C$		−2	−3.5	mA
		TMS 3001 LR, $T° = 25°C$		−2	−3.5	mA
f_{max}	Maximum clock frequency		1			MHz

† Unless otherwise noted, voltages are as shown in the nominal column of the recommended operating conditions (nominal operating voltages).
‡ All typical values are at $T_A = 25°C$.
* Current into a terminal is a positive value.

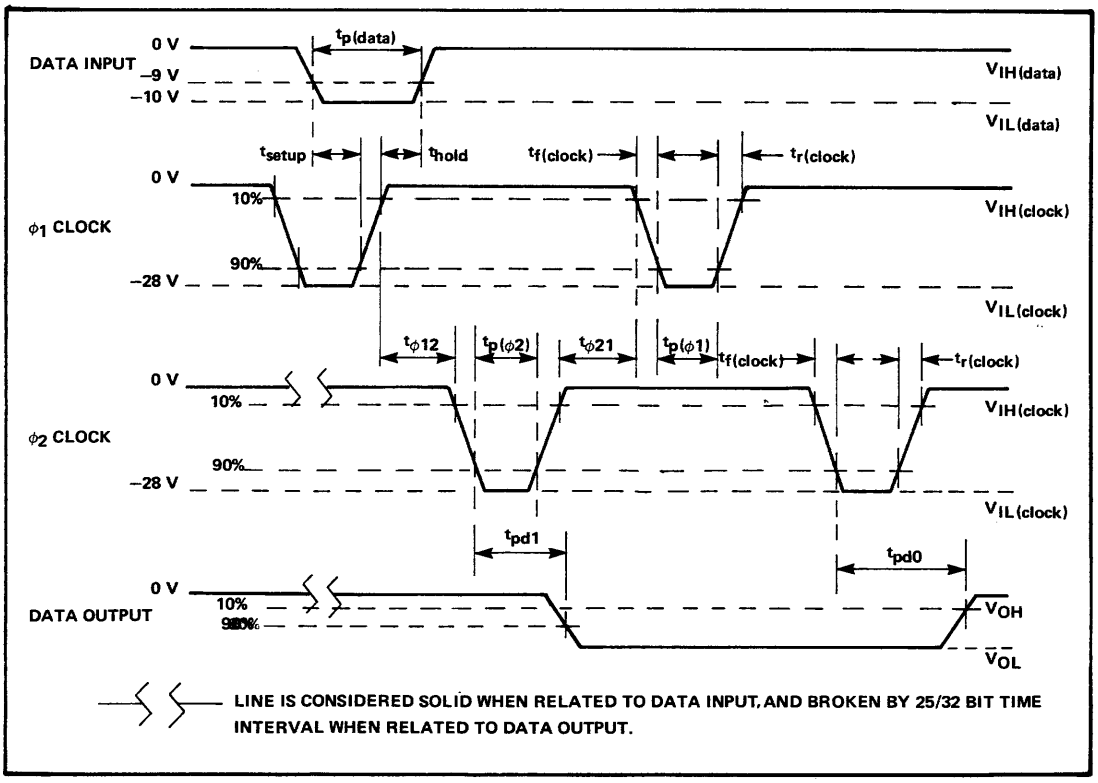
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics, V_{DD} = −14 V, V_{GG} = −28 V, R_L = 10 mΩ, C_L = 20 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation delay time to high level from ϕ_2 clock to data output	See voltage waveforms			325	475	ns
t_{pd1}	Propagation delay time to low level from ϕ_2 clock to data output	See voltage waveforms			325	475	ns
$C_{in(\phi1)}$	Capacitance of ϕ_1 clock input	V_I = 0 V, $V_{I(\phi2)}$ = 0 V, f = 1 MHz	TMS 3000 LR		8	12	pF
			TMS 3001 LR		11	15	pF
$C_{in(\phi2)}$	Capacitance of ϕ_2 clock input*	V_I = 0 V, $V_{I(\phi1)}$ = 0 V, f = 1 MHz	TMS 3000 LR		15	20	pF
			TMS 3001 LR		20	30	pF
C_{in}	Capacitance of data input	V_I = 0,	f = 1 MHz		5	7	pF

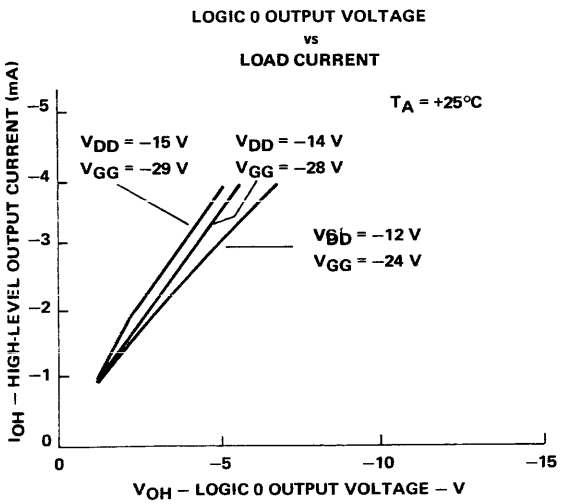
* $C_{in(\phi2)}$ includes the capacitance of the internal ϕ_2' clock.

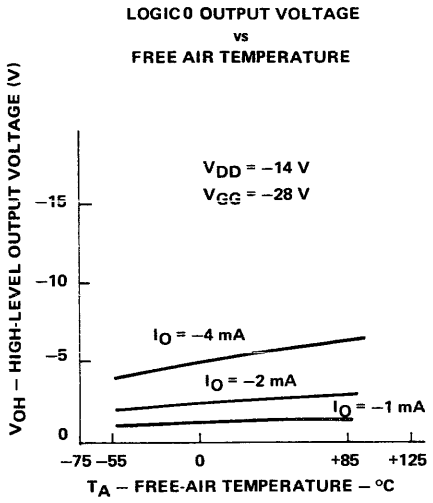
voltage waveforms

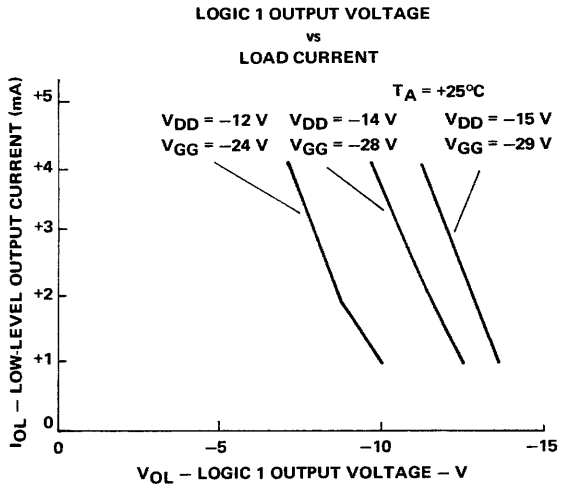


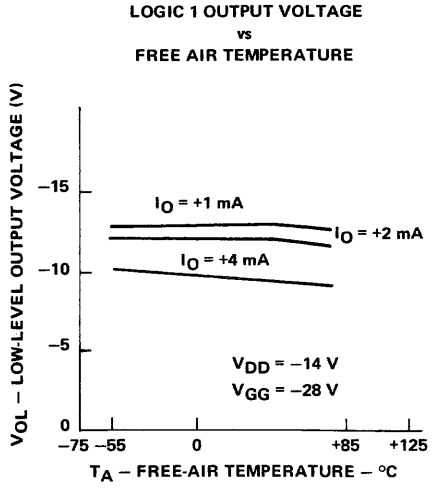
14

typical characteristics









typical application data

1) MOS/TTL interface

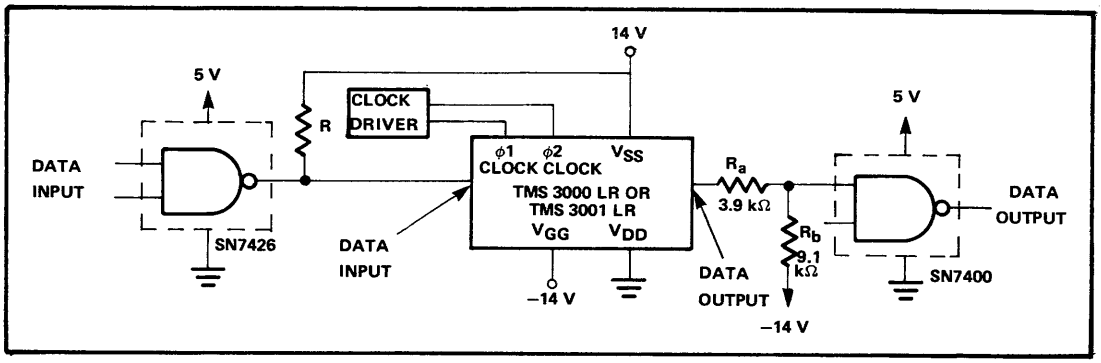
14

With proper supply voltages, interfacing can be achieved with only three resistors. A typical MOS/TTL interface is shown below.

An input pull-up resistor is required to provide the necessary input voltage swing. The value of this resistor (R) depends on the actual circuit requirements — values as low as 1 kΩ can be used for high-speed operation, while values as high as 15 kΩ can be used when low power consumption is important rather than high-speed.

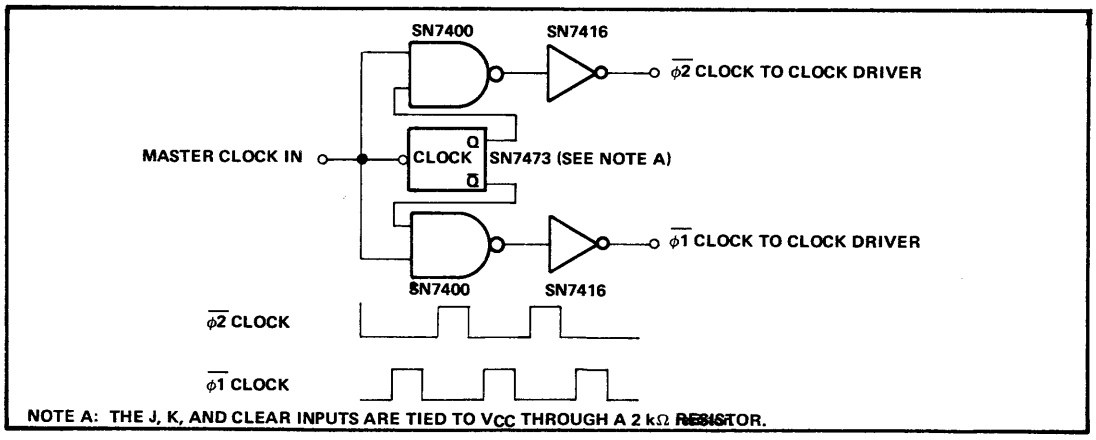
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

typical application data (continued)



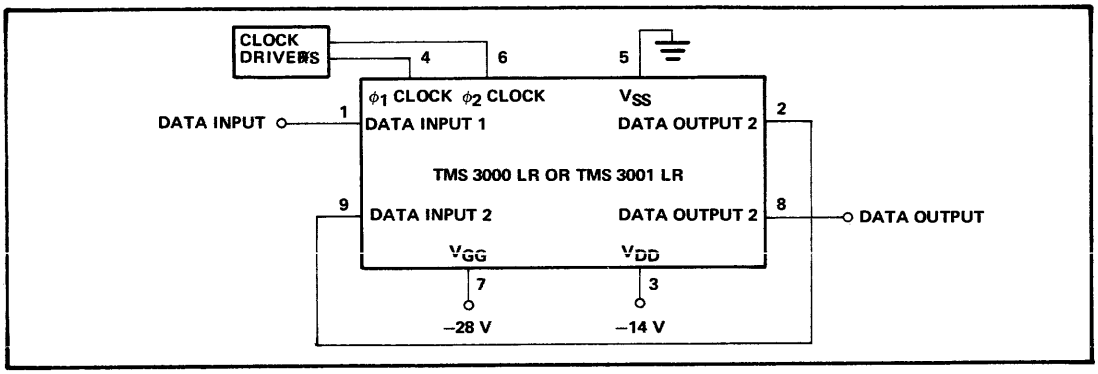
At the output interface, the 9.1-kΩ resistor sinks the 1.6 mA of TTL gate current when 0 volts is required on the TTL input. When 3 volts is required on the TTL input, the MOS output device supplies current from 14 volts, through the 3.9-kΩ resistor and the 9.1-kΩ resistor to −14 volts. The 3.9-kΩ resistor limits the voltage at the TTL gate input to 5 volts maximum.

2) Two-phase clock generator

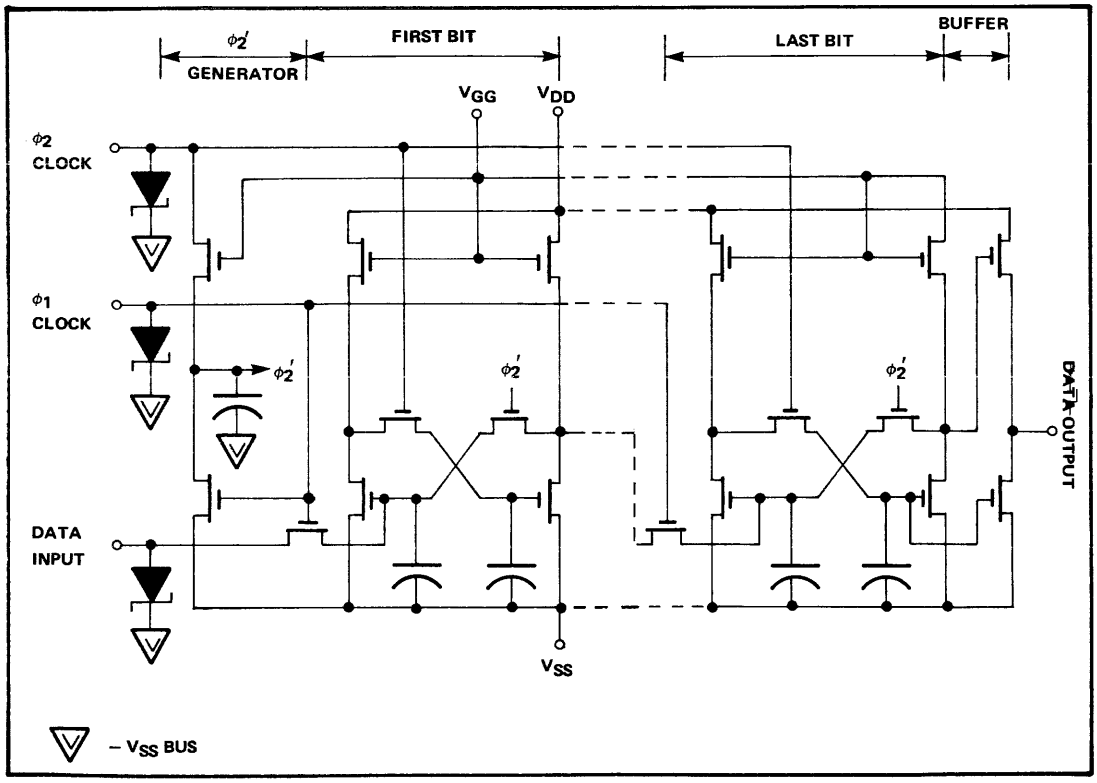


14

expansion to single 50- or 64-bit register



schematic (each register)



14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS
LSI

TMS 3002 LR-DUAL 50-BIT SHIFT REGISTER
TMS 3003 LR-DUAL 100-BIT SHIFT REGISTER

JANUARY, 1971

features

- Static logic
- DC to 1 MHz operation
- Low power dissipation
- Push-pull output buffers
- TTL compatible

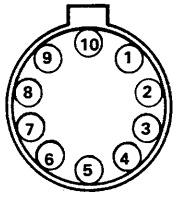
description

The TMS 3002 LR and TMS 3003 LR are dual static shift registers. Each device contains two dc-to-1-MHz shift registers with independent input and output terminals and common clocks and power. MOS thick-oxide technology is used to fabricate cross-coupled flip-flops for each register bit so that data can be stored indefinitely. The transistors in the device are the P-channel enhancement-mode type. All input leads have zener network protection and all outputs contain low-output-impedance non-inverting push-pull output buffers.

Two power-supply levels and two clocks are required for operation, with a third clock generated internally. Data is transferred into the register when the ϕ_1 clock is pulsed to logic 1. Data is shifted when the ϕ_1 clock is returned to logic 0 and the ϕ_2 clock is pulsed to logic 1. Output data appears on the logic 0 to logic 1 transition of the ϕ_2 clock. For long-term storage, the ϕ_1 clock must be held at logic 0 and the ϕ_2 clock at logic 1.

mechanical data and pin configuration

The TMS 3002 LR and TMS 3003 LR are mounted in TO-100 packages. (See MOS/LSI packaging section.)



BOTTOM VIEW

LEAD NO.	FUNCTION	LEAD NO.	FUNCTION
1	Input 1	6	Clock ϕ_2
2	Output 1	7	V_{GG}
3	V_{DD}	8	Output 2
4	Clock ϕ_1	9	Input 2
5	GND (V_{SS})	10	No connection

logic definition

Negative logic is assumed.

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} (See Note 1)	−30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−30 V to 0.3 V
Phase one clock input voltage $V_{\phi 1}$ range (See Note 1)	−30 V to 0.3 V
Phase two clock input voltage $V_{\phi 2}$ range (See Note 1)	−30 V to 0.3 V
Data input voltage V_I range (See Note 1)	−30 V to 0.3 V
Power dissipation	450 mW
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal, V_{SS}.

14

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−12	−14	−15	V
Supply voltage V_{GG}	−24	−28	−29	V
Logic 0 data input voltage $V_{i(0)}$ (See Note 2)	0.3	0	−2	V
Logic 1 data input voltage $V_{i(1)}$ (See Note 2)	−9.5	−14	−29	V
Width of data pulse, $t_{p(data)}$ (See voltage waveforms)	0.4†			μs
Data setup time, t_{setup} (See voltage waveforms and Note 3)	100			ns
Data hold time, t_{hold} (See voltage waveforms and Note 4)	20			ns
Logic 0 clock input voltage $V_{\phi 0(clock)}$ (See Note 2 and 5)	0.3	0	−2	V
Logic 1 clock input voltage $V_{\phi 1(clock)}$ (See Note 2 and 5)	−24	−28	−29	V
Rise time of clock pulse, $t_{r(clock)}$ (See voltage waveforms)		0	5	μs
Fall time of clock pulse, $t_{f(clock)}$ (See voltage waveforms)			5	μs
ϕ_1 clock pulse width, $t_{p(\phi 1)}$ (See voltage waveforms)	0.3†		10†	μs
ϕ_2 clock pulse width, $t_{p(\phi 2)}$ (See voltage waveforms)	0.4†		∞†	μs
Time interval from ϕ_1 clock to ϕ_2 clock input pulse, $t_{\phi 12}$ (See waveforms and Note 5)	0.01		10	μs
Time interval from ϕ_2 clock to ϕ_1 clock input pulse, $t_{\phi 21}$ (See waveforms and Note 5)	0.01		10	μs
Clock repetition rate	0		1	MHz

NOTES: 2. These voltage values are with respect to network ground terminal, V_{SS}.
3. Setup time is the interval immediately preceeding the positive-going edge of the phase 1 clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the positive-going edge of the phase 1 clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
5. The two clock pulses must never be simultaneously more than 3 volts more negative than V_{SS}.

† These values are at $V_{DD} = -14$ V, $V_{GG} = -28$ V, and $T_A = 25°C$.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNITS
I_{IL} Logic 1 input current into data input	$V_I = -20$ V, $T° = 25°C$			0.5	μA
$I_{IL(\phi)}$ Logic 1 input current into either clock input	$V_I = -28$ V, $V_{GG} = 0$ V, $T° = 25°C$			50	μA
V_{OH} Logic 0 output voltage	$I_O = 0$ mA, $C_L = 20$ pF		0.3	−1	V
	$I_O = 2$ mA, $C_L = 20$ pF		−2.6	−5	V
	$I_O = 0$ mA, $V_{dd} = -12$ V, $V_{gg} = -24$ V		−0.5	−1	
V_{OL} Logic 1 output voltage	$I_O = 0$ mA, $C_L = 20$ pF	−12.0	−13.5	−14	V
	$I_O = 0.5$ mA	−10.5	−12.5	−14	V
	$I_O = 0$ mA, $V_{dd} = -12$ V, $V_{gg} = -24$ V, $V_\phi, V_{\phi L} = -24$ V, $C_L = 20$ pF, $V_{in(1)} = -8.5$ V, $V_{in(0)} = -2$ V	−8.8	−10.5	−12	V
R_{OH} Output resistance, logic 0	$I_O = -2.0$ mA		1.5	2.5	kΩ
R_{OL} Output resistance, logic 1	$I_O = 0.5$ mA		1.5	7	kΩ
I_{DD} Supply current from V_{DD} terminal§	TMS 3002 LR, $T° = 25°C$		−8.5	−15	mA
	TMS 3003 LR, $T° = 25°C$		−16	−26	mA
I_{GG} Supply current from V_{GG} terminal§	TMS 3002 LR, $T° = 25°C$		−2	−3	mA
	TMS 3003 LR, $T° = 25°C$		−2	−3	mA
f_{max} Maximum clock frequency		1			MHz

† Unless otherwise noted, voltages are as shown in the nominal column of the recommended operating conditions (nominal operating voltages).
‡ All typical values are at $T_A = 25°C$.
§ Current into a terminal is a positive value.

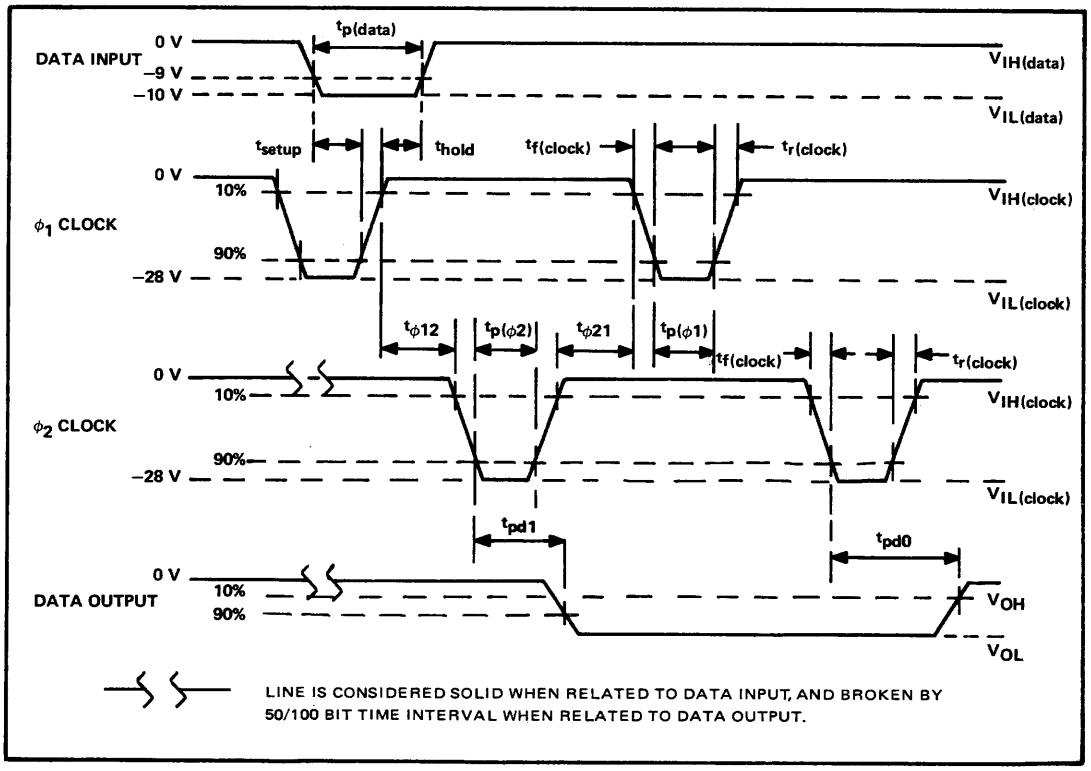
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics, $V_{DD} = -14$ V, $V_{GG} = -28$ V, $R_L = 10$ mΩ, $C_L = 20$ pF, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation delay time to high level from ϕ_2 clock to data output	See voltage waveforms			250	400	ns
t_{pd1}	Propagation delay time to low level from ϕ_2 clock	See voltage waveforms			250	350	ns
$C_{in(\phi1)}$	Capacitance of ϕ_1 clock input	$V_I = 0$ V, $V_{I(\phi2)} = 0$ V, f = 1 MHz	TMS 3002 LR		18	23	pF
			TMS 3003 LR		28	33	pF
$C_{in(\phi2)}$	Capacitance of ϕ_2 clock input*	$V_I = 0$ V, $V_{I(\phi1)} = 0$ V, f = 1 MHz	TMS 3002 LR		30	35	pF
			TMS 3003 LR		53	60	pF
C_{in}	Capacitance of data input	$V_I = 0$,	f = 1 MHz		5	7	pF

*$C_{in(\phi2)}$ includes the capacitance of the internal ϕ_2' clock.

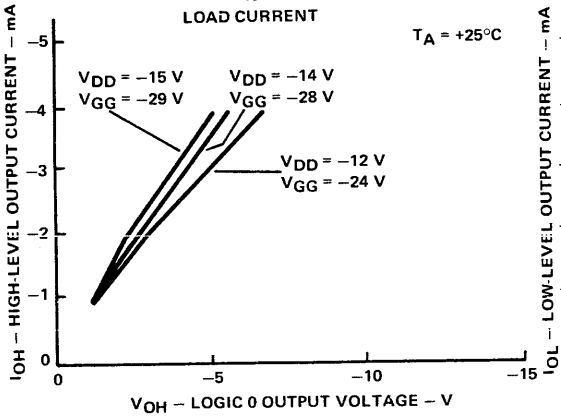
voltage waveforms



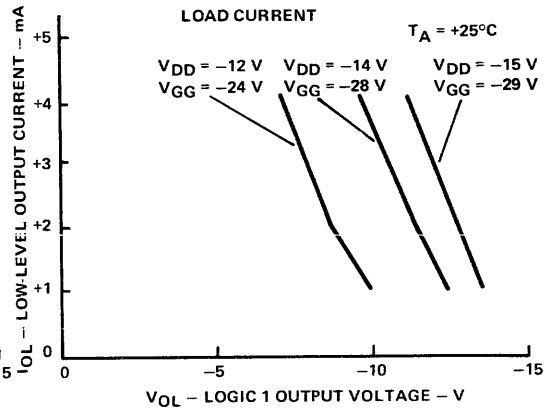
14

typical characteristics

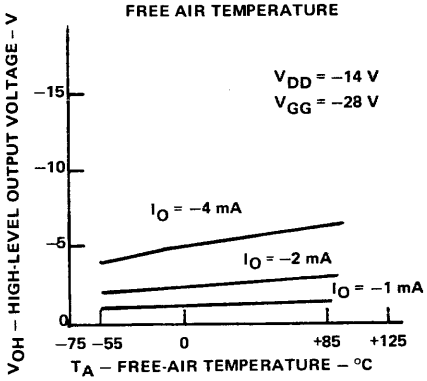
LOGIC 0 OUTPUT VOLTAGE
vs
LOAD CURRENT



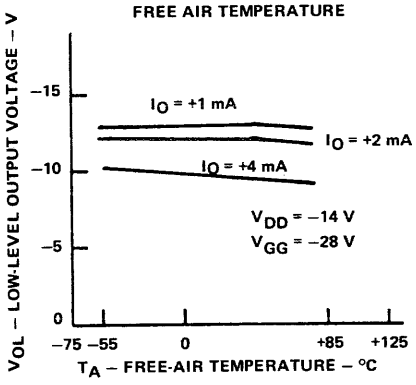
LOGIC 1 OUTPUT VOLTAGE
vs
LOAD CURRENT



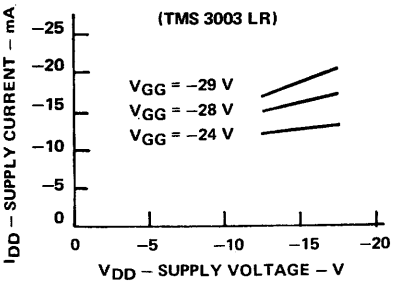
LOGIC 0 OUTPUT VOLTAGE
vs
FREE AIR TEMPERATURE



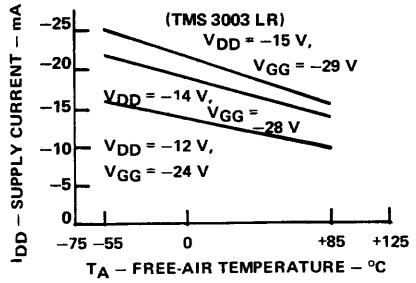
LOGIC 1 OUTPUT VOLTAGE
vs
FREE AIR TEMPERATURE



SUPPLY CURRENT
FROM V_{DD} SUPPLY
vs
DRAIN POWER SUPPLY VOLTAGE
(TMS 3003 LR)



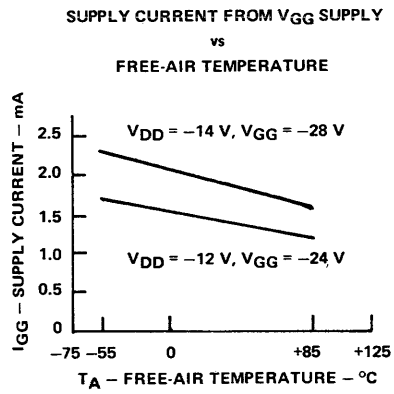
SUPPLY CURRENT
FROM V_{DD} SUPPLY
vs
FREE-AIR TEMPERATURE

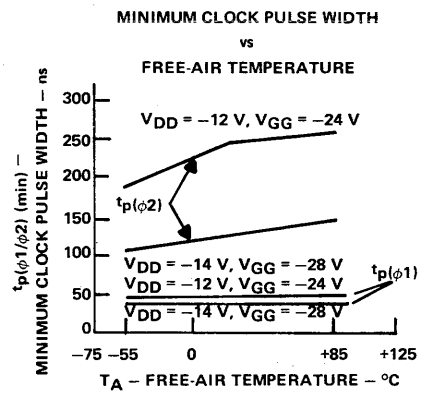


14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

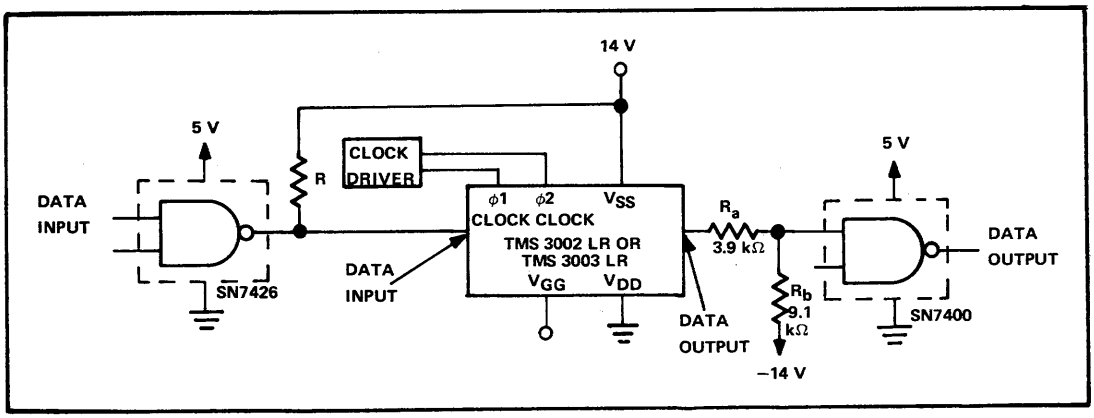
typical characteristics (continued)





typical application data

With proper supply voltages, interfacing can be achieved with only three resistors. A typical MOS/TTL interface is shown below.



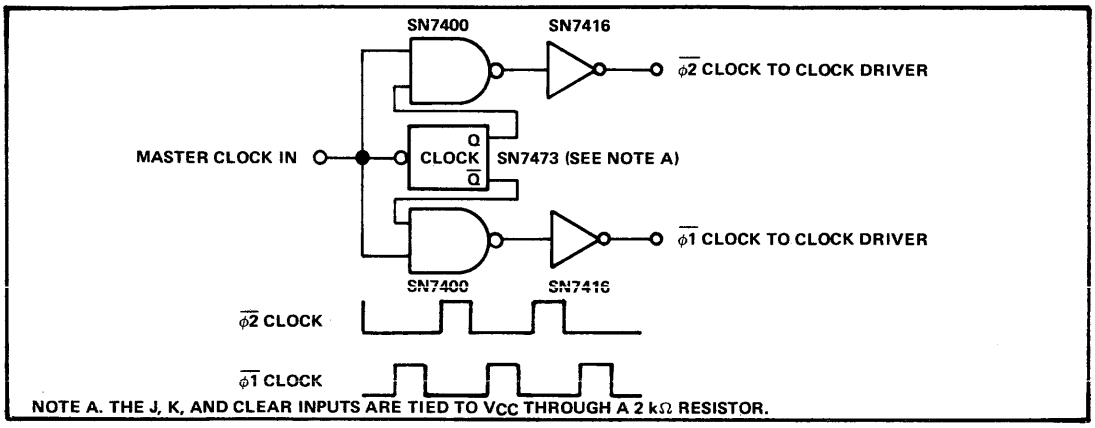
An input pull-up resistor is required to provide the necessary input voltage swing. The value of this resistor (R) depends on the actual circuit requirements – values as low as 1 kΩ can be used for high-speed operation while values as high as 15 kΩ can be used when low power consumption is important rather than high-speed.

At the output interface, the 9.1-kΩ resistor sinks the 1.6 mA of TTL-gate current when 0 volts is required on the TTL input. When 3 volts is required on the TTL input, the MOS output device supplies current from 14 volts, through the 3.9-kΩ resistor and the 9.1-kΩ resistor to –14 volts. The 3.9-kΩ resistor limits the voltage at the TTL gate input to 5 volts maximum.

14

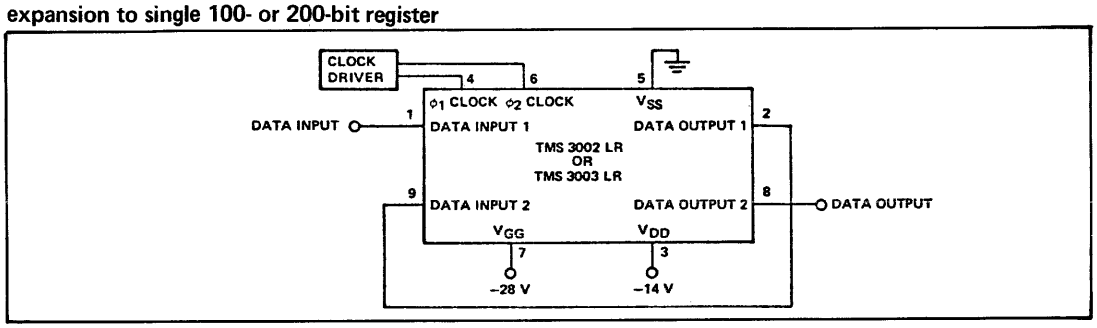
TMS 3002 LR-DUAL 50-BIT SHIFT REGISTER
TMS 3003 LR-DUAL 100-BIT SHIFT REGISTER

two-phase clock generator

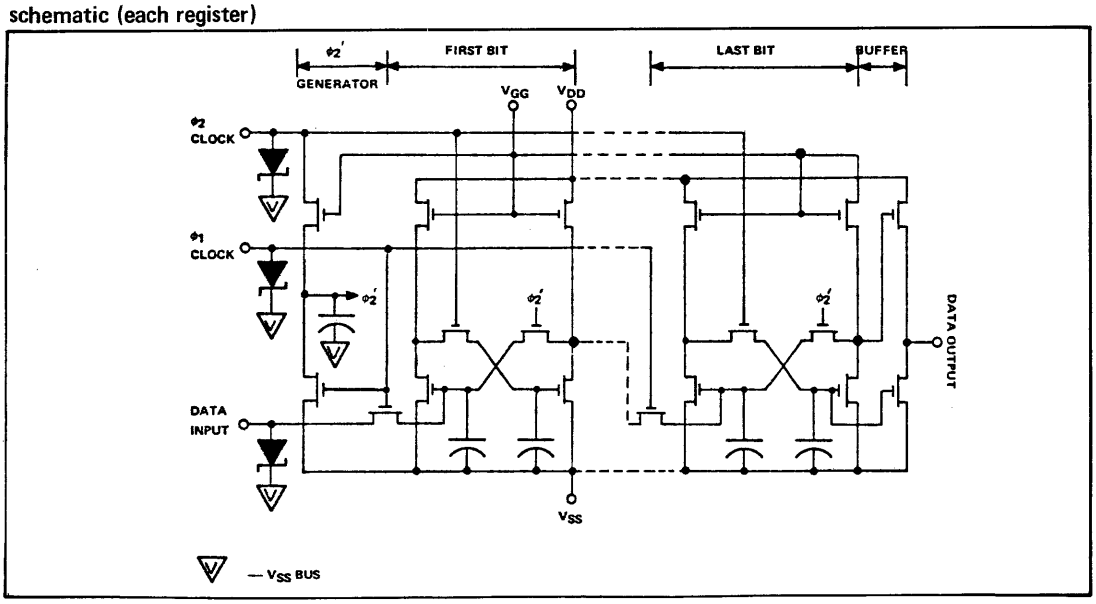


NOTE A. THE J, K, AND CLEAR INPUTS ARE TIED TO V_{CC} THROUGH A 2 kΩ RESISTOR.

expansion to single 100- or 200-bit register



schematic (each register)



14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS
LSI

TMS 3012 JC, NC - DUAL 128-BIT ACCUMULATOR
TMS 3028 LC - DUAL 128-BIT SHIFT REGISTER

FEBRUARY, 1971

features

- 256 bits of storage
- Single clock phase
- Static logic
- TTL compatible
- DC to 1 MHz operation
- Push-pull output buffers
- 16-pin dual-in-line package (TMS 3012 JC/NC)
- Recirculating control logic (TMS 3012 JC/NC)

description

The TMS 3012 JC/NC consists of two separate 128-bit static shift registers with independent input and output terminals and logic, within the circuit, for loading and recirculating information. Two power supplies and one external clock are required for operation. Three clocks are generated internally. Cross-coupled flip-flops are used to implement each bit of delay and enable data to be stored indefinitely between two clock pulses. The entire device is constructed on a single monolithic chip using thick-oxide techniques and MOS P-channel enhancement-mode transistors. A unit mounted in a 16-pin hermetically sealed ceramic dual-in-line package is designated "JC". "NC" is the designation for a unit mounted in a 16-pin plastic package.

The TMS 3028 LC is identical to the TMS 3012 JC/NC except for the fact that recirculate logic is not included on the chip and that the device is mounted in a TO-100 package instead of a dual-in-line package.

operation

Transferring data into the register and shifting the data in the register are accomplished when the ϕ_{IN} clock is at a logic 1; for long-term data storage, the ϕ_{IN} clock must be held at logic 0. Output appears on the positive-going edge of the ϕ_{IN} clock pulse.

logic definition

Negative logic is assumed.

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

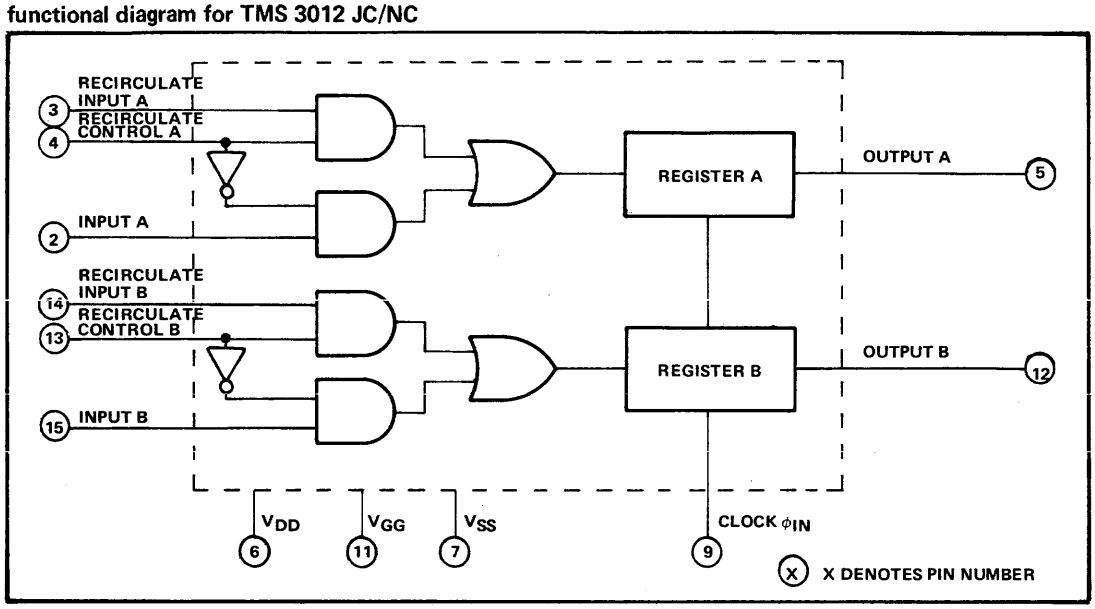
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range*	−30 V to 0.3 V
Supply voltage V_{GG} range*	−30 V to 0.3 V
Clock and data input voltage ranges*	−30 V to 0.5 V
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

* These voltage values are with respect to substrate terminal.

14

functional diagram for TMS 3012 JC/NC



recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−13	−14	−15	V
Supply voltage V_{GG}	−27	−28	−29	V
Width of data pulse, $t_{(data)}$ (See voltage waveforms)	0.4		10	μs
Width of clock pulses: t_p(Logic 1) See voltage waveforms	0.4		5	μs
t_p(Logic 0) See voltage waveforms	0.4		∞	μs
Rise time of clock pulse, $t_{r(clock)}$ (See voltage waveforms)			5	μs
Fall time of clock pulse, $t_{f(clock)}$ (See voltage waveforms)			1	μs
Clock repetition rate	0		1	MHz
$V_{in(1)}$* Data/Recirculate Control Logic 1 voltage	−9	−14	−15	V
$V_{in(0)}$* Data/Recirculate Control Logic 0 voltage	0	0	−2	V
$V_{in(1)\phi}$* Logic 1 clock input voltage	−9	−14	−15	V
$V_{in(0)\phi}$* Logic 0 clock input voltage	0	0	−2	V
Data change time before clock change to 0 (t_{db})	0.2			μs
Data change time after clock change to 0 (t_{da})	0.2			μs
Recirculate control change time before clock change to 0 (t_{rb}) (See Note 2)	0.3			μs
Recirculate control change time after clock change to 0 (t_{ra}) (See Note 2)	0.3			μs

NOTES: 1. All voltages are with respect to V_{SS}.
2. TMS 3012 JR only.

* To ensure correct data loading, the input should reach the desired level at least time t_{db} before the clock goes to logic 0, and should remain at that level for a time t_{da} after the clock has changed to 0. Similarly, the recirculate control input should not change state for a period t_{rb} before and t_{ra} after the clock change from logic 1 to logic 0.

14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics at nominal operating conditions and 25°C

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNITS
$V_{out(1)}$	Logic 1 output voltage	R_L = 10 kΩ to V_{SS}	−11	−13		V
$V_{out(0)}$	Logic 0 output voltage	R_L = 10 kΩ to V_{SS}		−0.3	−1	V
$I_{in(1)}$	Data input, leakage current	V_{in} = −20 V			−0.5	μA
$I_{in(1)\phi}$	Clock input, leakage current	$V_{in\phi}$ = −20 V, V_{GG} = 0			0.5	μA
Z_{out}	Output impedance to ground	V_{out} = 0 to −1 V		0.7	1.5	kΩ
I_{DD}	Supply current into V_{DD} terminal	V_{DD} = −15 V, V_{GG} = −29 V		−23	−30	mA
I_{GG}	Supply current into V_{GG} terminal	V_{DD} = −15 V, V_{GG} = −29 V		−3	−5.5	mA

† Unless otherwise noted, R_L = 10 kΩ, and C_L = 10 pF.

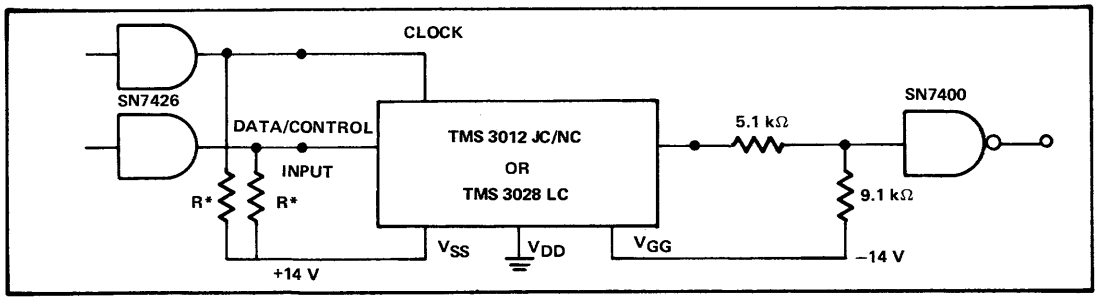
‡ All other pins are at V_{SS}

dynamic electrical characteristics, V_{DD} = −14 V, V_{GG} = −28 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Propagation delay time to logic 1 level from clock ϕ to data output	R_L = 10 kΩ to ground, C_L = 10 pF		500	700	ns
t_{pd0}	Propgation delay time to logic 0 level from clock ϕ to data output	R_L = 10 kΩ to ground, C_L = 10 pF		400	600	ns
C_{in}	Capacitance of data input	V_{in} = 0, f = 1 MHz, T_A = 25°C		3	5	pF
$C_{in\phi}$	Capacitance of clock input	$V_{in\phi}$ = 0, f = 1 MHz, T_A = 25°C		5	7	pF

interface circuits

a) TTL/DTL



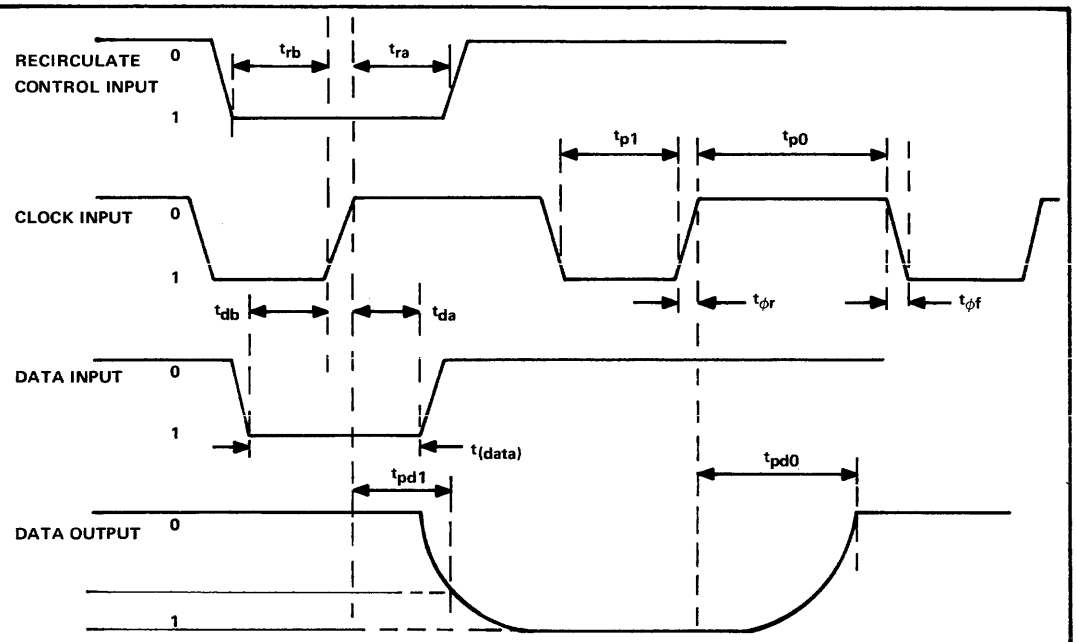
* Select R for speed and power requirements.

b) MOS

No external components are required.

14

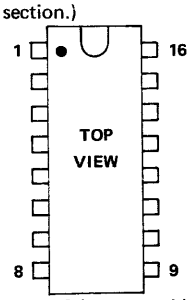
voltage waveforms (TMS 3012 JC/NC only)



TIMES ARE MEASURED AT 10% AND 90% VALUES OF THE WORST CASE LOGIC 1 AND LOGIC 0 LEVELS.

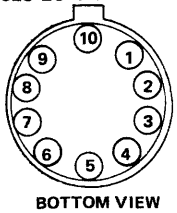
mechanical data

The TMS 3012 is available in both a 16-pin hermetically sealed ceramic dual-in-line package (JC) and a 16-pin plastic package (NC). The packages are designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	No connection	9	Clock ϕ
2	Input A	10	No connection
3	Recirculate Input A	11	V_{GG}
4	Recirculate Control A	12	Output B
5	Output A	13	Recirculate Control B
6	V_{DD}	14	Recirculate Input B
7	V_{SS}	15	Input B
8	No connection	16	No connection

The TMS 3028 LC is mounted in a TO-100 package. (See MOS/LSI packaging section.)



BOTTOM VIEW

LEAD NO.	FUNCTION	LEAD NO.	FUNCTION
1	Input 1	6	V_{SS}
2	Output 1	7	V_{GG}
3	V_{DD}	8	Output 2
4	Clock ϕ_1	9	Input 2
5	V_{SS}	10	No connection

14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 3016 LR
DUAL 16-BIT STATIC SHIFT REGISTER

JANUARY 1971

features

- Static logic
- DC to 1 MHz operation
- Low power dissipation
- Push-pull output buffers
- TTL compatible

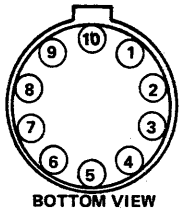
description

The TMS 3016 LR is a dual static shift register. This device contains two dc-to-1-MHz shift registers with independent input and output terminals and common clocks and power. MOS thick-oxide technology is used to fabricate cross-coupled flip-flops for each register bit so that data can be stored indefinitely. The transistors in the device are the P-channel enhancement-mode type. All input leads have zener network protection and all outputs contain low output impedance, non-inverting push-pull output buffers.

Two power supply levels and two clocks are required for operation with a third clock generated internally. Data is transferred into the register when the ϕ_1 clock is pulsed to logic 1. Data is shifted when the ϕ_1 clock is returned to logic 0 and the ϕ_2 clock is pulsed to logic 1. Output data appears on the logic 0 to logic 1 transition of the ϕ_2 clock. For long term storage, the ϕ_1 clock must be held at a logic 0 and the ϕ_2 clock at a logic 1.

mechanical data and pin configuration

The TMS 3016 LR is mounted in a TO-100 package. (See MOS/LSI packaging section.)



BOTTOM VIEW

LEAD NO.	FUNCTION	LEAD NO.	FUNCTION
1	No connection	6	V_{GG}
2	Clock ϕ_2	7	Output 2
3	Input 1	8	Clock ϕ_1
4	Input 2	9	Output 1
5	GND (V_{SS})	10	V_{DD}

logic definition

Negative logic is assumed

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−30 V to 0.3 V
Phase one clock input voltage $V_{\phi 1}$ range (See Note 1)	−30 V to 0.3 V
Phase two clock input voltage $V_{\phi 2}$ range (See Note 1)	−30 V to 0.3 V
Data input voltage V_I range (See Note 1)	−30 V to 0.3 V
Power dissipation	450 mW
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal, V_{SS}.

14

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−12	−14	−15	V
Supply voltage V_{GG}	−24	−28	−29	V
Logic 0 data input voltage $V_{i(0)}$ (See Note 2)	0.3	0	−2	V
Logic 1 data input voltage $V_{i(1)}$ (See Notes 2)	−9.5	−14	−29	V
Width of data pulse, $t_{p(data)}$ (See voltage waveforms)	0.4†			μs
Data setup time, t_{setup} (See voltage waveforms and Note 3)	100			ns
Data hold time, t_{hold} (See voltage waveforms and Note 4)	20			ns
Logic 0 clock input voltage $V_{\phi 0(clock)}$ (See Notes 2 and 5)	0.3	0	−2	V
Logic 1 clock input voltage $V_{\phi 1(clock)}$ (See Notes 2 and 5)	−24	−28	−29	V
Rise time of clock pulse, $t_{r(clock)}$ (See voltage waveforms)		0	5	μs
Fall time of clock pulse, $t_{f(clock)}$ (See voltage waveforms)			5	μs
ϕ_1 clock pulse width, $t_{p(\phi 1)}$ (See voltage waveforms)	0.3†		10†	μs
ϕ_2 clock pulse width, $t_{p(\phi 2)}$ (See voltage waveforms)	0.4†		∞†	μs
Time interval from ϕ_1 clock to ϕ_2 clock input pulse, $t_{\phi 12}$ (See voltage waveforms)	0.01		10	μs
Time interval from ϕ_2 clock to ϕ_1 clock input pulse, $t_{\phi 21}$ (See voltage waveforms)	0.01		10	μs
Clock repetition rate	0		1	MHz

NOTES: 2. These voltage values are with respect to network ground terminal, V_{SS}.
3. Setup time is the interval immediately preceeding the positive-going edge of the phase 1 clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the positive-going edge of the phase 1 clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
5. The two clock pulses must never be simultaneously more than 3 volts more negative than V_{SS}.

† These values are at $V_{DD} = -14$ V, $V_{GG} = -28$ V, and $T_A = 25°C$.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNITS
I_{IL}	Logic 1 input current into data input	$V_I = -20$ V,	$T° = 25°C$			0.5	μA
$I_{IL(\phi)}$	Logic 1 input current into either clock input	$V_I = -28$ V, $T° = 25°C$	$V_{GG} = 0$ V,			50	μA
V_{OH}	Logic 0 output voltage	$I_O = 0$ mA,	$C_L = 20$ pF		0.3	−1	V
		$I_O = 2$ mA,	$C_L = 20$ pF		−2.6	−5	V
		$I_O = 0$ mA, $V_{GG} = -24$ V	$V_{DD} = -12$ V,		−0.5	−1	V
V_{OL}	Logic 1 output voltage	$I_O = 0$ mA,	$C_L = 20$ pF	−12.0	−13.5	−14	V
		$I_O = 0.5$ mA		−10.5	−12.5	−14	V
		$I_O = 0$ mA, $V_{GG} = -24$ V, $C_L = 20$ pF, $V_{in(0)} = -2$ V	$V_{DD} = -12$ V, $V_\phi, V_{\phi 2} = -24$ V $V_{in(1)} = -8.5$ V	−8.8	−10.5	−12	V
R_{OH}	Output resistance, logic 0	$I_O = -2.0$ mA			1.5	2.5	kΩ
R_{OL}	Output resistance, logic 1	$I_O = 0.5$ mA			1.5	7	kΩ
I_{DD}	Supply current from V_{DD} terminal*				−8	−12	mA
I_{GG}	Supply current from V_{GG} terminal*				−1.6	−2.5	mA
f_{max}	Maximum clock frequency			1			MHz

† Unless otherwise noted, voltages are as shown in the nominal column of the recommended operating conditions (nominal operating voltages).
‡ All typical values are at $T_A = 25°C$. * Current into a terminal is a positive value.

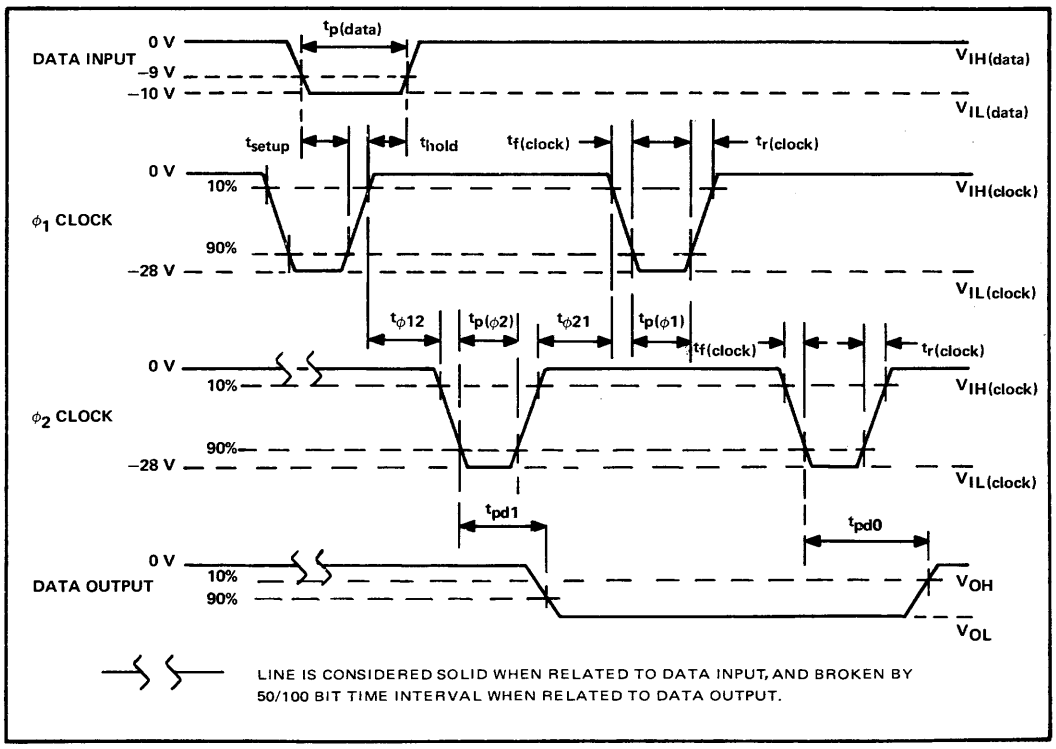
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics, $V_{DD} = -14$ V, $V_{GG} = -28$ V, $R_L = 10$ mΩ, $C_L = 20$ pF, $T_A = 25°C$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation delay time to high level from ϕ_2 clock to data output	See voltage waveforms		250	400	ns
t_{pd1}	Propagation delay time to low level from ϕ_2 clock to data output	See voltage waveforms		250	350	ns
$C_{in(\phi1)}$	Capacitance of ϕ_1 clock input	$V_I = 0$ V, $V_{I(\phi2)} = 0$ V, f = 1 MHz		6	10	pF
$C_{in(\phi2)}$	Capacitance of ϕ_2 clock input*	$V_I = 0$ V, $V_{I(\phi1)} = 0$ V, f = 1 MHz		15	20	pF
C_{in}	Capacitance of data input	$V_I = 0$, f = 1 MHz		2	14	pF

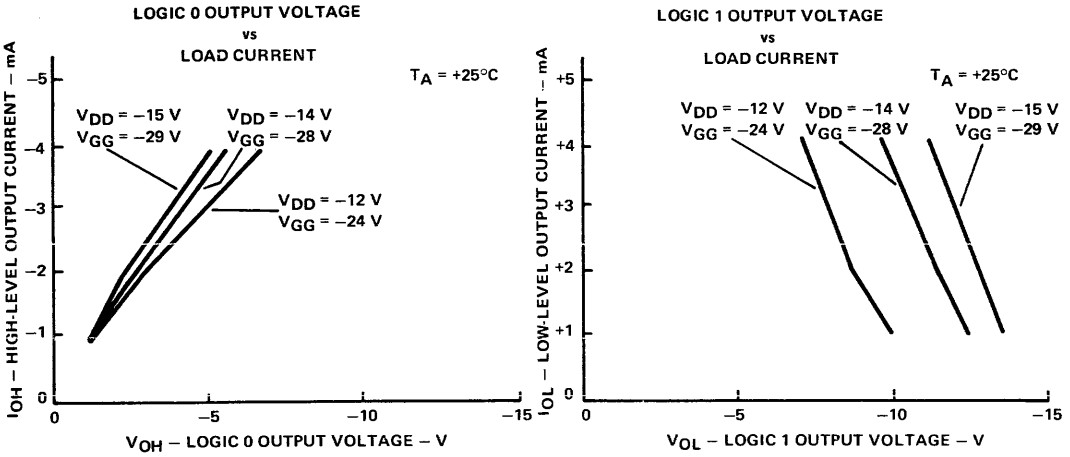
*$C_{in(\phi2)}$ includes the capacitance of the internal ϕ_2 clock.

voltage waveforms



14

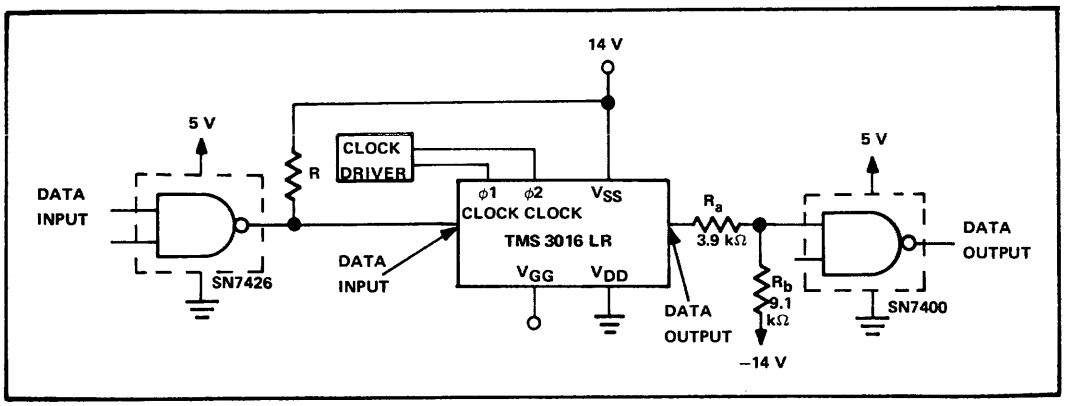
typical characteristics



typical applications data

1) MOS/TTL interface

With proper supply voltages, interfacing can be achieved with only three resistors. A typical MOS/TTL interface is shown below.



An input pull-up resistor is required to provide the necessary input voltage swing. The value of this resistor (R) depends on the actual circuit requirements – values as low as 1 kΩ can be used for high-speed operation while values as high as 15 kΩ can be used when low power consumption is important rather than high-speed.

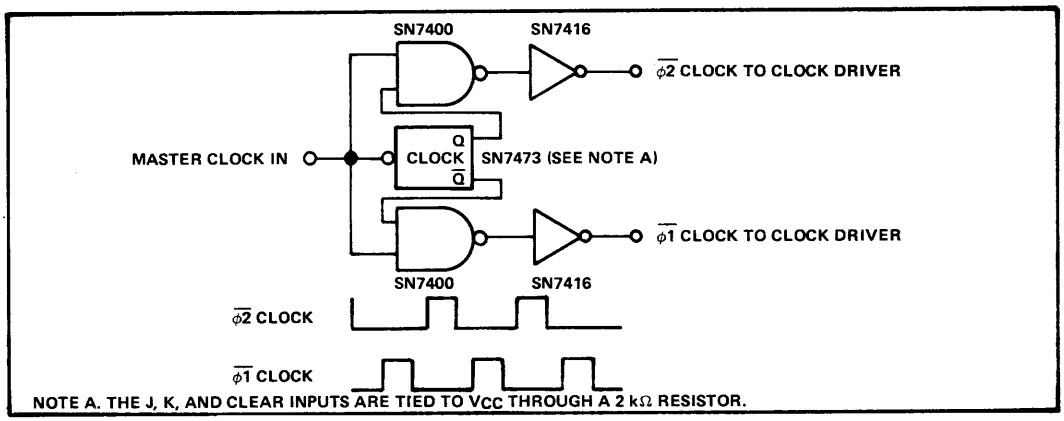
14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

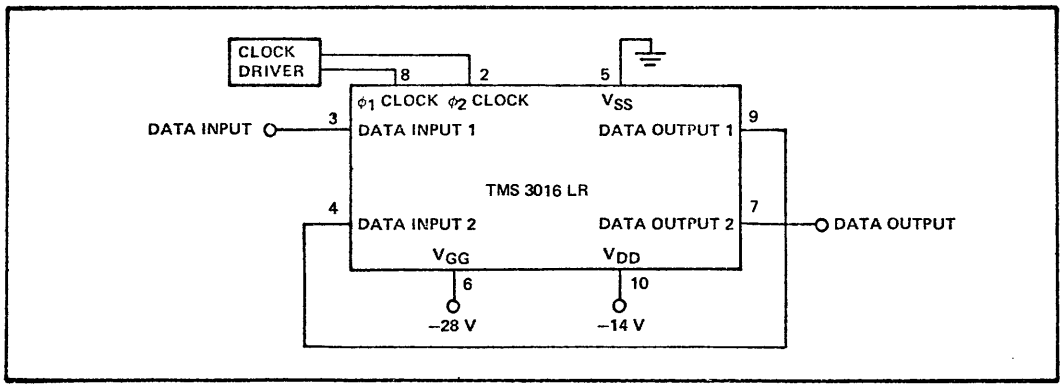
typical applications data (continued)

At the output interface, the 9.1-kΩ resistor sinks the 1.6 mA of TTL-gate current when 0 volts is required on the TTL input. When 3 volts is required on the TTL input, the MOS output device supplies current from 14 volts, through the 3.9 kΩ resistor and the 9.1-kΩ resistor to −14 volts. The 3.9-kΩ resistor limits the voltage at the TTL gate input to 5 volts maximum.

2) Two-phase clock generator

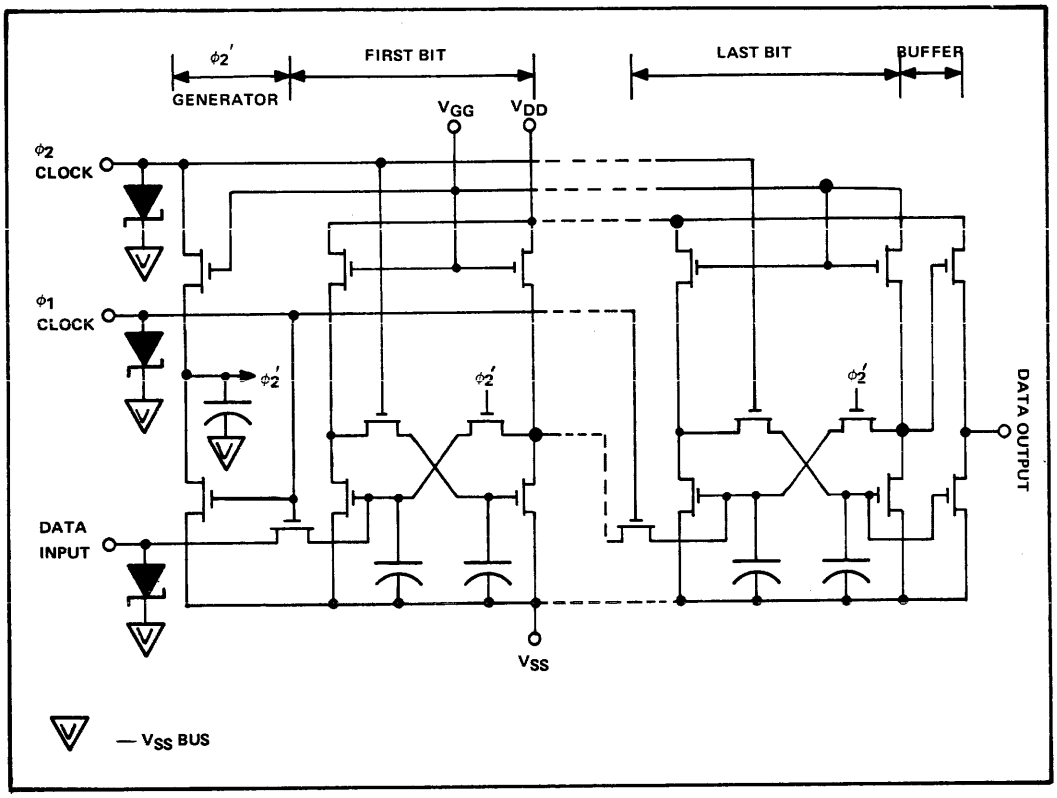


expansion to single 32 register



14

schematic (each register)



14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS
LSI

TMS 3101 LC, NC - DUAL 100-BIT STATIC SHIFT REGISTER
TMS 3102 LC, NC - DUAL 80-BIT STATIC SHIFT REGISTER
TMS 3103 LC, NC - DUAL 64-BIT STATIC SHIFT REGISTER

JANUARY, 1971

features

- DC to 2.5-MHz operation
- Low power dissipation
- Direct interface with DTL/TTL
- Static operation
- Push-pull output buffer
- Low-threshold technology

description

The TMS 3101 LC/NC is a dual 100-bit static shift register; the TMS 3102 LC/NC is a dual 80-bit static shift register; and the TMS 3103 LC/NC is a dual 64-bit static shift register. These circuits are constructed on a single monolithic chip using thick-oxide techniques and P-channel enhancement-mode transistors. Each register has independent input and output terminals, common clocks and power, and can operate from dc to 2.5 MHz. The inputs, which are zener protected, can be driven directly from DTL/TTL levels, and the register outputs can drive DTL/TTL circuits without the addition of external components.

The TMS 3100 series is a family of static shift registers, the lengths of which are programmable from 4 to 100 bits, through a single-mask-level change. The 100-, 80-, and 64-bit lengths are available from stock.

Units mounted in 10-lead TO-100 packages are designated "LC". Mounted in 16-pin dual-in-line plastic packages, the devices are designated "NC".

logic definition

Positive logic is assumed.

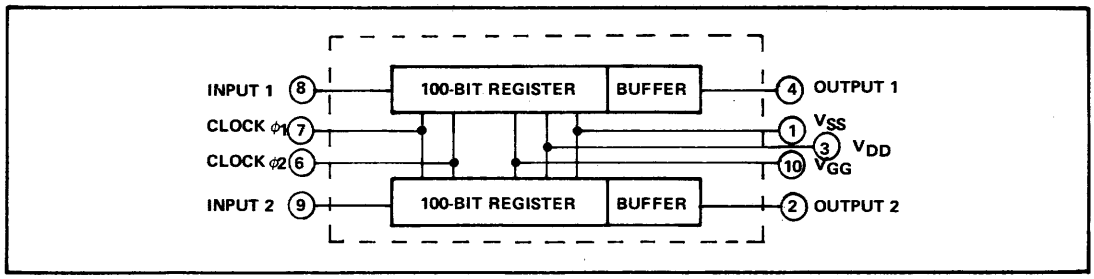
a) Logic 1 = most positive (HIGH) voltage

b) Logic 0 = most negative (LOW) voltage

operation

Cross-coupled flip-flops are used to implement each register bit and permit data to be stored indefinitely between clock pulses. Two external clock pulses are required for operation. Data is transferred into the register when the clock pulse $\phi 1$ is at a Low level. Data is shifted when clock pulse $\phi 1$ is returned to a High level and clock pulse $\phi 2$ is pulsed to a Low level. Output data appears on the High-to-Low transition of clock pulse $\phi 2$. For long-term storage, clock pulse $\phi 1$ must be held at a High level and clock pulse $\phi 2$ at a Low level.

functional block diagram and pin configuration



14

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −20 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −20 V to 0.3 V
Clock input voltage range (See Note 1) . . . . . −20 V to 0.3 V
Data input voltage range (See Note 1) . . . . . −20 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate supply V_{SS}	+4.75	+5	+5.25	V
Drain supply V_{DD}	0	0	0	V
Gate supply V_{GG}	−13	−12	−11	V
Logic Levels (Note 2)				
Input High level V_{IH}	+3.5		+5.25	V
Input Low level V_{IL}	−13	−12	0.8	V
Clock Voltage Levels				
Clock High level $V_{\phi H}$	+3		+5.25	V
Clock Low level $V_{\phi L}$	−13		−11	V
Pulse Timing				
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			3	μs
Clock pulse width 1 (See waveforms) $PW_{\phi 1}$	0.150		10	μs
Clock pulse width 2 $PW_{\phi 2}$	0.150		∞	μs
Pulse Spacing				
Clock delay $t_{D\phi 12}$			10	μs
Clock delay $t_{D\phi 21}$			10	μs
Data setup t_{DS}	150			ns
Data hold t_{DH}	10			ns
Pulse Overlap				
Clock (See Note 2)				
Pulse Repetition Rate PRR				
Data (See Note 2)	0		2.5	MHz
Clock (See Note 3)	0		2.5	MHz

NOTES: 2. Both clocks should not be simultaneously more than 2 V below V_{SS}.
3. C_L = 10 pF, one TTL load.

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input current	V_I = 0 V, V_{SS} = +5 V			500	μA
$I_{\phi L}$	Clock current	V_I = −12 V, V_{SS} = +5 V			20	μA
Output Voltage Levels						
V_{OL}	Output LOW level	(See Note 4) 1 TTL load			+0.4	V
V_{OH}	Output HIGH level	(See Note 4) 1 TTL load	+3.0	+3.5		V
V_{OL}	Output LOW level	(See Note 4) MOS load (3101)			+0.4	V
V_{OH}	Output HIGH level	(See Note 4) MOS load (3101)	3.6			V

NOTE 4: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and 20 pF. A worst-case MOS load is simulated by a load of 20 kΩ and 20 pF. All loads are connected between output and V_{SS}.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

static electrical characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Current						
I_{OSC}	Short circuit				30	mA
Power Supply Current Drain						
I_{SS}	Substrate supply	$V_{out} = V_{OH}$ (See Note 5)		16	20	mA
I_{DD}	Drain supply	See Note 6			0.5	mA
I_{GG}	Gate supply	$V_{out} = V_{OH}$ (See Note 5)		−16	−20	mA
P_D	Power dissipation			270	360	mW

NOTES: 5. The device uses saturated logic. The current sourced by the 5-V power supply is sunk by the −12-V power supply.

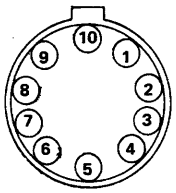
6. Does not include output stage load or transient current. In the MOS load mode, the current will consist of transients due to capacitor discharge and/or leakage current. In the TTL load mode the current is the current sunk by the TTL (up to 1.6 mA).

dynamic electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output Logic Delay							
t_{DLH_1}	Output LOW level	C_L = 10 pF,	TTL gate load		50	75	ns
t_{DHL_1}	Output HIGH level	C_L = 10 pF,	TTL gate load		100	125	ns
t_{DLH_2}	Output HIGH level	C_L = 10 pF,	MOS load		60	85	ns
t_{DHL_2}	Output LOW level	C_L = 10 pF,	MOS load		120	150	ns
Capacitance							
C_{IN}	Input	V_I = 0 V,	f = 1 MHz		9	12	pF
C_ϕ	Clock	V_I = 0 V,	f = 1 MHz		48	55	pF

mechanical data and pin configuration

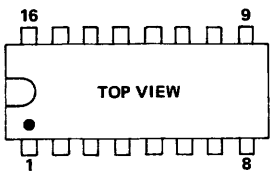
Units mounted in 10-lead TO-100 packages are designated "LC" (See MOS/LSI packaging section.)



BOTTOM VIEW

LEAD NO.	FUNCTION	LEAD NO.	FUNCTION
1	V_{SS}	6	Clock ϕ_2
2	Output 2	7	Clock ϕ_1
3	V_{DD}	8	Input 1
4	Output 1	9	Input 2
5	No connection	10	V_{GG}

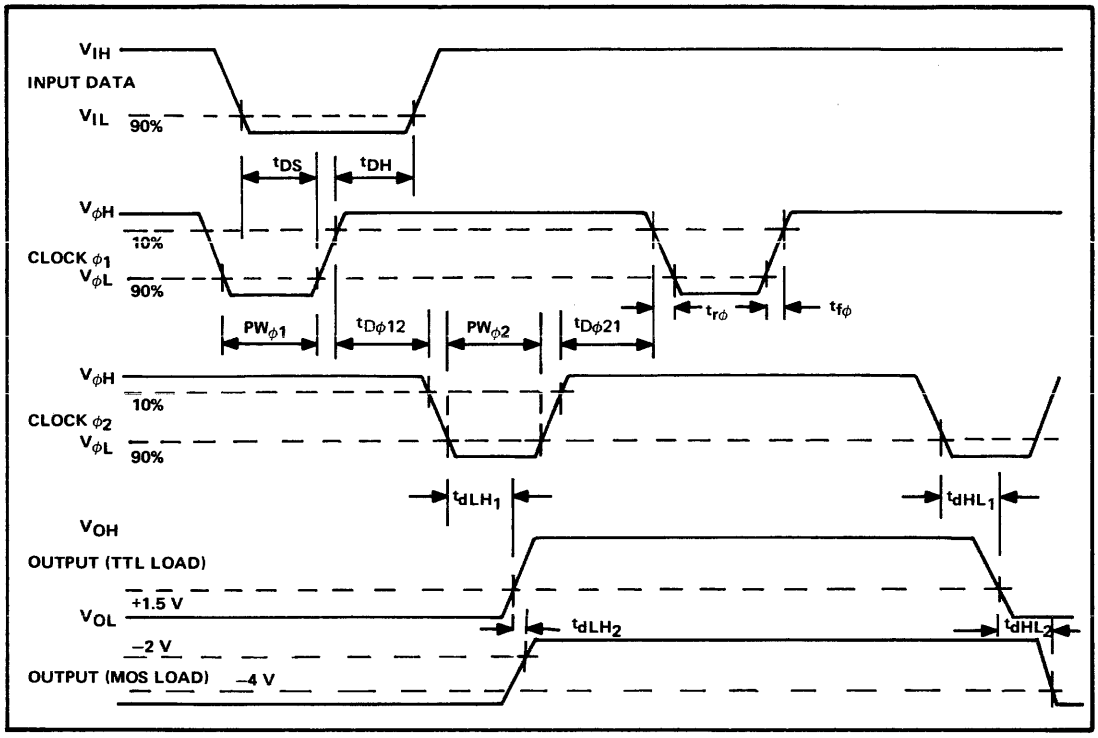
Mounted in 16-pin dual-in-line plastic packages, the devices are designated "NC" The package is designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)



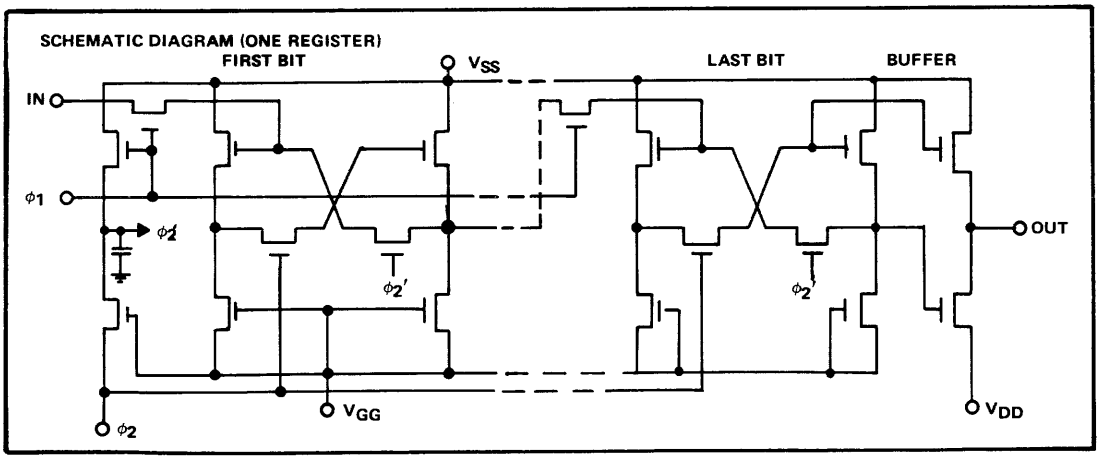
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	ϕ_2	9	V_{SS}
2	No connection	10	No connection
3	ϕ_1	11	No connection
4	Input 1	12	Output 2
5	Input 2	13	V_{DD}
6	No connection	14	Output 1
7	No connection	15	No connection
8	V_{GG}	16	No connection

14

timing diagram and voltage waveforms



circuit diagram

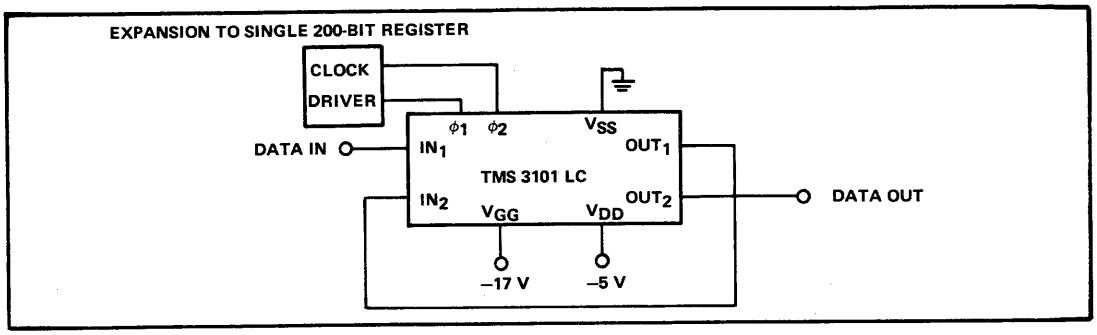


14

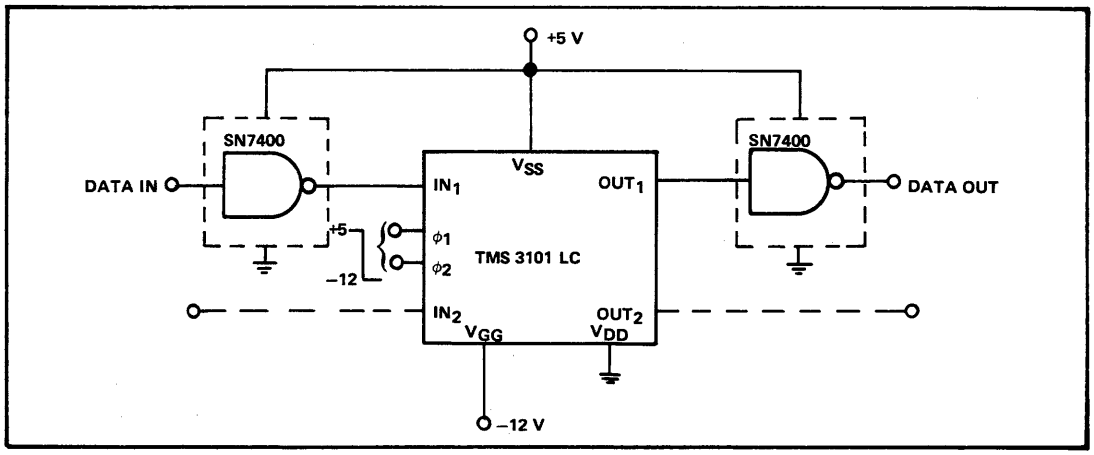
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

interface circuits

a) MOS



b) TTL



14

TMS 3112 JC, TMS 3112 NC
HEX 32-BIT STATIC SHIFT REGISTER

JANUARY, 1971

features

- Single clock (TTL levels)
- DTL/TTL compatible
- DC to 1 MHz
- Static operation
- Loading and recirculating control logic
- Gated-output control logic
- Dual-in-line package
- Single-ended (open drain) buffer
- Low-threshold technology

description

The TMS 3112 JC/NC contains six separate 32-bit static shift registers constructed on a single monolithic chip, using thick-oxide techniques and P-channel enhancement-mode low-threshold MOS transistors.

A single clock is required for operation. The clock and all inputs can be driven directly from DTL/TTL logic levels and each register output can drive DTL/TTL circuits. The device also contains common control logic for loading, recirculation, and output enable.

"TMS 3112 JC" is the part number for a unit mounted in a 24-pin hermetically sealed dual-in-line package. Mounted in a 24-pin plastic package the device is numbered "TMS 3112 NC".

logic definition

Positive logic is assumed.

a) Logic 1 = most positive (High) voltage

b) Logic 0 = most negative (Low) voltage

operation

Cross-coupled flip-flops are used to implement each register bit and permit data to be stored indefinitely between internal clock pulses. A single external clock pulse is required for operation. Data is transferred into the register when the clock pulse and recirculate control are at a Low level. Output data appears on the Low-to-High transition of the clock pulse. Data can be read out when the output gate control is held at a Low level. Recirculating data occurs when the recirculation control is at a High level.

The registers can drive DTL/TTL loads by using a 7.5-kΩ pull-down resistor connected between the output terminal and the V_{GG} supply.

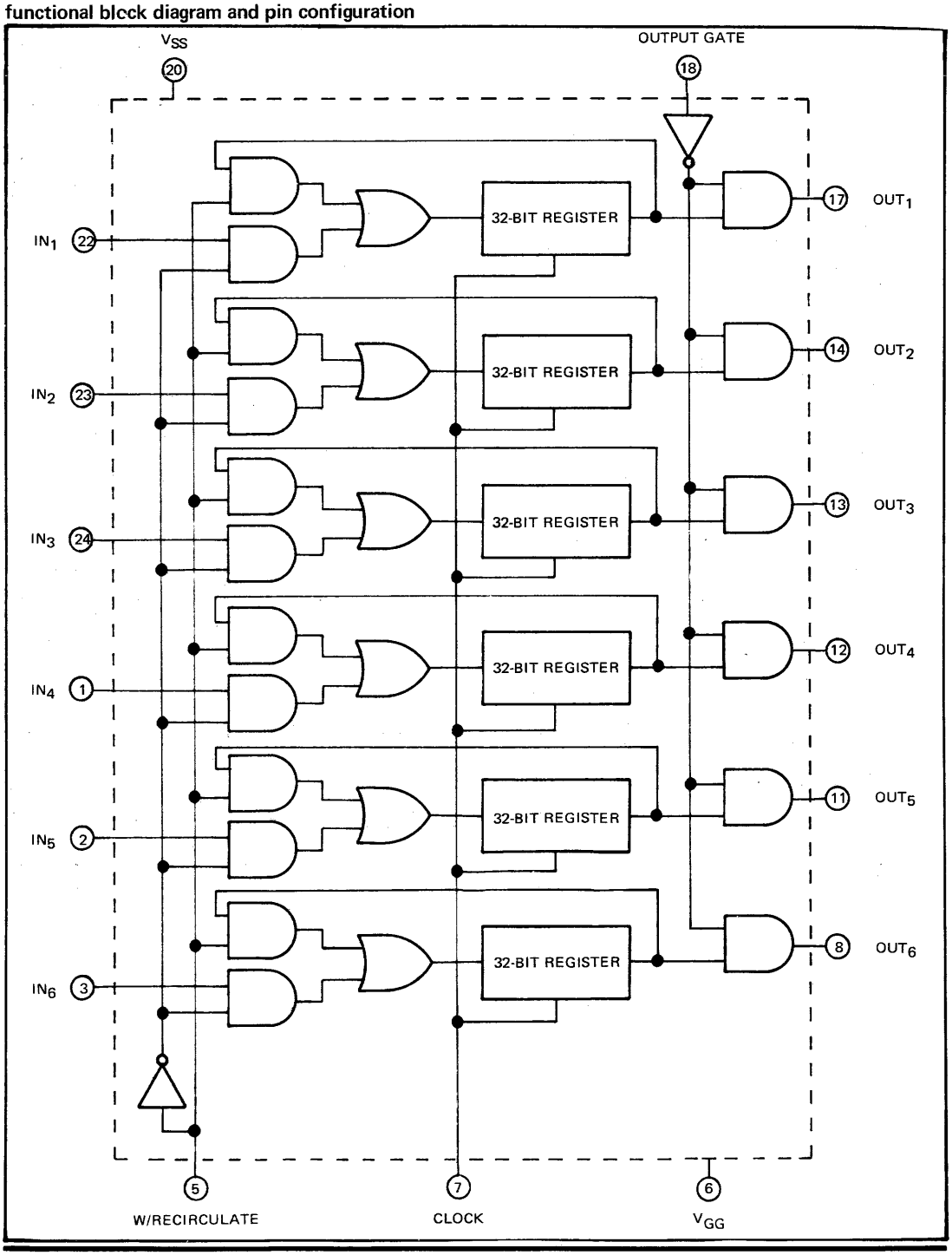
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{GG} range (See Note)	−20 V to 0.3 V
Clock input voltage range (See Note)	−20 V to 0.3 V
Data input voltage range (See Note)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE: These voltage values are with respect to V_{SS} (substrate).

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram and pin configuration



14

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Substrate supply V_{SS}	+4.75	+5	+5.25	V
Gate supply V_{GG}	−11	−12	−13	V
Input High level V_{IH}	+3.5			V
Input Low level V_{IL}			+0.6	V
Clock High level $V_{\phi H}$	+3.5			V
Clock Low level $V_{\phi L}$			+0.6	V
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			5000	ns
Clock High level $PW_{\phi H}$	600			ns
Clock Low level $PW_{\phi L}$	300			ns
Recirculate PW_s	600			ns
Output gate hold time t_{DGS}		180	250	ns
Output gate release time t_{DGR}		180	250	ns
Data setup t_{DS}	300			ns
Data hold t_{DH}	300			ns
Clock to store/recirculate t_{DCS}	300			ns
Clock PRR	0		1	MHz

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Input current	V_I = +0.6 V,	V_{SS} = +5 V			500	nA
$I_{\phi L}$	Clock current	V_ϕ = +0.6 V,	V_{SS} = +5 V			500	nA
V_{OL}	Output Low level	R_L = 7.5 kΩ to V_{GG},	I_{sink} = 1.6 mA			+0.5	V
V_{OH}	Output High level	R_L = 7.5 kΩ to V_{GG}		+4			V
I_{SS}	Substrate supply	V_{SS} = +5 V,	V_{GG} = −12 V		15	20	mA
I_{GG}	Gate supply	V_{SS} = +5 V,	V_{GG} = −12 V		15	20	mA
P_D	Power dissipation				255	340	mW
t_{dLH}	Output Low level	R_L = 7.5 kΩ,	C_L = 10 pF, TTL gate	350	450	600	ns
t_{dHL}	Output High level	R_L = 7.5 kΩ,	C_L = 10 pF, TTL gate	350	500	600	ns
C_{IN}	Input	V_I = 0 V,	f = 1 MHz		5	7	pF
C_ϕ	Clock	V_I = 0 V,	f = 1 MHz		6	7	pF

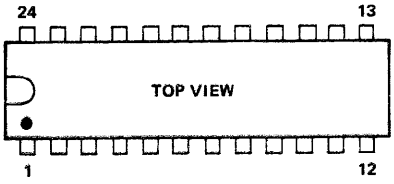
mechanical data and pin configuration

The device is available in both a 24-pin hermetically sealed ceramic dual-in-line package (TMS 3112 JC) and a 24-pin plastic package (TMS 3112 NC). The packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

— continued

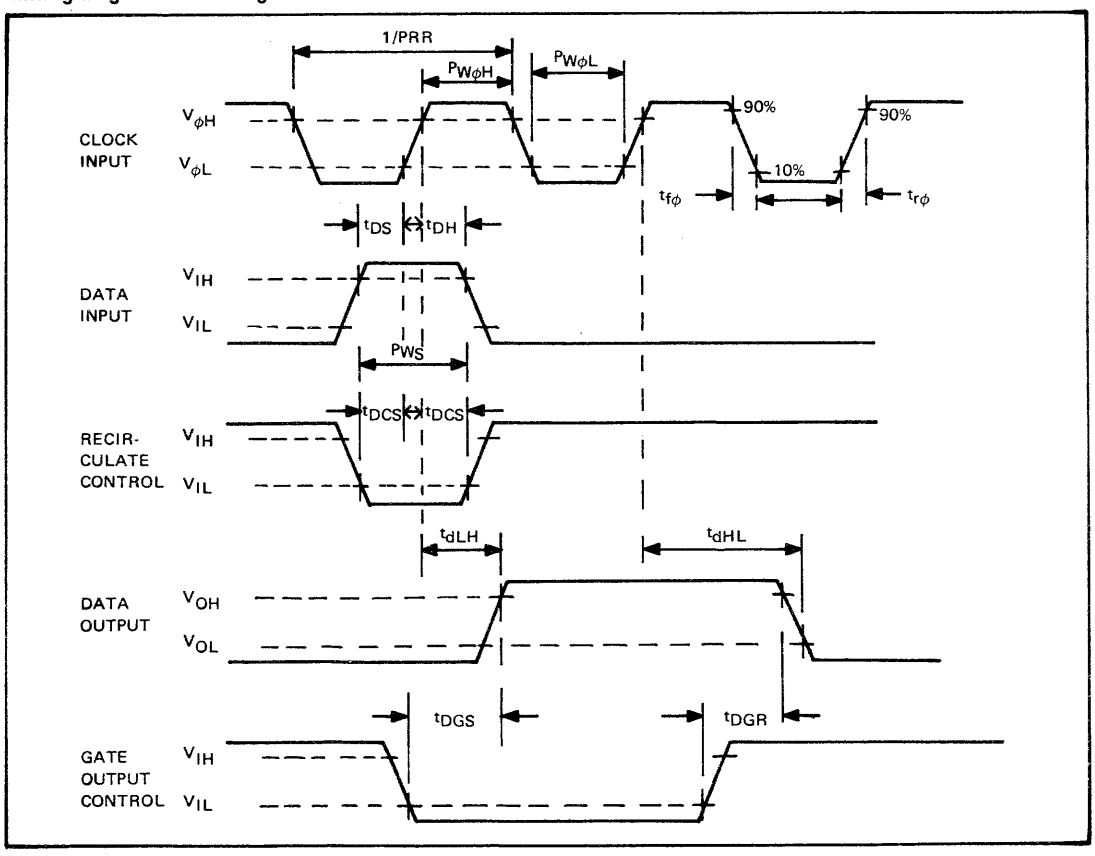
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

mechanical data and pin configuration (continued)



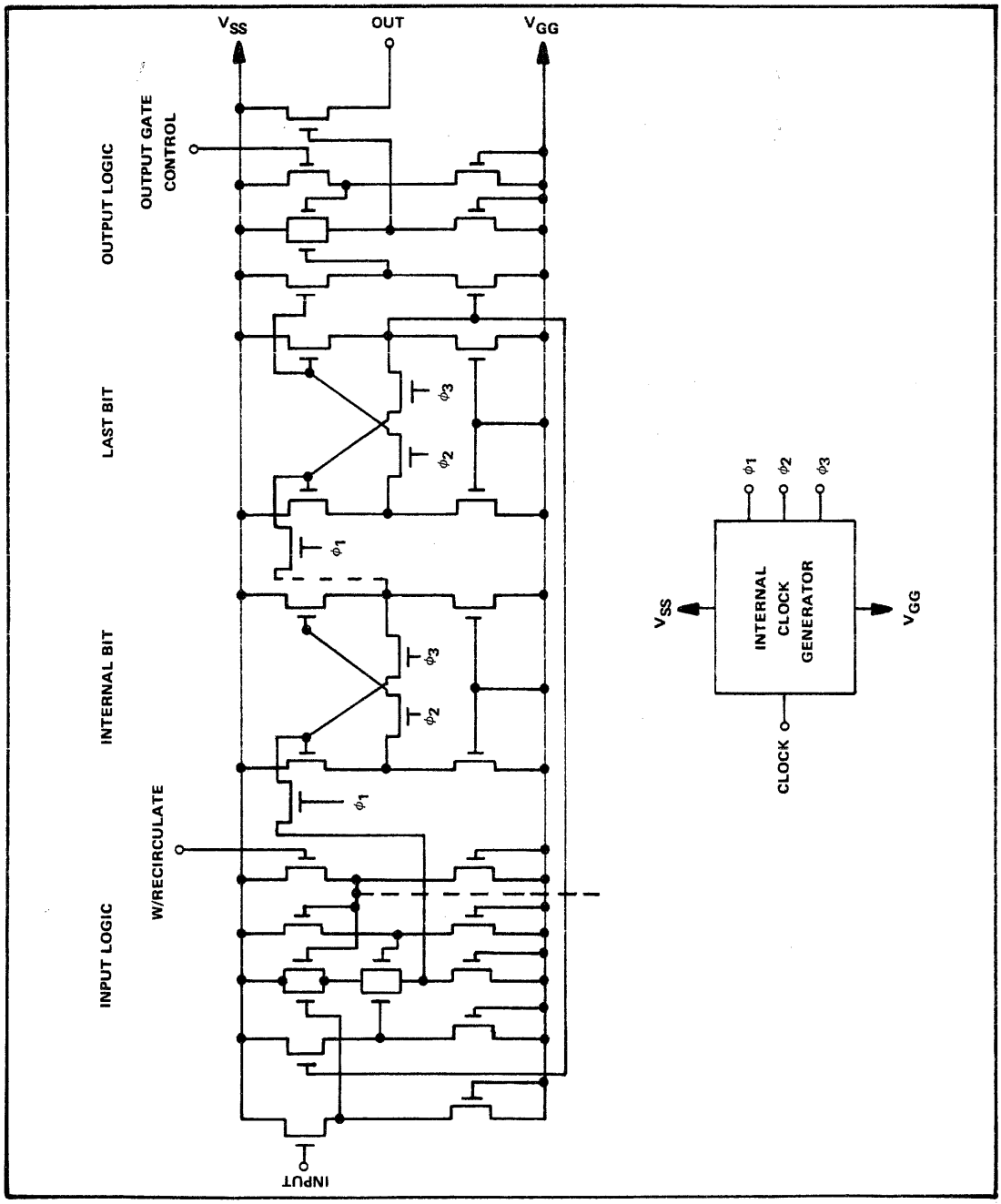
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Input 4	13	Output 3
2	Input 5	14	Output 2
3	Input 6	15	No connection
4	No connection	16	No connection
5	W/Recirculate Cont.	17	Output 1
6	V_{GG}	18	Output gate Cont.
7	Clock	19	No connection
8	Output 6	20	V_{SS}
9	No connection	21	No connection
10	No connection	22	Input 1
11	Output 5	23	Input 2
12	Output 4	24	Input 3

timing diagram and voltage waveforms



14

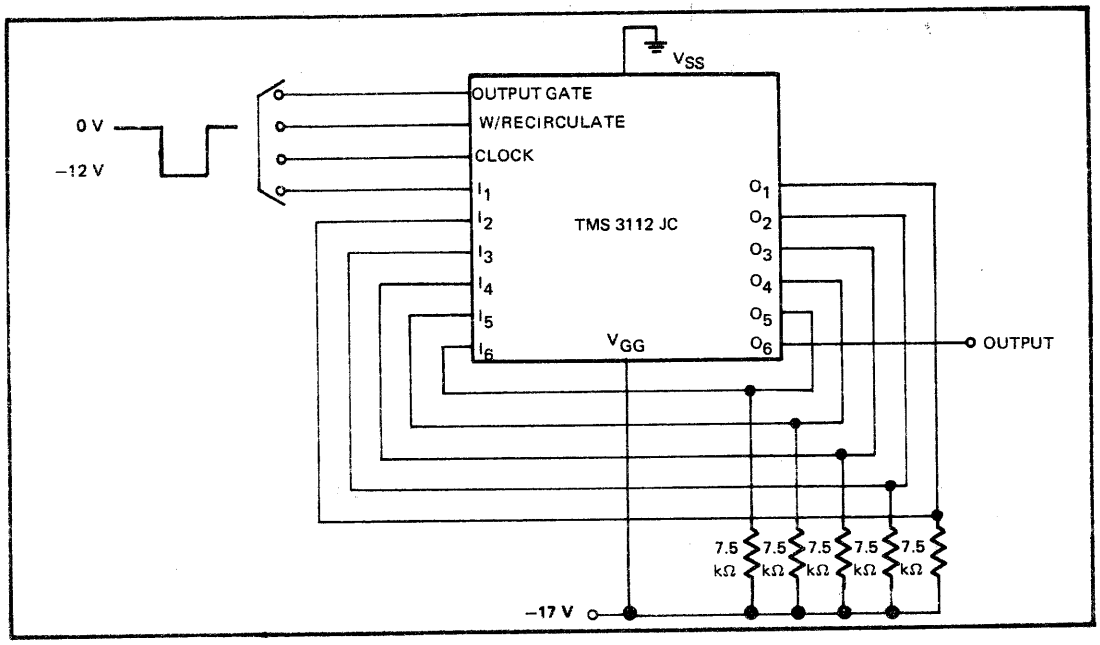
circuit diagram



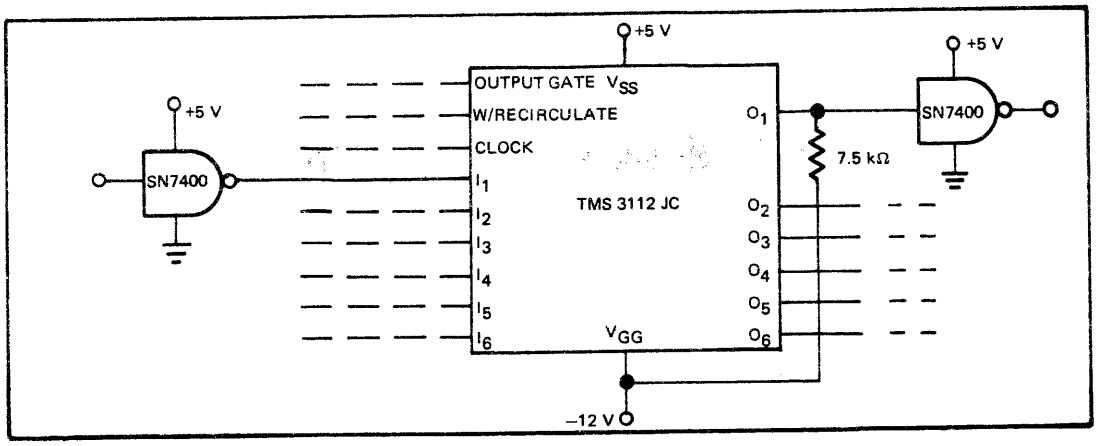
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

interface circuits

a) MOS



b) TTL



14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS
LSI

TMS 3113 JC, NC - DUAL 133-BIT STATIC ACCUMULATOR
TMS 3114 JC, NC - DUAL 128-BIT STATIC ACCUMULATOR

features

- Single-clock TTL level
- Loading and recirculate logic
- DC to 2-MHz operation
- Full TTL compatible (including clock)
- Static logic
- 16-pin dual-in-line package
- Low-threshold technology

description

The TMS 3113 JC/NC and TMS 3114 JC/NC are static accumulators, each consisting of two separate static shift registers with independent input and output terminals and logic for loading or recirculating information. The two shift registers in the TMS 3113 JC/NC are 133-bit devices. Two 128-bit shift registers compose the TMS 3114 JC/NC.

A single clock is required for operation. The clock and all inputs can be driven directly from DTL/TTL logic levels and each register output can drive DTL/TTL circuits. Three clocks are generated internally. Cross-coupled flip-flops are used to implement each bit of delay and enable data to be stored indefinitely between clock pulses.

The entire device is constructed on a single monolithic chip using thick-oxide techniques and low-threshold MOS P-channel enhancement-mode transistors.

Units mounted in 16-pin hermetically sealed ceramic dual-in-line packages are designated "JC". "NC" is the designation for units in 16-pin dual-in-line plastic packages.

logic definition

Positive logic is assumed.

a) LOGIC 1 = most positive voltage (high)

b) LOGIC 0 = most negative voltage (low)

operation

Transferring data into the register is accomplished when the clock and recirculate control are at logic 0. For long-term data storage the clock must be held at a logic 1.

Recirculate occurs when the recirculate control is at a logic 1. Output data appears on the 0-to-1 transition of the clock pulse.

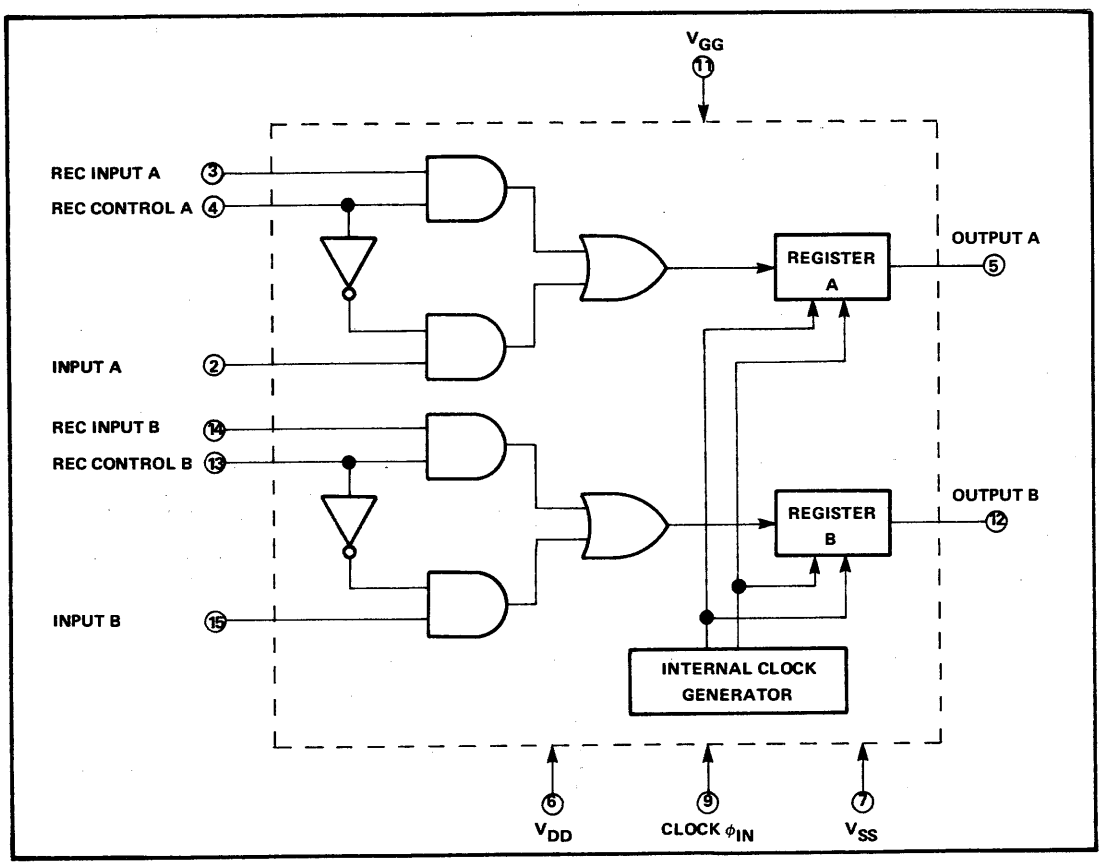
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−6 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−20 V to 0.3 V
Clock input voltage range (See Note 1)	−15 V to 0.3 V
Data input voltage range (See Note 1)	−15 V to 0.3 V
Operating free-air temperature range	−25°C to +85°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram and pin configuration



recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate supply V_{SS}	+4.75	+5	+5.25	V
Drain Supply V_{DD} (Output supply only)		0		V
Gate supply V_{GG}	−11	−12	−13	V
Logic Levels				
Input High level V_{IH}	+3.5			V
Input Low level V_{IL}			+0.6	V
Clock Voltage Levels				
Clock High level $V_{\phi H}$	+3.5			V
Clock Low level $V_{\phi L}$			+0.6	V

— continued

recommended operating conditions (continued)

PARAMETER	MIN	NOM	MAX	UNITS
Pulse Timing				
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			5	μs
Clock pulse width PW_{ϕ} (Clock cycle time)	500			ns
Clock pulse width High level $PW_{\phi H}$	330			ns
Clock pulse width Low level $PW_{\phi L}$	130			ns
Recirculate PW_R	250			ns
Pulse Spacing				
Data setup t_{DB}	100			ns
Data hold t_{DA}	100			ns
Clock to store/recirculate t_{RB}	100			ns
Clock to store/recirculate t_{RA}	150			ns
Pulse Repetition Rate PRR				
Data	0		2.0	MHz
Clock	0		2.0	MHz

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Input Current	V_I = +0.6 V				500	nA
$I_{\phi L}$	Clock Current	V_{ϕ} = +0.6 V				500	nA
Output Voltage Levels (See Note 2)							
V_{OL}	Output LOW level	I_{SINK} = 1.6 mA				+0.5	V
V_{OH}	Output HIGH level	I_{LOAD} = 0.20 mA		+4.0			V
Power Supply Current Drain							
I_{SS}	Substrate supply	V_{SS} = +5 V,	V_{GG} = −12 V		15		mA
I_{GG}	Gate supply	V_{SS} = +5 V,	V_{GG} = −12 V		17		mA
P_D	Power Dissipation	V_{SS} = +5 V,	V_{GG} = −12 V		280		mW

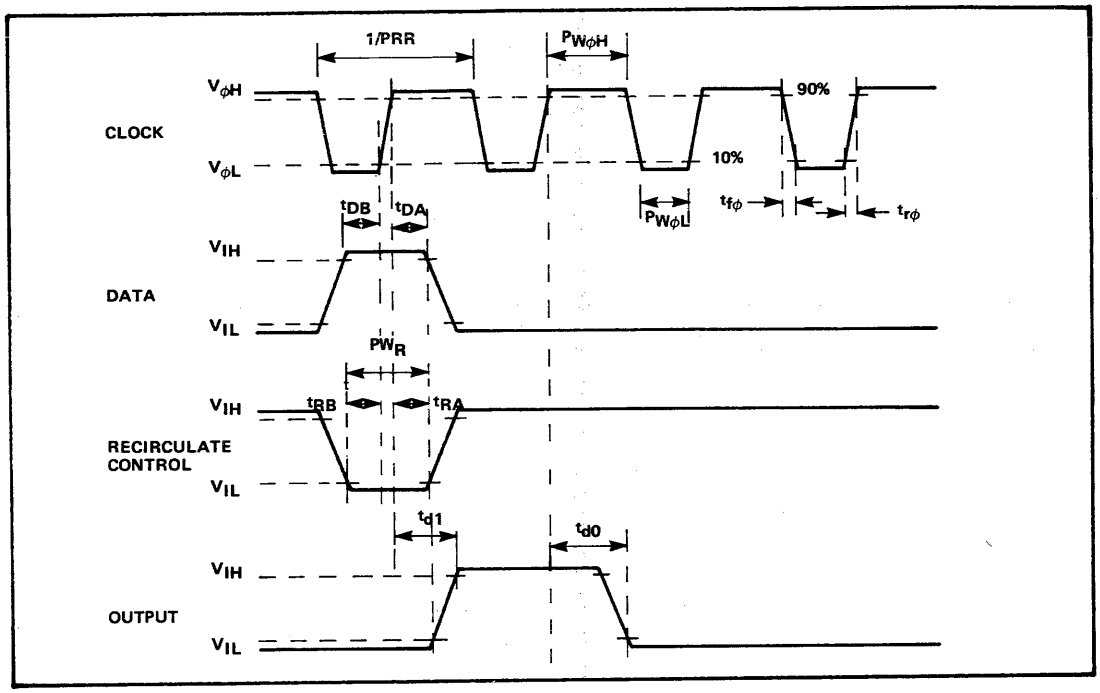
NOTE 2: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and 20 pF. A worst-case MOS load is simulated by a load of 20 kΩ and 20 pF. All loads are connected between output and V_{SS}.

dynamic electrical characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output Logic Delay							
t_{DL}	Output Low level	C_L = 10 pF,	TTL gate		300	350	ns
t_{DH}	Output High level	C_L = 10 pF,	TTL gate		300	350	ns
Capacitance							
C_{IN}	Input	V_I = 0 V,	F = 1.0 MHz		8	12	pF
C_{ϕ}	Clock	V_I = 0 V,	F = 1.0 MHz		9	13	pF

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

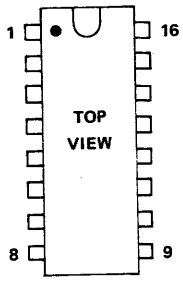
timing diagram and voltage waveforms



mechanical data

The devices are available both in 16-pin hermetically sealed ceramic dual-in-line package (TMS 3113 JC, TMS 3114 JC) and in 16-pin dual-in-line plastic packages (TMS 3113 NC, TMS 3114 NC). The packages are designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)

pin configuration

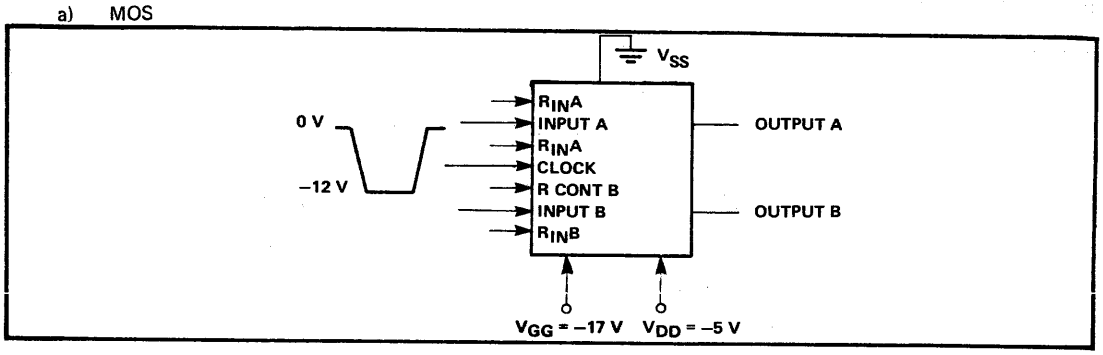


PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	No connection	16	No connection
2	Input A	15	Input B
3	Recirculate Input A	14	Recirculate Input B
4	Recirculate Control A	13	Recirculate Control B
5	Output A	12	Output B
6	V_{DD}	11	V_{GG}
7	V_{SS}	10	No connection
8	No connection	9	Clock ϕ_{IN}

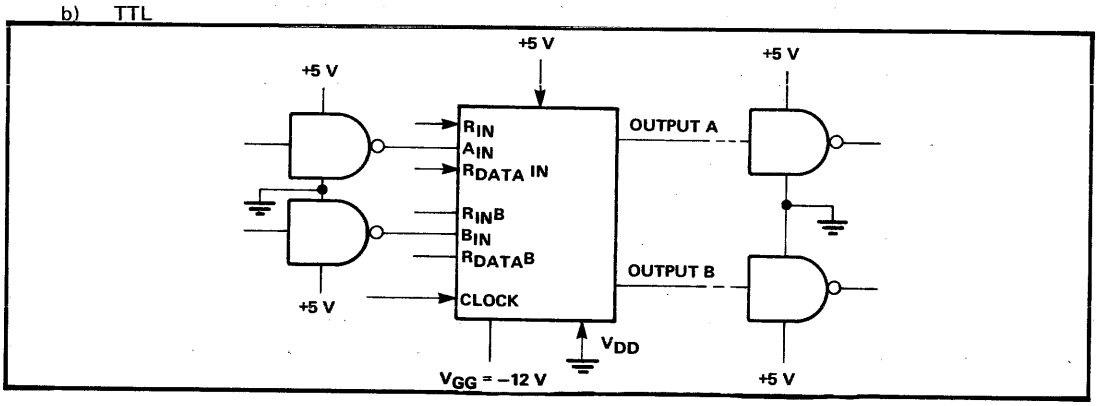
TMS 3113 JC, NC - DUAL 133-BIT STATIC ACCUMULATOR
TMS 3114 JC, NC - DUAL 128-BIT STATIC ACCUMULATOR

interface circuits

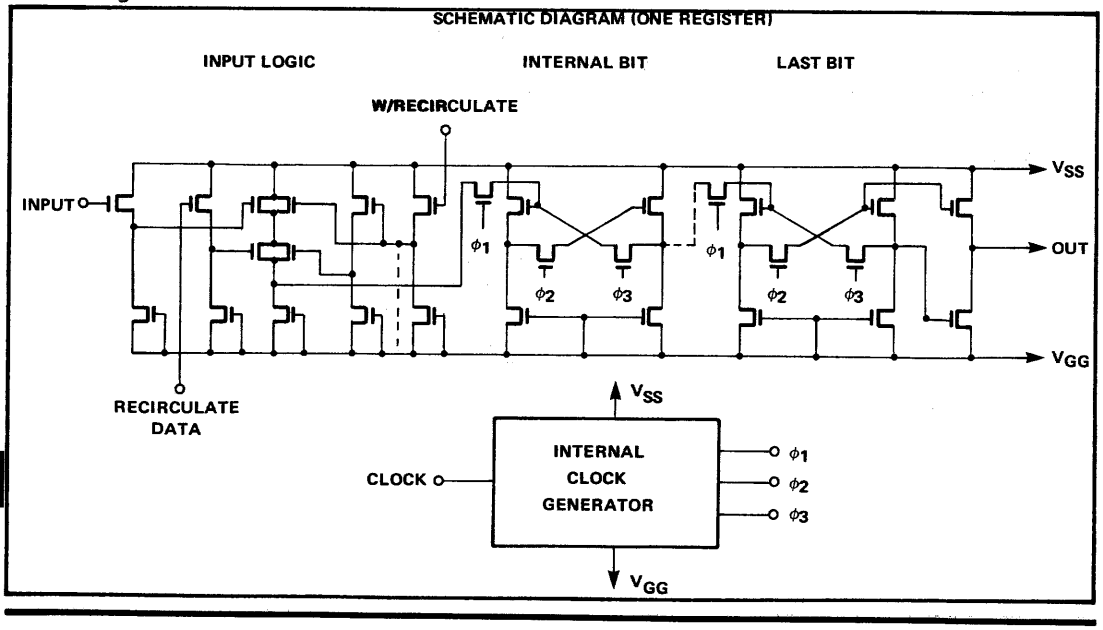
a) MOS



b) TTL



circuit diagram



14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS
LSI

TMS 3304 LR - TRIPLE 66-BIT DYNAMIC SHIFT REGISTER
TMS 3305 LR - TRIPLE 64-BIT DYNAMIC SHIFT REGISTER

JANUARY 1971

features

- 5-MHz operation
- TTL compatibility
- Single-ended (open-drain) output buffers
- Low power dissipation

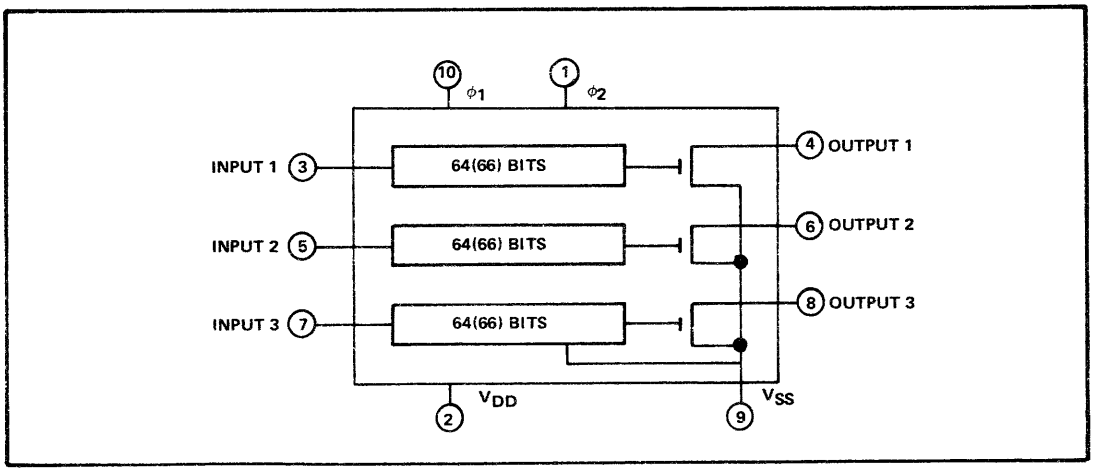
description

The TMS 3304 LR (TMS 3305 LR) consists of three separate 66(64) bit dynamic shift registers with independent input and output terminals and common clocks, power and ground. The gate capacitance of an MOS transistor is used for temporary storage of information between clock pulses. Each register has an unclocked single-ended output buffer to provide an output inverted from the input. The output level is determined by the external load resistor and load power supply.

operation

Transfer of data into the register is accomplished when the ϕ_1 clock is at a logic 1. Data shifting occurs when the ϕ_2 clock is momentarily pulsed to a logic 1, and the ϕ_1 clock to a logic 0. Output data appears on the negative going edge of the ϕ_2 clock pulse.

functional block diagram



logic definition

Negative logic is assumed.

a) Logic 1 = most negative voltage

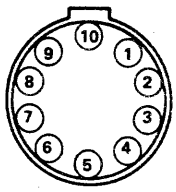
b) Logic 0 = most positive voltage

14

TMS 3304 LR-TRIPLE 66-BIT DYNAMIC SHIFT REGISTER
TMS 3305 LR-TRIPLE 64-BIT DYNAMIC SHIFT REGISTER

mechanical data and pin configuration

The TMS 3304 LR and TMS 3305 LR are mounted in TO-100 packages. (See MOS/LSI packaging section.)



BOTTOM VIEW

LEAD NO.	FUNCTION	LEAD NO.	FUNCTION
1	Clock ϕ_2	6	Out_2
2	V_{DD}	7	In_3
3	In_1	8	Out_3
4	Out_1	9	V_{SS}
5	In_2	10	Clock ϕ_1

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_0 range (See Note 1) . . . . . −30 V to 0.3 V
Clock and data input voltage range (See Note 1) . . . . . −30 V to 0.3 V
Power dissipation . . . . . 350 mW at T_A = 25°C
Operating free-air temperature range . . . . . −55°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal.

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−11	−14	−18	V
Supply voltage V_0	−5	−14	−29	V
Clock logic 0 voltage $V_{\phi(0)}$	0.3	0	−3	V
Clock logic 1 voltage $V_{\phi(1)}$	−20	−28	−29	V
Data logic 0 voltage $V_{in(0)}$	0.3	0	−3	V
Data logic 1 voltage $V_{in(1)}$	−8	−14	−29	V
Clock Overlap voltage (See Figure)			−3	V
Clock pulse width, t_p $V_{\phi 1}$ = −24 V V_{DD} = −12 V	0.1		50	μs
Clock pulse width, t_p V_ϕ = −28 V, V_{DD} = −14 V	0.08		50	μs
Data pulse width P_W	0.15			μs
Clock delay time, t_d (See Voltage Waveforms)			200	μs
Clock rise and fall times, t_r, t_f (See Voltage Waveforms)			5	μs
Clock repetition rate†	0.002	2	5	MHz
Data lead time, t_b (See Voltage Waveforms)	0.08			μs
Data delay time, t_a (See Voltage Waveforms)	0.01			μs

† V_{DD} = −14 V, $V_{\phi(1)}$ = −28 V, normal or extended with TTL output interface.

Nominal values of power supply and clock swing will result in maximum speed of operation. The device has been designed to operate over a broad range that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0 V, −12 V).

14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics at 25°C and nominal operating conditions unless otherwise noted

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{out}	Output voltage level logic 0 (V_ϕ between −20 V and −30 V)	V_O = −14 V, R_L = 10 kΩ		−0.8	−1.2	V
$V_{(1)}$	Output voltage level logic 1 (See Note 1)	V_O = −14 V, R_L = 10 kΩ	−9.0			V
$I_{out(1)}$	Output current logic 1	V_{out} = −14 V, V_ϕ = −28 V V_{out} = −12 V, V_ϕ = −24 V	8 5	12 10		mA mA
I_{dd}	Power supply current drain	V_{DD} = −14 V, V_ϕ = −28 V 20% clock duty cycle V_{DD} = −12 V, V_ϕ = −26 V 20% clock duty cycle		6 5	12 10	mA mA
$I_{\phi L}$	Clock leakage current	$V_{in\phi}$ = −28 V			10	μA
I_{in}	Input leakage current	V_{in} = −28 V			0.5	μA
	Power dissipation			100	350	mW

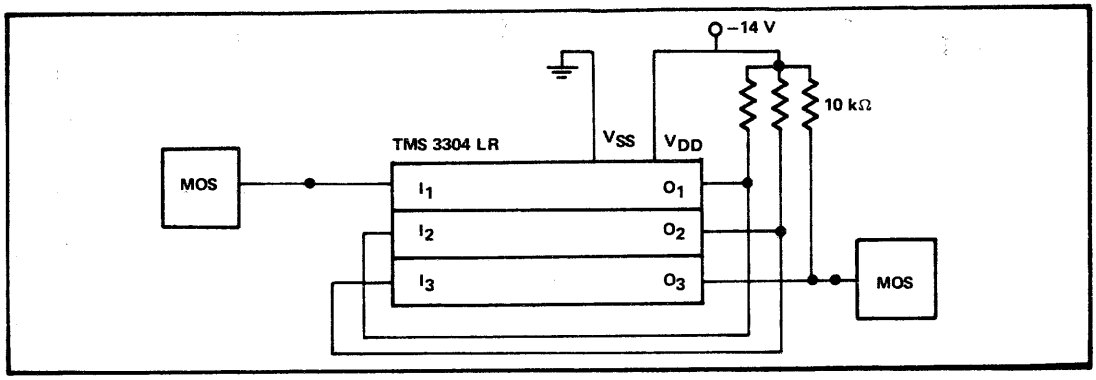
NOTE 1: For an output logic 1 the single ended MOS buffer transistor is "off" and the output voltage is equal to this output voltage power supply V_O.

dynamic electrical characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{d0}	Output logic delay MOS interface (See voltage waveforms)	R_L = 10 kΩ, C_L = 20 pF		60	150	ns
t_{d1}	Output logic delay MOS interface (See voltage waveforms)	R_L = 10 kΩ, C_L = 20 pF		120	250	ns
t_{d0}	Output logic delay TTL interface (See voltage waveforms)	R_L = 10 kΩ, C_L = 20 pF		50	100	ns
t_{d1}	Output logic delay TTL interface (See voltage waveforms)	R_L = 10 kΩ, C_L = 20 pF		60	120	ns
C_I	Data input capacitance	V_I = 0 V		5		pF
C_ϕ	Clock input capacitance	V_ϕ = 0 V		45		pF

interface circuits

a) MOS

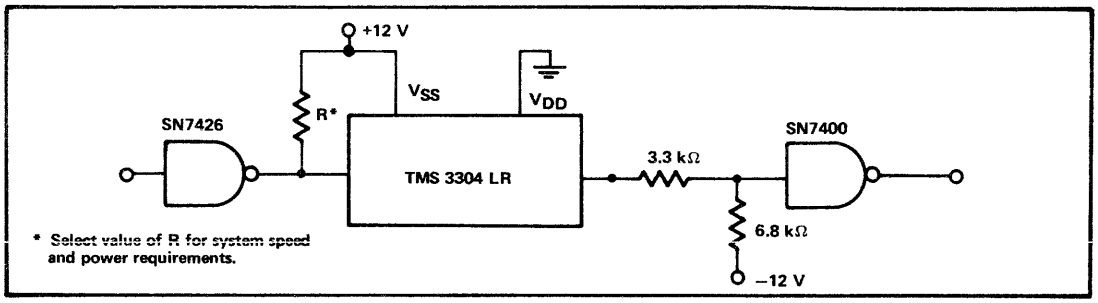


To demonstrate MOS interface the register has been connected as a 198-bit shift register.

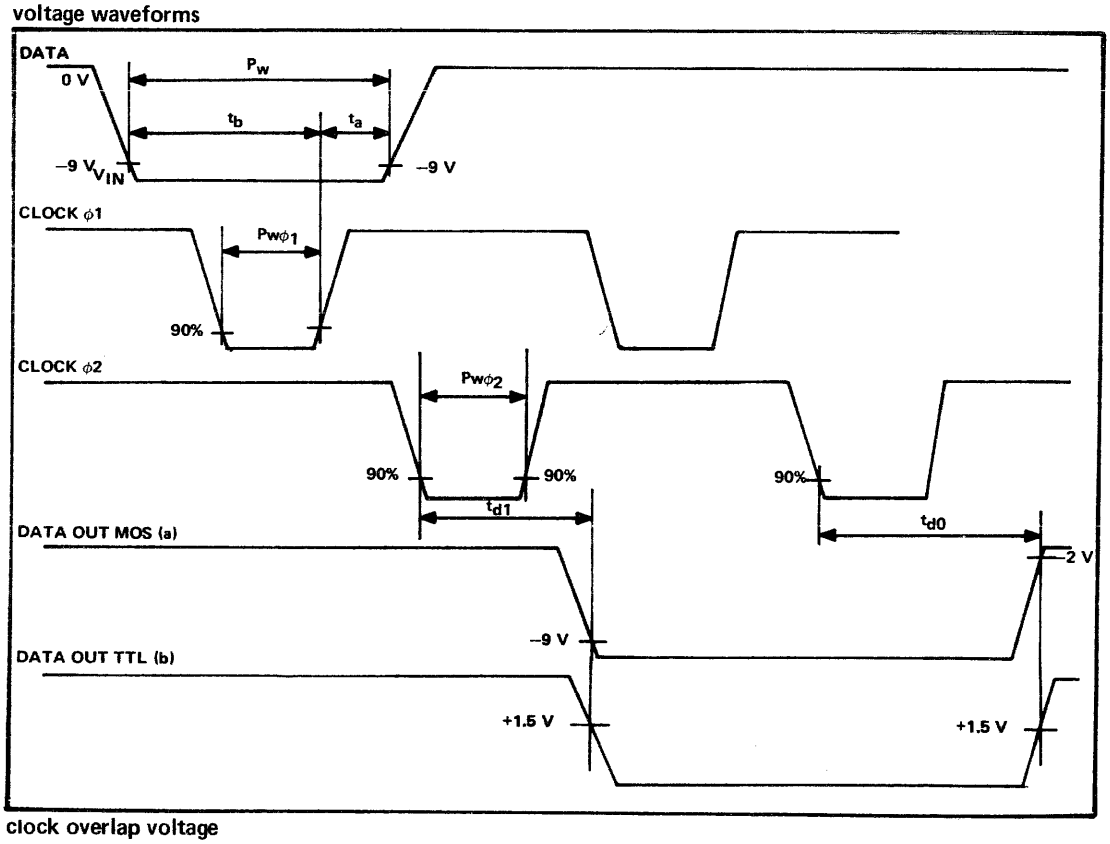
14

interface circuits (continued)

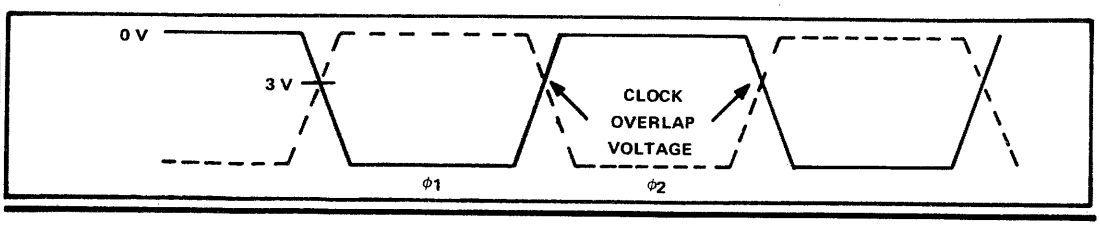
b) TTL



voltage waveforms



clock overlap voltage



14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 3309 JC
TWIN 512-BIT DYNAMIC SHIFT REGISTER/ACCUMULATOR

JANUARY, 1971

features

- Two independent registers/accumulators
- 10-MHz guaranteed operating frequency
- Low power dissipation (typical 90 μW/bit at 1 MHz)
- TTL/DTL compatible
- Recirculate logic on the chip

description

The TMS 3309 JC is a twin 512-bit 4-phase dynamic shift register/accumulator, constructed on a monolithic chip, using thick-oxide P-channel enhancement mode transistors. The device contains two separate register/accumulators with independent control logic for recirculating information, and separate clock lines. The register/accumulators operate at pulse repetition rates from 10 kHz to 5 MHz. A 10-MHz speed of operation is obtained by multiplexing the two registers. Power dissipation is less than 100 μW/bit at 1 MHz.

logic definition

Negative logic is assumed.

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

operation

Four clocks are required for operation of the register/accumulators. Input data is transferred into the register after the end of clock pulse ϕ_1 and before the end of clock pulse ϕ_2. True output data appears after the end of clock pulse ϕ_4 and before the start of the next ϕ_4 clock pulse. Recirculate control is functional when the store pulse overlaps the trailing edge of clock pulse ϕ_3.

The registers may be connected in cascade without external components. The circuit will interface with TTL/DTL and other bipolar logic.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Clock input voltage range (See Note 1)	−30 V to 0.3 V
Data input voltage range (See Note 1)	−30 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

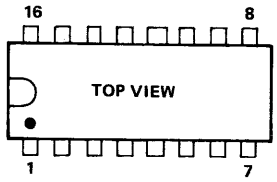
mechanical data

The TMS 3309 JC is mounted in a 16-pin hermetically sealed dual-in-line package consisting of a ceramic base, gold-plated cap, and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

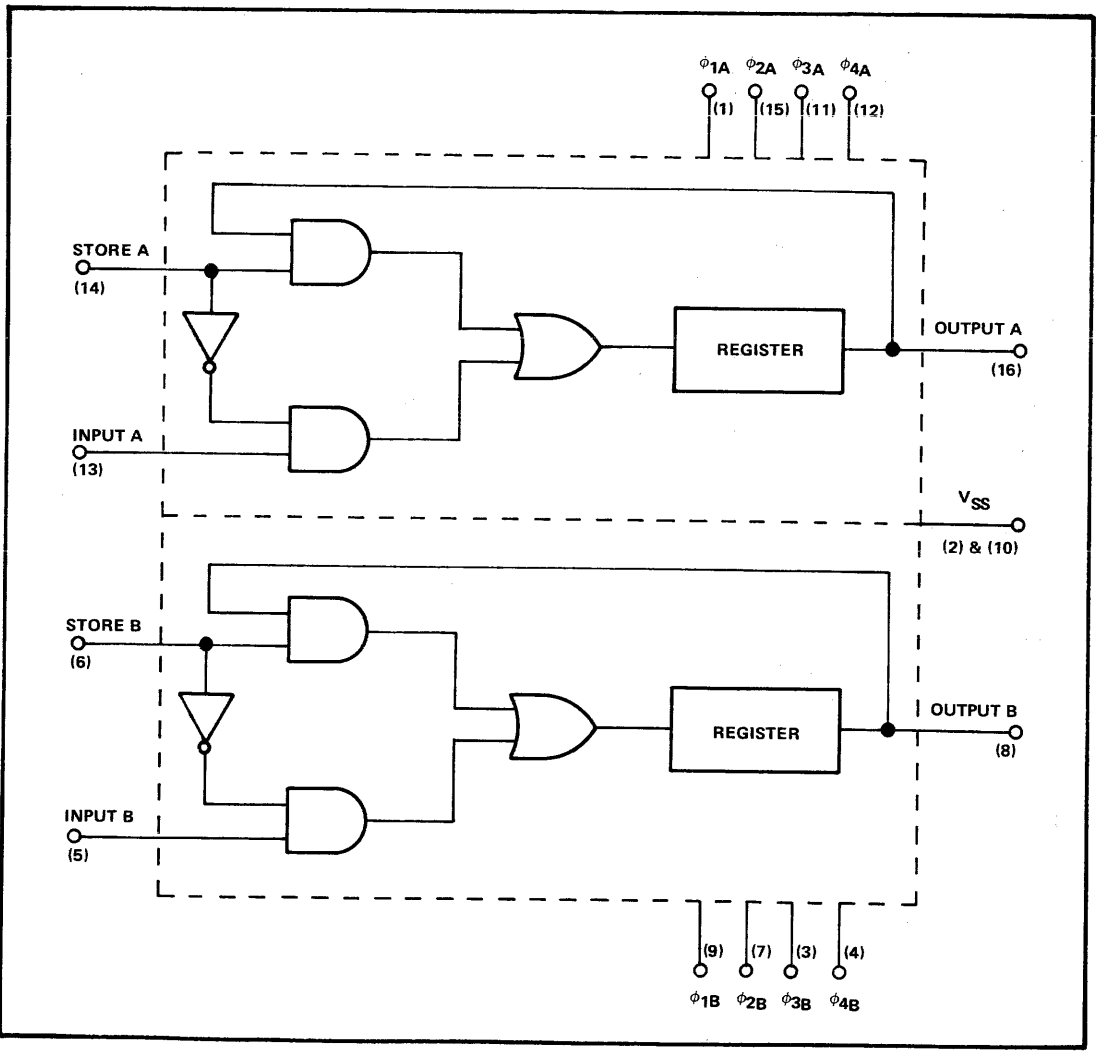
TMS 3309 JC
TWIN 512-BIT DYNAMIC SHIFT REGISTER/ACCUMULATOR

pin configuration



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	ϕ_1 A	9	ϕ_1 B
2	V_{SS}	10	V_{SS}
3	ϕ_3 B	11	ϕ_3 A
4	ϕ_4 B	12	ϕ_4 A
5	IN B	13	IN A
6	REC B	14	REC A
7	ϕ_2 B	15	ϕ_2 A
8	OUT B	16	OUT A

functional block diagram



14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNITS
Logic Levels					
Store and Input Logic 0 $V_{IN(0)}$		+0.3	0	−3.0	V
Store and Input Logic 1 $V_{IN(1)}$		−9	−12	−26	V
Clock Voltage Levels					
Clock Low Logic Level $V_{\phi(0)}$		0.3	0	−2	V
Clock High Logic Level $V_{\phi(1)}$		−22	−24	−26	V
Pulse Timing					
Clock pulse transition, $t_{r\phi}$, $t_{f\phi}$				10	μs
Clock pulse width 1 $PW_{\phi1}$	V_ϕ = −24 V	25			ns
Clock pulse width 2 $PW_{\phi2}$	V_ϕ = −24 V	75		25000	ns
Clock pulse width 3 $PW_{\phi3}$	V_ϕ = −24 V	25			ns
Clock pulse width 4 $PW_{\phi4}$	V_ϕ = −24 V	75		25000	ns
Store PW_S		50			ns
Pulse Spacing					
Clock delay $t_{D\phi23}$	V_ϕ = −24 V	0		25	μs
Clock delay $t_{D\phi41}$	V_ϕ = −24 V, C_L = 10 pF	0		25	μs
Data setup t_{DS}		10			ns
Data hold t_{DH}		10			ns
Store/recirculate setup t_{DCS}		30			ns
Store recirculate hold t_{DCH}		30			ns
Pulse Overlap (See Note 2)					
Clock − Clock $t_{D\phi12}$, $t_{D\phi34}$	V_ϕ = −24 V	60		10000	ns
Pulse Repetition Rate (See Note 3)					
Data PRR	V_ϕ = −24 V	0.01		5	MHz
Clock PRR	V_ϕ = −24 V	0.01		5	MHz

NOTES: 2. Only clock pulse pairs ϕ_1, ϕ_2 or pairs ϕ_3, ϕ_4 may be simultaneously more than 2 volts below V_{SS}.
3. The maximum operating frequency pertains to each shift register operated independently. If multiplexing is used, double the maximum operating frequency.

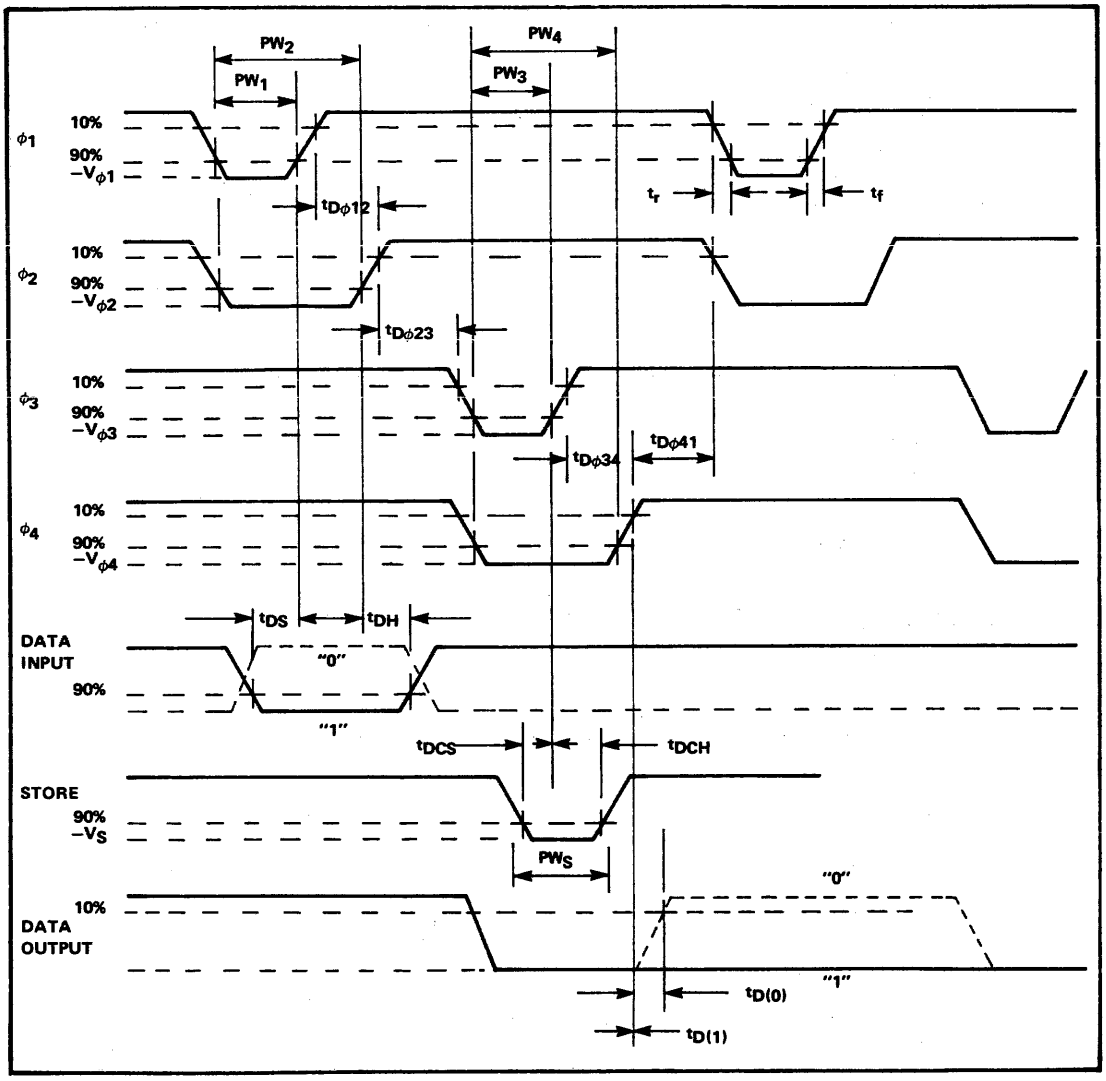
electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_L	Input Current (Leakage)	V_I = −20 V			500	nA
ϕ_L	Clock Current (Leakage)	V_{IN} = −26 V, Output Open			100	μA
Output Voltage Levels						
$V_{OUT(0)}$	Output Level (0)	$V_{\phi(0)}$ = −1.5 V, $V_{IN(0)}$ = −3.5 V		1.5	2.5	V
$V_{OUT(1)}$	Output Level (1)	$V_{\phi(1)}$ = −22 V, $V_{IN(1)}$ = −9 V	−10	−16		V
Power Dissipation/Bit		PRF = 1 MHz, V_ϕ = −24 V, C_L = 10 pF		90		μW
Output Logic Delay						
$t_{D(1)}$	Output Logical 1 Level				0	ns
$t_{D(0)}$	Output Logical 0 Level				20	ns
Capacitance (See Note 4)						
C_{IN}	Input	V_ϕ = 0 V		5		pF
C_ϕ	Clock $C_{\phi1} = C_{\phi3}$	V_ϕ = 0 V		90		pF
C_ϕ	Clock $C_{\phi2} = C_{\phi4}$	V_ϕ = 0 V		40		pF

NOTE 4: The capacitance pertains to each register.

14

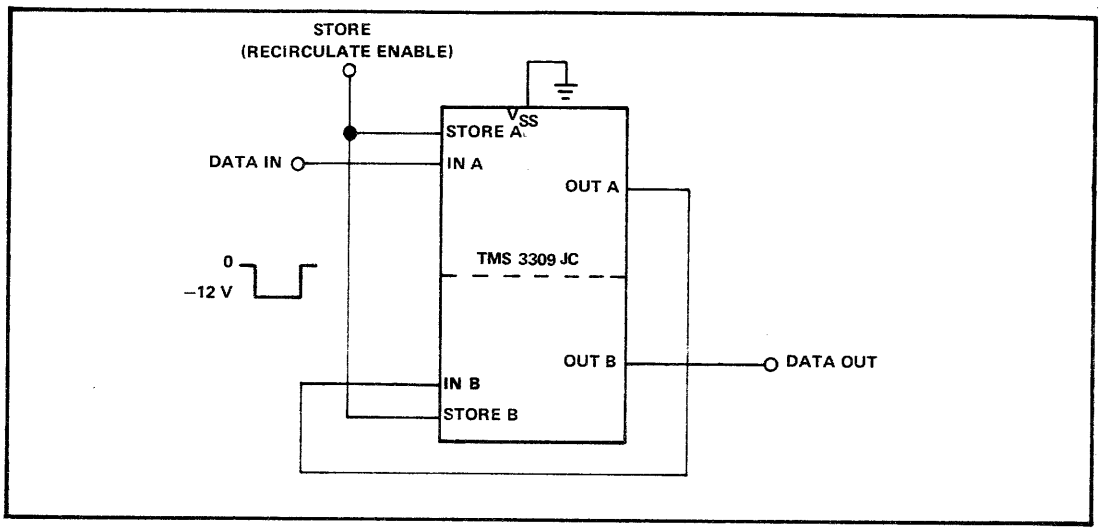
timing diagram and voltage waveforms



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

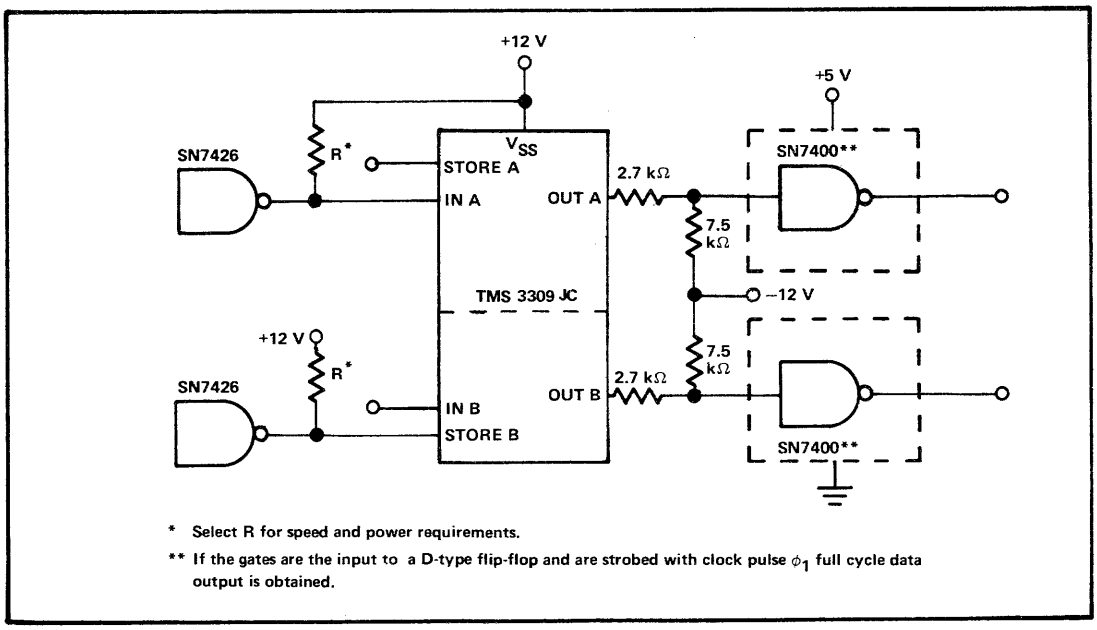
interface circuits

a) MOS interface



NOTE: In this figure the register has been connected as a 1024-bit shift register.

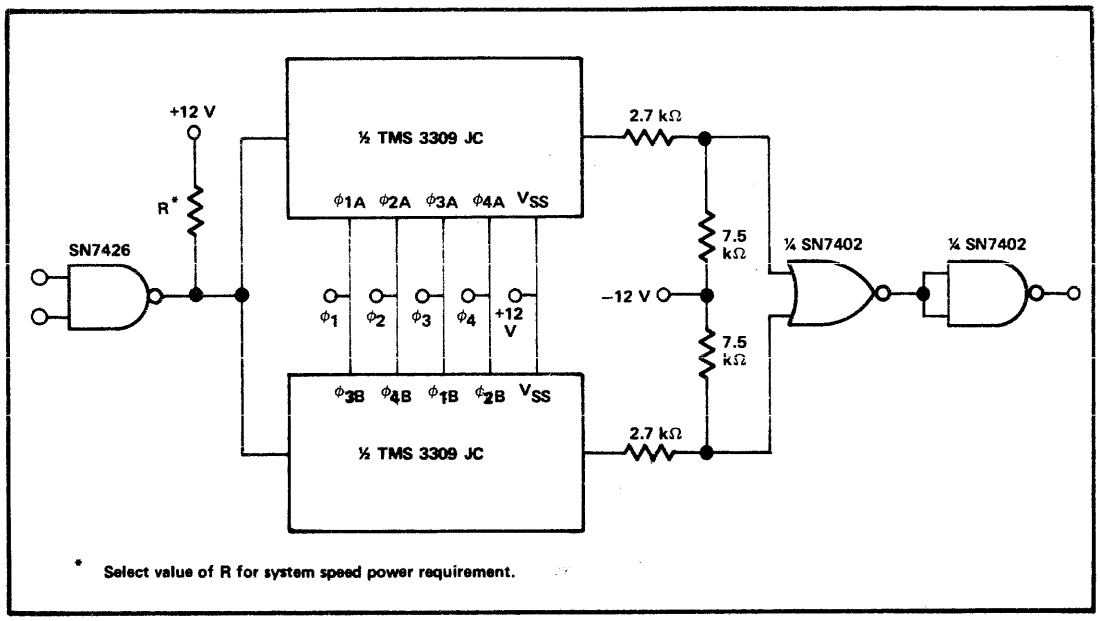
b) TTL interface



* Select R for speed and power requirements.

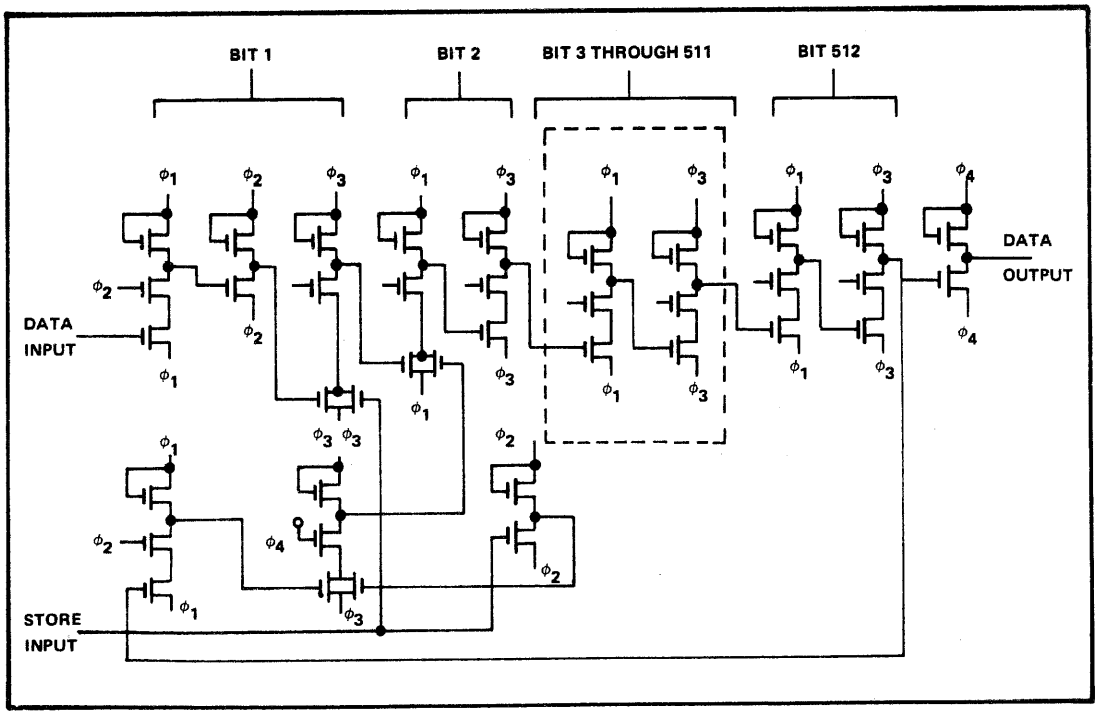
** If the gates are the input to a D-type flip-flop and are strobed with clock pulse ϕ_1 full cycle data output is obtained.

multiplexing of TMS 3309 JC 10-MHz operation



* Select value of R for system speed power requirement.

circuit diagram



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 3314 JC, TMS 3314 NC
TRIPLE (60+4) DYNAMIC SHIFT REGISTER

FEBRUARY, 1971

features

- 2-MHz operation
- TTL compatible
- Open-drain output buffers
- Three 60-bit registers
- Three 4-bit registers
- Dual-in-line package

description

The TMS 3314 JC/NC contains three separate 60-bit, and three separate 4-bit dynamic shift registers constructed on a single monolithic chip, using thick-oxide enhancement-mode P-channel MOS transistors.

Each register has independent input and output terminals and common clock and power lines. Each has an unlocked open-drain output buffer to provide an output inverted from the input. The inputs and outputs terminals of the registers are oriented for optimum printed-circuit-board layout.

The TMS 3314 JC/NC is ideal for data-handling applications in desk calculators, terminals, and peripheral equipment.

"TMS 3314 JC" is the part number for a unit mounted in a 16-pin hermetically sealed ceramic dual-in-line package. A unit mounted in a 16-pin plastic package is designated "TMS 3114 NC."

logic definition

Negative logic is assumed:

a) Logic 1 = most negative (LOW) voltage

b) Logic 0 = most positive (HIGH) voltage

operation

Two clock pulses are required for operation of the registers. The pulses should not simultaneously be at Low levels. Data is transferred into the registers when clock pulse ϕ_1 is pulsed to a Low level. Data shift occurs when clock pulse ϕ_2 is pulsed to a Low level. Output data appears on the High-to-Low transition of clock pulse ϕ_2.

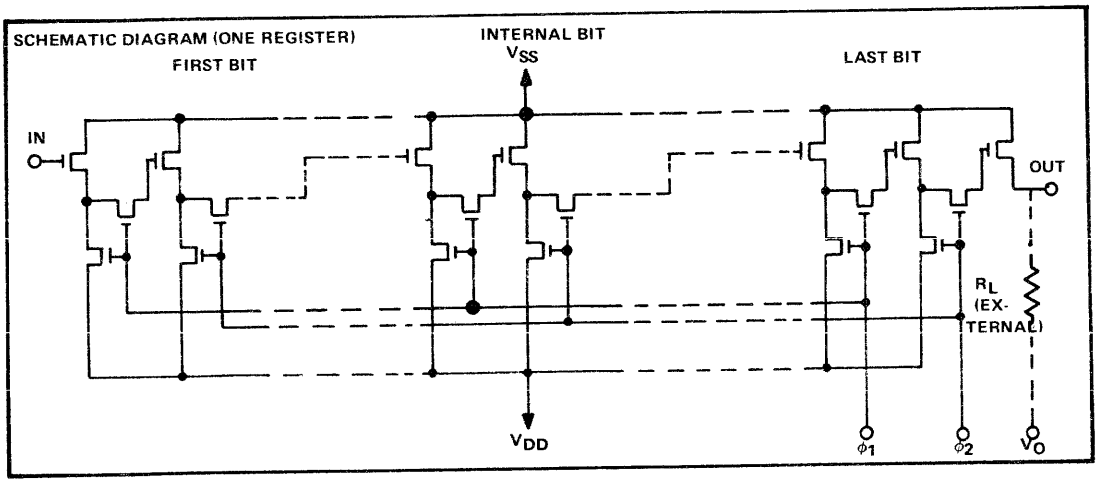
The registers can drive DTL/TTL gate loads by means of a pull-down resistor, connected between the output terminal and the V_{DD} supply.

absolute maximum ratings over operating free-air temperature range

Supply voltage V_{DD} range (See Note 1)	−30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−30 V to 0.3 V
Clock input voltage range (See Note 1)	−30 V to 0.3 V
Data input voltage range (See Note 1)	−30 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

circuit diagram



recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Operating Voltage				
Drain supply V_{DD}	−11	−14	−16	V
Output supply V_O	−11	−14	−16	V
Logic Levels				
Input HIGH level (logic 0) V_{IH}	−3	0	+0.3	V
Input LOW level (logic 1) V_{IL}	−8	−14	−29.0	V
Clock Voltage Levels				
HIGH level (logic 0) $V_{\phi H}$	−3	0	+0.3	V
LOW level (logic 1) $V_{\phi L}$	−22	−28	−29.0	V
Pulse Timing				
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			5	μs
Clock pulse width 1 $PW_{\phi 1}$	0.22		10	μs
Clock pulse width 2 $PW_{\phi 2}$	0.22		10	μs
Pulse Spacing				
Clock delay $t_{D\phi 12}$	0.01		100	μs
Clock delay $t_{D\phi 21}$	0.01		100	μs
Data setup t_{DS}	75			ns
Data hold t_{DH}	75			ns
Clock Pulse Overlap (See Note 2)		(NOTE 2)		ns
Pulse Repetition Rate (Note 3) PRR				
Data	0.01		2	MHz
Clock	0.01		2	MHz

NOTES: 2. The two clock pulses should not be simultaneously more than 3 V below V_{SS}.
3. R_L = 13 kΩ, C_L = 10 pF.

14

Maximum speed of operation will be obtained when operating at nominal conditions. The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V).

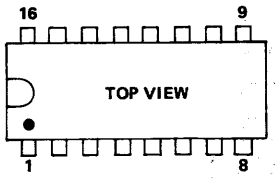
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Current (Leakage)	$V_I = -14$ V			500	nA
$I_{\phi L}$	Clock Current (Leakage)	$V_I = -29$ V			100	μA
Output Voltage Levels						
V_{OL}	Output LOW level (logic 1)	R_L = 13 kΩ to V_{DD}, C_L = 10 pF	−9	−10		V
V_{OH}	Output HIGH level (logic 0)	R_L = 13 kΩ to V_{DD} C_L = 10 pF			−2.5	V
Output Current						
I_O	Logic 0	−14 V applied to output			10	μA
I_O	Logic 1	−14 V applied to output	2			mA
Power Supply Current Drain						
I_{DD}	Drain supply	R_L = 13 kΩ to V_{DD}, $PW_{\phi 1} = PW_{\phi 2}$ = 200 ns, PRF = 2 MHz		15	20	mA
P_D	Power dissipation			210	280	mW
Output Logic Delay						
t_{DLH}	Output Low level (logic 1)	R_L = 13 kΩ, C_L = 10 pF, V_ϕ = −24 V		80	150	ns
t_{DHL}	Output High level (logic 0)	R_L = 13 kΩ, C_L = 10 pF, V_ϕ = −25 V		225	300	ns
Capacitance						
C_{IN}	Input	V_ϕ = 0 V, f = 1 MHz		3	5	pF
C_ϕ	Clock	V_ϕ = 0 V, f = 1 MHz		55	65	pF

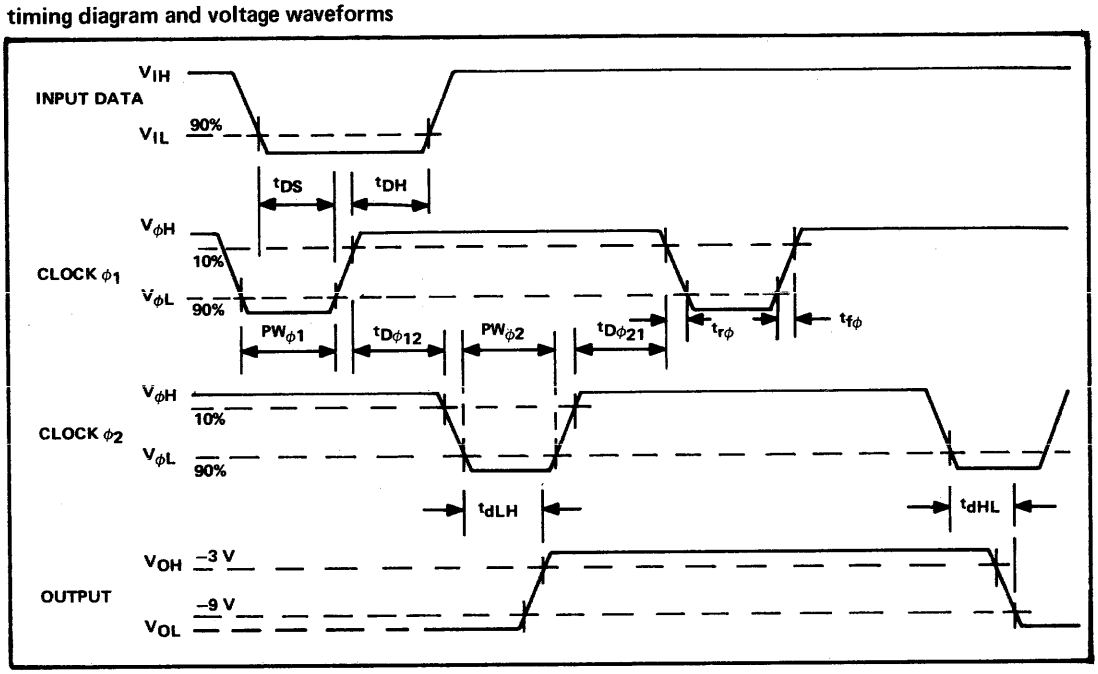
mechanical data and pin configuration

The device is available in both a 16-pin hermetically sealed ceramic dual-in-line package (TMS 3314 JC) and a 16-pin dual-in-line plastic package (TMS 3314 NC). The packages are designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)



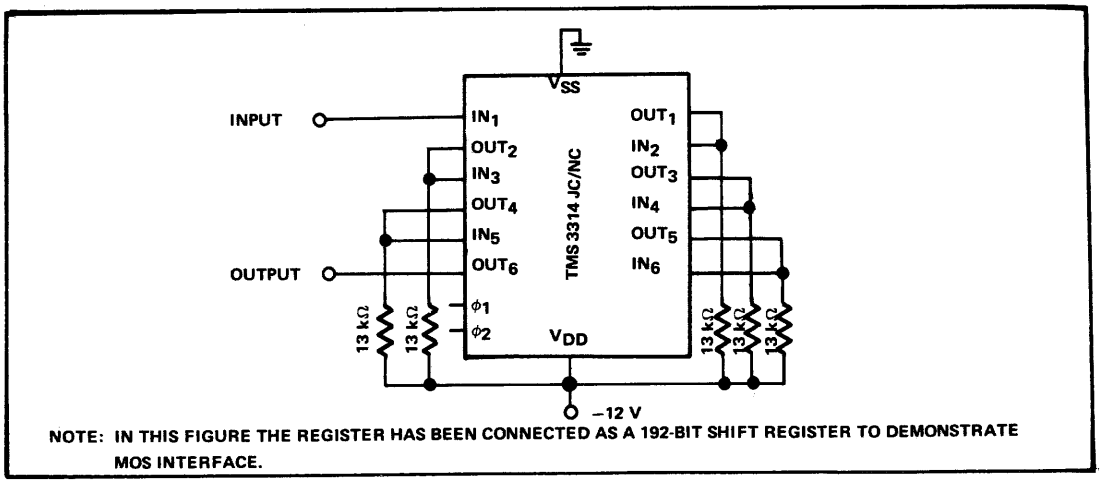
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	IN_1	9	$\phi 2$
2	OUT_2	10	IN_6
3	IN_3	11	OUT_5
4	OUT_4	12	IN_4
5	IN_5	13	OUT_3
6	OUT_6	14	IN_2
7	$\phi 1$	15	OUT_1
8	V_{SS}	16	V_{DD}

timing diagram and voltage waveforms



interface circuits

a) MOS

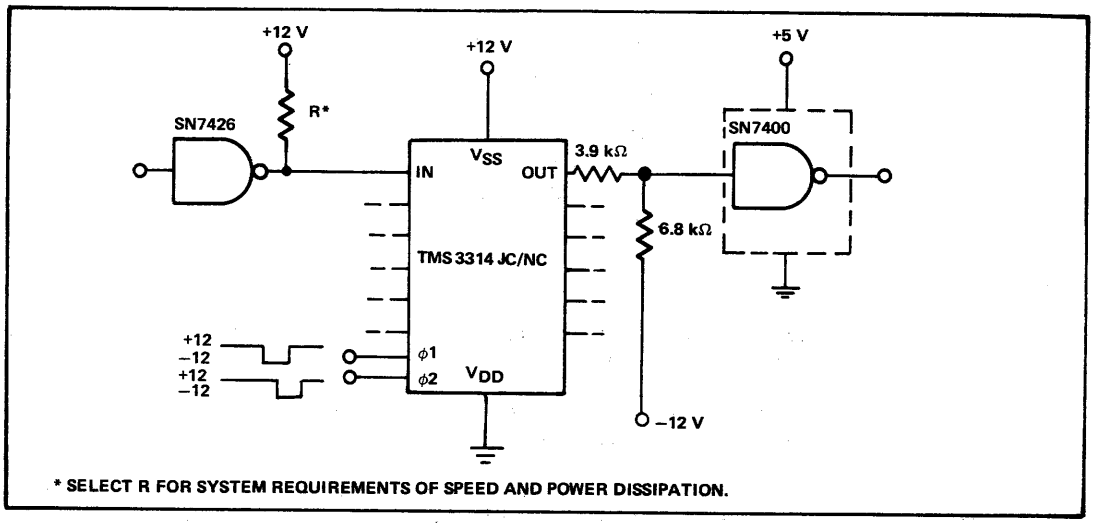


NOTE: IN THIS FIGURE THE REGISTER HAS BEEN CONNECTED AS A 192-BIT SHIFT REGISTER TO DEMONSTRATE MOS INTERFACE.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

interface circuits (continued)

b) TTL



* SELECT R FOR SYSTEM REQUIREMENTS OF SPEED AND POWER DISSIPATION.

14

MOS
LSI

TMS 3401 LC, NC - 512-BIT DYNAMIC SHIFT REGISTER
TMS 3402 LC, NC - 500-BIT DYNAMIC SHIFT REGISTER

features

- Two-phase dynamic logic
- 5-MHz operation
- Directly TTL compatible at input and output
- No external resistors required
- Low power dissipation — 0.2 mW/bit 1 MHz
- Output delay — 50 ns
- Low-threshold technology
- Power supplies — +5 V, −12 V
- Push-pull output buffer

description

The 512-bit TMS 3401 LC/NC and the 500-bit TMS 3402 LC/NC are high-speed dynamic shift registers. A ratioless two-phase design has been employed to minimize power consumption.

Because both input and output are TTL compatible without the use of external resistors, these registers can be strung together directly and can interface directly with bipolar systems.

The circuits are constructed using MOS P-channel thick-oxide and low-threshold technologies to implement low-threshold MOS devices. The design uses programmable techniques and the number of bits may be altered through single-level programming for a nominal charge.

logic definition

Positive logic is assumed.

a) Logic 1 = most positive (HIGH) voltage

b) Logic 0 = most negative (LOW) voltage

operation

Data is transferred into the register when the ϕ_1 clock is Low (−12 V). The data must be held steady for at least 30 nanoseconds before the clock goes to the High state (+5 V). One of two internal resistors (1.5 kΩ or 6 kΩ) can be connected to assist in pulling up the logic 1 level provided by DTL or TTL.

Output delay time is defined as the period required for the output to reach the DTL or TTL changeover threshold after the ϕ_2 clock reaches 90% of its Low voltage. This time is faster than 50 nanoseconds.

programming

The device has been so designed that by changing only one level of artwork the designer can obtain any bit length between 233 and 512 bits. The 512-bit length (TMS 3401 LC/NC) and the 500-bit length (TMS 3402 LC/NC) are available off the shelf. Other bit lengths are obtained through use of computer-aided design methods, providing fast, accurate and economical turnaround. The electrical characteristics and pin configuration are the same for the whole family of devices.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −20 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −20 V to 0.3 V
Clock input voltage range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage range (See Note 1) . . . . . −20 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C
Input pull-up resistor voltage range . . . . . −6 V to 0.3 V

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

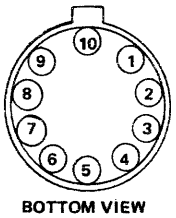
recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate supply V_{SS}	+4.5	+5	+5.5	V
Drain supply V_{DD}	0	0	0	V
Gate supply V_{GG}	−13	−12	−11	V
Logic Levels				
Input HIGH level V_{IH}	V_{SS} −1.5		V_{SS}	V
Input LOW level V_{IL}	−13		+0.8	V
Clock Voltage Levels				
Clock HIGH level $V_{\phi H}$ (See Note 2)	V_{SS} −1		V_{SS}	V
Clock LOW level $V_{\phi L}$	−14	−12	−11	V
Pulse Timing				
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			1	μs
Clock pulse width 1 (5 MHz) $PW_{\phi 1}$	0.075		10	μs
Clock pulse width 2 (5 MHz) $PW_{\phi 2}$	0.075		10	μs
Pulse Spacing				
Clock delay $t_{d\phi 12}$			50	μs
Clock delay $t_{d\phi 21}$			50	μs
Data setup t_{DS}	50			ns
Data hold t_{DH}	10			ns
Pulse Repetition Rate PRR				
Data	0.02		5	MHz
Clock	0.02		5	MHz

NOTE 2: Both clock pulses should not be simultaneously more than 2 V below V_{SS}.

mechanical data and pin configuration

The TMS 3401 LC and the 3402 LC are mounted in TO-100 packages. (See MOS/LSI packaging section.)



BOTTOM VIEW

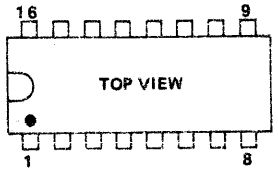
LEAD NO.	FUNCTION	LEAD NO.	FUNCTION
1	V_{DD}	6	Input pull-up resistor (1.5 kΩ)
2	Output	7	Input
3	V_{GG}	8	Input pull-up resistor (6 kΩ)
4	V_{SS}	9	Clock ϕ_2
5	No connection	10	Clock ϕ_1

14

— continued

mechanical data and pin configuration (continued)

The TMS 3401 NC and the TMS 3402 NC are mounted in 16-pin dual-in-line plastic packages designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Input	9	V_{GG}
2	R_2 (6 kΩ)	10	No connection
3	$\phi 2$	11	No connection
4	No connection	12	No connection
5	$\phi 1$	13	No connection
6	V_{DD}	14	No connection
7	No connection	15	R_1 (1.5 kΩ)
8	Output	16	V_{SS}

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Input current (leakage)	V_I = 0 V,	V_{SS} = +5 V			500	nA
$I_{\phi L}$	Clock current (leakage)	V_ϕ = 0 V,	V_{SS} = +5 V			50	μA
Output Voltage Levels							
V_{OL}	Output LOW level (Note 3)	TTL load, f = 5 MHz	C_L = 10 pF,		+0.15	+0.4	V
V_{OH}	Output HIGH level (Note 3)	TTL load, f = 5 MHz	C_L = 10 pF,	+3.6	+4.5		V
V_{OL}	Output LOW level (Note 3)	I_O = +1.6 mA			+0.15	+0.4	V
V_{OH}	Output HIGH level (Note 3)	I_O = −1 mA		+4.5	+4.7		V
Power Supply Current Drain							
I_{DD}	Drain supply (Note 4)	V_{SS} = 0,	V_{GG} = 17 V			0.1	mA
I_{GG}	Gate supply (Note 4)	V_{DD} = 5 V			3.5	7	mA
P_D	Power dissipation				350		mW

NOTES: 3. For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF. A worst-case MOS load is simulated by a load of 20 kΩ and 20 pF. All loads are connected between output and V_{SS}.

4. Does not include output stage load or transient current. In the MOS load mode, the current will consist of transients due to capacitor discharge and/or leakage current.

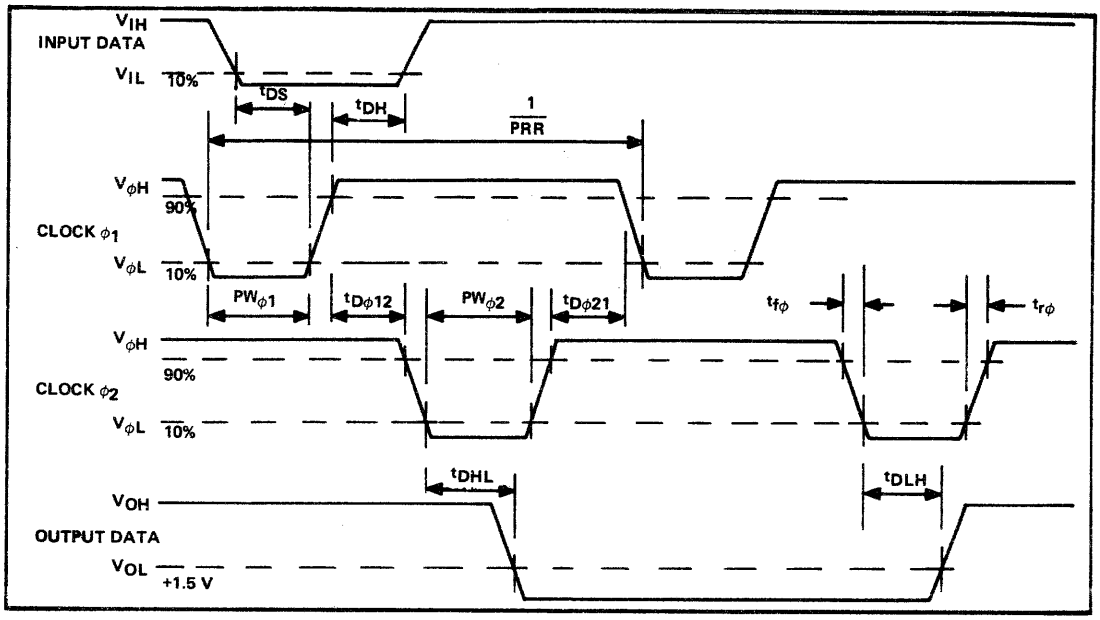
dynamic electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output Logic Delay							
t_{DLH}	Output LOW level	TTL load, f = 5 MHz	C_L = 10 pF,		10	50	ns
		R_L = 10 MΩ, f = 5 MHz	C_L = 10 pF,		15	50	ns
t_{DHL}	Output HIGH level	TTL load, f = 5 MHz	C_L = 10 pF,		11	50	ns
		R_L = 10 MΩ, f = 5 MHz	C_L = 10 pF,		4	30	ns
Capacitance							
C_{IN}	Input	V_I = V_{SS},	f = 1 MHz		5	7	pF
C_ϕ	Clock	V_ϕ = V_{SS},	f = 1 MHz		220	280	pF

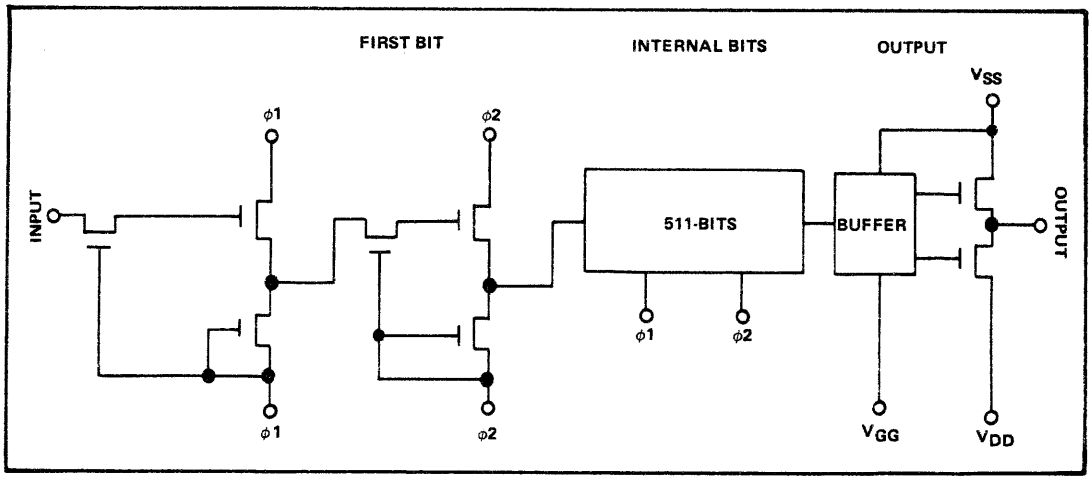
14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

timing diagram and voltage waveforms



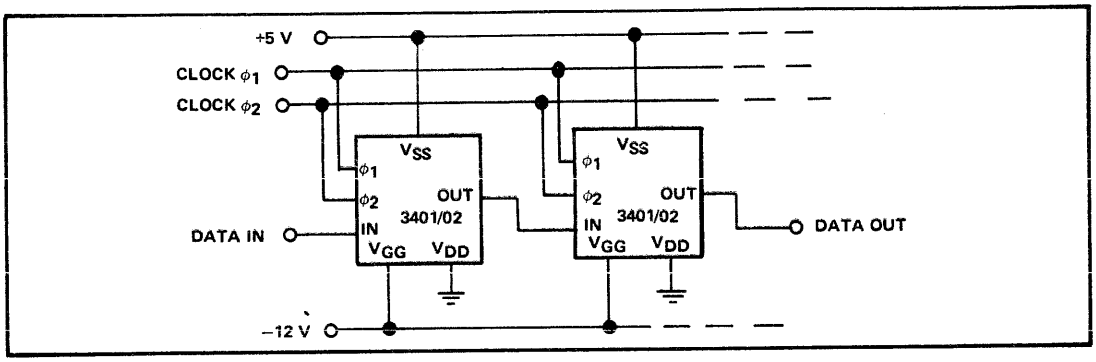
internal diagram



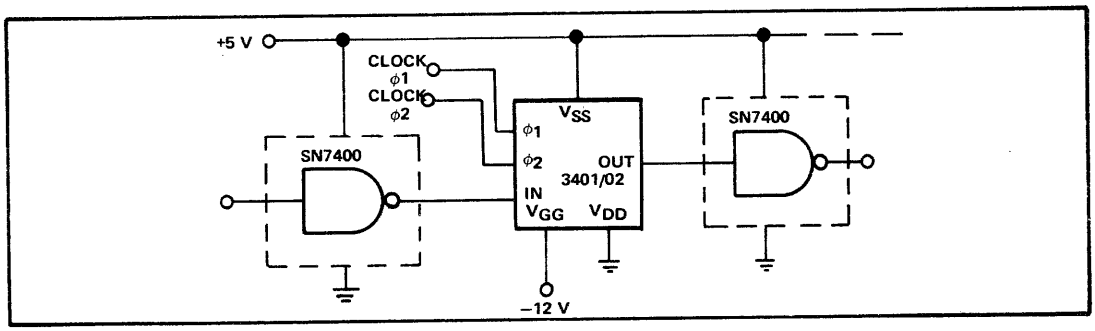
14

interface circuits

a) MOS



b) TTL



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS
LSI

TMS 3404 JC, TMS 3404 NC
DUAL 512-BIT DYNAMIC SHIFT REGISTER

FEBRUARY, 1971

features

- Two-phase dynamic logic
- 5-MHz shift rate
- Low power – 0.1 mW/bit at 1 MHz
- Power supplies – +5 V, –12 V
- Single-ended output
- TTL compatible – without external components
- Low-threshold technology

description

The TMS 3404 JC/NC consists of two high-speed 512-bit dynamic shift registers. The bits are implemented by a ratioless two-phase design to minimize power consumption. Inputs and outputs are TTL compatible—without use of external components.

The entire device is constructed on a single monolithic chip using thick-oxide techniques and low-threshold MOS P-channel enhancement-mode transistors.

TMS 3404 JC is the part number for this device mounted in a 16-pin ceramic dual-in-line package. Mounted in a 16-pin plastic package the device is designated TMS 3404 NC.

logic definition

Positive logic is assumed.

a) LOGICAL 1 = most positive voltage

b) LOGICAL 0 = most negative voltage

operation

Data is transferred into the register when the ϕ_1 clock is Low (–12 V). The data must be set up at least 100 nanoseconds before the clock ϕ_1 goes to the high state (+5 V) and held steady at least 20 nanoseconds after ϕ_1 reaches this state.

Output delay time is defined as the time required for the output to reach the DTL or TTL changeover threshold after the ϕ_2 clock reaches 90% of its Low voltage. This time is faster than 100 nanoseconds.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	–20 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	–20 V to 0.3 V
Clock input voltage range (See Note 1)	–20 V to 0.3 V
Data input voltage range (See Note 1)	–20 V to 0.3 V
Operating free-air temperature range	–25°C to 85°C
Storage temperature range	–55°C to 150°C

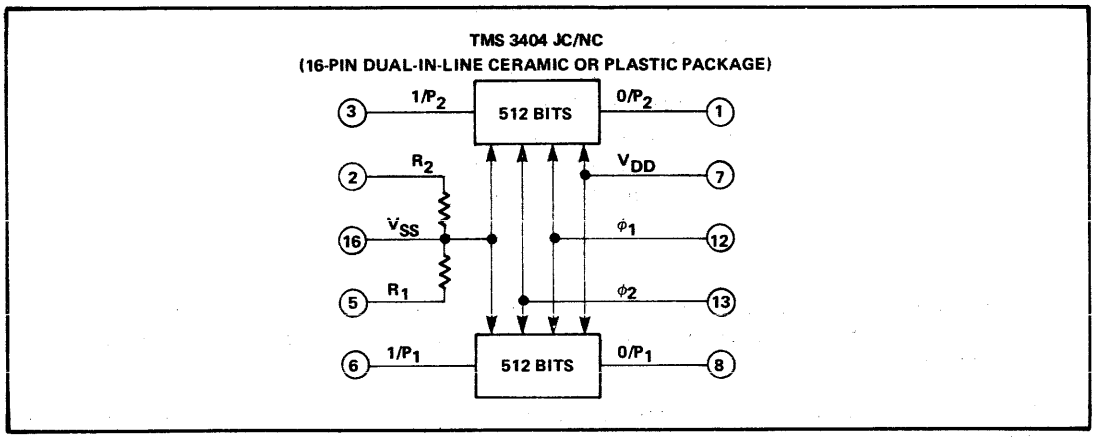
NOTE 1: These voltage values are with respect to V_{SS} (substrate).

14

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TMS 3404 JC, TMS 3404 NC
DUAL 512-BIT DYNAMIC SHIFT REGISTER

functional block diagram and pin configuration



recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate supply V_{SS}	+4.75	+5	+5.25	V
Gate supply V_{GG}	−13	−12	−11	V
Logic Levels				
Input High level V_{IH}	V_{SS} −1.6		V_{SS}	V
Input Low level V_{IL}	V_{SS} −18		V_{SS} −4.2	V
Clock Voltage Levels				
Clock HIGH level $V_{\phi H}$	V_{SS} − 1.0		V_{SS}	V
Clock LOW level $V_{\phi L}$	V_{SS} −19		V_{SS} −16	V
Pulse Timing				
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			1	μs
Clock pulse width $PW_{\phi 1}$	0.080		10	μs
Clock pulse width $PW_{\phi 2}$	0.080		10	μs
Pulse spacing				
Clock delay $t_{d\phi 12}$	0.010		50	μs
Clock delay $t_{d\phi 21}$	0.010		50	μs
Data setup t_{DS}	0.100			μs
Data hold t_{DH}	0.020			μs
Pulse Repetition Rate PRR				
Data	0		5.0	MHz
Clock	.01		5.0	MHz

14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

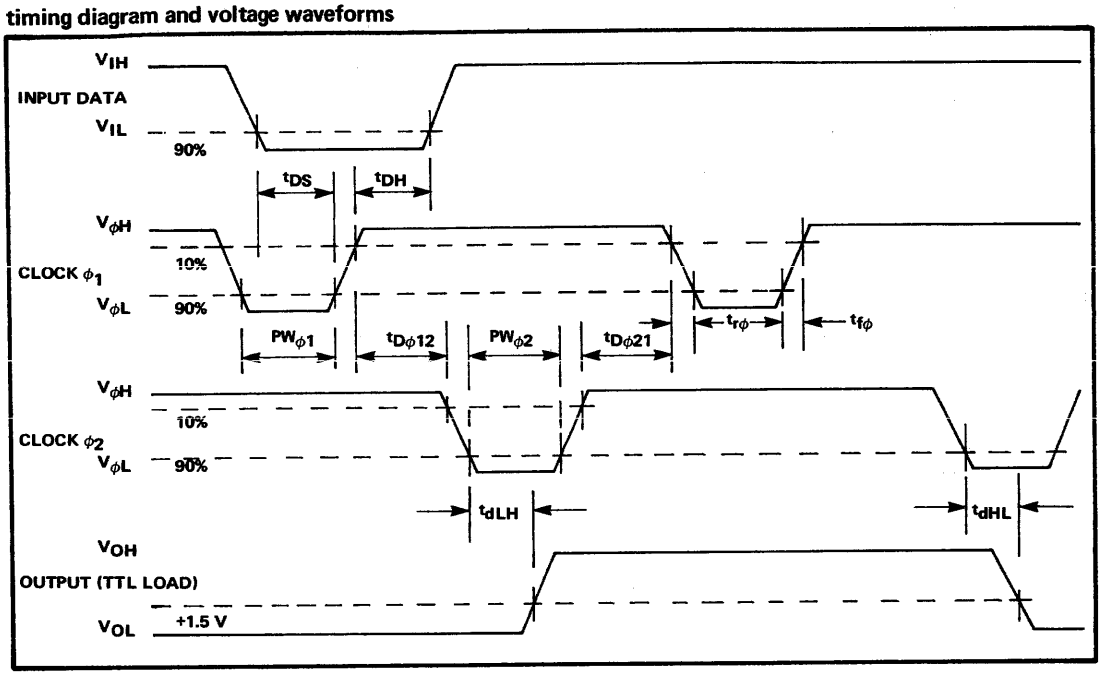
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Current	V_{IN} = −12 V, V_{SS} = +5 V			500	nA
$I_{\phi L}$	Clock Current	V_{ϕ} = −12 V, V_{SS} = +5 V			10	μA
Output Voltage Levels						
V_{OL}	Output LOW level	TTL load	V_{SS} −4.6			V
V_{OH}	Output HIGH level		V_{SS} −1.8		V_{SS}	V
Supply Current Drain						
I_{GG}	Gate supply	V_{SS} = 0 V, V_{GG} = −17 V			3	mA

NOTE 1: Power dissipation (mW) = 80 + 90 × F_{ϕ} (MHz) + 0.5 × [$PW_{\phi 1}$(ns) + $PW_{\phi 2}$(ns)] × F_{ϕ} (MHz).

dynamic electrical characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic Transition						
Time						
t_r	Rise			50		ns
t_f	Fall			50		ns
Output Logic Delay						
t_{DL}	Output Low level	TTL load		100		ns
t_{DH}	Output High level	TTL load		100		ns
Capacitance						
C_{IN}	Input			8		pF
C_{ϕ}	Clock			350		pF

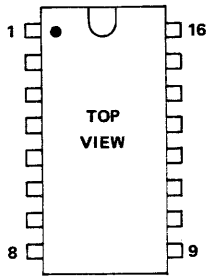
timing diagram and voltage waveforms



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

mechanical data and pin configuration

The device is available in both a 16-pin hermetically sealed ceramic dual-in-line package (TMS 3404 JC) and a 16-pin plastic package (TMS 3404 NC). The packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

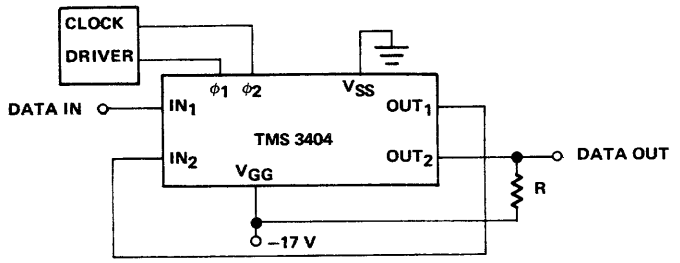


PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Output 2	9	Clock 1
2	NC	10	NC
3	NC	11	NC
4	Input 2	12	NC
5	Input 1	13	NC
6	V_{GG}	14	Clock 2
7	NC	15	NC
8	Output	16	V_{SS}

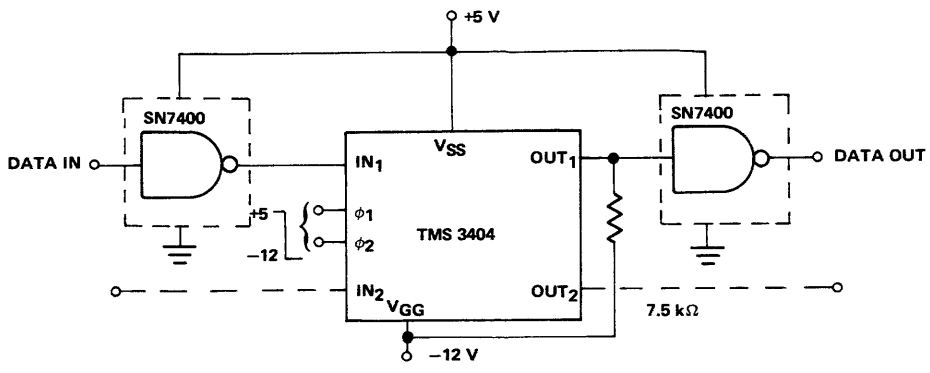
interface circuits

a) MOS

Note: In this figure the TMS 3404 has been connected as a single 1024-bit register to demonstrate MOS interface



b) TTL



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 3406 LR
DUAL 100-BIT DYNAMIC SHIFT REGISTER

JANUARY, 1971

features

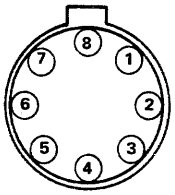
- Low power dissipation – 0.4 mW/bit typical at 1 MHz
  – 1 mW/bit typical at 2 MHz
- High-frequency operation – 2.5 MHz guaranteed
- TTL/DTL compatible
- Single-ended output buffer
- Low-threshold technology

description

The Texas Instruments TMS 3406 LR consists of two separate 100-bit dynamic shift registers with independent input and output terminals. Only one power supply and two clock phases are required for operation. Low-threshold, thick-oxide, MOS P-channel enhancement-mode circuitry has been employed to reduce power dissipation and permit easy interface between the TMS 3406 LR and Bipolar integrated circuits.

mechanical data and pin configuration

The TMS 3406 LR is mounted in a TO-99 package (see MOS/LSI packaging section).



BOTTOM VIEW

LEAD NO.	FUNCTION	LEAD NO.	FUNCTION
1	Input 1	5	Input clock (ϕ_1)
2	Output 1	6	Output 2
3	Input clock (ϕ_2)	7	Input 2
4	V_{SS}	8	V_{DD}

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . –20 V to 0.3 V
Clock voltage V_ϕ (See Note 1) . . . . . –20 V to 0.3 V
Data input voltage ranges (See Note 1) . . . . . –20 V to 0.3 V
Power dissipation . . . . . 600 mW
Operating free-air temperature range . . . . . –55°C to 85°C
Storage temperature range . . . . . –55°C to 150°C

recommended operating conditions (–55°C to 85°C)

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD} (See Note 1)	–9	–10	–12	V
Clock voltage $V_{\phi L}$ (See Note 1) logic 0	–15	–16	–18	V
Clock voltage $V_{\phi H}$ (See Note 1) logic 1	+0.3	–0.5	–1.5	V
Width of clock pulse t_{p1} (See voltage waveforms)	150			ns
Width of clock pulse t_{p2} (See voltage waveforms)	150			ns
Transient time of clock pulse, t_r, t_f (See voltage waveforms)			5	μs
Clock delay time, t_d (See voltage waveforms)	20			ns
Width of data pulse, t_p (See voltage waveforms)	170			ns
Data pulse before clock change t_{p0} (See voltage waveforms)	150			ns
Clock repetition rate	0.01		2.5	MHz

NOTE 1: These are voltage values with respect to most positive supply voltage, V_{SS}.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

logic definition

Positive logic is assumed

a) Logic 1 = most positive (high) voltage

b) Logic 0 = most negative (low) voltage

electrical characteristics (at nominal operating conditions and 25°C)

V_{DD} = −5 V, V_{SS} = +5 V, $V_{\phi H}$ = −11 V, $V_{\phi L}$ = +5 V, and C_L = 10 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{in(1)}$	Logic 1 data input voltage		+3.0	+5	+5.3	V
$V_{in(0)}$	Logic 0 data input voltage		−10	+0.2	+0.8	V
$V_{out(1)}$	Logic 1 output voltage	Load = 3.3 kΩ, t_{p1} = 150 ns	+3.5			V
$V_{out(0)}$	Logic 0 output voltage	Load = 3.3 kΩ, Load = 3.3 kΩ, I_L = 1.6 mA			−3.0 +0.4	V V
R_{out}	Output resistance	Output at logic 0		300	450	Ω
$I_{R(in)}$	Input leakage current	V_{in} = −5 V, T_A = 25°C			0.5	μA
C_{in}	Capacitance of input	V_{in} = +5 V, T_A = 25°C f = 1 MHz		5	7	
$C_{\phi 1,2}$	Capacitance of clock input	V_ϕ = +5 V, T_A = 25°C f = 1 MHz		40	50	
$I_{DD(1)}$	Average supply current (See Note 2)	f = 1 MHz (t_{p1} = 200 ns, t_{p2} = 200 ns) f = 1 MHz (t_{p1} = 150 ns, t_{p2} = 150 ns)		6 4.5	12 10	mA mA
$I_{\phi 1,2}$	Average supply current for clock mode	f = 1 MHz (t_{p1} = t_{p2} = 200 ns) f = 1 MHz (t_{p1} = t_{p2} = 150 ns)		0.5 0.4	1.5 1.2	mA mA

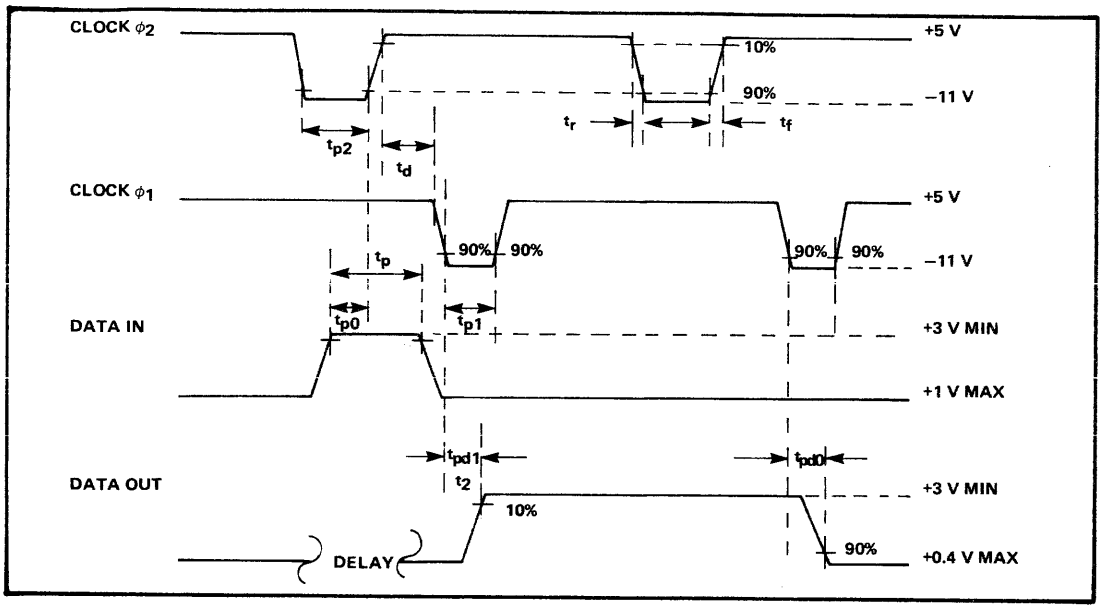
NOTE 2: These values do not include the current flowing through the load resistor.

switching characteristics

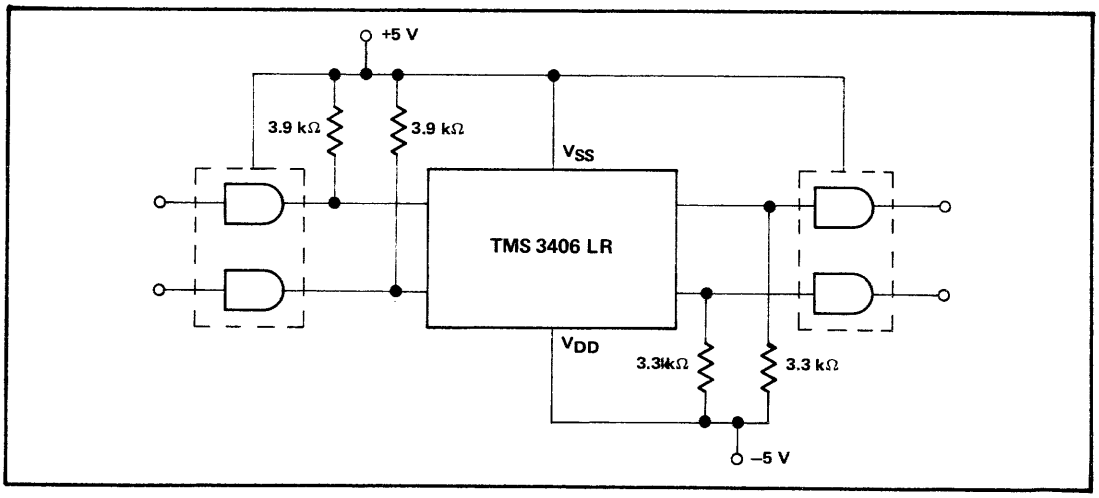
V_{DD} = −5 V, V_{SS} = +5 V, $V_{\phi H}$ = −11 V, $V_{\phi L}$ = +5 V, and C_L = 10 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Propagation delay time to logical 1 level from clock ϕ_1 to data output	See Voltage Waveforms Load = 3.3 kΩ		100	150	ns
t_{pd0}	Propagation delay time to logical 0 level from clock ϕ_1 to data output	See Voltage Waveforms Load = 3.3 kΩ		120	180	ns

timing diagram



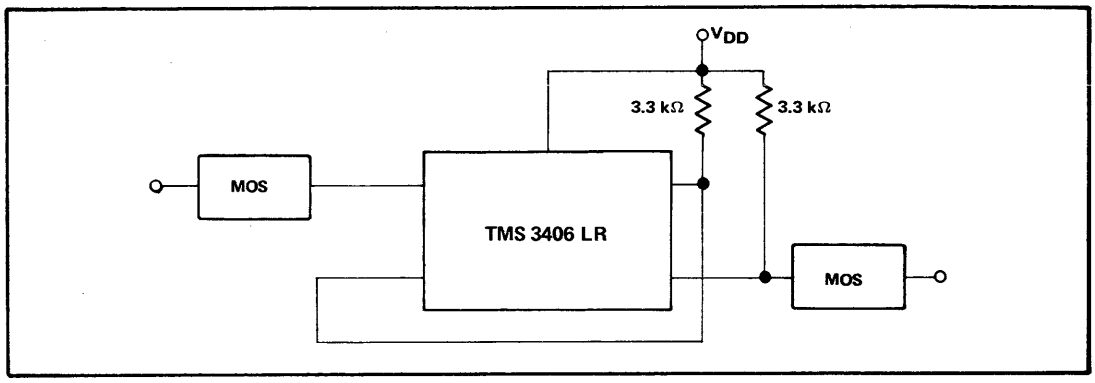
TTL interface



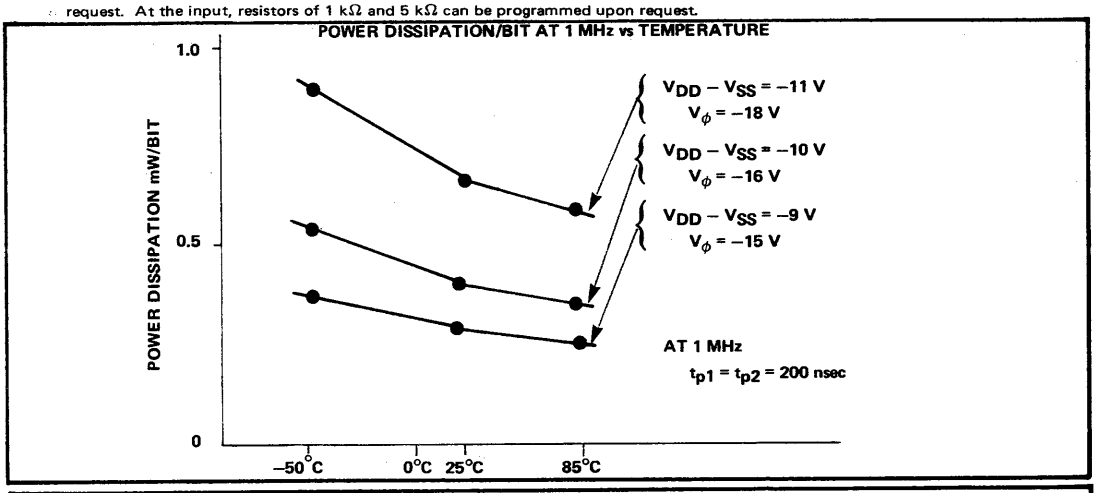
14

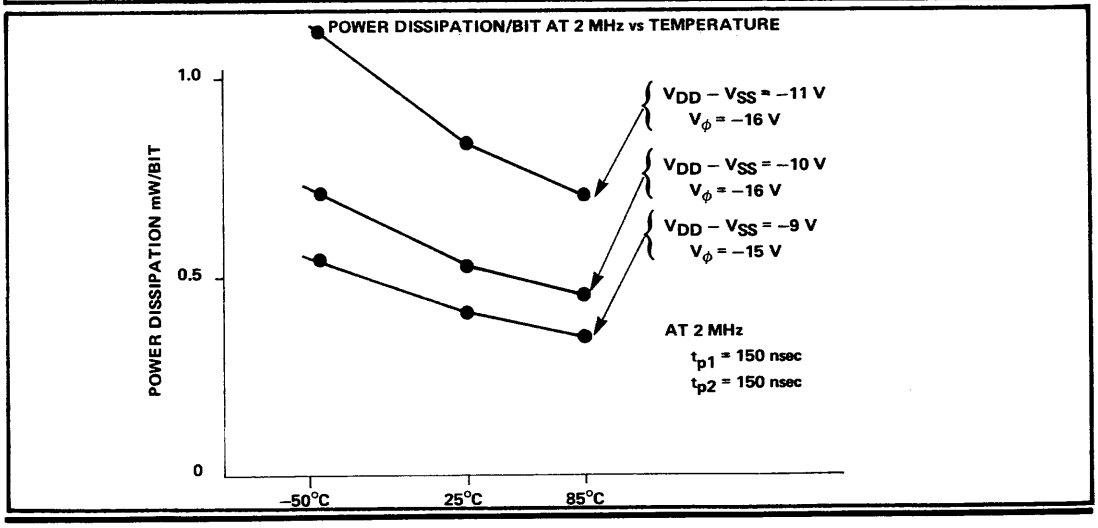
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS interface



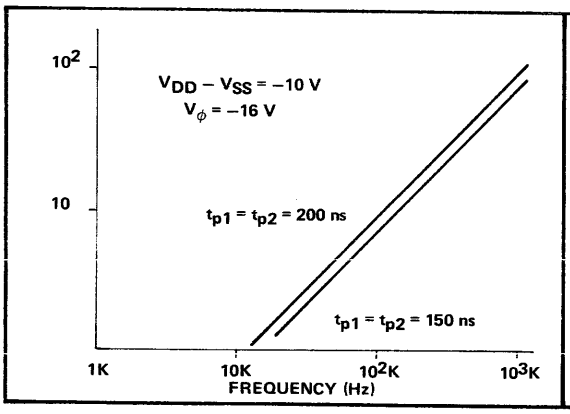
NOTE: The TMS 3406 LR features an open-ended buffer; however, load resistors of 3.3 kΩ and 20 kΩ can be programmed on the chip, upon request. At the input, resistors of 1 kΩ and 5 kΩ can be programmed upon request.



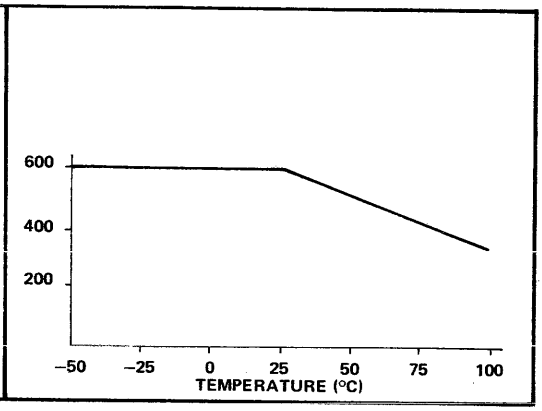


TMS 3406 LR
DUAL 100-BIT DYNAMIC SHIFT REGISTER

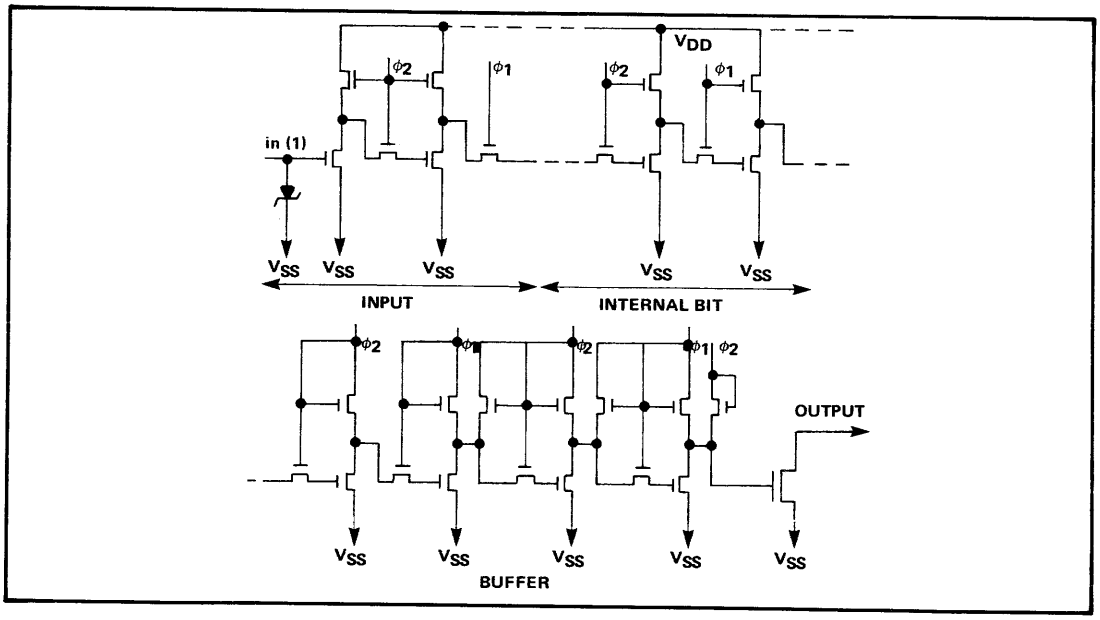
POWER DISSIPATION vs FREQUENCY



PACKAGE POWER DISSIPATION vs TEMPERATURE



SCHEMATIC OF TMS 3406 LR INTERNAL ORGANIZATION



14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS
LSI

TMC 3409 JC, TMC 3409 NC
QUADRUPLE 80-BIT DYNAMIC SHIFT REGISTER

FEBRUARY, 1971

features

- 2.5-MHz shift rate
- Recirculate logic
- Power supplies – +5 V, 0 V, –12 V
- All inputs TTL compatible
- Single TTL compatible clock
- TTL compatible outputs
- Low power – 300 mW
- Low-threshold technology
- Dual-in-line package

description

The TMC 3409 JC/NC consists of four 80-bit shift registers with separately controlled logic for recirculating data in each register. A single-clock generator provides two clock phases to all four registers. Data, recirculate-control and clock inputs are all TTL compatible. Each output interfaces directly with TTL without the use of external components.

Low-threshold, thick-oxide MOS P-channel enhancement-mode circuitry has been employed to reduce power dissipation and permit easy interface between the TMC 3409 JC/NC and bipolar integrated circuits.

"TMC 3409 JC" is the part number for a unit mounted in a 16-pin hermetically sealed ceramic dual-in-line package. A unit mounted in a 16-pin plastic package is designated "TMC 3409 NC".

logic definition

Positive logic is assumed.

a) Logical 1 = most positive voltage (High)

b) Logical 0 = most negative voltage (Low)

operation

Data is transferred into the register when the internal clock ϕ_1 is on. The internal clock is on when the external clock input is high, but the changes of level occur some 100 nanoseconds behind the external drive. To be entered, data must be held true at least 100 nanoseconds after the external clock drive has changed state.

True output data becomes available about 100 nanoseconds after the TTL clock goes to Low.

Information in the register during the recirculate mode continues to be read out.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	–20 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	–20 V to 0.3 V
Clock input voltage range (See Note 1)	–20 V to 0.3 V
Data input voltage range (See Note 1)	–20 V to 0.3 V
Operating free-air temperature range	–25°C to 85°C
Storage temperature range	–55°C to 150°C

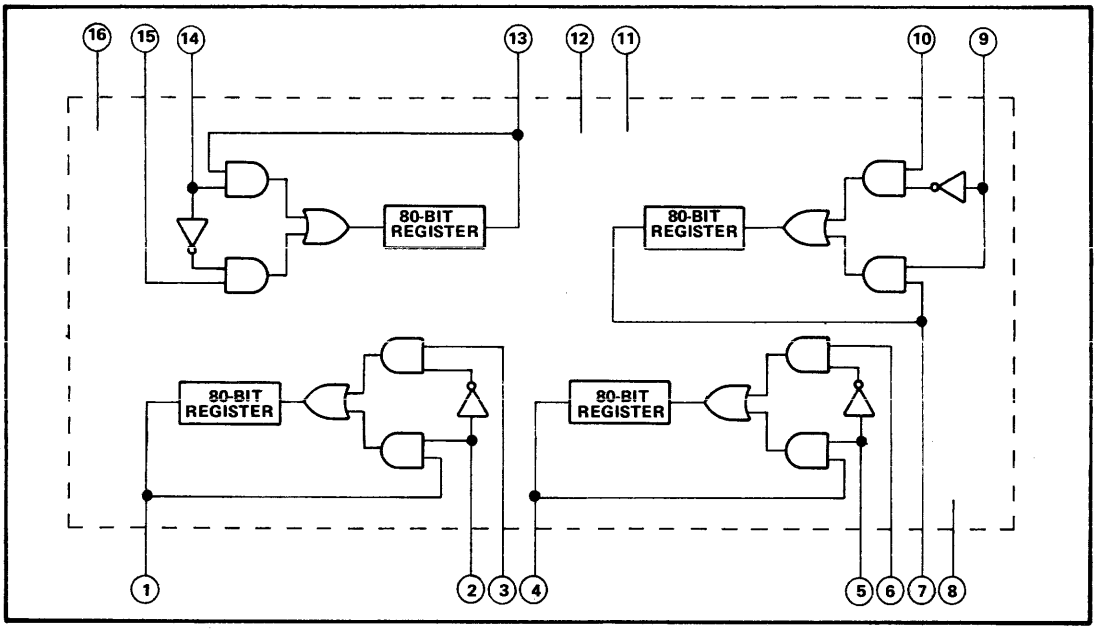
NOTE 1: These voltage values are with respect to V_{SS} (substrate).

14

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TMC 3409 JC, TMC 3409 NC
QUADRUPLE 80-BIT DYNAMIC SHIFT REGISTER

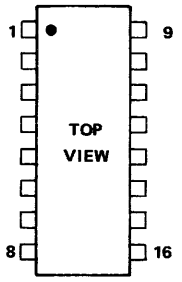
functional block diagram



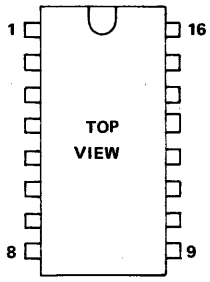
pin configuration

This device is available in both a 16-pin hermetically sealed ceramic dual-in-line package (TMC 3409 JC) and a 16-pin plastic package (TMC 3409 NC).

The package for TMC 3409 JC is designed for insertion in mounting-hole rows on 0.300-inch centers. For the TMC 3409 NC the package is designed for mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)



TMS 3409 JC



TMS 3409 NC

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Data Out A	9	Recirc Enable C
2	Recirc Enable A	10	Input C
3	Input A	11	Clock
4	Data Out A	12	V_{GG}
5	Recirc Enable B	13	Data Out D
6	Input B	14	Recirc Enable D
7	Data Out C	15	Input D
8	V_{CC}	16	V_{SS}

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate Supply V_{SS}	+4.75	+5.0	+5.25	V
Drain supply V_{DD}	0	0	0	V
Gate supply V_{GG}	−13	−12	−11	V
Logic Levels				
Input High level V_{IH}	V_{SS} −2.0		V_{SS}	V
Input Low level V_{IL}	−13		+0.8	V
Clock Voltage Levels				
Clock High level $V_{\phi H}$	V_{SS} −2.0		V_{SS}	V
Clock Low level $V_{\phi L}$	−13		+0.8	V
Pulse Timing				
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$		10	100	ns
Clock pulse width High $PW_{\phi H}$	150		50000	ns
Clock pulse width Low $PW_{\phi L}$	150		50000	ns
$PW_{\phi H} \div PW_{\phi L}$	.02		50	
Pulse Spacing				
Data setup t_{DS}	100			ns
Data hold t_{DH}	100			ns
Recirculate Enable setup t_{RS}	200			ns
Recirculate Enable hold t_{RH}	100			ns
Pulse Repetition Rate PRR				
Data f_D	0		2.5	MHz
Clock f_ϕ	.01		2.5	MHz

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

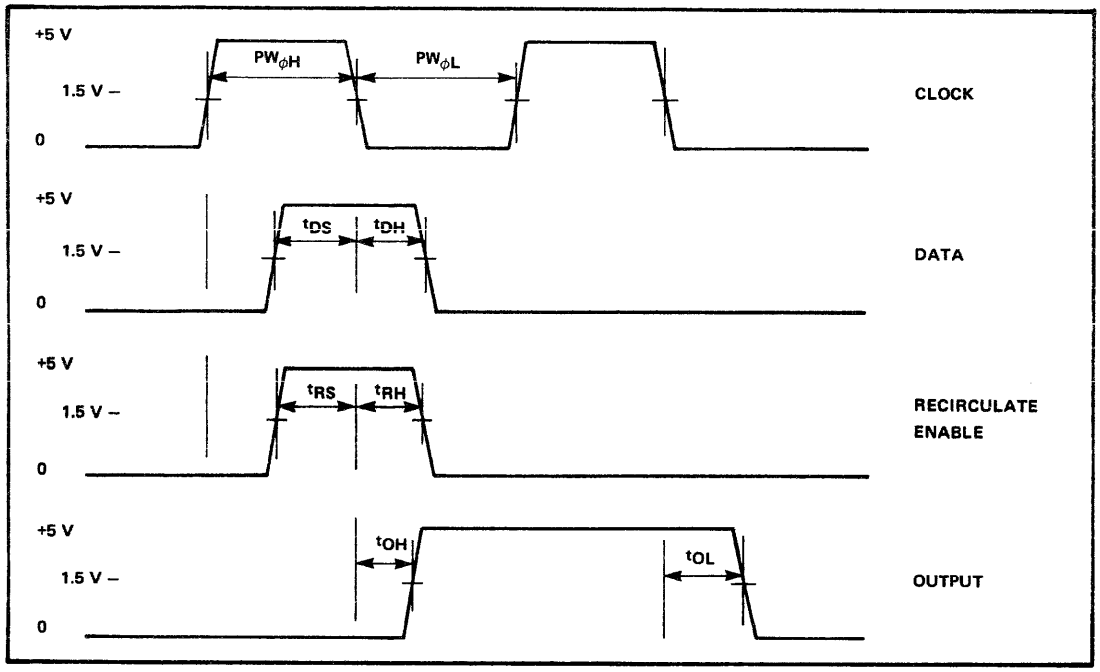
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Current	V_{IN} = 0			100	nA
$I_{\phi L}$	Clock Current	V_ϕ = 0			100	nA
Output Voltage Levels						
V_{OL}	Output Low level	I_{SINK} = 1.6 mA		0.3	0.4	V
V_{OH}	Output High level	I_{LOAD} = 0.5 mA	V_{SS} −1.0	V_{SS} −0.5	V_{SS}	V
Power Supply Current Drain						
I_{SS}	Substrate supply	25°C		25	30	mA
I_{DD}	Drain supply	25°C		15		mA
I_{GG}	Gate supply	25°C		10	12	mA
P_D	Power Dissipation	25°C		250	300	mW

dynamic electrical characteristics

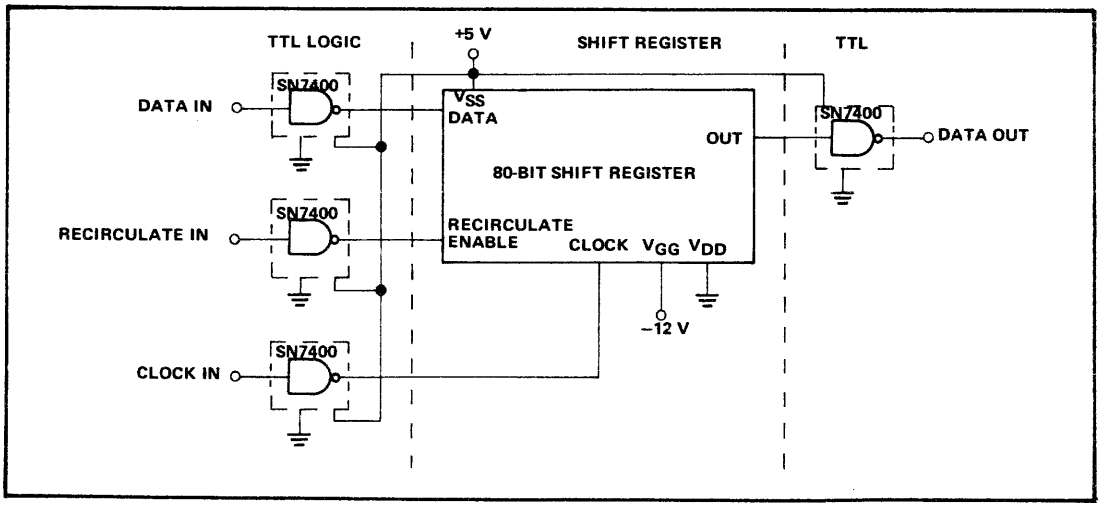
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic Transition Time						
t_r	Rise			30	50	ns
t_f	Fall			30	50	ns
Output Logic Delay						
t_{OL}	Output Low level			100	150	ns
t_{OH}	Output High level			100	150	ns
Capacitance						
C_{IN}	Input (Data and Recirc Enable)	V_{IN} = V_{SS}			10	pF
C_ϕ	Clock	V_ϕ = V_{SS}			25	pF

14

timing diagram and voltage waveforms



TTL interface



14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS
LSI

TMS 3412 JC, NC; TMS 3413 LC, NC; TMS 3414 LC, NC
1024-BIT DYNAMIC SHIFT REGISTER

FEBRUARY 1971

features

- 0.01-MHz to 6-MHz operation
- Low power dissipation
- Open-drain output buffer
- DTL, TTL compatible
- Low clock capacitance (70 pF typ)
- Low-threshold silicon-gate multilevel technology
- 4 x 256 bits TMS 3412
- 2 x 512 bits TMS 3413
- 1 x 1024 bits TMS 3414
- Dual-in-line or plug-in package

description

The circuits TMS 3412 JC/NC, TMS 3413 LC/NC and TMS 3414 LC/NC are a family of two-phase dynamic shift registers. Each device is constructed on a single monolithic chip by use of silicon-gate technology and P-channel enhancement-mode transistors. Input and output terminals in the multiple register circuits are independent; clocks and power are common. Internal multiplexing results in a data shift rate twice the clock rate. Each clock pulse on the phase-1 or phase-2 line shifts the data one bit.

A unit mounted in a 16-pin hermetically sealed ceramic dual-in-line package is designated "JC". "LC" is the designation for a device mounted in an 8-lead TO-99 package. A unit mounted in a 16-pin dual-in-line plastic package is designated "NC".

logic definition

Positive logic is assumed.

a) Logical 1 = most positive voltage

b) Logical 0 = most negative voltage

operation

Two clock pulses are required for operation of the registers. The pulses should not be at low level simultaneously or data errors will occur.

Data is transferred into the register when the clock pulse, phase 1 or phase 2, is at the low level. Output data appears after the high-to-low transition of the clock pulse, phase 1 or phase 2.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

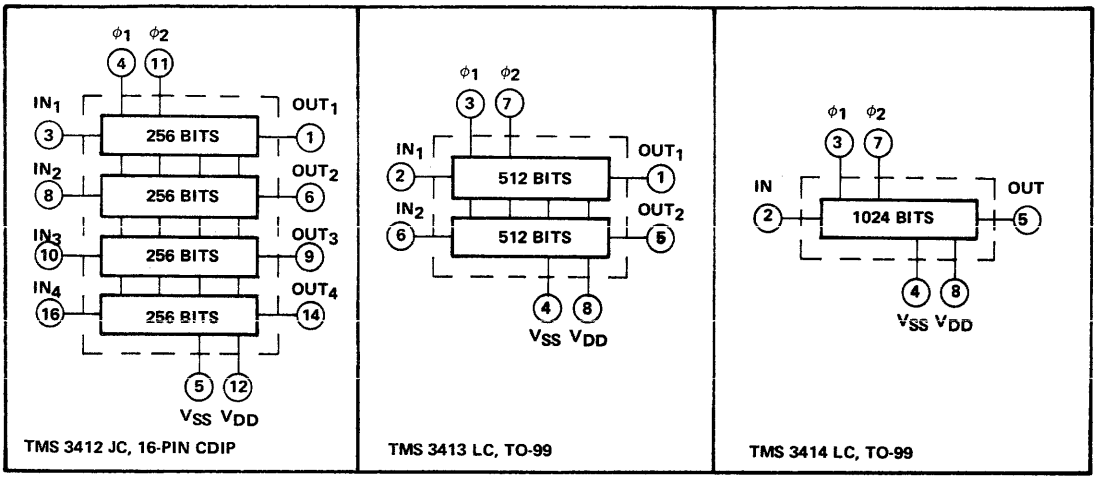
Supply voltage V_{DD} range (See Note 1)	−20 V to 0.3 V
Clock input voltage range (See Note 1)	−20 V to 0.3 V
Data input voltage range (See Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

14

TMS 3412 JC, NC; TMS 3413 LC, NC; TMS 3414 LC, NC
1024-BIT DYNAMIC SHIFT REGISTER

functional block diagram



recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNITS
Operating Voltage					
Substrate supply V_{SS}	V_{DD} = −5 V ± 5%	+4.75	5	5.25	V
Drain supply V_{DD}	V_{SS} = +5 V ± 5%	−4.75	−5	−5.25	V
Logic Levels					
Input High level V_{IH}		V_{SS}−1.7		V_{SS}+0.3	V
Input Low level V_{IL}		V_{SS}−4.2		V_{SS}−10	V
Clock Voltage Levels					
Clock High level $V_{\phi H}$		V_{SS}−1.0		V_{SS}+0.3	V
Clock Low level $V_{\phi L}$		V_{SS}−15.0		V_{SS}−17.0	V
Pulse Timing					
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$				1000	ns
Clock pulse width 1 $PW_{\phi 1}$		100			ns
Clock pulse width 2 $PW_{\phi 2}$		100			ns
Pulse spacing					
Clock delay $t_{D\phi 12}$	$PW_{\phi 1}$ = $PW_{\phi 2}$ = 100 ns	40			ns
Clock delay $t_{D\phi 21}$	$PW_{\phi 1}$ = $PW_{\phi 2}$ = 100 ns	40			ns
Data setup t_{DS}		40			ns
Data hold t_{DH}		40			ns
Pulse Repetition Rate PRR					
Data				6	MHz
Clock				3	MHz

14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Input Current	V_{IN} = −5 V,	V_{SS} = +5 V			500	nA
$I_{\phi L}$	Clock Current	V_{ϕ} = −10 V,	V_{SS} = +5 V			1000	nA
Output Voltage Levels							
V_{OL}	Output Low level	R_L = 3 kΩ, V_{SS} = +5 V	I_L = 1.6 mA,			0.5	V
V_{OH}	Output High level	Driving TTL, V_{SS} = 4.75 V	R_L = 3 kΩ,	2.5			V
Power Supply Current Drain							
I_{DD}	Drain supply	V_{SS} = +5 V, V_{ϕ} = −12 V	V_{DD} = −5 V,		35	50	mA
P_D	Power Dissipation	5-MHz Data Rate,	35% Duty Cycle			600	mW

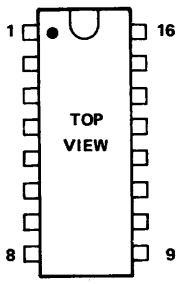
dynamic electrical characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic Delay						
t_{DLH1}	Output Low level	1 TTL load (See Note 2)			80	ns
t_{DHL1}	Output High level	1 TTL load (See Note 2)			80	ns
Output Logic Delay						
t_{DLH2}	Output Low level	MOS load (See Note 3)			80	ns
t_{DHL2}	Output High level	MOS load (See Note 3)			80	ns
Capacitance						
C_{IN}	Input	(See Note 4)	2.5		5	pF
C_{ϕ}	Clock		60	70	80	pF

NOTES: 2. V_{SS} = +5 V ± 5%, V_{DD} = −5 V ± 5%, $V_{\phi L}$ = −10 V
3. V_{SS} = 0 V, V_{DD} = −10 V ± 10%, $V_{\phi L}$ = −15 V
4. 16-pin CDIP – C_{IN} min, 7 pF; C_{IN} max, 8 pF

mechanical data and pin configuration

The TMS 3412 is available in both a 16-pin hermetically sealed ceramic dual-in-line package (JC) and a 16-pin plastic package (NC). The packages are designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)



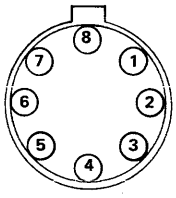
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	OUT_1	9	OUT_3
2	NC	10	IN_3
3	IN_1	11	ϕ_2
4	ϕ_1	12	V_{DD}
5	V_{CC} (V_{SS})	13	NC
6	OUT_2	14	OUT_4
7	NC	15	NC
8	IN_2	16	IN_4

14

– continued

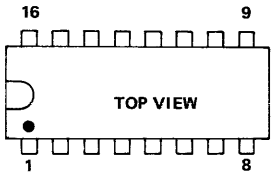
mechanical data and pin configuration (continued)

The TMS 3413 and TMS 3414 are available both in 8-lead TO-99 packages (LC) and in 16-pin dual-in-line plastic packages (NC) designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)



BOTTOM VIEW

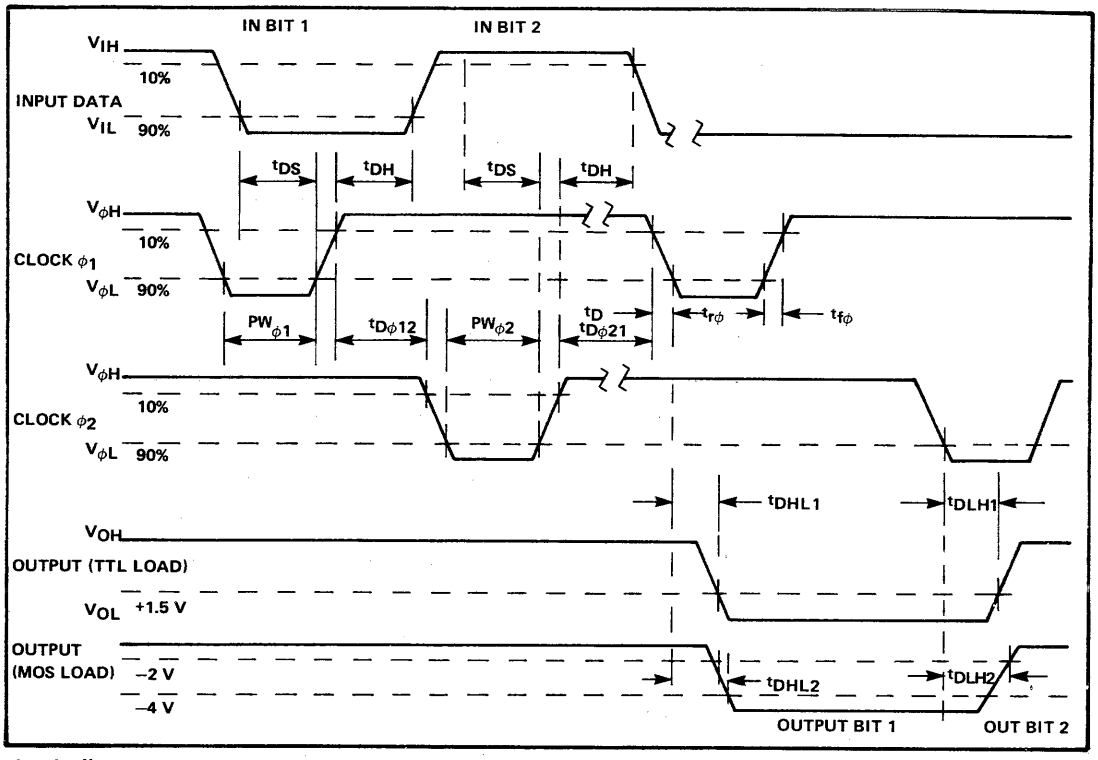
TMS 3413 LC		TMS 3414 LC	
LEAD NO.	FUNCTION	LEAD NO.	FUNCTION
1	Output 1	1	NC
2	Input 1	2	Input
3	ϕ_1	3	ϕ_1
4	V_{CC} (V_{SS})	4	V_{CC} (V_{SS})
5	Output 2	5	Output
6	Input 2	6	NC
7	ϕ_2	7	ϕ_2
8	V_{DD}	8	V_{DD}



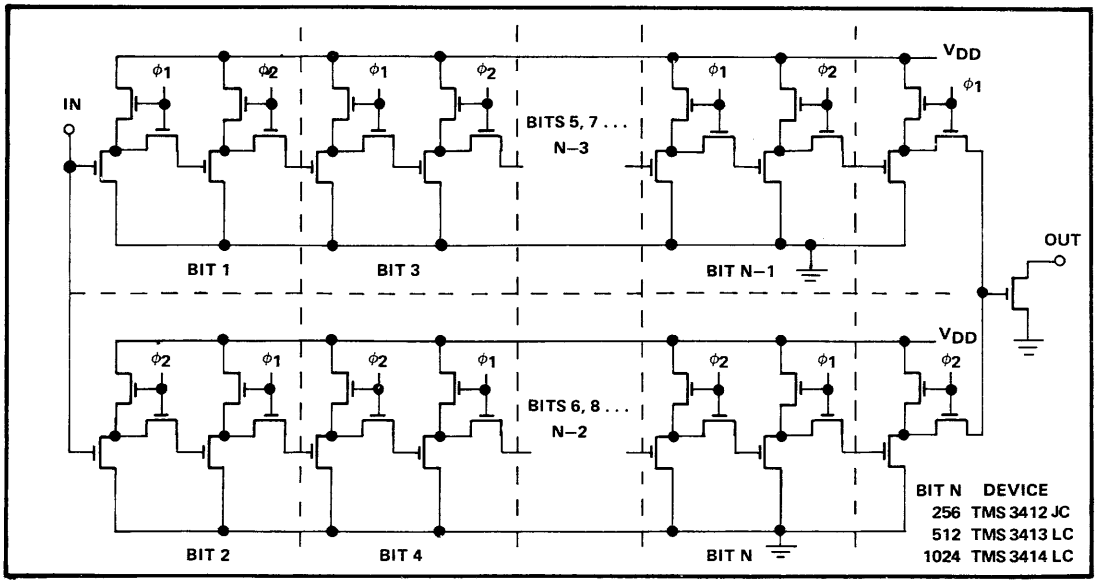
TMS 3413 NC		TMS 3414 NC	
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	NC	1	NC
2	NC	2	NC
3	Input 1	3	Input
4	ϕ_1	4	ϕ_1
5	V_{SS}	5	V_{SS}
6	Output 2	6	Output
7	NC	7	NC
8	NC	8	NC
9	NC	9	NC
10	Input 2	10	NC
11	ϕ_2	11	ϕ_2
12	V_{DD}	12	V_{DD}
13	NC	13	NC
14	Output 1	14	NC
15	NC	15	NC
16	NC	16	NC

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

timing diagram and voltage waveforms



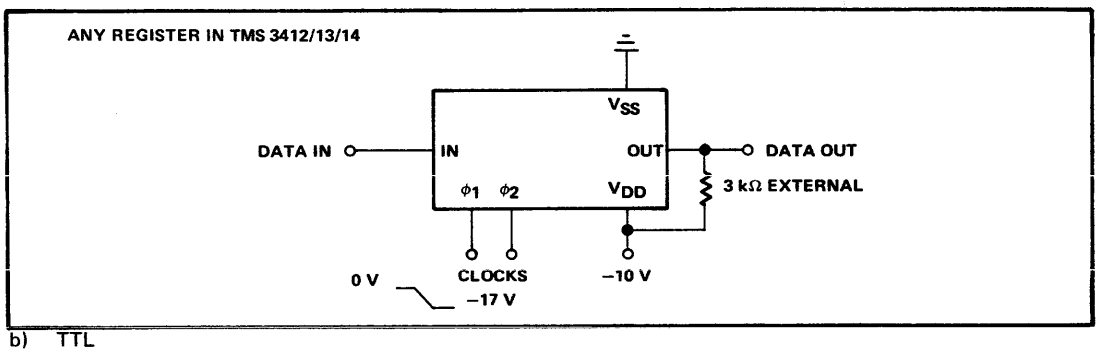
circuit diagram



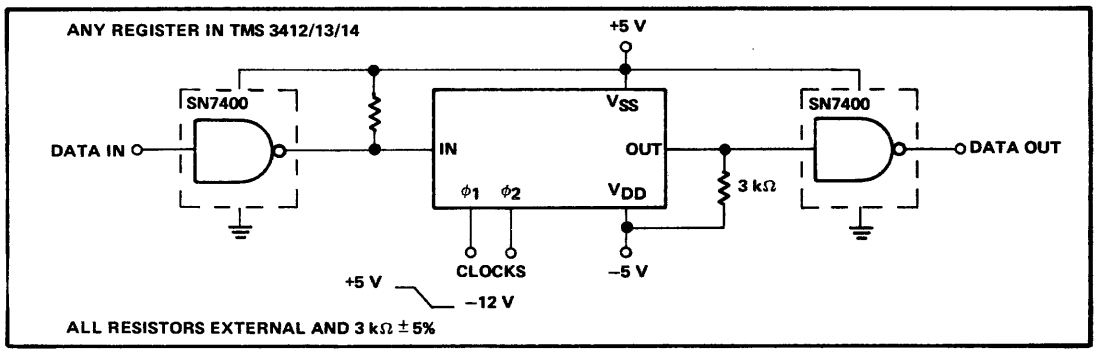
14

interface circuits

a) MOS



b) TTL



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

1) Introduction

The information stored in a Read-Only Memory (ROM) is permanently programmed into the circuit at the time of its manufacture. Once the information is entered it cannot be changed – it can, however, be read out as often as desired. Before MOS circuits became available, the only practical means of realizing a ROM were with discrete-diode matrices, or core memories. The most obvious advantages of MOS ROMs are:

Cost – MOS typically one tenth that of diode matrix

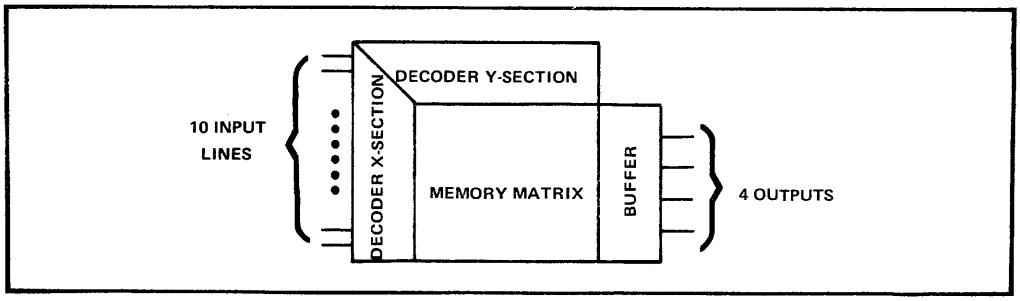
Size – MOS can put 4096 bits in a 24-pin package (chip size is 120 X 110 mil)

Speed – New MOS techniques can provide access times as low as 50 nsec.

2) Structure of an MOS ROM

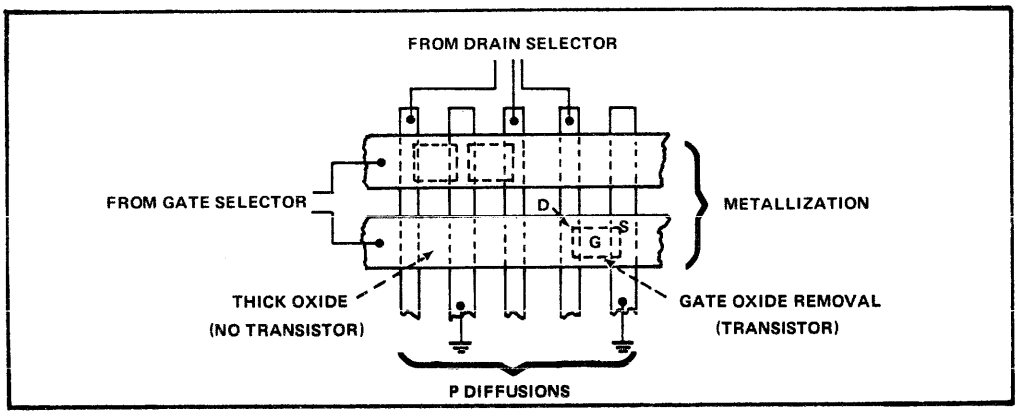
A single MOS ROM device will be made up of three sections:

- DECODER — in which the binary address is decoded and X-Y pairs of lines going to the memory matrix are enabled (one pair of X-Y lines if there is one bit per output word; two pairs of X-Y lines if there are two bits per output word, etc.)
- MEMORY MATRIX — containing as many MOS-transistor locations as there are bits in the memory.
- BUFFER — which supplies output levels for the external circuitry.



EXAMPLE 1024 x 4 ROM

Consider for example a 4096-bit ROM organized as 1024 words of 4 bits. At the intersection of every X-line and Y-line, an MOS transistor can be either constructed or omitted by growing either a thin-gate oxide or a thick-gate oxide. The absence of an MOS transistor will be interpreted by the buffer as a logic 0, and the presence of a thin-gate MOS transistor will be interpreted as a logic 1. The programming of the memory (placement of the thin-gate oxide transistors) is performed during the manufacturing process.



3) Static or Dynamic?

Aside from the organization of the ROM, which defines its bit capacity, the most important parameter in most applications is probably access time. Access time is defined as the time required for a valid output to appear after a valid input has been applied.

In a static ROM there are no clocks required. If a valid input address is applied to the memory, after the expiration of the required access time, a valid output will appear. The output will remain valid as long as the input address remains unchanged. The use of static read-only memories is very straightforward and TI has developed a complete line.

In a conventional dynamic read-only memory, the information is clocked in and clocked out. The output will only remain valid for a certain period. Dynamic read-only memories are advantageous to implementing synchronous logic. To take advantage of their logic flexibility and to allow the output to be kept valid as long as desired, TI has designed in latches on the outputs of all dynamic ROMs presently in production. TI's dynamic ROMs do not require clock drivers since these have been incorporated on the chip.

4) Typical Applications

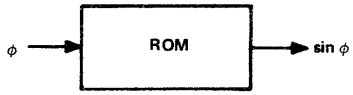
Now that economical ROMs are available, the logic designer is taking advantage of this element. The most common areas of applications are found in:

- DISPLAYS
- COMPUTERS
- COMPUTER TERMINALS
- CALCULATORS

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

The most common applications are:

a) LOOK-UP TABLES – where the output is a mathematical function of the input. In computers for military applications, trigonometric functions are commonly used. A ROM can be used to obtain the sine of an angle instead of having to compute it by algorithm.

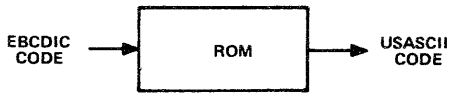


ROM as Trigonometric Look-Up Table

Some calculators also employ Look-up tables in performing arithmetic:

ROM as Arithmetic Look-Up Table

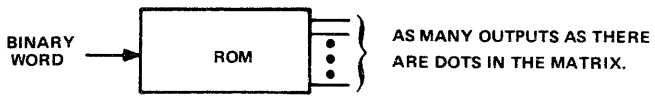
b) CODE CONVERSION – many applications require translating between one code and another. This is a common requirement of display manufacturers, computer terminal equipment manufacturers, and persons involved with punched card reading and processing. For example, a ROM can be designed to accept input words in EBCDIC code and convert to words of USASCII code at the output.



ROM Used for Code Conversion

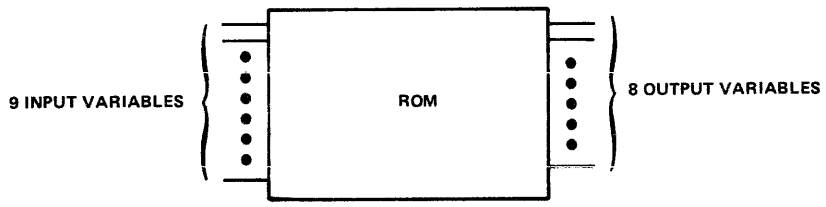
c) MICROPROGRAMMING – where a routine can be programmed directly (hard-wired programs), instead of being described (microprogram) on a stack of punched cards and then stored in the main memory. This technique is becoming more and more popular in medium-sized computers.

d) CHARACTER GENERATOR – where an alphanumeric character is represented by a binary word. The characters can be visually represented by use of nixie tubes, a dot matrix, or a segment display. An example of a ROM used as a dot-matrix character generator is shown below.



ROM Used as Character Generator

e) RANDOM LOGIC – ROMs can also be utilized to perform Boolean algebra. For example, a 4096-bit ROM organized as 512 words of 8 bits, has 9 inputs and 8 outputs. The ROM can be programmed to provide the outputs (which are Boolean functions of the input variables). The user needs only to develop the truth table for the desired logic function.



ROM USED IN PERFORMING RANDOM LOGIC

$$0_1 = f_1 (A, B, C, \ldots)$$

$$0_2 = f_2 (A, B, C, \ldots)$$

To perform sequential logic the outputs would be fed back to the inputs.

5) TI ROMS

a) General Purpose Static ROMs

TMS 2800 JC/NC	1024-bit capacity	256 X 4 organization
TMS 2600 JC/NC	2048-bit capacity	512 X 4 or 256 X 8 organization
TMS 2700 JC/NC	3072-bit capacity	256 X 12 organization
TMS 4400 JC/NC	4096-bit capacity	1024 X 4 or 512 X 8 organization

b) General Purpose Dynamic ROM

TMS 2300 JC/NC	2560-bit capacity	256 X 10 organization

c) Static character Generators (5 X 7 dot matrix)

TMS 2400 JC/NC	64 characters row output
TMS 4100 JC/NC	64 characters column output

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

For each series of devices TI has programmed at least one off-the-shelf device. This device can be used for evaluation by customers. For instance, in the TMS 2400 JC series the TMS 2403 JC is an off-the-shelf ASCII row-output character generator and the TMS 2404 JC is an off-the-shelf EBCDIC character generator.

CUSTOM BIT PATTERNS

The programming of a single photomask permits the user to choose:

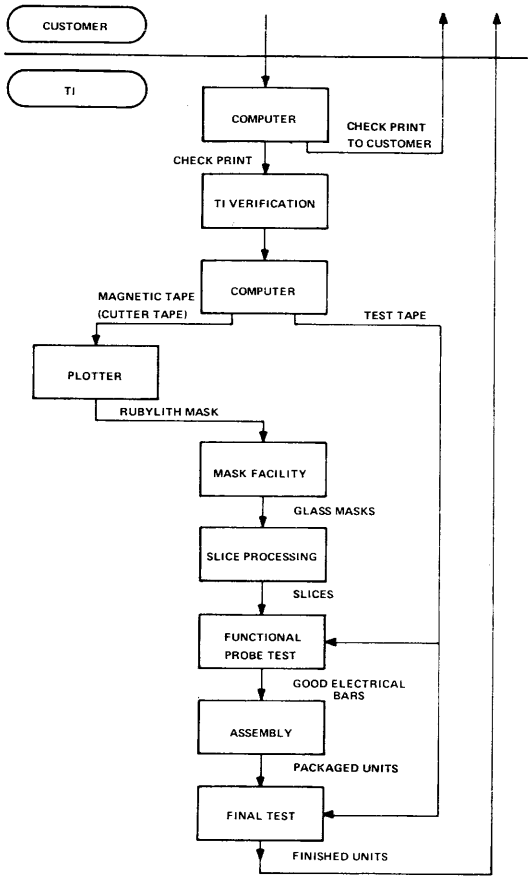
- Organization of the read-only memory
- Programming of the decode section
- Memory content
- Buffer configuration
- Chip-enable polarities

All other masks used during the processing are fixed and are common to a series of devices. For instance, all devices of the TMS 2600 JC series (2048-bit static ROM) use the same masks except for the gate-oxide-removal mask, which contains the custom pattern.

TI uses computer methods to assure a quick and foolproof implementation of a custom bit pattern. This also reduces the cost of the implementation. A "SOFTWARE PACKAGE" bulletin is used to transmit the customer inputs to TI, for each series of devices, these packages are available from the TI Sales Office. The Software Package describes the format in which the inputs should be transmitted for best interface with the computer. For character generators the Software Package includes grid on which the customer can map the desired outputs. For read-only memories the Software Package describes the format used for writing the truth table of the ROM on punched cards. Once the Software Package is received by TI, it can be directly fed into a computer, or punched cards can be prepared from it and the cards can be fed into the computer.

The first computer output is a checkprint. For a read-only memory the checkprint is a reconstitution of the truth table. In the case of a character generator, an overlay is produced. The overlay is in the same scale as the map included in the Software Package and permits easy verification of the punched cards. The checkprint is used for TI verification and a copy is sent to the customer.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222



Once the verification has been performed, the computer generates a magnetic tape that will be used to drive a plotter, and a testing tape to be used for probe test and at final test.

The magnetic tape (cutter tape) is used to drive a plotter which cuts a film of rubylith mask. The rubylith mask, when pealed, is an enlargement of the gate-oxide-removal mask, which is used to store the custom bit pattern. A glass mask is then made from the rubylith by a photographic process (reduction, step and repeat). This mask is used in production of the slice.

A slice contains many individual chips. Each chip is individually tested on a probe tester which uses the test tape generated by the computer.

The chips are packaged and the completed units are final tested (logic and parametric tests). Finished units are then delivered to the customer.

TMS 2300 JC, TMS 2300 NC
2560-BIT DYNAMIC READ-ONLY MEMORY

FEBRUARY, 1971

features

- **2560-bit capacity (256 x 10)**
- **Dynamic operation and static storage**
- **Maximum access time — 550 ns**
- **Maximum cycle time — 550 ns**
- **Full TTL/DTL compatible without external components**
- **TTL-level single clock**
- **Push-pull output buffers**
- **24- or 28-pin CDIP or plastic package**
- **Chip enable**

description

The TMS 2300 JC/NC series is a family of dynamic read-only memories, each having a capacity of 2560 bits.

Programming the memory contents is accomplished by changing a single mask during device fabrication. The memory contents consist of 256 words of 10 bits.

A chip enable input is available.

A single clock pulse line is required (TTL level).

Low-threshold, thick-oxide, MOS P-channel enhancement-mode circuitry has been employed to reduce power dissipation and permit easy interface between the TMS 2300 JC/NC and bipolar integrated circuits (no external pull-up resistors required).

"TMS 2300 JC" designates a unit mounted in a hermetically sealed ceramic dual-in-line package. A unit mounted in a dual-in-line plastic package is numbered "TMS 2300 NC".

logic definition

a) LOGICAL 1 = most positive voltage

b) LOGICAL 0 = most negative voltage

operation

The TMS 2300 JC/NC features dynamic operation; the output data is synchronized by an externally provided clock pulse.

By means of a dc output storage register, this device also performs a static operation; the output data will remain valid as long as a new clock pulse is not provided (even if the input address has changed in the meantime).

Access time is defined as the time between a change of data on any address input and the change of data on the output of the device.

Cycle time is defined as the period of the clock. The minimum cycle time corresponds to the minimum time interval between two address signals.

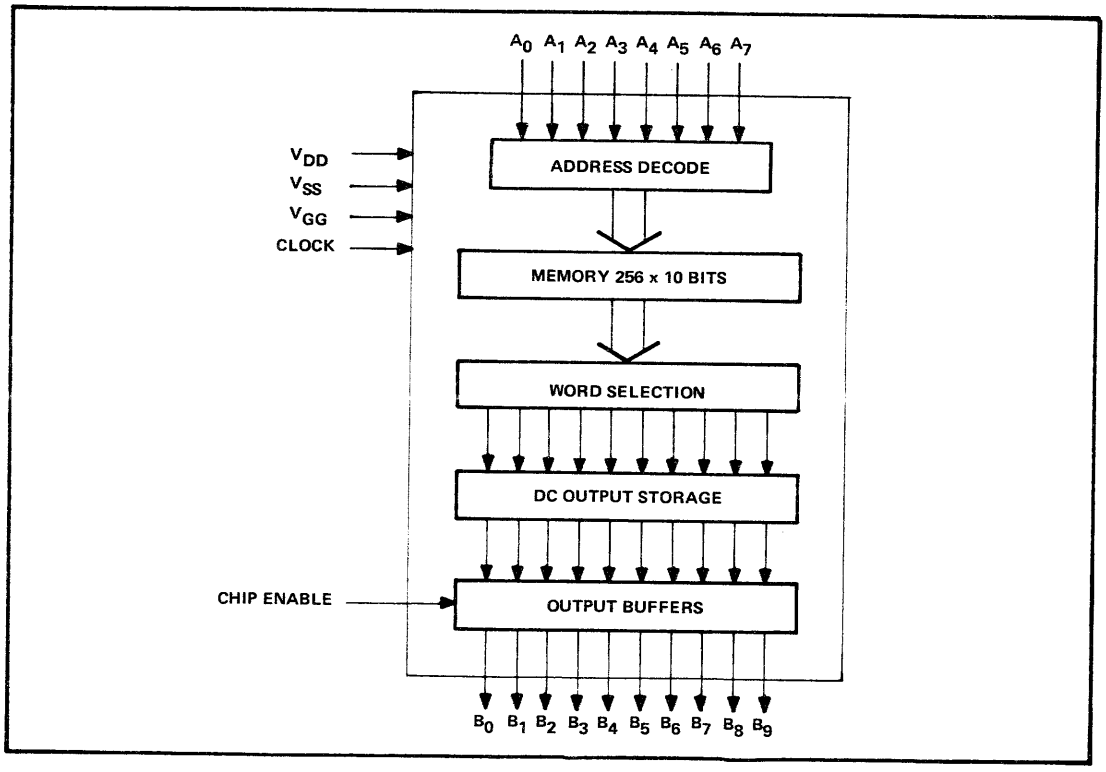
— continued

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operation (continued)

A logical 0 on the Chip-Enable input will cause the outputs to become open-circuits. The number of words per output is increased by hardwiring together the outputs of different devices. The internal operation of the device is not inhibited by the 0 state of Chip-Enable; any change of the address inputs results in the selection of a new 10-bit word, which is then transferred into the dc output register by the next clock pulse. The data outputs are up-dated as soon as the Chip-Enable signal goes back to logical 1.

functional block diagram and pin breakout



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−20 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−20 V to 0.3 V
Clock input voltage range (See Note 1)	−20 V to 0.3 V
Data input voltage range (See Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to +85°C
Storage temperature range	−55°C to +150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

14

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate supply V_{SS}	4.75	5.0	5.5	V
Drain supply V_{DD}	0.0	0	0.0	V
Gate supply V_{GG}	−11.0	−12.0	−13.0	V
Logic Levels (Data Inputs)				
Input HIGH level (logical 1) V_{IH}	3.5			V
Input LOW level (logical 0) V_{IL}			0.6	V
Clock Voltage Levels				
Clock HIGH level (logical 1) $V_{\phi H}$	3.5			V
Clock LOW level (logical 0) $V_{\phi L}$			0.6	V
Pulse Timing				
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			100	μs
Clock pulse width PW_{ϕ}	0.250		100	μs
Minimum clock frequency	0			MHz
Pulse Spacing				
Data setup (Note 1) t_{DS} at 25°C		240	290	ns
Data setup (Note 1) t_{DS} at 85°C		320	380	ns
Data Pulse Overlap Clock				
t_{DOC}	150			ns

NOTE 1: The clock input has to be at logic 0 during the minimum data setup (t_{DS} see timing diagram).

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{IL}	Input Leakage Current	−15 V applied to input			1	μA
Output Voltage Levels (See Note 2)						
V_{OL}	Output LOW level (logic 0)	1 TTL gate, C_L = 20 pF			0.45	V
V_{OH}	Output HIGH level (logic 1)	1 TTL gate, C_L = 20 pF	4.0			V
V_{OL}	Output LOW level (logic 0)	MOS load, C_L = 20 pF			0.3	V
V_{OH}	Output HIGH level (logic 1)	MOS load, C_L = 20 pF	4.0			V
Output Current						
I_{OSC}	Short circuit	Output shorted to ground			2.8	mA
R_{out}	Output resistance	Chip enable = 1, V_{out} = logic 0			300	Ω
R_{out}	Output resistance	Chip enable = 0	1			MΩ
Power Supply Current Drain (See Note 3)						
I_{SS}	Substrate supply			13.0		mA
I_{DD}	Drain supply			0		mA
I_{GG}	Gate supply			−13.0		mA
P_D	Power dissipation			225		mW

NOTE 2: For the final test purposes, worst-case TTL load is simulated by a resistor of 3.3 kΩ and 20 pF. An MOS load is simulated by a resistor of 20 kΩ and a capacitance of 20 pF.

NOTE 3: The current sink by the V_{SS} supply is sourced by the V_{GG} supply.

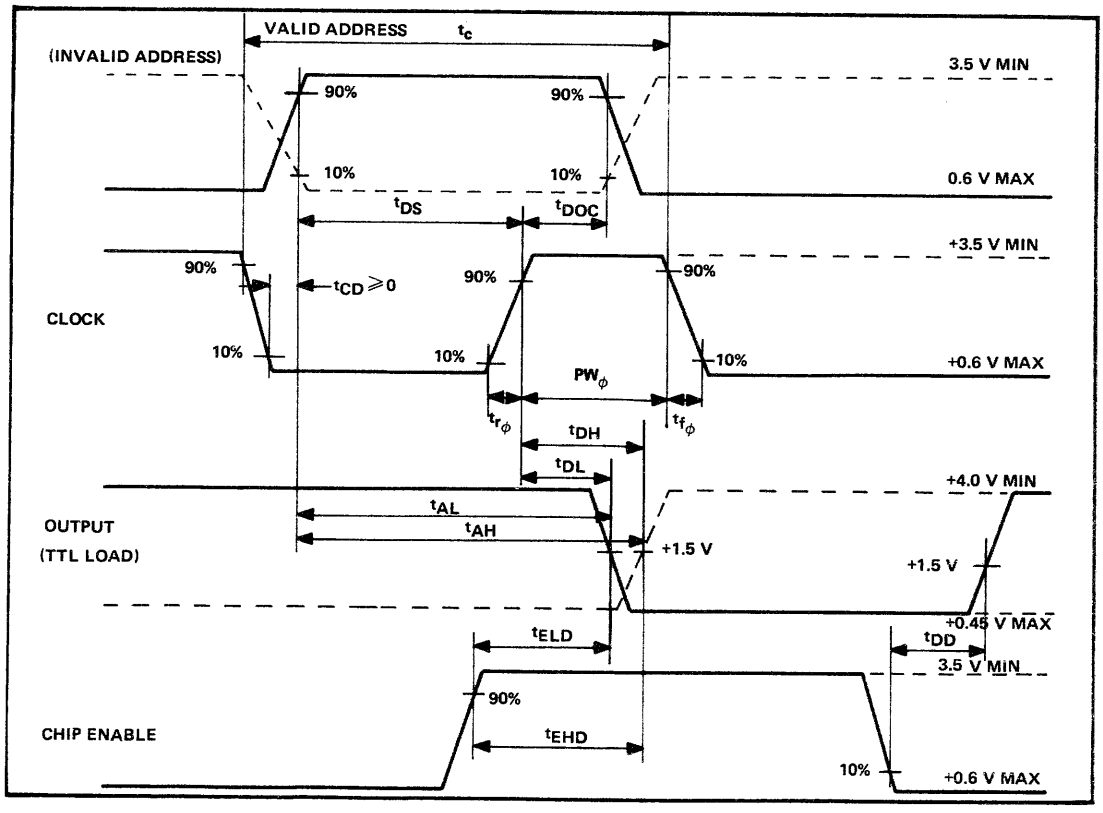
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

dynamic electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Cycle Time t_c		Load: 1 TTL gate, 20 pF		490	550	ns
Output Logic Delay (See Note 4)						
t_{DL}	Output LOW level	Load: 1 TTL gate, 20 pF			170	ns
t_{DH}	Output HIGH level	Load: 1 TTL gate, 20 pF			250	ns
Access Time (See Note 4)						
t_{AL}	Output LOW level	Load: 1 TTL gate, 20 pF		400	500	ns
t_{AH}	Output HIGH level	Load: 1 TTL gate, 20 pF		470	550	ns
Capacitance						
C_{IN}	Input	V_{in} = +5.0 V, f = 2 MHz		3	7	pF
C_ϕ	Clock	V_{in} = +5.0 V, f = 2 MHz		5	8	pF
Chip Enable Delay						
t_{ELD}	Enable output delay LOW level	Load = 20 pF to V_{DD}			150	ns
t_{EHD}	Enable output delay HIGH level	Load = 20 pF to V_{DD}			150	ns
t_{DD}	Disable output delay	Load = 20 pF to V_{DD}, 3.6 kΩ to V_{SS}			240	ns

NOTE 4: Output delay and access time are defined for V_{OUT} = +1.5 V (see timing diagram).

timing diagram and voltage waveforms



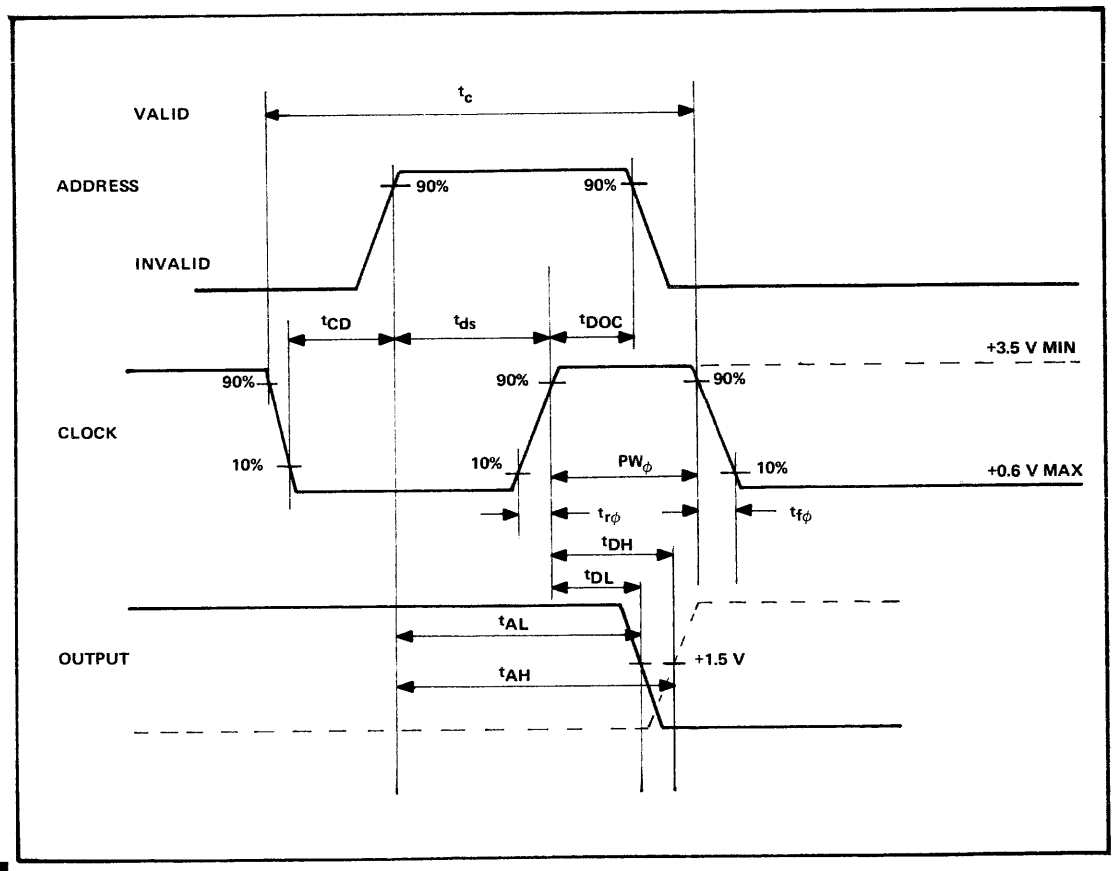
— continued

timing diagram and voltage waveforms (continued)

For specific applications the following timing scheme may be used for a t_{CD} (clock-to-address delay) of at least 150 ns and a t_{ds} (data set-up time) of at least 150 ns.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_c	Cycle Time	Load: 1 TTL gate, 20 pF		490	550	ns
Output Logic Delay (See Note 5)						
t_{DL}	Output LOW level	Load: 1 TTL gate, 20 pF		180	250	ns
t_{DH}	Output HIGH level	Load: 1 TTL gate, 20 pF		290	240	ns

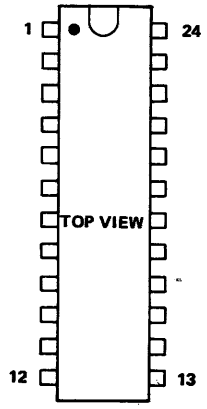
NOTE 5: This timing scheme does not affect chip enable timing.



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

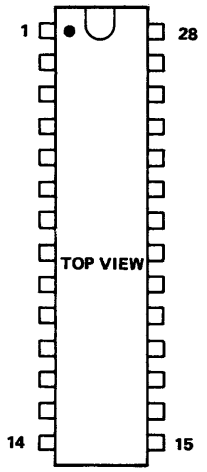
mechanical data and pin configuration

The device is normally mounted in a 24-pin hermetically sealed ceramic dual-in-line package (TMS 2300 JC) or a 24-pin plastic dual-in-line package (TMS 2300 NC), with pin configuration as follows:



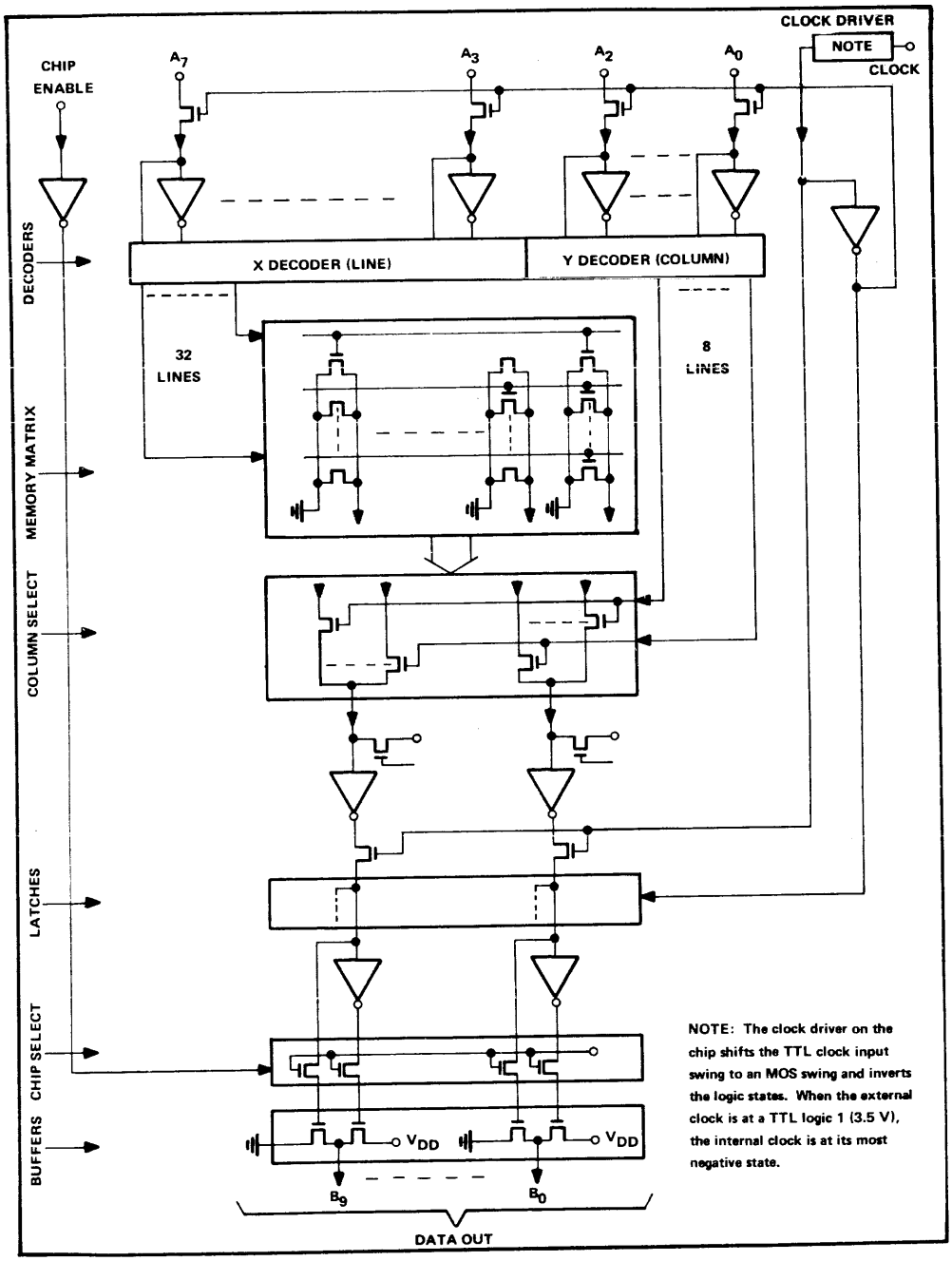
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	V_{SS}	13	Chip Enable
2	V_{GG}	14	V_{DD}
3	Input A_1	15	Output B_0
4	Input A_0	16	Output B_1
5	Input A_2	17	Output B_2
6	Input A_7	18	Output B_3
7	Input A_6	19	Output B_4
8	Input A_5	20	Output B_5
9	Input A_4	21	Output B_6
10	Clock	22	Output B_7
11	Input A_3	23	Output B_8
12	No Connection	24	Output B_9

Upon special request the device may be mounted in a 28-pin hermetically sealed ceramic dual-in-line package (TMS 2300 JC) or a 28-pin plastic dual-in-line package (TMS 2300 NC). (See MOS/LSI packaging section.) In this case the pin configuration is:



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	No connection	15	No Connection
2	No connection	16	Chip Enable
3	V_{SS}	17	V_{DD}
4	V_{GG}	18	Output B_0
5	Input A_1	19	Output B_1
6	Input A_0	20	Output B_2
7	Input A_2	21	Output B_3
8	Input A_7	22	Output B_4
9	Input A_6	23	No Connection
10	Input A_5	24	Output B_5
11	Input A_4	25	Output B_6
12	No Connection	26	Output B_7
13	Clock	27	Output B_8
14	Input A_3	28	Output B_9

The packages are designed for insertion in mounting-hole rows on 0.600-inch centers.

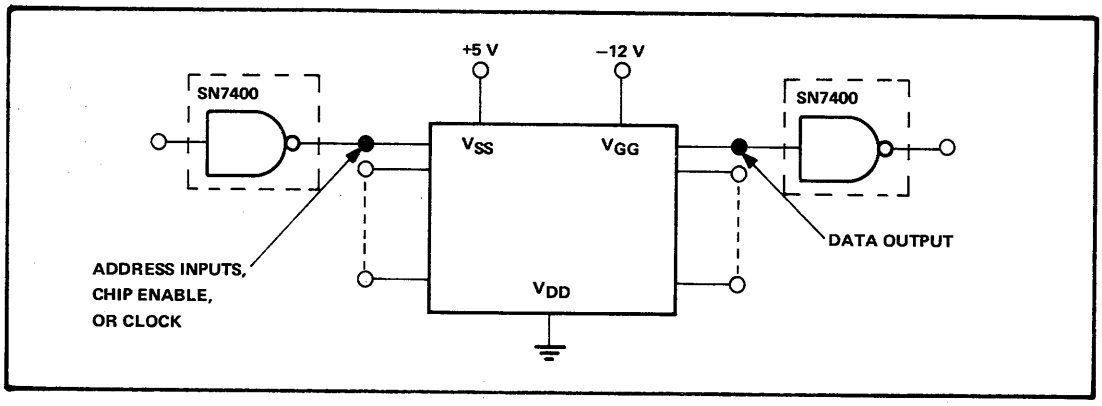


TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

interface circuits

a) TTL interface

No components are needed for TTL interface



b) Increase of noise margin

Noise margin may be increased by use of pull-up resistors to +5 V on the inputs (see schematic on page 7).

off-the-shelf devices

The TMS 2301 JC/NC has been programmed by TI to demonstrate the capabilities of the TMS 2300 JC/NC series. It is available off-the-shelf as a sample device.

truth table, TMS 2301 JC/NC

INPUT ADDRESS	$B_9B_8B_7B_6B_5B_4B_3B_2B_1B_0$	INPUT ADDRESS	$B_9B_8B_7B_6B_5B_4B_3B_2B_1B_0$	INPUT ADDRESS	$B_9B_8B_7B_6B_5B_4B_3B_2B_1B_0$	INPUT ADDRESS	$B_9B_8B_7B_6B_5B_4B_3B_2B_1B_0$
0	0000000000	64	1110000000	128	1111110000	192	1111111110
1	0000000000	65	1110000000	129	1111110000	193	1111111110
2	0000000000	66	1110000000	130	1111110000	194	1111111110
3	0000000000	67	1110000000	131	1111110000	195	1111111100
4	0000000000	68	1110000000	132	1111110000	196	1111111100
5	0000000000	69	1110000000	133	1111110000	197	1111111100
6	0000000000	70	1110000000	134	1111110000	198	1111111100
7	0000000000	71	1110000000	135	1111110000	199	1111111100
8	1000000000	72	1110000000	136	1111110000	200	1111111110
9	1000000000	73	1110000000	137	1111110000	201	1111111110
10	0000000000	74	1110000000	138	1111110000	202	1111111110
11	0000000000	75	1110000000	139	1111110000	203	1111111110
12	0000000000	76	1110000000	140	1111110000	204	1111111100
13	0000000000	77	1110000000	141	1111110000	205	1111111100
14	0000000000	78	1110000000	142	1111110000	206	1111111100
15	0000000000	79	1110000000	143	1111110000	207	1111111100
16	1000000000	80	1111000000	144	1111110000	208	1111111110
17	1000000000	81	1111000000	145	1111110000	209	1111111110
18	1000000000	82	1111000000	146	1111110000	210	1111111110
19	1000000000	83	1111000000	147	1111110000	211	1111111110
20	0000000000	84	1111000000	148	1111110000	212	1111111110
21	0000000000	85	1111000000	149	1111110000	213	1111111110
22	0000000000	86	1111000000	150	1111110000	214	1111111100
23	0000000000	87	1111000000	151	1111110000	215	1111111100
24	1000000000	88	1111000000	152	1111111000	216	1111111100
25	1000000000	89	1111000000	153	1111111000	217	1111111110
26	1000000000	90	1111000000	154	1111110000	218	1111111110
27	1000000000	91	1111000000	155	1111110000	219	1111111110
28	1000000000	92	1111000000	156	1111110000	220	1111111110
29	1000000000	93	1111000000	157	1111110000	221	1111111110
30	0000000000	94	1111000000	158	1111110000	222	1111111110
31	0000000000	95	1111000000	159	1111110000	223	1111111110
32	1000000000	96	1111000000	160	1111111000	224	1111111111
33	1000000000	97	1111000000	161	1111111000	225	1111111111
34	1000000000	98	1111000000	162	1111111000	226	1111111110
35	1000000000	99	1111000000	163	1111111000	227	1111111110
36	1000000000	100	1111000000	164	1111110000	228	1111111110
37	1000000000	101	1111000000	165	1111110000	229	1111111110
38	1000000000	102	1111000000	166	1111110000	230	1111111110
39	1000000000	103	1111000000	167	1111110000	231	1111111110
40	1100000000	104	1111000000	168	1111111000	232	1111111111
41	1100000000	105	1111000000	169	1111111000	233	1111111111
42	1000000000	106	1111000000	170	1111111000	234	1111111111
43	1000000000	107	1111000000	171	1111111000	235	1111111111
44	1000000000	108	1111000000	172	1111111000	236	1111111110
45	1000000000	109	1111000000	173	1111111000	237	1111111110
46	1000000000	110	1111000000	174	1111110000	238	1111111110
47	1000000000	111	1111000000	175	1111110000	239	1111111110
48	1100000000	112	1111100000	176	1111111000	240	1111111111
49	1100000000	113	1111100000	177	1111111000	241	1111111111
50	1100000000	114	1111100000	178	1111111000	242	1111111111
51	1100000000	115	1111000000	179	1111111000	243	1111111111
52	1000000000	116	1111000000	180	1111111000	244	1111111111
53	1000000000	117	1111000000	181	1111111000	245	1111111111
54	1000000000	118	1111000000	182	1111111000	246	1111111110
55	1000000000	119	1111000000	183	1111111000	247	1111111110
56	1100000000	120	1111100000	184	1111111100	248	1111111111
57	1100000000	121	1111100000	185	1111111100	249	1111111111
58	1100000000	122	1111100000	186	1111111000	250	1111111111
59	1100000000	123	1111100000	187	1111111000	251	1111111111
60	1100000000	124	1111000000	188	1111111000	252	1111111111
61	1100000000	125	1111000000	189	1111111000	253	1111111111
62	1000000000	126	1111000000	190	1111111000	254	1111111111
63	1000000000	127	1111000000	191	1111111000	255	1111111111

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

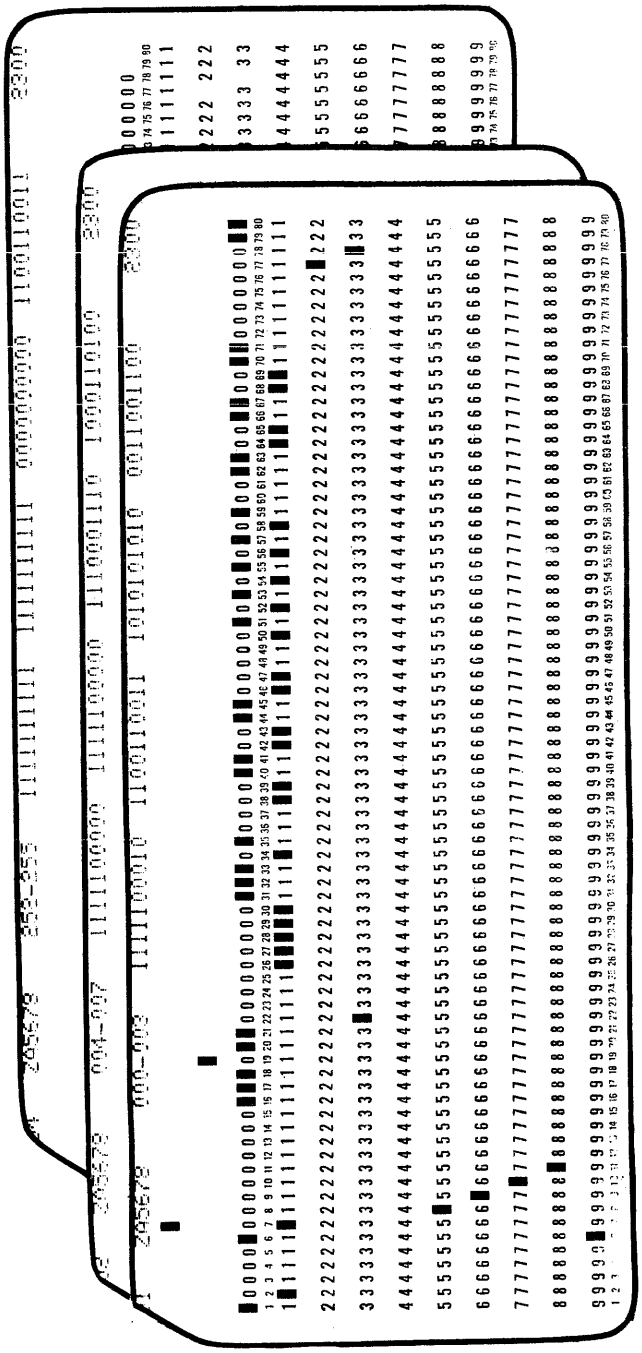
data encoding – software format

Programming information for the TMS 2300 JC/NC should be transmitted to TI in the form of a DECK OF 64 STANDARD 80-COLUMN COMPUTER CARDS, accompanied by a listing of these cards. This method eliminates many chances for error and guarantees the fastest delivery schedule of ROMs. Upon receipt of each deck, a computer run will be made and a copy of the computer-generated truth table sent back to the customer. This copy should be checked carefully. If any errors are discovered, TI must be notified immediately so that work can be stopped and the necessary adjustments made.

Each card in the data deck describes the outputs for four input addresses. All addresses must have their outputs defined. The addresses must also be placed in consecutive order. Cards should be punched according to the following format.

Column Nos.	
1–2	Punch the sequential card starting with 01 and ending with 64 (I2).
3–5	Blank
6–11	Punch either TM or ZA followed by a four digit number as supplied by MOS Marketing (TI part number.
12–15	Blank
16–18	Punch the address associated with the first output word described on the card (I3).
19	Punch a – (minus).
20–22	Punch the address associated with the last output word described on the card (I3).
	NOTE: Address locations are the numbers 000 through 255 and are derived from the binary-to-decimal conversion of the input address A_7, A_6, A_5, A_4, A_3, A_2, A_1, A_0. A_0 is considered the least-significant binary bit.
23–25	Blank
26–35	Punch the data associated with the outputs of the first memory location described on the card (10I1).
36–37	Blank
38–47	Punch the data associated with the outputs of the second memory location described on the card (10I1).
48–49	Blank
50–59	Punch the data associated with the outputs of the third memory location described on the card (10I1).
60–61	Blank
62–71	Punch the data associated with the outputs of the fourth memory location described on the card (10I1).
	NOTE: Outputs are defined in groups of ten. The order is B_9, B_8, B_7, B_6, B_5, B_4, B_3, B_2, B_1, B_0.
72–76	Blank
77–80	Punch 2300
	NOTE: For both inputs and outputs logic levels are punched in the form of 1s and 0s. Positive logic is assumed throughout. A logic 1 is the most positive voltage level and a logic 0 is the most negative voltage level.

TMS 2300 JC/NC — first, second and last cards



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS
LSI

TMS 2400 JC, TMS 2400 NC
ROW OUTPUT CHARACTER GENERATOR

JANUARY 1971

features

- Static operation
- 2240-bit capacity
- 64 characters of 35 bits (5 x 7)
- 7-Input character decoder
- 3-Input row decode
- 800-ns character access time
- Chip enable
- Open-drain or double-ended buffers
- TTL compatible
- Dual-in-line package

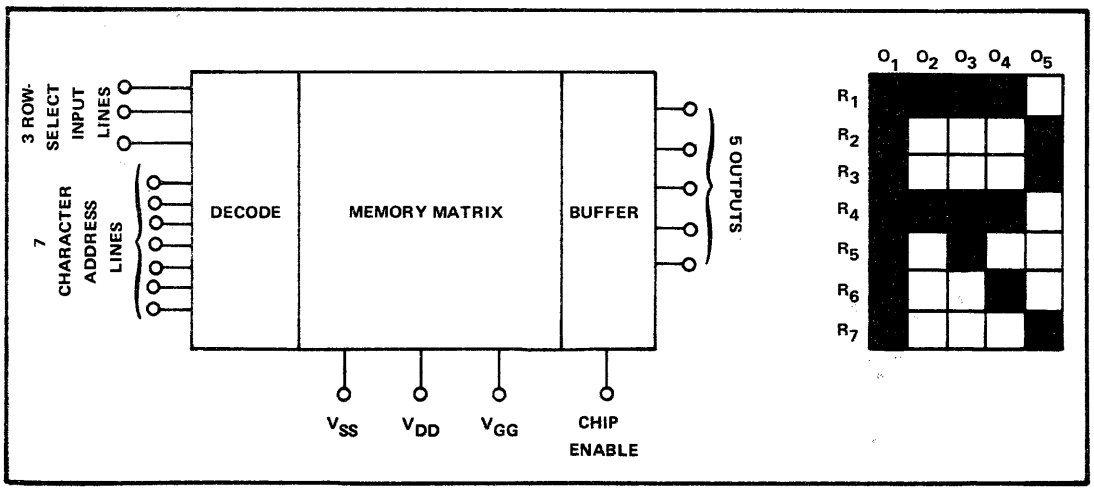
description

The TMS 2400 JC/NC series is a family of read-only-memory subsystem components manufactured using MOS P-channel enhancement-mode technology. All components in the series contain a 7-bit parallel-input character-address decoder and a 3-bit parallel-input row-address decoder, both complete with input inverters. Either open-drain or double-ended output buffers are provided for flexibility in external interfaces. The memory organization and data are permanently stored by programming a single mask during manufacture.

The memory is organized to function primarily as a row-output character generator. The five outputs represent a row in a 5 x 7 dot matrix.

"TMS 2400 JC" designates a unit mounted in a 28-pin hermetically sealed ceramic dual-in-line package, and "TMS 2400 NC" is used for a unit mounted in a 28-pin plastic package.

functional diagram



operation

The TMS 2400 JC/NC series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip enable) remains unchanged.

"Access time" is defined as the time required for all outputs to reach the minimum 1 level or maximum 0 level with the correct data. This time is measured from the point at which all address inputs and chip enable inputs are valid.

14

character scanning

The output character appears as a 7-word sequence on each of the five output lines. The sequence is controlled by the 3 row-select lines. The five outputs represent a row in a 5 x 7 character matrix. The row address can remain fixed while the character address changes (raster scan), or the character address may remain fixed while the row address changes (vertical or character scan).

row select truth table

ROW SELECT (NEGATIVE LOGIC)			SELECTS ROW
R_{s3}	R_{s2}	R_{s1}	
0	0	0	None
0	0	1	R 1
0	1	0	R 2
0	1	1	R 3
1	0	0	R 4
1	0	1	R 5
1	1	0	R 6
1	1	1	R 7

output buffers

The output buffers of the TMS 2400 JC/NC may be programmed to be either single-ended (open drain) to drive TTL/DTL logic, or double-ended to drive MOS logic.

The number of characters is increased by hardwiring together the outputs of different chips. Note that when using the hardwired output technique, all the chips that are hardwired together at the output should be single-ended chips.

chip enable

The chip enable may be programmed to be either a 1 or a 0.

The decoder will accept a 7-bit parallel input. Because only 6 bits are required in order to give out the 64 input words, the seventh bit may be used as an extra chip enable in single-ended operations.

A disable input on the chip enable input will cause the outputs to become open circuits on the "single-ended" (open-drain) type output buffer and will cause the outputs to go to V_{DD} on the double-ended (push-pull) type output buffer.

logic definition

Negative logic is assumed on the inputs.

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

An output blank is defined as the logic 1 output level, while an output dot is defined as the logic 0 output level.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage ranges (See Note 1) . . . . . −30 V to 0.5 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−11	−14	−16	V
Supply voltage V_{GG}	−22	−28	−29	V
Input, row select and enable, logic 1	−9	−14	−16	V
Input, row select and enable, logic 0	+0.3	0	−3	V

Maximum speed of operation will be obtained when operating at the nominal values. The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V).

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER (See Note 1)		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{out(1)}$	Output blank current (open drain)	−14 V applied to output			10	μA
$I_{out(0)}$	Output dot current (open drain)	−14 V applied to output	3	5		mA
$I_{out(0)}$	Output dot current (open drain)	V_{DD} = −12 V, V_{GG} = −24 V, −12 V applied to output	2	3		mA
$V_{out(0)}$	Output dot voltage (open drain)	I_O = 0.5 mA		−0.7	−2	V
$V_{out(0)}$	Output dot voltage (open drain)	I_O = 1 mA		−1.4	−2.5	V
$V_{out(0)}$	Output dot voltage (open drain)	I_O = 1.5 mA		−2.0	−4	V
$V_{out(0)}$	Output dot voltage (open drain)	I_O = 2 mA		−3	−5	V
$V_{out(1)}$	Output blank voltage (push-pull)	R_L = 1 mΩ	−10			V
$V_{out(0)}$	Output dot voltage (push-pull)	R_L = 1 mΩ			−2	V
	Power dissipation (Note 2)			450		mW
	Input leakage	−14 V applied to input			1	μA
I_{DD}	Drain current			20	30	mA
I_{GG}	Gate current			5	8.5	mA
	Input capacitance				10	pF

NOTES: 1. All voltages are measured with respect to V_{SS}.
2. Open-drain buffer, all outputs blank.

switching characteristics, under nominal operating conditions and at 25°C unless otherwise noted (refer to switching diagram)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Character access time (open drain) TTL load			550	900	ns
Character access time (open drain) TTL load	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		650	1200	ns
Row access time (open drain) TTL load			450	750	ns
Row access time (open drain) TTL load	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		500	900	ns
Chip enable access time (open drain) TTL load			100	250	ns
Chip enable access time (open drain) TTL load	V_{SS} = +12 V, V_{DD} = −0 V, V_{GG} = −12 V		125	300	ns

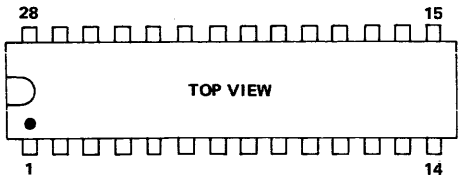
14

TMS 2400 JC, TMS 2400 NC
ROW OUTPUT CHARACTER GENERATOR

mechanical data

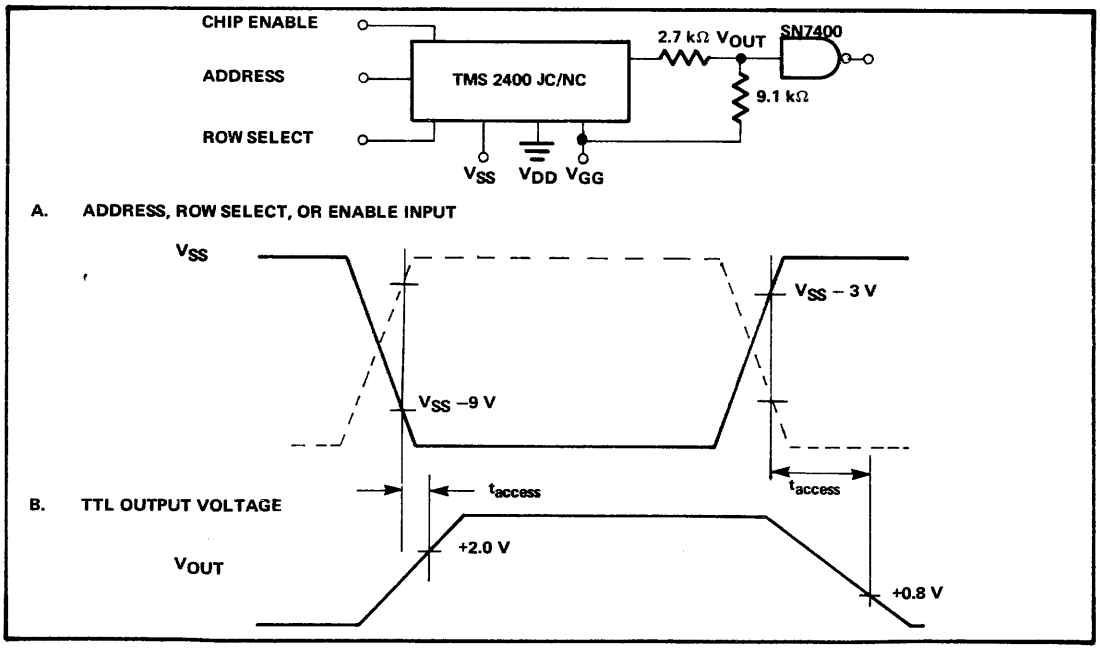
This device is available in both a 28-pin hermetically sealed ceramic dual-in-line package (TMS 2400 JC) and a 28-pin plastic package (TMS 2400 NC). These packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

pin configuration



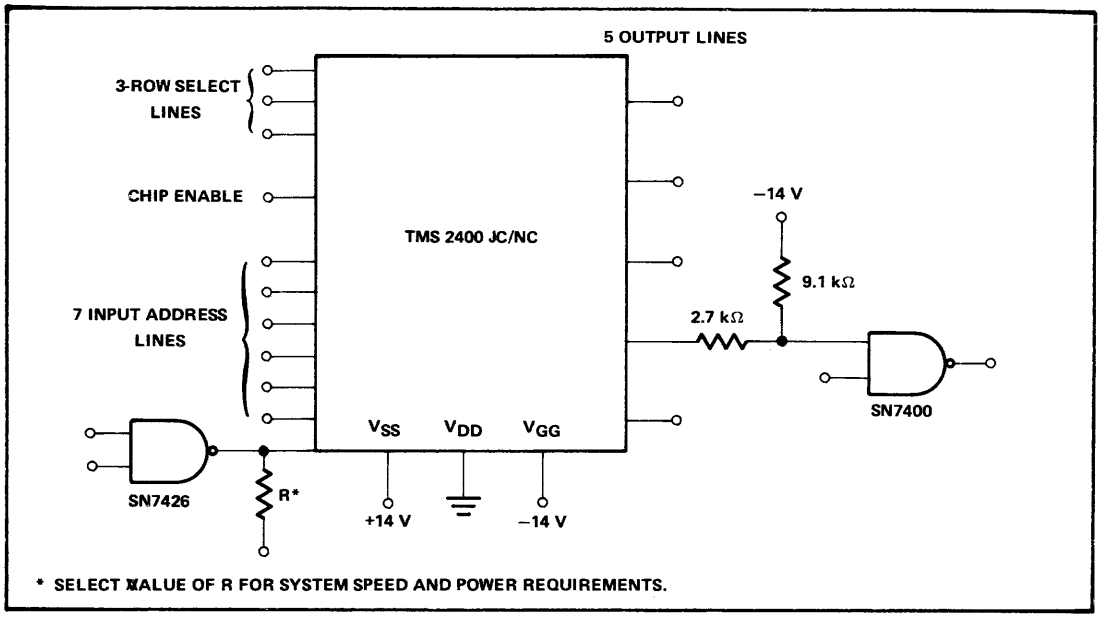
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	No connection	15	V_{SS}
2	RS_1	16	No connection
3	RS_2	17	V_{DD}
4	RS_3	18	No connection
5	No connection	19	I_1
6	O_1	20	I_2
7	O_2	21	I_3
8	O_3	22	I_4
9	O_4	23	I_5
10	O_5	24	I_7
11	No connection	25	No connection
12	Enable	26	V_{GG}
13	No connection	27	No connection
14	No connection	28	I_6

switching circuit and timing diagram (open-drain buffer, TTL load)



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

interfacing TMS 2400 JC/NC in a TTL system



* SELECT VALUE OF R FOR SYSTEM SPEED AND POWER REQUIREMENTS.

custom circuits

The TMS 2400 JC/NC series is programmed during the gate oxide removal stage of manufacturing. Only one mask per unique design need be created and all other processing steps remain the same for all devices. Options available to the customer during programming are:

- Character Format
- Enable Logic Polarity
- Single- or Double-ended Outputs

The TMS 2400 JC/NC series may also be used in microprogramming applications wherever a 448-word x 5-bit ROM may be useful.

Encoding of the gate mask is done by computer to provide a fast, error-free encoding process.

Standard encoding sheets (Software Package) are used. These encoding sheets are available from the TI sales offices.

standard circuits

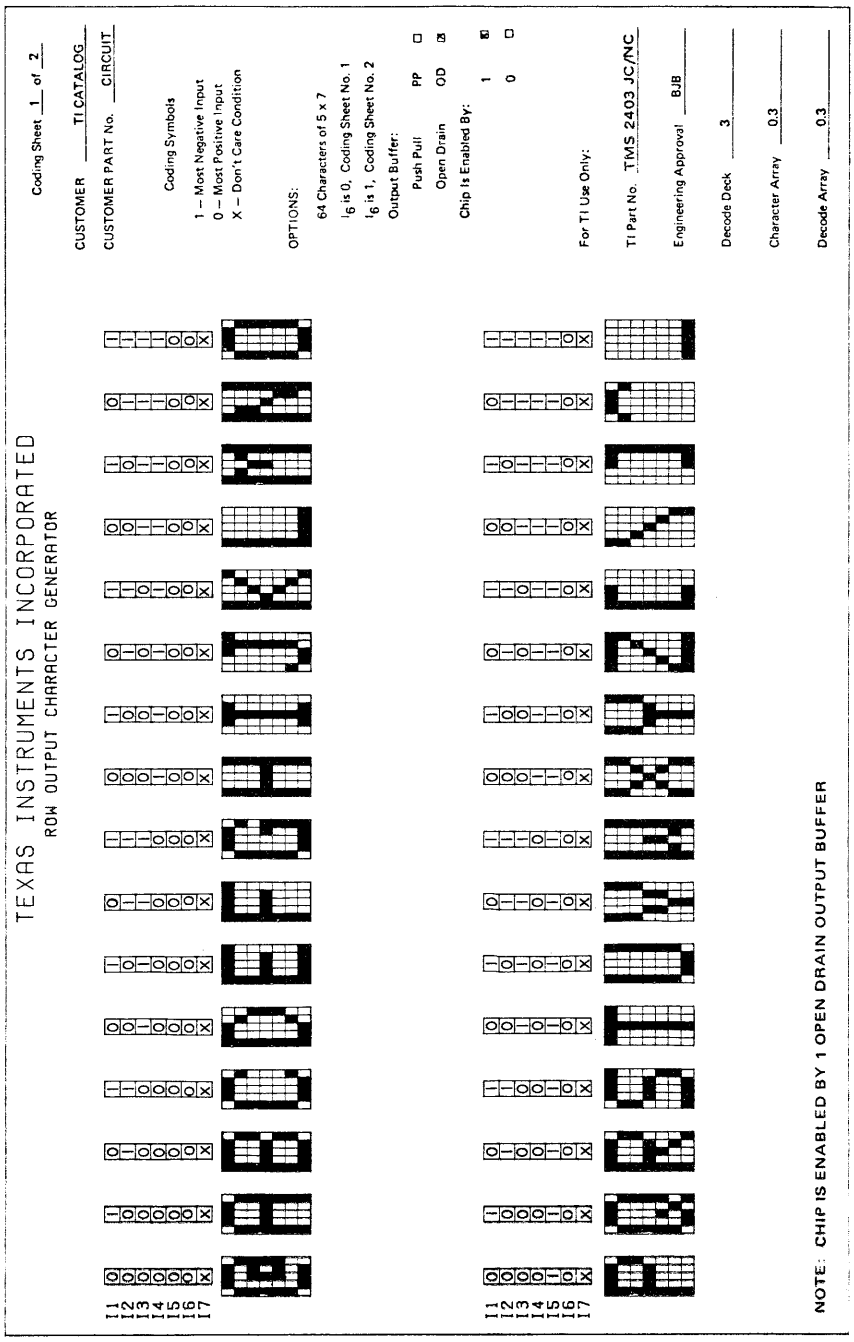
Because certain codes are widely used, TI has created a series of standard devices that are available off-the-shelf and for which there is no coding charge. The most widely used standard device is: TMS 2403 JC/NC USASCII CODE (See attached character format).

standard circuits (continued)

Organization: 64-Character Storage
35-Bit Character Matrix
Chip Enable = 1
Open-Drain outputs

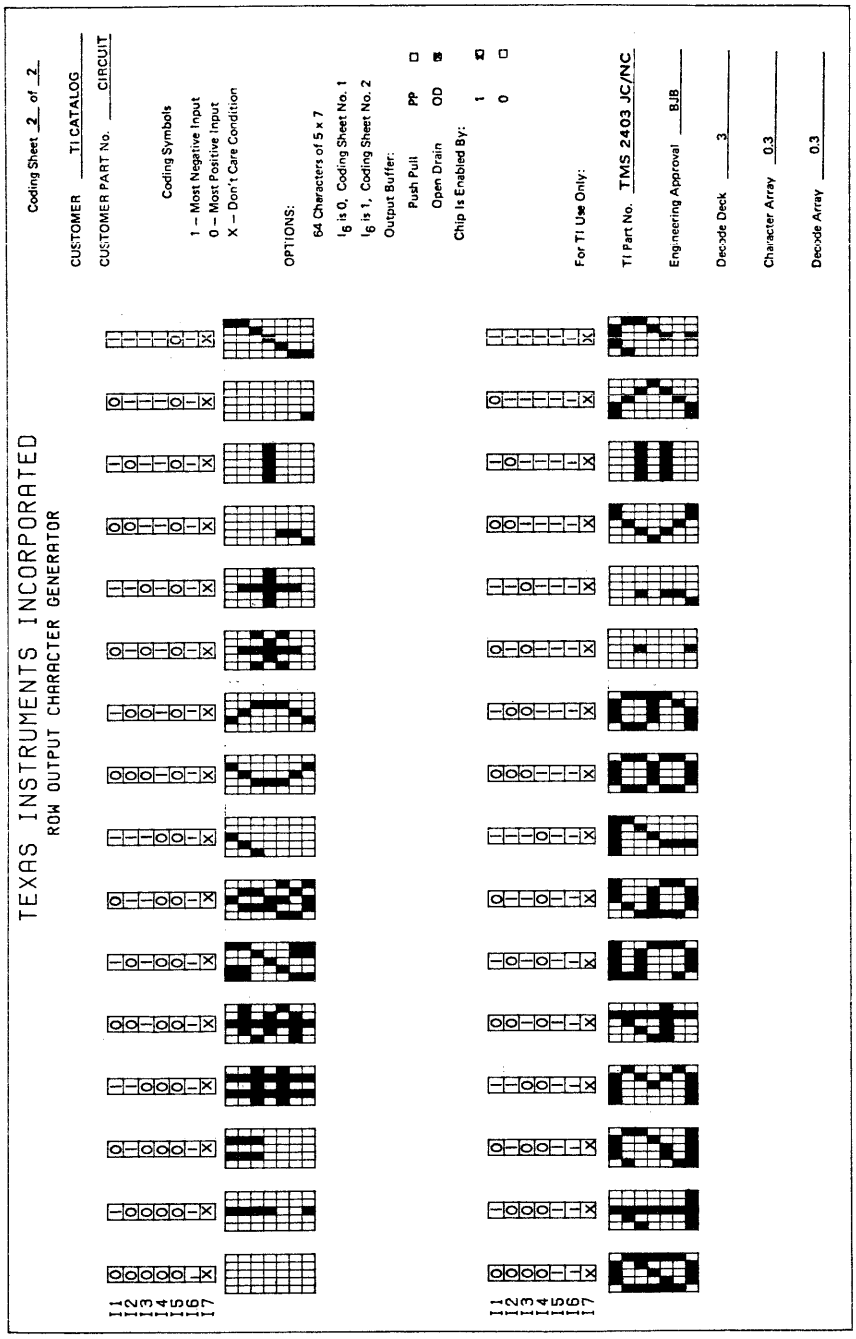
Other Available Standard Circuits:
TMS 2404 JC/NC — EBCDIC Character Generator (See attached character format)
64-Character Storage
35-bit Character Matrix
Chip Enable = 1
Open-Drain outputs

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222



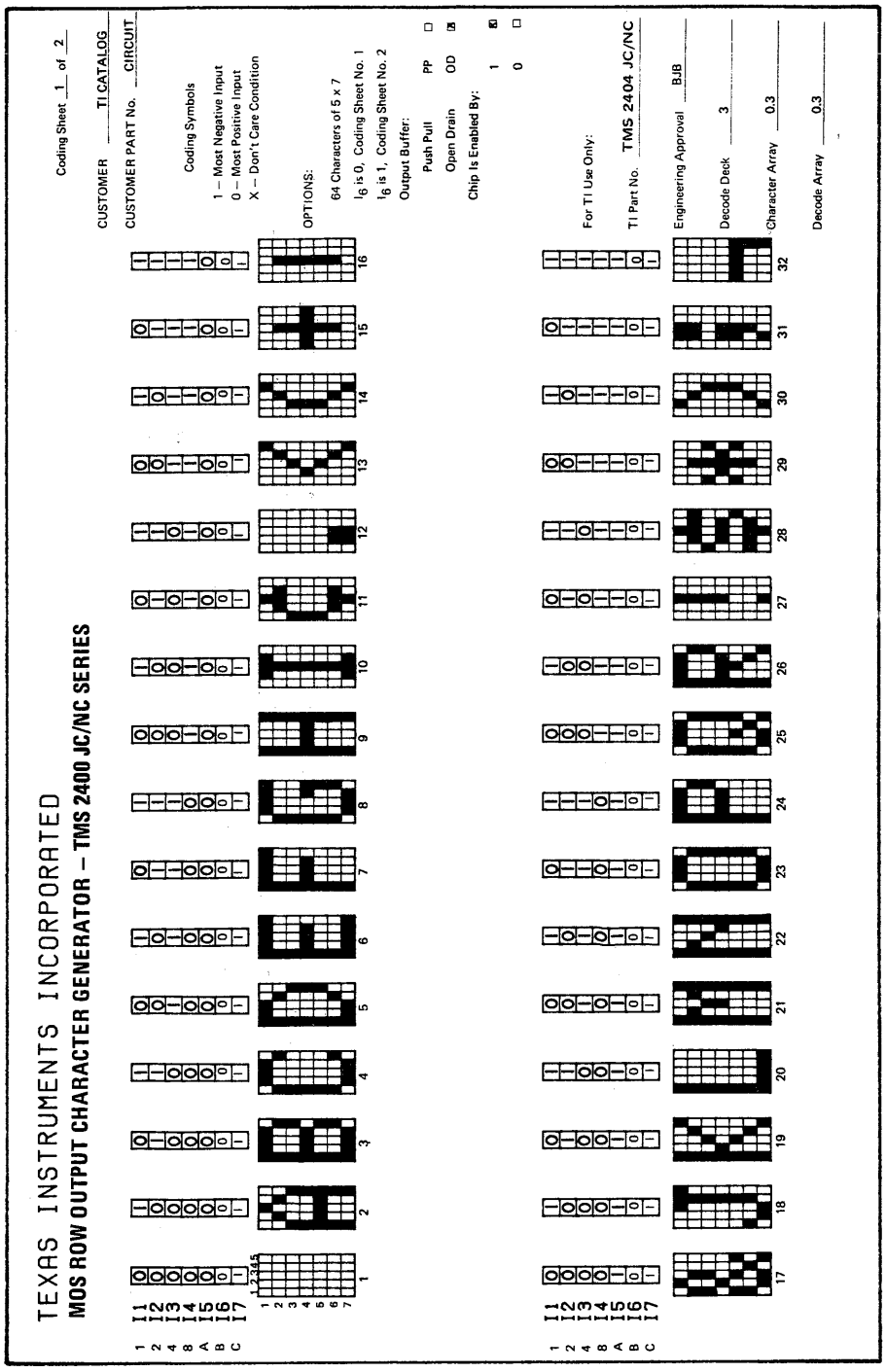
TMS 2403 JC/NC Character Font

14



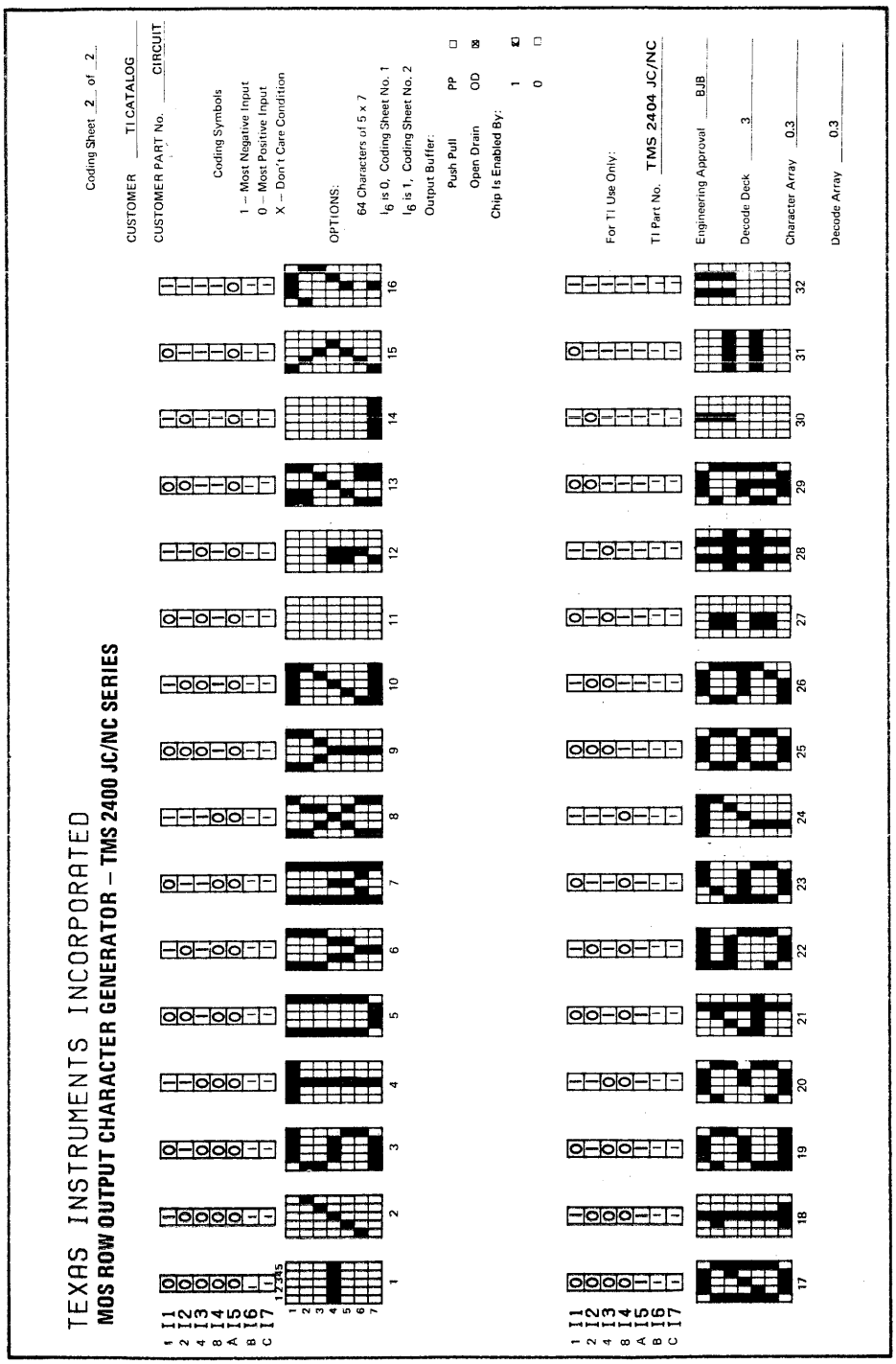
TMS 2403 JC/NC Character Font

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222



TMS 2404 JC/NC Character Font

14



TMS 2404 JC/NC Character Font

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 2500 JC, TMS 2500 NC
2560-BIT STATIC READ-ONLY MEMORY

features

- **Full TTL compatibility**
- **Two organizations available**
  - **512 words of 5 bits; 64 characters of 40 bits (5 x 8)**
  - **256 words of 10 bits; 32 characters of 80 bits (8 x 10)**
- **Static operation**
- **6-input character decoder**
- **3-input column or row-select decoder**
- **Typical access time — 350 ns**
- **Two programmable chip select inputs**
- **Push-pull output buffers**
- **Low threshold technology**
- **24-pin CDIP or 24-pin plastic package**

description

The TMS 2500 JC/NC series is a family of static character generators. Each of these devices has 2560-bit capacity.

Programming the memory content, chip organization and chip select is accomplished by changing a single mask during device fabrication.

In character generator applications, the 6-input decoder is employed for character address and the 3-input decoder is used for column/row select. In ROM applications all 9 inputs are used as a single decoder.

The output buffer is capable of driving one 74 series TTL gate or eight 74L series gates — with no external components.

"TMS 2500 JC" designates a unit mounted in a 24-pin hermetically sealed ceramic dual-in-line package, and "TMS 2500 NC" is used for a unit mounted in a 24-pin plastic package.

logic definition

a) LOGICAL 1 = most positive voltage

b) LOGICAL 0 = most negative voltage

operation

Featuring static operation, the TMS 2500 JC/NC requires no clocks. The output data remains valid as long as the input address (including chip select) remains unchanged. Access time is defined as the duration from the time the data on all logic inputs and chip select lines is valid to the time the output of a TTL gate is valid. (See switching circuit.)

In the 512 x 5 configuration there are two chip-select lines. The user chooses which logic input combination in these two lines enables the chip. For any other logic combination on these chip-select lines, the chip will be disabled (floating outputs).

In the 256 x 5 configuration the input Ig may be used as a third chip select.

Any or all of the chip select inputs may be programmed as Don't Care.

The number of characters available is increased by hardwiring together the outputs of different devices.

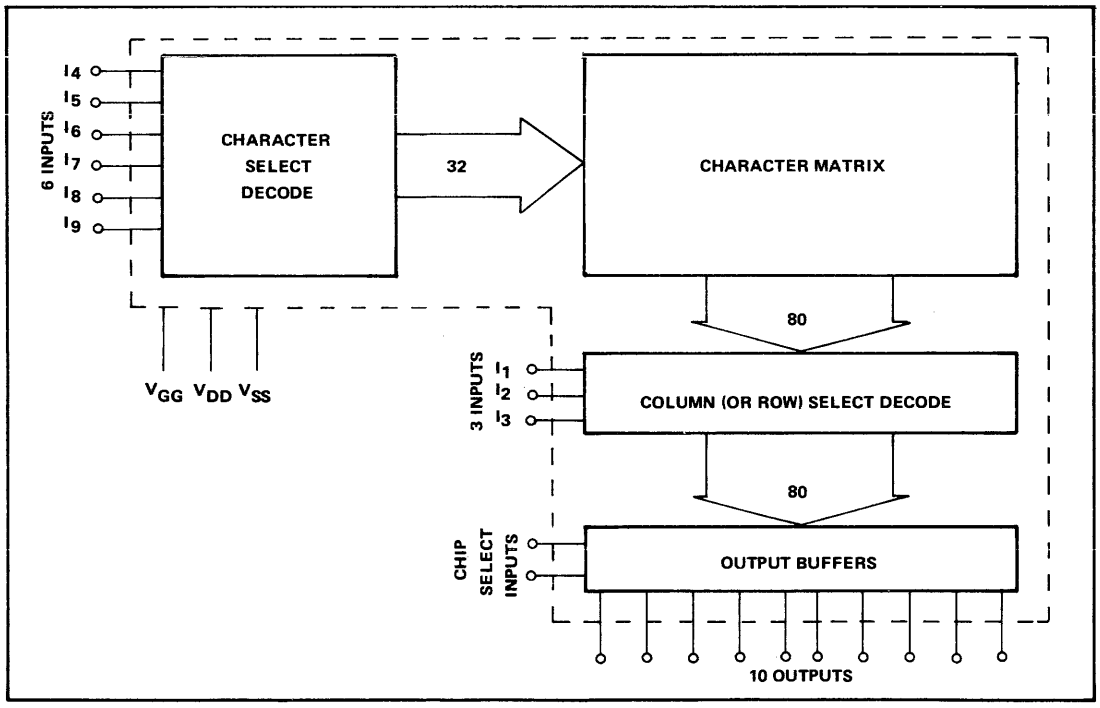
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−25 V to 0.3 V
Supply voltage V_{GG} range (Note 1)	−25 V to 0.3 V
Clock input voltage range (Note 1)	−25 V to 0.3 V
Data input voltage range (Note 1)	−25 V to 0.3 V
Operating free-air temperature range	−25°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

functional block diagram



recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate supply V_{SS}	+4.75	+5.00	5.25	V
Drain supply V_{DD}		0.00		V
Gate supply V_{GG}	−10	−12	−14	V
Logic Levels (See Note 1)				
Input level logic 0			1.0	V
Input level logic 1	3.5			V

NOTE 1: These input levels are given for V_{SS} = 5.0 V. If V_{SS} is other than 5.0 V the input levels must track V_{SS}.

14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels (Notes 2 and 3)					
Output logic 0 level V_{OL}	Load is one series 74 TTL gate		0.4	0.8	V
Output logic 1 level V_{OH}		3.0	4.5		V
Output Current					
Output logic 0	Output voltage of 0.5	−2		−3	mA
Output logic 1, case 1	Output voltage of 3.0	+1		+1.3	mA
Output logic 1, case 2	Output voltage of 4.5	+0.3		+0.4	mA
Power Supply Current Drain					
Substrate supply I_{SS}	Under static conditions.	10	12	15	mA
Drain supply I_{DD}	All outputs at logic 0.	20	24	30	mA
Gate supply I_{GG}	Under static conditions.	10	12	15	mA
Power Dissipation	All outputs at logic 0.	180	220	270	mW

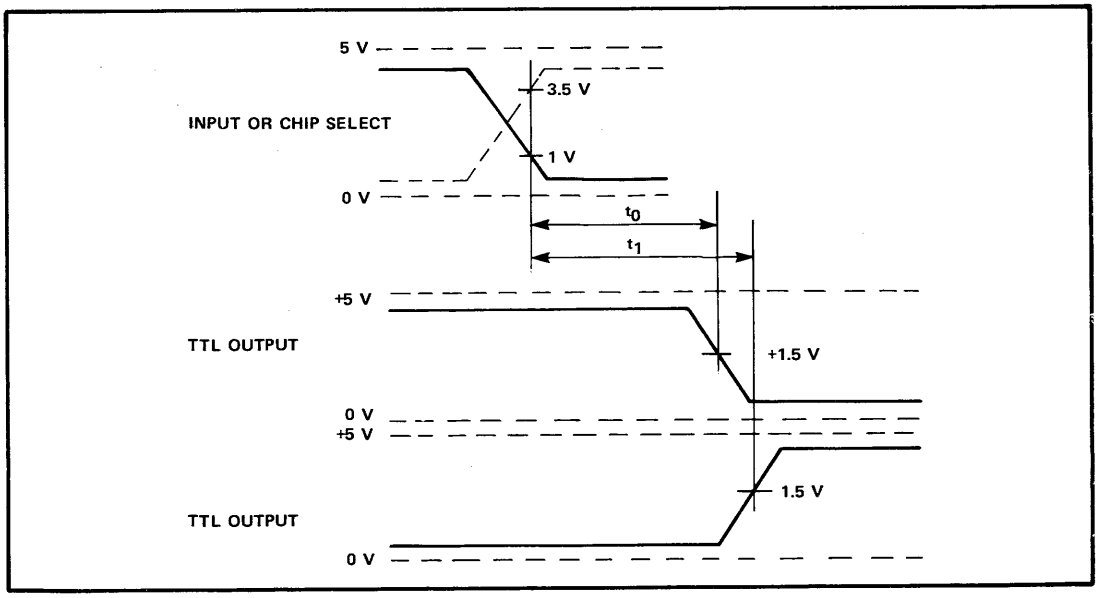
NOTES: 2. For V_{SS}, other than nominal output levels track V_{SS}.

3. For final test purposes, a worst-case TTL load is simulated by a load of 2.5 kΩ and a capacitance of 20 pF. All loads are connected between output and V_{SS}.

dynamic electrical characteristics (over −25°C to +70°C temperature range)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Access Time					
Output logic 0 level t_0	Load is one series 74 TTL gate	150	350	550	ns
Output logic 1 level t_1	C_L = 20 pF	150	350	550	ns
Input Capacitance C_{IN}	f = 100 kHz			5	pF

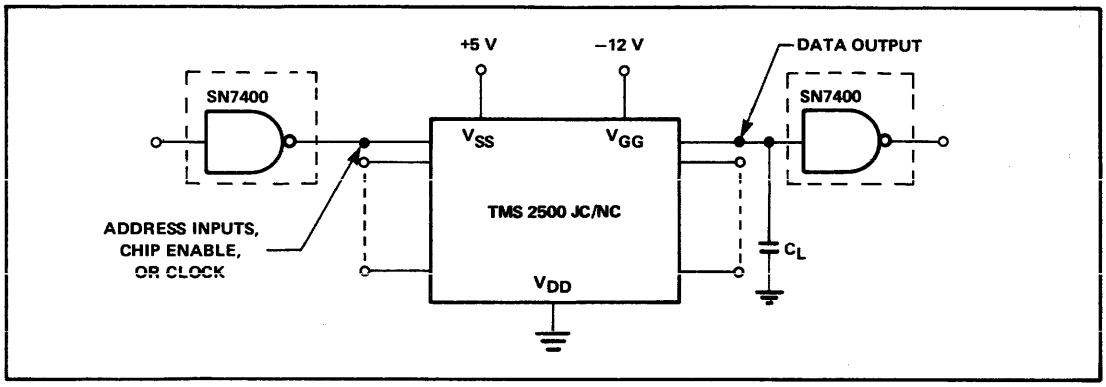
timing diagram and voltage waveforms



14

TTL interface and switching circuit

No components are needed for TTL interface.

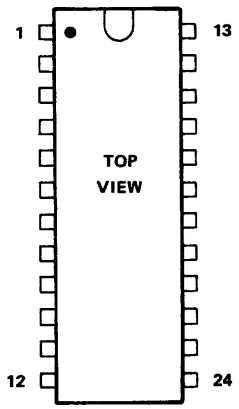


The load capacitance is used in the switching circuit to simulate parasitic capacitance loading in actual use.

mechanical data

This device is available in both a 24-pin hermetically sealed ceramic dual-in-line package (TMS 2500 JC) and a 24-pin plastic package (TMS 2500 NC). These packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

pin configuration



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	V_{GG}	13	CS1
2	O_1	14	CS2
3	O_2	15	I_9
4	O_3	16	I_8
5	O_4	17	I_7
6	O_5	18	I_6
7	O_6	19	I_5
8	O_7	20	I_4
9	O_8	21	I_3
10	O_9	22	I_2
11	O_{10}	23	I_1
12	V_{DD}	24	V_{SS}

For organization of 512 x 5, outputs are hardwired together as follows:

O_1 and O_2
O_3 and O_4
O_5 and O_6
O_7 and O_8
O_9 and O_{10}

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 2600 JC, TMS 2600 NC
2048-BIT STATIC READ-ONLY MEMORY

JANUARY, 1971

features

- 2048-bit capacity
- Static operation
- Maximum access time under 1 microsecond
- Two organizations available
- Open-drain output buffers or double-ended buffers
- TTL compatible
- 24-pin dual-in-line package

description

The TMS 2600 JC/NC series is a family of static read-only memories,each with capacity of 2048 bits.

Programming the memory content and output buffer configuration is accomplished by changing a single mask during device fabrication.

Inputs are available for enabling the chip and for selecting between a memory organization of 512 words of four bits or 256 words of eight bits.

Two types of output buffers are available:

- Single-Ended (open drain)

  Designed for driving TTL, this output has one MOS device with its drain at the output and its source at chip ground (substrate).

- Double-Ended

  Designed for driving the inputs to other MOS integrated circuits and devices, this version has its own MOS load resistor provided internally. It requires no additional external circuitry.

"TMS 2600 JC" designates a unit mounted in a 24-pin hermetically sealed ceramic dual-in-line package, and "TMS 2600 NC" is used for a unit mounted in a 24-pin plastic package.

logic definition

Negative logic is assumed.

a) Logical 1 = most negative voltage

b) Logical 0 = most positive voltage

operation

The TMS 2600 JC/NC series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip select) remains unchanged. The V_{GG} supply may be clocked to reduce power consumption without affecting access times. Access time is defined as the time between a change of data on any logic input or chip select line and a change of data on the output of a TTL gate. (See switching circuit).

operation (continued)

A logical 0 on the chip select input will cause the outputs to become open circuits on the "single-ended" (open-drain) type output buffer and will cause the outputs to go to V_{DD} on the double-ended (push-pull) type output buffer.

The number of words per output is increased by hardwiring together the outputs of different devices. Note that, when using the hardwired output technique, all devices should have single-ended buffers. Hardwiring outputs performs the AND function in negative logic.

organizational control logic

		OUTPUTS	
		B_1 B_3 B_5 B_7	B_2 B_4 B_6 B_8
256 words of 8 bits (MC = Logical 0):	A_9 = Logical 1	Enabled	Enabled
512 words of 4 bits (MC = Logical 1):	A_9 = Logical 0	Enabled	Logical 1
	A_9 = Logical 1	Logical 1	Enabled

To use the device as a 512 words of 4 bits, connect B_1 to B_2, B_3 to B_4, B_5 to B_6, B_7 to B_8.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage ranges (See Note 1) . . . . . −30 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−9	−12	−16	V
Supply voltage V_{GG}	−18	−24	−29	V
Input, chip select logic 1	−8	−12	−16	V
Input, chip select logic 0	+0.3	0	−3	V
Input pulse width	650			ns

The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V). Larger power supplies (e.g., +14 V, −14 V) may be used.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

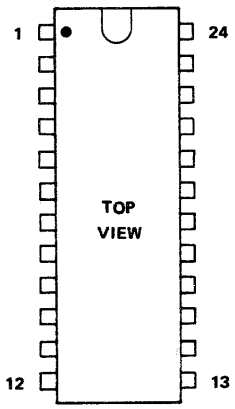
electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{out(0)}$	Logical 0 output current (Note 1)	−12 V applied	3	7		mA
$I_{out(1)}$	Logical 1 output current (Note 1)	−12 V applied			10	μA
$Z_{out(1)}$	Logical 1 output impedance (Note 2)	V applied = V_{DD} + 3		18	25	kΩ
$Z_{out(0)}$	Logical 0 output impedance (Note 4)	V applied = V_{SS} −3		0.8	1.1	kΩ
$V_{out(1)}$	Logical 1 output voltage (Note 2)	R_L = 1 mΩ	−9		−12	V
$V_{out(0)}$	Logical 0 output voltage (Note 2)	R_L = 1 mΩ	0		−2.0	V
t_{A1}	Access time (Notes 1 and 3)	See switching circuit		600	1000	ns
t_{A2}	Access time (Notes 1 and 3)	See switching circuit		550	1000	ns
P_d	Power dissipation (Note 2)	All outputs at Logical 0		180		mW
I_L	Input leakage current	−12 V applied to input			1	μA
C_{in}	Input capacitance	V_{in} = 0 V, f = 1 MHz		5		pF
I_{DD}	Drain current (Note 2)	All outputs = Logical 0		15		mA
I_{GG}	Gate current			1.0		μA

NOTES: 1. Open drain buffer
2. Push-pull buffer
3. See Switching Diagram
4. Either open-drain or push-pull configuration

mechanical data and pin configuration

This device is available in both a 24-pin hermetically sealed ceramic dual-in-line package (TMS 2600 JC) and a 24-pin plastic package (TMS 2600 NC). These packages are designed for insertion in mounting-hole rows on 0.600-inch centers.



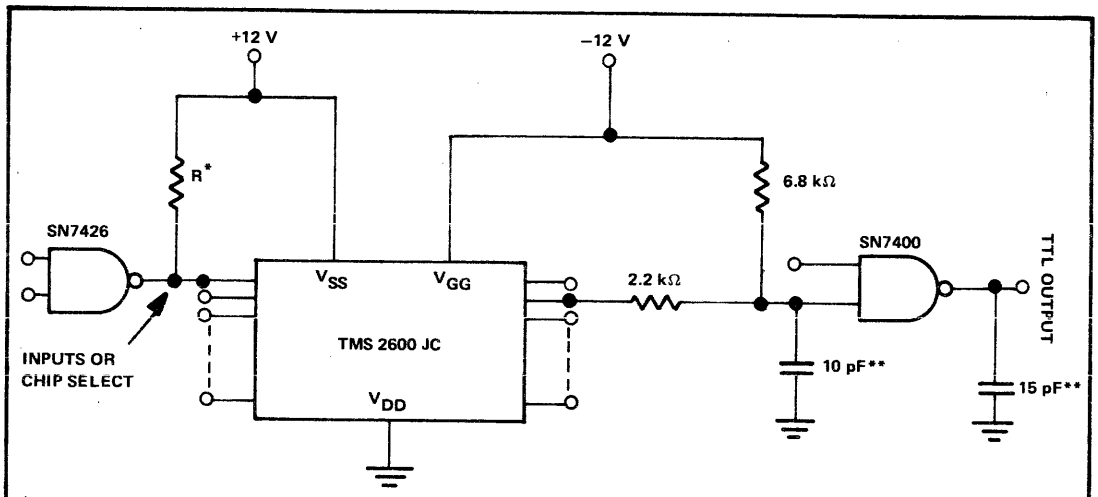
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	A_3	13	A_9
2	A_2	14	CS
3	A_1	15	MC
4	B_1	16	V_{GG}
5	B_2	17	A_8
6	B_3	18	A_7
7	B_4	19	A_6
8	B_5	20	A_5
9	B_6	21	A_4
10	B_7	22	NC
11	B_8	23	NC
12	V_{SS}	24	V_{DD}

A – input
B – output
MC – mode control
CS – chip select

V_{DD} – drain power supply
V_{GG} – ground power supply
V_{SS} – substrate

14

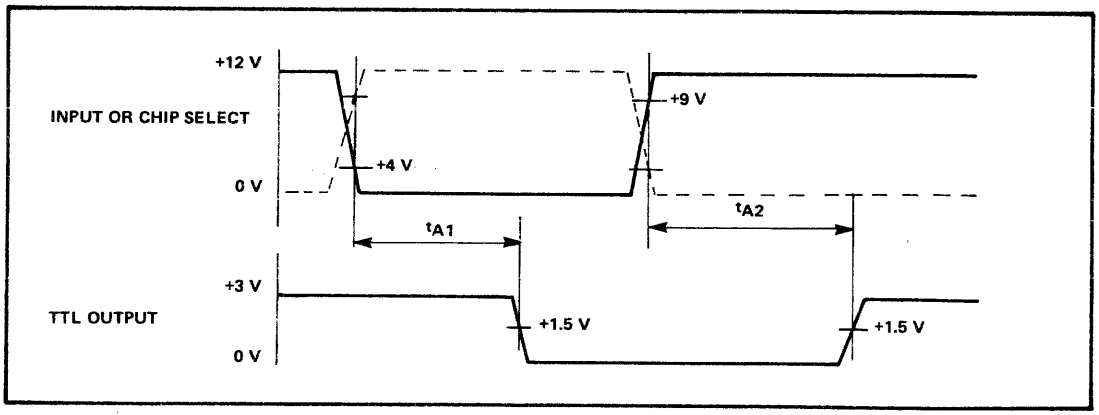
switching circuit and TTL interface



* Value of R depends on system speed and power requirements.

** The output capacitances are not part of the TTL interface. They are used in the switching circuits to simulate parasitic capacitance loading in actual use (board, interconnect, etc.).

switching diagram



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

off the shelf devices

These devices have been programmed by TI and are available off the shelf:

1) TMS 2601 JC/NC

   This device has been programmed to demonstrate the capabilities of the TMS 2600 JC/NC series. It is used as a sample device. The buffers are single ended.

2) TMS 2602 JC/NC Code Converter

   This device converts the USASCII code into the selectric line code and vice versa.

3) TMS 2603 JC/NC Code Converter

   This device converts the full EBCDIC code into the USASCII code.

Truth tables for the TMS 2602 JC/NC and 2603 JC/NC are available upon request.

TRUTH TABLE, TMS 2601 JC/NC

INPUT ADDRESS	$O_8O_7O_6O_5O_4O_3O_2O_1$	INPUT ADDRESS	$O_8O_7O_6O_5O_4O_3O_2O_1$	INPUT ADDRESS	$O_8O_7O_6O_5O_4O_3O_2O_1$	INPUT ADDRESS	$O_8O_7O_6O_5O_4O_3O_2O_1$
0	1 1 1 1 1 1 1 1	64	1 1 1 1 1 1 0 0	128	1 1 1 1 0 0 0 0	192	1 1 0 0 0 0 0 0
1	1 1 1 1 1 1 1 1	65	1 1 1 1 1 1 0 0	129	1 1 1 1 0 0 0 0	193	1 1 0 0 0 0 0 0
2	1 1 1 1 1 1 1 1	66	1 1 1 1 1 1 0 0	130	1 1 1 1 0 0 0 0	194	1 1 0 0 0 0 0 0
3	1 1 1 1 1 1 1 1	67	1 1 1 1 1 1 0 0	131	1 1 1 1 0 0 0 0	195	1 1 0 0 0 0 0 0
4	1 1 1 1 1 1 1 1	68	1 1 1 1 1 1 0 0	132	1 1 1 1 0 0 0 0	196	1 1 0 0 0 0 0 0
5	1 1 1 1 1 1 1 1	69	1 1 1 1 1 1 0 0	133	1 1 1 1 0 0 0 0	197	1 1 0 0 0 0 0 0
6	1 1 1 1 1 1 1 1	70	1 1 1 1 1 1 0 0	134	1 1 1 1 0 0 0 0	198	1 1 0 0 0 0 0 0
7	1 1 1 1 1 1 1 1	71	1 1 1 1 1 1 0 0	135	1 1 1 1 0 0 0 0	199	1 1 0 0 0 0 0 0
8	1 1 1 1 1 1 1 0	72	1 1 1 1 1 0 0 0	136	1 1 1 0 0 0 0 0	200	1 0 0 0 0 0 0 0
9	1 1 1 1 1 1 1 0	73	1 1 1 1 1 0 0 0	137	1 1 1 0 0 0 0 0	201	1 0 0 0 0 0 0 0
10	1 1 1 1 1 1 1 1	74	1 1 1 1 1 1 0 0	138	1 1 1 1 0 0 0 0	202	1 1 0 0 0 0 0 0
11	1 1 1 1 1 1 1 1	75	1 1 1 1 1 1 0 0	139	1 1 1 1 0 0 0 0	203	1 1 0 0 0 0 0 0
12	1 1 1 1 1 1 1 1	76	1 1 1 1 1 1 0 0	140	1 1 1 1 0 0 0 0	204	1 1 0 0 0 0 0 0
13	1 1 1 1 1 1 1 1	77	1 1 1 1 1 1 0 0	141	1 1 1 1 0 0 0 0	205	1 1 0 0 0 0 0 0
14	1 1 1 1 1 1 1 1	78	1 1 1 1 1 1 0 0	142	1 1 1 1 0 0 0 0	206	1 1 0 0 0 0 0 0
15	1 1 1 1 1 1 1 1	79	1 1 1 1 1 1 0 0	143	1 1 1 1 0 0 0 0	207	1 1 0 0 0 0 0 0
16	1 1 1 1 1 1 1 0	80	1 1 1 1 1 0 0 0	144	1 1 1 0 0 0 0 0	208	1 0 0 0 0 0 0 0
17	1 1 1 1 1 1 1 0	81	1 1 1 1 1 0 0 0	145	1 1 1 0 0 0 0 0	209	1 0 0 0 0 0 0 0
18	1 1 1 1 1 1 1 0	82	1 1 1 1 1 0 0 0	146	1 1 1 0 0 0 0 0	210	1 0 0 0 0 0 0 0
19	1 1 1 1 1 1 1 0	83	1 1 1 1 1 0 0 0	147	1 1 1 0 0 0 0 0	211	1 0 0 0 0 0 0 0
20	1 1 1 1 1 1 1 1	84	1 1 1 1 1 1 0 0	148	1 1 1 1 0 0 0 0	212	1 1 0 0 0 0 0 0
21	1 1 1 1 1 1 1 1	85	1 1 1 1 1 1 0 0	149	1 1 1 1 0 0 0 0	213	1 1 0 0 0 0 0 0
22	1 1 1 1 1 1 1 1	86	1 1 1 1 1 1 0 0	150	1 1 1 1 0 0 0 0	214	1 1 0 0 0 0 0 0
23	1 1 1 1 1 1 1 1	87	1 1 1 1 1 1 0 0	151	1 1 1 1 0 0 0 0	215	1 1 0 0 0 0 0 0
24	1 1 1 1 1 1 1 0	88	1 1 1 1 1 0 0 0	152	1 1 1 0 0 0 0 0	216	1 0 0 0 0 0 0 0
25	1 1 1 1 1 1 1 0	89	1 1 1 1 1 0 0 0	153	1 1 1 0 0 0 0 0	217	1 0 0 0 0 0 0 0
26	1 1 1 1 1 1 1 0	90	1 1 1 1 1 0 0 0	154	1 1 1 0 0 0 0 0	218	1 0 0 0 0 0 0 0
27	1 1 1 1 1 1 1 0	91	1 1 1 1 1 0 0 0	155	1 1 1 0 0 0 0 0	219	1 0 0 0 0 0 0 0
28	1 1 1 1 1 1 1 0	92	1 1 1 1 1 0 0 0	156	1 1 1 0 0 0 0 0	220	1 0 0 0 0 0 0 0
29	1 1 1 1 1 1 1 0	93	1 1 1 1 1 0 0 0	157	1 1 1 0 0 0 0 0	221	1 0 0 0 0 0 0 0
30	1 1 1 1 1 1 1 1	94	1 1 1 1 1 1 0 0	158	1 1 1 1 0 0 0 0	222	1 1 0 0 0 0 0 0
31	1 1 1 1 1 1 1 1	95	1 1 1 1 1 1 0 0	159	1 1 1 1 0 0 0 0	223	1 1 0 0 0 0 0 0
32	1 1 1 1 1 1 1 0	96	1 1 1 1 1 0 0 0	160	1 1 1 0 0 0 0 0	224	1 0 0 0 0 0 0 0
33	1 1 1 1 1 1 1 0	97	1 1 1 1 1 0 0 0	161	1 1 1 0 0 0 0 0	225	1 0 0 0 0 0 0 0
34	1 1 1 1 1 1 1 0	98	1 1 1 1 1 0 0 0	162	1 1 1 0 0 0 0 0	226	1 0 0 0 0 0 0 0
35	1 1 1 1 1 1 1 0	99	1 1 1 1 1 0 0 0	163	1 1 1 0 0 0 0 0	227	1 0 0 0 0 0 0 0
36	1 1 1 1 1 1 1 0	100	1 1 1 1 1 0 0 0	164	1 1 1 0 0 0 0 0	228	1 0 0 0 0 0 0 0
37	1 1 1 1 1 1 1 0	101	1 1 1 1 1 0 0 0	165	1 1 1 0 0 0 0 0	229	1 0 0 0 0 0 0 0
38	1 1 1 1 1 1 1 0	102	1 1 1 1 1 0 0 0	166	1 1 1 0 0 0 0 0	230	1 0 0 0 0 0 0 0
39	1 1 1 1 1 1 1 0	103	1 1 1 1 1 0 0 0	167	1 1 1 0 0 0 0 0	231	1 0 0 0 0 0 0 0
40	1 1 1 1 1 1 0 0	104	1 1 1 1 0 0 0 0	168	1 1 0 0 0 0 0 0	232	0 0 0 0 0 0 0 0
41	1 1 1 1 1 1 0 0	105	1 1 1 1 0 0 0 0	169	1 1 0 0 0 0 0 0	233	0 0 0 0 0 0 0 0
42	1 1 1 1 1 1 1 0	106	1 1 1 1 1 0 0 0	170	1 1 1 0 0 0 0 0	234	1 0 0 0 0 0 0 0
43	1 1 1 1 1 1 1 0	107	1 1 1 1 1 0 0 0	171	1 1 1 0 0 0 0 0	235	1 0 0 0 0 0 0 0
44	1 1 1 1 1 1 1 0	108	1 1 1 1 1 0 0 0	172	1 1 1 0 0 0 0 0	236	1 0 0 0 0 0 0 0
45	1 1 1 1 1 1 1 0	109	1 1 1 1 1 0 0 0	173	1 1 1 0 0 0 0 0	237	1 0 0 0 0 0 0 0
46	1 1 1 1 1 1 1 0	110	1 1 1 1 1 0 0 0	174	1 1 1 0 0 0 0 0	238	1 0 0 0 0 0 0 0
47	1 1 1 1 1 1 1 0	111	1 1 1 1 1 0 0 0	175	1 1 1 0 0 0 0 0	239	1 0 0 0 0 0 0 0
48	1 1 1 1 1 1 0 0	112	1 1 1 1 0 0 0 0	176	1 1 0 0 0 0 0 0	240	0 0 0 0 0 0 0 0
49	1 1 1 1 1 1 0 0	113	1 1 1 1 0 0 0 0	177	1 1 0 0 0 0 0 0	241	0 0 0 0 0 0 0 0
50	1 1 1 1 1 1 0 0	114	1 1 1 1 0 0 0 0	178	1 1 0 0 0 0 0 0	242	0 0 0 0 0 0 0 0
51	1 1 1 1 1 1 0 0	115	1 1 1 1 0 0 0 0	179	1 1 0 0 0 0 0 0	243	0 0 0 0 0 0 0 0
52	1 1 1 1 1 1 1 0	116	1 1 1 1 1 0 0 0	180	1 1 1 0 0 0 0 0	244	1 0 0 0 0 0 0 0
53	1 1 1 1 1 1 1 0	117	1 1 1 1 1 0 0 0	181	1 1 1 0 0 0 0 0	245	1 0 0 0 0 0 0 0
54	1 1 1 1 1 1 1 0	118	1 1 1 1 1 0 0 0	182	1 1 1 0 0 0 0 0	246	1 0 0 0 0 0 0 0
55	1 1 1 1 1 1 1 0	119	1 1 1 1 1 0 0 0	183	1 1 1 0 0 0 0 0	247	1 0 0 0 0 0 0 0
56	1 1 1 1 1 1 0 0	120	1 1 1 1 0 0 0 0	184	1 1 0 0 0 0 0 0	248	0 0 0 0 0 0 0 0
57	1 1 1 1 1 1 0 0	121	1 1 1 1 0 0 0 0	185	1 1 0 0 0 0 0 0	249	0 0 0 0 0 0 0 0
58	1 1 1 1 1 1 0 0	122	1 1 1 1 0 0 0 0	186	1 1 0 0 0 0 0 0	250	0 0 0 0 0 0 0 0
59	1 1 1 1 1 1 0 0	123	1 1 1 1 0 0 0 0	187	1 1 0 0 0 0 0 0	251	0 0 0 0 0 0 0 0
60	1 1 1 1 1 1 0 0	124	1 1 1 1 0 0 0 0	188	1 1 0 0 0 0 0 0	252	0 0 0 0 0 0 0 0
61	1 1 1 1 1 1 0 0	125	1 1 1 1 0 0 0 0	189	1 1 0 0 0 0 0 0	253	0 0 0 0 0 0 0 0
62	1 1 1 1 1 1 1 0	126	1 1 1 1 1 0 0 0	190	1 1 1 0 0 0 0 0	254	1 0 0 0 0 0 0 0
63	1 1 1 1 1 1 1 0	127	1 1 1 1 1 0 0 0	191	1 1 1 0 0 0 0 0	255	1 0 0 0 0 0 0 0

14

SOFTWARE PACKAGE

input format

Programming information for the TMS 2600 JC/NC should be transmitted to TI in the form of a DECK of 43 STANDARD 80-COLUMN COMPUTER CARDS, accompanied by a listing of these cards. This method eliminates many chances for error and guarantees the fastest delivery schedule of ROMs. Upon receipt of each deck, a computer run will be made and a copy of the computer-generated truth table sent back to the customer. This copy should be checked carefully. If any errors are discovered, TI should be notified immediately so that work can be stopped and the necessary adjustments made.

Information on the various circuit options desired will be transmitted on a special form supplied by TI.

The main memory array can be so programmed that for any binary input of A_8 through A_1 (0 to 255), the outputs B_8 through B_1 are uniquely determined. Since A_9 and MC are used to select output paths, the internal storage of data in the array is the same regardless of organization – 256 x 8 or 512 x 4.

Each card in the data deck describes the outputs for six or twelve input addresses, depending on whether eight or four outputs are desired. All addresses must have their outputs defined. The addresses must also be placed in consecutive order. Cards should be punched according to the following format.

data card format

Column	
1-2	Punch the sequential card number (01 through 43)
3	Blank
4-5	Punch a "26" to signify TMS 2600 JC
6-11	Punch the Z identification number supplied by TI MOS Marketing (2 letters, 4 numbers)
12	Blank (a space for the revision letter if necessary)
13	Punch a "8" if using the 256 x 8 configuration, or punch a "4" if using the 512 x 4 configuration
14	Punch a "D" for open-drain type output buffers, or punch a "P" for push-pull type output buffers
15-17	Punch a right-justified integer representing the binary input address (0-255 if 8 outputs, 0-511 if only 4 outputs) for the first set of outputs described on the card
18	Punch a "–" (minus sign)
19-21	Punch a right-justified integer representing the binary input address for the last set of outputs described on the card
22	Blank
23-80	Punch a description of the output sets selected for the range of input addresses specified on the card. A "1" for a logical 1 and a "0" for a logical 0

For a 256 x 8 configuration each card will describe 6 output sets. The 43rd card will contain only 4 output sets.

23-30	Punch the outputs desired for B_8, B_7, B_6, B_5, B_4, B_3, B_2, and B_1, in that order, for the first address specified on the card
33-40	Punch the outputs desired for the second address
43-50	Punch the outputs desired for the third address

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

data card format (continued)

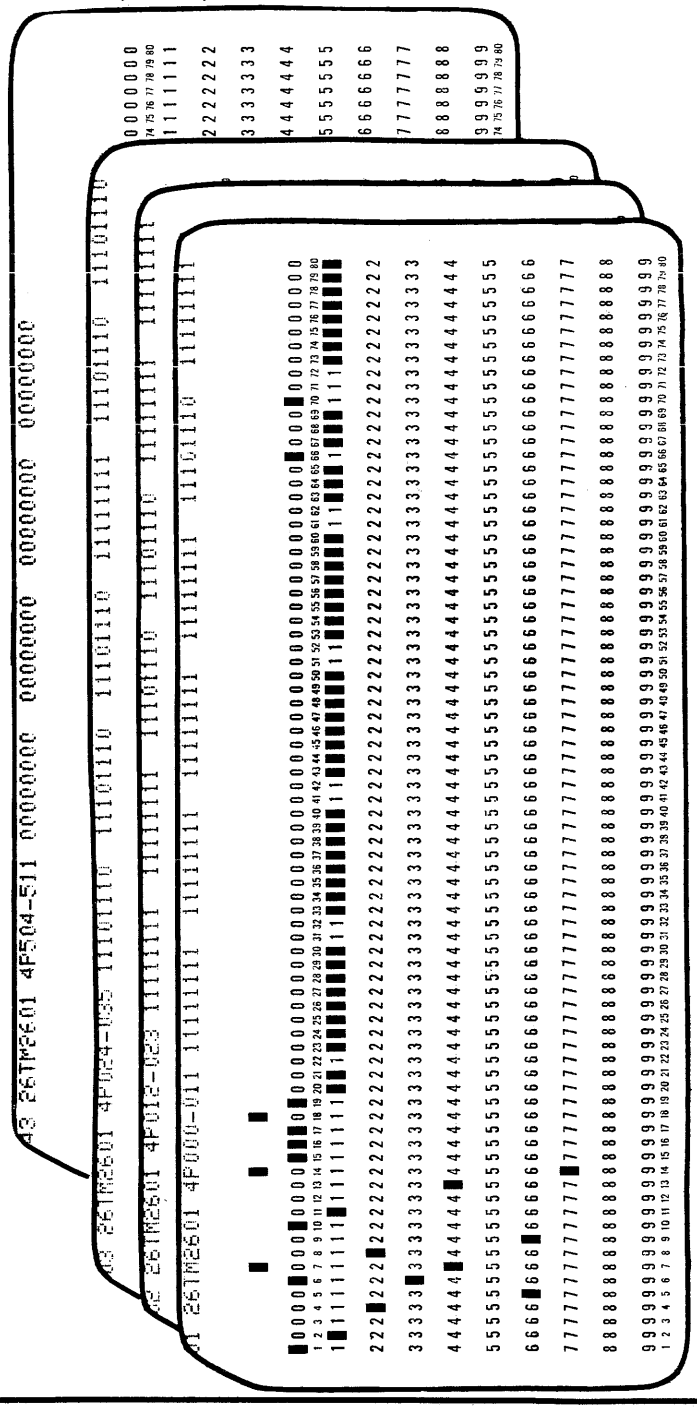
Column	
53-60	Punch the outputs desired for the fourth address
63-70	Punch the outputs desired for the fifth address
73-80	Punch the outputs desired for the sixth address

For a 512 x 4 configuration, each card will describe 12 output sets. The 43rd card will contain only 8 output sets.

23-26	Punch the outputs desired for B_8 or B_7, B_6 or B_5, B_4 or B_3, B_2 or B_1, in that order, for the first address specified on the card.
27-30	Punch the outputs desired for the second address
33-36	Punch the outputs desired for the third address
37-40	Punch the outputs desired for the fourth address
43-46	Punch the outputs desired for the fifth address
47-50	Punch the outputs desired for the sixth address
53-56	Punch the outputs desired for the seventh address
57-60	Punch the outputs desired for the eighth address
63-66	Punch the outputs desired for the ninth address
67-70	Punch the outputs desired for the tenth address
73-76	Punch the outputs desired for the eleventh address
77-80	Punch the outputs desired for the twelfth address

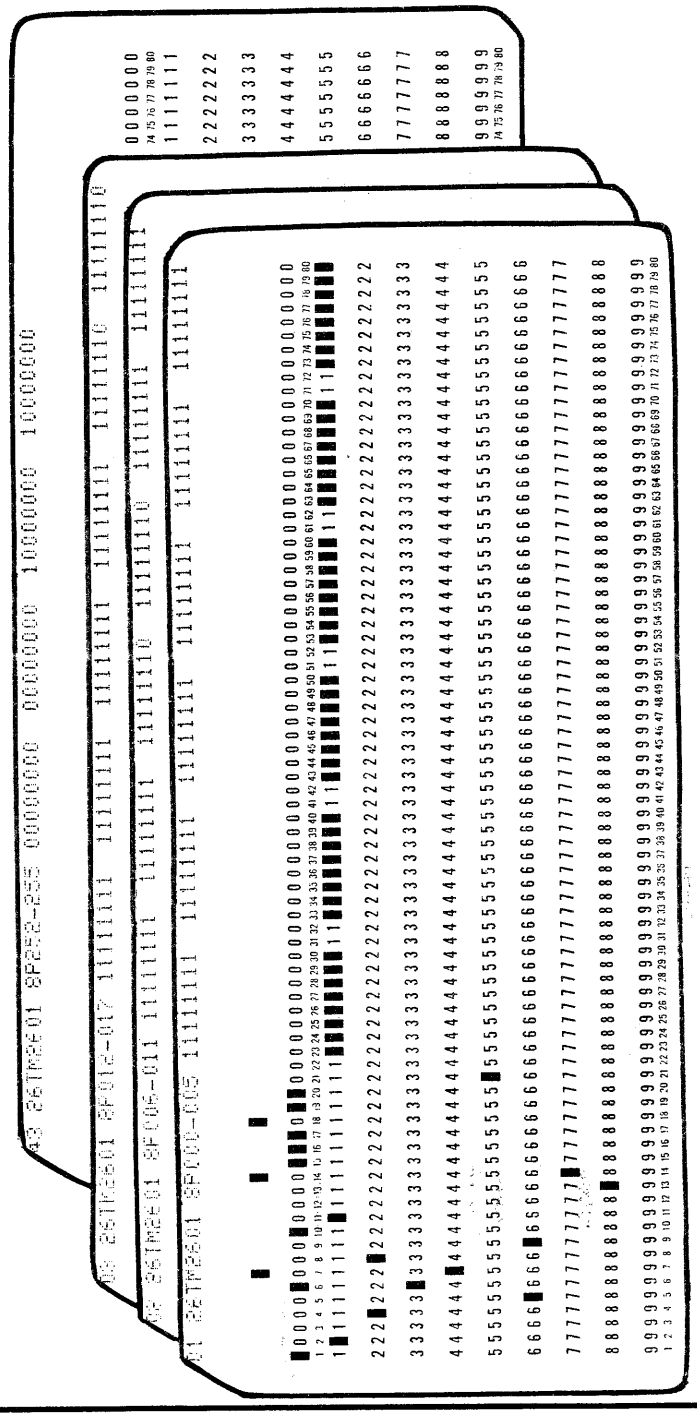
TMS 2600 JC, TMS 2600 NC
2048-BIT STATIC READ-ONLY MEMORY

512 x 4 organization — first, second, third and last cards



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

256 x 8 organization — first, second, third and last cards



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 2602 JC, TMS 2602 NC
USASCII-TO-SELECTRIC/SELECTRIC-TO-USASCII CODE CONVERTER

description

The TMS 2602 JC/NC is programmed TMS 2600 JC/NC ROM capable of converting both USASCII to Selectric Line Code, and Selectric Line Code to USASCII. **Electrical and mechanical characteristics, interfacing, and timing are identical to those of the TMS 2600 JC/NC.**

Inputs I_1 through I_7, and Outputs O_2 through O_8 of the ROM correspond to the two codes as follows:

ROM INPUT	SELECTRIC BIT	USASCII BIT	ROM OUTPUT
I_1	1	b_1	O_2
I_2	2	b_2	O_3
I_3	4	b_3	O_4
I_4	8	b_4	O_5
I_5	A	b_5	O_6
I_6	B	b_6	O_7
I_7	S	b_7	O_8

mode selection

Output O_1 is even parity for the 7-bit output word.

Input I_8 at logic 0 — USASCII is converted to Selectric Line Code

Input I_8 at logic 1 — Selectric Line Code is converted to USASCII

logic definition

As with the TMS 2600 JC/NC, negative logic is assumed.

Logical 1 = most negative voltage

Logical 0 = most positive voltage

code definition

The standard USASCII table is used as the USASCII code. The selectric code used is the IBM Correspondence Selectric Line Code. The following tables show the mapping from USASCII to Selectric and vice versa.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SELECTRIC TO USASCII (I_8 = logic 1)

SELECTRIC / USASCII

S B A →	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
8 4 2 1 ↓ / COL → / ROW ↓	0	1	2	3	4	5	6	7
0 0 0 0	0	SPACE1 / SPACE	t / t	¢ / !	j / j	SPACE2 / SPACE	T / T	o / <	J / J
0 0 0 1	1	1 / 1	x / x	m / m	g / g	± /]	X / X	M / M	G / G
0 0 1 0	2	2 / 2	n / n	. / .	= / =	@ / @	N / N	. / .	+ / +
0 0 1 1	3	3 / 3	u / u	v / v	f / f	# / #	U / U	V / V	F / F
0 1 0 0	4	5 / 5	e / e	' / /	p / p	% / %	E / E	" / "	P / P
0 1 0 1	5	7 / 7	d / d	r / r	; / ;	& / &	D / D	R / R	: / :
0 1 1 0	6	6 / 6	k / k	i / i	q / q	¢ / >	K / K	I / I	Q / Q
0 1 1 1	7	8 / 8	c / c	a / a	, / ,	* / *	C / C	A / A	, / ,
1 0 0 0	8	4 / 4	l / l	o / o	/ / /	$ / $	L / L	O / O	? / ?
1 0 0 1	9	O / O	h / h	s / s	y / y	) /)	H / H	S / S	Y / Y
1 0 1 0	10	z / z	① / RS	② / VT	③ / RS	Z / Z	④ / RS	⑤ / FF	⑥ / RS
1 0 1 1	11	9 / 9	b / b	w / w	— / —	(/ (	B / B	W / W	— / —
1 1 0 0	12	PN1 / DC2	BY1 / SUB	RES1 / EM	PF1 / DC4	PN2 / DC2	BY2 / FS	RES2 / GS	PF2 / DC4
1 1 0 1	13	RS1 / DC3	LF1 / LF	NL1 / CR	HTI / HT	RS2 / DC1	LF2 / LF	NL2 / CR	HT2 / HT
1 1 1 0	14	UC1 / SO	EOB1 / ETX	BS1 / BS	LC1 / BEL	UC2 / ENQ	EOB2 / ETB	BS2 / BS	LC2 / SI
1 1 1 1	15	EOT1 / EOT	PRE1 / ESC	IL1 / NUL	DEL1 / DEL	EOT2 / EOT	PRE2 / DLE	IL2 / NUL	DEL2 / NUL

USASCII TO SELECTRIC (I_8 = logic 0)

USASCII / SELECTRIC

b7 b6 b5 →	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b4 b3 b2 b1 / ROW ↓ COL →	0	1	2	3	4	5	6	7
0 0 0 0	0	NUL / IL1	DLE / PRE2	SPACE / SPACE1	0 / 0	@ / @	P / P	\ / '	p / p
0 0 0 1	1	SOH / b	DC1 / RS2	! / !	1 / 1	A / A	Q / Q	a / a	q / q
0 0 1 0	2	STX / 9	DC2 / PN1	" / "	2 / 2	B / B	R / R	b / b	r / r
0 0 1 1	3	ETX / EOB1	DC3 / RS1	# / #	3 / 3	C / C	S / S	c / c	s / s
0 1 0 0	4	EOT / EOT1	DC4 / PF1	$ / $	4 / 4	D / D	T / T	d / d	t / t
0 1 0 1	5	ENQ / UC2	NAK / !	% / %	5 / 5	E / E	U / U	e / e	u / u
0 1 1 0	6	ACK / –	SYN / IL2	& / &	6 / 6	F / F	V / V	f / f	v / v
0 1 1 1	7	BEL / LC1	ETB / EOB2	/ / '	7 / 7	G / G	W / W	g / g	w / w
1 0 0 0	8	BS / BS1	CAN / !	(/ (	8 / 8	H / H	X / X	h / h	x / x
1 0 0 1	9	HT / HT1	EM / RES1	) /)	9 / 9	I / I	Y / Y	i / i	y / y
1 0 1 0	10	LF / LF1	SUB / BY1	* / *	: / :	J / J	Z / Z	j / j	z / z
1 0 1 1	11	VT / ②	ESC / PRE1	+ / +	; / ;	K / K	[/ ±	k / k	[/ ±
1 1 0 0	12	FF / ⑤	FS / BY2	, / ,	< / °	L / L	\ / ±	l / l	; / ±
1 1 0 1	13	CR / HL1	GS / RES2	– / –	= / =	M / M	] / ±	m / m	] / ±
1 1 1 0	14	SO / UC1	RS / RES2	. / .	> / ¢	N / N	⁀ / ±	n / n	~ / ±
1 1 1 1	15	SI / LC2	US / BY2	/ / /	? / ?	O / O	— / —	o / o	DEL / DEL1

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 2603 JC, TMS 2603 NC
EBCDIC-TO-USASCII CODE CONVERTER

description

The TMS 2603 JC/NC is a programmed TMS 2600 JC/NC ROM capable of converting 8-bit EBCDIC to standard USASCII. **Electrical and mechanical characteristics, interfacing, and timing are identical to those of the TMS 2600 JC/NC.**

Inputs I_1 through I_8 and outputs O_2 through O_8 of the ROM correspond to the codes as follows:

ROM OUTPUT	EBCDIC BIT	USASCII BIT	ROM OUTPUT*
I_1	B_7 (LSB)	b_2	O_2
I_2	B_6	b_3	O_3
I_3	B_5	b_4	O_4
I_4	B_4	b_5	O_5
I_5	B_3	b_6	O_6
I_6	B_2	b_7	O_7
I_7	B_1	b_8	O_8
I_8	B_0 (MSB)		

* Output O_1 is even parity for the 7-bit USASCII output word.

logic definition

As with the TMS 2600 JC/NC negative logic is assumed.

Logic 1 = most negative voltage

Logic 0 = most positive voltage

code definition

Standard EBCDIC and USASCII codes are used for the conversion. The following table shows the mapping from EBCDIC to USASCII.

EBCDIC TO USASCII

EBCDIC / USASCII

0 → 1 → 2 → 3 →		0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1
4 5 6 7 ↓	COL → / ROW ↓	0	1	2	3	4	5	6	7
0 0 0 0	0	NUL / NUL	DLE / DLE	DS / NUL		SP / SP	& / &		
0 0 0 1	1	SOH / SOH	DC1 / DC1	SOS / NUL				/ /	
0 0 1 0	2	STX / STX	DC2 / DC2	FS / NUL	SYN / SYN				
0 0 1 1	3	ETX / ETX	DC3 / DC3						
0 1 0 0	4	PF / NUL	RES / NUL	BYP / NUL	PN / NUL				
0 1 0 1	5	HT / HT	NL / NUL	LF / LF	RS / NUL				
0 1 1 0	6	LC / NUL	BS / BS	EOB / ETB	UC / NUL				
0 1 1 1	7	DEL / DEL	IL / NUL	PRE / ESC	EOT / EOT				
1 0 0 0	8		CAN / CAN						
1 0 0 1	9		EM / EM						
1 0 1 0	10	SMM / NUL	CC / NUL	SM / NUL		¢ / NUL	! / !		: / :
1 0 1 1	11	VT / VT				. / .	$ / $	, / ,	# / #
1 1 0 0	12	FF / FF	IFS / FS		DC4 / DC4	< / <	* / *	% / %	@ / @
1 1 0 1	13	CR / CR	IGS / GS	ENQ / ENQ	NAK / NAK	(/ (	) /)	— / —	' / /
1 1 1 0	14	SO / SO	IRS / RS	ACK / ACK		+ / +	; / ;	> / >	= / =
1 1 1 1	15	SI / SI	IUS / US	BEL / BEL	SUB / SUB	| / :	¬ / NUL	? / ?	" / "

— Continued

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

EBCDIC TO USASCII (Continued)

EBCDIC / USASCII

0 1 2 3 →	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
4 5 6 7 ↓ / ROW ↓ / COL →	0	1	2	3	4	5	6	7
0 0 0 0	0							0 0
0 0 0 1	1	a a	j j			A A	J J	1 1
0 0 1 0	2	b b	k k	s s		B B	K K	S S	2 2
0 0 1 1	3	c c	l l	t t		C C	L L	T T	3 3
0 1 0 0	4	d d	m m	u u		D D	M M	U U	4 4
0 1 0 1	5	e e	n n	v v		E E	N N	V V	5 5
0 1 1 0	6	f f	o o	w w		F F	O O	W W	6 6
0 1 1 1	7	g g	p p	x x		G G	P P	X X	7 7
1 0 0 0	8	h h	q q	y y		H H	Q Q	Y Y	8 8
1 0 0 1	9	i i	r r	z z		I I	R R	Z Z	9 9
1 0 1 0	10								
1 0 1 1	11								
1 1 0 0	12								
1 1 0 1	13								
1 1 1 0	14								
1 1 1 1	15								

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 2604 JC, TMS 2604 NC
USASCII-TO-EBCDIC/SELECTRIC-TO-EBCDIC CODE CONVERTER

JANUARY, 1971

description

The TMS 2604 JC/NC is a programmed TMS 2600 JC/NC ROM capable of converting both USASCII and Selectric Line Code to EBCDIC. **Electrical and mechanical characteristics, interfacing, and timing are identical to those of the TMS 2600 JC/NC.**

Inputs I_1 through I_7 and Outputs O_1 through O_8 of the ROM correspond to the 3 codes as follows:

ROM OUTPUT	USASCII BIT	SELECTRIC BIT	EBCDIC BIT	ROM OUTPUT
I_1	b_1	1	B_7	O_1
I_2	b_2	2	B_6	O_2
I_3	b_3	4	B_5	O_3
I_4	b_4	8	B_4	O_4
I_5	b_5	A	B_3	O_5
I_6	b_6	B	B_2	O_6
I_7	b_7	S	B_1	O_7
			B_0	O_8

mode selection

Input I_8 at logical 0 — USASCII is converted to EBCDIC.

Input I_8 at logical 1 — Selectric is converted to EBCDIC.

logic definition

As with the TMS 2600 JC/NC, negative logic is assumed.

Logic 1 = most negative voltage

Logic 0 = most positive voltage

code definition

Standard USASCII and EBCDIC are used along with IBM correspondence Selectric Line Code to produce the following conversion table:

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

USASCII TO EBCDIC
($I_8 = 0$)

USASCII / EBCDIC

b_4 b_3 b_2 b_1	ROW / COL	b_7 b_6 b_5 = 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
		0	1	2	3	4	5	6	7
0 0 0 0	0	NUL / NUL	DLE / DLE	SP / SP	0 / 0	@ / @	P / P	↑ / ↑	p / p
0 0 0 1	1	SOH / SOH	DC1 / DC1	! / SP	1 / 1	A / A	Q / Q	a / a	q / q
0 0 1 0	2	STX / STX	DC2 / DC2	" / "	2 / 2	B / B	R / R	b / b	r / r
0 0 1 1	3	ETX / ETX	DC3 / DC3	# / #	3 / 3	C / C	S / S	c / c	s / s
0 1 0 0	4	EOT / EOT	DC4 / DC4	$ / $	4 / 4	D / D	T / T	d / d	t / t
0 1 0 1	5	ENQ / ENQ	NAK / NAK	% / %	5 / 5	E / E	U / U	e / e	u / u
0 1 1 0	6	ACK / ACK	SYN / SYN	& / &	6 / 6	F / F	V / V	f / f	v / v
0 1 1 1	7	BEL / BEL	ETB / EOB	' / '	7 / 7	G / G	W / W	g / g	w / w
1 0 0 0	8	BS / BS	CAN / CAN	(/ (	8 / 8	H / H	X / X	h / h	x / x
1 0 0 1	9	HT / HT	EM / EM	) /)	9 / 9	I / I	Y / Y	i / i	y / y
1 0 1 0	10	LF / LF	SUB / SUB	* / *	: / :	J / J	Z / Z	j / j	z / z
1 0 1 1	11	VT / VT	ESC / PRE	+ / +	; / ;	K / K	[/ (	k / k	[/ (
1 1 0 0	12	FF / FF	FS / IFS	, / ,	< / <	L / L	\ / /	l / l	; / l
1 1 0 1	13	CR / CR	GS / IGS	– / –	= / =	M / M	] /)	m / m	] /)
1 1 1 0	14	SO / SO	RS / IRS	. / .	> / >	N / N	⌒ / ¬	n / n	~ / ¢
1 1 1 1	15	SI / SI	US / IUS	/ / /	? / ?	O / O	— / —	o / o	DEL / DEL

SELECTRIC TO EBCDIC
(I8 = 1)

SELECTRIC / EBCDIC

S→ B→ A→		0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
8 4 2 1 ↓	COL → / ROW ↓	0	1	2	3	4	5	6	7
0 0 0 0	0	SPACE 1 / SPACE	t / t	¢ / !	j / j	SPACE 2 / SPACE	T / T	ø / <	J / J
0 0 0 1	1	1 / 1	x / x	m / m	g / g	± /)	X / X	M / M	G / G
0 0 1 0	2	2 / 2	n / n	. / .	= / =	@ / @	N / N	. / .	+ / +
0 0 1 1	3	3 / 3	u / u	v / v	f / f	# / #	U / U	V / V	F / F
0 1 0 0	4	5 / 5	e / e	' / '	p / p	% / %	E / E	" / "	P / P
0 1 0 1	5	7 / 7	d / d	r / r	; / ;	& / &	D / D	R / R	: / :
0 1 1 0	6	6 / 6	k / k	i / i	q / q	¢ / ¢	K / K	I / I	Q / Q
0 1 1 1	7	8 / 8	c / c	a / a	, / ,	* / *	C / C	A / A	, / ,
1 0 0 0	8	4 / 4	l / l	o / o	/ / /	$ / $	L / L	O / O	? / ?
1 0 0 1	9	O / O	h / h	s / s	y / y	) /)	H / H	S / S	Y / Y
1 0 1 0	10	z / z	① / IRS	② / VT	③ / RS	Z / Z	④ / IRS	⑤ / FF	⑥ / IRS
1 0 1 1	11	9 / 9	b / b	w / w	– / –	(/ (	B / B	W / W	— / —
1 1 0 0	12	PN1 / PN	BY1 / SUB	RES1 / RES	PF1 / PF	PN2 / DC2	BY2 / IFS	RES2 / IGS	PF2 / DC4
1 1 0 1	13	RS1 / IRS	LF1 / LF	NL1 / NL	HTI / HT	RS2 / DC1	LF2 / LF	NL2 / CR	HT2 / HT
1 1 1 0	14	UC1 / UC	EOB1 / EOB	BS1 / BS	LC1 / LC	UC2 / ENQ	EOB2 / EOB	BS2 / BS	LC2 / SI
1 1 1 1	15	EOT1 / EOT	PRE1 / PRE	IL1 / IL	DEL1 / DEL	EOT2 / EOT	PRE2 / DLE	IL2 / NUL	DEL2 / NUL

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 2605 JC, TMS 2605 NC
USASII, BAUDOT, SELECTRIC, EBCDIC CODE GENERATOR

FEBRUARY 1971

features

- 2048-bit capacity
- Static operation
- Maximum access time of 900 nsec
- Open-drain output buffers or double-ended buffers
- TTL compatible

description

The TMS 2605 JC/NC is a multiple-code generator designed to exercise and test keyboards, data communication links, and typing mechanisms, by generating the "Quick Brown Fox" message.

Six inputs of the TMS 2605 JC/NC are fed from a 6-bit binary count. The seventh and eighth inputs are used as code selects. The message can be generated in the four codes listed below:

I_7	I_8	CODE GENERATED
0	0	Selectric (7 bits plus parity)
1	0	EBCDIC (8 bits)
0	1	Baudot (5 bits)
1	1	ASCII (7 bits plus parity)

For normal operation of this device, Chip Enable (pin 14) must be at logic 1, I_9 (pin 13) at logic 1, and Mode Control (pin 15) at logic 0.

The outputs of the ROM correspond as follows:

ROM OUTPUT	SELECTRIC	EBCDIC	BAUDOT	ASCII
O_1	1	B_7	1	B_1
O_2	2	B_6	2	B_2
O_3	4	B_5	3	B_3
O_4	8	B_4	4	B_4
O_5	A	B_3	5	B_5
O_6	B	B_2	—	B_6
O_7	S	B_1	—	B_7
O_8	Parity	B_0	—	Parity

In typical applications the TMS 2605 JC/NC will be connected to a 6-bit binary counter. As the counter counts from 0 to 63, the following message will be generated in the selectric code.

THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG 1234567890 DE

electrical characteristics

All electrical and mechanical characteristics of this device are identical to those of the TMS 2600 JC/NC. "TMS 2605 JC" designates a unit mounted in a 24-pin hermetically sealed ceramic dual-in-line package. Mounted in a 24-pin plastic package the device is numbered "TMS 2605 NC." (See MOS/LSI packaging section.)

TMS 2605 JC, TMS 2605 NC
USASII, BAUDOT, SELECTRIC, EBCDIC CODE GENERATOR

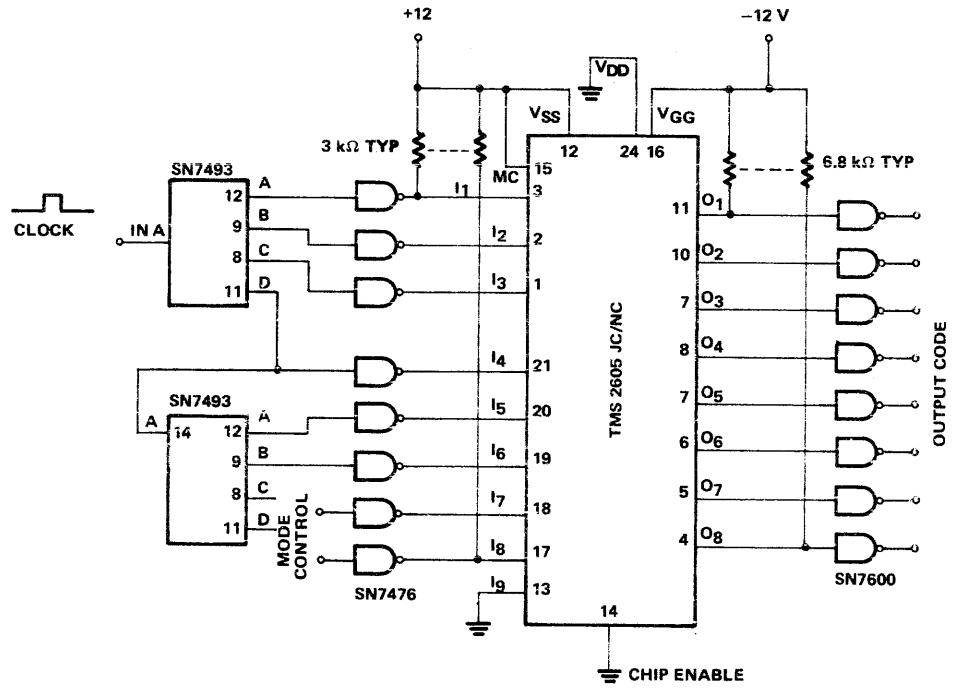
logic definition

Negative logic is assumed.

a) Logical 1 = most negative voltage

b) Logical 0 = most positive voltage

interface and typical applications data



NOTE: A BINARY COUNTER FURNISHES THE INPUTS FOR THE ROM. THE SELECTED CODE WORD APPEARS IN INVERTED FORM (NEGATIVE MOS LOGIC) AT THE OUTPUT OF THE ROM, AND IN INVERTED FORM (POSITIVE TTL LOGIC) AT THE OUTPUT OF THE TTL GATES.

truth table

The truth table of the TMS 2605 JC/NC is given for the 4 selected codes:

ADDRESS	CODE	I_7	I_8
0 – 63	Selectric	0	0
64 – 127	EBCDIC	1	0
128 – 191	Baudot	0	1
192 – 255	USASCII	1	1

14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

truth table (continued)

		O_8 PARITY	O_7 S	O_6 B	O_5 A	O_4 8	O_3 4	O_2 2	O_1 1	
			SELECTRIC							
0	IL1	0	1	0	1	0	0	0	0	NULL 64
1	NL	1	1	0	1	0	0	0	1	CR 65
2	IL1	0	1	0	1	0	0	0	0	CA 66
3	IL1	0	1	0	1	0	0	0	0	LF 67
4	T	1	0	1	0	1	1	1	1	T 68
5	H	1	0	1	0	0	1	1	0	H 69
6	E	0	0	1	0	1	0	1	1	E 70
7	SP	1	1	1	1	1	1	1	1	SP 71
8	Q	0	0	0	0	1	0	0	1	Q 72
9	U	1	0	1	0	1	1	0	0	U 73
10	I	1	0	0	1	1	0	0	1	I 74
11	C	0	0	1	0	1	0	0	0	C 75
12	K	1	0	1	0	1	0	0	1	K 76
13	SP	1	1	1	1	1	1	1	1	SP 77
14	B	0	0	1	0	0	1	0	0	B 78
15	R	1	0	0	1	1	0	1	0	R 79
16	O	0	0	0	1	0	1	1	1	O 80
17	W	0	0	0	1	0	1	0	0	W 81
18	N	0	0	1	0	1	1	0	1	N 82
19	SP	1	1	1	1	1	1	1	1	SP 83
20	F	0	0	0	0	1	1	0	0	F 84
21	O	0	0	0	1	0	1	1	1	O 85
22	X	0	0	1	0	1	1	1	0	X 86
23	SP	1	1	1	1	1	1	1	1	SP 87
24	J	0	0	0	0	1	1	1	1	J 88
25	U	1	0	1	0	1	1	0	0	U 89
26	M	0	0	0	0	1	1	1	0	M 90
27	P	1	0	0	0	1	0	1	1	P 91
28	S	1	0	0	1	0	1	1	0	S 92
29	SP	1	1	1	1	1	1	1	1	SP 93
30	O	0	0	0	1	0	1	1	1	O 94
31	V	1	0	0	1	1	1	0	0	V 95
32	E	0	0	1	0	1	0	1	1	E 96
33	R	1	0	0	1	1	0	1	0	R 97
34	SP	1	1	1	1	1	1	1	1	SP 98
35	T	1	0	1	0	1	1	1	1	T 99
36	H	1	0	1	0	0	1	1	0	H 100
37	E	0	0	1	0	1	0	1	1	E 101
38	SP	1	1	1	1	1	1	1	1	SP 102
39	L	0	0	1	0	0	1	1	1	L 103
40	A	0	0	0	0	1	1	0	0	A 104
41	Z	0	0	1	1	0	1	0	1	Z 105
42	Y	0	0	0	0	0	1	1	0	Y 106
43	SP	1	1	1	1	1	1	1	1	SP 107
44	D	1	0	1	0	1	0	1	0	D 108
45	O	0	0	0	1	0	1	1	1	O 109
46	G	1	0	0	0	1	1	1	0	G 110
47	SP	1	1	1	1	1	1	1	1	SP 111
48	1	0	1	1	1	1	1	1	0	1 112
49	2	0	1	1	1	1	1	0	1	2 113
50	3	1	1	1	1	1	1	0	0	3 114
51	4	0	1	1	1	0	1	1	1	4 115
52	5	0	1	1	1	1	0	1	1	5 116
53	6	1	1	1	1	1	0	0	1	6 117
54	7	1	1	1	1	1	0	1	0	7 118
55	8	0	1	1	1	1	0	0	0	8 119
56	9	0	1	1	1	0	1	0	0	9 120
57	0	1	1	1	1	0	1	1	0	0 121
58	SP	1	1	1	1	1	1	1	1	SP 122
59	D	1	0	1	0	1	0	1	0	D 123
60	E	0	0	1	0	1	0	1	1	E 124
61	SP	1	1	1	1	1	1	1	1	SP 125
62	DEL	1	1	0	0	0	0	0	0	DEL 126
63	DEL	1	1	0	0	0	0	0	0	DEL 127

		O_8	O_7 B_0	O_6 B_1	O_5 B_2	O_4 B_3	O_3 B_4	O_2 B_5	O_1 B_6	B_7
			EBCDIC							
0	NULL		1	1	1	1	1	1	1	1
1	CR		1	1	1	1	0	0	1	0
2	CA		1	1	1	1	0	0	1	0
3	LF		1	1	0	1	1	0	1	0
4	T		0	0	0	1	1	1	0	0
5	H		0	0	0	1	1	0	1	1
6	E		0	0	0	1	1	0	1	0
7	SP		1	0	0	1	1	1	1	1
8	Q		0	0	0	1	0	1	1	1
9	U		0	0	0	1	1	0	1	1
10	I		0	0	0	1	1	1	1	0
11	C		0	0	0	1	1	1	0	0
12	K		0	0	1	0	1	1	0	1
13	SP		1	0	1	1	1	1	1	1
14	B		0	0	1	1	1	1	0	1
15	R		0	0	1	1	0	1	1	0
16	O		0	0	1	1	0	1	1	1
17	W		0	0	1	1	0	0	0	1
18	N		0	0	1	1	0	1	1	0
19	SP		1	0	1	1	1	1	1	1
20	F		0	0	1	1	1	0	0	1
21	O		0	0	1	1	1	0	1	1
22	X		0	0	1	1	1	1	0	0
23	SP		1	0	1	1	1	1	1	1
24	J		0	1	0	1	1	1	1	0
25	U		0	1	0	1	1	0	1	1
26	M		0	1	0	1	1	1	0	0
27	P		0	1	0	1	1	1	1	0
28	S		0	1	1	0	1	1	0	0
29	SP		1	0	1	1	1	1	1	1
30	O		0	0	1	1	1	0	0	1
31	V		0	0	1	1	1	0	1	0
32	E		0	0	1	1	1	0	1	1
33	R		0	0	1	1	1	1	0	0
34	SP		1	0	1	1	1	1	1	1
35	T		0	0	1	1	1	1	0	0
36	H		0	0	1	1	0	1	1	1
37	E		0	0	1	1	1	0	1	1
38	SP		1	0	1	1	1	1	1	1
39	L		0	0	1	1	0	1	1	0
40	A		0	0	1	1	1	1	1	0
41	Z		0	0	1	1	0	1	1	0
42	Y		0	0	1	1	0	1	1	1
43	SP		1	0	1	1	1	1	1	1
44	D		0	0	1	1	1	0	1	1
45	O		0	0	1	1	1	1	1	1
46	G		0	0	1	1	1	1	0	0
47	SP		1	0	1	1	1	1	1	1
48	1		0	0	0	0	1	1	1	1
49	2		0	0	0	0	1	1	1	0
50	3		0	0	0	0	1	1	0	0
51	4		0	0	0	0	1	0	1	1
52	5		0	0	0	0	1	0	1	0
53	6		0	0	0	0	1	0	0	1
54	7		0	0	0	0	1	0	0	0
55	8		0	0	0	0	0	1	1	1
56	9		0	0	0	0	0	1	1	0
57	0		0	0	0	0	0	1	0	1
58	SP		1	0	1	1	1	1	1	1
59	D		1	0	0	1	1	1	0	1
60	E		1	0	0	1	1	1	1	0
61	SP		1	0	1	1	1	1	1	1
62	DEL		1	1	1	1	1	0	0	0
63	DEL		1	1	1	1	1	0	0	0

		O_8	O_7 —	O_6 —	O_5 —	O_4 5	O_3 4	O_2 3	O_1 2	1
			BAUDOT							
128	CR		1	1	1	1	0	1	1	1
129	CR		1	1	1	1	0	1	1	1
130	LF		1	1	1	1	1	1	0	1
131	LTR		1	1	1	0	0	0	0	0
132	T		1	1	1	0	1	1	1	1
133	H		1	1	1	0	1	0	1	1
134	E		1	1	1	1	1	1	1	0
135	SP		1	1	1	1	1	0	1	1
136	Q		1	1	1	0	1	1	0	0
137	U		1	1	1	1	1	0	0	0
138	I		1	1	1	1	1	0	0	1
139	C		1	1	1	1	0	0	0	1
140	K		1	1	1	1	0	0	1	0
141	SP		1	1	1	1	1	0	1	1
142	B		1	1	1	0	0	1	1	0
143	R		1	1	1	1	0	1	0	1
144	O		1	1	1	0	0	1	1	1
145	W		1	1	1	0	1	1	0	0
146	N		1	1	1	1	0	0	1	1
147	SP		1	1	1	1	1	0	1	1
148	F		1	1	1	1	0	0	1	0
149	O		1	1	1	0	0	1	1	1
150	X		1	1	1	0	0	0	1	0
151	SP		1	1	1	1	1	0	1	1
152	J		1	1	1	1	0	1	0	0
153	U		1	1	1	1	1	0	0	0
154	M		1	1	1	0	0	0	1	1
155	P		1	1	1	0	1	0	0	1
156	S		1	1	1	1	1	0	1	0
157	SP		1	1	1	1	1	0	1	1
158	O		1	1	1	0	0	1	1	1
159	V		1	1	1	0	0	0	0	1
160	E		1	1	1	1	1	1	1	0
161	R		1	1	1	1	0	1	0	1
162	SP		1	1	1	1	1	0	1	1
163	T		1	1	1	0	1	1	1	1
164	H		1	1	1	0	1	0	1	1
165	E		1	1	1	1	1	1	1	0
166	SP		1	1	1	1	1	0	1	1
167	L		1	1	1	0	1	1	0	1
168	A		1	1	1	1	1	1	0	0
169	Z		1	1	1	0	1	1	1	0
170	Y		1	1	1	0	1	0	1	0
171	SP		1	1	1	1	1	0	1	1
172	D		1	1	1	1	0	1	1	0
173	O		1	1	1	0	0	1	1	1
174	G		1	1	1	0	0	1	0	1
175	SP		1	1	1	1	1	0	1	1
176	FIG		1	1	1	0	0	1	0	0
177	1		1	1	1	0	1	0	0	0
178	2		1	1	1	0	1	1	0	0
179	3		1	1	1	1	1	1	1	0
180	4		1	1	1	1	0	1	0	1
181	5		1	1	1	0	1	1	1	1
182	6		1	1	1	0	1	0	1	0
183	7		1	1	1	1	1	0	0	0
184	8		1	1	1	1	1	0	0	1
185	9		1	1	1	0	0	1	1	1
186	0		1	1	1	0	1	0	0	1
187	SP		1	1	1	1	1	0	1	1
188	LTR		1	1	1	0	0	0	0	0
189	D		1	1	1	1	0	1	1	0
190	E		1	1	1	1	1	1	1	0
191	SP		1	1	1	1	1	0	1	1

		PARITY	O_8 B_7	O_7 B_6	O_6 B_5	O_5 B_4	O_4 B_3	O_3 B_2	O_2 B_1	O_1
			USASCII							
192	NULL		0	0	0	0	0	0	0	0
193	CR		0	1	1	1	0	0	1	0
194	CR		0	1	1	1	0	0	1	0
195	LF		1	1	1	1	0	1	0	1
196	T		0	0	1	0	1	0	1	1
197	H		1	0	1	1	0	1	1	1
198	E		1	0	1	1	0	1	1	0
199	SP		0	1	0	1	1	1	1	1
200	Q		0	0	1	0	1	1	1	0
201	U		1	0	1	0	1	0	1	0
202	I		0	0	1	1	0	1	1	0
203	C		0	0	1	1	1	1	0	0
204	K		1	0	1	1	0	1	0	0
205	SP		0	1	0	1	1	1	1	1
206	B		1	0	1	1	1	1	0	1
207	R		0	0	1	0	1	1	0	1
208	O		0	0	1	1	0	0	0	0
209	W		0	0	1	0	1	0	0	0
210	N		1	0	1	1	0	0	0	1
211	SP		0	1	0	1	1	1	1	1
212	F		0	0	1	1	1	0	0	1
213	O		0	0	1	1	0	0	0	0
214	X		0	0	1	0	1	1	1	1
215	SP		0	1	0	1	1	1	1	1
216	J		0	0	1	0	1	0	1	1
217	U		1	0	1	0	1	0	1	0
218	M		1	0	1	1	0	0	1	0
219	P		1	0	1	0	1	1	1	1
220	S		1	0	1	0	1	0	0	0
221	SP		0	1	0	1	1	1	1	1
222	O		0	0	1	1	0	0	0	0
223	V		1	0	1	0	1	0	0	1
224	E		0	0	1	1	1	0	1	0
225	R		0	0	1	0	1	1	0	1
226	SP		0	1	0	1	1	1	1	1
227	T		0	0	1	0	1	1	1	1
228	H		1	0	1	1	0	1	1	1
229	E		0	0	1	1	1	0	1	0
230	SP		0	1	0	1	1	1	1	1
231	L		0	0	1	1	0	0	1	1
232	A		1	0	1	1	1	1	1	0
233	Z		1	0	1	1	0	0	1	1
234	Y		1	0	1	0	1	0	1	0
235	SP		0	1	0	1	1	1	1	1
236	D		1	0	1	1	1	0	1	1
237	Q		0	0	1	1	0	0	0	0
238	G		1	0	1	1	1	0	0	1
239	SP		0	1	0	1	1	1	1	1
240	1		0	1	0	0	1	1	1	0
241	2		0	1	0	0	1	1	0	1
242	3		1	1	0	0	1	1	0	0
243	4		0	1	0	0	1	0	1	1
244	5		1	1	0	0	1	0	1	0
245	6		1	1	0	0	1	0	0	1
246	7		0	1	0	0	1	0	0	0
247	8		0	1	0	0	0	1	1	1
248	9		1	1	0	0	0	1	1	0
249	0		1	1	0	0	0	1	0	1
250	SP		0	1	0	1	1	1	1	1
251	D		1	0	1	1	1	0	1	1
252	E		0	0	1	1	1	0	1	0
253	SP		0	1	0	1	1	1	1	1
254	DEL		0	0	0	0	0	0	0	0
255	DEL		0	0	0	0	0	0	0	0

MOS
LSI

TMS 2700 JC, TMS 2700 JM, TMS 2700 NC
3072-BIT STATIC READ-ONLY MEMORY

FEBRUARY, 1971

features

- 256 x 12 organization
- Static operation
- Direct TTL compatibility
- Single-ended output buffers
- 28-lead dual-in-line package
- 3-line programmable chip select
- Chip enable
- 900-ns access time
- Low-threshold technology
- Full military temperature range (TMS 2700 JM)

description

The TMS 2700 is a static read-only memory with a capacity of 256 12-bit words. The device is constructed on a single monolithic chip, with MOS P-channel enhancement-mode low-threshold technology. Single-ended output buffers and a 3-line chip select allow the user to wire OR up to eight of these static ROMs, with no additional logic.

Programming of the memory content and output buffer configuration is accomplished by changing a single mask during device fabrication.

The TMS 2700 JC and JM are mounted in 28-pin ceramic dual-in-line packages. TMS 2700 NC is mounted in a 28-pin plastic package.

The temperature range is −25°C to +85°C for the TMS 2700 JC and the TMS 2700 NC, and −55°C to +125°C for the TMS 2700 JM.

logic definition

a) Logical 1 = most positive voltage

b) Logical 0 = most negative voltage

operation

The TMS 2700 series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip select) remains unchanged.

"Access time" is defined as the maximum time required for all outputs to reach the minimum logic 1 levels or maximum logic 0 levels with the correct data. This duration is measured from that point in time at which all address inputs and chip-select inputs are valid.

A disable input on the chip-enable input will cause the outputs to become open circuits. The memory will be enabled when the chip select is at logic 0.

14

The output buffers are single ended, open drain and allow the wired-OR connection.

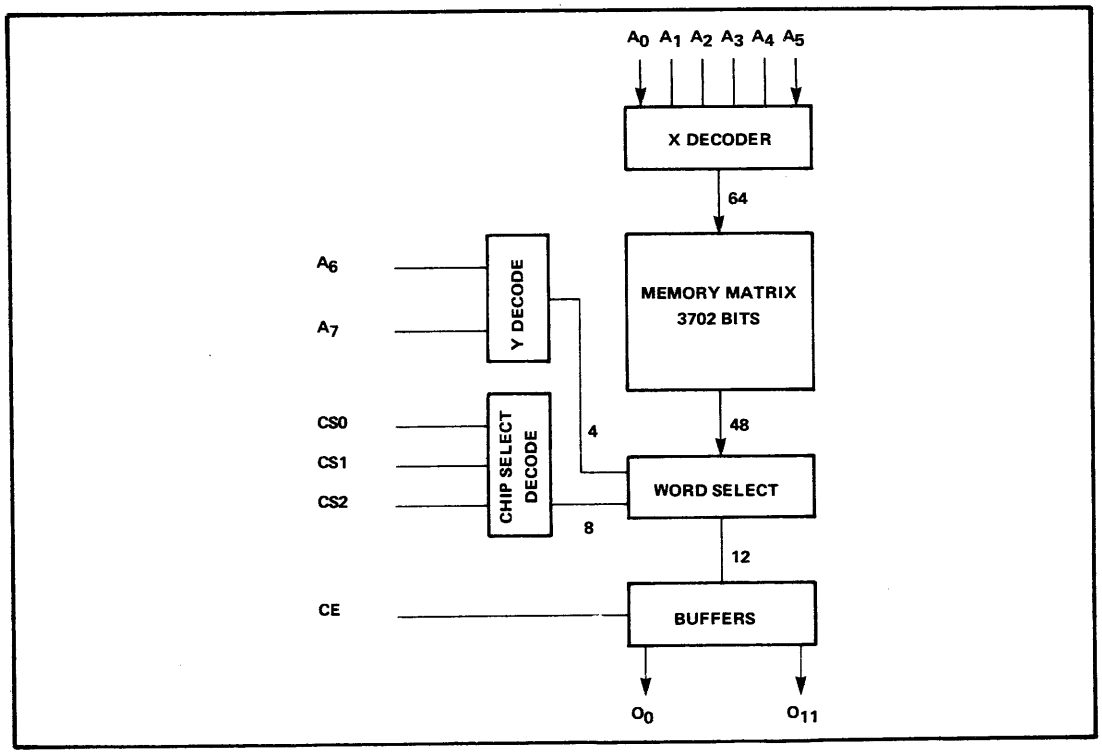
Three chip-select lines (CS_0, CS_1. CS_2) allow the user to wire OR up to eight TMS 2700 devices. The memory will be selected for one and only one chip-select word. This word is selected by the user and programmed in the memory when the memory content is programmed.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

data encoding

Information concerning memory content and chip select should be submitted on the TMS 2700 Software Package. Data to be stored in the memory should be entered on punched cards in the format described by the Software Package.

functional block diagram and pin configuration



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{GG} range (See Note 1) . . . . . −22 V to 0.3 V
Chip enable voltage range (See Note 1) . . . . . −22 V to 0.3 V
Address and chip select voltage range . . . . . −22 V to 0.3 V
Operating free-air temperature range
— TMS 2700 JC/NC . . . . . −25 V to 85 V
— TMS 2700 JM . . . . . −55 V to 125 V
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

14

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate supply V_{SS}	4.75	5.00	5.25	V
Gate supply V_{GG}	−13.5	−15	−16.5	V
Logic Levels				
Input HIGH level (1) V_{IH}	2.6		5.00	V
Input LOW level (0) V_{IL}			0.5	V

static electrical characteristics (under nominal operating conditions over operating temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL} Input Current	V_{IN} = 0 V			2	μA
Output Voltage Levels					
V_{OL} Output LOW level (0)	See Note 3				V
V_{OH} Output HIGH level (1)	I_{SOURCE} = 2.5 μA, V_{SS} = 4.75 V	2.4			V
V_{OL} Output LOW level (0)	Load 20 kΩ to −15 V (Note 4)	−13.5	−14.5		V
V_{OH} Output HIGH level (1)	Load 20 kΩ to −15 V (Note 4)	+3.5	+4.0		V
Power Supply Current Drain					
I_{SS} Substrate supply				32	mA
I_{GG} Gate supply				32	mA
P_D Power dissipation	Chip enable logic 1			350	mW
	Chip enable logic 0			650	mW

NOTES: 3. For an output logic 0, the output buffer transistor is Off and the impedance between the output terminal and V_{SS} is of several MΩ (leakage current <10 μA).

4. Recommended for MOS interface.

dynamic electrical characteristics

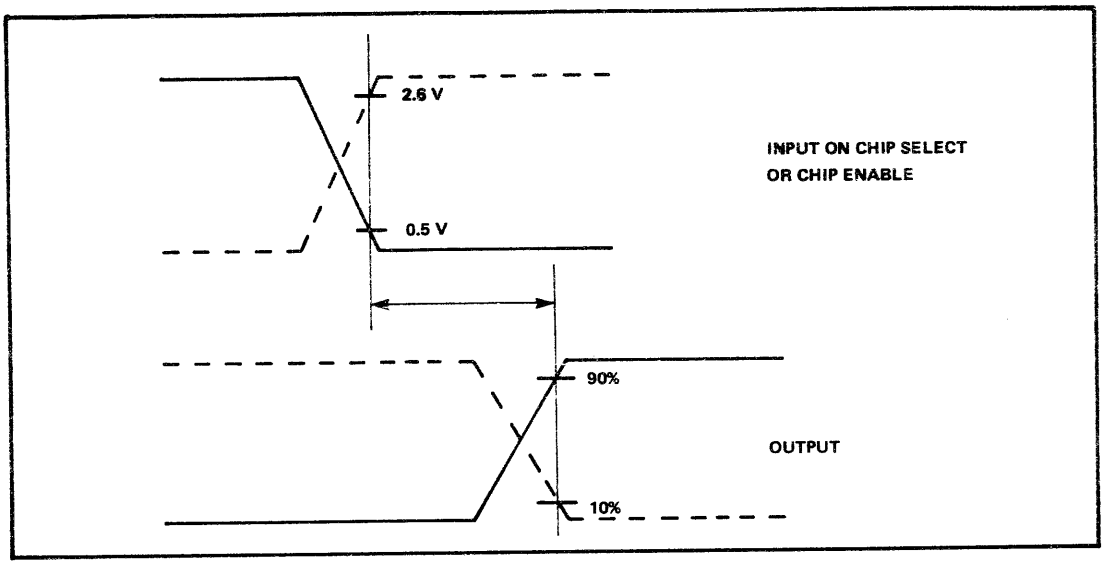
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Access Time (Notes 5 and 6)					
t_{AC}	−10°C to +70°C			900	ns
t_{AR}	−55°C to +125°C			1150	ns
Capacitance					
Input and chip select				5	pF

NOTES: 5. Load is one TTL gate plus a 20 pF capacitance. For final test purposes a worst-case TTL load is simulated by a 2.7-kΩ resistor and a 20 pF capacitance.

6. See timing diagram.

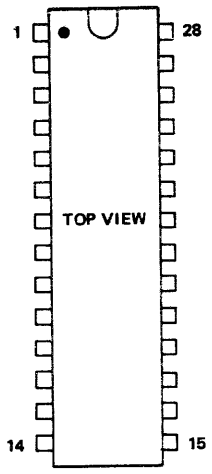
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

timing diagram and voltage waveforms



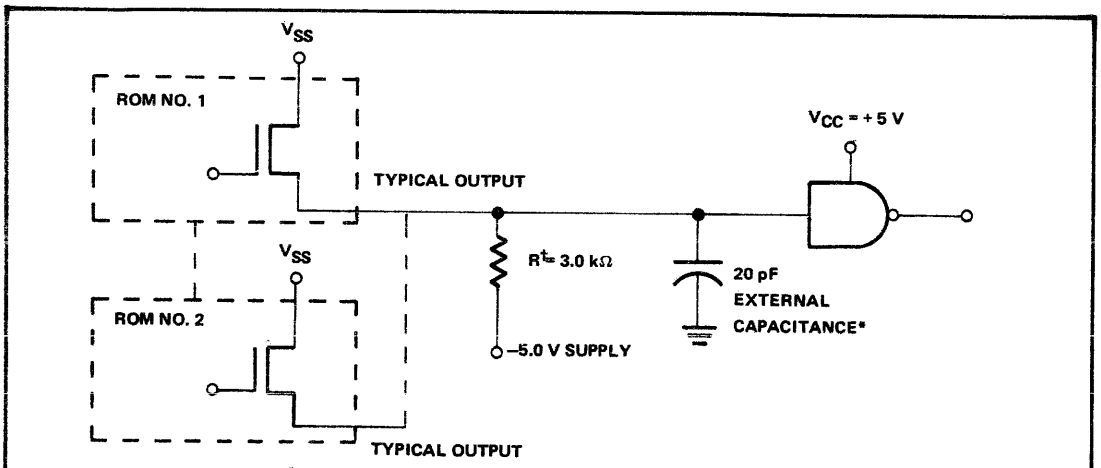
mechanical data and pin configuration

The TMS 2700 JC and TMS 2700 JM are mounted in 28-pin hermetically sealed dual-in-line packages consisting of a ceramic base, gold-plated cap, and gold-plated leads. The TMS 2700 NC is mounted in a 28-pin plastic dual-in-line package. The packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	O_{10}	15	CS_1
2	O_9	16	CE
3	O_8	17	A_5
4	O_7	18	A_4
5	O_6	19	A_3
6	O_5	20	A_2
7	O_4	21	A_1
8	O_3	22	A_0
9	O_2	23	A_6
10	O_1	24	A_7
11	O_0	25	No connection
12	V_1	26	V_{SS}
13	CS_3	27	No connection
14	CS_2	28	O_{11}

TTL interface circuit



* THE OUTPUT CAPACITANCE IS NOT PART OF THE TTL INTERFACE. IT IS USED IN SWITCHING CIRCUITS TO SIMULATE PARASITIC CAPACITANCE LOADING IN ACTUAL USE (BOARD, INTERCONNECT, ETC.).

† ALTERNATE RESISTOR VALUE – 6.8 kΩ to –15 V SUPPLY.

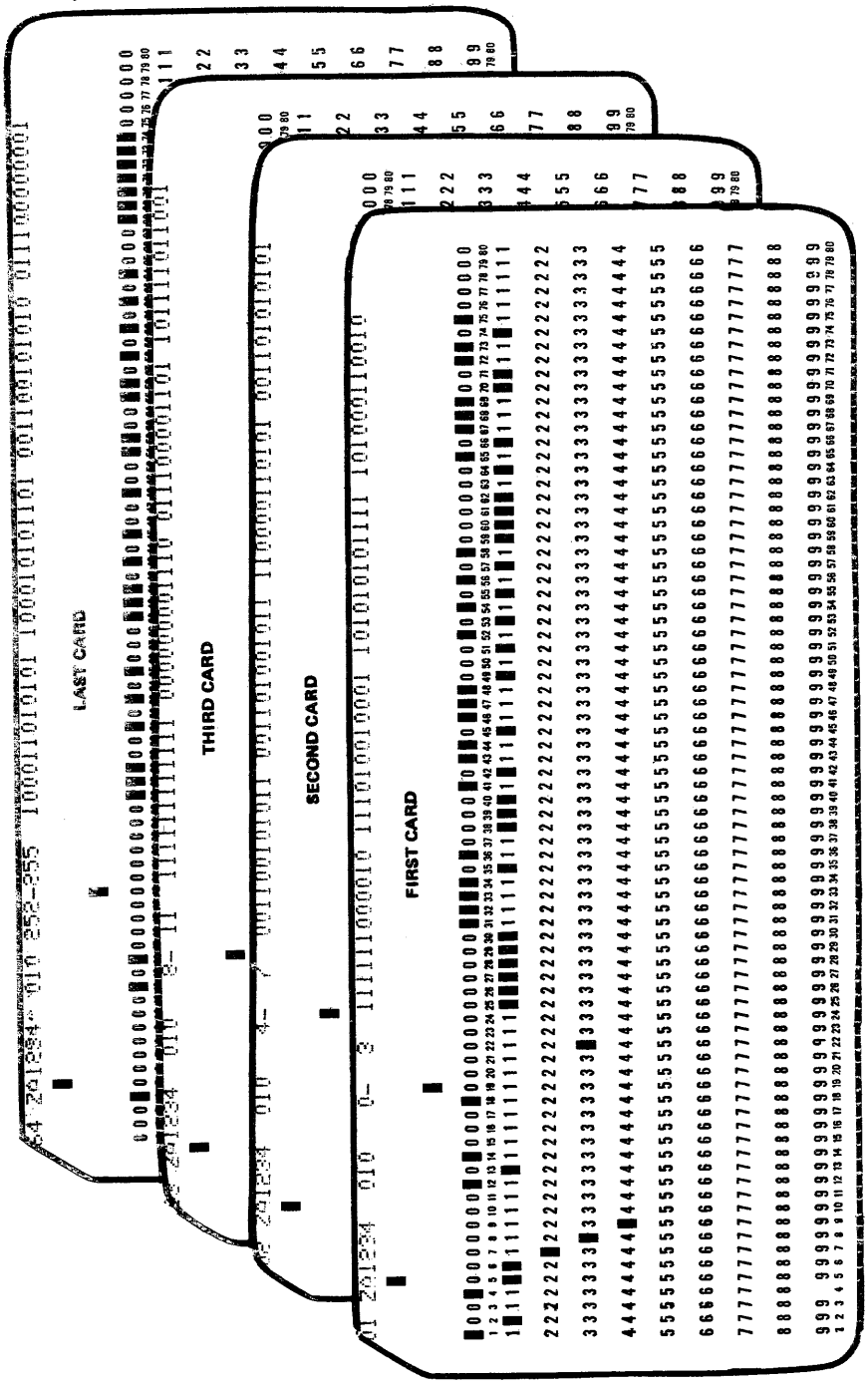
SOFTWARE PACKAGE

Programming information for the TMS 2700 should be transmitted to TI in the form of a DECK OF 64 STANDARD 80-COLUMN COMPUTER CARDS, accompanied by a listing of these cards. This method eliminates many chances for error and guarantees the fastest delivery schedule of ROMs. Upon receipt of each deck, a computer run will be made and a copy of the computer-generated truth table sent back to the customer. This copy should be checked carefully. If any errors are discovered, TI must be notified immediately so that work can be stopped and the necessary adjustments made.

Each card in the data deck describes the outputs for four input addresses. All addresses must have their outputs defined. The addresses must also be placed in consecutive order. Cards should be punched according to the following format.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 2700 — first, second, third and last cards



data card format

COLUMN	
1–2	Punch the sequential card number (01 through 64).
3	Blank
4–9	Punch the Z identification number supplied by TI MOS Marketing (2 letters, 4 numbers).
10	Blank (a space for the revision letter if necessary)
11	Blank
12–14	Punch chip-select logic CS0, CS1, CS2. A "1" for a logical 1 and a "0" for a logical 0.
15	Blank
16–18	Punch a right-justified integer representing the binary input address (0-255) for the first set of outputs described on the card
19	Punch a "–" (minus sign)
20–22	Punch a right-justified integer representing the binary input address for the last set of outputs described on the card.
23–24	Blank
25–75	Punch a description of the output sets selected for the range of input addresses specified on the card. A "1" for a logical 1 and a "0" for a logical 0. Each card will describe 4 output sets.
25–36	Punch the outputs desired for O_{11}, O_{10}, O_9, O_8, O_7, O_6, O_5, O_4, O_3, O_2, O_1, O_0, in that order, for the first address specified on the card.
38–49	Punch the outputs desired for the second address.
51–62	Punch the outputs desired for the third address.
64–75	Punch the outputs desired for the fourth address.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 2800 JC, TMS 2800 NC
1024-BIT STATIC READ-ONLY MEMORY

JANUARY, 1971

features

- 1024-bit capacity
- Static operation
- Maximum access time under 1 microsecond
- Open-drain output buffers or double-ended buffers
- TTL compatible
- 16-pin dual-in-line package

description

The TMS 2800 JC/NC series is a family of static read-only memories, each having a capacity of 1024 bits.

Programming of the memory content and output buffer configuration is accomplished by changing a single mask during device fabrication.

A chip-select input is available.

The memory contents consist of 256 words of four bits.

Two types of output buffers are available:

- Single-Ended (open drain)

  Designed for driving TTL, this output has one MOS device with its drain at the output and its source at chip ground.

- Double-Ended

  Designed for driving the inputs to other MOS integrated circuits and devices, this version has its own MOS load resistor provided internally. It requires no additional external circuitry.

"TMS 2800 JC" designates a unit mounted in a 16-pin hermetically sealed ceramic dual-in-line package, and "TMS 2800 NC" is used for a unit mounted in a 16-pin plastic package.

logic definition

Negative logic is assumed.

a) Logical 1 = most negative voltage

b) Logical 0 = most positive voltage

operation

The TMS 2800 JC/NC series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip select) remains unchanged. The V_{GG} supply may be clocked to reduce power consumption without affecting access times.

Access time is defined as the time between a change of data on any logic input or chip-select line and the change of data on the output of a TTL gate. (See timing diagram)

— continued

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operation (continued)

A logical 0 on the chip select input will cause the outputs to become open circuits on the "single-ended" (open-drain) type output buffer and will cause the outputs to go to V_{DD} on the double-ended (push-pull) type output buffer.

The number of words per output is increased by hardwiring together the outputs of different devices. Note that, when using the hardwired output technique, all devices should have single-ended buffers. Hardwiring outputs performs the AND function in negative logic.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage ranges (See Note 1) . . . . . −30 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−9	−12	−22	V
Supply voltage V_{GG}	−18	−24	−29	V
Input, chip select logic 1	−8	−12	−22	V
Input, chip select logic 0	+0.3	0	−3	V
Input pulse width	550			ns

The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V). Larger power supplies (e.g., +14 V, −14 V) may be used.

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

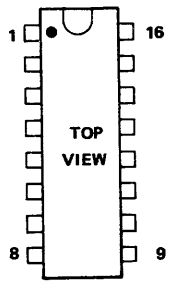
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{out(0)}$	Logical 0 output current (Note 1)	−12 V applied	3	7		mA
$I_{out(1)}$	Logical 1 output current (Note 1)	−12 V applied			10	μA
$Z_{out(1)}$	Logical 1 output impedance (Note 2)	V applied = V_{DD} + 3		18	25	kΩ
$Z_{out(0)}$	Logical 0 output impedance (Note 4)	V applied = V_{SS} −3		0.8	1.1	kΩ
$V_{out(1)}$	Logical 1 output voltage (Note 2)	R_L = 1 mΩ	−9		−12	V
$V_{out(0)}$	Logical 0 output voltage (Note 2)	R_L = 1 mΩ	0		−2.0	V
t_{A1}	Access time (Note 3)	See switching circuit		600	900	ns
t_{A2}	Access time (Note 3)	See switching circuit		620	900	ns
P_d	Power dissipation (Note 2)	All outputs at Logical 0		170		mW
I_L	Input leakage current	−12 V applied to input			1	μA
C_{in}	Input capacitance	V_{in} = 0 V, f = 1 MHz		5		pF
I_{DD}	Drain current	All outputs @ Logical 0		15		mA
I_{GG}				1.0		μA

NOTES: 1. Open-drain buffer
2. Push-pull buffer
3. See switching diagram
4. Either open-drain or push-pull configuration

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

mechanical data and pin configuration

This device is available in both a 16-pin hermetically sealed ceramic dual-in-line package (TMS 2800 JC) and a 16-pin plastic package (TMS 2800 NC). These packages are designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)

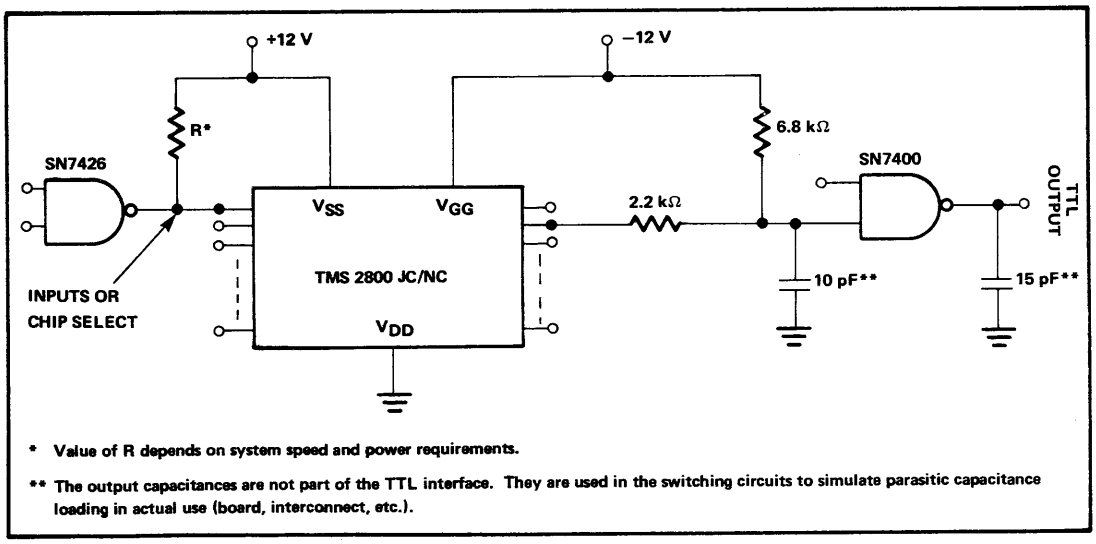


PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	A_3	9	A_8
2	A_2	10	CS
3	A_1	11	V_{GG}
4	B_1	12	A_7
5	B_2	13	A_6
6	B_3	14	A_5
7	B_4	15	A_4
8	V_{SS}	16	V_{DD}

A – input
B – output
V_{SS} – substrate

V_{DD} – drain supply
V_{GG} – gate supply

switching circuit and TTL interface

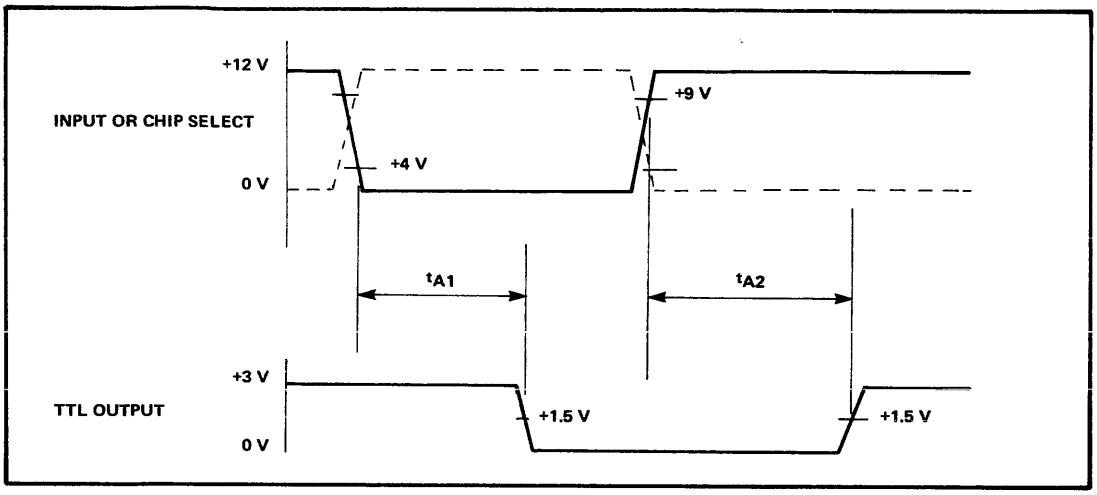


* Value of R depends on system speed and power requirements.

** The output capacitances are not part of the TTL interface. They are used in the switching circuits to simulate parasitic capacitance loading in actual use (board, interconnect, etc.).

14

switching diagram



SOFTWARE PACKAGE

input format

Programming information for the TMS 2800 JC/NC should be transmitted to TI in the form of a DECK of 22 STANDARD 80-COLUMN COMPUTER CARDS, accompanied by a listing of these cards. This method eliminates many chances for error and guarantees the fastest delivery schedule of ROMs. Upon receipt of each deck, a computer run will be made and a copy of the computer-generated truth table sent back to the customer. This copy should be checked carefully. If any errors are discovered, TI should be notified immediately so that work can be stopped and the necessary adjustments made.

Information on the buffer option desired will be transmitted on a special form supplied by TI.

Each card in the data deck describes the outputs for twelve input addresses. All addresses must have their outputs defined. The addresses must also be placed in consecutive order. Cards should be punched according to the following format.

data card format

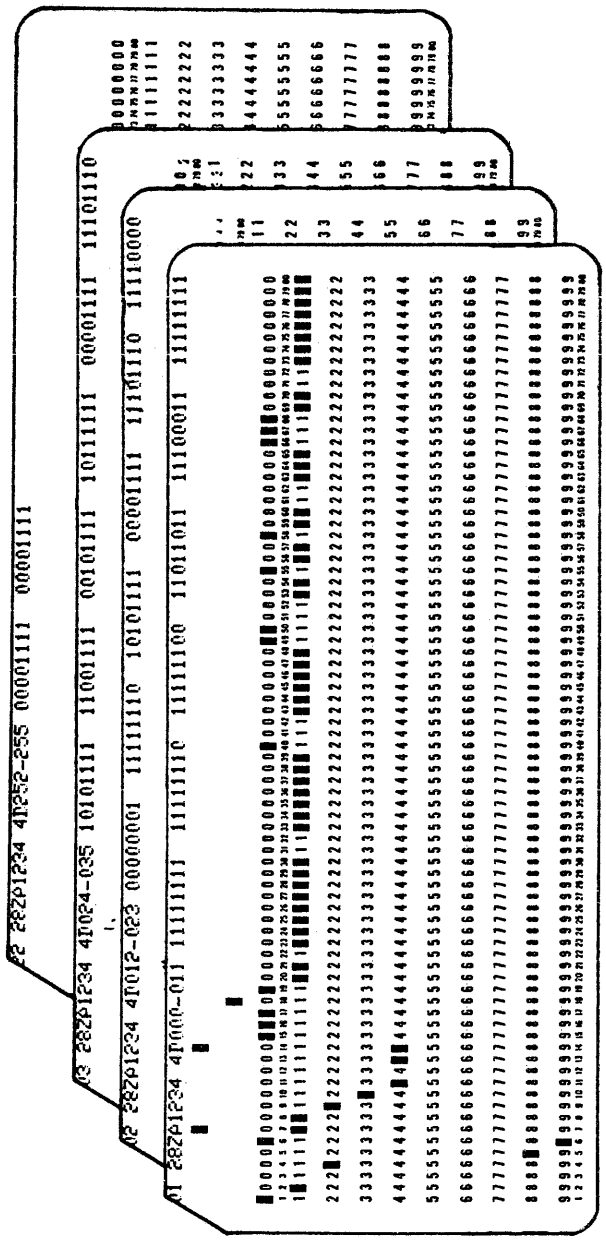
Column	
1-2	Punch the sequential card number (01 through 22)
3	Blank
4-5	Punch a "28" to signify TMS 2800 JC/NC
6-11	Punch the Z identification number supplied by TI MOS Marketing (2 letters, 4 numbers)

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

data card format (continued)

Column	
12	Blank (a space for the revision letter if necessary)
13	Punch a "4" to signify four outputs
14	Punch a "D" for open-drain type output buffers or punch a "P" for push-pull type output buffers
15-17	Punch a right-justified integer representing the binary input address (0-255) for the first set of outputs described on the card
18	Punch a "–" (minus sign)
19-21	Punch a right-justified integer representing the binary input address for the last set of outputs described on the card
22	Blank
23-80	Punch a description of the output sets selected for the range of input addresses specified on the card. A "1" for a logical 1 and a "0" for a logical 0. Each card will describe 12 output sets. The 22nd card will contain only 4 output sets.
23-26	Punch the outputs desired for B_4, B_3, B_2, B_1 in that order, for the first address specified on the card.
27-30	Punch the outputs desired for the second address
33-36	Punch the outputs desired for the third address
37-40	Punch the outputs desired for the fourth address
43-46	Punch the outputs desired for the fifth address
47-50	Punch the outputs desired for the sixth address
53-56	Punch the outputs desired for the seventh address
57-60	Punch the outputs desired for the eighth address
63-66	Punch the outputs desired for the ninth address
67-70	Punch the outputs desired for the tenth address
73-76	Punch the outputs desired for the eleventh address
77-80	Punch the outputs desired for the twelfth address

TMS 2800 JC — first, second, third and last cards



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 2801 JC, TMS 2801 NC
EIGHT-LEVEL PRIORITY ENCODER

FEBRUARY, 1971

features

- 1024-bit capacity
- static operation
- maximum access time under 1 microsecond
- open-drain output buffers
- TTL compatible

description

The TMS 2801 JC/NC is a programmed TMS 2800 JC/NC. All electrical and mechanical characteristics of the TMS 2800 JC/NC apply (See MOS product brochure CB-126) to this 1024-bit MOS read-only memory.

Programmed as a priority encoder, the TMS 2801 JC/NC generates an output code according to the priority levels present at its inputs. Each input corresponds to a priority level. The highest priority line that is "true" produces its characteristic output code, regardless of the state of the lower priority input lines. Although one TMS 2800 JC/NC has only enough inputs for eight priority levels, the chip-select input can be used to cascade devices for as many priority levels as necessary.

"TMS 2801 JC" designates a unit mounted in a 16-pin hermetically sealed ceramic dual-in-line package. A unit mounted in a 16-pin plastic dual-in-line package is numbered "TMS 2801 NC".

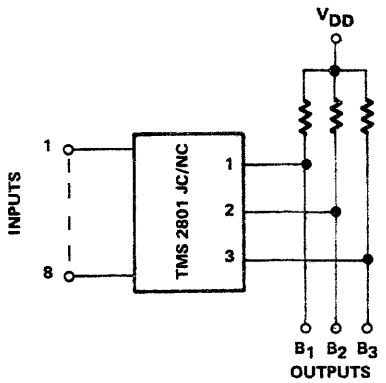
logic definition

Positive logic is assumed.

a) Logical 1 = most positive voltage

b) Logical 0 = most negative voltage

TMS 2801 JC/NC truth table for 8 priority levels

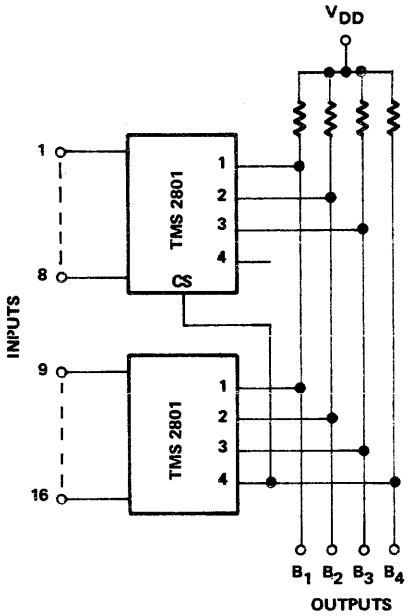


MOST SIGNIFICANT INPUT AT A LOGICAL 1	OUTPUTS		
	B_3	B_2	B_1
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

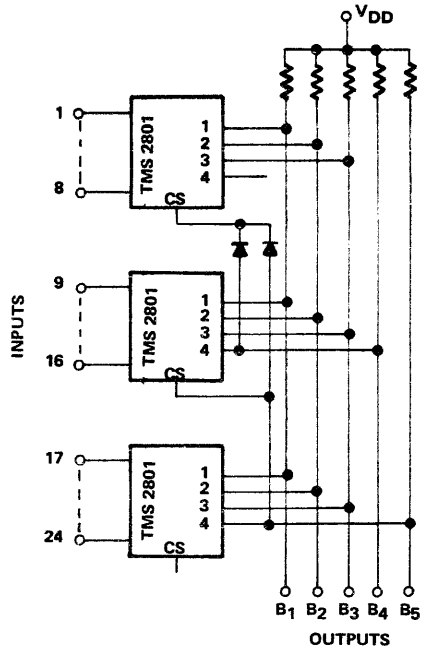
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

extension to 16-level priority encoder



MOST SIGNIFICANT INPUT AT A LOGICAL 1	OUTPUTS			
	B_4	B_3	B_2	B_1
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1
7	0	1	1	0
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1
11	1	0	1	0
12	1	0	1	1
13	1	1	0	0
14	1	1	0	1
15	1	1	1	0
16	1	1	1	1

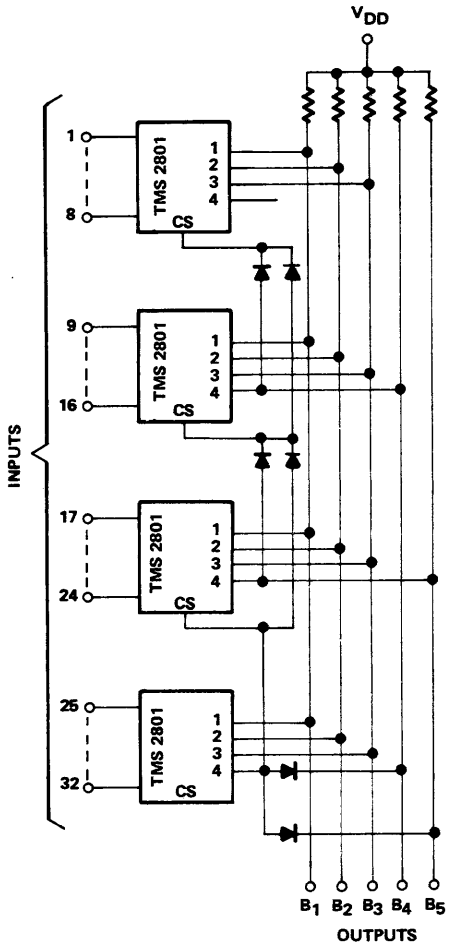
extension to 24-level priority encoder



MOST SIGNIFICANT INPUT AT A LOGICAL 1	OUTPUTS				
	B_5	B_4	B_3	B_2	B_1
1	0	0	0	0	0
2	0	0	0	0	1
3	0	0	0	1	0
4	0	0	0	1	1
5	0	0	1	0	0
6	0	0	1	0	1
7	0	0	1	1	0
8	0	0	1	1	1
9	0	1	0	0	0
10	0	1	0	0	1
11	0	1	0	1	0
12	0	1	0	1	1
13	0	1	1	0	0
14	0	1	1	0	1
15	0	1	1	1	0
16	0	1	1	1	1
17	1	0	0	0	0
18	1	0	0	0	1
19	1	0	0	1	0
20	1	0	0	1	1
21	1	0	1	0	0
22	1	0	1	0	1
23	1	0	1	1	0
24	1	0	1	1	1

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

extension of 32-level priority encoder



MOST SIGNIFICANT INPUT AT A LOGICAL 1	OUTPUTS				
	B_5	B_4	B_3	B_2	B_1
1	0	0	0	0	0
2	0	0	0	0	1
3	0	0	0	1	0
4	0	0	0	1	1
5	0	0	1	0	0
6	0	0	1	0	1
7	0	0	1	1	0
8	0	0	1	1	1
9	0	1	0	0	0
10	0	1	0	0	1
11	0	1	0	1	0
12	0	1	0	1	1
13	0	1	1	0	0
14	0	1	1	0	1
15	0	1	1	1	0
16	0	1	1	1	1
17	1	0	0	0	0
18	1	0	0	0	1
19	1	0	0	1	0
20	1	0	0	1	1
21	1	0	1	0	0
22	1	0	1	0	1
23	1	0	1	1	0
24	1	0	1	1	1
25	1	1	0	0	0
26	1	1	0	0	1
27	1	1	0	1	0
28	1	1	0	1	1
29	1	1	1	0	0
30	1	1	1	0	1
31	1	1	1	1	0
32	1	1	1	1	1

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4100 JC, TMS 4100 NC
SERIES CHARACTER GENERATOR

FEBRUARY, 1971

features

- Static operation
- 2240-bit capacity
- 64 Characters of 35 bits (5 x 7) or
- 32 Characters of 70 bits (5 x 14)
- TTL compatible
- 700-ns maximum access time
- 7-bit input address
- Single-ended open-drain output buffers

description

The TMS 4100 JC/NC series is a family of MOS read-only memories, each with a capacity of 2240 bits. Two organizations are available:

1) 64 words of 35 bits (5 x 7)

2) 32 words of 70 bits (5 x 14)

The memory is organized to function primarily as a character generator. The seven outputs represent a column in a 5 x 7 dot matrix.

The output word appears as a 5-word sequence on each of the output lines. Sequence is controlled by 5 strobe lines (column select), which feed directly into the buffer section of the memory. By enabling the first strobe line, the first group of 7 bits (first column) is obtained at the output. Then the second, third, fourth, and fifth strobe lines are enabled. The column select can remain fixed while the character address changes, or the character address may remain fixed while the column select changes.

The decoder will accept a 7-bit parallel input. Because only six bits are required in order to decode the 64 input words, the seventh bit may be used as a chip enable. If the memory is organized as 32 words of 70 bits, it is possible to have two chip-enable lines.

The TMS 4100 JC/NC series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip select) remains unchanged. The V_{GG} supply may be clocked to reduce power consumption without affecting access times.

Output buffers are single ended, open drain and allow the wired-OR connection.

The number of words per output is increased by hardwiring together the outputs of different devices. Hardwiring outputs perform the AND function in negative logic.

"TMS 4100 JC" designates a unit mounted in a 28-pin hermetically sealed ceramic dual-in-line package, and "TMS 4100 NC" is the part number for the unit mounted in a 28-pin plastic package.

logic definition

Negative logic is assumed for all inputs.

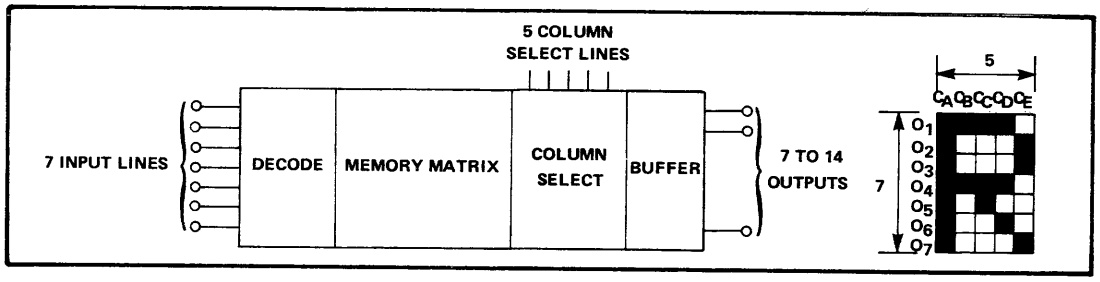
a) Logic 1 = most negative voltage (−14 V)

b) Logic 0 = most positive voltage (0 V)

An output dot is defined as the "on" state of the output MOS transistor and an output blank as the "off" state.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage ranges (See Note 1) . . . . . −30 V to 0.5 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−12	−14	−16	V
Supply voltage V_{GG}	−24	−28	−29	V
Input, column select and enable logic 1	−9	−14	−16	V
Input, column select and enable logic 0	+0.3	0	−3	V

Maximum speed of operation will be obtained when operating at the nominal values. The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V).

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

	PARAMETER (See Note 1)	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{(1)}$	Output Blank Current (Note 2)	−14 V applied to output			10	μA
$I_{(0)}$	Output Dot Current (Note 2)	−14 V applied to output	1	2		mA
$I_{(0)}$	Output Dot Current (Note 2)	V_{DD} = −12 V, V_{GG} = −24 V, −12 V applied to output	0.5	1		mA
$V_{(0)}$	Output Voltage for a Dot (Note 2)	I_O = 0.5 mA		−1.3	−2.8	V
$V_{(1)}$	Output Voltage for a Dot (Note 2)	I_O = 1 mA		−2.5	−6	V
	Input and Column Select Leakage Current	−14 V applied to input			1	μA
I_{DD}	Drain Supply Current			14	25	mA
I_{GG}	Gate Supply Current				1	mA
	Power Dissipation			250	400	mW
	Address Input Capacitance			6	15	pF

NOTES: 1. These voltage values are with respect to network ground terminal (V_{SS}).
2. An output dot is defined as the On state of the MOS output transistor. An output blank is defined as the Off state.

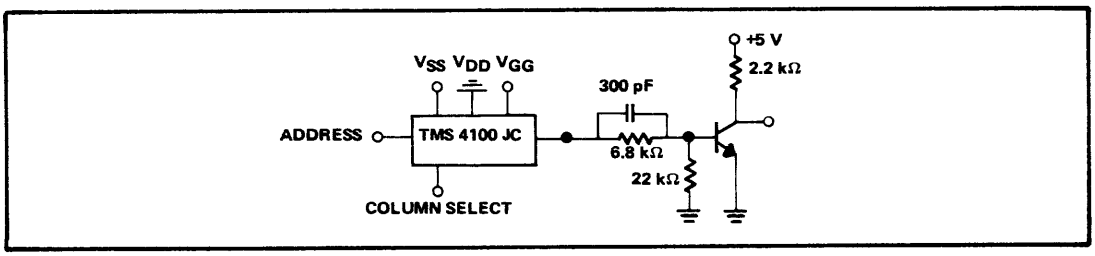
14

switching characteristics (at nominal operating conditions and 25°C unless otherwise noted)

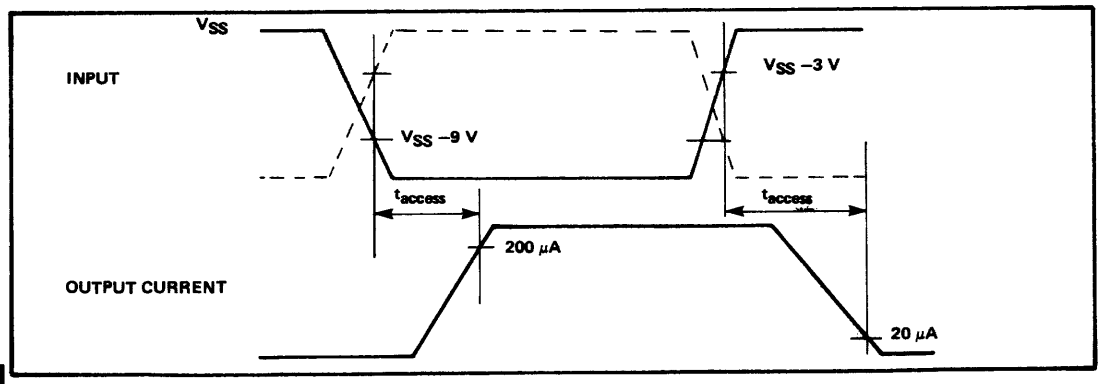
PARAMETER (Refer to Switching Diagram)	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Character Access Time, Bipolar Load			400	700	ns
Character Access Time, Bipolar Load	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		500	700	ns
Column-Select Access Time Bipolar Load			150	300	ns
Column-Select Access Time, Bipolar Load	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		200	350	ns
Character Access Time, Low Power TTL Load			500	850	ns
Character Access Time, Low Power TTL Load	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		600	950	ns
Column-Select Access Time, Low Power TTL Load			200	400	ns
Column-Select Access Time, Low Power TTL Load	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		300	500	ns

switching circuit and switching diagram

a) Bipolar load



address or column-select input voltage

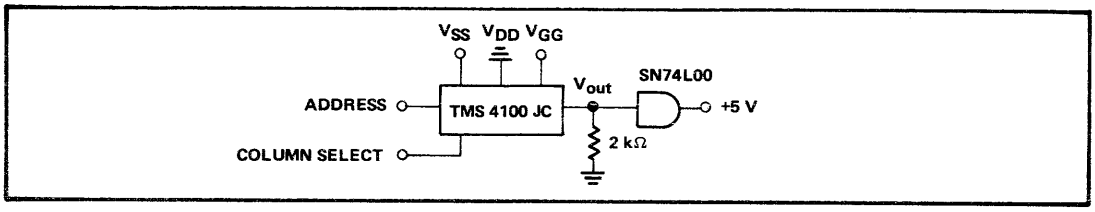


14

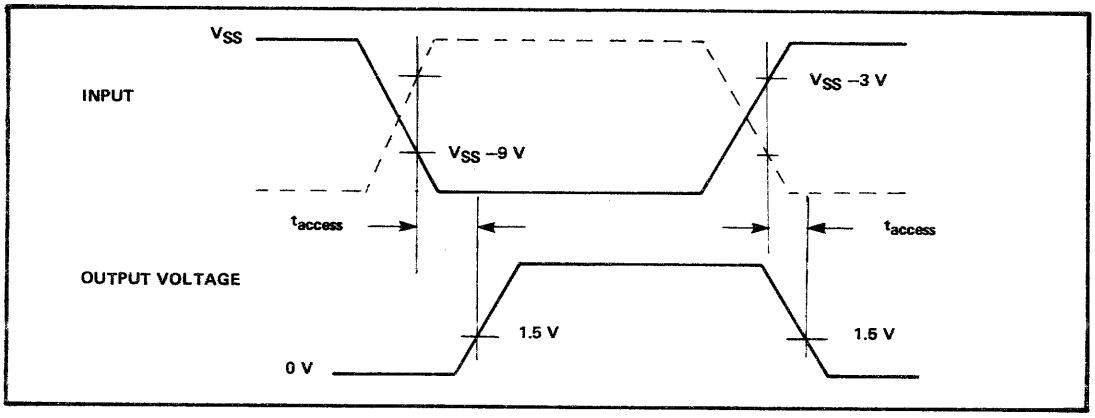
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching circuit and switching diagram (continued)

b) Low power TTL load



address or column select voltage



custom programmed devices

The TMS 4100 JC/NC series is programmed at the gate-oxide stage of manufacturing. Programming charges are reduced to a minimum because only one mask per unique design need be created (gate oxide removal mask). All other processing steps remain the same for all devices. Options available to the customer during programming are:

- memory organization
- character format
- enable logic polarity (or permanently enabled)

The encoding of the gate mask is done by computer to provide a fast, error-free encoding process.

Standard encoding sheets are used. These encoding sheets (SOFTWARE PACKAGE) are available from the TI sales office.

mechanical data

This device is available in both a 28-pin hermetically sealed ceramic dual-in-line package (TMS 4100 JC) and a 28-pin plastic package (TMS 4100 NC). These packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

14

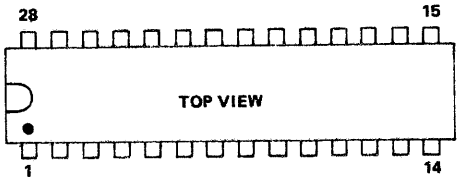
pin configuration

Depending on the organization of the memory, three pin configurations may be used.

Package Pin Configuration, TMS 4100 JC/NC

PIN NO.	CONFIGURATION A — TOTAL OUTPUTS— 7 OR FEWER	CONFIGURATION B — TOTAL OUTPUTS— MORE THAN 7, FEWER THAN 14	CONFIGURATION C — TOTAL OUTPUTS— 14
1	O_1	O_1	O_1
2	NC	O_2	O_2
3	O_2	O_3	O_3
4	NC	O_4	O_4
5	O_3	O_5	O_5
6	NC	O_6	O_6
7	O_4	O_7	O_7
8	NC	O_8	O_8
9	O_5	O_9	O_9
10	NC	O_{10}	O_{10}
11	O_6	O_{11}	O_{11}
12	NC	O_{12}	O_{12}
13	O_7	O_{13}	O_{13}
14	V_{DD}	V_{DD}	O_{14}
15	V_{GG}	V_{GG}	V_{DD}
16	I_6	I_6	V_{GG}
17	V_{SS}	V_{SS}	I_6
18	C_A	C_A	V_{SS}
19	C_B	C_B	C_A
20	C_C	C_C	C_B
21	C_D	C_D	C_C
22	C_E	C_E	C_D
23	I_5	I_5	C_E
24	I_4	I_4	I_5
25	I_3	I_3	I_4
26	I_2	I_2	I_3
27	I_1	I_1	I_2
28	I_7	I_7	I_1

NC – NOT CONNECTED O – OUTPUT I – INPUT
C – COLUMN SELECT



standard devices

Because certain codes are widely used, TI has created a series of standard devices that are available off the shelf and for which there is no coding charge. The most widely used standard device is: TMS 4103 JC/NC USASCII CODE (See attached character format).

14

Organization:
- 64-Character Storage
- 35-Bit Character Matrix
- 6-Parallel Character-Address Input
- Chip Enabled by Logic 1 Applied to I_7

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

standard devices (continued)

Other Available Standard Circuits:

- TMS 4177 JC/NC and TMS 4178 JC/NC. These two devices are used as a unit to implement a 7 x 10 row output character generator. The two devices are wired OR and are scanned in succession.

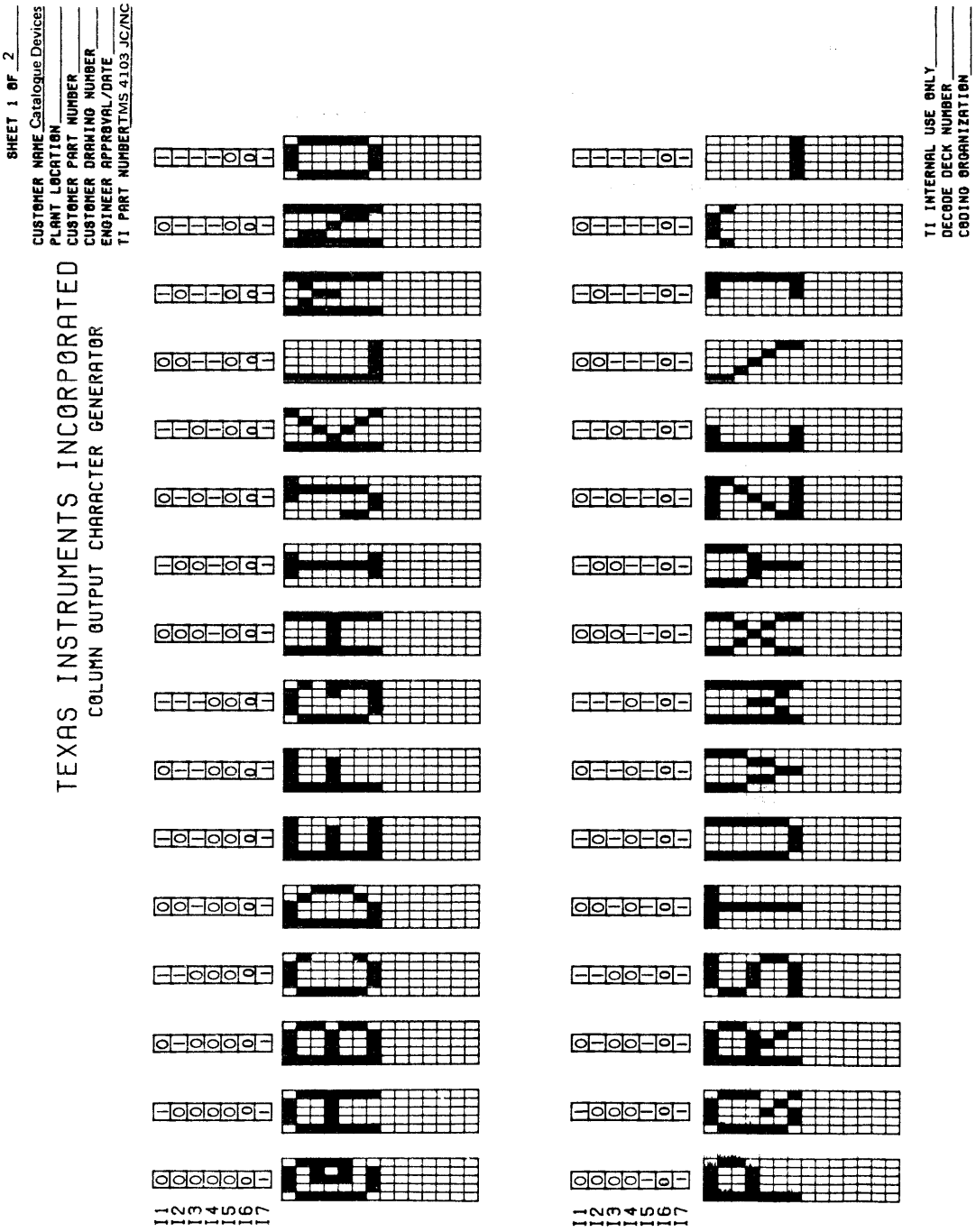
  - USASCII Code
  - 64-Character Storage
  - 7-Bit Parallel Input

  See attached character format.

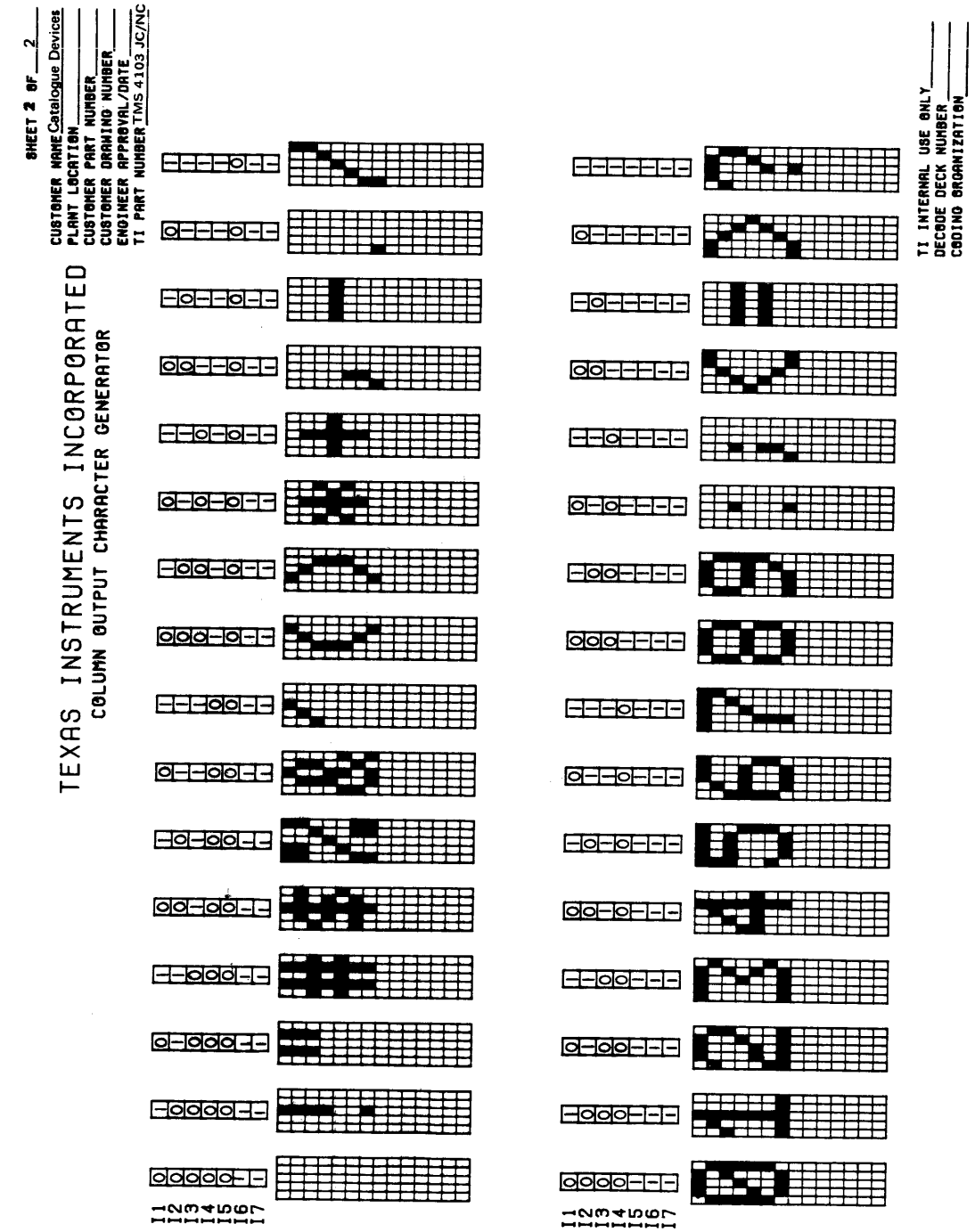
- TMS 4179 JC/NC

  - EBCDIC Code
  - 64-Character Storage
  - 7-Bit Parallel Input

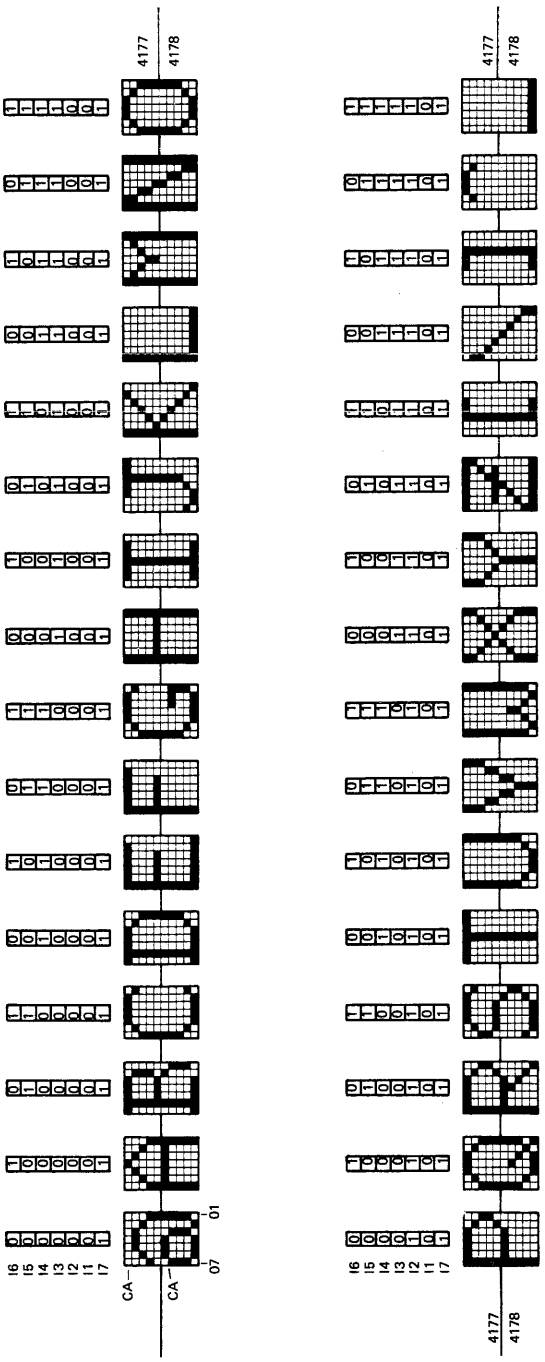
  See attached character format.



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

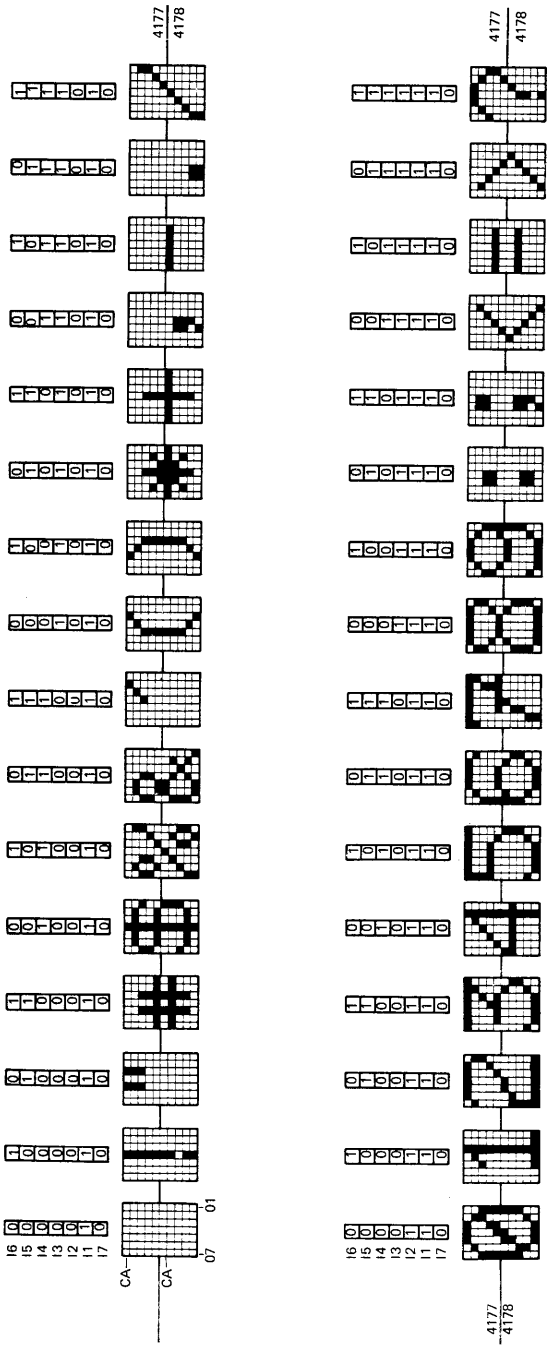

SHEET 2 OF 2
CUSTOMER NAME Catalogue Devices
PLANT LOCATION
CUSTOMER PART NUMBER
CUSTOMER DRAWING NUMBER
ENGINEER APPROVAL/DATE
TI PART NUMBER TMS 4103 JC/NC
TEXAS INSTRUMENTS INCORPORATED
COLUMN OUTPUT CHARACTER GENERATOR
TI INTERNAL USE ONLY
DECODE DECK NUMBER
CODING ORGANIZATION
I1 I2 I3 I4 I5 I6 I7
I1 I2 I3 I4 I5 I6 I7

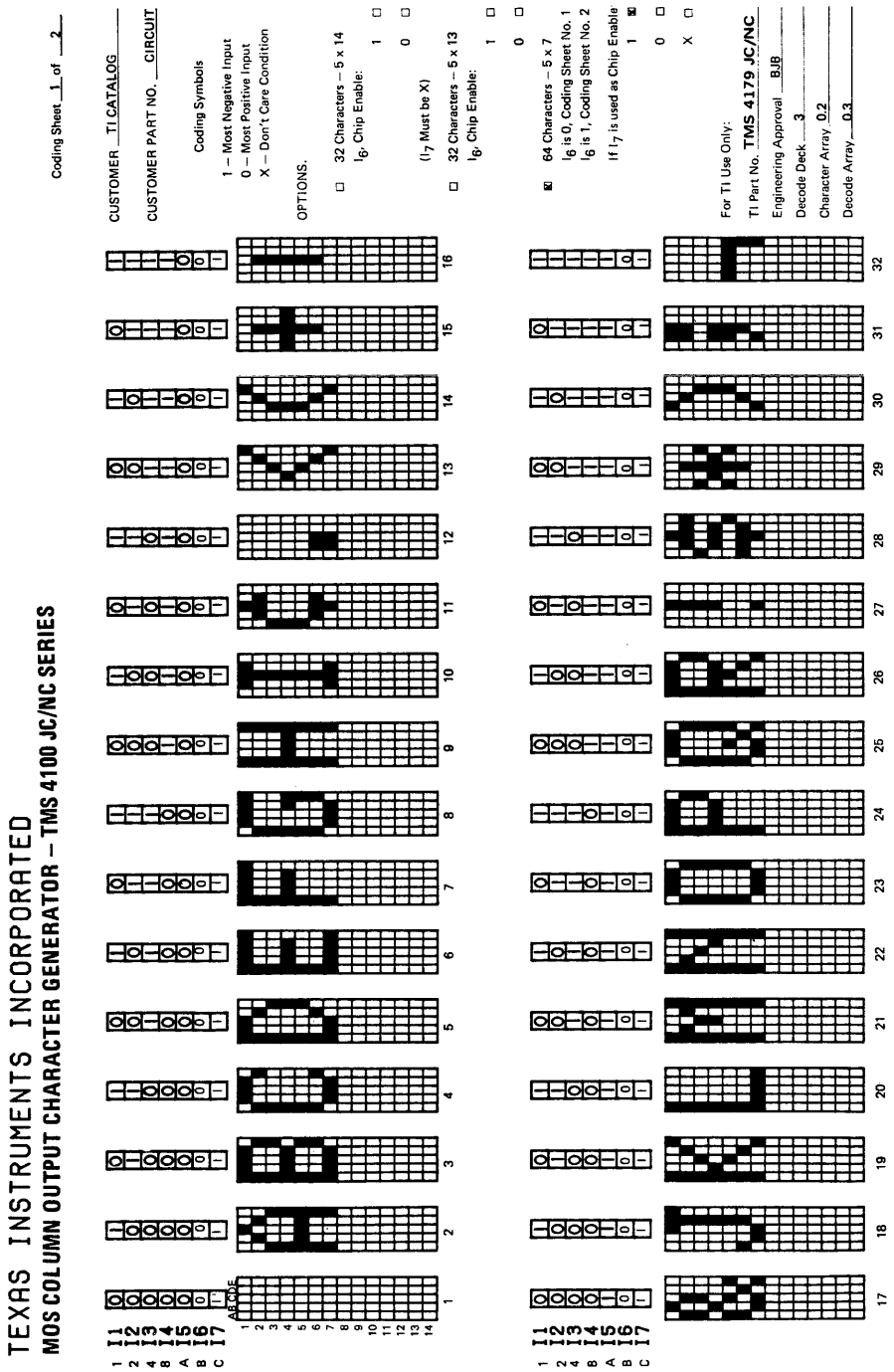
TEXAS INSTRUMENTS INCORPORATED
TMS 4177 JC/NC – TMS 4178 JC/NC (Sheet 1 of 2)
7 x 10 USASCII CHARACTER DISPLAY



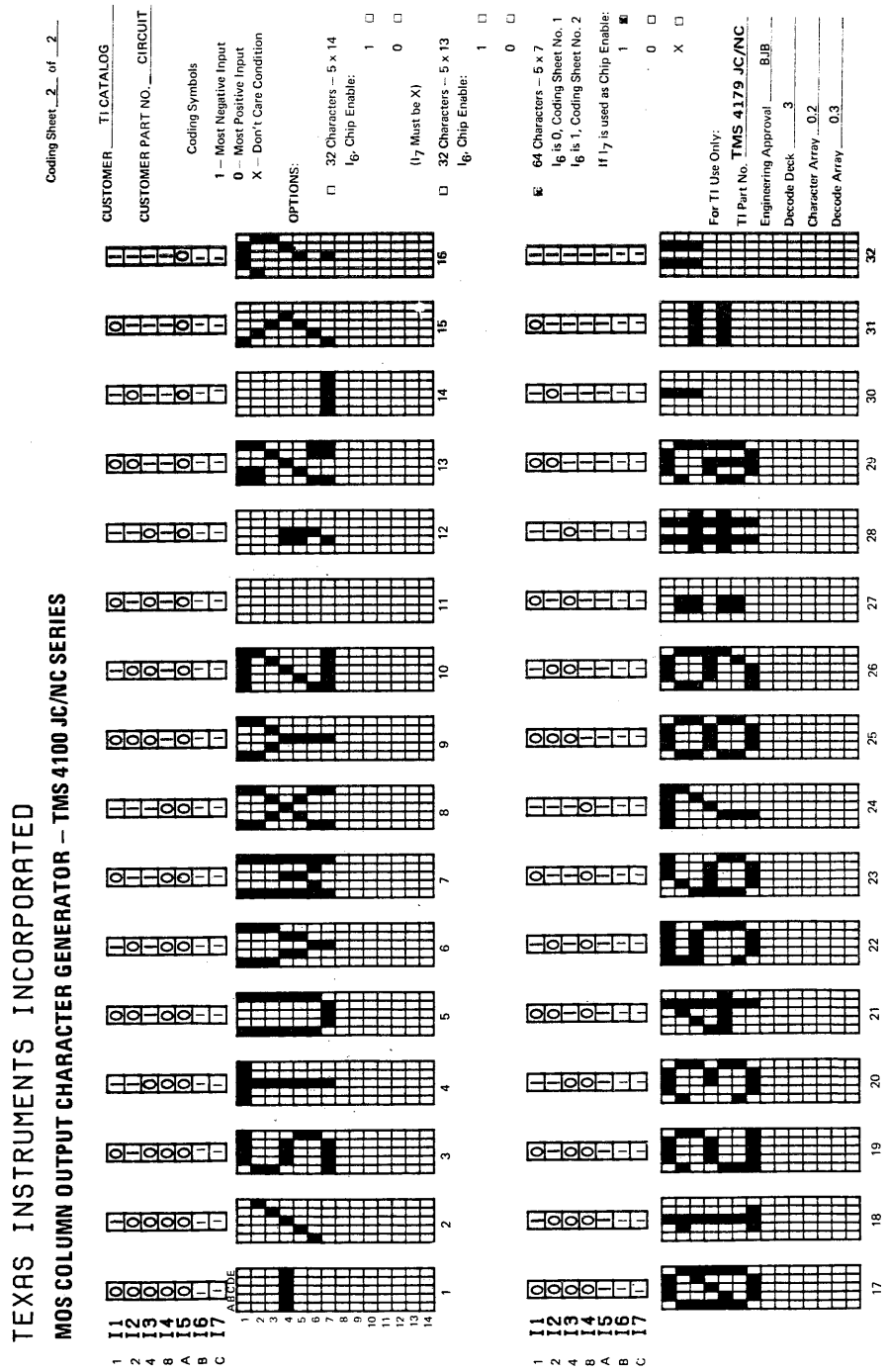
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TEXAS INSTRUMENTS INCORPORATED
TMS 4177 JC/NC – TMS 4178 JC/NC (Sheet 2 of 2)
7 x 10 USASCII CHARACTER DISPLAY





TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222



14

TMS 4400 JC, TMS 4400 NC
4096-BIT STATIC READ-ONLY MEMORY

features

- 4096-bit capacity
- Static operation
- Access time less than 1 microsecond (typical)
- Two organizations available
- Open-drain output buffers or double-ended buffers
- TTL compatible
- Three chip-select lines available
- 24-pin dual-in-line package
  - ceramic – TMS 4400 JC
  - plastic – TMS 4400 NC

description

The TMS 4400 JC/NC series is a family of static read-only memories, each with a capacity of 4096 bits. Two memory organizations and two output buffer configurations are provided through single-level mask programming.

The memory may be organized as 1024 words of four bits, or 512 words of eight bits.

"TMS 4400 JC" designates a unit mounted in a 24-pin ceramic dual-in-line package, and "TMS 4400 NC" is used for a unit mounted in a 24-pin plastic package.

Two types of output buffers are available:

- Single-Ended (open drain)

  Designed for driving TTL, this output has one MOS device with its drain at the output and its source at chip ground.

- Double-Ended

  Designed for driving the inputs to other MOS integrated circuits and devices, this version has its own MOS load resistor provided internally. It requires no additional external circuitry.

Depending on the device organization chosen by the user, there are either three chip selects (1024 words by 4 bits) or four (512 words by 8 bits).

Each bit of the chip select address may be programmed as a logic 1, a logic 0, or a "don't care" (unused) input.

logic definition

Negative logic is assumed.

a) Logic 1 = most negative voltage.

b) Logic 0 = most positive voltage.

operation

The TMS 4400 JC/NC series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip select) remains unchanged.

– continued

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operation (continued)

"Access time" is defined as the maximum time required for all outputs to reach the minimum logic 1 levels or maximum logic 0 levels with the correct data. This time is measured from that point in time at which all address inputs and chip-select inputs are valid.

A disable input word on the chip-select input will cause the outputs to become open circuits on the "single-ended" (open-drain) type output buffer and will cause the outputs to go to V_{DD} on the double-ended (push-pull) type output buffer.

The number of words per output is increased by hardwiring together the outputs of different devices. This means that if the 512 x 8 chip configuration is used, a memory system may be built using 16 TMS 4400 JC/NC devices for a 8192-words-of-8-bits memory without additional external logic. If the 1024 x 4 organization is chosen, eight TMS 4400 JC/NC devices may be hardwired without additional logic. When using the hardwired output technique, note that all devices should have single-ended buffers. Hardwiring outputs performs the AND function in negative logic.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage ranges (See Note 1) . . . . . −30 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−9	−12	−22	V
Supply voltage V_{GG}	−18	−24	−29	V
Input, chip select logic 1	−8	−12	−22	V
Input, chip select logic 0	+0.3	0	−3	V
Input pulse width	550			ns

The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V). Larger power supplies (e.g., +14 V, −14 V) may be used.

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{out(0)}$	Logical 0 output current (Note 1)	−12 V applied to output	3	7		mA
$I_{out(1)}$	Logical 1 output current (Note 1)	−12 V applied to output			10	μA
$Z_{out(1)}$	Logical 1 output impedance (Note 2)	V applied = V_{DD} + 3		18	25	kΩ
$Z_{out(0)}$	Logical 0 output impedance (Note 3)	V applied = V_{SS} −3		0.8	1.1	kΩ
$V_{out(1)}$	Logical 1 output voltage (Note 2)	R_L = 1 mΩ	−10			V
$V_{out(0)}$	Logical 0 output voltage (Note 2)	R_L = 1 mΩ			−2.0	V

NOTES: 1. Open-drain buffer
2. Double-ended buffer
3. Either open-drain or double-ended configuration

— continued

14

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted) — continued

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
P_d	Power dissipation (Note 2)	All outputs at Logical 0		250		mW
I_L	Input leakage current	−12 V applied to input			1	μA
C_{in}	Input capacitance	V_{in} = 0 V, f = 1 MHz		10		pF
I_{DD}	Drain current (Note 2)	All outputs = Logical 0		20		mA
I_{GG}	Gate current			1.0		μA

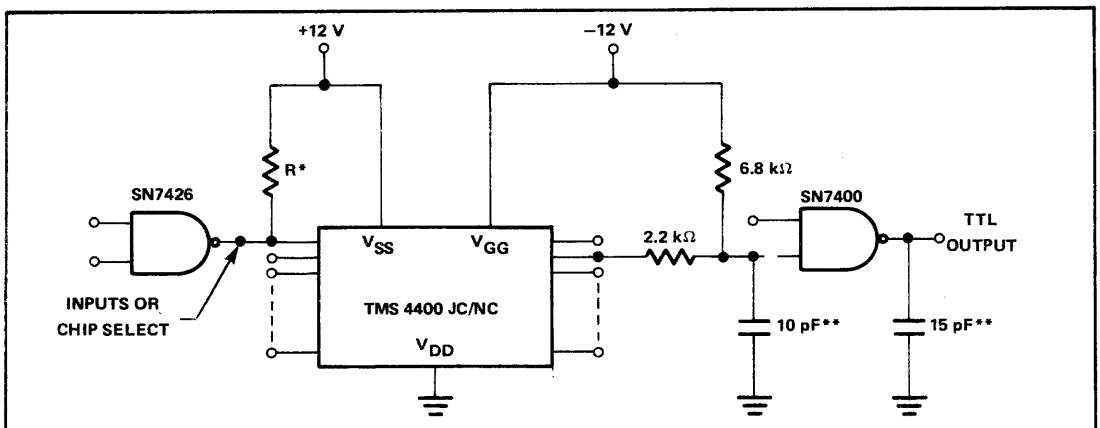
NOTE 2: Double-ended buffer

dynamic electrical characteristics (under nominal operating conditions and at 25°C unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{A1}	Access time TTL load (Notes 1 & 2)	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		900	1500	ns
t_{A2}	Access time TTL load (Notes 1 & 2)	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		700	1300	ns
t_{A1}	Access time (Notes 2 & 3)	V_{GG} = −24 V, V_{DD} = −12 V		1.5	2.0	μs
t_{A2}	Access time (Notes 2 & 3)	V_{GG} = −24 V, V_{DD} = −12 V		0.8	1.5	μs

NOTES: 1. Open ended buffer
2. See Switching Diagram
3. Double-ended buffer R_L = 1 MΩ, C = 20 pF

switching circuit and TTL interface

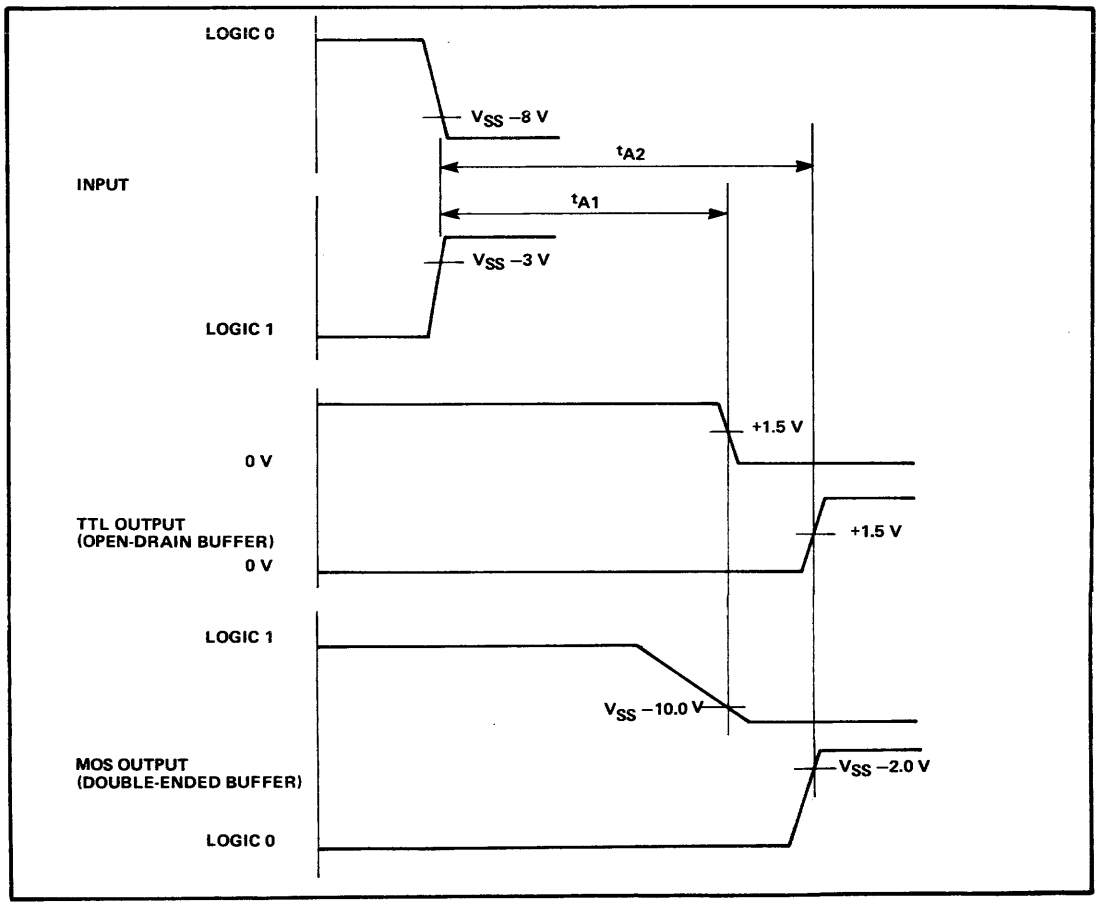


* VALUE OF R DEPENDS ON SYSTEM SPEED AND POWER REQUIREMENTS.

** THE OUTPUT CAPACITANCES ARE NOT PART OF THE TTL INTERFACE. THEY ARE USED IN THE SWITCHING CIRCUITS TO SIMULATE PARASITIC CAPACITANCE LOADING IN ACTUAL USE (BOARD, INTERCONNECT, ETC.).

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

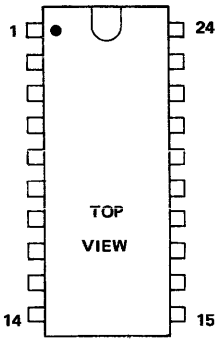
switching diagram (TTL load)



mechanical data and pin configuration

The device is available in both a 24-pin hermetically sealed ceramic dual-in-line package (TMS 4400 JC) and a 24-pin plastic package (TMS 4400 NC). These packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

Depending on the organization of the memory, 2 pin configurations may be used:



PIN NO.	512 x 8	1024 x 4	PIN NO.	512 x 8	1024 x 4
1	I_1	I_1	13	O_4	O_2
2	I_0	I_0	14	O_3	O_1
3	CS1	CS1	15	O_2	NC
4	CS2	CS2	16	O_1	NC
5	CS3	CS3	17	V_{SS}	V_{SS}
6	CS4	I_9	18	I_8	I_8
7	V_{GG}	V_{GG}	19	I_7	I_7
8	V_{DD}	V_{DD}	20	I_6	I_6
9	O_8	NC	21	I_5	I_5
10	O_7	NC	22	I_4	I_4
11	O_6	O_4	23	I_3	I_3
12	O_5	O_3	24	I_2	I_2

I	INPUT	NC	NO CONNECTION
O	OUTPUT	CS	CHIP SELECT

custom programmed devices

The TMS 4400 JC/NC series is programmed at the gate-oxide stage of manufacturing. Programming charges are reduced to a minimum because only one mask per unique design need be created (gate-oxide-removal mask). All other processing steps remain the same for all devices. Options available to the customer during programming are:

- memory organization – 512 x 8 or 1024 x 4
- memory contents
- chip-select word
- output buffer type

The encoding of the gate mask is done by computer to provide a fast, error-free encoding process.

input format

Programming information for the TMS 4400 JC/NC will be transmitted to TI in the form of a *deck of 64 standard 80-column computer cards*, accompanied by a listing of these cards. This method eliminates many chances for error and guarantees the fastest delivery schedule of ROMs. Upon receipt of each deck, a computer run will be made and a copy of the computer-generated truth table sent back to the customer. This copy should be checked carefully. If any errors are discovered, TI must be notified immediately so that work can be stopped and the necessary adjustments made.

Information on the various circuit options desired will be transmitted on a special form supplied by TI. A copy of the form is included in this bulletin.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DATA CARD FORMAT

Column No.

1-2	Punch a right-justified integer for the card number (1-64).
3-6	Punch the ZA identification number supplied by TI MOS Marketing (4 numbers).
7	Blank
8-11	Punch a right-justified integer representing the binary input address for the first set of outputs described on the card.
12	Blank
13-16	Punch a right-justified integer representing the binary input address for the last set of outputs described on the card.
17-80	Punch the desired output data for the range of addresses specified on the card — a "1" for a logical 1 and a "0" for a logical 0.

Input addresses and output data are dependent upon the configuration.

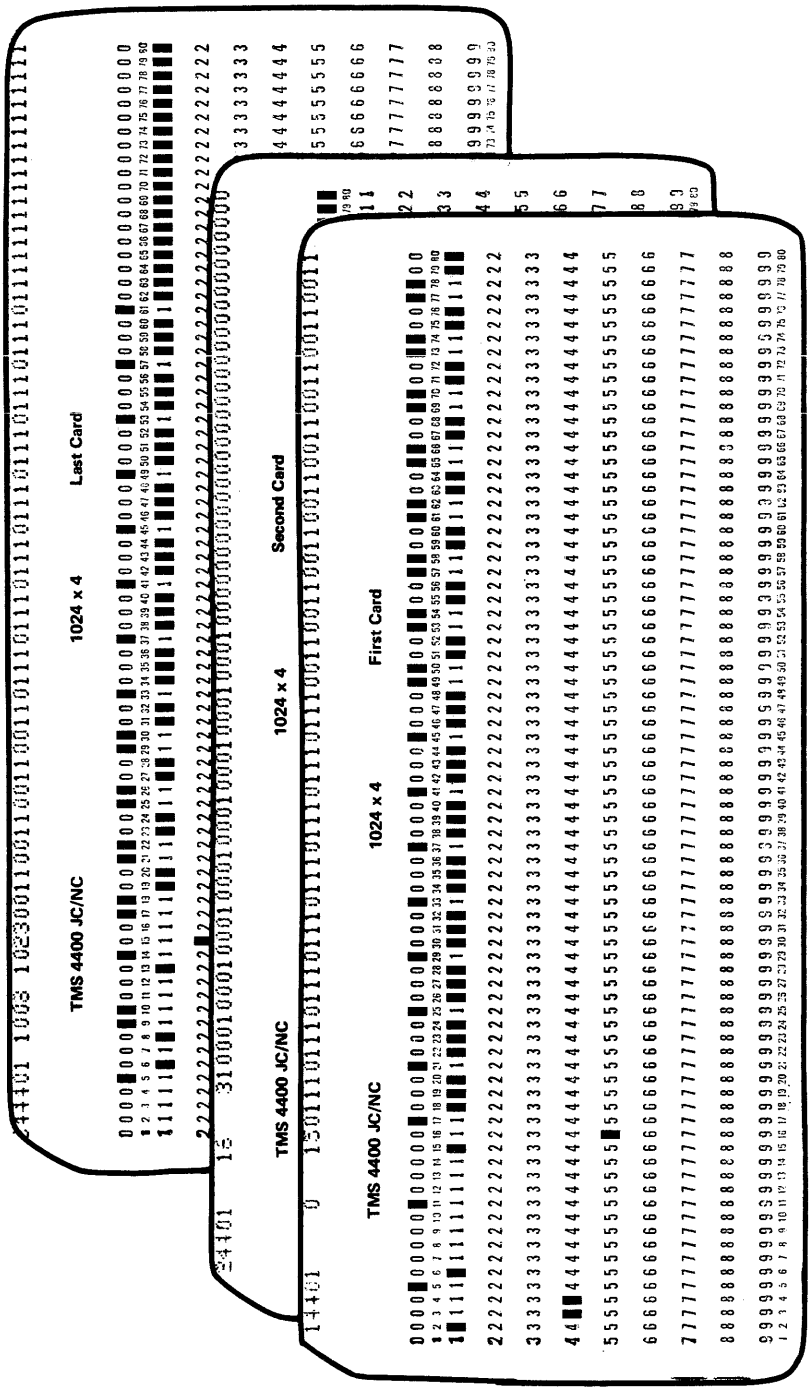
512 Word x 8-Bit Organization

Each card will describe 8 sets of output data. The address words will be sequential from 0 to 511. The output data sets will each be 8 columns long and describe the outputs O_1, O_2, O_3, O_4, O_5, O_6, O_7, and O_8, in that order.

1024 Word x 4-Bit Organization

Each card will describe 16 sets of output data. The address words will be sequential from 0 to 1023. The output data sets will each be 4 columns long and describe the outputs O_1, O_2, O_3 and O_4 in that order.

data cards



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4400 JC/NC CUSTOM CODING INFORMATION

ZA Identification:_____ Date:_____

Customer _____

Address _____ _____

_____

Customer Part Number:_____

Chip Organization

512 x 8 ☐ (8) 1024 x 4 ☐ (4)

Chip Address

512 x 8

	CS1	CS2	CS3	CS4
Pin Nos.	3	4	5	6

1024 x 4

	CS1	CS2	CS3
Pin Nos.	3	4	5

NOTE: 0 – Logical zero level (negative logic)
1 – Logical one level (negative logic)
X – Do not wish to use

Output Buffer Type

Open Drain, TTL Compatible ☐ (OD)

Push-Pull, MOS Compatible ☐ (PP)

truth table, TMS 4401 JC/NC (sheet 1 of 4)

ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4
0	0	1	1	1	64	1	1	1	1	128	1	1	1	1	192	1	1	1	1
1	0	1	1	1	65	0	1	1	1	129	0	1	1	1	193	0	1	1	1
2	0	1	1	1	66	0	1	1	1	130	0	1	1	1	194	0	1	1	1
3	0	1	1	1	67	0	1	1	1	131	0	1	1	1	195	0	1	1	1
4	0	1	1	1	68	0	1	1	1	132	0	1	1	1	196	0	1	1	1
5	0	1	1	1	69	0	1	1	1	133	0	1	1	1	197	0	1	1	1
6	0	1	1	1	70	0	1	1	1	134	0	1	1	1	198	0	1	1	1
7	0	1	1	1	71	0	1	1	1	135	0	1	1	1	199	0	1	1	1
8	0	0	1	1	72	0	0	1	1	136	0	0	1	1	200	0	0	1	1
9	0	0	1	1	73	0	0	1	1	137	0	0	1	1	201	0	0	1	1
10	0	0	1	1	74	0	0	1	1	138	0	0	1	1	202	0	0	1	1
11	0	0	1	1	75	0	0	1	1	139	0	0	1	1	203	0	0	1	1
12	0	0	1	1	76	0	0	1	1	140	0	0	1	1	204	0	0	1	1
13	0	0	1	1	77	0	0	1	1	141	0	0	1	1	205	0	0	1	1
14	0	0	1	1	78	0	0	1	1	142	0	0	1	1	206	0	0	1	1
15	0	0	1	1	79	0	0	1	1	143	0	0	1	1	207	0	0	1	1
16	0	0	0	1	80	0	0	0	1	144	0	0	0	1	208	0	0	0	1
17	0	0	0	1	81	0	0	0	1	145	0	0	0	1	209	0	0	0	1
18	0	0	0	1	82	0	0	0	1	146	0	0	0	1	210	0	0	0	1
19	0	0	0	1	83	0	0	0	1	147	0	0	0	1	211	0	0	0	1
20	0	0	0	1	84	0	0	0	1	148	0	0	0	1	212	0	0	0	1
21	0	0	0	1	85	0	0	0	1	149	0	0	0	1	213	0	0	0	1
22	0	0	0	1	86	0	0	0	1	150	0	0	0	1	214	0	0	0	1
23	0	0	0	1	87	0	0	0	1	151	0	0	0	1	215	0	0	0	1
24	0	0	0	0	88	0	0	0	0	152	0	0	0	0	216	0	0	0	0
25	0	0	0	0	89	0	0	0	0	153	0	0	0	0	217	0	0	0	0
26	0	0	0	0	90	0	0	0	0	154	0	0	0	0	218	0	0	0	0
27	0	0	0	0	91	0	0	0	0	155	0	0	0	0	219	0	0	0	0
28	0	0	0	0	92	0	0	0	0	156	0	0	0	0	220	0	0	0	0
29	0	0	0	0	93	0	0	0	0	157	0	0	0	0	221	0	0	0	0
30	0	0	0	0	94	0	0	0	0	158	0	0	0	0	222	0	0	0	0
31	0	0	0	0	95	0	0	0	0	159	0	0	0	0	223	0	0	0	0
32	0	0	0	0	96	0	0	0	0	160	0	0	0	0	224	0	0	0	0
33	0	0	0	0	97	0	0	0	0	161	0	0	0	0	225	0	0	0	0
34	0	0	0	0	98	0	0	0	0	162	0	0	0	0	226	0	0	0	0
35	0	0	0	0	99	0	0	0	0	163	0	0	0	0	227	0	0	0	0
36	0	0	0	0	100	0	0	0	0	164	0	0	0	0	228	0	0	0	0
37	0	0	0	0	101	0	0	0	0	165	0	0	0	0	229	0	0	0	0
38	0	0	0	0	102	0	0	0	0	166	0	0	0	0	230	0	0	0	0
39	0	0	0	0	103	0	0	0	0	167	0	0	0	0	231	0	0	0	0
40	0	0	0	1	104	0	0	0	1	168	0	0	0	1	232	0	0	0	1
41	0	0	0	1	105	0	0	0	1	169	0	0	0	1	233	0	0	0	1
42	0	0	0	1	106	0	0	0	1	170	0	0	0	1	234	0	0	0	1
43	0	0	0	1	107	0	0	0	1	171	0	0	0	1	235	0	0	0	1
44	0	0	0	1	108	0	0	0	1	172	0	0	0	1	236	0	0	0	1
45	0	0	0	1	109	0	0	0	1	173	0	0	0	1	237	0	0	0	1
46	0	0	0	1	110	0	0	0	1	174	0	0	0	1	238	0	0	0	1
47	0	0	0	1	111	0	0	0	1	175	0	0	0	1	239	0	0	0	1
48	0	0	1	1	112	0	0	1	1	176	0	0	1	1	240	0	0	1	1
49	0	0	1	1	113	0	0	1	1	177	0	0	1	1	241	0	0	1	1
50	0	0	1	1	114	0	0	1	1	178	0	0	1	1	242	0	0	1	1
51	0	0	1	1	115	0	0	1	1	179	0	0	1	1	243	0	0	1	1
52	0	0	1	1	116	0	0	1	1	180	0	0	1	1	244	0	0	1	1
53	0	0	1	1	117	0	0	1	1	181	0	0	1	1	245	0	0	1	1
54	0	0	1	1	118	0	0	1	1	182	0	0	1	1	246	0	0	1	1
55	0	0	1	1	119	0	0	1	1	183	0	0	1	1	247	0	0	1	1
56	0	1	1	1	120	0	1	1	1	184	0	1	1	1	248	0	1	1	1
57	0	1	1	1	121	0	1	1	1	185	0	1	1	1	249	0	1	1	1
58	0	1	1	1	122	0	1	1	1	186	0	1	1	1	250	0	1	1	1
59	0	1	1	1	123	0	1	1	1	187	0	1	1	1	251	0	1	1	1
60	0	1	1	1	124	0	1	1	1	188	0	1	1	1	252	0	1	1	1
61	0	1	1	1	125	0	1	1	1	189	0	1	1	1	253	0	1	1	1
62	0	1	1	1	126	0	1	1	1	190	0	1	1	1	254	0	1	1	1
63	1	1	1	1	127	1	1	1	1	191	1	1	1	1	255	1	1	1	1

14

CS1 = 1 CS2 = 1 CS3 = 1 push-pull outputs

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

truth table, TMS 4401 JC/NC (sheet 2 of 4)

ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4
256	1	1	1	1	320	1	1	1	1	384	1	1	1	1	448	1	1	1	1
257	1	1	1	1	321	1	1	1	1	385	1	1	1	1	449	1	1	1	1
258	0	1	1	1	322	0	1	1	1	386	1	1	1	1	450	1	1	1	1
259	0	1	1	1	323	0	1	1	1	387	1	1	1	1	451	1	1	1	1
260	0	1	1	1	324	0	1	1	1	388	0	1	1	1	452	0	1	1	1
261	0	1	1	1	325	0	1	1	1	389	0	1	1	1	453	0	1	1	1
262	0	1	1	1	326	0	1	1	1	390	0	1	1	1	454	0	1	1	1
263	0	1	1	1	327	0	1	1	1	391	0	1	1	1	455	0	1	1	1
264	0	1	1	1	328	0	1	1	1	392	0	1	1	1	456	0	1	1	1
265	0	1	1	1	329	0	1	1	1	393	0	1	1	1	457	0	1	1	1
266	0	1	1	1	330	0	1	1	1	393	0	1	1	1	458	0	1	1	1
267	0	1	1	1	331	0	1	1	1	394	0	1	1	1	459	0	1	1	1
268	0	0	1	1	332	0	0	1	1	395	0	1	1	1	460	0	0	1	1
269	0	0	1	1	333	0	0	1	1	396	0	0	1	1	461	0	0	1	1
270	0	0	1	1	334	0	0	1	1	397	0	0	1	1	462	0	0	1	1
271	0	0	1	1	335	0	0	1	1	398	0	0	1	1	463	0	0	1	1
272	0	0	1	1	336	0	0	1	1	399	0	0	1	1	464	0	0	1	1
273	0	0	1	1	337	0	0	1	1	400	0	0	1	1	465	0	0	1	1
274	0	0	1	1	338	0	0	1	1	401	0	0	1	1	466	0	0	1	1
275	0	0	1	1	339	0	0	0	1	402	0	0	1	1	467	0	0	1	1
276	0	0	0	1	340	0	0	0	1	403	0	0	1	1	468	0	0	0	1
277	0	0	0	1	341	0	0	0	1	404	0	0	0	1	469	0	0	0	1
278	0	0	0	1	342	0	0	0	1	405	0	0	0	1	470	0	0	0	1
279	0	0	0	1	343	0	0	0	1	406	0	0	0	1	471	0	0	0	1
280	0	0	0	1	344	0	0	0	1	407	0	0	0	1	472	0	0	0	1
281	0	0	0	1	345	0	0	0	1	408	0	0	0	1	473	0	0	0	1
282	0	0	0	1	346	0	0	0	1	409	0	0	0	1	474	0	0	0	1
283	0	0	0	1	347	0	0	0	1	410	0	0	0	1	475	0	0	0	1
284	0	0	0	0	348	0	0	0	0	411	0	0	0	1	476	0	0	0	0
285	0	0	0	0	349	0	0	0	0	412	0	0	0	0	477	0	0	0	0
286	0	0	0	0	350	0	0	0	0	413	0	0	0	0	478	0	0	0	0
287	0	0	0	0	351	0	0	0	0	414	0	0	0	0	479	0	0	0	0
288	0	0	0	0	352	0	0	0	0	415	0	0	0	0	480	0	0	0	0
289	0	0	0	0	353	0	0	0	0	416	0	0	0	0	481	0	0	0	0
290	0	0	0	0	354	0	0	0	0	417	0	0	0	0	482	0	0	0	0
291	0	0	0	0	355	0	0	0	0	418	0	0	0	0	483	0	0	0	0
292	0	0	0	1	356	0	0	0	1	419	0	0	0	0	484	0	0	0	1
293	0	0	0	1	357	0	0	0	1	420	0	0	0	1	485	0	0	0	1
294	0	0	0	1	358	0	0	0	1	421	0	0	0	1	486	0	0	0	1
295	0	0	0	1	359	0	0	0	1	422	0	0	0	1	487	0	0	0	1
296	0	0	0	1	360	0	0	0	1	423	0	0	0	1	488	0	0	0	1
297	0	0	0	1	361	0	0	0	1	424	0	0	0	1	489	0	0	0	1
298	0	0	0	1	362	0	0	0	1	425	0	0	0	1	490	0	0	0	1
299	0	0	0	1	363	0	0	0	1	426	0	0	0	1	491	0	0	0	1
300	0	0	1	1	364	0	0	1	1	427	0	0	0	1	492	0	0	1	1
301	0	0	1	1	365	0	0	1	1	428	0	0	1	1	493	0	0	1	1
302	0	0	1	1	366	0	0	1	1	429	0	0	1	1	494	0	0	1	1
303	0	0	1	1	367	0	0	1	1	430	0	0	1	1	495	0	0	1	1
304	0	0	1	1	368	0	0	1	1	431	0	0	1	1	496	0	0	1	1
305	0	0	1	1	369	0	0	1	1	432	0	0	1	1	497	0	0	1	1
306	0	0	1	1	370	0	0	1	1	433	0	0	1	1	498	0	0	1	1
307	0	0	1	1	371	0	0	1	1	434	0	0	1	1	499	0	0	1	1
308	0	1	1	1	372	0	1	1	1	435	0	0	1	1	500	0	1	1	1
309	0	1	1	1	373	0	1	1	1	436	0	1	1	1	501	0	1	1	1
310	0	1	1	1	374	0	1	1	1	437	0	1	1	1	502	0	1	1	1
311	0	1	1	1	375	0	1	1	1	438	0	1	1	1	503	0	1	1	1
312	0	1	1	1	376	0	1	1	1	439	0	1	1	1	504	0	1	1	1
313	0	1	1	1	377	0	1	1	1	440	0	1	1	1	505	0	1	1	1
314	0	1	1	1	378	0	1	1	1	441	0	1	1	1	506	0	1	1	1
315	0	1	1	1	379	0	1	1	1	442	0	1	1	1	507	0	1	1	1
316	0	1	1	1	380	0	1	1	1	443	0	1	1	1	508	1	1	1	1
317	0	1	1	1	381	0	1	1	1	444	1	1	1	1	509	1	1	1	1
318	1	1	1	1	382	1	1	1	1	445	1	1	1	1	510	1	1	1	1
319	1	1	1	1	383	1	1	1	1	446	1	1	1	1	511	1	1	1	1

CS1 = 1 CS2 = 1 CS3 = 1 push-pull outputs

truth table, TMS 4401 JC/NC (sheet 3 of 4)

ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4
512	1	1	1	1	576	1	1	1	1	640	1	1	1	1	704	1	1	1	1
513	1	1	1	1	577	1	1	1	1	641	1	1	1	1	705	1	1	1	1
514	1	1	1	1	578	1	1	1	1	642	1	1	1	1	706	1	1	1	1
515	1	1	1	1	579	1	1	1	1	643	1	1	1	1	707	1	1	1	1
516	1	1	1	1	580	1	1	1	1	644	1	1	1	1	708	1	1	1	1
517	1	1	1	1	581	1	1	1	1	645	1	1	1	1	709	1	1	1	1
518	1	1	1	1	582	1	1	1	1	646	1	1	1	1	710	1	1	1	1
519	1	1	1	1	583	1	1	1	1	647	1	1	1	1	711	1	1	1	1
520	0	1	1	1	584	0	1	1	1	648	0	1	1	1	712	0	1	1	1
521	0	1	1	1	585	0	1	1	1	649	0	1	1	1	713	0	1	1	1
522	0	1	1	1	586	0	1	1	1	650	0	1	1	1	714	0	1	1	1
523	0	1	1	1	587	0	1	1	1	651	0	1	1	1	715	0	1	1	1
524	0	1	1	1	588	0	1	1	1	652	0	1	1	1	716	0	1	1	1
525	0	1	1	1	589	0	1	1	1	653	0	1	1	1	717	0	1	1	1
526	0	1	1	1	590	0	1	1	1	654	0	1	1	1	718	0	1	1	1
527	0	1	1	1	591	0	1	1	1	655	0	1	1	1	719	0	1	1	1
528	0	0	1	1	592	0	1	1	1	656	0	0	1	1	720	0	0	1	1
529	0	0	1	1	593	0	0	1	1	657	0	0	1	1	721	0	0	1	1
530	0	0	1	1	594	0	0	1	1	658	0	0	1	1	722	0	0	1	1
531	0	0	1	1	595	0	0	1	1	659	0	0	1	1	723	0	0	1	1
532	0	0	1	1	596	0	0	1	1	660	0	0	1	1	724	0	0	1	1
533	0	0	1	1	597	0	0	1	1	661	0	0	1	1	725	0	0	1	1
534	0	0	1	1	598	0	0	1	1	662	0	0	1	1	726	0	0	1	1
535	0	0	1	1	599	0	0	1	1	663	0	0	1	1	727	0	0	1	1
536	0	0	0	1	600	0	0	0	1	664	0	0	0	1	728	0	0	0	1
537	0	0	0	1	601	0	0	0	1	665	0	0	0	1	729	0	0	0	1
538	0	0	0	1	602	0	0	0	1	666	0	0	0	1	730	0	0	0	1
539	0	0	0	1	603	0	0	0	1	667	0	0	0	1	731	0	0	0	1
540	0	0	0	1	604	0	0	0	1	668	0	0	0	1	732	0	0	0	1
541	0	0	0	1	605	0	0	0	1	669	0	0	0	1	733	0	0	0	1
542	0	0	0	1	606	0	0	0	1	670	0	0	0	0	734	0	0	0	0
543	0	0	0	1	607	0	0	0	1	671	0	0	0	0	735	0	0	0	0
544	0	0	0	1	608	0	0	0	0	672	0	0	0	0	736	0	0	0	0
545	0	0	0	1	609	0	0	0	1	673	0	0	0	0	737	0	0	0	0
546	0	0	0	1	610	0	0	0	1	674	0	0	0	1	738	0	0	0	1
547	0	0	0	1	611	0	0	0	1	675	0	0	0	1	739	0	0	0	1
548	0	0	0	1	612	0	0	0	1	676	0	0	0	1	740	0	0	0	1
549	0	0	0	1	613	0	0	0	1	677	0	0	0	1	741	0	0	0	1
550	0	0	0	1	614	0	0	0	1	678	0	0	0	1	742	0	0	0	1
551	0	0	0	1	615	0	0	0	1	679	0	0	0	1	743	0	0	0	1
552	0	0	1	1	616	0	0	1	1	680	0	0	1	1	744	0	0	1	1
553	0	0	1	1	617	0	0	1	1	681	0	0	1	1	745	0	0	1	1
554	0	0	1	1	618	0	0	1	1	682	0	0	1	1	746	0	0	1	1
555	0	0	1	1	619	0	0	1	1	683	0	0	1	1	747	0	0	1	1
556	0	0	1	1	620	0	0	1	1	684	0	0	1	1	748	0	0	1	1
557	0	0	1	1	621	0	0	1	1	685	0	0	1	1	749	0	0	1	1
558	0	0	1	1	622	0	0	1	1	686	0	0	1	1	750	0	0	1	1
559	0	0	1	1	623	0	0	1	1	687	0	0	1	1	751	0	0	1	1
560	0	1	1	1	624	0	1	1	1	688	0	1	1	1	752	0	1	1	1
561	0	1	1	1	625	0	1	1	1	689	0	1	1	1	753	0	1	1	1
562	0	1	1	1	626	0	1	1	1	690	0	1	1	1	754	0	1	1	1
563	0	1	1	1	627	0	1	1	1	691	0	1	1	1	755	0	1	1	1
564	0	1	1	1	628	0	1	1	1	692	0	1	1	1	756	0	1	1	1
565	0	1	1	1	629	0	1	1	1	693	0	1	1	1	757	0	1	1	1
566	0	1	1	1	630	0	1	1	1	694	0	1	1	1	758	0	1	1	1
567	0	1	1	1	631	0	1	1	1	695	0	1	1	1	759	0	1	1	1
568	1	1	1	1	632	1	1	1	1	696	1	1	1	1	760	1	1	1	1
569	1	1	1	1	633	1	1	1	1	697	1	1	1	1	761	1	1	1	1
570	1	1	1	1	634	1	1	1	1	698	1	1	1	1	762	1	1	1	1
571	1	1	1	1	635	1	1	1	1	699	1	1	1	1	763	1	1	1	1
572	1	1	1	1	636	1	1	1	1	700	1	1	1	1	764	1	1	1	1
573	1	1	1	1	637	1	1	1	1	701	1	1	1	1	765	1	1	1	1
574	1	1	1	1	638	1	1	1	1	702	1	1	1	1	766	1	1	1	1
575	1	1	1	0	639	1	1	1	1	703	1	1	1	1	767	1	1	1	1

14

CS1 = 1 CS2 = 1 CS3 = 1 push-pull outputs

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

truth table, TMS 4401 JC/NC (sheet 4 of 4)

ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4
768	1	1	1	1	832	1	1	1	1	896	1	1	1	1	960	1	1	1	1
769	1	1	1	1	833	1	1	1	1	897	1	1	1	1	961	1	1	1	1
770	1	1	1	1	834	1	1	1	1	898	1	1	1	1	962	1	1	1	1
771	1	1	1	1	835	0	1	1	1	899	1	1	1	1	963	1	1	1	1
772	0	1	1	1	836	0	1	1	1	900	0	1	1	1	964	0	1	1	1
773	0	1	1	1	837	0	1	1	1	901	0	1	1	1	965	0	1	1	1
774	0	1	1	1	838	0	1	1	1	902	0	1	1	1	966	0	1	1	1
775	0	1	1	1	839	0	1	1	1	903	0	1	1	1	967	0	1	1	1
776	0	1	1	1	840	0	1	1	1	904	0	1	1	1	968	0	1	1	1
777	0	1	1	1	841	0	1	1	1	905	0	1	1	1	969	0	1	1	1
778	0	1	1	1	842	0	1	1	1	906	0	1	1	1	970	0	1	1	1
779	0	1	1	1	843	0	1	1	1	907	0	1	1	1	971	0	1	1	1
780	0	0	1	1	844	0	0	1	1	908	0	0	1	1	972	0	0	1	1
781	0	0	1	1	845	0	0	1	1	909	0	0	1	1	973	0	0	1	1
782	0	0	1	1	846	0	0	1	1	910	0	0	1	1	974	0	0	1	1
783	0	0	1	1	847	0	0	1	1	911	0	0	1	1	975	0	0	1	1
784	0	0	1	1	848	0	0	1	1	912	0	0	1	1	976	0	0	1	1
785	0	0	1	1	849	0	0	1	1	913	0	0	1	1	977	0	0	1	1
786	0	0	1	1	850	0	0	1	1	914	0	0	1	1	978	0	0	1	1
787	0	0	1	1	851	0	0	1	1	915	0	0	1	1	979	0	0	1	1
788	0	0	0	1	852	0	0	0	1	916	0	0	0	1	980	0	0	0	1
789	0	0	0	1	853	0	0	0	1	917	0	0	0	1	981	0	0	0	1
790	0	0	0	1	854	0	0	0	1	918	0	0	0	1	982	0	0	0	1
791	0	0	0	1	855	0	0	0	1	919	0	0	0	1	983	0	0	0	1
792	0	0	0	1	856	0	0	0	1	920	0	0	0	1	984	0	0	0	1
793	0	0	0	1	857	0	0	0	1	921	0	0	0	1	985	0	0	0	1
794	0	0	0	1	858	0	0	0	1	922	0	0	0	1	986	0	0	0	1
795	0	0	0	1	859	0	0	0	1	923	0	0	0	1	987	0	0	0	1
796	0	0	0	0	860	0	0	0	0	924	0	0	0	0	988	0	0	0	0
797	0	0	0	0	861	0	0	0	0	925	0	0	0	0	989	0	0	0	0
798	0	0	0	0	862	0	0	0	0	926	0	0	0	0	990	0	0	0	0
799	0	0	0	0	863	0	0	0	0	927	0	0	0	0	991	0	0	0	0
800	0	0	0	0	864	0	0	0	0	928	0	0	0	0	992	0	0	0	0
801	0	0	0	0	865	0	0	0	0	929	0	0	0	0	993	0	0	0	0
802	0	0	0	0	866	0	0	0	0	930	0	0	0	0	994	0	0	0	0
803	0	0	0	0	867	0	0	0	0	931	0	0	0	0	995	0	0	0	0
804	0	0	0	1	868	0	0	0	1	932	0	0	0	1	996	0	0	0	1
805	0	0	0	1	869	0	0	0	1	933	0	0	0	1	997	0	0	0	1
806	0	0	0	1	870	0	0	0	1	934	0	0	0	1	998	0	0	0	1
807	0	0	0	1	871	0	0	0	1	935	0	0	0	1	999	0	0	0	1
808	0	0	0	1	872	0	0	0	1	936	0	0	0	1	1000	0	0	0	1
809	0	0	0	1	873	0	0	0	1	937	0	0	0	1	1001	0	0	0	1
810	0	0	0	1	874	0	0	0	1	938	0	0	0	1	1002	0	0	0	1
811	0	0	0	1	875	0	0	0	1	939	0	0	0	1	1003	0	0	0	1
812	0	0	1	1	876	0	0	1	1	940	0	0	1	1	1004	0	0	1	1
813	0	0	1	1	877	0	0	1	1	941	0	0	1	1	1005	0	0	1	1
814	0	0	1	1	878	0	0	1	1	942	0	0	1	1	1006	0	0	1	1
815	0	0	1	1	879	0	0	1	1	943	0	0	1	1	1007	0	0	1	1
816	0	0	1	1	880	0	0	1	1	944	0	0	1	1	1008	0	0	1	1
817	0	0	1	1	881	0	0	1	1	945	0	0	1	1	1009	0	0	1	1
818	0	0	1	1	882	0	0	1	1	946	0	0	1	1	1010	0	0	1	1
819	0	0	1	1	883	0	0	1	1	947	0	0	1	1	1011	0	0	1	1
820	0	1	1	1	884	0	1	1	1	948	0	1	1	1	1012	0	1	1	1
821	0	1	1	1	885	0	1	1	1	949	0	1	1	1	1013	0	1	1	1
822	0	1	1	1	886	0	1	1	1	950	0	1	1	1	1014	0	1	1	1
823	0	1	1	1	887	0	1	1	1	951	0	1	1	1	1015	0	1	1	1
824	0	1	1	1	888	0	1	1	1	952	0	1	1	1	1016	0	1	1	1
825	0	1	1	1	889	0	1	1	1	953	0	1	1	1	1017	0	1	1	1
826	0	1	1	1	890	0	1	1	1	954	0	1	1	1	1018	0	1	1	1
827	0	1	1	1	891	0	1	1	1	955	0	1	1	1	1019	0	1	1	1
828	1	1	1	1	892	1	1	1	1	956	1	1	1	1	1020	1	1	1	1
829	1	1	1	1	893	1	1	1	1	957	1	1	1	1	1021	1	1	1	1
830	1	1	1	1	894	1	1	1	1	958	1	1	1	1	1022	1	1	1	1
831	1	1	1	1	895	1	1	1	1	959	1	1	1	1	1023	1	1	1	1

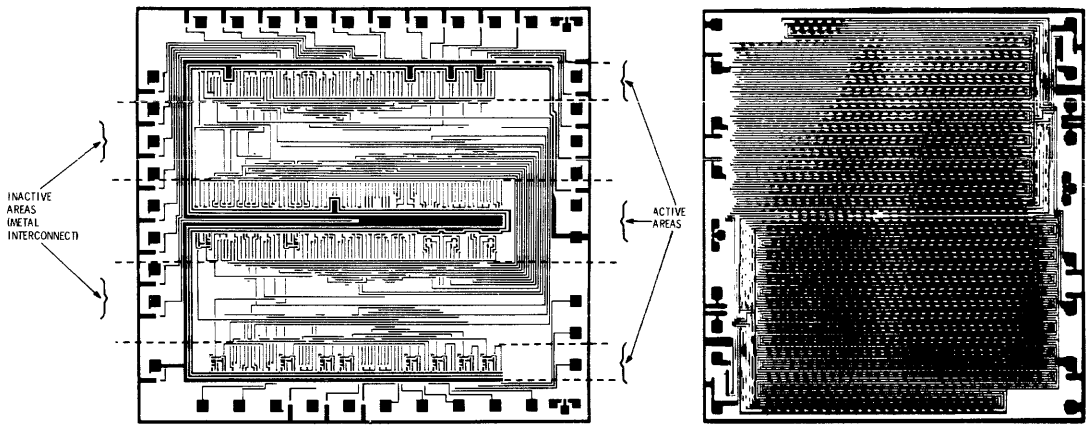
CS1 = 1 CS2 = 1 CS3 = 1 push-pull outputs

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PROGRAMMABLE LOGIC ARRAYS

Programmable logic arrays represent an economical and efficient method to implement random logic using programmable techniques. "Random Logic" means a logic circuit that is not strongly structured, as opposed to circuits such as shift registers, read-only memories, etc. When a random-logic circuit is implemented in MOS, a large part of the chip area is used for interconnection between the cells, as can be seen from the pictures below. This area is essentially wasted.

Random-Logic Chip **Shift-Register Chip**



1) Some Economics

A customer who wants to build a random-logic circuit can choose any of three approaches: bipolar, relatively low-complexity integrated circuits; a custom MOS circuit; a programmable MOS circuit (such as a read-only memory or a PLA).

A custom MOS circuit will be designed from scratch. The customer's logic will be implemented on a piece of silicon. TI will reduce the size of the chip as much as possible, but there will still be a large inactive area for interconnections. With the programmable approach, TI starts with a circuit that is already designed. In order to program the device, only one photomask is modified and this is accomplished easily and economically.

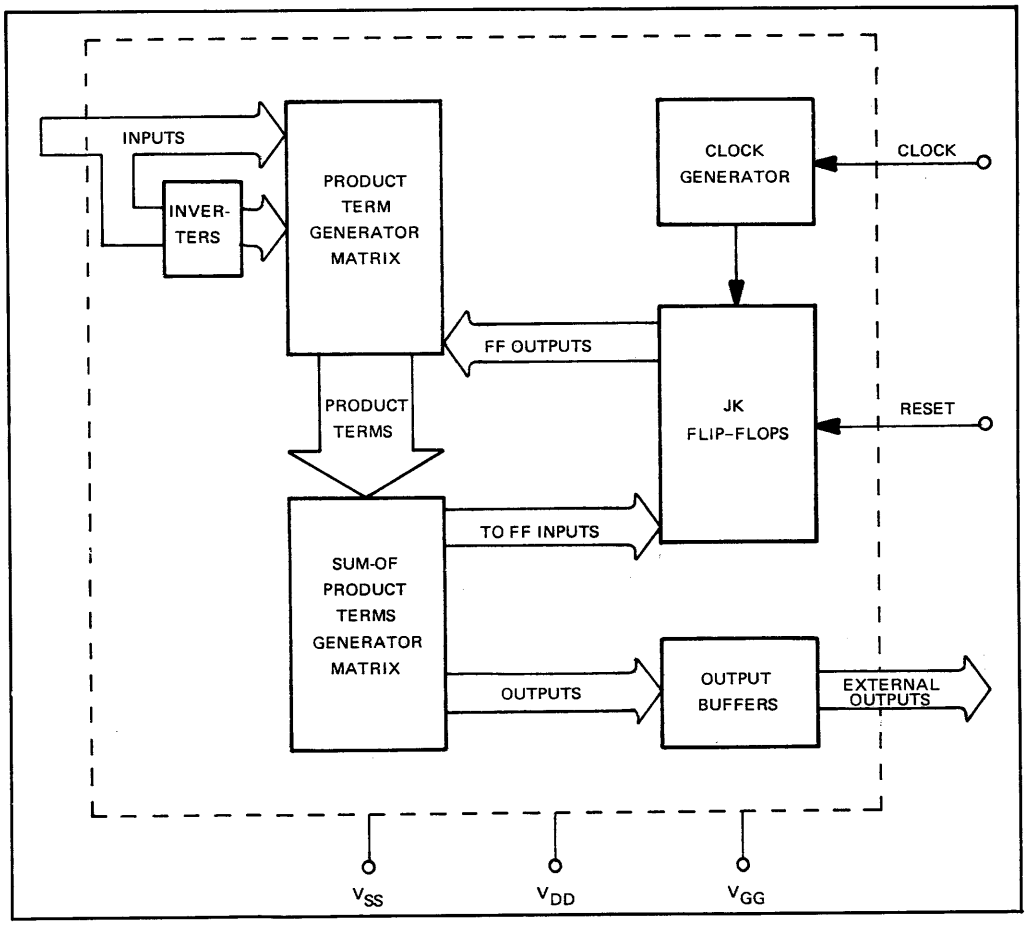
2) PLA Structure

The PLA structure is extremely simple. Any logic equation can be written as a sum of products or as a product of sums, and that is exactly what has been implemented on the array.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

The logic expression is written as a sum of products:

- A first programmable matrix generates the products terms (AND matrix)
- A second programmable matrix generates the sum of products (OR matrix)
- Flip-flops are used in feedback loops to permit implementation of sequential logic.



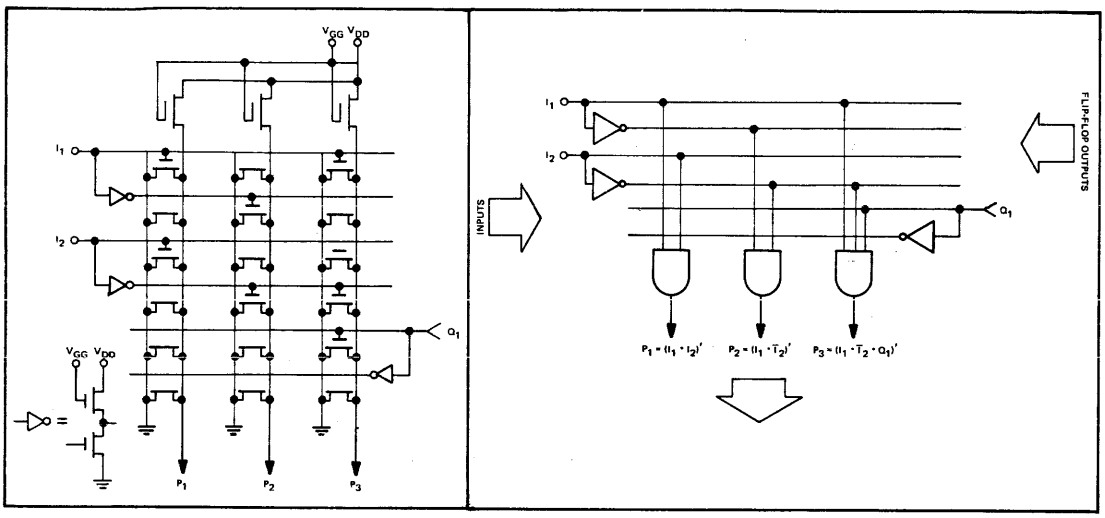
a) **AND Matrix**

The role of the AND matrix is to form the product terms of the input terms, and their complements.

The number of product terms has been arrived at by heuristic methods. We have set a limit of 60 product terms for the TMS 2000 JC, and 72 for the TMS 2200 JC.

PLA 'AND' MATRIX

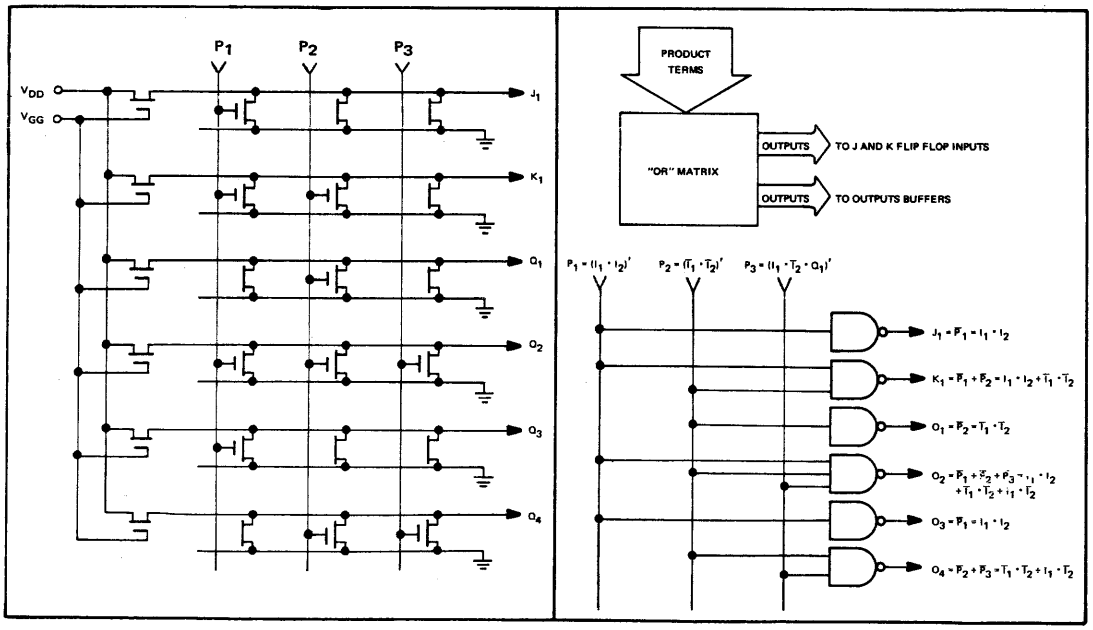
LOGIC EQUIVALENT OF PLA 'AND' MATRIX



b) OR Matrix (Sum of Products)

PLA 'OR' MATRIX

LOGIC EQUIVALENT OF PLA 'OR' MATRIX

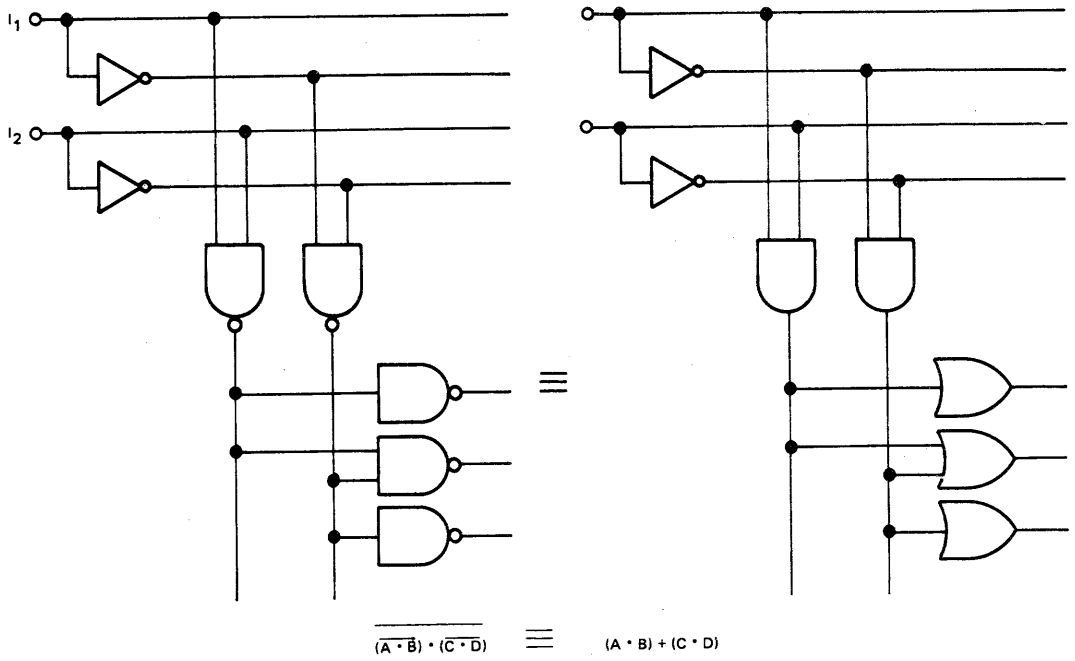


TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

The AND matrix feeds into the OR matrix. The OR matrix generates sums of product terms. Some of the outputs of the OR matrix are fed to the outside while others are fed back to the first matrix (AND) through flip-flops.

Both matrices are programmable. A product term can be of as many of the inputs and their complements as the designer wants. By this same token a sum of product terms can be of as many of the products as the designer wishes.

LOGIC EQUIVALENT OF PLA ORGANIZATION



c) Feedback Loops, Flip-Flops

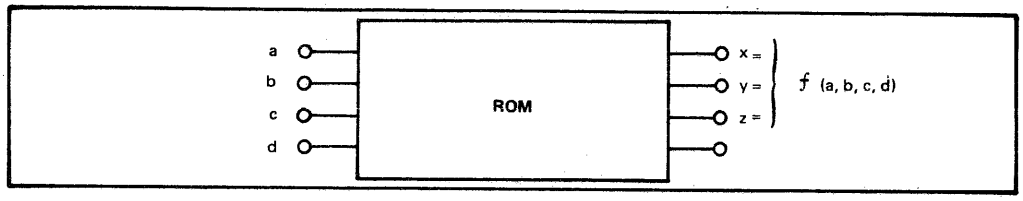
In order to implement sequential logic, feedback loops are necessary. These feedback loops must be timed. If we fed back directly the outputs of this second matrix (OR matrix) to the inputs of the first matrix (AND), a race condition could develop. We use one JK master-slave flip-flop per feedback loop to take care of this timing. We are able to reset all these flip-flops to initialize the logic. The designer is free to choose which and how many outputs are fed back to the first matrix.

3) PLA versus ROM

A PLA is actually a big Read Only Memory with a non-exhaustive decode section that has been adapted to the implementation of random logic. How does a PLA differ from a ROM and what are the advantages?

a) **Combinational Logic**

Combinational logic is easily implemented on a read-only memory. The truth table is written in such a way that the outputs are logic functions of the inputs.



The main drawback to this scheme is that every time an input variable is added, the size of the ROM is doubled. This is because the decode scheme of the read-only memory is exhaustive. All the product terms are generated, and that soon becomes prohibitive. To do what our PLA TMS 2000 JC does through straight read-only-memory techniques would take 2^{25} words (17 external inputs and 8 inputs from the flip-flops), that is 8,288,608 words of 26 bits (18 external outputs and 8 feedback loops) – or a total capacity of 218,103,808 bits which is a ludicrous size for any read-only memory.

In a PLA all the product terms are not generated. TI has set the limit at 60 product terms for the TMS 2000 JC and to 72 for the TMS 2200 JC. These numbers have been arrived at through heuristic methods and have proven to be sufficiently large. It is not often that an equation is presented with 60 terms, each one being a product of up to 25 variables.

b) **Sequential Logic**

To perform sequential logic with a read-only memory, the outputs must be fed back to the inputs through a gating arrangement.

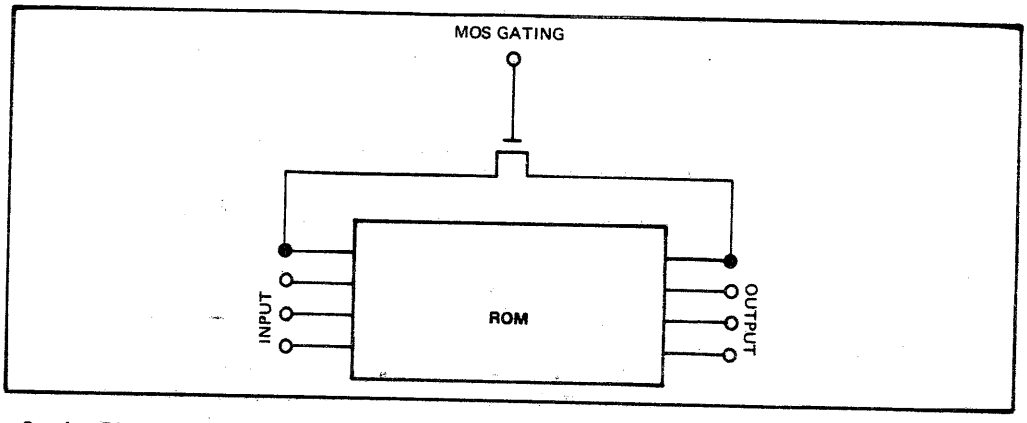
This is comparatively easy to do but has drawbacks:

- For each feedback loop two package pins are wasted.
- The gating arrangement has to be provided.
- Initialization of the logic is difficult.

In the PLAs the feedback loops are never brought outside, which saves a number of pins. The initialization is easy because JK flip-flops are used.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

ROM CONNECTED TO PERFORM SEQUENTIAL LOGIC



4) **Catalog PLAs**

TI presently markets two catalog PLAs:

TMS 2000 JC	TMS 2200 JC
40 pins	28 pins
17 external inputs	13 external inputs
18 outputs	10 outputs
8 flip-flops	10 flip-flops
60 product terms	72 product terms

These devices are produced using silicon nitride technology, which permits easy interface with TTL/DTL.

5) **Design Considerations**

a) **Logic Design**

Logic design with PLAs is easy. With the PLA approach the designer writes down the logic equations of each of the outputs in terms of the external inputs and feedback inputs.

Once this is done the programming of the matrices is handled by a computer program. A SOFTWARE PACKAGE bulletin describes in detail the mechanical aspects of the operation.

b) **Design Efficiency**

The PLA is an extremely powerful tool. The designer must be careful to use as fully as possible the capability of the PLAs. To help him do that TI has published a SOFTWARE PACKAGE bulletin and application report which includes design considerations. The PLA technique is extremely efficient from a silicon real-estate point of view.

TMS 2000 JC, NC; TMS 2200 JC, NC
PROGRAMMABLE LOGIC ARRAYS

features

- Low-threshold MOS/bipolar technology
- Static operation
- Push-pull or single-ended output buffers
- Optional internal MOS pull-up resistor on inputs
- TTL compatible
- CDIP or plastic package

description

The programmable logic array (PLA) is a device that is programmable by gate-oxide mask. It is used to perform sequential and combinational logic.

The TMS 2000 JC/NC and TMS 2200 JC/NC series are groups of programmable logic arrays manufactured using P-channel enhancement-mode low-threshold MOS and NPN bipolar techniques.

A PLA is a unique combination of master-slave JK flip-flops and static read-only memories on a single MOS/LSI chip. The programmable logic arrays have been designed to permit the implementation of custom random logic with the same low cost and quick turnaround provided by a read-only memory. Sequential and combinational logic may be implemented in a PLA. The logic is described in the form of Boolean equations, which are converted by TI software routines into the gate-oxide mask.

In the TMS 2000 JC/NC seventeen external inputs and the eight flip-flop outputs are combined by a product term generator into 60 product terms. These are then combined by a sum-of-product-terms generator into 16 lines for the 8J and 8 K inputs to the 8 JK master-slave flip-flops and into 18 external outputs. The flip-flop operation is controlled by a common reset input and a single clock.

In the TMS 2200 JC/NC thirteen external inputs and the ten flip-flop outputs are combined by a product term generator into 72 product terms. These are then combined by a sum-of-product-terms generator into 20 lines for the 10 J and 10 K inputs to the 10 JK master-slave flip-flops and into 10 external outputs. The flip-flop operation is controlled by a common reset input and a single clock.

The device inputs have optional internal pull-up resistors for easy interface. The output buffers incorporate bipolar NPN transistors and either push-pull or open-ended buffers may be chosen. These features facilitate interfacing the PLAs in TTL systems.

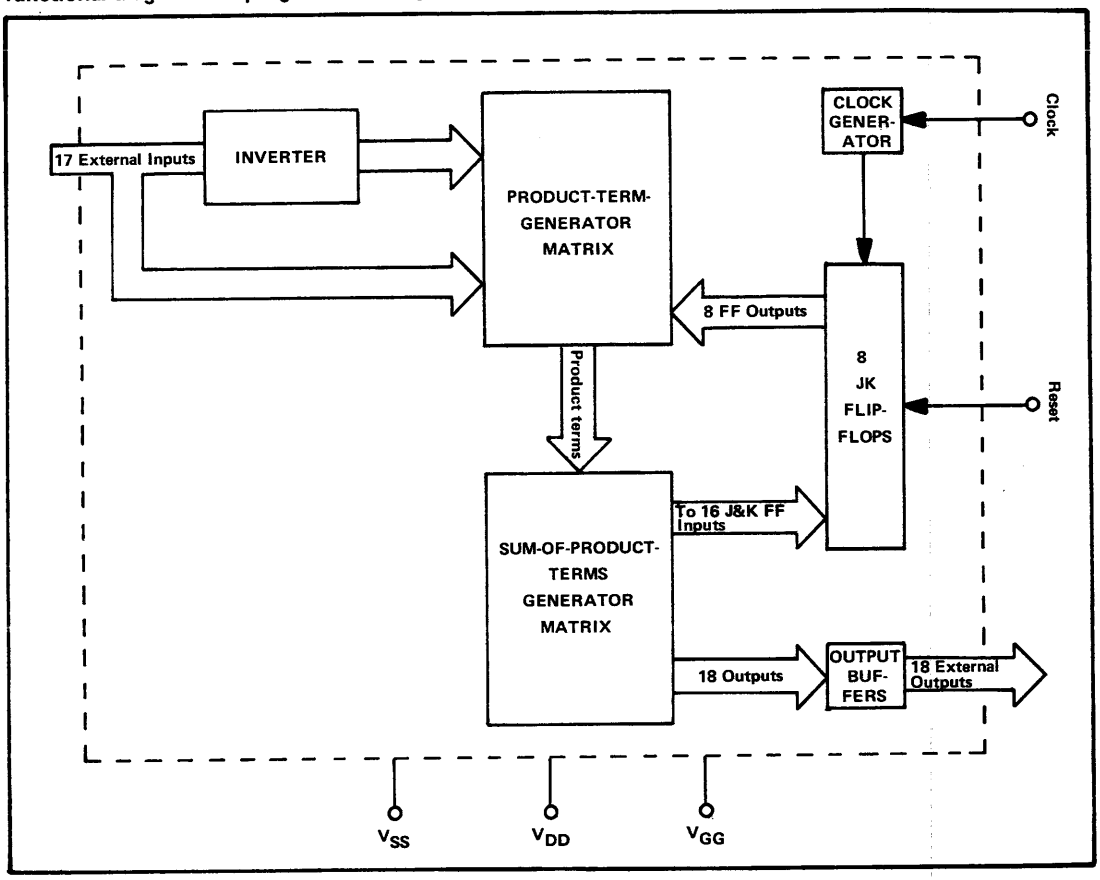
The PLAs are designated TMS 2000 JC and TMS 2200 JC when mounted in hermetically sealed ceramic dual-in-line packages. In dual-in-line plastic packages the units are numbered TMS 2000 NC and TMS 2200 NC.

organization

	TMS 2000 JC/NC	TMS 2200 JC/NC
Number of product terms	60	72
Number of external inputs	17	13
Number of external outputs	18	10
Number of JK flip-flops	8	10

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional diagram of a programmable logic array (TMS 2000 JC/NC)



operation

1) Input

The present external inputs and the previous flip-flop outputs control the state of the internal flip-flops.

2) Internal

Data is entered into the master flip-flop during the positive edge of the clock inputs, while the slave flip-flop is set during the negative edge.

The flip-flops may be reset at any time by applying a low voltage on the reset input. However, if the reset input is taken high while the clock is high, an indeterminate flip-flop state may result.

3) Output

The external outputs can be a function of the present inputs or the present flip-flop outputs, or a function of both.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See note) . . . . . −15 V to 0.3 V
Supply voltage V_{GG} range (See note) . . . . . −25 V to 0.3 V
Clock and data input voltage ranges (See note) . . . . . −15 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C
Power dissipation . . . . . 300 mW

NOTE: These voltage values are with respect to V_{SS}.

logic definition

Positive logic is assumed.

a) Logic 1 = most positive voltage

b) Logic 0 = most negative voltage

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−4.7	−10	−11	V
Supply voltage V_{GG}	−15	−17	−18.5	V
$V_{in(0)}$ with internal resistor (TTL)	−4	−5	−5.25	V
$V_{in(1)}$ with internal resistor (TTL)	0	−5	−1.5	V
$V_{in(0)}$ without internal resistor (MOS)	−4	−5	−11	V
$V_{in(1)}$ without internal resistor (MOS)	+0.3	−0.5	−1.5	V

NOTE: All voltages are with respect to V_{SS}.

The design of the unit permits a broad range of operations that allows the user to take advantage of readily available power supplies (e.g., +5 V, −5 V, −12 V).

electrical characteristics at nominal operating conditions and 25°C

PARAMETER		TEST CONDITIONS†	MIN	NOM	MAX	UNITS
$V_{out(1)}$	Logical 1 output voltage	R_L = 10 kΩ to V_{DD} (See Note 1)	0	−0.7	−1.0	V
$V_{out(0)}$	Logical 0 output voltage	R_L = 10 kΩ to V_{SS} (See Note 1)	−8	−9	−10	V
$V_{out(1)}$	Logical 1 output voltage	R_L = 6.8 kΩ to V_{GG} (Note 2)	0	−1.0	−1.5	V
$V_{out(0)}$	Logical 0 output voltage	R_L = 6.8 kΩ to V_{GG} (Note 1)	−10	−11	−17	V
$I_{in(0)}$	Input leakage current	V_{IN} = −10 V (See Note 3)			−1.0	μA
$I_{in(0)}$	With internal resistor (TTL)		−0.8	−0.9	−1.1	mA
$I_{in(1)}$	With internal resistor (TTL)		0	−40	−125	μA

† Unless otherwise noted, R_L = 10 kΩ to V_{SS}.

NOTES: 1. Push-pull output buffers used
2. Single-ended output buffer used
3. Optional input resistors not used

— continued

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics at nominal operating conditions and 25°C (continued)

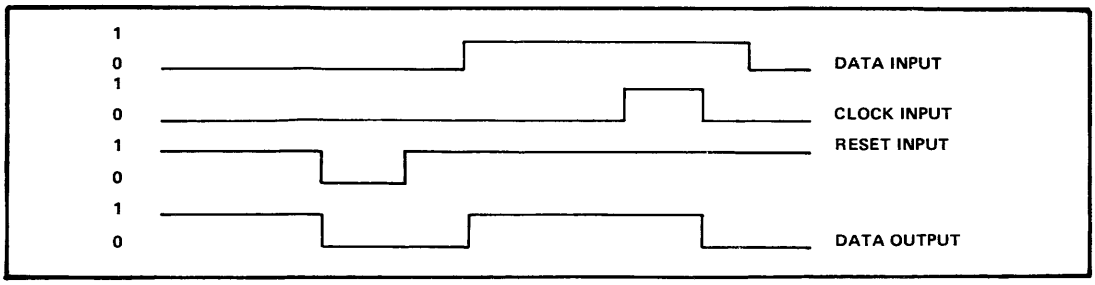
PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNITS
R_{in}	Input impedance	V_{IN} = 0 V to −10 V (Note 4)	5	7	12	kΩ
C_{in}	Input Capacitance	V_{IN} = 0, f = 1 MHz		3	5	pF
I_{DD}	Supply current into V_{DD} terminal			18	25	mA
I_{GG}	Supply current into V_{GG} terminal			1.0	4.0	mA
I_{GG}	Supply current into V_{GG} terminal	(See Note 5)		15	20	mA

NOTES: 4. Optional input resistors used
5. All outputs at logic 1

switching characteristics at nominal operating conditions and 25°C (unless otherwise noted)

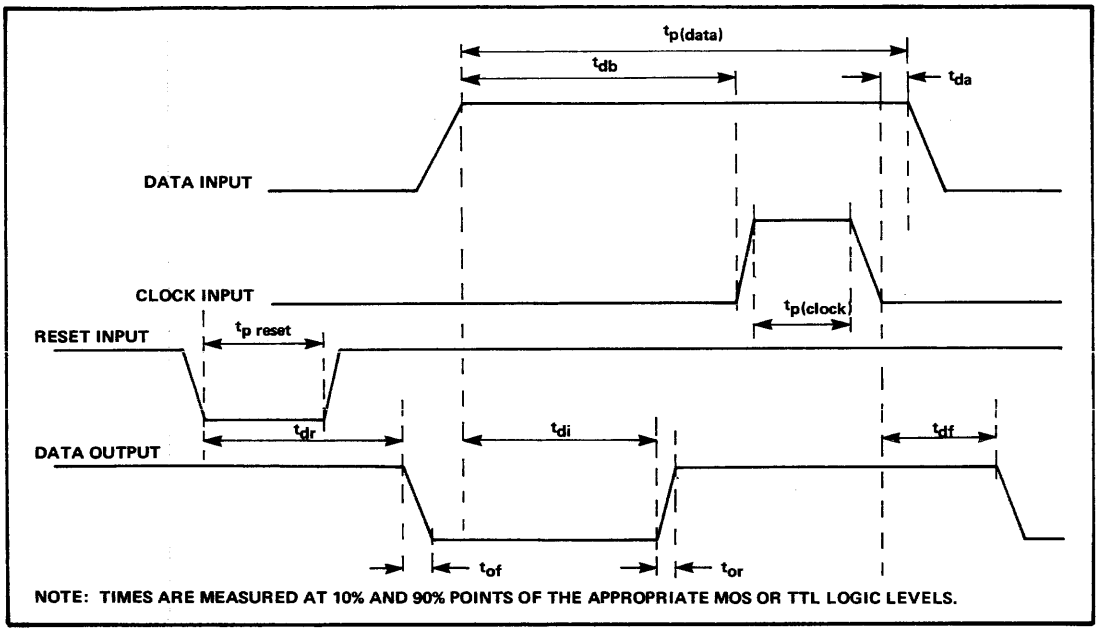
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$t_{p(data)}$	Width of data pulse	C_L = 30 pF, R_L = 1 MΩ	2.0			μs
$t_{p(clock)}$	Width of clock pulse	C_L = 30 pF, R_L = 1 MΩ	0.5			μs
$t_{p(reset)}$	Width of reset pulse	C_L = 30 pF, R_L = 1 MΩ	0.5			μs
f	Clock repetition rate	C_L = 30 pF, R_L = 1 MΩ	0		200	kHz
t_{di}	Propagation delay time from input to output with no clock	C_L = 30 pF, R_L = 1 MΩ	0.9	1.1	1.4 (25°C) 1.9 (85°C)	μs μs
t_{dr}	Propagation delay time from reset input to a change in external output	C_L = 30 pF, R_L = 1 MΩ		1.1	1.4 (25°C) 1.9 (85°C)	μs μs
t_{df}	Propagation delay time from clock input to a change in external output	C_L = 30 pF, R_L = 1 MΩ	0.9	1.1	1.4 (25°C) 2.1 (85°C)	μs μs
t_{db}	Delay time required between data input and positive edge of clock	C_L = 30 pF, R_L = 1 MΩ	1.9			μs
t_{da}	Input hold time after negative edge of clock	C = 30 pF, R_L = 1 MΩ	0.1			μs
t_{or}	Output rise time (single-ended output)	6.8 kΩ to V_{GG}	20	60	200	ns
t_{of}	Output fall time (single-ended output)	6.8 kΩ to V_{GG}	100	250	350	ns
t_{or}	Output rise time (push-pull output)	C_L = 30 pF, R_L = 1 MΩ	20	60	200	ns
t_{of}	Output fall time (push-pull output)	C_L = 30 pF, R_L = 1 MΩ	100	200	300	ns

timing diagram



14

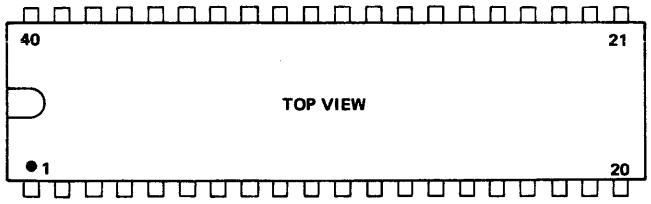
voltage waveforms



NOTE: TIMES ARE MEASURED AT 10% AND 90% POINTS OF THE APPROPRIATE MOS OR TTL LOGIC LEVELS.

pin configuration — TMS 2000 JC/NC

"TMS 2000 JC" is the part number for a unit mounted in a 40-pin hermetically sealed dual-in-line package. Mounted in a 40-pin dual-in-line plastic package, the unit is designated TMS 2000 NC.

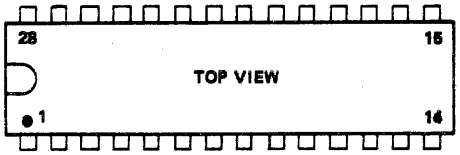


PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	V_{DD}	11	O_{10}	21	RESET	31	I_{10}
2	O_1	12	O_{11}	22	I_1	32	I_{11}
3	O_2	13	O_{12}	23	I_2	33	I_{12}
4	O_3	14	O_{13}	24	I_3	34	I_{13}
5	O_4	15	O_{14}	25	I_4	35	I_{14}
6	O_5	16	O_{15}	26	I_5	36	I_{15}
7	O_6	17	O_{16}	27	I_6	37	I_{16}
8	O_7	18	O_{17}	28	I_7	38	I_{17}
9	O_8	19	O_{18}	29	I_8	39	CLOCK
10	O_9	20	V_{SS}	30	I_9	40	V_{GG}

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

mechanical data and pin configuration — TMS 2200 JC/NC

"TMS 2200 JC" is the part number for this device mounted in a 28-pin hermetically sealed ceramic dual-in-line package. Mounted in a 28-pin dual-in-line plastic package, the unit is designated TMS 2200 NC. The packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	V_{DD}	8	O_6	15	I_1	22	I_8
2	V_{GG}	9	O_7	16	I_2	23	I_9
3	O_1	10	O_8	17	I_3	24	I_{10}
4	O_2	11	O_9	18	I_4	25	I_{11}
5	O_3	12	O_{10}	19	I_5	26	I_{12}
6	O_4	13	V_{SS}	20	I_6	27	I_{13}
7	O_5	14	RESET	21	I_7	28	CLOCK

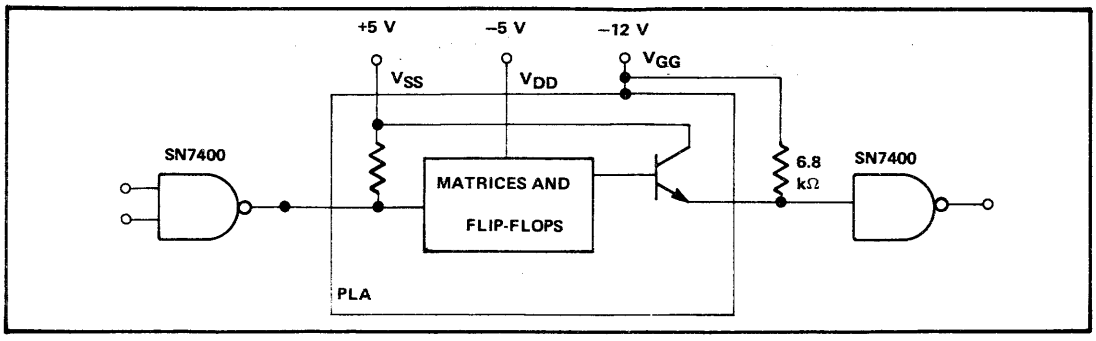
interfacing

a) To TTL system

Each external input of the PLA has an optional internal MOS pull-up resistor available for interfacing with TTL. With V_{SS} at +5 volts, this internal resistor serves to pull up a logic 1 from the TTL specified level of 2.4 V to V_{SS}.

The output buffer may be chosen at its programming stage as either push-pull or open-ended. To interface with TTL systems or when the wired-OR capability is required, the open-ended buffer would be used with an external resistor.

INTERFACE CIRCUITS WITH TTL SYSTEMS



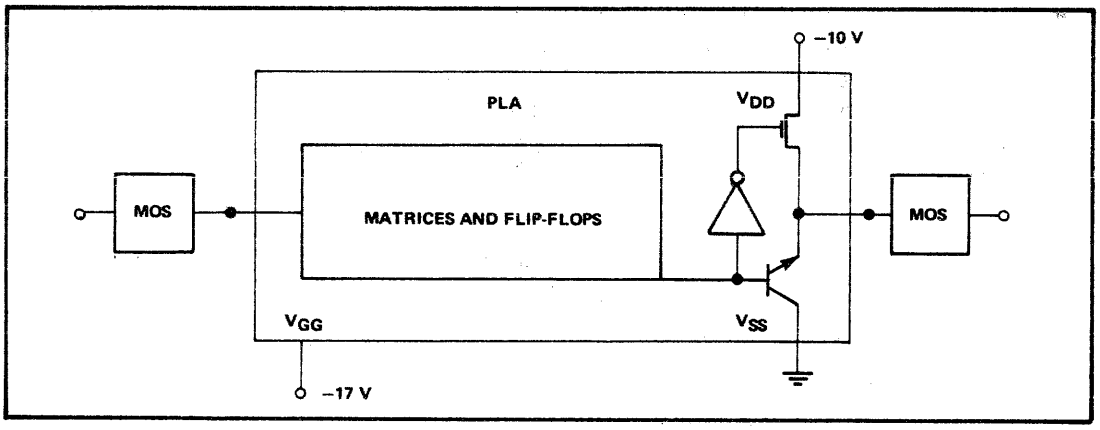
interfacing (continued)

b) To MOS systems

For input interfacing from other MOS devices, the internal pull-up resistors are not required.

The output buffer is selected as a push-pull type to provide a high-capacitive drive without the need of an external resistor.

INTERFACING WITHIN MOS SYSTEMS



custom programming

The logic functions performed by the PLA are controlled by programming or coding the product-terms-generator matrix and the sum-of-product-terms-generator matrix.

The number of different product terms is limited to 60 (TMS 2000 JC/NC) or 72 (TMS 2200 JC/NC).

The logic equations define the sum of product terms. There will be one equation for each output and for each flip-flop input. A computer program is used to implement the logic equations on the chip.

Complete information on programming Texas Instruments MOS/LSI programmable logic arrays is contained in a PLA SOFTWARE PACKAGE available from the TI field sales office.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

The rapid evolution of MOS technology has resulted in MOS memories that are competitive in cost with core memories and superior in performance. From 256 to 2000 bits, and for static or dynamic operation, MOS memories can be used for applications covering the entire spectrum of data handling systems from scratch-pad to computer main-frame memories.

1) Characteristics

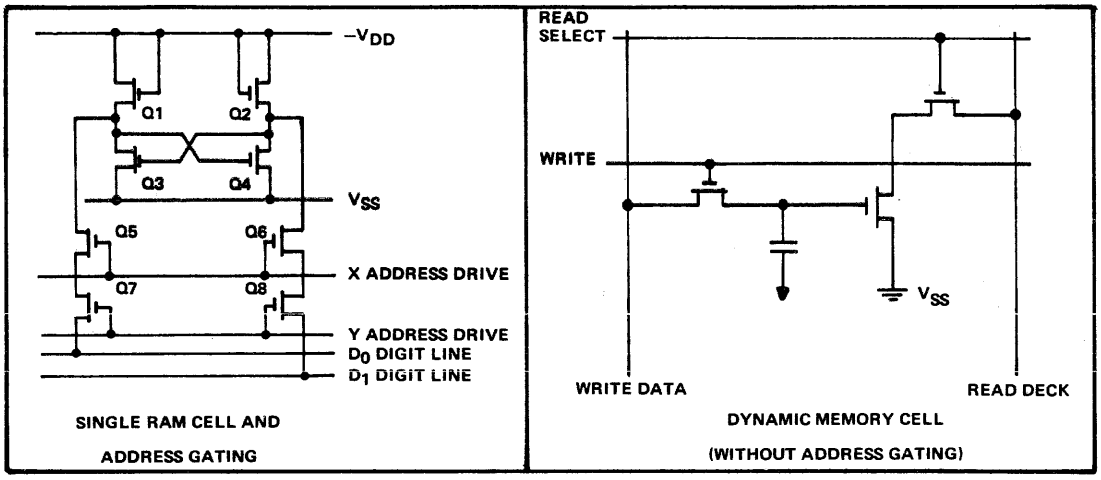
MOS RAMs are ideally suited for those applications requiring high speeds and low power dissipation. They can replace core memories used for scratch pads or for computers, while offering faster access times and a simpler drive circuitry. Their low access times make them attractive in applications where other semiconductor memories were considered, but found unsatisfactory for reasons of cost, power dissipation, or package count. For small systems, fully-decoded memories are easier to use. However, the speed of a fully decoded random-access memory is less than the speed of an off-the-chip bipolar decode X-Y select memory.

Random-access memories presently on the market are either static or dynamic.

- STATIC – An MOS flip-flop is used to store the information. Clocks are not needed. The data will stay in storage as long as the power is maintained.
- DYNAMIC – MOS capacitors are used as data storage elements. Data must be refreshed to assure integrity.

Random-access memories can also be defined as:

- Fully-Decoded Memories – A binary address determines the location in which the Write or Read operation is performed.
- Two-Dimensional Decode – The address of the word is given by an X-Y select.



SINGLE RAM CELL AND ADDRESS GATING

DYNAMIC MEMORY CELL (WITHOUT ADDRESS GATING)

2) Features

Whatever type of MOS RAM is considered, the following features are inherent:

- Nondestructuve Read out – In an MOS RAM the reading of information does not affect the content stored. So it is not necessary to perform a Write after every Read operation as is normal for magnetic memories. This is why the important parameter in an MOS memory is the access time rather than cycle time.
- Speed – Speeds of 150 ns with separate decoding, or 300 ns with decoding on the chip are typical.
- Power Dissipation – Power dissipation is typically less than 1-tenth mW per bit.
- Flexibility – MOS memories are available in much smaller sizes than the equivalent core memories. The memory configuration is very flexible and can be altered without appreciably increasing the basic price.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

- Environmental Characteristics (temperature range, mechanical, etc.) – Semiconductors are able to work in much more rugged environment than cores with much greater reliability.
- Cost – MOS memories are already more economical than magnetic memory cores for small- and medium-size systems. Mass assembly techniques, such as beam-lead MOS devices are being used to manufacture MOS memory systems and to further reduce the cost.

3) TI Devices

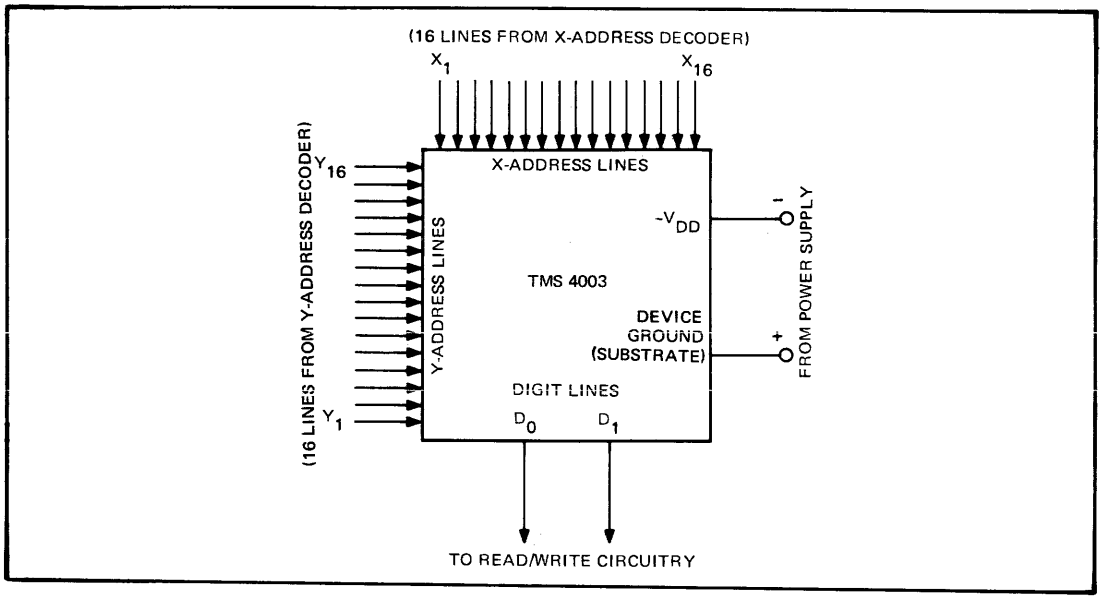
TI produces seven MOS RAM memory elements:

- TMS 1101 NC – 256-bit static RAM with decode
- TMS 4003 JR/NC – 256-bit high-speed random-access memory (with separate decode)
- TMS 1103 NC – 1024-bit dynamic RAM with decode
- TMS 4020 NC – 2048-bit dynamic RAM, high-speed, two external clocks
- TMS 4023 NC – 1024-bit dynamic RAM, medium-speed, low cost
- TMS 4025 NC – 2048-bit dynamic RAM, high-speed, low power
- TMS 4000 JC/NC – 128-bit content addressable (associative) memory

TMS 4003 JC – 256-bit high-speed random-access memory

The TMS 4003 JC/NC is a direct-address memory, having 16 X-address and 16 Y-address lines. Any one of the 256 bits in the memory can be selected by driving one X- and one Y-address line in coincidence. Sensing the logical state of the selected bit is achieved by differentially observing two outputs, D_0 and D_1, digit lines. The same digit lines are used to write information into an addressed bit. A block diagram of the TMS 4003 is shown on the following page.

DESCRIPTIVE BLOCK DIAGRAM OF THE TMS 4003 MOS RAM



No clock signals are required to operate the TMS 4003 JC/NC or to retain information. Such a design is referred to as static as distinguished from dynamic which requires the continuous application of single or multiple clock signals to function properly.

The memory organization of the TMS 4003 JC/NC is referred to as 256-words-by-1-bit, because an address can only select one bit at a time. Larger memory systems can be constructed using this 256 X 1 memory as a basic cell.

Paralleling address lines can increase word size. For example, if eight memories were connected by tying their respective X- and Y-address lines together, a 256-word by 8-bit memory would be formed. A single X-Y address applied to this system would produce eight separate digital outputs.

The number of words can be increased by paralleling digit lines. For instance, to make a 1024-word by 1-bit memory plane, four 256 X 1 memories are used, resulting in 32 X-address and 32 Y-address lines and a single output consisting of two digit lines.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Memory planes like the one described can be paralleled in the same manner as individual memories. If eight 1024 X 1 planes, for example, had their corresponding X- and Y-address lines connected together, a 1024 X 8 memory system would result. A total of 32 TMS 4003 JC/NC MOS RAMs would be necessary for such a system. Even larger systems are possible, the ultimate size being limited by the drive capabilities of the external address and write circuitry.

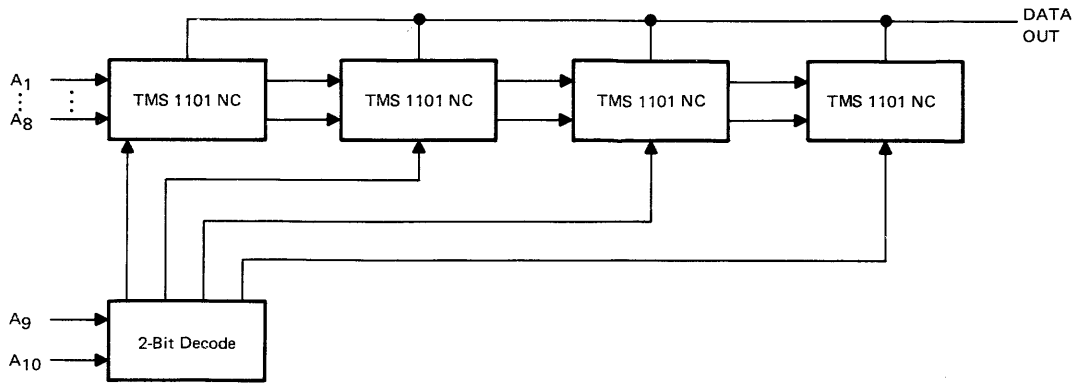
TMS 1101 NC — 256-bit random-access memory with decode

The TMS 1101 NC is a 256-bit fully decoded static random-access memory. Any one of the 256 bits in the memory can be selected by properly addressing the eight address lines. All inputs and outputs of TMS 1101 NC, including addresses and control logics, are fully TTL/DTL compatible; this will minimize interface problems in system designs.

The TMS 1101 NC is a full static circuit; no clock signals are required in operating the circuit.

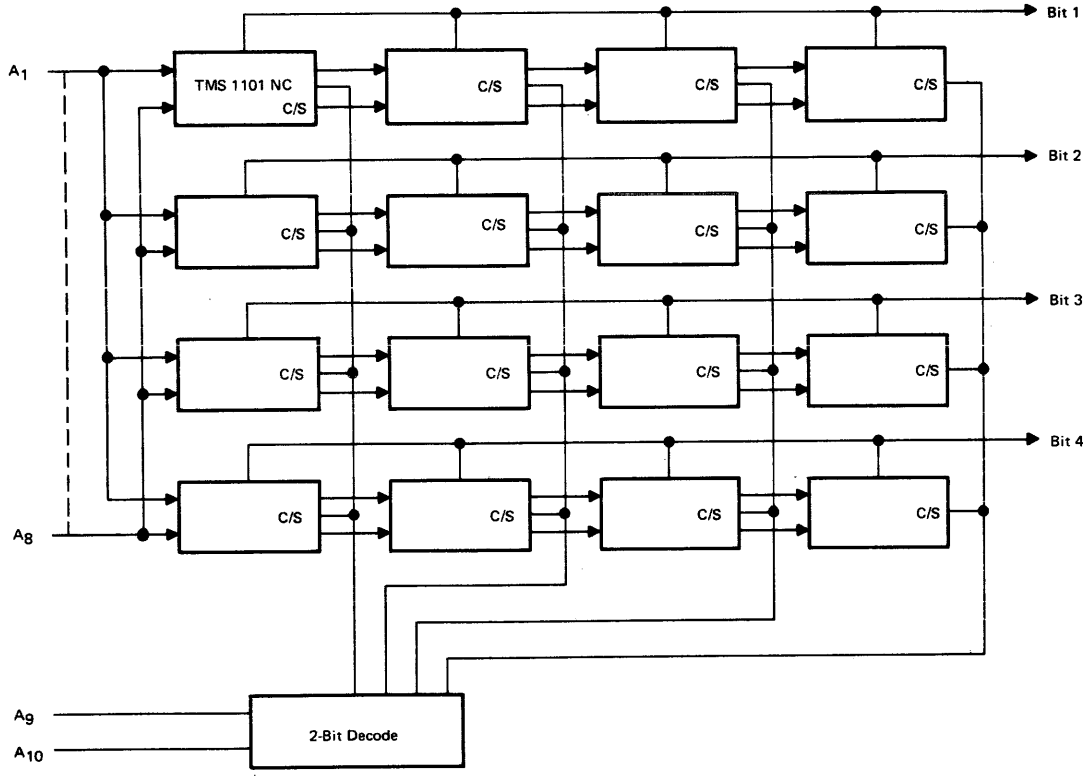
A chip-select control provided by the TMS 1101 NC allows several circuits to be wired-OR together, which makes the expanded organization of the memory a very simple operation.

The TMS 1101 NC can be considered to have a 251-words-by-1-bit organization. To expand the bit length of a word from 1 bit to n bits, it is only necessary to connect all address lines and control logics of n circuits in parallel. To increase the word size from 256 words to as many as m times 256 words, a decoder must be provided to select one out of m circuits which are all wired-OR together. Chip select controls of the circuits provide the means for the above expansion. A memory size of 1K words X 1 bit using TMS 1101 NC is illustrated in the following block diagram.



ORGANIZATION OF 1K-X-1 MEMORY USING TMS 1101 NC

To expand the 1K-X-1 memory into 1K X 4, the 2-bit decode can be shared by the four 1K planes as shown:



ORGANIZATION OF 4K-X-4 MEMORY USING TMS 1101 NC

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

By the same approach, memory size of any word length and bit length can be organized easily using TMS 1101 NC.

There are several common factors in the following circuits:

- TMS 1103 NC – 1024-bit dynamic RAM
- TMS 4020 NC – 2048-bit dynamic RAM
- TMS 4023 NC – 1024-bit dynamic RAM
- TMS 4025 NC – 2048-bit dynamic RAM

For example, they are all dynamic; all provide an output sense current. However, there are also many characteristics which distinguish one circuit from the other. The table below lists key parameters of each memory circuit.

RAM Key Parameters

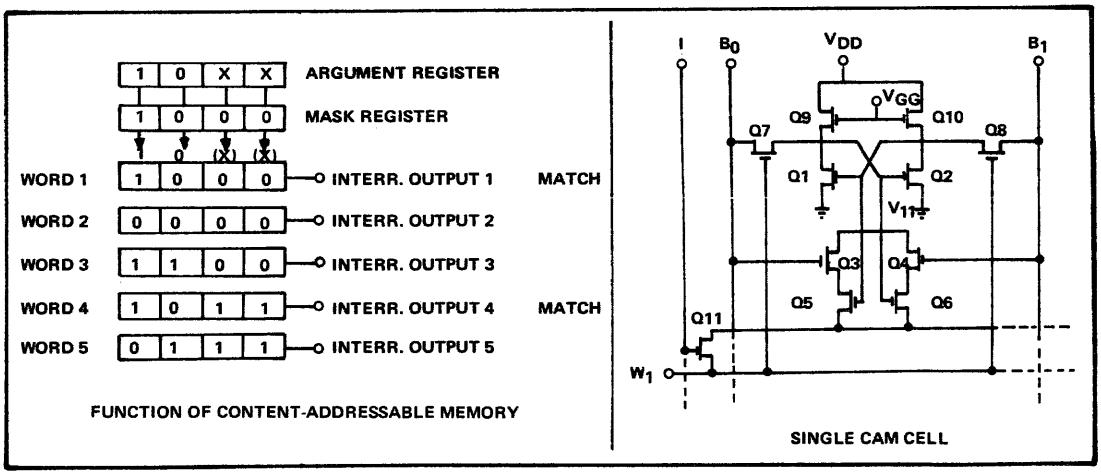
PARAMETER	UNITS	TMS 1103 NC	TMS 4020 NC	TMS 4023 NC	TMS 4025 NC
Total Bits	Bits	1024	2048	1024	2048
Organization	Bits	1024 X 1	1024 X 2	1024 X 1	1024 X 2
Access Time (min)	ns	300	320	650	280
Cycle Time (min)	ns	580	640	900	640
Power per bit at minimum cycle time and 25°C	mW/bit	0.3	0.15	0.08	0.07
Sense Current (min)	mA	0.6	1.2	1.0	1.2
Process		Si-Gate	S-A Gate	Nitride	S-A Gate
Refresh Period	μs	2	2	2	2
Read Cycle/Refresh Period		32	16	32	16
Chip Select/1K bit		1	2	1	1
Package		18-pin PDIP	24-pin PDIP	24-pin PDIP	24-pin PDIP

All dynamic memory cells use MOS capacitance and PN junction capacitance (parasitic) as temporary charge storage elements. However, due to the leakage property of PN junctions, charges stored in the capacitances must be restored periodically to assure the integrity of the information. This refreshing rate is temperature dependent, and must be performed once every two μs at 70°C. At room temperature the refreshing rate can be once every 50 μs.

In the dynamic RAM circuits, a refreshing operation is always performed during a Read cycle. The minimum number of Read cycles that must be performed in each refreshing period is dependent upon the organization of memory arrays. By considering the digit lines as a memory matrix or columns, and the Read or Write select lines as rows, all cells in the row selected during a Read cycle will be refreshed. Therefore, the minimum number of Read cycles required in each refresh period is the same as the number of rows in the memory matrix. For example, TMS 1103 NC is organized 32 rows X 32 columns; 32 Read cycles are required in each refresh cycle. TMS 4025 NC is organized 16 rows X 64 columns; therefore only 16 Read cycles are required.

All the dynamic RAMs (TMS 1103 NC, TMS 4020 NC, TMS 4023 NC, and TMS 4025 NC) have one or more chip-select controls; therefore, expansion of memory organization into any size can be achieved easily as shown in the preceding paragraphs on TMS 1101 NC.

The concept of a content-addressable memory has been around for many years but because of cost has not previously been practical. However, the performance and economics of MOS integrated circuits now make the concept highly desirable from both technical and cost standpoints. MOS integrated-circuit technology has finally made practical the content-addressable memory.



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

A content-addressable memory (CAM) is a cell in which the words contained can all be matched simultaneously against an argument word, and outputs given wherever a true match is obtained. Each word has a Write input which can also be used to interrogate that word for a match. Two bit lines run through each column of cells allowing the word data to be written in. They may also be used for reading the contents of a word or for masking parts of the argument word where a "Don't Care" state exists.

In the basic CAM cell transistors, Q_1, Q_2, Q_9 and Q_{10} compose a flip-flop for data storage. Q_7 and Q_8 are selection transistors which, when turned On by the application of a negative voltage to the W line, connect the flip-flop nodes to the B_0 and B_1 bit lines. When the W line is at a 0, Q_7 and Q_8 are Off, isolating the flip-flop from the bit lines. Transistors Q_3, Q_4, Q_5, Q_6 and Q_{11} perform the Interrogate logic. For this mode each W line is grounded through a small resistor and Q_{11} is turned On. Transistors Q_3, Q_4, Q_5 and Q_6 compare the state of the memory cell flip-flop with the voltages externally applied to the bit lines. Thus the Word lines are controls for Write and Read operations but outputs for the Interrogate operation. The bit lines are inputs for Write and Interrogate, but outputs for Read.

TMS 1101 JC, TMS 1101 NC
256-BIT RANDOM-ACCESS MEMORY

features

- Low power dissipation
- 600-nsec access time (typ), 750 nsec (max)
- Direct DTL and TTL compatibility
- Wire-OR capability
- Fully decoded on chip
- Inputs fully protected
- Data Out and $\overline{\text{Data Out}}$ available
- Single chip-select line
- Single Read/Write line

description

The TMS 1101 JC/NC is a 256-bit RAM, organized as 256 one-bit words and using P-channel enhancement-mode (normally Off) MOS transistors. The TMS 1101 JC/NC will interface directly with standard TTL and DTL bipolar integrated circuits. A separate chip-select lead allows easy selection of an individual package when outputs are used in a wire-OR fashion.

logic definition

Positive logic is assumed.

a) LOGICAL 1 = most positive voltage

b) LOGICAL 0 = most negative voltage

operation

An 8-bit address code selects any one of 256 bits for either Read or Write operation — all address input levels being TTL or DTL logic levels.

A logic 0 level applied to the R/W control will result in a Read operation, and may be presented simultaneously or before application of the address code. Read-out is non-destructive.

A logic 1 level applied to the R/W control will create the condition for the Write operation. The duration of the Write command must be at least 400 nanoseconds to ensure that the data is written into the memory. The Write command should be Off by the time the address code is changed. The input data should coincide with at least the last 300 nanoseconds of the Write command.

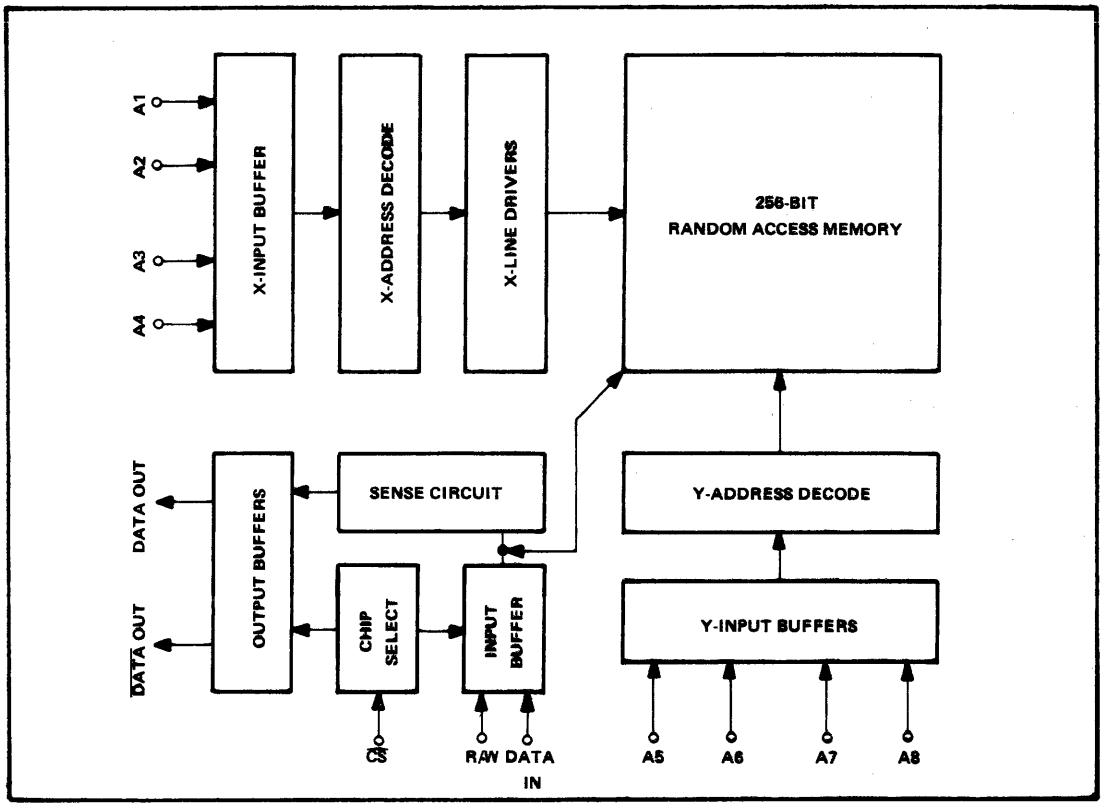
The memory is inhibited with the application of a logic 1 to the chip-select line. This action renders the Read/Write line and data inputs ineffective. The address decode will not be inhibited. Also, the output leads are open when the array is inhibited, allowing many chips to be wired-OR together.

A unit mounted in a 16-pin hermetically sealed ceramic dual-in-line package is designated "TMS 1101 JC". Mounted in a 16-pin plastic dual-in-line package, the device is numbered "TMS 1101 NC".

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_D range (See Note 1)	−20 V to 0.3 V
Supply voltage V_{DD} range (See Note 1)	−20 V to 0.3 V
Data input voltage range (Note 1)	−20 V to 0.3 V
Storage temperature range	−55°C to 150°C
Operating free-air temperature range	−25°C to 85°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate supply V_{SS}	+4.75	+5.0	+5.25	V
Supply V_{DD}	−9.50	−10.0	−10.50	V
Supply V_D	−9.50	−10.0	−10.50	V
Logic Levels				
Input HIGH level V_{IH}	+3.5			V
Input LOW level V_{IL}			+0.6	V
Pulse Timing				
Write Pulse Width t_{WP}		400		ns
Write Delay t_{Wd}		0		ns
Write Time t_W	300			ns
Data Overlap t_{DO}	100			ns

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Current				500	nA
Output Current						
I_{LO}	Leakage current				1000	nA
I_{OL}	Sink current	V_{OUT} = 0.4 V	1.6			mA
	Source current	V_{OUT} = 0.0 V		0.1		mA
Output Voltage						
V_{OL}	Output LOW voltage				+0.4	V
V_{OH}	Output HIGH voltage		+4.0			V
Capacitance						
C_{IN}	Input	V_{IN} = +5 V, F = 1 MHz			10	pF
C_{OUT}	Output	V_{IN} = +5 V, F = 1 MHz			10	pF
Power Supply Current						
V_{DD}	Supply				13	mA
V_D	Supply				19	mA

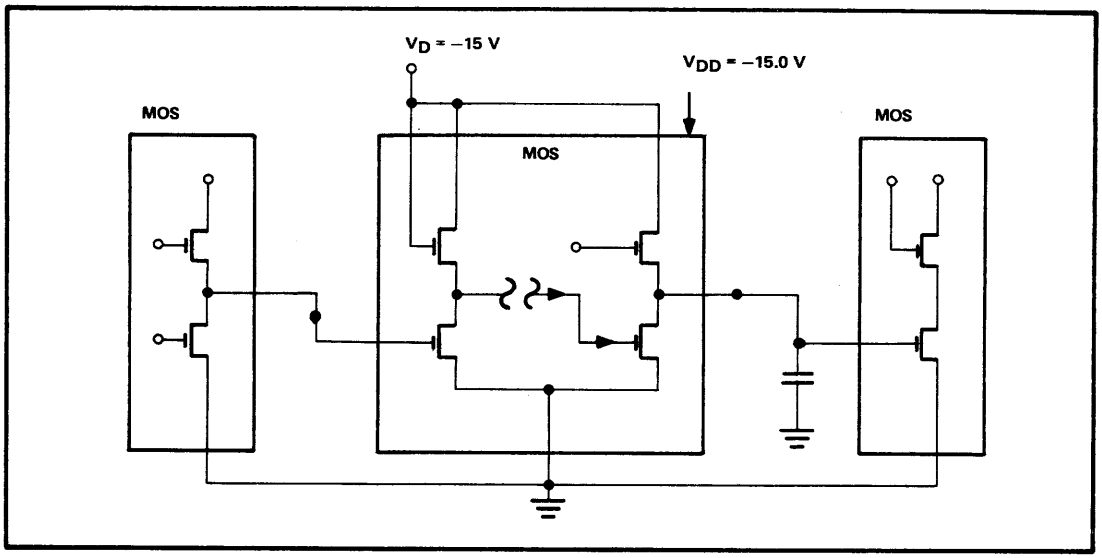
dynamic electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNITS
Access Time					
t_{AL}	Output LOW level		600	750	ns
t_{AH}	Output HIGH level		600	750	ns

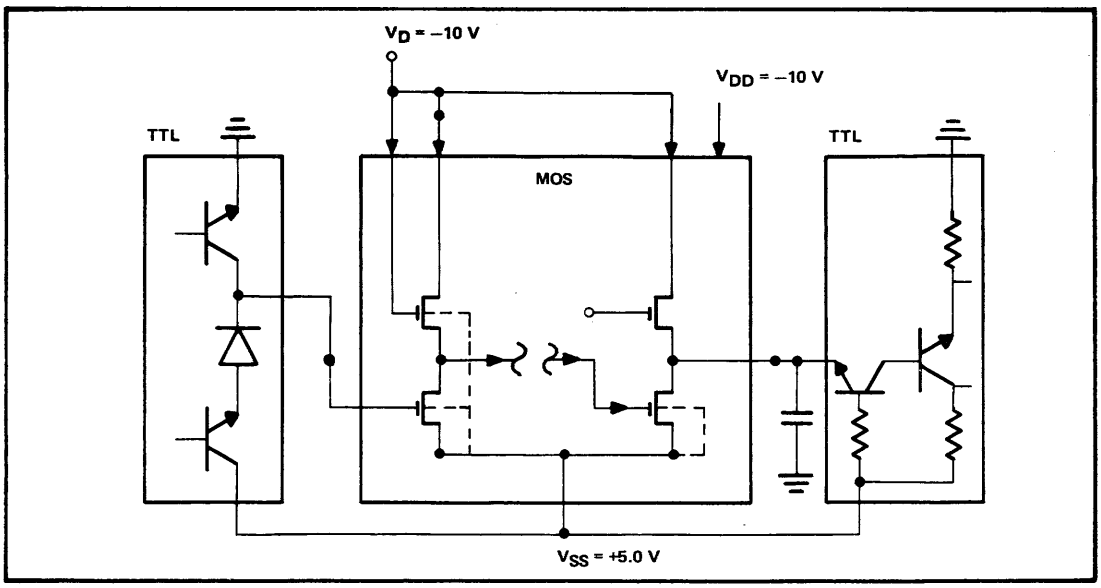
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

interface circuits

a) MOS

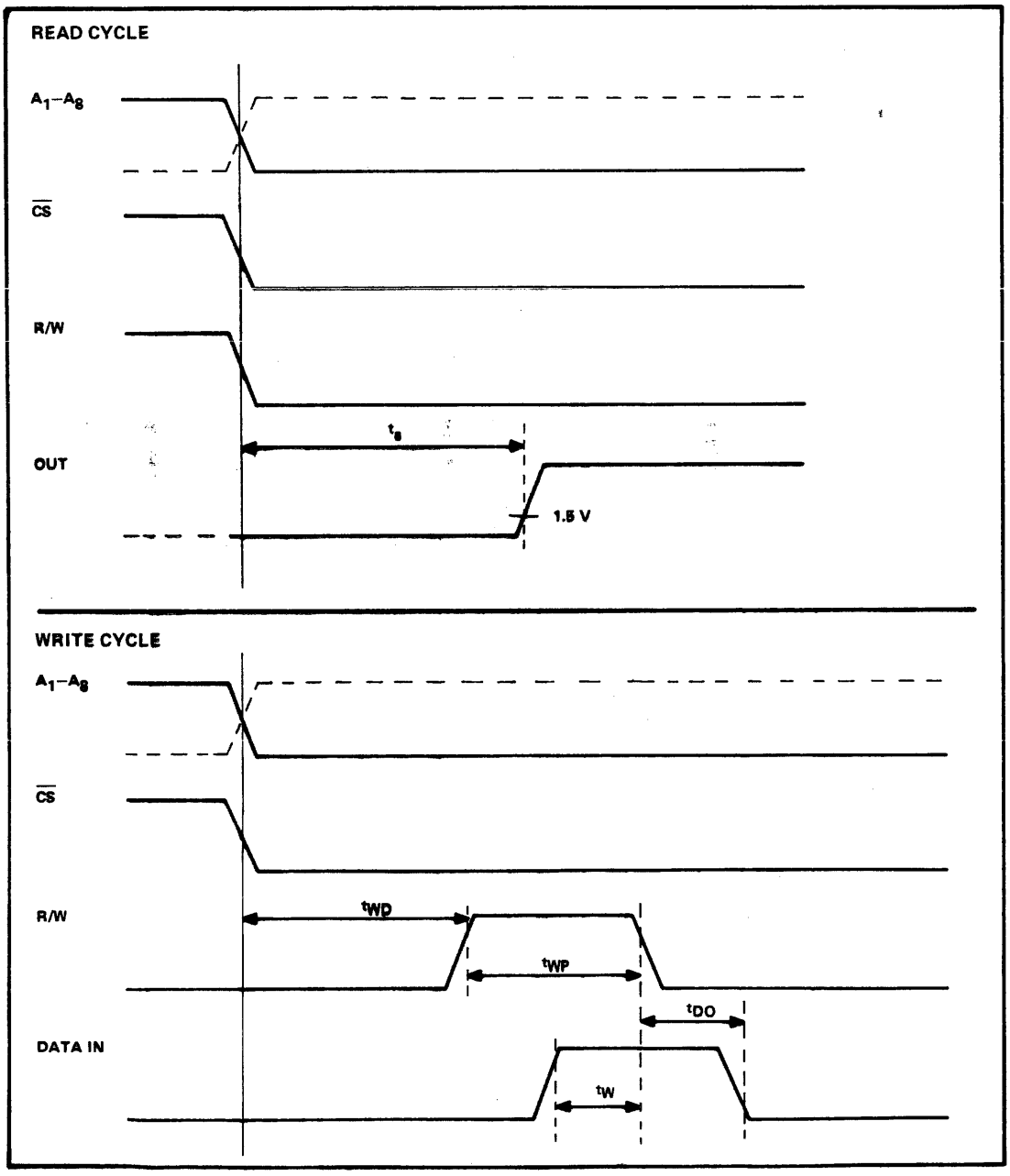


b) TTL



14

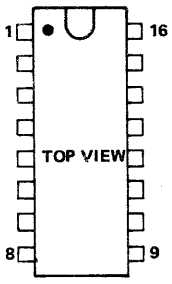
timing diagram and voltage waveforms



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

mechanical data and pin configuration

The device is available in both a 16-pin hermetically sealed ceramic dual-in-line package (TMS 1101 JC) and in a 16-pin plastic dual-in-line package (TMS 1101 NC). The packages are designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Address 6	9	Address 3
2	Address 8	10	Address 2
3	Address 7	11	Address 4
4	V_D	12	Data in
5	V_{SS}	13	Data out
6	Address 5	14	$\overline{\text{Data out}}$
7	Address 1	15	Read/Write
8	V_{DD}	16	$\overline{\text{Chip Select}}$

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 1103 NC
FULLY-DECODED 1024-BIT RAM

features

- Low power dissipation
- Cycle time – 500 nsec
- Access time – 300 nsec
- Expansion capability
- Fully decoded
- Static charge protection
- 18-lead plastic package

description

The TMS 1103 NC is a low-cost main-frame memory design used for large-storage high-performance applications.

Organized as a 1024- by 1-bit random access memory, the TMS 1103 NC is a fully decoded monolithic array. This feature permits the use of an 18-pin dual-in-line package.

This dynamic memory has nondestructive readout, and refreshes all 1024 bits in 32 Read cycles.

Utilizing the latest silicon-gate low-threshold technology makes possible a high functional density.

logic definition

a) LOGICAL 1 = most positive voltage

b) LOGICAL 0 = most negative voltage

operation

Refer to functional block diagram and timing diagram. Access begins time t_{AC} before the negative transistion of chip enable. In this duration the precharge is active and the row and column decoders settle out. Next, during the period t_{OV}, the contents of the 32 cells along the selected row are written into the refresh amplifiers. One is required at each column of the array. During the overlap interval, the data output is held high by the selected column amplifier. At the positive transistion of precharge, the contents of the refresh amplifiers are rewritten into their respective columns and the data output is valid t_{PO} later. A suitable time t_{PW} after precharge, the state of the In Data line may be copied into the selected cell using a Write pulse of minimum time t_{WP}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

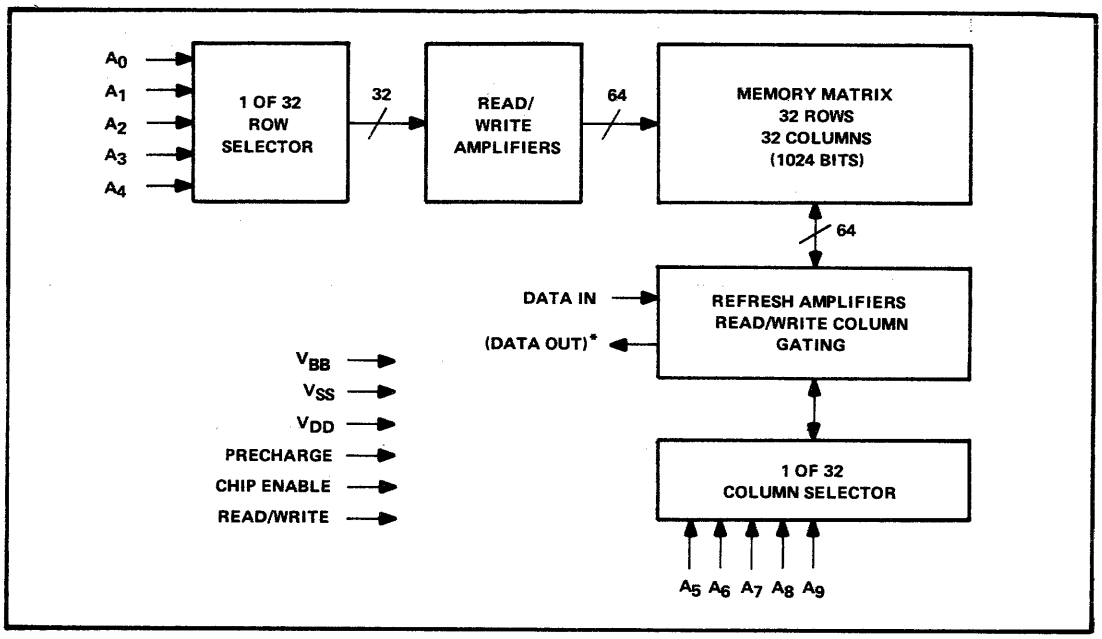
Supply voltage V_{DD} range (See Note 1)	–24 V to 0.3 V
Clock input voltage range (See Note 1)	–24 V to 0.3 V
Data input voltage range (See Note 1)	–24 V to 0.3 V
Operating free-air temperature range	–25°C to 70°C
Storage temperature range	–55°C to 150°C

NOTE 1: These voltage values are with respect to V_{BB} (substrate).

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram and pin configuration



recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
System ground V_{SS}	+15	+16	+17	V
Drain supply V_{DD}		0		
Substrate bias supply V_{BB}	$V_{SS}+3$	$V_{SS}+3.5$	$V_{SS}+4$	V
Pulse Timing				
Precharge pulse width t_{PC}	240	250	315	ns
Precharge and Chip Enable overlap t_{OV}	0	10	100	ns
Address set-up time to Chip Enable t_{AC}	150			ns
Precharge to Read/Write t_{PW}	200		500	ns
Read/Write pulse width (Note 1) t_{WP}	70			ns
Address to valid output t_{ACC1}	300			
Precharge to valid output t_{ACC2}	390			
Refresh interval t_{REF}			2	ms
Precharge to end of Chip Enable t_{POV}	200		600	ns
Precharge to valid output t_{PO}		110	150	ns
Write or Read/Write Cycle t_{WC} or t_{RWC}	580			
Read Cycle t_{RC}	580			

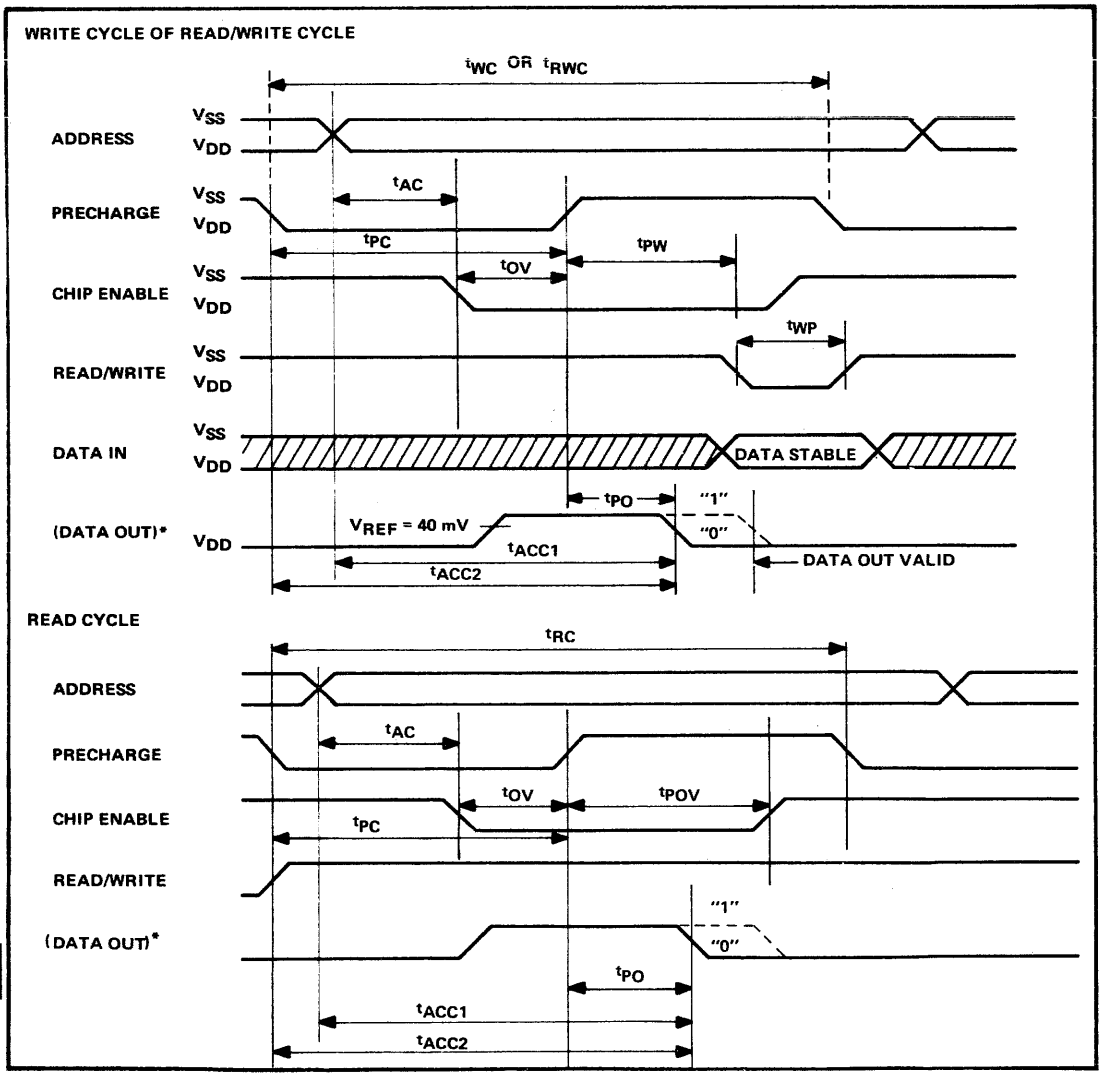
NOTE: 1. Data IN must be stable during t_{WP} and remain stable for at least 20 ns after t_{WP}.

14

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNITS
V_{IL}	Input LOW voltage		$V_{SS}-17$	$V_{SS}-16$	$V_{SS}-15$	
V_{IH}	Input HIGH voltage		$V_{SS}-1$	V_{SS}	$V_{SS}+1$	
I_{IN}	Input Load Current				1	μA
I_{OH}	Output HIGH Current		700	900		μA
I_{OL}	Output Leakage Current				1	μA
I_{DD}	Average V_{DD} Current	t_{PC} = 240 ns		14	20	mA

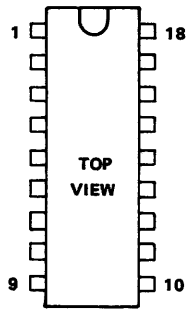
timing diagram and voltage waveforms



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

mechanical data and pin configuration

The TMS 1103 NC is mounted in an 18-pin plastic dual-in-line package. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	A_3	10	V_{BB}
2	A_2	11	V_{DD}
3	A_1	12	Data In
4	A_0	13	A_8
5	Precharge	14	(Data Out)*
6	A_9	15	A_4
7	A_6	16	Chip Enable
8	A_5	17	V_{SS}
9	A_7	18	Read/Write

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS
LSI

TMS 4000 JC, TMS 4000 NC
HIGH-SPEED CONTENT-ADDRESSABLE MEMORY

features

- Static operation
- Nondestructive readout and interrogation
- High-speed operation — 250-ns typical system cycle time
- Low standby power dissipation
- Masked write and interrogation capability
- Low threshold technology

description

The TMS 4000 JC/NC is a high-speed content-addressable memory organized as 16 eight-bit words. The entire device is constructed on a single monolithic chip using low-threshold MOS P-channel enhancement-mode transistors. Active-element design permits nondestructive readout and interrogation of memory contents. Bit lines can be wire-OR connected to obtain memory planes greater than 16 words. Word lines can be wire-OR connected to achieve word lengths of greater than eight bits per word. Selection of a given word for reading or writing is accomplished by connecting the selected word line to a negative voltage while holding all other word lines at ground. The common interrogation control 1, when returning to a negative voltage, allows all sixteen words to be interrogated simultaneously.

Memory writing is accomplished by addressing a desired word and bringing the appropriate bit lines to ground while holding the other bit lines at a negative potential. If both lines of a selected bit are held at the negative potential, the information in the bit will be unchanged during a writing cycle. Masked writing therefore can be achieved.

Reading each bit content of an addressed word requires sensing differential current between the two bit lines. Both lines should be held near a logic 1.

Interrogation of memory content is accomplished by activating the interrogation command I, bringing bit lines to appropriate voltages, and simultaneously sensing the current in each word line. If both bit lines of a particular bit are held at ground potential during an interrogation cycle, that bit will be excluded from the interrogation. If a word perfectly matches the interrogation information, no current will flow through the word lines. One or more mismatches will cause at least 200 μA to flow in the word line.

"TMS 4000 JC" designates a unit mounted in a 40-pin hermetically sealed dual-in-line package, and "TMS 4000 NC" is the number for a unit mounted in a 40-pin dual-in-line plastic package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage at any terminal relative to substrate (GND) . . . . . +0.3 V to −14 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

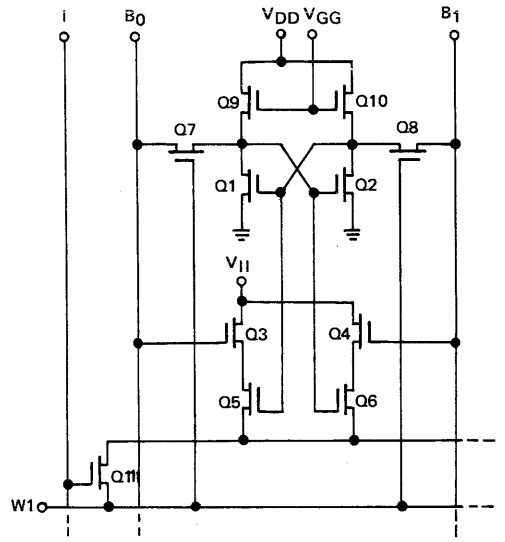
recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{GG}	−11	−12	−13	V
Supply voltage V_{DD}	−11	−12	−13	V
Supply voltage V_{II}	2.7	−3	−13	V
Write time (t_W)	60			ns
Settling time (t_s)	50			ns

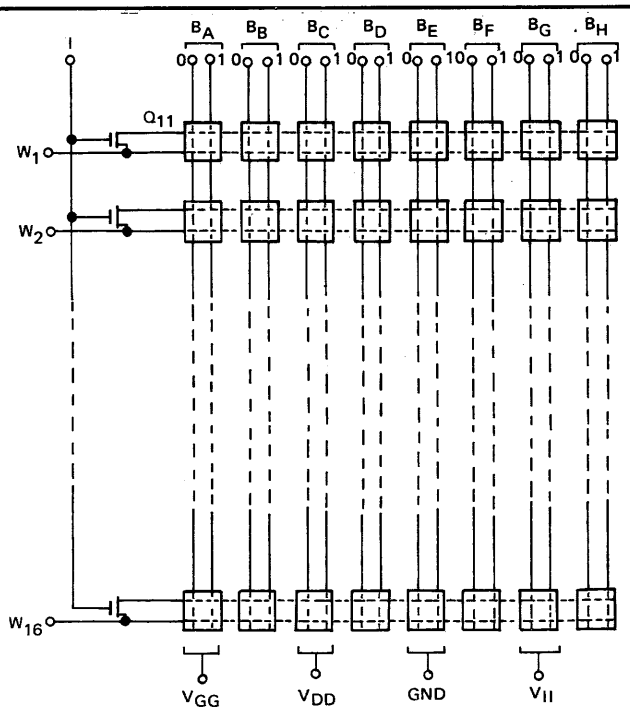
14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CONTENT-ADDRESSABLE MEMORY CELL



CONTENT-ADDRESSABLE MEMORY ORGANIZATION



14

logic definition

Negative logic is assumed

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

OPERATION	INPUT VOLTAGE				OUTPUT SIGNALS
	I	W	B_0	B_1	
Write 0	0	1	1	0	
Write 1	0	1	0	1	
Masked Write	0	1	1	1	
Read 0	0	1	1	1	Current in B_1 (200 μA minimum)
Read 1	0	1	1	1	Current in B_0 (200 μA minimum)
Interrogate 0	1	0	1	0	Current in W indicates mismatch (200 μA minimum)
Interrogate 1	1	0	0	1	
Masked Interrogate	1	0	0	0	No current in W from this bit
Standby	0	0	X	X	(See Note 1)

NOTE 1: X = 1 or 0 (don't care)

electrical characteristics (under nominal operating conditions at 25°C, unless otherwise noted)

R_L = 100 Ω (See CAM operational requirements)

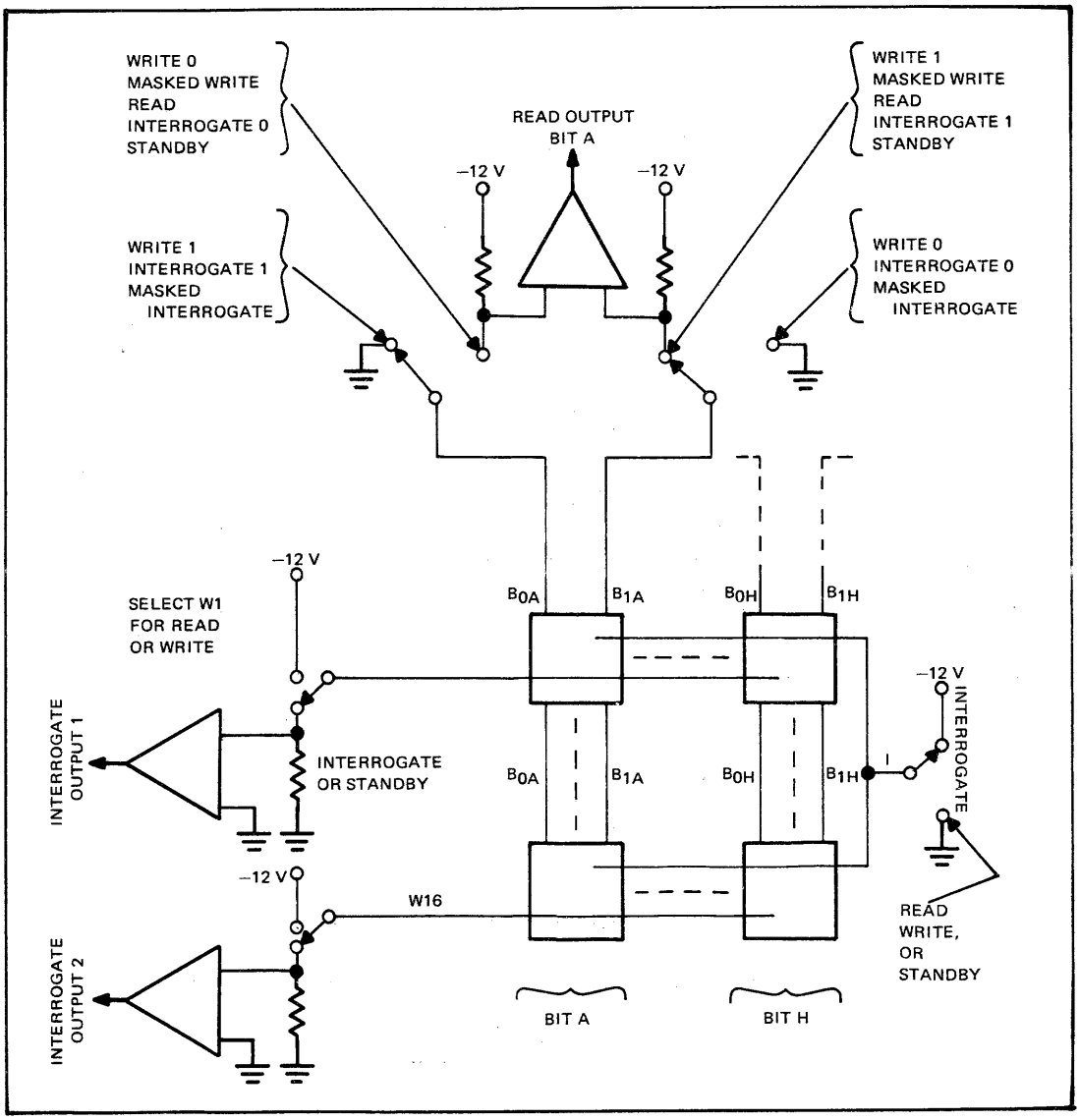
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
	Read-mode sense current	Logic 0 stored in a bit cell	B_0			−10	μA
			B_1	−200	−400		
		Logic 1 stored in a bit cell	B_0	−200	−400		
			B_1			−10	
	Interrogate-mode sense current	Matched				−10	μA
		One bit mismatched		−200	−400		
		All bits (8) mismatched			−2000	−3000	
I_B	Bit-line leakage current	16 in parallel @ −12 V				10	μA
I_W	Word-line leakage current	16 in parallel @ −12 V				10	μA
I_I	Interrogate line leakage current	At −12 V				100	μA
I_{DD}	Drain supply current				3.0	5.0	mA
I_{II}	Interrogation supply current per word	One bit mismatched		-0.2	−0.4		mA
		All bits (8) mismatched			−2.0	−3.0	
	Total power dissipation	Standby			40	60	mW
		Read or Write				100	
		Interrogation				200	
C_B	Bit-line capacitance	V_B = 0 V,	f = 1 MHz		13		pF
C_W	Word-line capacitance	V_W = 0 V,	f = 1 MHz		12		pF
C_I	Interrogate-line capacitance	V_I = 0 V,	f = 1 MHz		40		pF

switching characteristics (under nominal operating conditions at 25°C, unless otherwise noted)

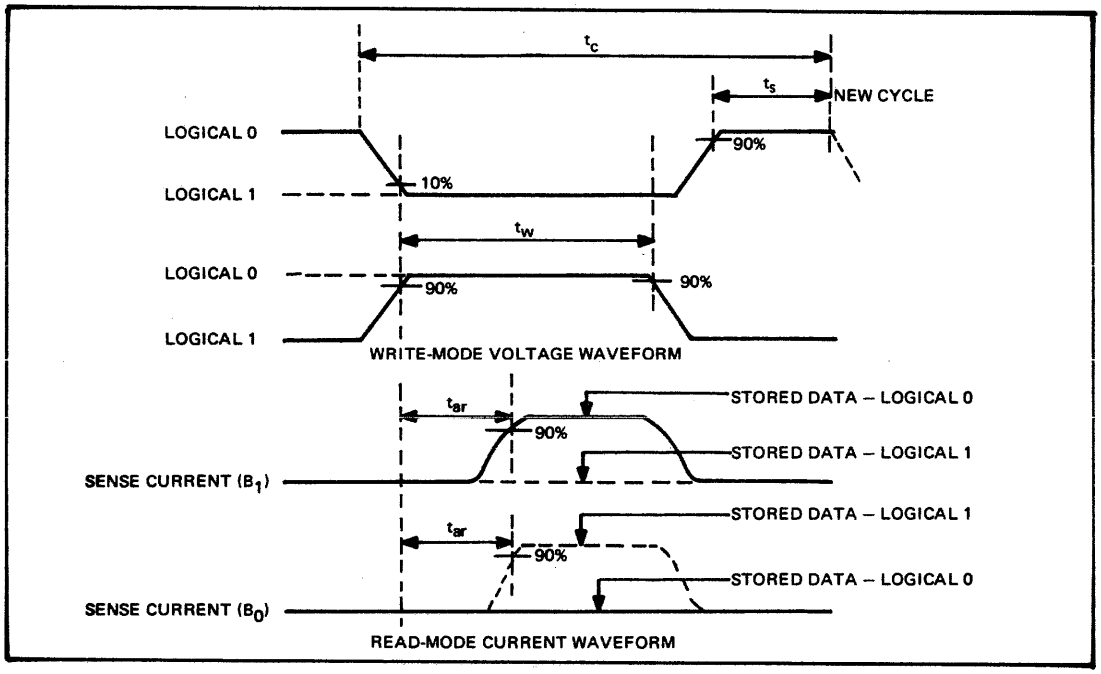
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_s	Settling time				50	ns
t_{ai}	Interrogate access time			50	80	ns
t_{ar}	Read access time			30	60	ns

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

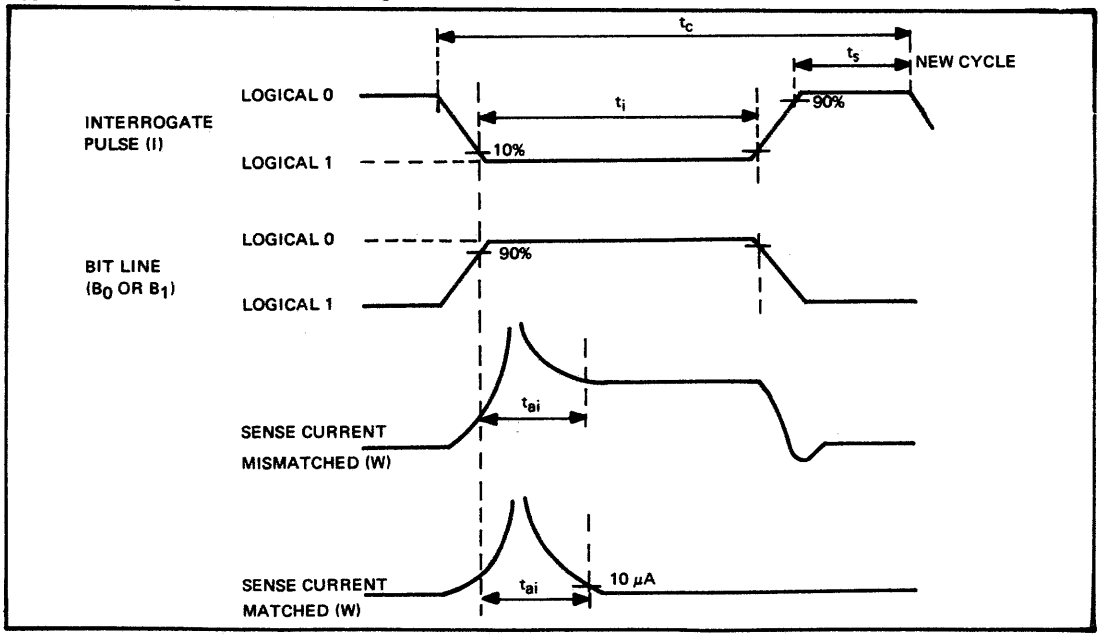
content-addressable memory operational requirements



typical switching waveforms (read and write)



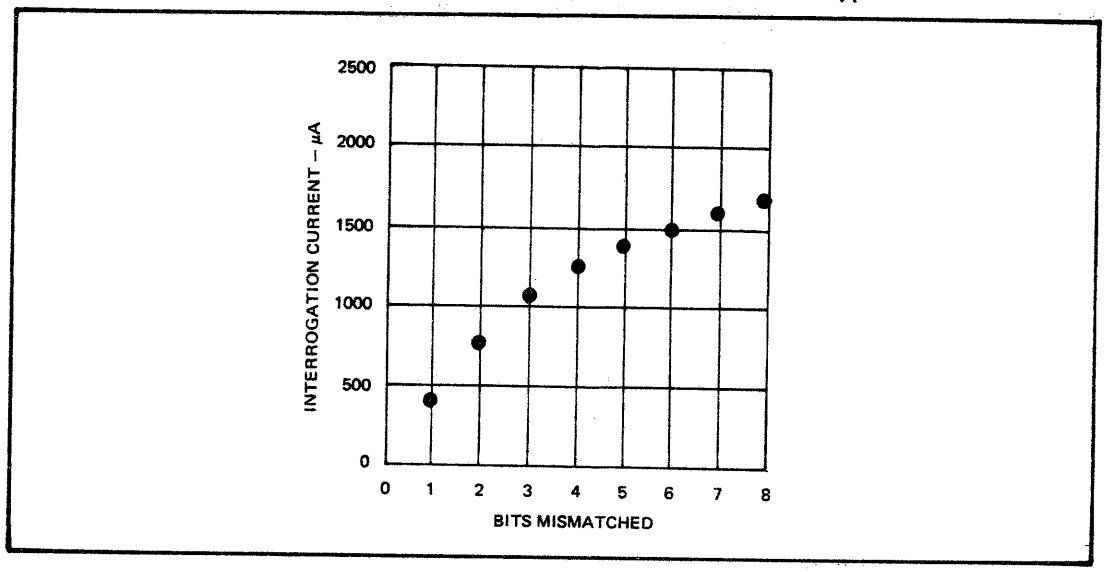
typical switching waveforms (interrogation)

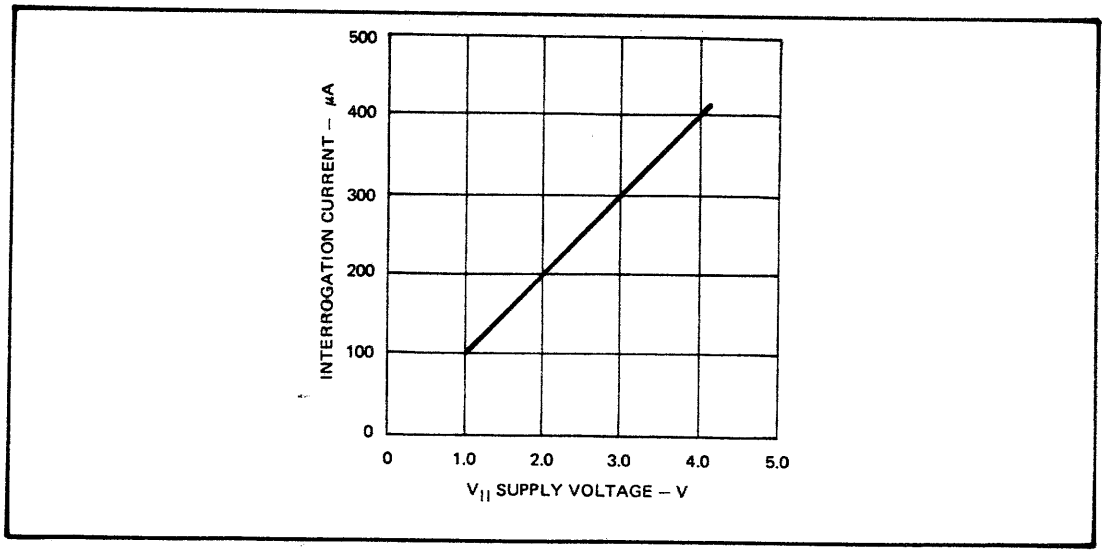


TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Interrogation Current vs Number of Bits Mismatched, And vs V_{II} Supply Voltage

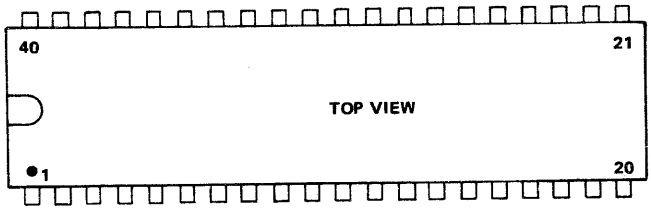
(R = 100 Ω, V_{DD} = −12 V, V_{GG} = −12 V, Logical 1 = −12 V, T_A = 25°C)





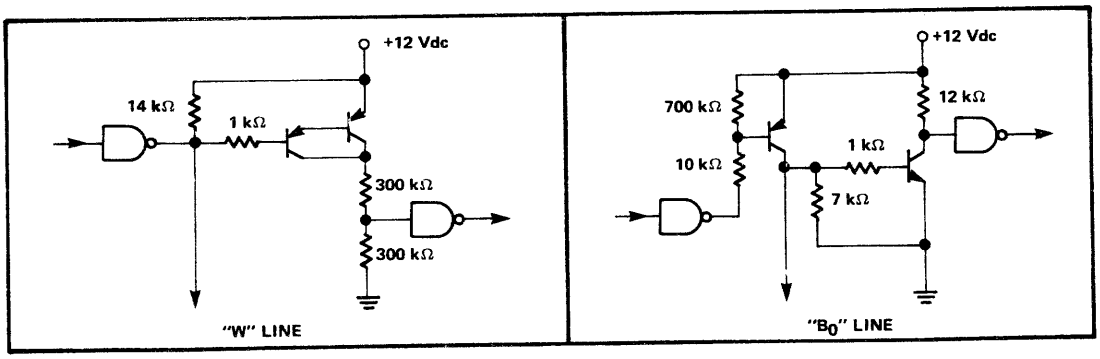
mechanical data and pin configuration

The device is available in both a 40-pin hermetically sealed ceramic dual-in-line package (TMS 4000 JC) and a 40-pin dual-in-line plastic package (TMS 4000 NC). The packages are designed for insertion in mounting-hole rows on 0.600-inch centers.



PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	0 } B_6	11	W_8	21	1 } B_3	31	W_9
2	1 }	12	W_6	22	0 }	32	W_{11}
3	0 } B_8	13	W_4	23	1 } B_1	33	W_{13}
4	1 }	14	W_2	24	0 }	34	W_{15}
5	I	15	V_{GG}	25	V_{DD}	35	NC
6	GND	16	NC	26	NC	36	V_{II}
7	W_{16}	17	1 } B_5	27	W_1	37	0 } B_2
8	W_{14}	18	0 }	28	W_3	38	1 }
9	W_{12}	19	1 } B	29	W_5	39	0 } B_4
10	W_{10}	20	0 }	30	W_7	40	1 }

typical read/write interface for one-microsecond operation



NOTE: All gates = SN7400

14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4003 JR, TMS 4003 NC
256-BIT RANDOM-ACCESS MEMORY

FEBRUARY, 1971

FOR MEMORY APPLICATIONS REQUIRING HIGH-SPEED READ/WRITE CAPABILITY

- **Nondestructive readout**
- **Static operation**
- **System access time under 200 ns**
- **Low power dissipation**

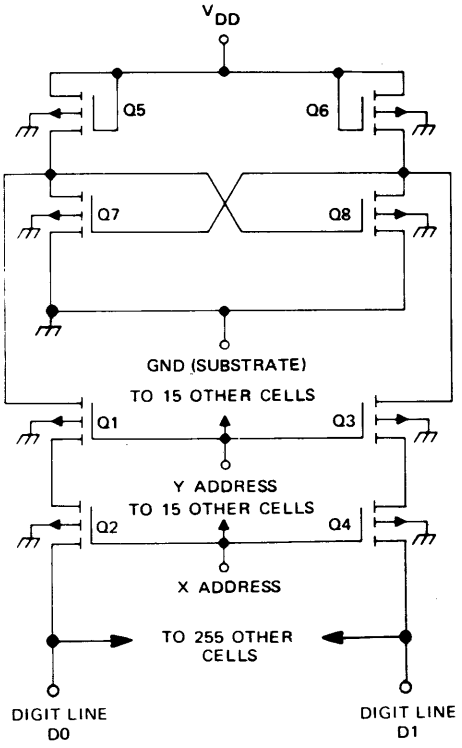
description

The TMS 4003 JR/NC is a high-speed random-access memory consisting of 256 cross-coupled flip-flops organized as 256 one-bit words. The entire device is constructed on a single monolithic chip using thick-oxide techniques to produce MOS P-channel enhancement-type transistors. Active-element design permits nondestructive readout, because addressing each bit tends to reinforce its existing state. Digit lines can be wire-OR connected to obtain memory planes greater than 256 words. External decoding circuitry can be used for additional planes to achieve desired word length. Selection of a given bit for reading or writing is accomplished by the coincident addressing of one of 16 X lines and one of 16 Y lines. These two lines are taken to V_{DD} while all other X and Y lines are held at ground.

Memory writing is accomplished by externally addressing the desired cell and bringing the appropriate digit line to ground while holding the other digit line at its nominal V_{DD} potential.

Reading an addressed cell requires sensing a differential current between the two digit lines. Both digit lines should be held near their nominal value of V_{DD}. This causes addressing transistors Q1, Q2, Q3, and Q4 to act as additional load resistors in parallel with standby load resistors Q5 and Q6, (see Figure 1). Depending on the flip-flop state, current will flow in one of the digit lines and not the other.

Maximum speed of the circuit is limited by the propagation delay of the Y address voltage through a series of P-diffused tunnels. The write or read cycle time, including this delay and the TTL address-decode delay, will be under 200 nanoseconds (see Figure 2).



CELL SCHEMATIC (1 OF 256 CELLS)

FIGURE 1

Power dissipation is typically 0.6 mW per bit when the memory is operated with an 18-volt dc power supply. Significantly lower average power dissipation may be obtained without sacrifice of system performance by synchronously or asynchronously pulsing the V_{DD} power supply. This feature is a result of the temporary data storage provided by the gate capacitance of transistors Q7 and Q8.

— continued

description (continued)

A unit mounted in a 40-pin hermetically sealed ceramic dual-in-line package is designated "TMS 4003 JR". Mounted in a 40-pin plastic dual-in-line package the device is numbered "TMS 4003 NC".

logic

Logic levels for this memory are defined in terms of standard NEGATIVE LOGIC where:

−16 V to −20 V = LOGICAL 1
+0.3 V to −2 V = LOGICAL 0

OPERATING MODE	ADDRESS LINES OF SELECTED CELL		DIGIT-LINE TERMINALS	
	X	Y	D1	D0
Read	1	1	1	1
Write a zero	1	1	1	0
Write a one	1	1	0	1

A selected cell has both its X and Y address lines at logical 1. During read and write operations, only one cell should be selected at a time. An unselected cell is a cell which has at least one of its address lines at logical 0.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage at any terminal relative to substrate (GND) . . . . . +0.3 V to −22 V
Operating free-air temperature range . . . . . −55°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNIT
Supply voltage V_{DD}	−16	−18	−20	V
Write access time, t_{aw} (See Note 1 and Figure 3)	80			ns
Write pulse width, t_{pw} (See Figure 3)	30			ns

NOTE: 1. Write access time is the delay between the application of address voltages at the X and Y inputs and the start of the write pulse. Premature application of the write pulse may cause undesired writing into cells other than the addressed cell.

operating characteristics (unless otherwise noted T_A = 25°C)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Read-mode sense current	$V_{Xn} = V_{Ym} = V_{in(D0)} = V_{in(D1)} = V_{DD} = -16$ V, Logical 0 stored in cell nm	D0	−200	−400		μA
		D1		−0.1	−10	
	$V_{Xn} = V_{Ym} = V_{in(D0)} = V_{in(D1)} = V_{DD} = -16$ V, Logical 1 stored in cell nm	D0		−0.1	−10	
		D1	−200	−400		
	$V_{Xn} = V_{Ym} = V_{in(D0)} = V_{in(D1)} = V_{DD} = -18$ V, Logical 0 stored in cell nm	D0	−300	−500		
		D1		−0.1	−10	
	$V_{Xn} = V_{Ym} = V_{in(D0)} = V_{in(D1)} = V_{DD} = -18$ V, Logical 1 stored in cell nm	D0		−0.1	−10	
		D1	−300	−500		
Address-line current (16 lines in parallel)	V_X or V_Y = −20 V, $V_{in(D0)} = V_{in(D1)} = V_{DD}$ = 0 V				−10	μA
Total power dissipation	One cell addressed, V_{DD} = −18 V			150	300	mW
	One cell addressed, V_{DD} = −20 V, T_A = −55°C				500	

14

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operating characteristics, continued (unless otherwise noted $V_{DD} = -18$ V, $T_A = 25°C$)

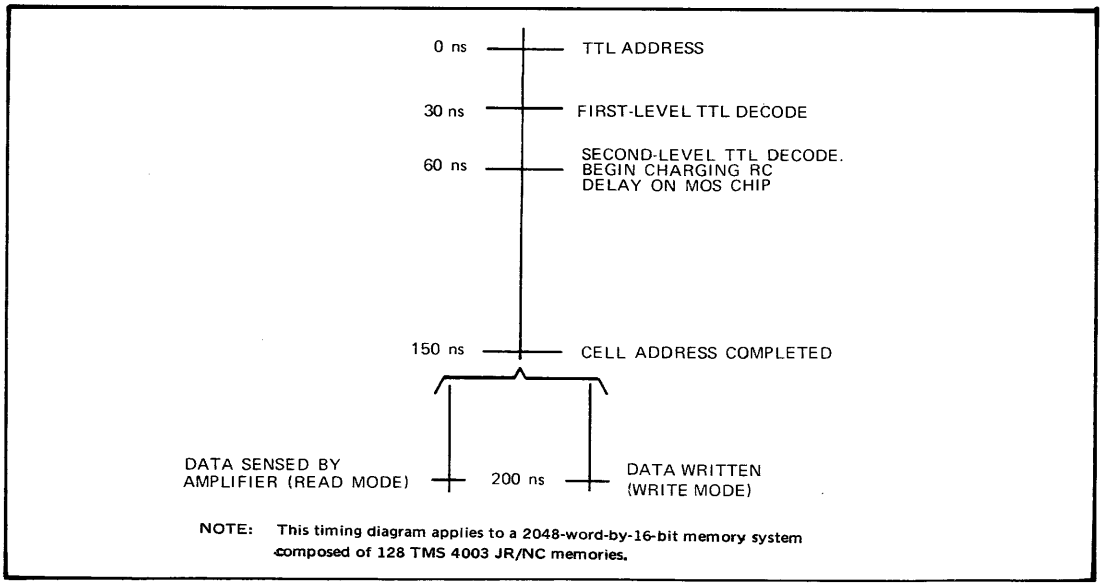
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Capacitance between digit-line terminal and substrate	$V_{in(D0)} = V_{in(D1)} = 0$ V, f = 140 kHz, $V_X = V_Y = 0$ V (or one cell addressed), See Note 2		50		pF
	$V_{in(D0)} = V_{in(D1)} = -18$ V, f = 140 kHz, $V_X = V_Y = 0$ V (or one cell addressed), See Note 2		30		
Capacitance between digit-line terminal and physically adjacent address terminal (D0-to-X2 or D1-to-Y1, see Note 3)	$V_{in(D0)} = V_{in(X2)} = 0$ to -18 V, $V_{in(D1)} = V_{in(Y1)} = 0$ to -18 V, f = 140 kHz, See Note 2		8†		pF
Capacitance between address terminal and substrate	$V_X = V_Y = 0$ to -18 V, f = 140 kHz, See Note 2		8†		pF
Capacitance between V_{DD} terminal and substrate	$V_{DD} = V_X = V_Y = 0$ to -18 V, f = 140 kHz, See Note 2		50†		pF
Read access time, t_{ar} (see Note 4)	See Figure 3, $R_L = 51\ \Omega$		30	60	ns

NOTES: **2. All capacitances are measured with all other elements ac grounded.**

3. Typical capacitance between digit-line terminals and all other address lines will be less than that shown for the adjacent address lines.

4. Read access time is the delay between the application of address voltages at the X and Y inputs and the availability of differential current between the digit lines.

†These typical values are the average for the voltage range 0 to −18 V.



NOTE: This timing diagram applies to a 2048-word-by-16-bit memory system composed of 128 TMS 4003 JR/NC memories.

FIGURE 2 – TYPICAL SYSTEM CYCLE TIME

14

PARAMETER MEASUREMENT INFORMATION

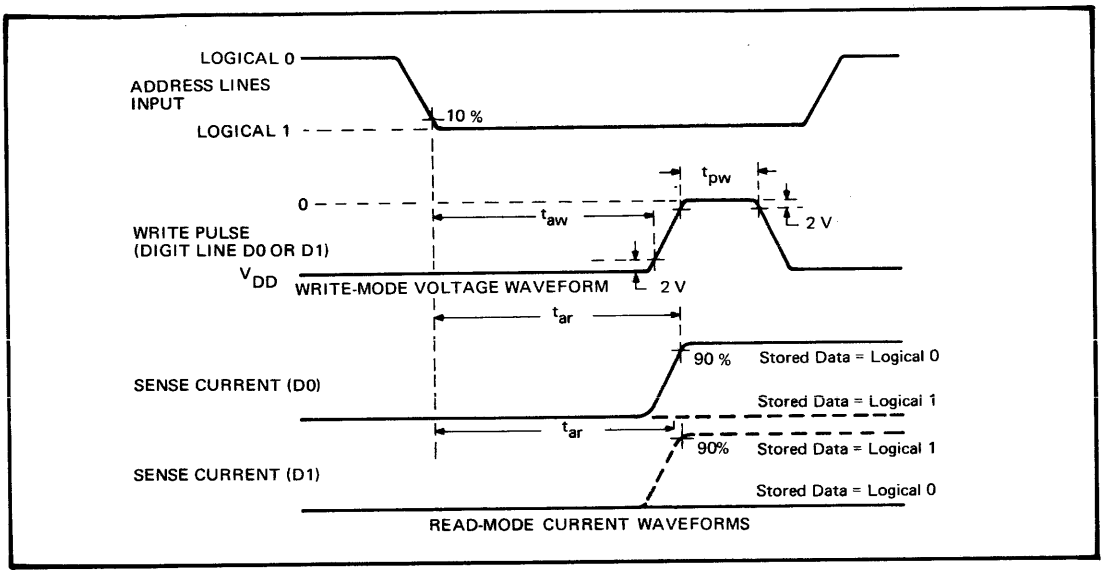


FIGURE 3 – TYPICAL SWITCHING WAVEFORMS

TYPICAL CHARACTERISTICS

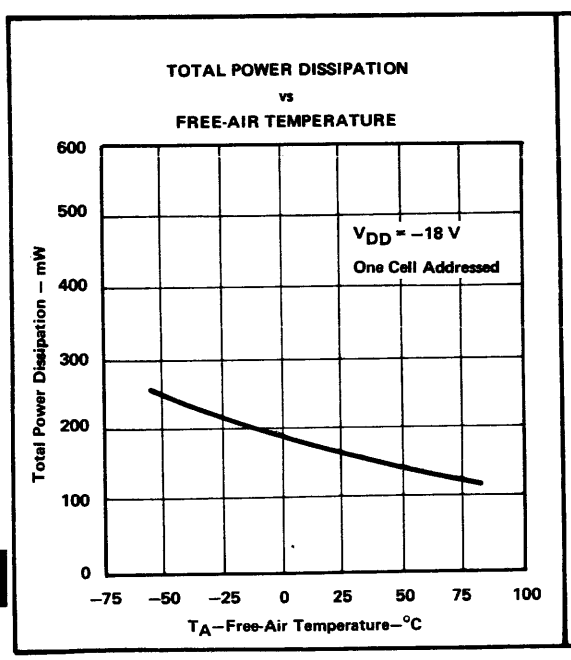


FIGURE 4

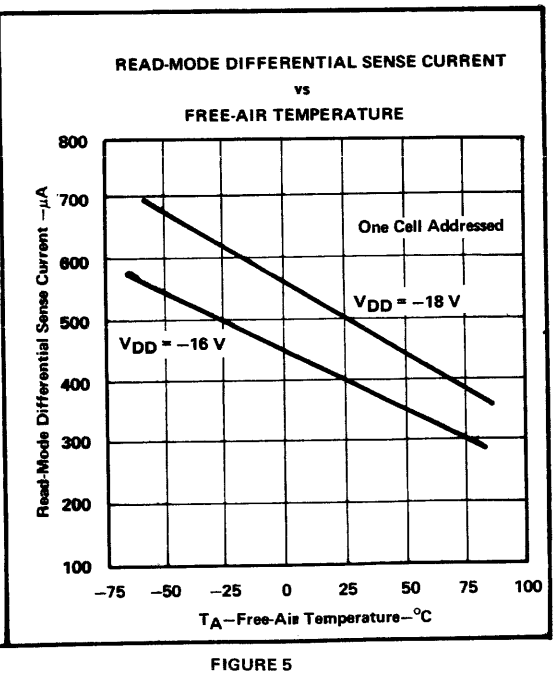
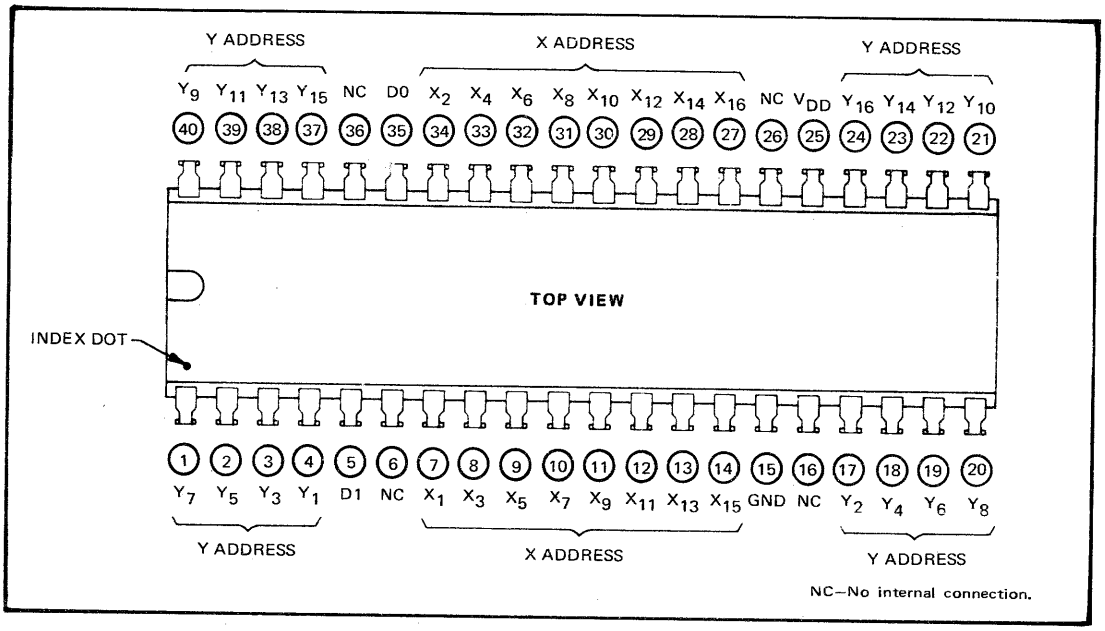


FIGURE 5

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

mechanical data and pin configuration

The device is available in both a 40-pin hermetically sealed ceramic dual-in-line package (TMS 4003 JR) and a 40-pin plastic dual-in-line package (TMS 4003 NC). These packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)



TYPICAL APPLICATION DATA

An actual negative supply for V_{DD} is not necessary. The V_{DD} terminal can be returned to system ground with a positive potential equal in magnitude to the voltage specified for V_{DD} applied to device ground (pin 15). This simplifies external circuitry, particularly when using bipolar systems such as TTL. The MOS device ground V_{SS}, is nominally +18 V while the V_{DD} terminal is at system ground. Addressing occurs when one X-address line and one Y-address line are pulled to ground. Unselected address lines should remain at V_{SS}.

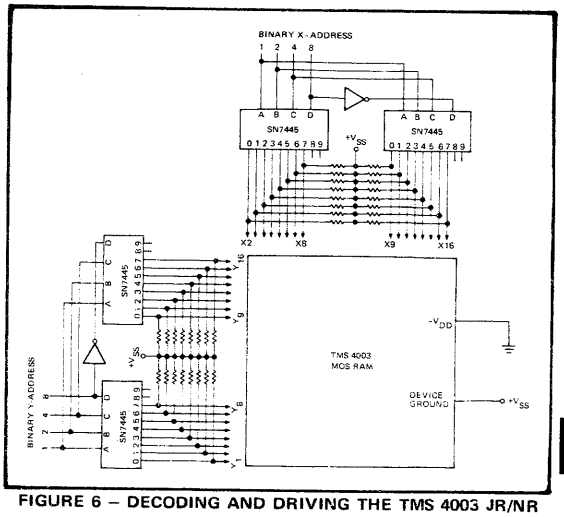
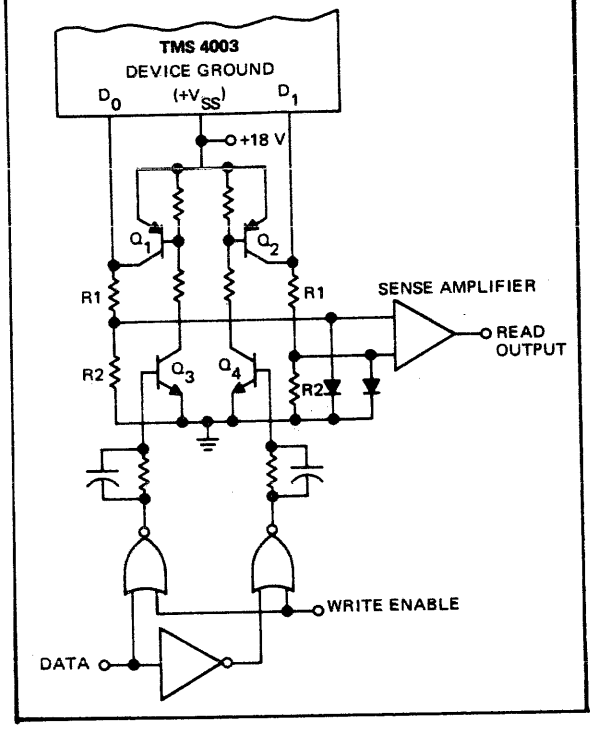


FIGURE 6 – DECODING AND DRIVING THE TMS 4003 JR/NR BY USE OF THE SN74154

14

TYPICAL APPLICATION DATA (Continued)

TMS 4003 JR/NC MEMORIES WITH PARALLEL CONNECTED DIGIT LINES

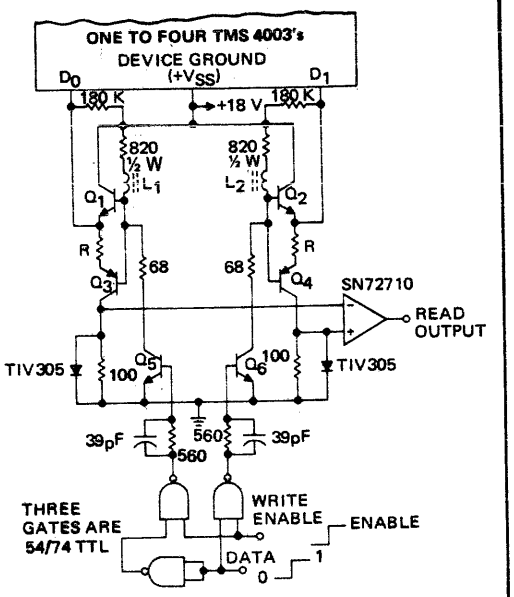


CIRCUIT COMPONENTS INFORMATION

Q1 and Q2: 2N3629
Q3 and Q4: 2N3014

FIGURE 7 – BASIC READ/WRITE CIRCUIT LIMITED TO LOW-SPEED OPERATION

TMS 4003 JR/NC MEMORIES WITH PARALLEL CONNECTED DIGIT LINES



CIRCUIT COMPONENTS INFORMATION

L1 and L2: 2 1/2 T, No. 30 wire on Ferrite Bead (Allen-Bradley No. T0 135G144A or equivalent)
Q1, Q2, Q5, and Q6: 2N3014
Q3 and Q4: 2N3829

$$\text{R1 and R2: } \frac{180\ \Omega}{\text{No. of TMS 4003 JR memories}}$$

FIGURE 8 – HIGH-SPEED READ/WRITE CIRCUIT

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4020 NC
2048-BIT DYNAMIC RANDOM-ACCESS MEMORY

FEBRUARY 1971

features

- Low power dissipation
- Full decode
- Access time – 320 nsec max
- Cycle time – 640 nsec max
- High output-current capability (2 mA typ)
- Low-threshold technology
- 24-pin plastic package

description

The TMS 4020 NC is a 1024-word by 2-bit random-access memory, constructed on a single chip, with MOS P-channel enhancement-mode transistors. The device has two 1024-bit storage arrays with a 10-bit address decode common to both. There are four input chip selects – two for each array.

The address decode as well as the memory arrays are implemented with dynamic circuitry, thus enabling low power dissipation. Data stored in memory is nondestructively read. Refreshing of stored data is required every two milliseconds and refreshing the entire 2048 bits is accomplished with 16 Read cycles.

The outputs of the device are open ended, allowing several circuits to be wired-OR. The information read from the array is opposite in polarity to the write input.

The TMS 4020 NC is fabricated with a thick-oxide, low-threshold, self-aligned gate process.

logic definition

Positive logic is assumed.

a) LOGICAL 1 = most positive voltage

b) LOGICAL 0 = most negative voltage

operation

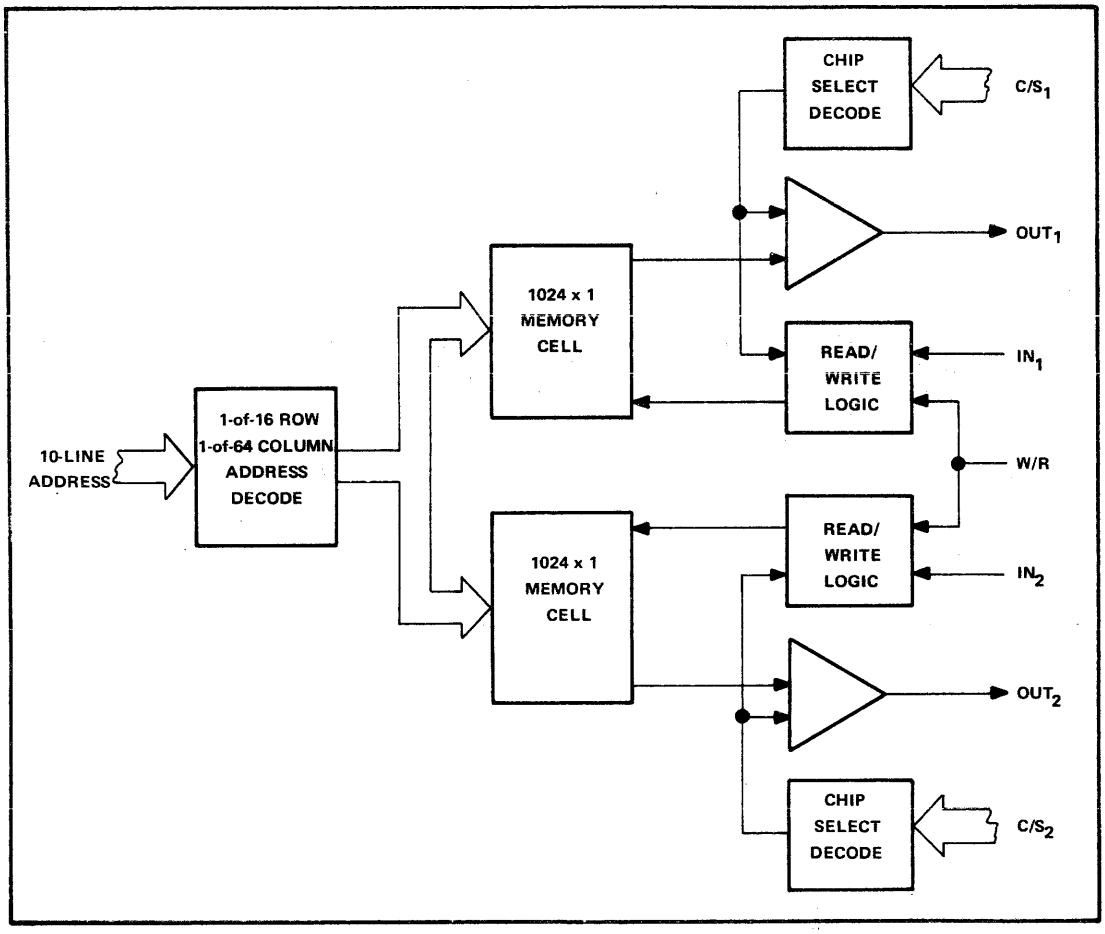
The Precharge Cycle ϕ_1 is used to set up the dynamic decode logic for address selection, which occurs during Generate Time ϕ_2.

During the Generate Time ϕ_2 the address decode is propagated and the memory arrays are precharged. With the return of ϕ_2 to the most positive voltage, the propagation of selected X-rows (1 of 16) of both arrays is initiated. The information in the two bits selected by the Y decode is then available at the output in 100 nsec.

If a Read cycle is required, the data can be sampled at this time. An additional 100 nsec is required in the cycle to assure the completion of the refresh cycle. If a Write cycle is required, the Write strobe should be initiated 130 nsec after the termination of the Generate ϕ_2 signal concurrent with the new information being written. The remaining positions in the X-row (not being written into) will complete the refresh cycle.

All X-rows not read during a 2-msec period should be refreshed via Read cycle to assure the integrity of the data.

functional block diagram and pin configuration



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} and V_{SS} range (See Note 1)	−24 V to 0.3 V
Clock input voltage range (See Note 1)	−24 V to 0.3 V
Data input voltage range (See Note 1)	−24 V to 0.3 V
Operating free-air temperature range	−25°C to 70°C
Storage temperature range	−25°C to 150°C

NOTE 1: These voltage values are with respect to V_{SUB} (substrate).

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions (see note 2)

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate Voltage V_{SUB}	1.5	2.0	2.5	V
Drain supply V_{DD}	−17	−16	−15	V
Logic Levels				
Input HIGH level V_{IH}	−1.5	0	+0.3	V
Input LOW level V_{IL}	−17	−16	−15	V
Clock Voltage Levels				
Clock HIGH level $V_{\phi H}$	−1.0	0	+0.3	V
Clock LOW level $V_{\phi L}$	−17	−16	−15	V
Pulse Timing				
Pulse transition t_r, t_ϕ			1000	ns
Clock pulse width of ϕ_1 PW_1	90			ns
Clock pulse width ϕ_2 PW_2	170			ns
Clock delay from ϕ_1 to ϕ_2 P_{d1}	0			ns
Clock delay from ϕ_2 to ϕ_1 P_{d2} (Read and Refresh)	200			ns
Clock delay from ϕ_2 to ϕ_1 P_{d2} (Write)	310			ns
Address set-up time P_{AS}	0			ns
Address hold time P_{AH}	0			ns
ϕ_2-to-write pulse delay time P_{dW}	130			ns
Write pulse width P_{WW}	150			ns
Pulse Spacing				
Data set-up time P_{DS}	10			ns
Data hold time P_{DH}	10			ns
Chip select set-up time P_{CS}	0			ns
Chip select hold time P_{CH}	0			ns
Cycle time (Read and Refresh)	530			ns
Cycle time (Write)	640			ns
Strobe data width P_0	100			ns
Refreshing Time P_{REF}			2	ms

NOTE 2: These voltage values are with respect to V_{SS}.

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

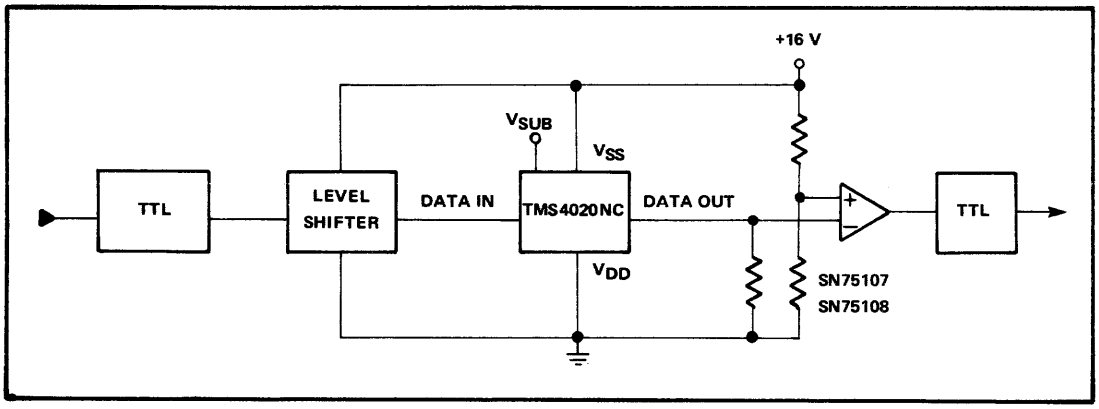
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output High Current $I_{OS(H)}$ Sense	Load = 100 Ω	1.2	2.0		mA
Output Leakage Current $I_{L(out)}$	V_{OUT} = −16 V			1	μA
Input (Load) Current $I_{L(in)}$	V_{IN} = −16 V			1	μA
Substrate Leakage Current I_{SUB}	V_{SUB} = +2 V			100	μA
Supply Current I_{DD}					
During PW_1			15	20	mA
During PW_2			26	34	mA
During P_{d2}			1.5	2	mA
Average Supply Current $I_{DD(AV)}$			13	18	mA

14

dynamic electrical characteristics (under nominal operating conditions from 0°C to +70°C unless otherwise noted)

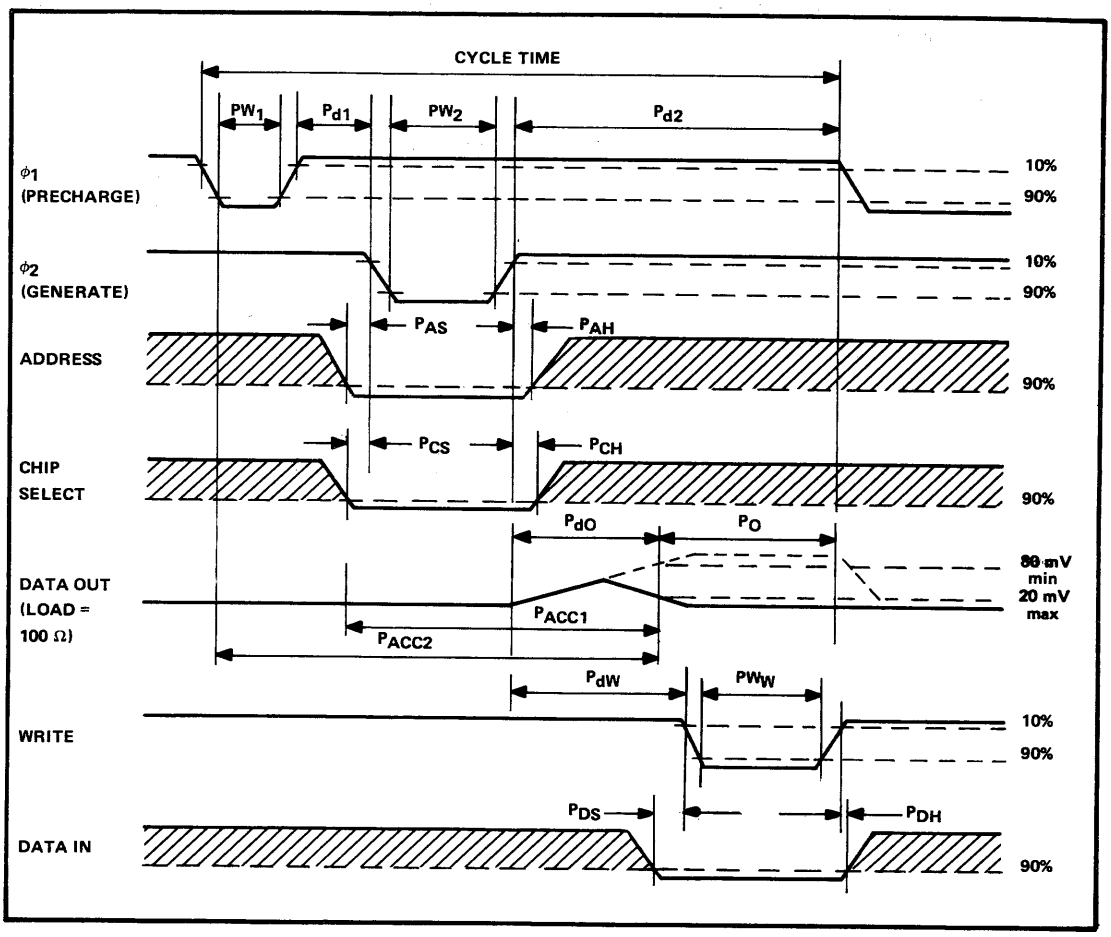
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
End of ϕ_2 to output delay P_{d0}	LOAD = 100 Ω		70	100	ns
Address to output access time P_{ACC1}	$I_{OS(HIGH)}$ = 0.8 mA min		290	320	ns
ϕ_1 to output access time P_{ACC2}	$I_{OS(LOW)}$ = 0.2 mA min		410	440	ns
Address Capacitance					
A_0 through A_3			8	11	pF
A_4 through A_8	F = 1 MHz at 25°C,		6	8	pF
A_9	$V_{AF} = V_{SS}$		4	6	pF
Clock Capacitance					
ϕ_1	F = 1 MHz,		18	22	pF
ϕ_2	$V_\phi = V_{SS}$ at 25°C		30	38	pF
Read/Write Capacitance					
Chips selected	F = 1 MHz,		27	33	pF
Chips not selected	$V_{R/W} = V_{SS}$ at 25°C		15	20	pF
Data Input Capacitance					
Chips selected	F = 1 MHz,		20	25	pF
Chips not selected	$V_{in} = V_{SS}$ at 25°C		5	7	pF
Data Output Capacitance					
Chips selected	F = 1 MHz,		8	12	pF
Chips not selected	$V_{out} = V_{SS}$ at 25°C		3	5	pF

TTL interface



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

timing diagram and voltage waveforms



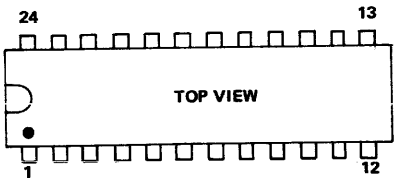
14

TMS 4020 NC
2048-BIT DYNAMIC RANDOM-ACCESS MEMORY

mechanical data

The TMS 4020 NC is mounted in a 24-pin plastic dual-in-line package, designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

pin configuration



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	A_6	13	A_1
2	A_5	14	A_0
3	A_4	15	ϕ_2
4	$\overline{IN_1}$	16	C/S_2
5	OUT_1	17	C/S_2
6	C/S_1	18	R/W
7	C/S_1	19	OUT_2
8	ϕ_1	20	$\overline{IN_2}$
9	A_3	21	A_9
10	A_2	22	A_8
11	V_{SUB}	23	A_7
12	V_{DD}	24	V_{SS}

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4023 NC
1024-BIT RANDOM-ACCESS MEMORY

FEBRUARY 1971

features

- Low power dissipation
- Access time – 650 nsec (maximum)
- Cycle time – 900 ns (maximum
- Refresh Period – 2 ms for 0°C–70°C
- Fully decoded
- Wired-OR capability
- Inputs fully protected
- 24-lead plastic package

description

The TMS 4023 NC is a 1024-bit RAM, organized as 1024 one-bit words, using P-channel enhancement-mode transistors. A fully decoded monolithic array, the device is available in a low-cost, standard, 24-pin dual-in-line plastic package. The dynamic memory has nondestructive readout and refreshes all 1024 bits in 32 read cycles (or 32 microseconds). The TMS 4023 NC is designed as a low-cost main-frame memory for large-storage high-performance operations.

logic definition

Negative logic is assumed.

a) LOGICAL 1 = most negative voltage

b) LOGICAL 0 = most positive voltage

operation (refer to functional block diagram and timing diagram)

A 10-bit address code selects any one of the 1024 bits for either Read or Write operation. A Read or Write operation may be performed with the application of a logic 1 on the chip-enable line. The memory is inhibited with the application of a logic 0 to the chip-select line. This renders the data Input/Output line open and ineffective, which allows wired-OR operation. The address decode is not inhibited however.

Application of a logic 0 to the Read/Write line will result in a Read operation. This may be presented simultaneously with or before application of the address code. Read-out is nondestructive.

A logic 1 applied to the Read/Write and chip enable will result in a Write operation. Duration of the Write command must be at least 560 nanoseconds to ensure that the data is written into memory.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

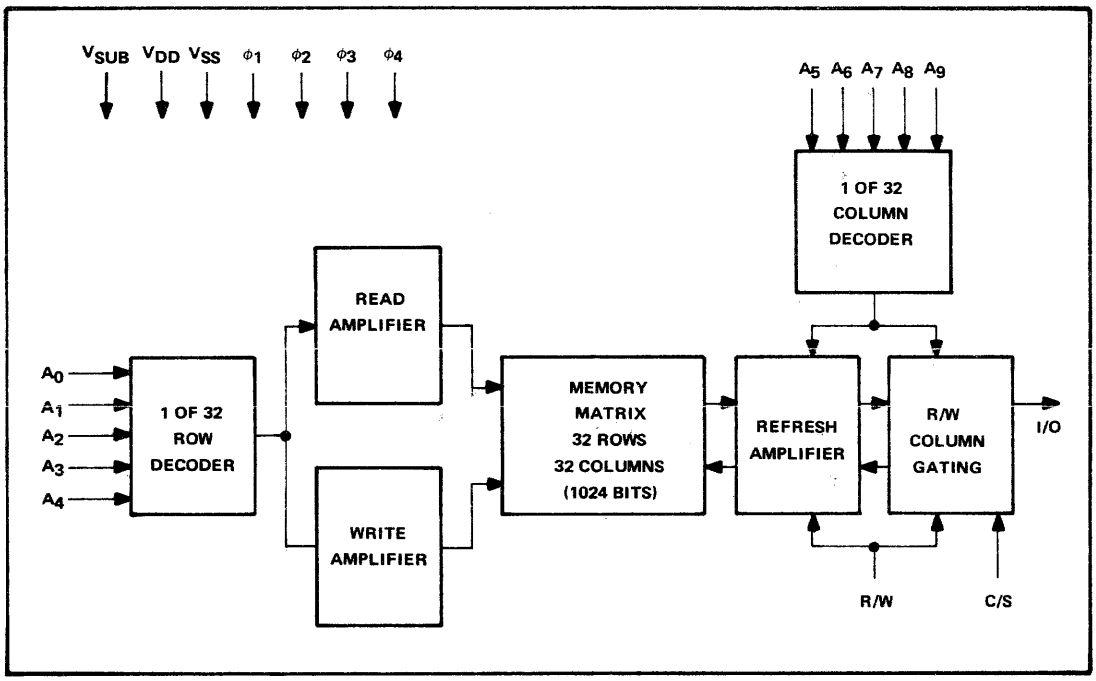
Supply voltages V_{DD} and V_{SS} range (See Note 1)	−24 V to 0.3 V
Clock input voltage range (See Note 1)	−24 V to 0.3 V
Data input voltage range (See Note 1)	−24 V to 0.3 V
Operating free-air temperature range	−25°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SUB} (substrate).

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram and pin configuration



recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage (See Note 1)				
Substrate Supply V_{SUB}	+1.5	+2.0	+2.5	V
V_{SS}		0		V
V_{DD}	−19	−20	−21	V
Logic Levels (See Note 1)				
Input HIGH level V_{IH}	−1.5		+0.3	V
Input LOW level V_{IL}	−19	−20	−21	V
Clock Voltage Levels (See Note 1)				
Clock HIGH level $V_{\phi H}$	−1.5		+0.3	V
Clock LOW level $V_{\phi L}$	−19	−20	−21	V
Pulse Timing				
Pulse widths				
Clock pulse width 1 $PW_{\phi 1}$	120			ns
Clock pulse width 2 $PW_{\phi 2}$	130			ns
Clock pulse width 3 $PW_{\phi 3}$	380			ns
Clock pulse width 4 $PW_{\phi 4}$	110			ns
Pulse Spacing				
Clock delay $t_{d\phi 1}$, $t_{d\phi 2}$, $t_{d\phi 3}$, $t_{d\phi 4}$	0			ns

NOTE 1: These voltage values are with respect to V_{SS}.

— continued

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions (continued)

PARAMETER	MIN	NOM	MAX	UNITS
Pulse Spacing (continued)				
Address setup t_{AS}	10			ns
Address hold t_{AH}	10			ns
Chip-select setup time t_{CS}	0			ns
Chip-select hold time t_{CH}	0			ns
R/W overlap C/S t_{WS} and t_{WH}	10			ns
Data setup t_{DS}	10			ns
Data hold t_{DH}	10			ns
Refreshing time T_{REF}			2	ms

static electrical characteristics (under recommended operating conditions and for T_A = 0°C to 70°C)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Leakage Current					
Substrate				100	μA
Address Input				1	μA
Clock Input				1	μA
C/S Chip Select				1	μA
R/W Read/Write				1	μA
I/O Input/Output				1	μA
Output High Current					
I_{OS} Sense	R_{LOAD} = 200 Ω	1.1			mA
Supply Current Drain					
I_{DD} Drain Supply			1.0		mA

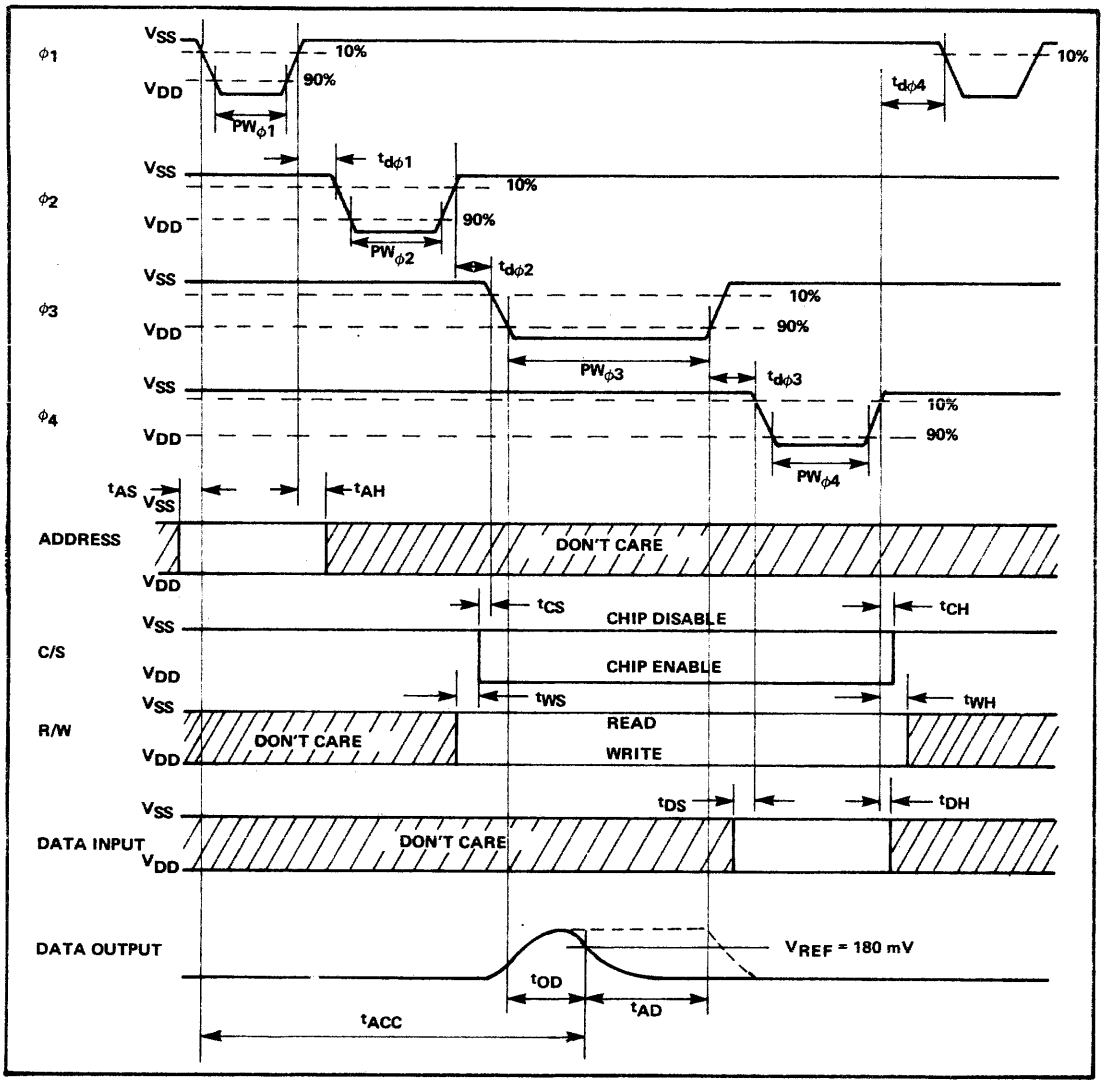
dynamic electrical characteristics (under recommended operating conditions and for T_A = 0°C to 70°C)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Cycle Time	C_{LOAD} = 100 pF, R_{LOAD} = 200 Ω, V_{REF} = 180 mV	900			ns
t_{OD} Output Delay				350	ns
t_{ACC} Access time (Note 2)	C_{LOAD} = 100 pF, R_{LOAD} = 200 Ω, V_{REF} = 180 mV		650		ns
t_{AD} Available data on output		50			ns
Capacitance					
C_{IN} Address Input			5	8	pF
$C_{\phi1}$, $C_{\phi2}$, $C_{\phi3}$, $C_{\phi4}$ Clock			17	20	pF
C/S Chip Select			9	11	pF
R/W Read/Write			8	10	pF
I/O Input/Output					
Chip Selected			24	27	pF
Chip Not Selected			7	9	pF

NOTE 2: Access time is given for rise and fall times of input signals of no more than 15 ns.

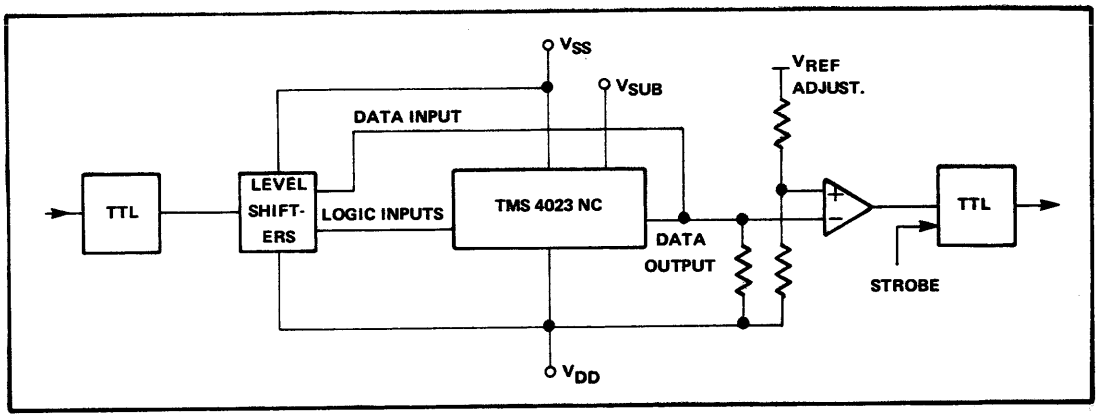
14

timing diagram and voltage waveforms



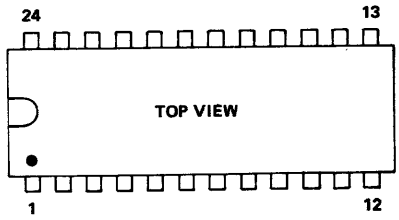
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TTL interface



mechanical data and pin configuration

The TMS 4023 NC is mounted in a 24-pin dual-in-line plastic package, designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	–	13	–
2	A_9	14	I/O
3	A_8	15	C/S
4	A_7	16	R/W
5	V_{SS}	17	A_1
6	A_6	18	A_0
7	A_5	19	ϕ_3
8	A_4	20	V_{DD}
9	A_3	21	ϕ_4
10	A_2	22	ϕ_1
11	–	23	ϕ_2
12	–	24	V_{SUB}

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4025 NC
2048-BIT DYNAMIC RANDOM-ACCESS MEMORY

features

- Low power dissipation
- Full decode
- Access time – 280 nsec max
- Cycle time – 640 nsec max
- High output-current capability (2 mA typ)
- Low-threshold technology
- 24-pin plastic package

description

The TMS 4025 NC is a 1024-word by 2-bit random-access memory, constructed on a single chip, with MOS P-channel enhancement-mode transistors. The device has two 1024-bit storage arrays with a 10-bit address decode common to both. There are two input chip selects – one for each array.

The address decode as well as the memory arrays are implemented with dynamic circuitry, thus enabling low power dissipation. Data stored in memory is nondestructively read. Refreshing of stored data is required every two milliseconds and refreshing the entire 2048 bits is accomplished with 16 Read cycles.

The outputs of the device are open ended, allowing several circuits to be wired-OR. The information read from the array is opposite in polarity to the write input.

The TMS 4025 NC is fabricated with a thick-oxide, low-threshold, self-aligned gate process.

logic definition

Positive logic is assumed.

a) LOGICAL 1 = most positive voltage

b) LOGICAL 0 = most negative voltage

operation

The Precharge Cycle ϕ_1 is used to set up the dynamic decode logic for address selection, which occurs during Generate Time ϕ_2.

During the Generate Time ϕ_2 the address decode is propagated and the memory arrays are precharged. With the return of ϕ_2 to the most positive voltage, the propagation of selected X-rows (1 of 16) of both arrays is initiated. During the Read/Write time ϕ_3 the information in the two bits selected by the Y decode is then available at the output in 60 nsec.

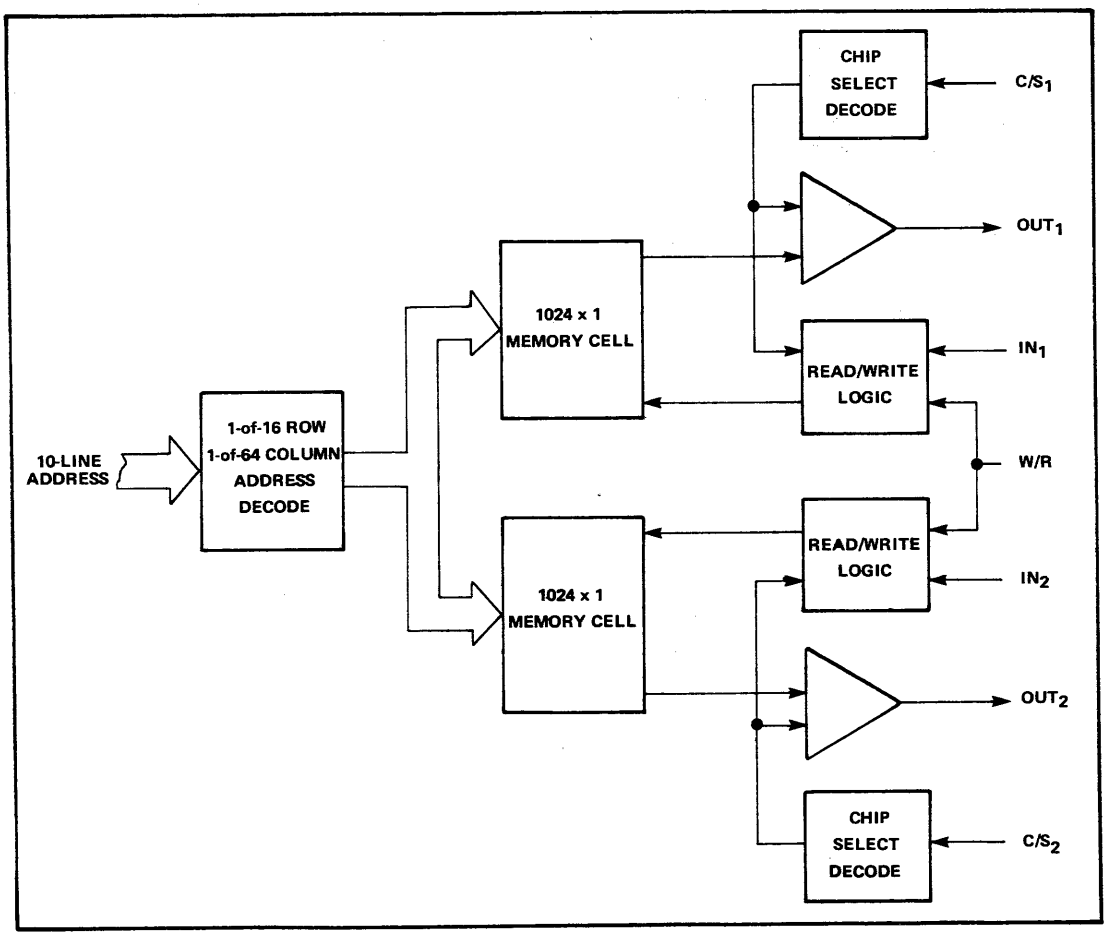
If a Read cycle is required, the data can be sampled at this time. An additional 180 nsec is required in the cycle to assure the completion of the refresh cycle. If a Write cycle is required, the Write strobe should be initiated 90 nsec after the ϕ_3 signal concurrent with the new information being written. The remaining positions in the X-row (not being written into) will complete the refresh cycle.

All X-rows not read during a 2-msec period should be refreshed via Read cycle to assure the integrity of the data.

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram and pin configuration



14

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} and V_{SS} range (See Note 1)	−24 V to 0.3 V
Clock input voltage range (See Note 1)	−24 V to 0.3 V
Data input voltage range (See Note 1)	−24 V to 0.3 V
Operating free-air temperature range	−25°C to 70°C
Storage temperature range	−25°C to 150°C

NOTE 1: These voltage values are with respect to V_{SUB} (Substrate).

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions (see note 2)

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate Voltage V_{SUB}	1.5	2.0	2.5	V
Drain supply V_{DD}	−17	−16	−15	V
Logic Levels				
Input HIGH level V_{IH}	−1.5	0	+0.3	V
Input LOW level V_{IL}	−17	−16	−15	V
Clock Voltage Levels				
Clock HIGH level $V_{\phi H}$	−1.0	0	+0.3	V
Clock LOW level $V_{\phi L}$	−17	−16	−15	V
Pulse Timing				
Pulse transition t_r, t_ϕ			1000	ns
Clock pulse width of ϕ_1 PW_1	90			ns
Clock pulse width of ϕ_2 PW_2	170			ns
Clock pulse width of ϕ_3 PW_3				
(READ and REF)	220			ns
(WRITE)	280			ns
Clock delay from ϕ_1 to ϕ_2 P_{d1}	0			ns
Clock delay from ϕ_2 to ϕ_3 P_{d2}	0			ns
Clock delay from ϕ_3 to ϕ_1 P_{d3}	0			ns
Address set-up time P_{AS}	0			ns
Address hold time P_{AH}	0			ns
ϕ_3-to-write pulse delay time P_{dW}	90			ns
Write pulse width P_{WW}	150			ns
Pulse Spacing				
Data set-up time P_{DS}	10			ns
Data hold time P_{DH}	10			ns
Chip select set-up time P_{CS}	0			ns
Chip select hold time P_{CH}	0			ns
Cycle time (Read and Refresh)	580			ns
Cycle time (Write)	640			ns
Strobe data width P_0	150			ns
Refreshing Time P_{REF}			2	msec

NOTE 2: These voltage values are with respect to V_{SS}.

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

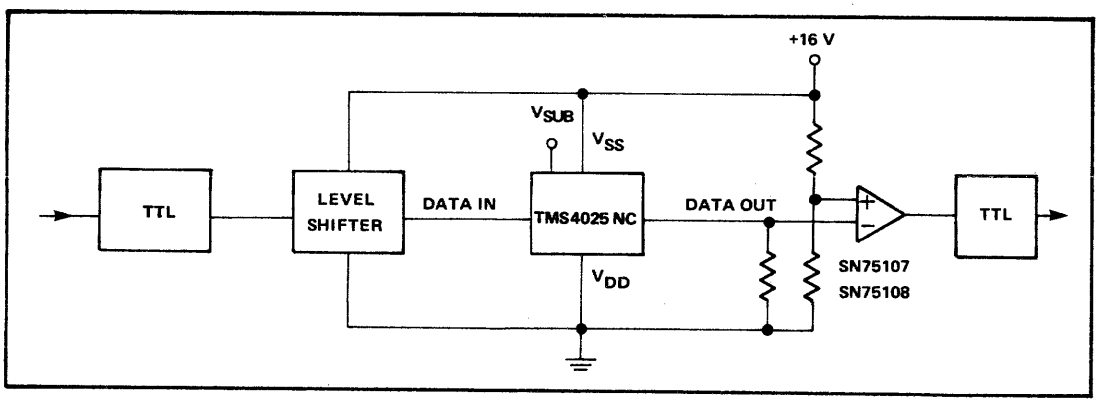
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output High Current Sense $I_{OS(H)}$	Load = 100 Ω	1.2	2.0		mA
Output Leakage Current $I_{L(OUT)}$	V_{OUT} = −16 V			1	μA
Input (Load) Current $I_{L(IN)}$	V_{IN} = −16 V			1	μA
Substrate Leakage Current I_{SUB}	V_{SUB} = +2 V			100	μA
Supply Current I_{DD}					
during PW_1			3	5	mA
during PW_2			6	9	mA
during PW_3			2.5	4	mA
Average Supply Current $I_{DD(AV)}$			3.5	6	mA

14

dynamic electrical characteristics (under nominal operating conditions from 0°C to 70°C unless otherwise noted)

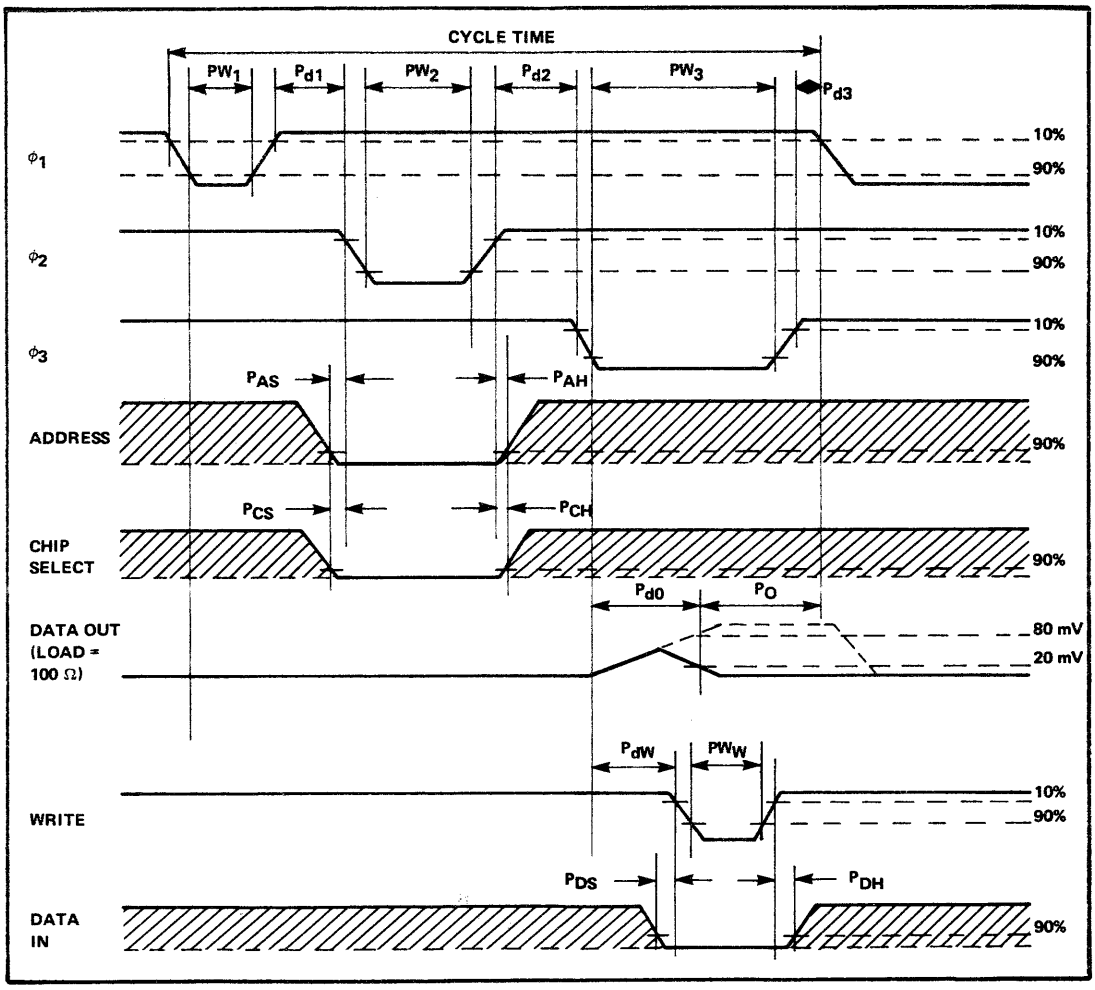
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
End of ϕ_2 to output delay P_{d0}	Load = 100 Ω		45	60	ns
Address-to-output access time P_{ACC1}	$I_{OS(HIGH)}$ = 0.8 mA min,		265	280	ns
ϕ_1-to-output access time P_{ACC2}	$I_{OS(LOW)}$ = 0.2 mA min		385	400	ns
Address Capacitance					
A_0 through A_3	F = 1 MHz at 25°C,		8	11	pF
A_4 through A_8	$V_A = V_{SS}$		6	8	pF
A_9			4	6	pF
Clock capacitance ϕ_1			18	22	pF
Clock capacitance ϕ_2	F = 1 MHz, $V_\phi = V_{SS}$ at 25°C		30	38	pF
Clock capacitance ϕ_3			35	42	pF
Read/Write Capacitance					
Chips selected	F = 1 MHz,		27	33	pF
Chips not selected	$V_{R/W} = V_{SS}$ at 25°C		15	20	pF
Data Input Capacitance					
Chips selected	F = 1 MHz,		20	25	pF
Chips not selected	$V_{in} = V_{SS}$ at 25°C		5	7	pF
Data Output Capacitance					
Chips selected	F = 1 MHz,		8	12	pF
Chips not selected	$V_{out} = V_{SS}$ at 25°C		3	5	pF

TTL interface



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

timing diagram and voltage waveforms

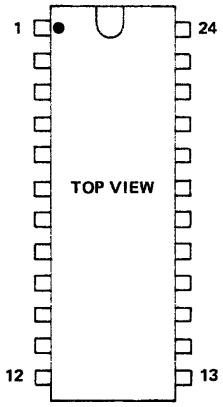


mechanical data

The TMS 4025 NC is mounted in a 24-pin plastic dual-in-line package, designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

— continued

mechanical data (continued)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	A_6	13	A_1
2	A_5	14	A_0
3	A_4	15	ϕ_2
4	$\overline{IN_1}$	16	NC
5	ϕ_3	17	C/S_2
6	OUT_1	18	R/W
7	C/S_1	19	OUT_2
8	ϕ_1	20	$\overline{IN_2}$
9	A_3	21	A_9
10	A_2	22	A_8
11	V_{SUB}	23	A_7
12	V_{DD}	24	V_{SS}

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

This section presents special-purpose devices produced by TI.

1) Analog Switches

The MOS transistor takes its place among the many techniques available to the designer for analog switching, which include:

- Mechanical choppers
- Bipolar transistors
- FETs
- Photoelectrical devices

It has several definite advantages over other techniques:

a) If there is no activating signal, the resistance between drain and source is extremely large and all inputs are insulated.

b) The MOS transistor is completely symmetrical with respect to its source and drain (the more positive terminal is called the source). Depending on the voltage applied, either side of the transistor can act as source or drain.

c) The gate of the transistor is completely insulated and does not draw current.

TI presently manufactures the following devices.

TMS 6000 JC/NC	10-channel common-source analog switch
TMS 6002 JC/NC	6-channel common-drain analog switch
TMS 6005 JC/NC	6-channel common-source analog switch
TMS 6009 JC/NC	6-channel common-source analog switch

2) Digital-Storage Buffers

The TMS 4006 JC is a first-in first-out store, particularly useful in communication applications. It allows the user to buffer digital information coming from a transmission line.

TMS 4006 JC, TMS 4006 NC
DIGITAL STORAGE BUFFER

features

- **Asynchronous input and output clocks**
- **Serial or parallel input capability**
- **No minimum clock rate (long-term storage)**
- **Low output impedance**
- **Double-ended buffer**
- **28-pin CDIP or dual-in-line plastic package**
- **Memory expansion by cascading units**

description

The TMS 4006 JC/NC is a data storage register with a capacity of 11 or 13 words of 6 bits each. It performs storage on a first-in first-out basis. The device employs a method of storage commonly referred to as "silo" mode.

Input and output of the digital storage buffer operate entirely independently. A word is transferred into the TMS 4006 JC/NC on the positive-going edge of the data input clock (DIC). A word is transferred out of the register on the positive going edge of the data output clock (DOC).

The input and output clocks are completely independent of each other. There is no minimum clock rate. Logic used in the TMS 4006 JC/NC is purely static and the device has long-term retention.

Once a character is entered it will be stored temporarily in the first available register. A control logic associated with the next register will indicate whether or not that register already contains a valid word. If the next register is full, the input word will stay in the first register. If the next register is empty the word will fall down in parallel and be transferred. This operation will be repeated time after time until a full register is met. The operation is completely independent of the input, output clocks, and of all terminals.

The input word can be loaded either in serial or in parallel.

To load the device in parallel, the serial parallel (S/P) control must be at a logic 1.

To load in serial, the S/P control must be at a logical 0. A marker bit will be loaded concurrently with the first shift pulse (data input clock). This marker bit will be a logical 0. In serial mode the input word will then be 7 bits (1 marker bit and 6 data bits). Parallel inputs should be held at less than −10 volts or left floating. In parallel operation, the serial input should be held greater than −1.5 volts or left floating.

The TMS 4006 JC/NC can store 11 words when operating in the serial mode and 13 words when operating in the parallel mode.

When in serial mode a word cannot be "all zero"; at least one of the data bits must be a 1.

Several outputs will allow the user to find out how much data is stored in the TMS 4006 JC/NC:

A Flag 1 output will indicate whether the first (first-in word) register is full.

A Flag 10 output will indicate whether the 10th register is full.

A Flag 13 output will indicate whether the 13th register is full.

Flag outputs may be used to generate a readout command when a certain number of registers are full.

An ADIS (any data-in storage) output allows the user to detect lock-up, which may occur if power supplies are disconnected. Different outputs on ADIS and Flag 1 indicate lock-up. The register must then be cleared.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

description (continued)

A Clear input will allow the user to clear all the registers of the TMS 4006 JC/NC simultaneously.

TMS 4006 JC/NC can be connected in cascade or in parallel to extend system storage capacity in increments of six digits and/or 13 characters. To extend the character positions, two controls are provided: a next-register input clock (NRC), which provides the input clock signal to the next register in a cascaded string, and a previous-register output clock (PRC) which provides the output clock signal to the previous register in a cascaded string.

"TMS 4006 JC" is the part number for a unit mounted in a 28-pin ceramic dual-in-line package. In a 28-pin plastic package the device is numbered "TMS 4006 NC".

operation

Transferring data into the device occurs on the positive-going edge of DIC. Output data appears on the positive-going edge of the DOC and resets to one on the negative-going edge of the DOC.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range* . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range* . . . . . −30 V to 0.3 V
Clock and data input voltage ranges* . . . . . −30 V to 0.5 V
Operating free-air temperature ranges . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

* These voltages are with respect to network ground terminal.

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNIT
Supply voltage V_{GG}	−23	−24	−28	V
Supply voltage V_{DD}	−13	−14	−18	V
Data input voltage				
$V_{in(0)}$ logical 0	0	−2.0	−3.0	V
$V_{in(1)}$ logical 1	−11	−12	−16	V
Clock input voltage				
$V_{\phi(0)}$ logical 0	0	−2.0	−3.0	V
$V_{\phi(1)}$ logical 1	−11	−12	−16	V
S/P input				
Serial mode	−0.3	0	−1.5	V
Parallel mode	−23	−24	−28	V
Clear command				
Logical 0	+0.3	0	−1.5	V
Logical 1	−23	−24	−28	V
Marker bit for serial input	0	−2.0	−3.0	V
Width of data pulse $t_{p(data)}$†	10			μsec
Rise-time of clock pulses, $t_{r(clock)}$†			2	μsec
Fall-time of clock pulses, $t_{f(clock)}$†			2	μsec
Clock repetition rate†	0		25.0	kHz
Width of clock pulses, $t_{p(clock)}$†	5			μsec
Overlap of data to clock, t_{OV}†	0	1.0		μsec

† See Timing Diagram

NOTE: Maximum speed of operation will be obtained when operating at the nominal values. The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies.

14

electrical characteristics (under nominal operating conditions at 25°C unless otherwise specified)

	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
$V_{out(1)}$	Logical 1 output voltage		−11		−16	V
$V_{out(0)}$	Logical 0 output voltage		−2.0	−2.5	−3.0	V
Z_{out}	Output impedance	V_{out} = 0 to 3 V		700	1000	Ω
	All flag outputs*	$R_L \leqslant$ 50 kΩ to GND	45			μA
PRC (1)	Previous register clock logical 1 level	$R_L \geqslant$500 kΩ to GND $C_L \leqslant$20 pF	−8	−10	−12	V
PRC (0)	Previous register clock logical 0 level	$R_L \geqslant$500 kΩ to GND, $C_L \leqslant$20 pF	−2.0	−2.5	−3.0	V
NRC (1)	Next register clock logical 1 level	$R_L \geqslant$500 kΩ to GND $C_L \leqslant$20 pF	−8	−10	−12	V
NRC (0)	Next register clock logical 0 level	$R_L \geqslant$500 kΩ to GND $C_L \leqslant$20 pF	−2.0	−2.5	−3.0	V
$I_{in(1)}$	Logical 1 level input leakage current	V_{in} = −15 V, V_{DD} = 0 V, V_{GG} = 0 V			6.0	μA
$I_{in(1)\phi}$	Logical 1 level input leakage current into the clock input	$V_{in\phi}$ = −20 V, V_{DD} = 0 V, V_{GG} = 0 V			10.0	μA
C_{in}	Capacitance of data input	V_{in} = 0 V, T_A = 25°C, $F_{(clock)}$ = 25 kHz		3.0	5.0	pF
$C_{in\phi}$	Capacitance of clock inputs	V_{in} = 0 V, T_A = 25°C, $F_{(clock)}$ = 25 kHz		3.0	5.0	pF
I_{DD}	Supply current into V_{DD} terminal	V_{DD} = −14 V, V_{GG} = −24 V		20	30	mA
I_{GG}	Supply current into V_{GG} terminal	V_{DD} = −14 V, V_{GG} = −24 V		4	10	mA
	Power dissipation			250		mW

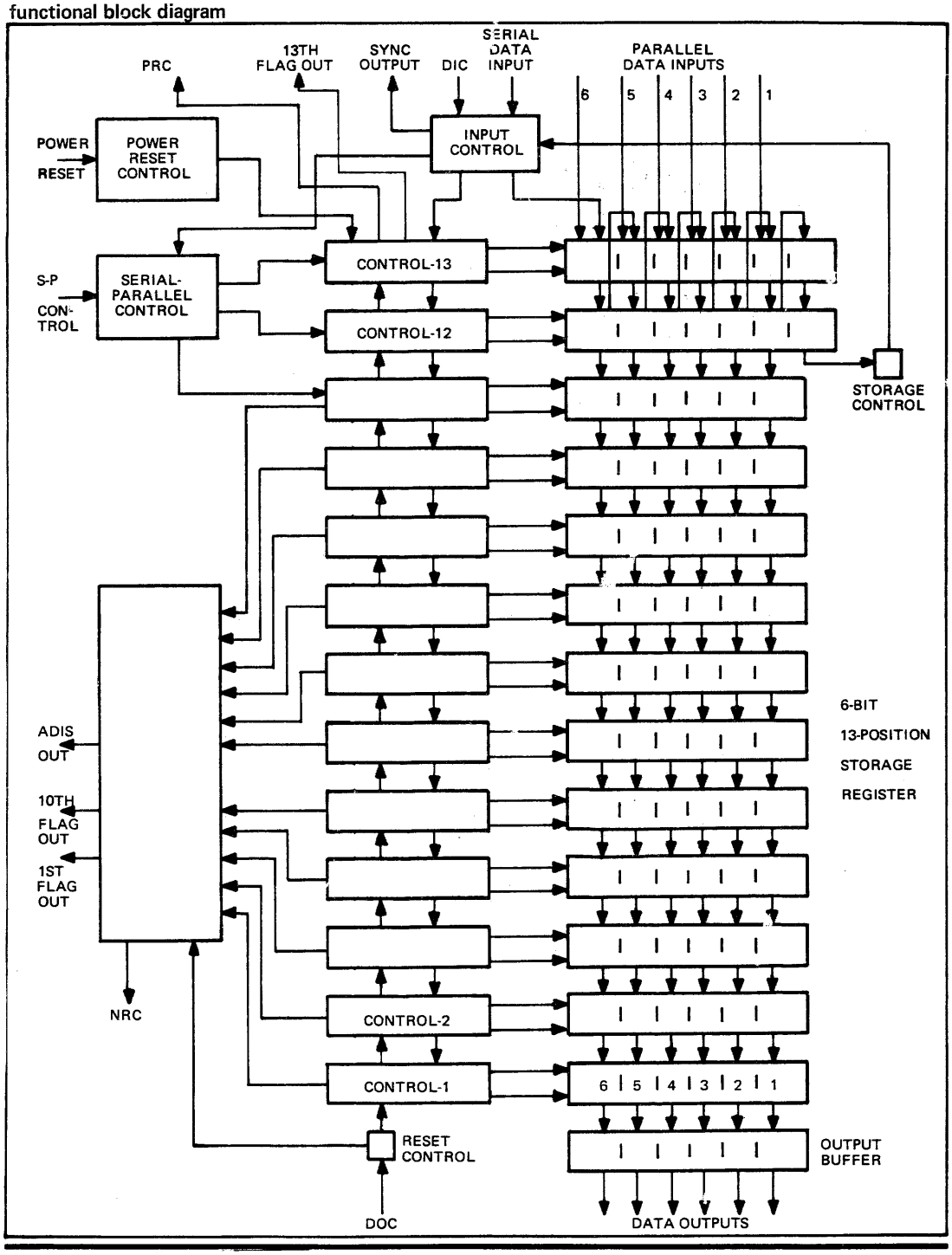
* Includes SYNC, 1st Flag, 10th Flag, 13th Flag and ADIS.

switching characteristics

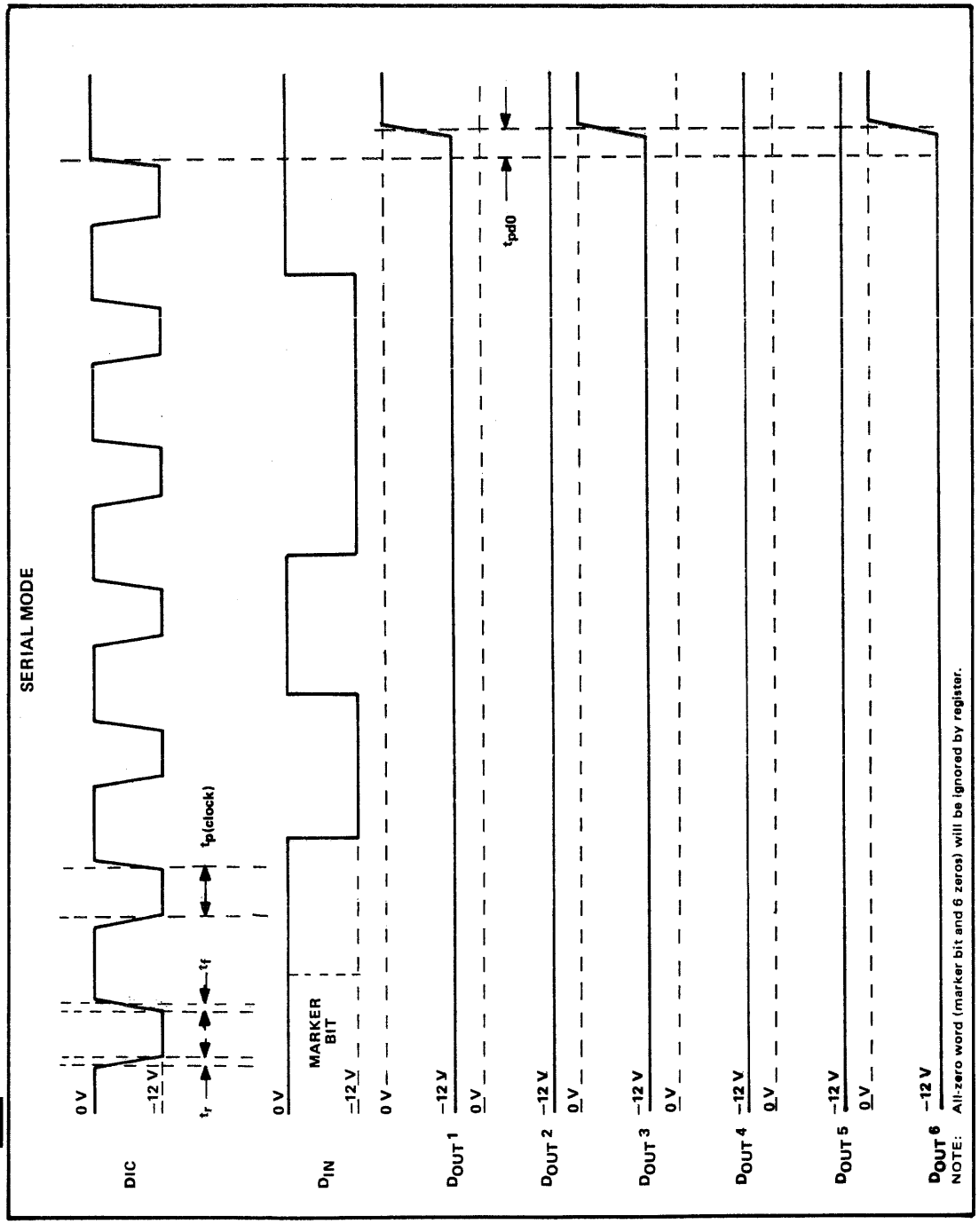
	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from DIC to appearance of data at output of empty register (13 register levels of delay)	(See Timing Diagram)		5	7	μsec
t_{pd0}	Propagation delay time to logical 0 level from DIC to appearance of data at output of empty register (13 register levels of delay)	(See Timing Diagram)		5	7	μsec
t_{pda}	Propagation delay time to Flag 10 turn-on from DIC to appearance of data at level 10 (4 register levels of delay).	(See Timing Diagram)		1	2	μsec
t_{pdb}	Propagation delay time to Flag 10 turn-off from DOC to disappearance of data at level 10 (10 register levels of delay)	(See Timing Diagram)		3	5	μsec
t_{pdc}	Propagation delay time to Flag 13 turn-off from DOC to disappearance of data at level 13 (13 register levels of delay).	(See Timing Diagram)		5	7	μsec

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram



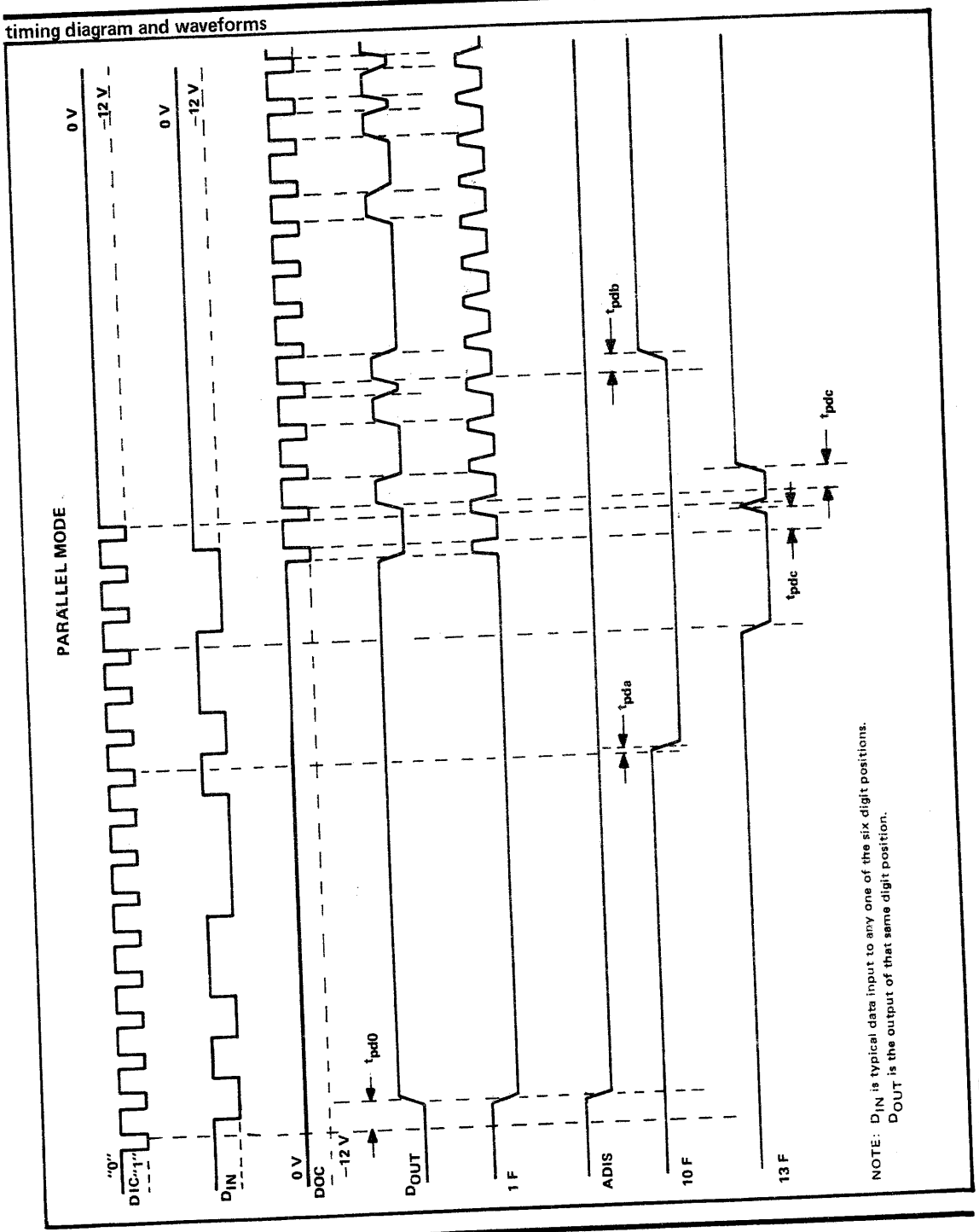
timing diagram and waveforms



NOTE: All-zero word (marker bit and 6 zeros) will be ignored by register.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

timing diagram and waveforms



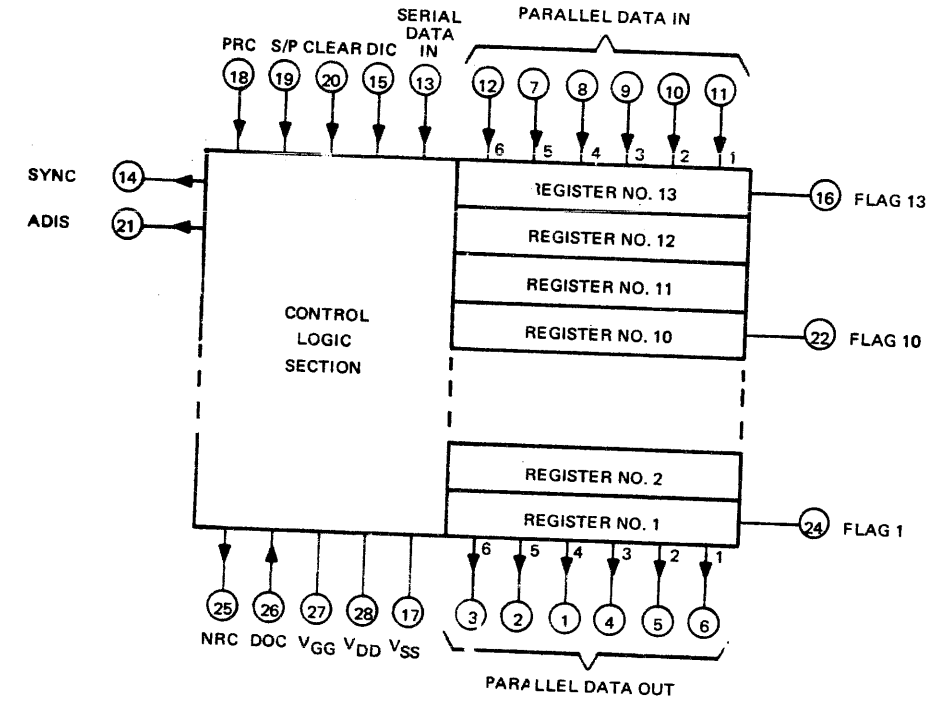
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4006 JC, TMS 4006 NC
DIGITAL STORAGE BUFFER

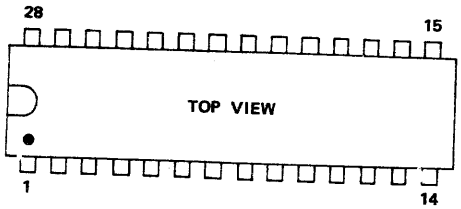
mechanical data

The digital storage buffer is available in both a 28-pin hermetically sealed dual-in-line package (TMS 4006 JC) and a 28-pin dual-in-line plastic package (TMS 4006 NC). The package is designed for insertion in mounting hole rows on 0.600-inch centers. (See MOS/LSI packaging section.).

pin configuration



PRC	–	PREVIOUS-REGISTER CLOCK
NRC	–	NEXT-REGISTER CLOCK
ADIS	–	ANY DATA IN STORAGE
S/P	–	SERIAL/PARALLEL CONTROL
DIC	–	DATA-INPUT CLOCK
DOC	–	DATA-OUTPUT CLOCK
V_{SS}	–	SUBSTRATE
V_{DD}	–	DRAIN POWER SUPPLY
V_{GG}	–	GATE POWER SUPPLY

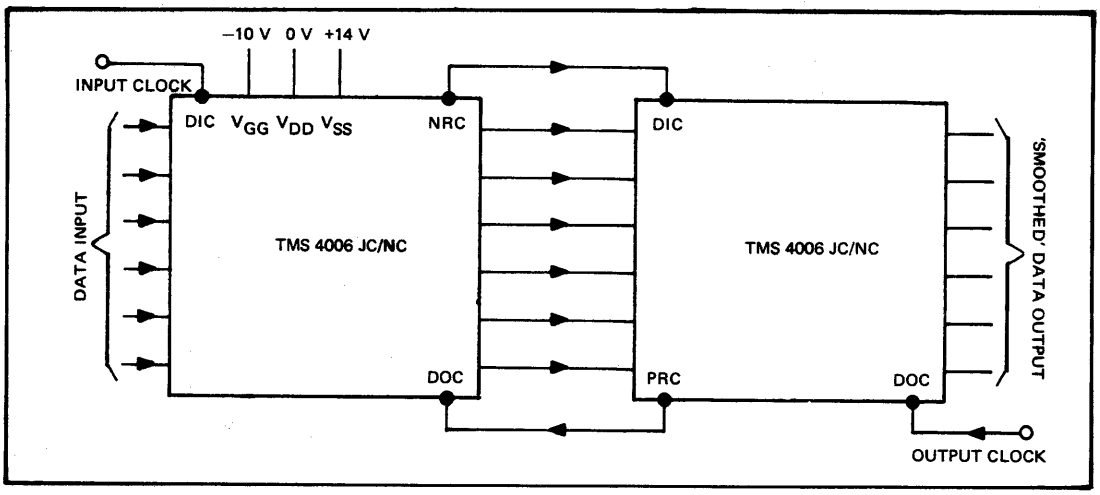


TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

memory expansion

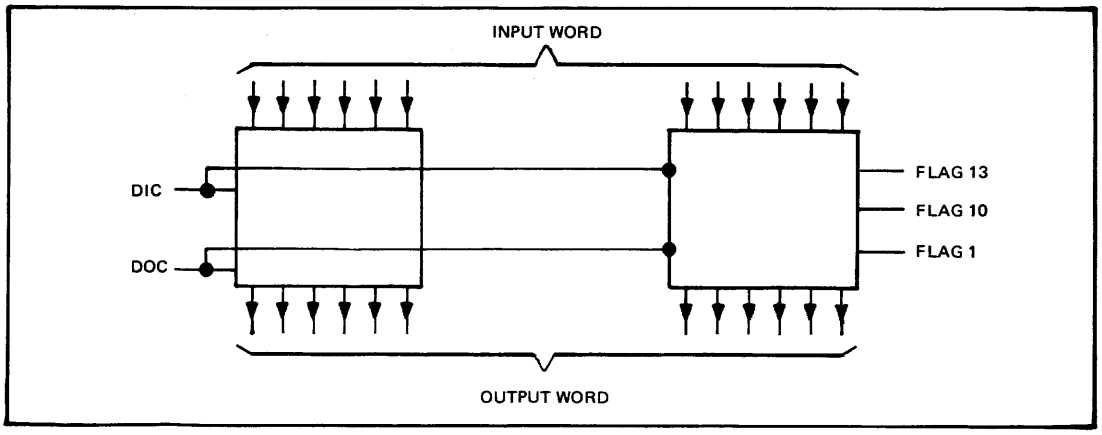
DSBs can be connected in cascade or in parallel to extend system storage capacity in increments of six digits and/or 13 characters. To extend the character positions, two controls are provided: an NRC which provides the input clock signal to the next register in a cascaded string, and a PRC which provides the output clock signal to the previous register in a cascaded string. There is no limit, in terms of performance, to the number of registers in a cascaded string. To extend the digit positions, the input and output control signals of a number of registers are tied in parallel. N registers tied in this fashion to store 6N digit characters can only accept characters serially in 6-bit sub-characters with the restriction that a marker pulse must proceed each 6-bit sub-character. There are no restrictions on input character format in the parallel mode.

a) Cascading



Digital storage buffers can be cascaded very simply to provide extra capacity since all the control clocks and gating are generated internally permitting direct connection of one DSB to the next.

b) Paralleling



14

TMS 6000 JR, TMS 6000 NC
COMMON-SOURCE 10-CHANNEL ANALOG SWITCH

DESIGNED FOR HIGH-SPEED MULTIPLEXING APPLICATIONS

- Dual-in-line package
- $R_{DS(ON)}$ = 200 Ω

description

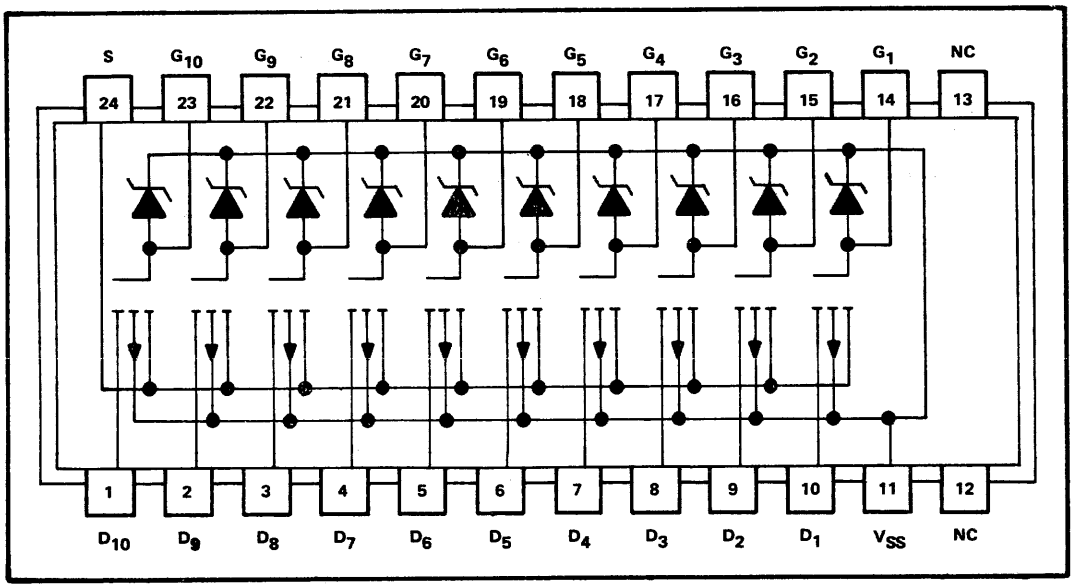
The TMS 6000 JR/NC analog switch is a P-channel enhancement-mode MOS monolithic integrated circuit, designed for high-speed multiplexing applications. It consists of ten MOS transistors having all ten sources interconnected.

A gate input impedance greater than 10^{10} ohms coupled with low-source-cutoff current, zero inherent offset voltage, and low on-state resistance ideally suits these switches for time-division multiplexing of analog and digital signals.

"TMS 6000 JR" designates a unit mounted in a 24-pin hermetically sealed ceramic dual-in-line package, and "TMS 6000 NC" is the part number for a unit mounted in a 24-pin dual-in-line plastic package.

schematic and pin configuration

TOP VIEW



D = Drain G = Gate S = Source V_{SS} = Substrate NC = No Connection

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Drain-source voltage	−30 V
Gate-source voltage	−30 V
Gate-drain voltage	−30 V
Drain current	−50 mA
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = -10\ \mu A$,	$V_{GS} = 0$ V	−30			V
$V_{(BR)GSS}$	Gate-source breakdown voltage	$I_G = -10\ \mu A$,	$V_{DS} = 0$ V	−30			V
$V_{(BR)SDS}$	Source-drain breakdown voltage	$I_S = -10\ \mu A$,	$V_{GD} = 0$ V	−30			V
I_{GSSF}	Gate-terminal forward current	$V_{GS} = -20$ V,	$V_{DS} = 0$ V		−0.05	−1	nA
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = -20$ V,	$V_{GS} = 0$ V			−3	nA
I_{SDS}	Zero-gate-voltage source current	$V_{SD} = -20$ V,	$V_{GD} = 0$			−6	nA
$V_{GS(th)}$	Gate-source threshold voltage	$V_{DS} = 0$ V,	$I_D = -10\ \mu A$	−2.5	−4	−6	V
$r_{DS(on)}$	Static-drain-source on-state resistance	$V_{GS} = -20$ V,	$I_D = -100\ \mu A$		140	200	Ω
$\lvert Y_{fs} \rvert$	Small-signal common-source forward transadmittance	$V_{DS} = -10$ V, $f = 1$ kHz	$V_{GS} = -10$ V,		3		mmho
$C_{(in)}$	Input capacitance (See Note 1)	$V_{DS} = -5$ V,	$V_{GS} = 0$ V		4	7	pF
$C_{(out)}$	Output capacitance (See Note 2)	$V_{SD} = -5$ V, $f = 1$ MHz	$V_{GS} = -5$ V,		13	20	pF
C_{gs}	Gate-source capacitance (See Note 3)	$V_{DS} = 0$ V, $f = 1$ MHz	$V_{GS} = 0$ V,		3	4.5	pF
C_{gd}	Gate-drain capacitance (See Note 3)	$V_{DS} = 0$ V, $f = 1$ MHz	$V_{GS} = 0$ V		2	3	pF
$t_{d(on)}$	Turn on delay time	See Switching Circuit			22	33	ns

NOTES: 1. $C_{(in)}$ is the capacitance between the drain terminal and all other terminals of the transistor under test.
2. $C_{(out)}$ is the capacitance between the source terminal and all other terminals of the transistor under test.
3. C_{gs} and C_{gd} measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The drain and substrate, respectively, are connected to the guard terminal of the bridge.

mechanical data

This device is available in both a 24-pin hermetically sealed ceramic dual-in-line package (TMS 6000 JR) and a 24-pin plastic package (TMS 6000 NC). The packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

switching characteristics

PARAMETER MEASUREMENT INFORMATION

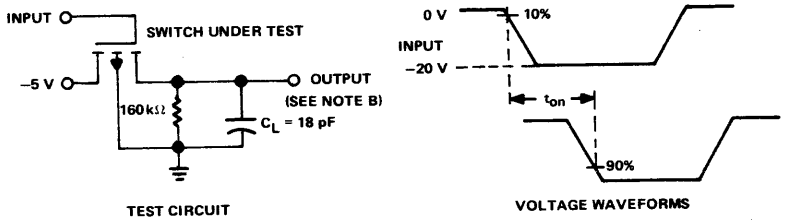


FIGURE 1

NOTES: A. The input waveform is supplied by a generator with the following characteristics: $t_r \leqslant 10$ ns, $Z_{out} = 50\ \Omega$.
B. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leqslant 10$ ns, $R_{in} \geqslant 10\ M\Omega$, C_L includes oscilloscope input capacitance plus stray capacitance.

TYPICAL CHARACTERISTICS

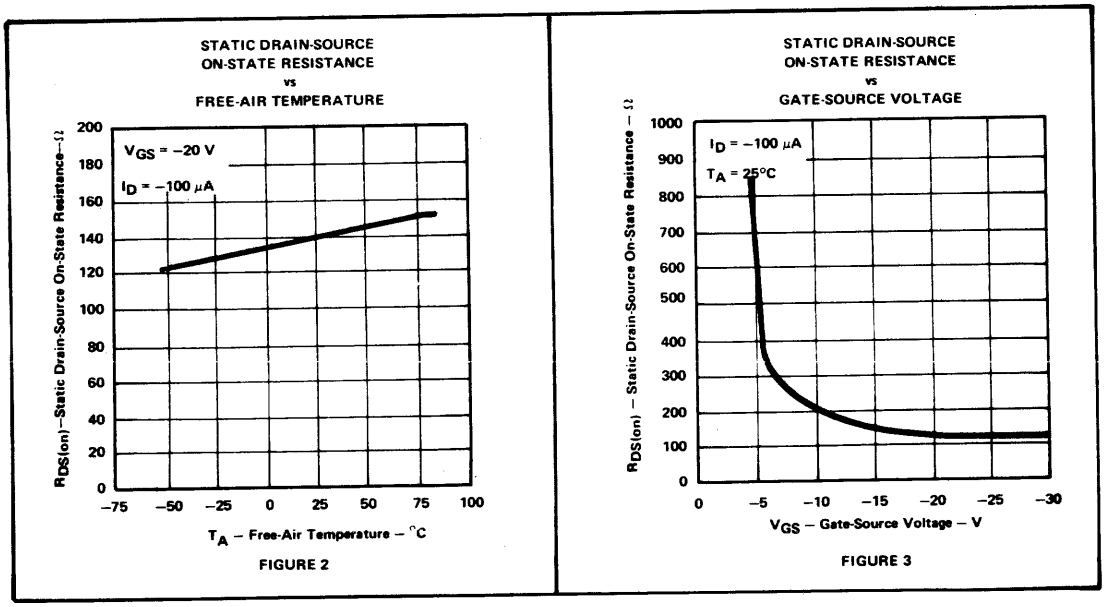


FIGURE 2

FIGURE 3

typical applications data

In the following circuit, each input is sequentially connected through an MOS switch to an output circuit represented by load resistance R_L. A Series 54/74 TTL counter and decimal decoder are used to obtain sequential driving from a single clock.

An interface circuit using a PNP transistor translates TTL output voltage levels to those required by the MOS switch. In this circuit, +5 volts is used to turn the switch off, −20 volts is used to turn it on. Because the transistor saturates, a storage time exists which delays turn-off. This delay (about 150 to 300 ns) is used in the interface circuit shown to

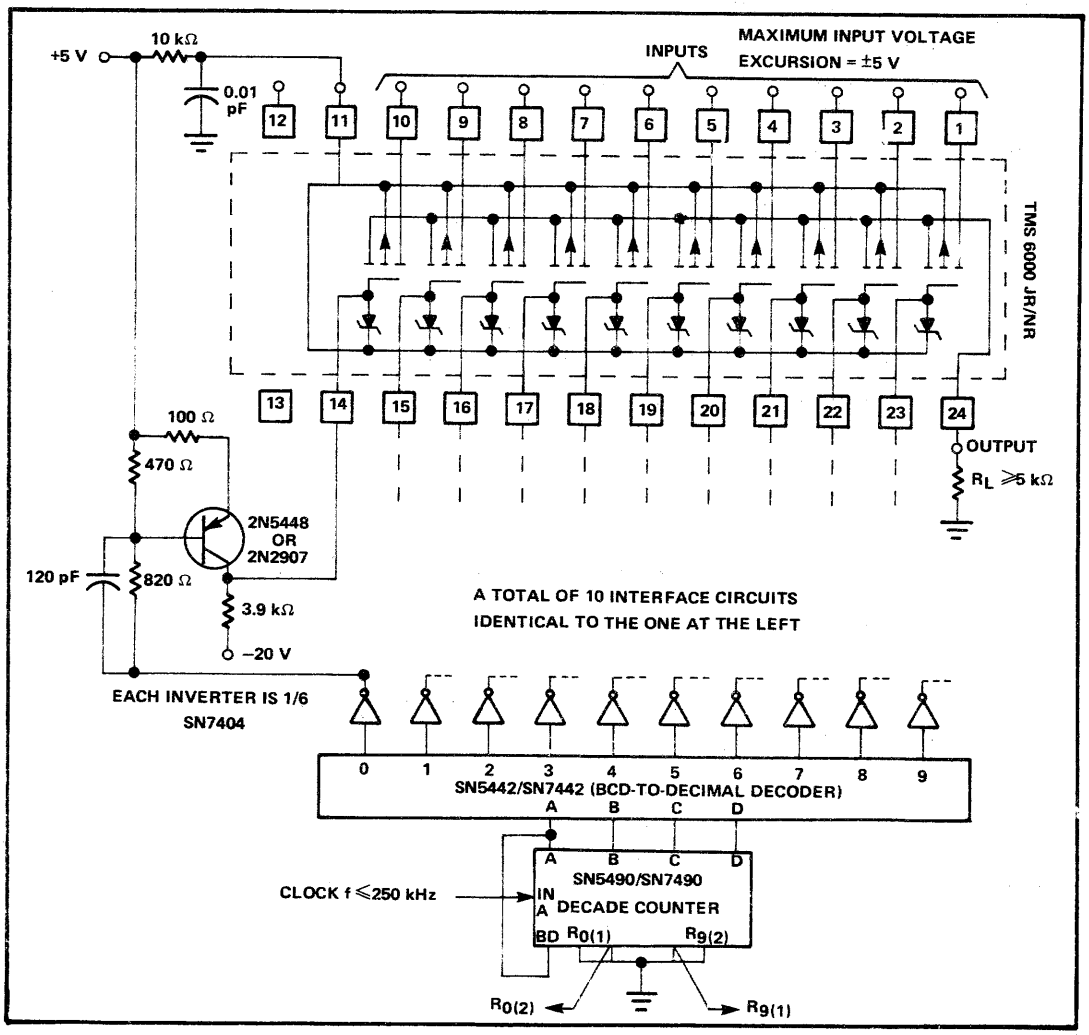
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

typical applications data (continued)

allow the previous MOS switch to turn off comp.. tely before the next one turns on. Cloc‹ frequency, t_{clock}, is limited by interface circuit storage and fall times to about 250 kHz before these times become an appreciable fraction of a clock cycle.

The substrate is biased at +12 V to allow the drains and sources of the MOS switches to go positive without forward-biasing the drain-substrate and source-substrate diffused diodes. Only leakage current flows into the substrate, so the simple RC filter shown is sufficient to prevent noise from the +12 volt supply from interfering with switch operation.

DIRECT-COUPLED MULTIPLEXER ADDRESSED FROM SERIES 54/74 TTL



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 6002 JR, TMS 6002 NC
SIX-CHANNEL ANALOG SWITCHES

DESIGNED FOR HIGH-SPEED MULTIPLEXING APPLICATIONS

- Dual-in-line ceramic or plastic package
- $R_{DS(on)}$ . . . 200 Ω maximum

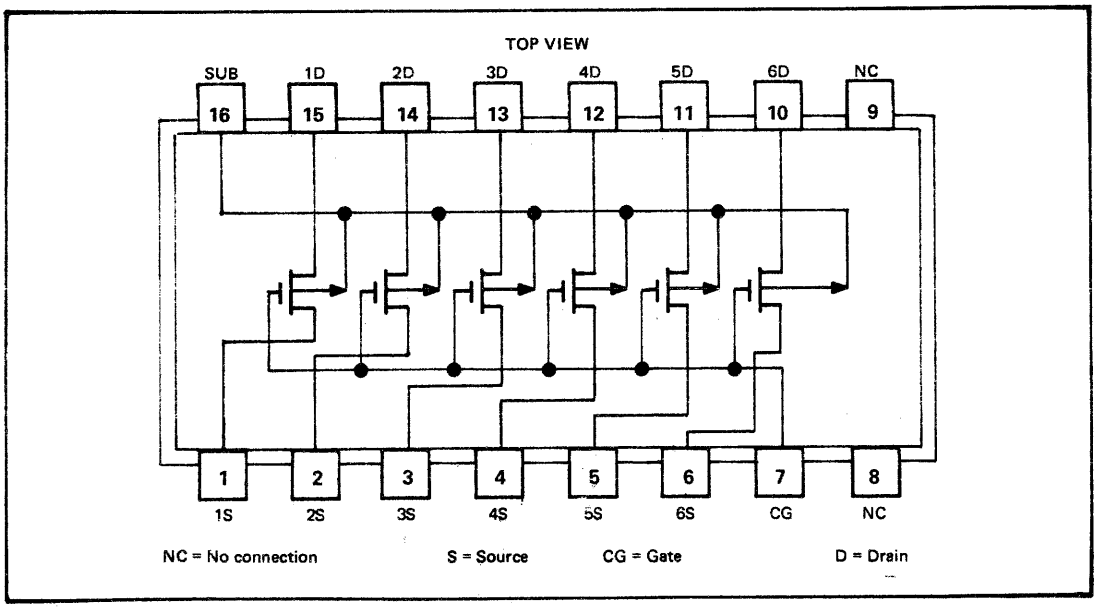
description

The TMS 6002 JR/NC analog switch is a P-channel enhancement-mode MOS monolithic integrated circuit, utilizing thick-oxide technology. This general-purpose device consists of six MOS transistors having all six gates interconnected. The common gate is protected by a diode circuit and must be switched by an external driver. The analog switch is packaged in 16-pin dual-in-line ceramic package.

A gate input impedance greater than 10^{10} ohms coupled with low source-cutoff current, zero inherent offset voltage, and low on-state resistance ideally suits this switch for time-division multiplexing.

schematic and pin configuration

This device is available in both a 16-pin hermetically sealed ceramic dual-in-line package (TMS 6000 JR) and a 16-pin plastic package (TMS 6002 NC). The packages are designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Drain-source voltage	−30 V
Forward gate-source voltage (See Note 1)	−30 V
Gate-drain voltage	−30 V
Drain current	−50 mA
Gate-terminal reverse current (forward direction for zener clamp)	0.1 mA
Continuous dissipation at (or below) 25°C free-air temperature (see Note 2)	500 mW
Operating free-air temperature range (See Note 3)	−55°C to 85°C
Storage temperature range	−55°C to 150°C

NOTES: 1. Forward gate-source voltage is of such polarity that an increase in its magnitude above a threshold level causes the channel resistance to decrease.
2. Derate linearly to 85°C free-air temperature at the rate of 8.3 mW/°C.
3. Operating free-air temperature for TMS 6002 NC is −25°C to +85°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = -10\ \mu A$, $V_{GS} = 0$	−30			V
$V_{(BR)GSS}$	Gate-source breakdown voltage	$I_G = -10\ \mu A$, $V_{DS} = 0$	−30			V
$V_{(BR)SDS}$	Source-drain breakdown voltage	$I_S = -10\ \mu A$, $V_{GD} = 0$	−30			V
I_{GSSF}	Gate-terminal forward current 6 gates	$V_{GS} = -20$ V, $V_{DS} = 0$		0.3	6.0	nA
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = -20$ V, $V_{GS} = 0$			3.0	nA
I_{SDS}	Zero-gate-voltage source current	$V_{SD} = -20$ V, $V_{GS} = 0$			6.0	nA
$V_{GS(th)}$	Gate-source threshold voltage	$V_{DG} = 0$, $I_D = -10\ \mu A$	−2.5	−4	−6	V
$R_{DS(on)}$	Static drain-source on-state resistance	$V_{GS} = -20$ V, $I_D = -100\ \mu A$		140	200	Ω
$\lvert y_{fs} \rvert$	Small-signal common gate forward transfer admittance	$V_{DS} = -10$ V, $V_{GS} = -10$ V, f = 1 kHz		3		mmho
$C_{(in)}$	Input capacitance (See Note 3)	$V_{DS} = -5$ V, $V_{GS} = 0$, f = 1 MHz		4	7	pF
$C_{(out)}$	Output capacitance (See Note 4)	$V_{SD} = -5$ V, $V_{GS} = -5$ V, f = 1 MHz		4	7	pF
C_{gs}	Gate-source capacitance (See Note 5)	$V_{DS} = 0$, $V_{GS} = 0$, f = 1 MHz		3	4.5	pF
C_{gd}	Gate-drain capacitance (See Note 5)	$V_{DS} = 0$, $V_{GS} = 0$,		2	3	pF
t_{don}	Turn on delay time	See Switching Circuit		50	75	ns

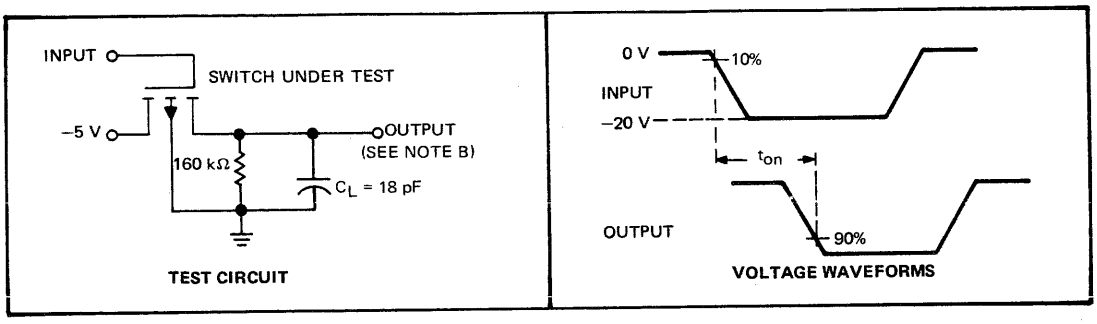
NOTES: 3. $C_{(in)}$ is the capacitance between the drain terminal and all other terminals of the transistor under test.
4. $C_{(out)}$ is the capacitance between the source terminal and all other terminals of the transistor under test.
5. C_{gs} and C_{gd} measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The drain and substrate or the source and substrate, respectively, are connected to the guard terminal of the bridge.

† The body (substrate) terminal is grounded to the reference terminal unless otherwise noted.

14

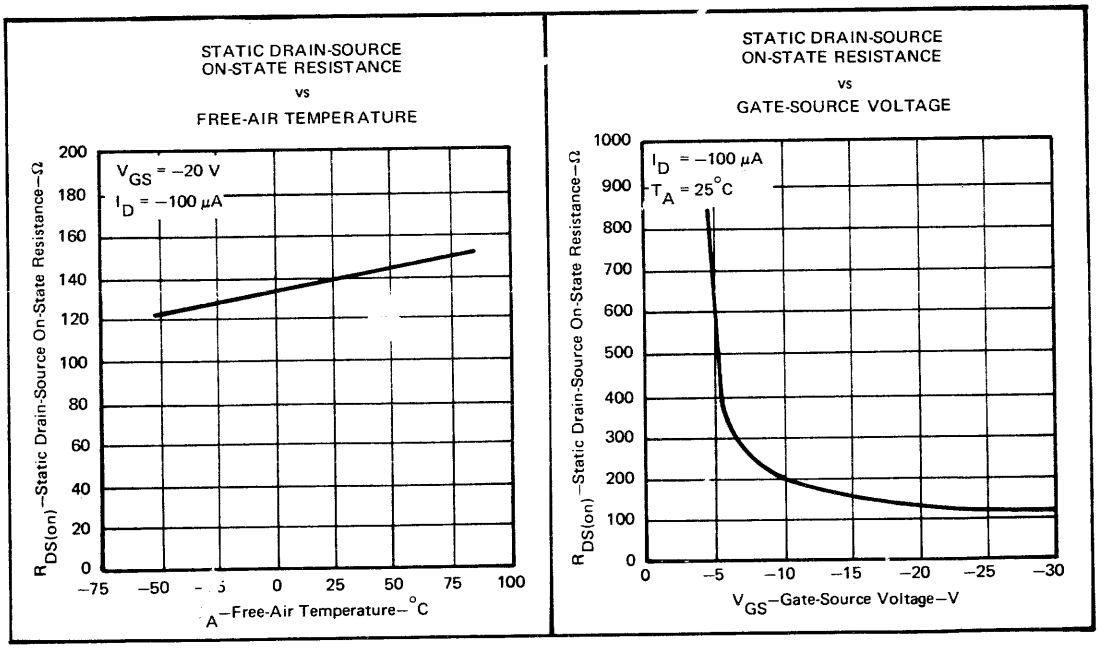
switching characteristics

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 10$ ns, $Z_{out} = 50\ \Omega$.
B. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 10$ ns, $R_{in} \geq 10\ M\Omega$, C_L includes oscilloscope input capacitance plus stray capacitance.

TYPICAL CHARACTERISTICS



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 6005 JR, NC; TMS 6009 JR, NC
SIX-CHANNEL ANALOG SWITCHES

FEBRUARY, 1971

DESIGNED FOR HIGH-SPEED MULTIPLEXING APPLICATIONS

- Dual-in-line package
- $r_{DS(on)}$ . . . 200 Ω max

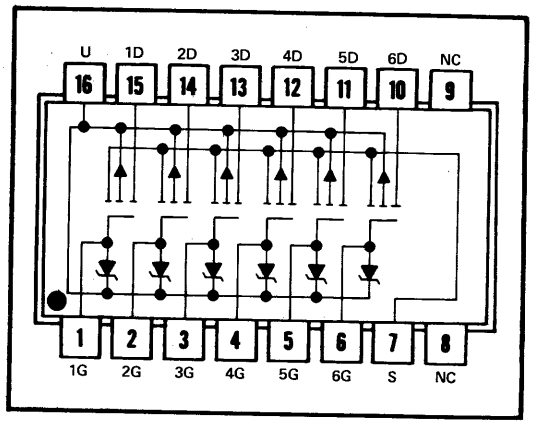
description

The TMS 6005 JR/NC and TMS 6009 JR/NC analog switches are P-channel enhancement-mode MOS monolithic integrated circuits utilizing thick-oxide technology. Each consists of six MOS transistors having all six sources interconnected. The gate of each MOS device is protected by a diode circuit and must be switched by an external driver. The analog switches are packaged in 16-pin dual-in-line ceramic packages or 16-pin plastic packages.

The TMS 6009 JR/NC is intended for applications requiring extremely low leakage currents. The TMS 6005 JR/NC is a general-purpose device.

A gate input impedance greater than 10^{10} ohms coupled with low source cutoff current, zero inherent offset voltage, and low on-state resistance makes these switches ideally suited for time-division multiplexing of analog and digital signals.

TOP VIEW



G — Gate S — Source D — Drain
NC — No Internal connection

mechanical data

Mounted in a 16-pin hermetically sealed ceramic dual-in-line package the analog switches are numbered TMS 6005 JR, and TMS 6009 JR. In 16-pin plastic packages the devices are designated TMS 6005 NC and TMS 6009 NC. The packages are designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Drain-source voltage	−30 V
Forward gate-source voltage (see Note 1)	−30 V
Gate-drain voltage	−30 V
Drain current	−50 mA
Gate-terminal reverse current (forward direction for zener clamp)	0.1 mA
Continuous dissipation at (or below) 25°C free-air temperature (see Note 2)	500 mW
Operating free-air temperature range (see Note 3)	−55°C to 85°C
Storage temperature range	−55°C to 150°C

NOTES: 1. Forward gate-source voltage is of such polarity that an increase in its magnitude above a threshold level causes the channel resistance to decrease.
2. Derate linearly to 85°C free-air temperature at the rate of 8.3 mW/°C.
3. Operating temperature range for TMS 6005 NC and TMS 6009 NC is −25 to +85°C.

electrical characteristics at 25°C free-air temperature

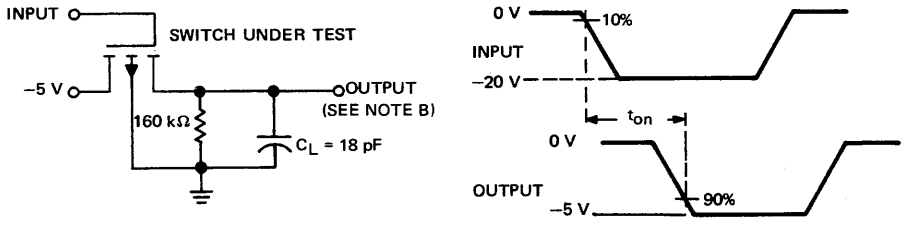
PARAMETER		TEST CONDITIONS†	TMS6005JR			TMS6009JR			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = -10\ \mu A$, $V_{GS} = 0$	−30			−30			V
$V_{(BR)GSS}$	Gate-source breakdown voltage	$I_G = -10\ \mu A$, $V_{DS} = 0$	−30			−30			V
$V_{(BR)SDS}$	Source-drain breakdown voltage	$I_S = -10\ \mu A$, $V_{GD} = 0$	−30			−30			V
I_{GSSF}	Gate-terminal forward current	$V_{GS} = -20$ V, $V_{DS} = 0$			−5		−0.05	−1	nA
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = -20$ V, $V_{GS} = 0$			−10			−3	nA
I_{SDS}	Zero-gate-voltage source current (total for six switches)	$V_{SD} = -20$ V, $V_{GD} = 0$			−30			−6	nA
$V_{GS(th)}$	Gate-source threshold voltage	$V_{DG} = 0$, $I_D = -10\ \mu A$	−2.5	−4	−6	−2.5	−4	−6	V
$r_{DS(on)}$	Static drain-source on-state resistance	$V_{GS} = -20$ V, $I_D = -100\ \mu A$		140	200		140	200	Ω
$\lvert y_{fs} \rvert$	Small-signal common-source forward transfer admittance	$V_{DS} = -10$ V, $V_{GS} = -10$ V, f = 1 kHz		3			3		mmho
$C_{(in)}$	Input capacitance (see Note 3)	$V_{DS} = -5$ V, $V_G = V_S = V_{SS}$ f = 1 MHz		4	7		4	7	pF
$C_{(out)}$	Output capacitance (see Note 4)	$V_{SD} = -5$ V, $V_G = V_S = V_{SS}$ f = 1 MHz		13	20		13	20	pF
C_{gs}	Gate-source capacitance (see Note 5)	$V_{DS} = 0$, $V_{GS} = 0$, f = 1 MHz		3	4.5		3	4.5	pF
C_{gd}	Gate-drain capacitance (see Note 5)	$V_{DS} = 0$, $V_{GS} = 0$, f = 1 MHz		2	3		2	3	pF
t_{on}	Turn-on time	See Figure 1		50	75		50	75	ns

NOTES: 3. $C_{(in)}$ is the capacitance between the drain terminal and all other terminals of the transistor under test.
4. $C_{(out)}$ is the capacitance between the source terminal and all other terminals of the transistor under test.
5. C_{gs} and C_{gd} measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The drain and substrate or the source and substrate, respectively, are connected to the guard terminal of the bridge.

†The body (substrate) terminal is grounded to the reference terminal unless otherwise noted.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 10$ ns, $Z_{out} = 50\ \Omega$.
B. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 10$ ns, $R_{in} \geq 10\ M\Omega$, C_L includes oscilloscope input capacitance plus stray capacitance.

FIGURE 1

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs FREE-AIR TEMPERATURE

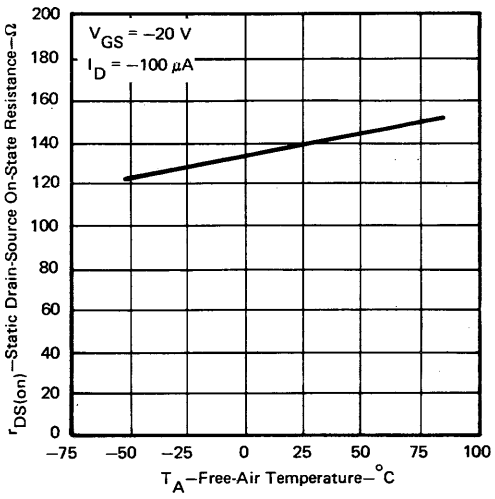


FIGURE 2

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs GATE-SOURCE VOLTAGE

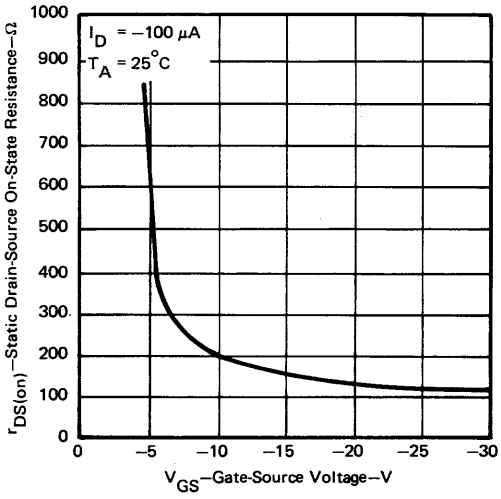


FIGURE 3

TYPICAL APPLICATION DATA

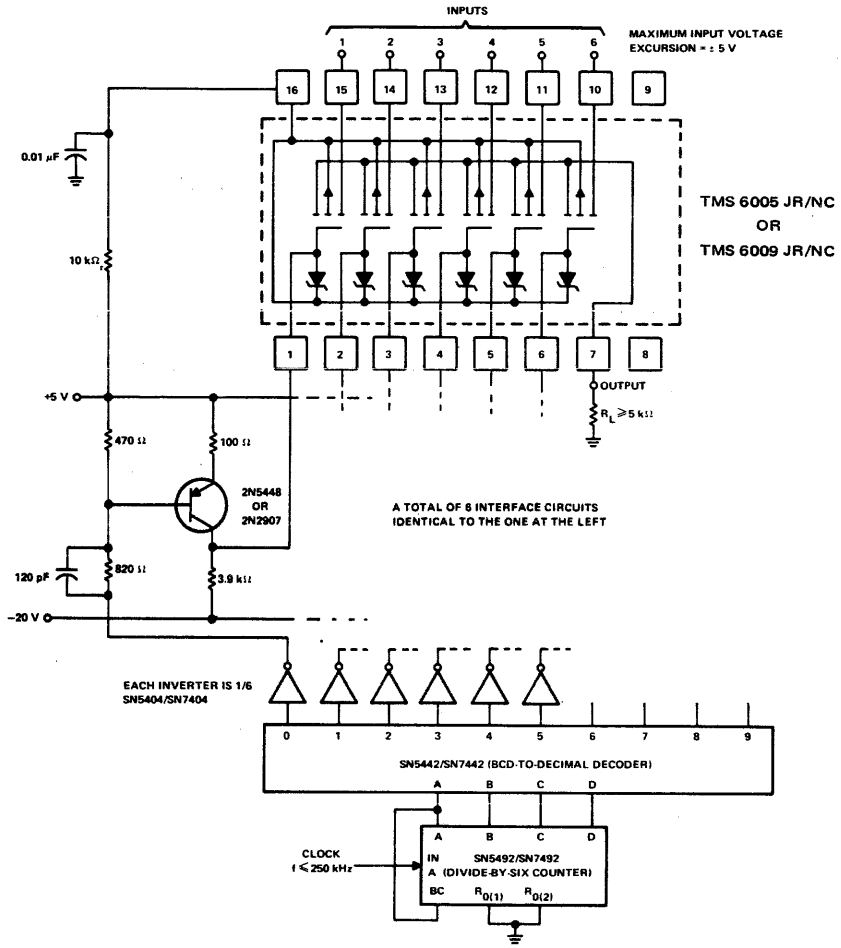
In the following circuit, each input is sequentially connected through an MOS switch to an output circuit represented by load resistance R_L. A Series 54/74 TTL counter and decimal decoder are used to obtain sequential driving from a single clock.

An interface circuit using a PNP transistor translates TTL output voltage levels to those required by the MOS switch. In this circuit, +5 volts is used to turn the switch off, −20 volts is used to turn it on. Because the transistor saturates, a storage time exists which delays turn-off. This delay (about 150 to 300 ns) is used in the interface circuit shown to allow the previous MOS switch to turn off completely before the next one turns on. Clock frequency, f_{clock}, is limited by interface circuit storage and fall times to about 250 kHz before these times become an appreciable fraction of a clock cycle.

The substrate is biased at +5 volts to allow the drains and sources of the MOS switches to go positive without forward-biasing the drain-substrate and source-substrate diffused diodes. Only leakage current flows into the substrate, therefore the simple RC filter shown is sufficient to prevent noise from the +5 volts supply from interfering with switch operation.

TYPICAL APPLICATION DATA

DIRECT-COUPLED MULTIPLEXER ADDRESSED FROM SERIES 54/74 TTL



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CUSTOM MOS/LSI

MOS/LSI is very well suited for custom design:

High level of integration	*lower package count* *lower cost*
Two dimensional design	*easy simulation* *fast turnaround times*
Simple process	*high reliability* *low cost*

To respond to the large demand for MOS/LSI custom subsystems, TI has geared its operations to handle hundreds of custom designs each year.

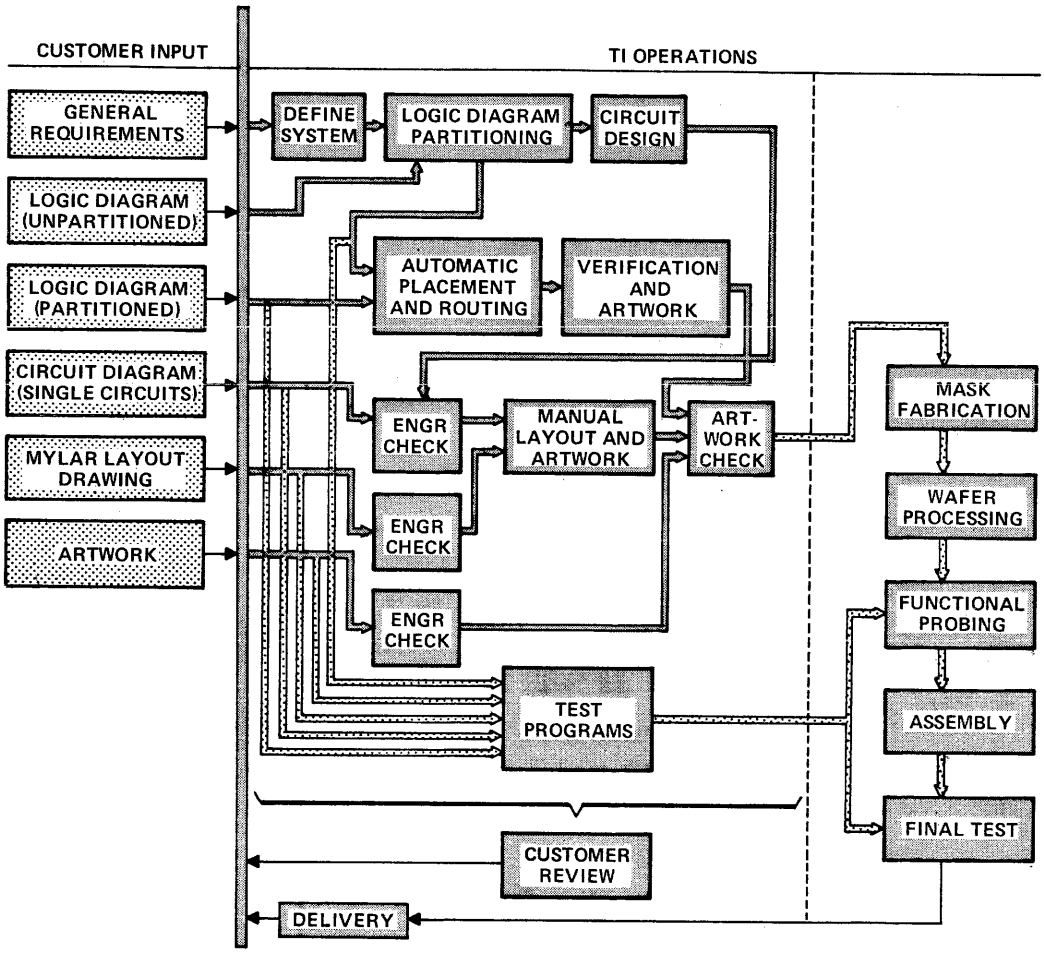
The level of complexity of MOS/LSI subsystems design is very high. Circuit designs are assisted by other specialists. A typical team approach to multichip system design will consist of

- Systems Engineers
- Circuit Designers
- Software Specialists
- Test and Reliability Engineers

In order to optimize design and minimize cost, many computer programs have been developed. In a typical MOS/LSI multichip design the following computer-aided design will be used to optimize the design:

- Subsystem simulation
- Circuit analysis
- Circuit simulation
- Automatic placement and routing (mask design)
- Manually assisted placement and routing (CRT implementation of mask design)
- Computer drawing
- Mask cutting
- Test pattern generation and grading

TI's involvement in custom MOS/LSI is complete. The TI-customer interface is very flexible. Inputs may range from general requirements ("Black Box" specifications) to finished working glass photomasks. Experience has shown that the best interface point is with partitioned logic diagrams; however, TI can also partition your logic diagrams or convert TTL/DTL implemented logic to MOS/LSI.



For more information on custom MOS/LSI design please contact the nearest TI sales office .

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SEMICONDUCTOR MEMORY ARRAYS

Multichip memory arrays are an extension of the line of memory products presently available in both MOS/LSI and bipolar technologies. Only TI has the full range of semiconductor technologies, including MOS/LSI, TTL and ECL, that permit selection of the right technologies to provide optimum memory performance.

Economy, high performance, low power requirements, high packaging density, and improved reliability are among the obvious advantages of multichip memory arrays. The standard arrays use beam leaded circuit chips thermo-compression bonded to thick film ceramic substrates for highest reliability. Standard arrays use MOS/LSI random access memory chips with TTL chips performing the decoding. MOS decoding is also available. Texas Instruments provides the total semiconductor capability required to produce complex storage functions using the best combination of technologies to meet system performance requirements.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

2048 - BIT
SEMICONDUCTOR RAM STORAGE ARRAY

FEATURES:

- High density semiconductor storage
- Adaptable to a wide variety of memory systems
- Isolated sense line
- Minimum of 200 microamperes of sense current
- Static operation — no refresh requirements
- 12 V operation
- Ceramic flat pack

description

This specification defines the SMA 1001 256 x 8 MOS Memory Array to be used as building blocks in a large Active Element Memory. The 256 x 8 MOS Memory Array is packaged as eight individual 256 x 1 MOS Memory Chips beam-leaded to a multilayer ceramic substrate.

organization

The Memory Array is organized as a 256-word by 8-bit memory. The Array has four power connections, sixteen X-address connections, sixteen Y-address connections, eight sense line connections, and sixteen digit line connections.

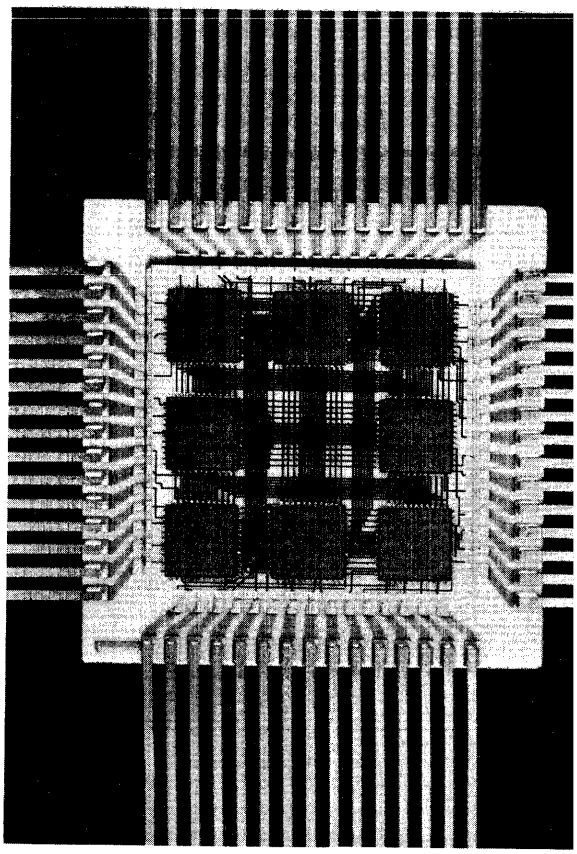
operations

Read Mode —

The contents of 8 memory cells may be non-destructively read from any of the 256 addressable cells on a single memory cycle. The digit lines will be held to the most negative level during a read operation.

Write Mode —

The contents of one to eight memory cells may be forced to a "1" or "0" state by raising the corresponding bit digit-1 or digit-0 line to the most positive voltage level. Placing a high level on both digit-1 and digit-0 lines simultaneously will not cause damage to the array. A high level on the digit-1 line corresponds to a sense current ($I_{S(1)}$) at the sense output during a read.



SMA 1001 SEMICONDUCTOR MEMORY ARRAY

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operations (continued)

Addressing –

A single memory cell in each of the 8 bits will be addressed by driving one X line and one Y line to the most negative voltage level. All other X and Y lines will be held at the most positive voltage level. A simultaneous address of up to 256 words by driving multiple X and/or Y lines to the most negative voltage level will not degrade data stored at any location if all digit lines are held low.

recommended operating conditions

	MIN	TYP	MAX	UNITS
V_{SS}	8	10	15	V
Operating temperature range with 700 FPM air flow	0	25	70	(°C)

static characteristics (V_{SS} = 12 V, T_A = 0 - 70°C)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
C_A	Address line capacitance	V_A = 0 V		95		pF
C_D	Digit line capacitance	V_D = 0 V		32		pF
C_D	Digit line capacitance	$V_D = V_{SS}$		60		pF
C_S	Sense line capacitance	V_S = 0		35		pF
$V_{A(0)}$	Address line voltage for unaddressed state	$I_{S(00)}$ = 2.5 μA MAX	6-13*			
$V_{A(1)}$	Address line voltage for addressed state	$I_{S(1)}$ = 200 μA			0.4	V
$V_{D(0)}$	Digit line write voltage	V_A = 0.4 V,	6-13*		8.5-15.5†	V
$V_{D(1)}$	Digit line non-destructive read voltage	V_A = 0.4 V,	0		1.0	V
$I_{S(0)}$	Sense line current when addressed cell contains a (0)	V_A = 0.4 V, R_S = 1 K			2.5	μA
$I_{S(1)}$	Sense line current when addressed cell contains a (1)	R_S = 1 K or less, V_A = 0.4 V	200			μA
$I_{A(2)}$	Address line leakage current	V_A = 0 V			10	μA
I_{SS}	Power supply current	V_{SS} = 12.0 V ± 5%, $V_A = V_{SS}$			85	

* The gate to source voltage must be 2 volts or less for any V_{SS}.
† This voltage must not be greater than V_{SS} + 0.5 V.

dynamic characteristics (V_{SS} = 12 V, T_A = 25°C)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
T_W	Digit line pulse width for writing into an addressed cell	V_A = 0.4 V, V_D = 0.9 V_{SS}		50		ns
T_A	Time for sense line current to reach 90% of final value after addressing	V_A = 0.2 V		25		ns

mechanical data

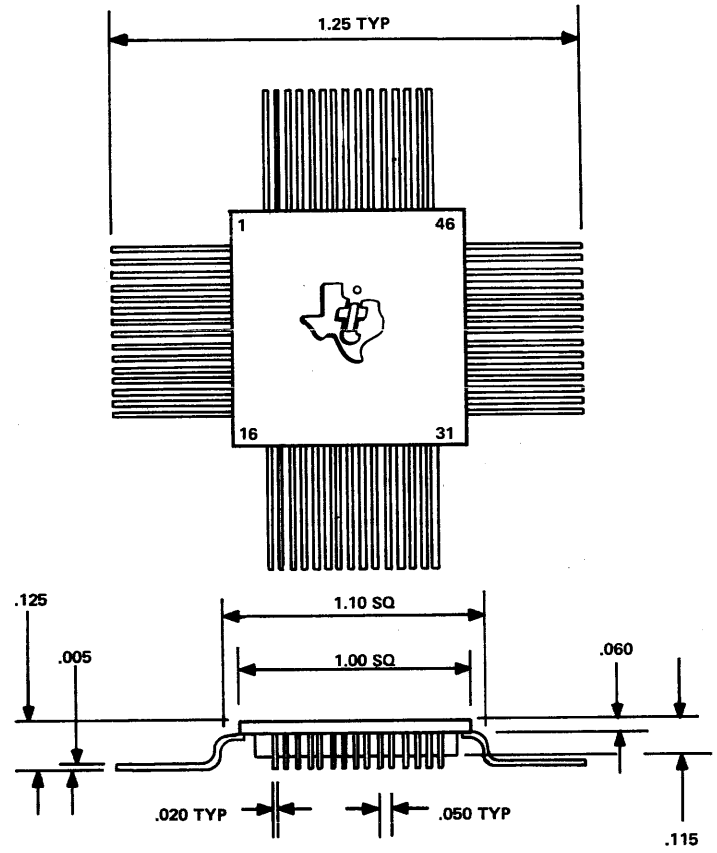
This semiconductor memory array consists of 8 individual beam leaded MOS memory chips thermocompression bonded to a multi-level interconnect system and contained in a epoxy sealed ceramic package.

The MOS chips are processed using low threshold nitride process. Beam leads and the internal interconnections are corrosion resistant and all contacts are gold to gold.

The package has a flat pack lead configuration with 60 leads on four sides on 50 mil centers.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

mechanical data (continued)



OUTLINE DIMENSIONS

pin configuration

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	Y_{15}	11	X_7	21	$D_{0\text{-}6}$	31	S_8	41	S_7	51	$D_{0\text{-}1}$
2	Y_{16}	12	X_6	22	Y_8	32	Y_1	42	V_{SS2}	52	Y_9
3	S_5	13	X_5	23	Y_7	33	V_{SS1}	43	X_{11}	53	Y_{10}
4	X_8	14	X_4	24	Y_6	34	X_9	44	X_{12}	53	Y_{11}
5	$D_{1\text{-}5}$	15	X_3	25	Y_5	35	X_{10}	45	S_1	55	Y_{12}
6	V_{DD1}	16	S_6	26	Y_4	36	S_2	46	X_{13}	56	Y_{13}
7	$D_{0\text{-}5}$	17	$D_{1\text{-}6}$	27	$D_{0\text{-}8}$	37	$D_{1\text{-}2}$	47	X_{14}	57	S_3
8	S_4	18	V_{DD2}	28	$D_{1\text{-}8}$	38	$D_{0\text{-}2}$	48	X_{15}	58	$D_{1\text{-}3}$
9	$D_{1\text{-}4}$	19	X_2	29	Y_3	39	$D_{0\text{-}7}$	49	X_{16}	59	Y_{14}
10	$D_{0\text{-}4}$	20	X_1	30	Y_2	40	$D_{1\text{-}7}$	50	$D_{1\text{-}1}$	60	$D_{0\text{-}3}$

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

2048-BIT
HIGH PERFORMANCE SEMICONDUCTOR RAM ARRAY

description

This specification defines a 2048-bit memory array to be used as a building block for organizing larger memory systems. The memory array is a multi-chip array made up of beam leaded MOS storage chips and beam leaded bipolar decoding, sense, write and control chips. This total array is packaged in a ceramic dual-in-line 28 pin package for the commercial temperature range (0 – 70°C).

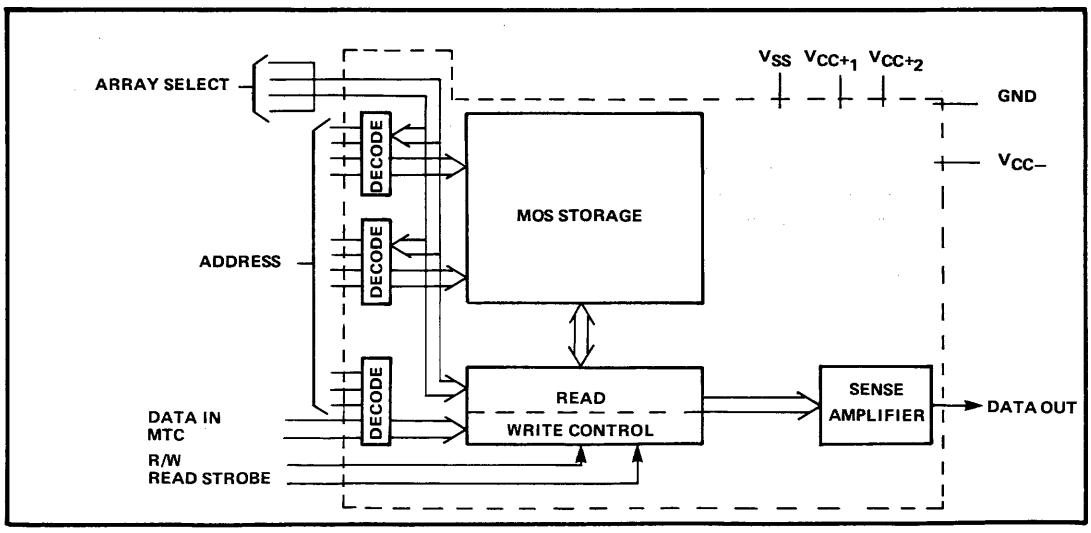
features

- Fast read access time . . . . . 125 ns typical
- Fast write time . . . . . 125 ns typical
- Fast cycle time . . . . . 150 ns typical
- Low memory power dissipation . . . . . 0.65 mW/bit typical
- Open collector output for OR tie
- Directly compatible with DTL and TTL logic circuits
- Easy memory expansion through 4 chip select inputs
- Read strobe control
- Standard TTL loading
- +5 V, GND, −5 V operation
- DIP packaging

organization

The memory array is organized as a 2K x 1 fully decoded memory.

block diagram



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operation

Read Mode – Binary levels are applied to address lines (TTL levels) and data appears at output at access time (125 ns) when READ STROBE is LOW and R/W is HIGH in the READ MODE.

Write Mode – Binary levels are applied to address lines (TTL levels). Data is present at DATA IN. R/W is LOW for the WRITE mode. READ STROBE is HIGH. MTC is LOW until indicated time in WRITE cycle.

Array Select – All four array selects must be LOW to have array selected. When array is not selected, array output is HIGH and data cannot be written into the array.

Timing – Waveform timing is shown on attached timing diagram.

absolute maximum ratings (over operating temperature range unless otherwise noted)†

V_{SS} (See Note 7)	7 V
$V_{CC}+$ (See Note 7)	7 V
$V_{CC}-$ (See Note 7)	−7 V
Input voltage (See Note 8)	5.5 V
Operating Ambient Temperature with 700 FPM of air flow	0 to 70°C
Storage temperature range	−65 to 150°C
Output sink current (Note 9)	20 mA

† Maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.

recommended operating conditions

	MIN	NOM	MAX
V_{SS}	4.75	5.0	5.25
$V_{CC}+$	4.75	5.0	5.25
$V_{CC}-$	−4.75	−5.0	−5.25
Output sink current (See Note 9)			16 mA
Operating Ambient Temperature with 700 FPM of air flow	0°C		70°C

NOTES:
1. All array selects must be LOW for array to be selected.
2. Unselected array data out at HIGH level.
3. Read strobe should be LOW for data out only during read cycle.
4. HIGH data in gives HIGH data out.
5. R/W is HIGH for read, LOW for write.
6. MTC must be LOW at all times except at end of write cycle.
7. With respect to network ground terminal.
8. Input signals must be zero or positive with respect to network ground terminal.
9. Output 1 equals output 2.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics (over ambient temperature range unless otherwise noted)

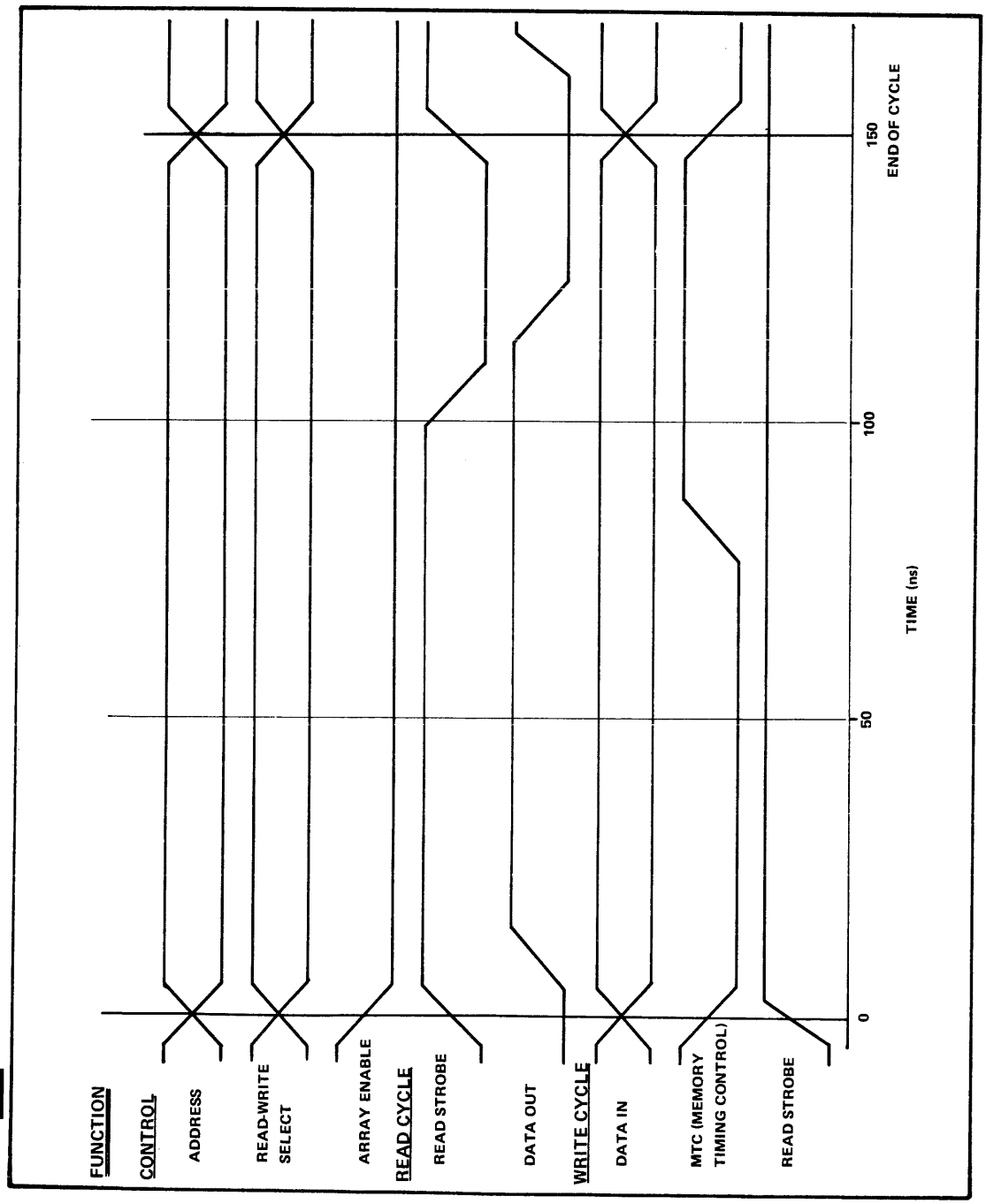
PARAMETERS	TEST CONDITIONS†		MIN	TYP*	MAX	UNITS
Inputs						
I_{IH} (All inputs except R/W and Array Selects)	V_{IH} = 2.4 V,	$V_{CC}+$ = MAX			40	μA
I_{IL} (All inputs except R/W and Array Selects)	V_{IL} = 0.4 V,	$V_{CC}+$ = MAX			−1.6	mA
V_{IH} (All inputs except R/W and Array Selects)		$V_{CC}+$ = MIN	2.0			V
V_{IL} (All inputs except R/W and Array Selects)		$V_{CC}+$ = MIN			0.8	V
Inputs						
I_{IH} (R/W and Array Select inputs only)	V_{IH} = 2.4 V,	$V_{CC}+$ = MAX			80	μA
I_{IL} (R/W and Array Select inputs only)	V_{IL} = 0.4 V,	$V_{CC}+$ = MAX			−3.2	mA
V_{IH} (R/W and Array Select inputs only)		$V_{CC}+$ = MIN	2.0			V
V_{IL} (R/W and Array Select inputs only)		$V_{CC}+$ = MIN			0.8	V
Outputs						
V_{OH}	Open Collector					
V_{OL}	I_{sink} = 16 mA,	$V_{CC}-$ = MIN, $V_{CC}+$ = MIN			0.4	V
I_{OH}	V_{OH} = 5.25 V,	$V_{CC}-$ = MIN, $V_{CC}+$ = MIN			250	μA
Supply Currents						
$I_{CC}+$ (Includes I_{SS})				248		
$I_{CC}-$				20		
Power Dissipation						
Total				1340		mW
Per Bit				0.65		mW
Dynamic Characteristics (See Timing Diagram)						
Read Access				125		ns
50% input address line change to 50% data output with read strobe LOW and R/W signal HIGH	R_{OUT} = 330 Ω ± 5% C_{OUT} = 30 pF					
Write Cycle				150		ns
50% input address line change to start of next cycle						

* All typical values are at $V_{CC}+ = V_{SS} = -V_{CC}- = +5$ V and $T_A = 25°C$.

† $V_{CC}+ = V_{CC_1} = V_{CC_2}$

14

timing diagram



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

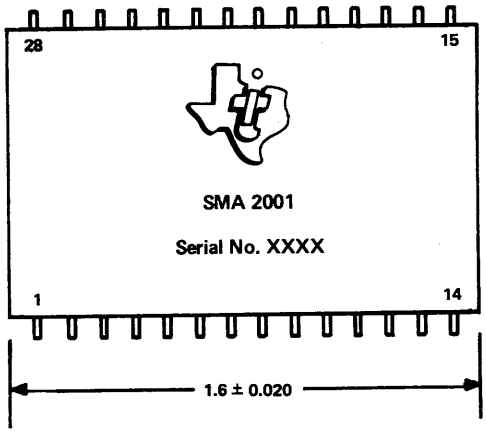
mechanical data

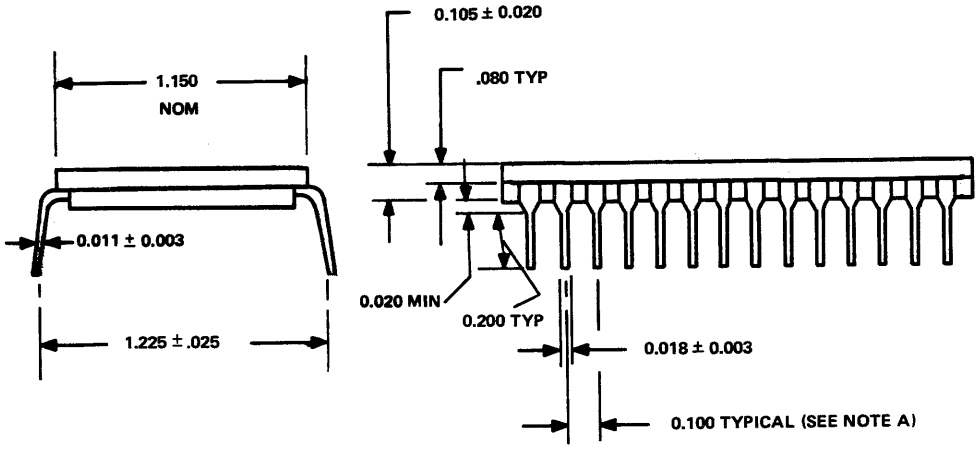
This semiconductor memory array consists of individual beam leaded MOS memory and bipolar interface chips thermocompression bonded to a multilevel interconnect system and contained in an epoxy sealed ceramic package.

The package has a dual-in-line configuration with 28 leads on 100 mil centers. This package is intended for insertion in mounting-hole rows on 1.200 inch centers.

pin configuration

1. GND	15. GND
2. A_{10}	16. NC
3. A_9	17. AS4–ARRAY SEL
4. A_8	18. AS3–ARRAY SEL
5. DATA IN 1	19. A_0
6. MTC–TIMING CONTROL	20. A_1
7. READ STROBE	21. A_2
8. OUTPUT 1 } See Note 9 Page 2	22. A_3
9. OUTPUT 2 }	23. AS2–ARRAY SEL
10. R/W–READ/WRITE	24. AS1–ARRAY SEL
11. $-V_{CC}$	25. A_4
12. V_{CC_2}	26. A_5
13. V_{CC_1}	27. A_6
14. V_{SS}	28. A_7





NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ± 0.010 of its true longitudinal position relative to pins (1) and (28).

B. All dimensions in inches.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

2048-BIT
HIGH PERFORMANCE SEMICONDUCTOR RAM ARRAY

description

This specification defines a 2048-bit memory array to be used as a building block for organizing larger memory systems. The memory array is a multi-chip array made up of beam leaded MOS storage chips and beam leaded bipolar decoding, sense, write and control chips. This total array is packaged in a ceramic dual-in-line 28 pin package for the commercial temperature range (0 – 70°C).

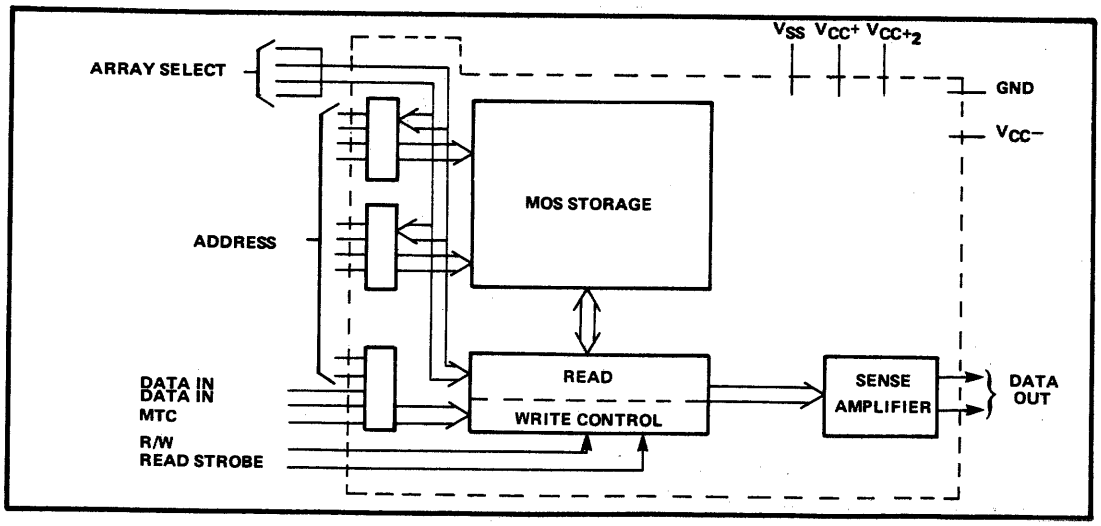
features

- Fast read access time . . . . . 125 ns typical
- Fast write time . . . . . 125 ns typical
- Fast cycle time . . . . . 150 ns typical
- Low memory power dissipation . . . . . 0.65 mW/bit typical
- Open collector output for OR tie
- Directly compatible with DTL and TTL logic circuits
- Easy memory expansion through 4 chip select inputs
- Read strobe control
- Standard TTL loading
- +5 V, GND, –5 V operation
- DIP packaging

organization

The memory array is organized as a 1K x 2 fully decoded memory.

block diagram



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operation

Read Mode – Binary levels are applied to address lines (TTL levels) and data appears at output at access time (125 ns) when READ STROBE is LOW and R/W is HIGH in the READ MODE.

Write Mode – Binary levels are applied to address lines (TTL levels). Data is present at DATA IN. R/W is LOW for the WRITE mode. READ STROBE is HIGH. MTC is LOW until indicated time in WRITE cycle.

Array Select – All four array selects must be LOW to have array selected. When array is not selected, array output is HIGH and data cannot be written into the array.

Timing – Waveform timing is shown on attached timing diagram.

absolute maximum ratings (over operating temperature range unless otherwise noted)†

V_{SS} (See Note 7)	7 V
$V_{CC}+$ (See Note 7)	7 V
$V_{CC}-$ (See Note 7)	–7 V
Input voltage (See Note 8)	5.5 V
Operating Ambient Temperature with 700 FPM of air flow	0 to 70°C
Storage temperature range	–65 to 150°C
Output sink current	20 mA

† Maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.

recommended operating conditions

	MIN	NOM	MAX
V_{SS}	4.75	5.0	5.25
$V_{CC}+$	4.75	5.0	5.25
$V_{CC}-$	–4.75	–5.0	–5.25
Output sink current			16 mA
Operating Ambient Temperature with 700 FPM of air flow	0°C		70°C

NOTES:
1. All array selects must be LOW for array to be selected.
2. Unselected array data out at HIGH level.
3. Read strobe should be LOW for data out only during read cycle.
4. HIGH data in gives HIGH data out.
5. R/W is HIGH for read, LOW for write.
6. MTC must be LOW at all times except at end of write cycle.
7. With respect to network ground terminal.
8. Input signals must be zero or positive with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics (over ambient temperature range unless otherwise noted)

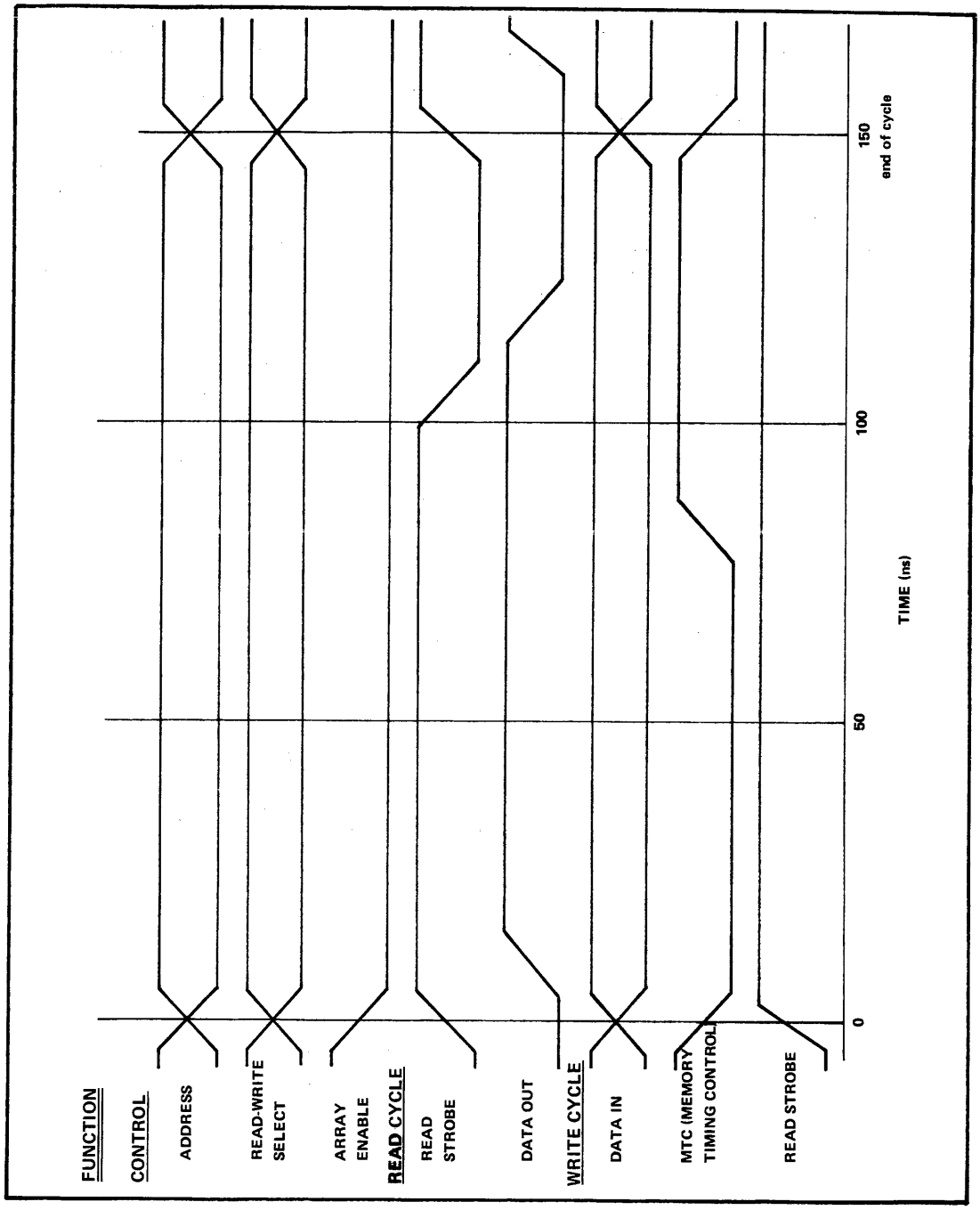
PARAMETER		TEST CONDITIONS†		MIN	TYP*	MAX	UNITS
Inputs							
I_{IH}	All inputs	V_{IH} = 2.4 V,	$V_{CC}+$ = MAX			40	μA
I_{IL}	except	V_{IL} = 0.4 V,	$V_{CC}+$ = MAX			−1.6	mA
V_{IH}	R/W and		$V_{CC}+$ = MIN	2.0			V
V_{IL}	Array Selects		$V_{CC}+$ = MIN			0.8	V
Inputs							
I_{IH}	R/W and	V_{IH} = 2.4 V,	$V_{CC}+$ = MAX			80	μA
I_{IL}	Array Select	V_{IL} = 0.4 V,	$V_{CC}+$ = MAX			−3.2	mA
V_{IH}	inputs		$V_{CC}+$ = MIN	2.0			V
V_{IL}	only		$V_{CC}+$ = MIN			0.8	V
Outputs							
V_{OH}		Open Collector					
V_{OL}		I_{sink} = 16 mA,	$V_{CC}-$ = MIN, $V_{CC}+$ = MIN			0.4	V
I_{OH}		V_{OH} = 5.25 V,	$V_{CC}-$ = MIN, $V_{CC}+$ = MIN			250	μA
Supply Currents							
$I_{CC}+$ (Includes I_{SS})					248		
$I_{CC}-$					20		
Power Dissipation							
Total					1340		mW
Per Bit					0.65		mW
Dynamic Characteristics (See Timing Diagram)							
Read Access		R_{OUT} = 330 Ω ± 5%			125		ns
	50% input address line change to 50% data output with read strobe LOW and R/W signal HIGH	C_{OUT} = 30 pF					
Write Cycle							
	50% input address line change to start of next cycle				150		ns

* All typical values are at $V_{CC}+ = V_{SS} = -V_{CC}- = +5$ V and $T_A = 25°C$.

† $V_{CC}+ = V_{CC_1} = V_{CC_2}$

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

timing diagram



14

SMA 2002
2048-BIT SEMICONDUCTOR MEMORY ARRAY

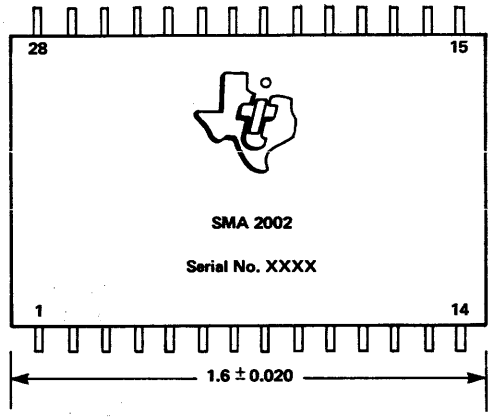
mechanical data

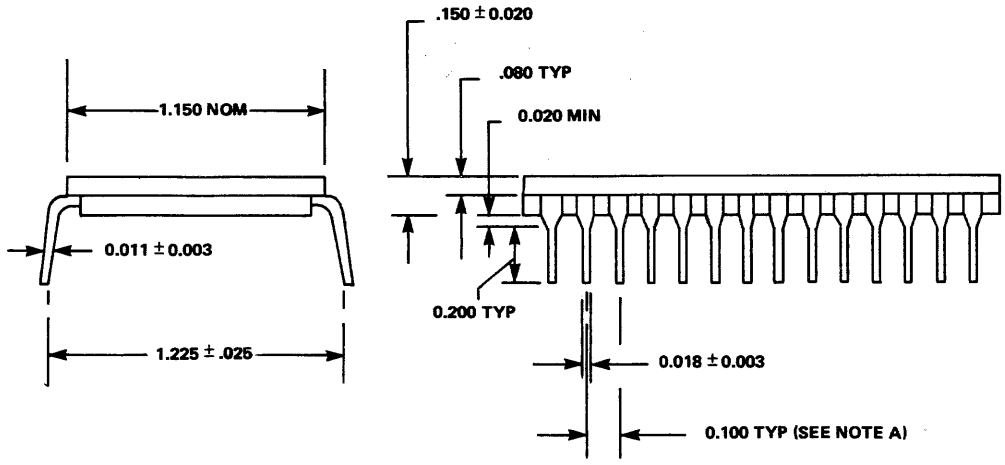
This semiconductor memory array consists of individual beam leaded MOS memory and bipolar interface chips thermo-compression bonded to a multilevel interconnect system and contained in an epoxy sealed ceramic package.

The package has a dual-in-line lead configuration with 28 leads on 100 mil centers. This package is intended for insertion in mounting-hole rows on 1.200 inch centers.

pin configuration

1. GND	15. GND
2. DATA IN 2	16. NC
3. A_9	17. AS4—ARRAY SEL
4. A_8	18. AS3—ARRAY SEL
5. DATA IN 1	19. A_0
6. MTC—TIMING CONTROL	20. A_1
7. READ STROBE	21. A_2
8. OUTPUT 1	22. A_3
9. OUTPUT 2	23. AS2—ARRAY SEL
10. R/W—READ/WRITE	24. AS1—ARRAY SEL
11. $-V_{CC}$	25. A_4
12. V_{CC_2}	26. A_5
13. V_{CC_1}	27. A_6
14. V_{SS}	28. A_7





NOTES: A. The true position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (1) and (28).

B. All dimensions in inches.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Hybrid Integrated Circuits

HYBRID INTEGRATED CIRCUITS

Texas Instruments is pleased to present the following technical data for your use in evaluating and specifying hybrid integrated circuits. These data sheets describe standard hybrid integrated circuits that are now available. Additional standard circuits are planned for early release.

In addition to these standard components, Texas Instruments offers a total capability for design, fabrication and testing of custom circuits to meet your special needs.

Texas Instruments has been engaged in the development and application of hybrid integrated circuit techniques, both thick-film and thin-film, for more than ten years. These techniques include various methods for thin-film metal deposition, thick-film printing and screening, photo-etching, component and chip attachment, film resistor and capacitor fabrication, special packaging and beam-lead component attachment.

A wide range of materials are available for thin film circuit applications. These include gold, aluminum, nichrome, tantalum, tantalum nitride and cermets. Substrate materials include ceramic, glass and silicon.

Reliability is given major consideration at Texas Instruments and each hybrid circuit is subjected to pre-cap visual inspection, stabilization bake, temperature cycle, centrifuge, fine and gross leak and functional electrical tests. Additional testing is performed if required by customer specifications.

Electrical testing is performed using a computer-controlled, automatic test system capable of testing up to 40 active pins. Functional, dynamic and d-c tests can be performed with data logged by teletype or on magnetic tape. The test head provides space for special interface circuitry necessary to test a specific hybrid and permits testing at various temperature extremes.

A competent engineering staff, with both prototype and production fabrication facilities available, will assist you in satisfying your hybrid integrated circuit needs.

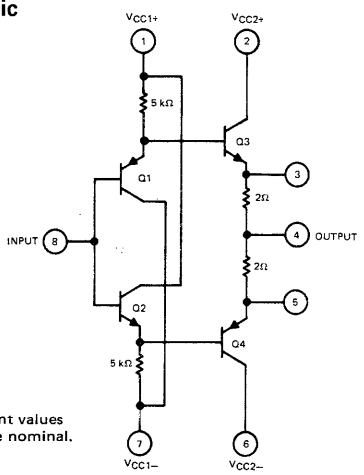
HYBRID MICROCIRCUIT

TYPE HIC037 CURRENT AMPLIFIER

JANUARY 1971

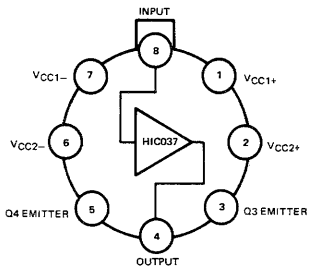
- High Input Impedance—200 kΩ
- Low Output Impedance—6 Ω
- High Power Efficiency
- High Output Voltage Swing
- Operation from ±5 V to ±20 V Supply
- Low Harmonic Distortion
- D-C to 30 MHz Bandwidth

schematic



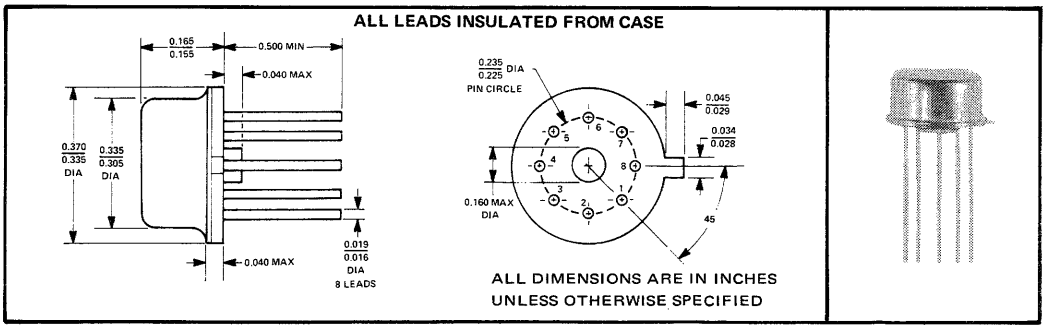
Component values shown are nominal.

pin assignments



BOTTOM VIEW

mechanical data



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltages V_{CC1+} and V_{CC2+} (See Note 1)	22 V
Supply voltages V_{CC1-} and V_{CC2-} (See Note 1)	−22 V
Input voltage (See Note 1)	$\leq V_{CC1}$
Steady-state output current	±100 mA
Pulsed output current (50 ms on, 1 sec off)	±400 mA
Continuous power dissipation at (or below) 25°C free-air temperature (See Note 2)	600 mW
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C

NOTES: 1. All voltage values are with respect to the common zero-reference level of the supply voltages (ground).
2. Derate linearly to 125°C free-air temperature at the rate of 6 mW/°C.

15

PRELIMINARY DATA SHEET: Supplementary data will be published at a later date.

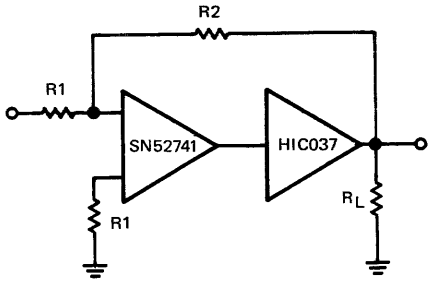
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics (see note 3)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
A_V	Large-signal voltage amplification	R_S = 10 kΩ, V_I = 3 V pp, T_A = −55°C to 125°C	R_L = 1 kΩ, f = 1 kHz,	0.95	0.97		
z_i	Input impedance	R_S = 200 kΩ, f = 1 kHz,	V_i = 1 V rms, R_L = 1 kΩ	180	200		kΩ
z_o	Output impedance	V_i = 1 V rms, R_L = 50 Ω,	f = 1 kHz, R_S = 10 kΩ		6	10	Ω
V_{OPP}	Maximum output voltage swing	R_L = 1 kΩ,	f = 1 kHz	±10	±11		V
V_{IO}	Input offset voltage	R_S = 10 kΩ, T_A = −55°C to 125°C	R_L = 1 kΩ,		±40	±100	mV
I_{IO}	Input offset current	R_S = 10 kΩ, T_A = −55°C to 125°C	R_L = 1 kΩ,		±6	±10	μA
THD	Total harmonic distortion	V_i = 5 V rms,	f = 1 kHz		0.1		%
BW	Bandwidth (3 dB)	V_i = 1 V rms, f = 1 MHz	R_L = 50 Ω,	30	50		MHz
I_{CC+}	Positive supply current	R_S = 10 kΩ,	R_L = 1 kΩ		6	10	mA
I_{CC-}	Negative supply current	R_S = 10 kΩ,	R_L = 1 kΩ		−6	−10	mA

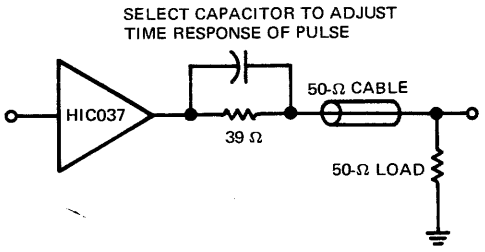
NOTE 3: Specification applies for T_A = 25°C with +12 V on Pins 1 and 2; −12 V on Pins 6 and 7, unless otherwise specified.
†All typical values are at T_A = 25°C.

TYPICAL APPLICATION DATA



SUPPLY = ±5 V to ±15 V

HIGH-CURRENT OPERATIONAL AMPLIFIER



LINE DRIVER

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

HYBRID MICROCIRCUIT

TYPE HIC106
POSITIVE VOLTAGE REGULATOR

JANUARY 1971

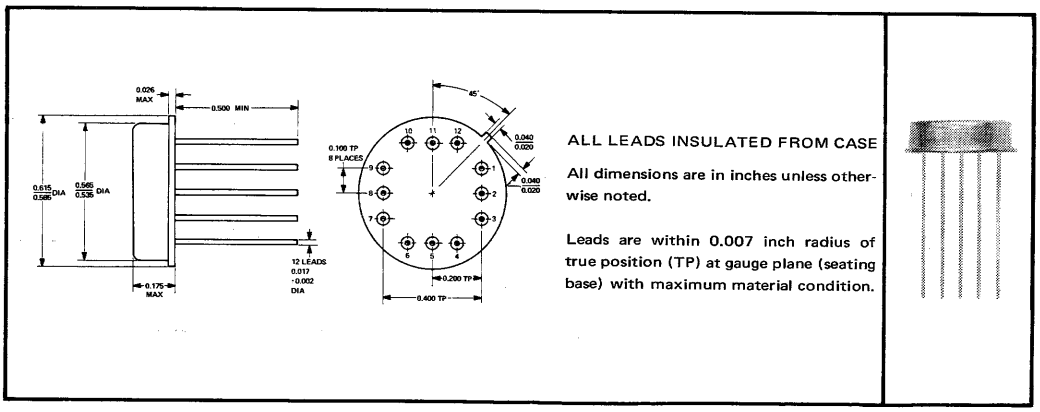
- Output current to 1 ampere without external pass transistor
- No external compensation required
- Output voltage adjustable from 2 to 37.5 volts
- Optional output with internal current limiting
- Series or shunt operation

description

The HIC106 is a hybrid voltage regulator featuring internal compensation, an optional output with internal current limiting, and regulated output currents up to 1 ampere. The HIC106 regulator requires only one external component during normal operation.

Applications include logic card regulators, sub-system and system regulators, instrument power supplies and other power supplies for linear and digital circuits.

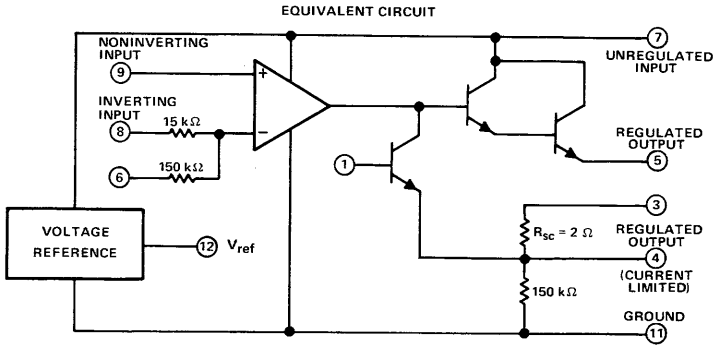
mechanical data



pin connections (see equivalent circuit)

Pin 1 = Base of Limit Transistor
Pin 2 = NC
Pin 3 = Limit Resistor
Pin 4 = Output (Current Limited)
Pin 5 = Output
Pin 6 = Feedback Resistor
Pin 7 = Unregulated Input
Pin 8 = Inverting Input
Pin 9 = Noninverting Input
Pin 10 = NC
Pin 11 = Ground
Pin 12 = V_{ref}

EQUIVALENT CIRCUIT



15

71

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TYPE HIC106
POSITIVE VOLTAGE REGULATOR

absolute maximum ratings

Input Voltage (See Note 1)	40 V
Input-Output Voltage Differential	40 V
Maximum Output Current	1 A
Internal Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	2.7 W
Internal Power Dissipation at (or below) 25°C Case Temperature (See Note 3)	5.0 W
Operating Temperature Range	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. All voltages, unless otherwise noted, are with respect to device ground terminal.
2. Derate linearly above 25°C free-air temperature at the rate of 15.4 mW/°C.
3. Derate linearly above 25°C case temperature at the rate of 28.5 mW/°C.

electrical characteristics, see note 4

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Voltage Range			9.5		40	V
Output Voltage Range			2		37.5	V
Input-Output Voltage Differential			2.5		40	V
Load Regulation $\frac{\Delta V_O}{V_O \text{ at } I_O = 1\text{ mA}} \times 100\%$	I_O = 1 mA to 300 mA, V_I = 40 V,	V_O = 35 V			0.2	%
Line Regulation $\frac{\Delta V_O}{\Delta V_I} \times 100\%$	V_I = 40 V to 20 V, V_O = 15 V				0.15	%
Ripple Rejection	C_{ref} = 0†,	f = 120 Hz		74		dB
	C_{ref} = 5 μF†,	f = 120 Hz		86		
Temperature Coefficient $\pm\left[\frac{V_O \text{ at } 125°C - V_O \text{ at } -55°C}{V_O \text{ at } 25°C}\right] \frac{100\%}{180°C}$	T_A = −55°C to 125°C, V_O = 25 V,	I_O = 1 mA			±0.02	%/°C
Standby Current Drain	I_O = 0			4.3	6	mA
Short-Circuit Current Limit, I_{OS}	V_I = 9.5 V,	V_O = 0		350		mA
Reference Voltage, V_{ref}			6.3	6.8	7.3	V

†C_{ref} is connected between pin 12 and ground.

NOTE 4: Unless otherwise specified, T_A = 25°C, V_I = 30 V, V_O = 15 V, I_O = 15 mA. V_I is the unregulated input voltage, V_O is the regulated output voltage, and I_O is the output current.

TYPICAL CHARACTERISTICS

MAXIMUM LOAD CURRENT
AS A FUNCTION OF INPUT-OUTPUT
VOLTAGE DIFFERENTIAL

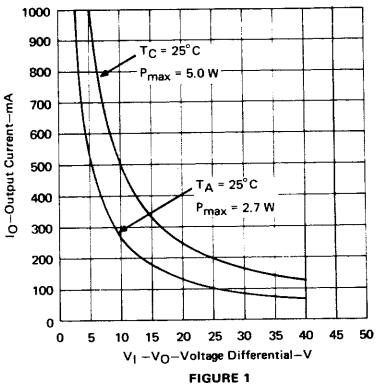
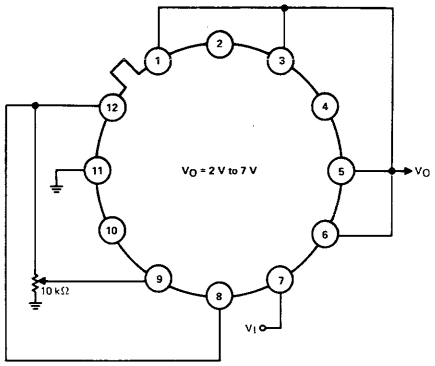


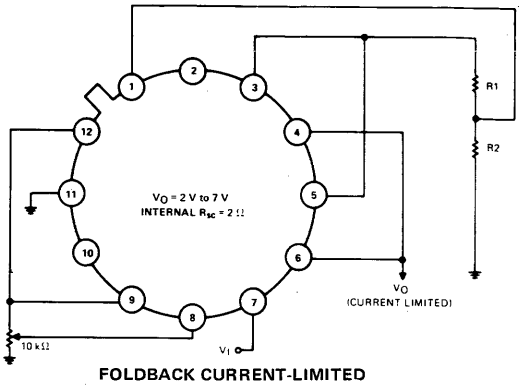
FIGURE 1

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

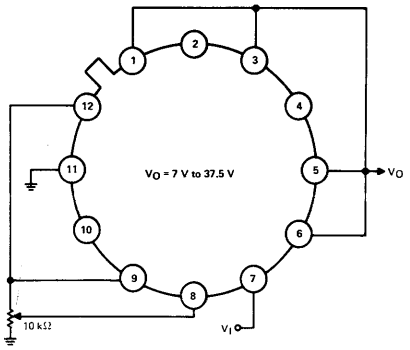
TYPICAL APPLICATION DATA



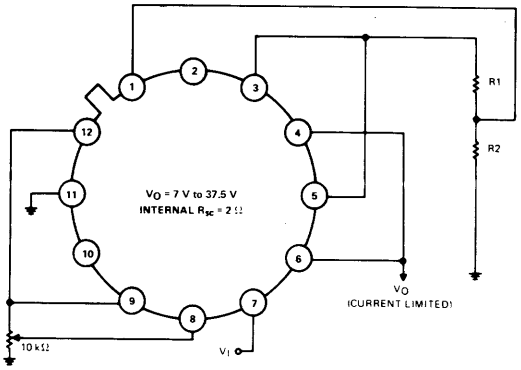
LOW-VOLTAGE REGULATOR
FIGURE 2



FOLDBACK CURRENT-LIMITED
LOW-VOLTAGE REGULATOR
FIGURE 3



HIGH-VOLTAGE REGULATOR
FIGURE 4



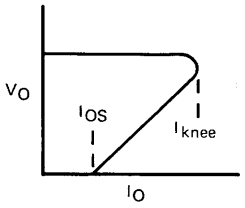
FOLDBACK CURRENT-LIMITED
HIGH-VOLTAGE REGULATOR
FIGURE 5

FOLDBACK CURRENT LIMITING

$$I_{OS} = \frac{(V_{1,4})\ (R1 + R2)}{R_{SC}\ (R2)}$$

$$I_{knee} = \frac{V_O\ R1}{R_{SC}\ R2} + I_{OS}$$

$V_{1,4}$ (voltage between pins 1 and 4) is typically 0.6 V



BOTTOM VIEWS SHOWN

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

HYBRID MICROCIRCUIT

TYPE HIC107
NEGATIVE VOLTAGE REGULATOR

JANUARY 1971

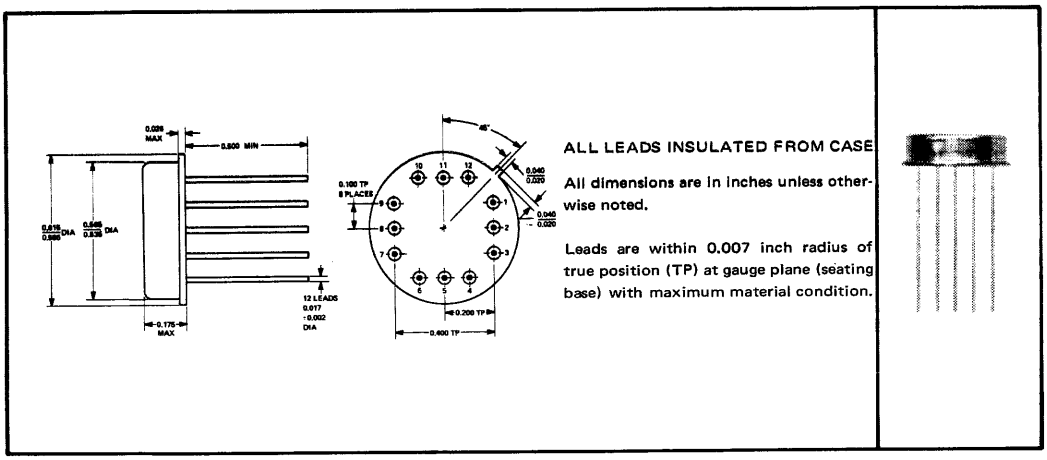
- Output current to 1 ampere without external pass transistor
- No external compensation required
- Output voltage adjustable from −2 to −37 volts
- Optional output with internal current limiting
- Series or shunt operation

description

The HIC107 is a hybrid voltage regulator featuring internal compensation, an optional output with internal current limiting, and regulated output currents up to 1 ampere. The HIC107 regulator requires only one external component during normal operation.

Applications include logic card regulators, sub-system and system regulators, instrument power supplies and other power supplies for linear and digital circuits.

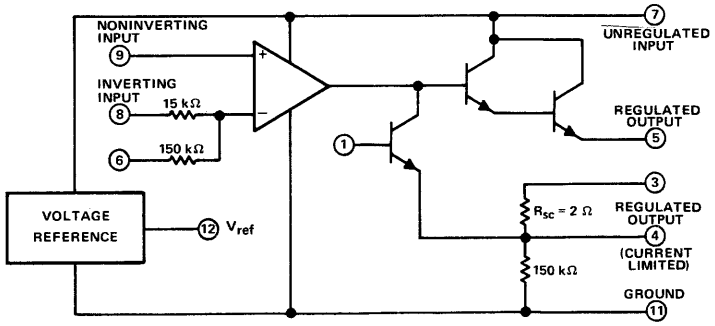
mechanical data



pin connections (see equivalent circuit)

Pin 1 = Base of Limit Transistor
Pin 2 = NC
Pin 3 = Limit Resistor
Pin 4 = Output (Current Limited)
Pin 5 = Output
Pin 6 = Feedback Resistor
Pin 7 = Unregulated Input
Pin 8 = Inverting Input
Pin 9 = Noninverting Input
Pin 10 = NC
Pin 11 = Ground
Pin 12 = V_{ref}

EQUIVALENT CIRCUIT



15

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings

Input Voltage (See Note 1)	−40 V
Input-Output Voltage Differential	−40 V
Maximum Output Current	−1 A
Internal Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	2.7 W
Internal Power Dissipation at (or below) 25°C Case Temperature (See Note 3)	5.0 W
Operating Temperature Range	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. All voltages, unless otherwise noted, are with respect to device ground terminal.
2. Derate linearly above 25°C free-air temperature at the rate of 15.4 mW/°C.
3. Derate linearly above 25°C case temperature at the rate of 28.5 mW/°C.

electrical characteristics, see note 4

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		−9.5		−40	V
Output Voltage Range		−2		−37	V
Input-Output Voltage Differential		−3		−40	V
Load Regulation $\frac{\Delta V_O}{V_O \text{ at } I_O = 1\text{ mA}}$ X 100%	I_O = 1 mA to 300 mA, $-V_I$ = −40 V, V_O = −35 V			0.2	%
Line Regulation $\frac{\Delta V_O}{\Delta V_I}$ X 100%	$-V_I$ = −40 V to −20 V, V_O = −15 V			0.15	%
Ripple Rejection	C_{ref} = 0†, f = 120 Hz		74		dB
	C_{ref} = 5 μF†, f = 120 Hz		86		
Temperature Coefficient $\pm\left[\frac{V_O \text{ at } 125°C - V_O \text{ at } -55°C}{V_O \text{ at } 25°C}\right]\frac{100\%}{180°C}$	T_A = −55°C to 125°C, V_O = −25 V, I_O = −1 mA			±0.02	%/°C
Standby Current Drain	I_O = 0		−4.3	−6	mA
Short-Circuit Current Limit, I_{OS}	$-V_I$ = −9.5 V, V_O = 0		−350		mA
Reference Voltage, V_{ref}		−6.3	−6.8	−7.3	V

†C_{ref} is connected between pin 12 and ground.
NOTE 4: Unless otherwise specified, T_A = 25°C, V_I = −30 V, V_O = −15 V, I_O = −15 mA. V_I is the unregulated input voltage, V_O is the regulated output voltage, and I_O is the output current.

TYPICAL CHARACTERISTICS

MAXIMUM LOAD CURRENT
AS A FUNCTION OF INPUT-OUTPUT
VOLTAGE DIFFERENTIAL

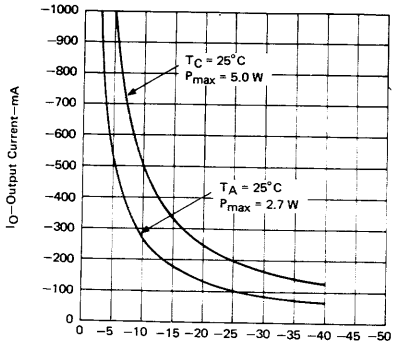
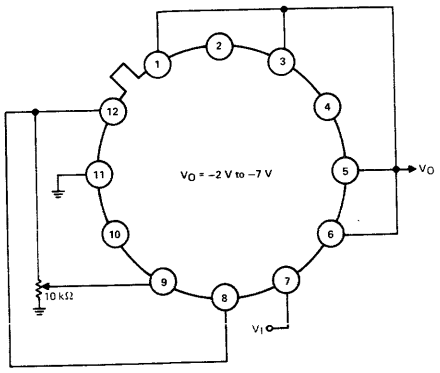


FIGURE 1

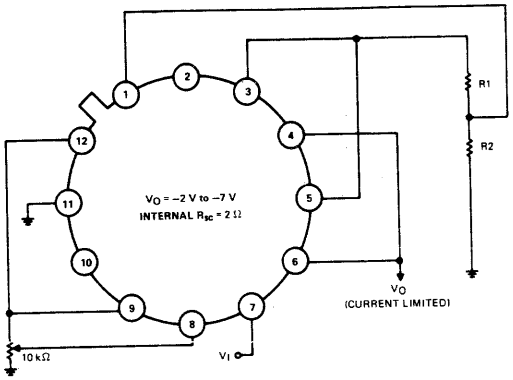
15

TYPE HIC107
NEGATIVE VOLTAGE REGULATOR

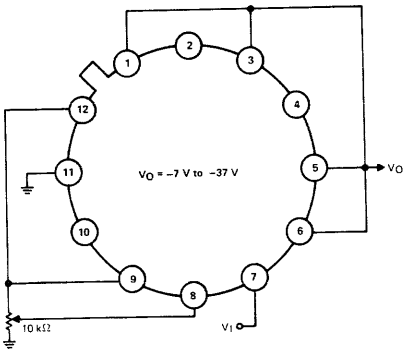
TYPICAL APPLICATION DATA



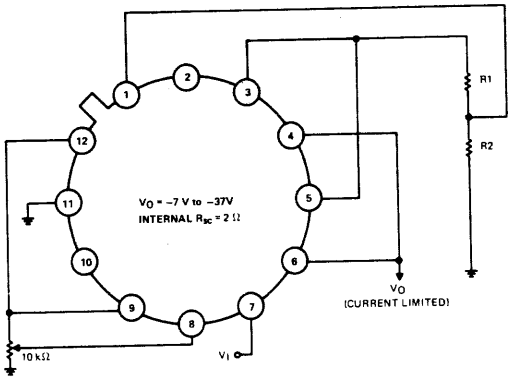
LOW-VOLTAGE REGULATOR
FIGURE 2



FOLDBACK CURRENT-LIMITED
LOW-VOLTAGE REGULATOR
FIGURE 3



HIGH-VOLTAGE REGULATOR
FIGURE 4



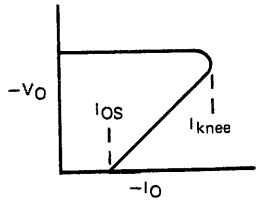
FOLDBACK CURRENT-LIMITED
HIGH-VOLTAGE REGULATOR
FIGURE 5

FOLDBACK CURRENT LIMITING

$$I_{OS} = \frac{(V_{1,4})\ (R1 + R2)}{R_{SC}\ (R2)}$$

$$I_{knee} = \frac{V_O\ R1}{R_{SC}\ R2} + I_{OS}$$

$V_{1,4}$ (voltage between pins 1 and 4) is typically −0,6 V



15

BOTTOM VIEWS SHOWN

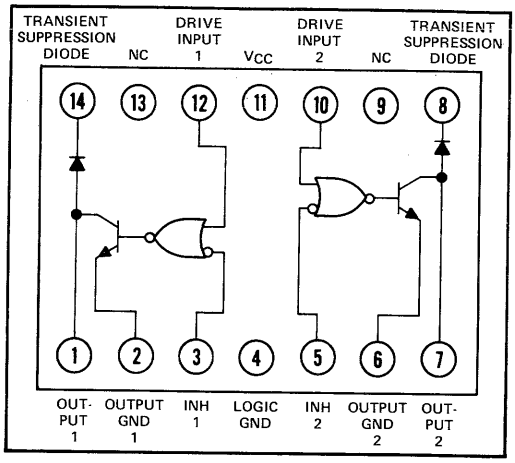
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE TIH101
DUAL POWER LOGIC MODULE

CIRCUIT TYPE TIH101
BULLETIN NO. DL-S 7111431, JANUARY 1971

- Low Power Dissipation
- Two Power Logic Functions per Package
- Inputs Compatible with Most TTL and DTL Families
- Pin Spacing Same as Standard 14-Pin Dual-In-Line Package

terminal assignments (top view)



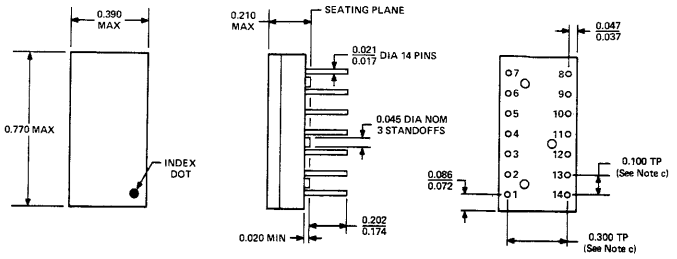
NC—No internal connection

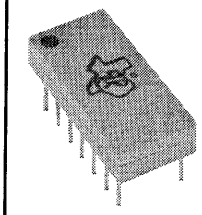
description

The TIH101 is a hybrid circuit designed for applications where the drive requirements exceed the capabilities of standard logic gates. The device contains two electrically independent circuits, each having both drive and inhibit inputs for greater design flexibility. The inputs are compatible with most TTL and DTL families. Each output is capable of sinking up to 6.5 amperes at a 5% duty cycle and pulse widths up to 1.25 milliseconds. A transient suppression diode is included for driving inductive loads. These devices are commonly used as hammer drivers in high-speed printers.

mechanical data

The circuit is mounted on a ceramic substrate enclosed in a glass and ceramic dual-in-line package. The package is intended for mounting-hole rows on 0.300-inch centers.





NOTES: a. All dimensions are in inches.
b. Terminal identification is provided by the index dot on the top of the package.
c. Leads are within 0.005 radius of true position (TP) at maximum material condition.

15

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE TIH101
DUAL POWER LOGIC MODULE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Applied output voltage (see Note 1)	60 V
Continuous output current: one output operating	0.75 A
both outputs operating	0.5 A
Peak output current ($t_w \leqslant 1.25$ ms, duty cycle = 5%): one output operating	6.5 A
both outputs operating	6.5 A
Voltage between logic ground and output ground	±1 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE 1: Supply (V_{CC}) and input voltages are with respect to the logic ground terminal; output voltage is with respect to the output ground terminal for that particular circuit.

electrical characteristics over operating free-air temperature range, V_{CC} = 4.75 V to 5.25 V

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
$V_{O(on)}$	On-state output voltage	$I_{O(on)}$ = 6 A, See Notes 2 and 3			1.6	V
$I_{O(off)}$	Off-state output current	$V_{O(off)}$ = 60 V			10	μA
I_I	Input current at maximum input voltage	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_I = 0.4 V			−1.6	mA
$I_{CC(off)}$	Off-state supply current	See Note 4		8	15	mA
$I_{CC(on)}$	On-state supply current (one circuit on)	See Note 5		110	175	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

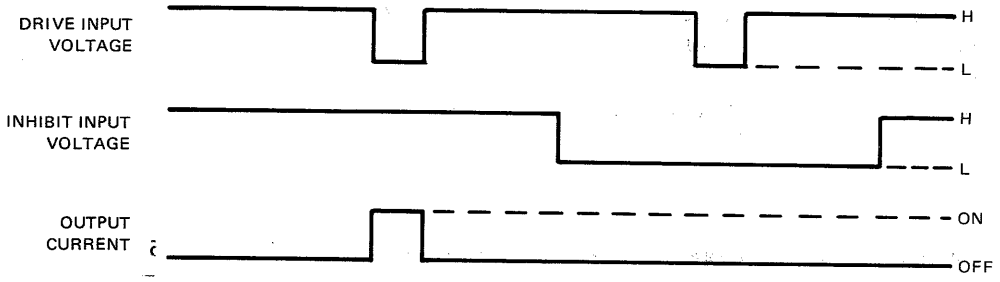
electrical characteristics of transient suppression diode over operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_R	Static reverse current	V_R = 60 V			100	μA
V_F	Static forward voltage	I_F = 6 A, See Notes 2 and 3			2	V

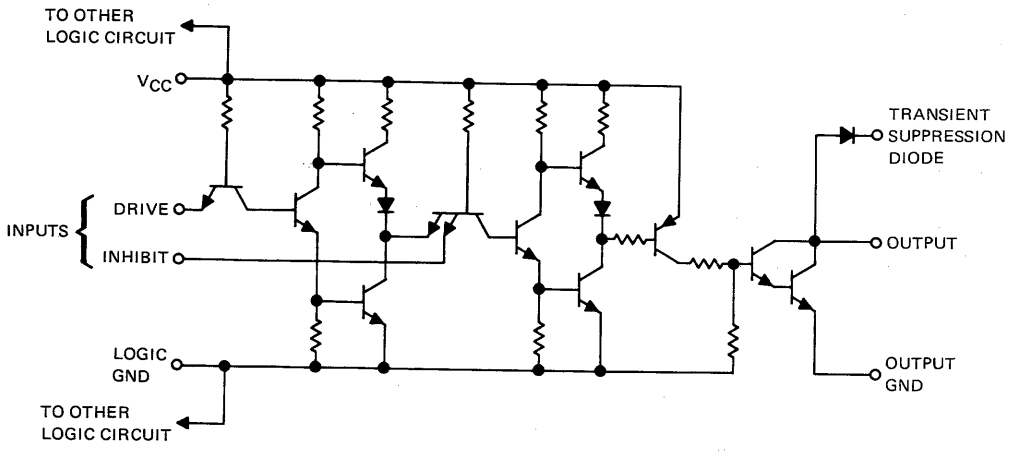
NOTES: 2. This parameter must be measured using pulse techniques. t_w = 300 μs, duty cycle ⩽ 2%.
3. This parameter is measured with voltage-sensing contacts separate from the current-carrying contacts.
4. $I_{CC(off)}$ is measured with the drive inputs at 4.5 V and the inhibit inputs grounded.
5. $I_{CC(on)}$ is measured by applying 4.5 V to the inhibit input of one circuit and the drive input of the other circuit with the remaining inputs grounded, then likewise for the other circuit.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

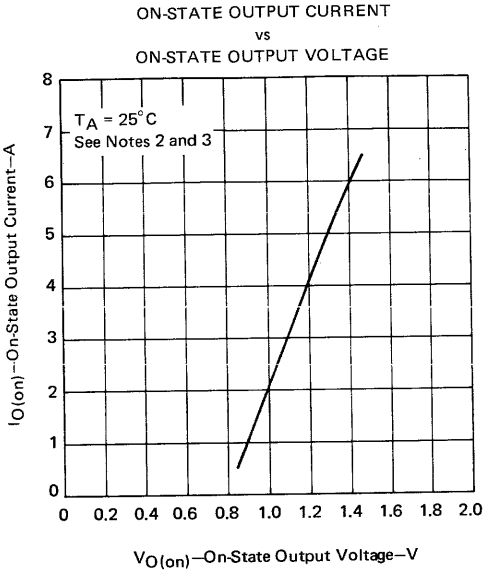
input voltage and output current relationships



schematic (each circuit)

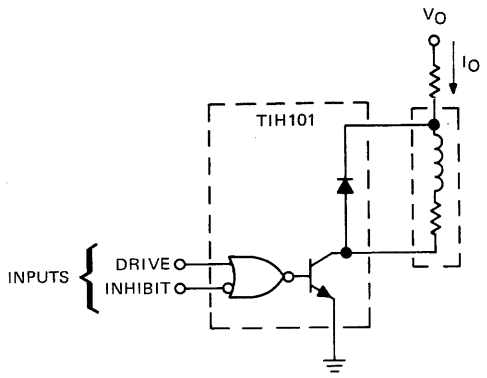


TYPICAL CHARACTERISTICS



NOTES: 2. This parameter must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.
3. This parameter is measured with voltage-sensing contacts separate from the current-carrying contacts.

TYPICAL APPLICATION DATA



SOLENOID DRIVER

15

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222